3 V/5 V, ±10 V Input Range, 1 mW 3-Channel 16-Bit, Sigma-Delta ADC

AD7707

FEATURES

Charge balancing ADC
- **16 bits, no missing codes**
- **±0.003% nonlinearity**

High level (±10 V) and low level (±10 mV) input channels
True bipolar ±100 mV capability on low level input
- **Channels without requiring charge pumps**

Programmable gain front end
- **Gains from 1 to 128**

3-wire serial interface
- **SPI, QSPI™, MICROWIRE™ and DSP compatible**
- **Schmitt trigger input on SCLK**

Ability to buffer the analog input
2.7 V to 3.3 V or 4.75 V to 5.25 V operation
Power dissipation 1 mW at 3 V
Standby current 8 µA maximum
20-lead SOIC and TSSOP packages

GENERAL DESCRIPTION

The AD7707 is a complete analog front end for low frequency measurement applications. This 3-channel device can accept either low level input signals directly from a transducer or high level (±10 V) signals and produce a serial digital output. It employs a Σ-Δ conversion technique to realize up to 16 bits of no missing codes performance. The selected input signal is applied to a proprietary programmable gain front end based around an analog modulator. The modulator output is processed by an on-chip digital filter. The first notch of this digital filter can be programmed via an on-chip control register allowing adjustment of the filter cutoff and output update rate.

The AD7707 operates from a single 2.7 V to 3.3 V or 4.75 V to 5.25 V supply. The AD7707 features two low level pseudo differential analog input channels, one high level input channel and a differential reference input. Input signal ranges of 0 mV to 20 mV through 0 V to 2.5 V can be accommodated on both low level input channels when operating with a VDD of 5 V and a reference of 2.5 V. They can also handle bipolar input signal ranges of ±20 mV through ±2.5 V, which are referenced to the LCOM input. The AD7707, with a 3 V supply and a 1.225 V reference, can handle unipolar input signal ranges of 0 mV to 10 mV through 0 V to 1.225 V. Its bipolar input signal ranges are ±10 mV through ±1.225 V.

The high level input channel can accept input signal ranges of ±10 V, ±5 V, 0 V to 10 V and 0 V to 5 V. The AD7707 thus performs all signal conditioning and conversion for a 3-channel system.

The AD7707 is ideal for use in smart, microcontroller or DSP-based systems. It features a serial interface that can be configured for 3-wire operation. Gain settings, signal polarity and update rate selection can be configured in software using the input serial port. The part contains self-calibration and system calibration options to eliminate gain and offset errors on the part itself or in the system.

CMOS construction ensures very low power dissipation, and the power-down mode reduces the standby power consumption to 20 µW typical. This part is available in a 20-lead wide body (0.3 inch) small outline (SOIC) package and a low profile 20-lead TSSOP.

FUNCTIONAL BLOCK DIAGRAM

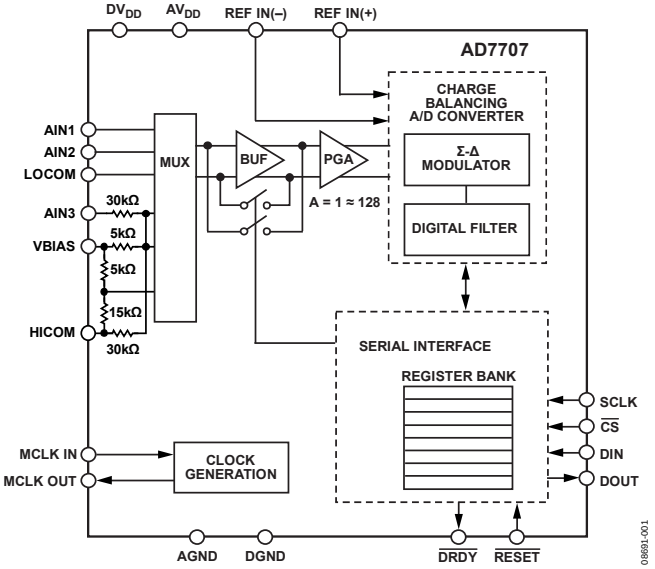

Figure 1.

PRODUCT HIGHLIGHTS

1. The AD7707 consumes less than 1 mW at 3 V supplies and 1 MHz master clock, making it ideal for use in low power systems. Standby current is less than 8 µA.
2. On-chip thin-film resistors allow ±10 V, ±5 V, 0 V to 10 V, and 0 V to 5 V high level input signals to be directly accommodated on the analog inputs without requiring split supplies or charge-pumps.
3. The low level input channels allow the AD7707 to accept input signals directly from a strain gage or transducer removing a considerable amount of signal conditioning.
4. The part features excellent static performance specifications with 16 bits, no missing codes, ±0.003% accuracy, and low rms noise. Endpoint errors and the effects of temperature drift are eliminated by on-chip calibration options, which remove zero-scale and full-scale errors.

Rev. B

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SPECIFICATIONS

AV_{DD} = DV_{DD} = 3 V or 5 V, REF IN(+) = 1.225 V with AV_{DD} = 3 V and 2.5 V with AV_{DD} = 5 V; REF IN(−) = GND; VBIAS = REFIN(+); MCLK IN = 2.4576 MHz unless otherwise noted. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	Unit	Conditions/Comments
STATIC PERFORMANCE			
Low Level Input Channels (AIN1 and AIN2)			
No Missing Codes	16	Bits min	Guaranteed by design; filter notch < 60 Hz
Output Noise	See Table 7 to Table 10		Depends on filter cutoffs and selected gain
Integral Nonlinearity[2]	±0.003	% of FSR max	Filter notch < 60 Hz; typically ±0.0003%
Unipolar Offset Error[3]			
Unipolar Offset Drift[4]	0.5	µV/°C typ	
Bipolar Zero Error[3]			
Bipolar Zero Drift[4]	0.5	µV/°C typ	For gains of 1, 2, and 4
	0.1	µV/°C typ	For gains of 8, 16, 32, 64, and 128
Positive Full-Scale Error[3, 5]			
Full-Scale Drift[4, 6]	0.5	µV/°C typ	
Gain Error[3, 7]			
Gain Drift[4, 8]	0.5	ppm of FSR/°C typ	
Bipolar Negative Full-Scale Error[2]	±0.003	% of FSR max	Typically ±0.0007%
Bipolar Negative Full-Scale Drift[4]	1	µV/°C typ	For gains of 1 to 4
	0.6	µV/°C typ	For gains of 8 to 128
HIGH LEVEL INPUT CHANNEL (AIN3)			
No Missing Codes	16	Bits min	Guaranteed by design; filter notch < 60 Hz
Output Noise	See Table 11 to Table 13		Depends on filter cutoffs and selected gain
Integral Nonlinearity[2]	±0.003	% of FSR max	Filter notch < 60 Hz; typically ±0.0003%
Unipolar Offset Error[9]	±10	mV max	Typically within ±1.5 mV
Unipolar Offset Drift	4	µV/°Ctyp	
Bipolar Zero Error[9]	±10	mV max	Typically within ±1.5 mV
Bipolar Zero Drift	4	µV/°C typ	For gains of 1, 2, and 4
	1	µV/°C typ	For gains of 8, 16, 32, 64, and 128
Gain Error	±0.2	% typ	Typically within ±0.05%
Gain Drift	0.5	ppm of FSR/°C typ	
Negative Full-Scale Error[2]	±0.0012	% of FSR typ	
LOW LEVEL ANALOG INPUTS/REFERENCE INPUTS			Specifications for AIN and REF IN, unless otherwise noted
Input Common-Mode Rejection (CMR)[2]			Low level input channels, AIN1 and AIN2
AV_{DD} = 5 V			
Gain = 1	100	dB typ	
Gain = 2	105	dB typ	
Gain = 4	110	dB typ	
Gain = 8 to 128	130	dB typ	
AV_{DD} = 3 V			
Gain = 1	105	dB typ	
Gain = 2	110	dB typ	
Gain = 4	120	dB typ	
Gain = 8 to 128	130	dB typ	
Normal-Mode 50 Hz Rejection[2]	98	dB typ	For filter notches of 10 Hz, 25 Hz, 50 Hz; ±0.02 × f_{NOTCH}
Normal-Mode 60 Hz Rejection[2]	98	dB typ	For filter notches of 10 Hz, 20 Hz, 60 Hz; ±0.02 × f_{NOTCH}
Common-Mode 50 Hz Rejection[2]	150	dB typ	For filter notches of 10 Hz, 25 Hz, 50 Hz; ±0.02 × f_{NOTCH}

Parameter	B Version[1]	Unit	Conditions/Comments
Common-Mode 60 Hz Rejection[2]	150	dB typ	For filter notches of 10 Hz, 20 Hz, 60 Hz, $\pm 0.02 \times f_{NOTCH}$
Absolute/Common-Mode REF IN Voltage[2]	AGND to AV_{DD}	V min to V max	
Absolute/Common-Mode AIN Voltage[2, 10]	AGND – 100 mV	V min	BUF bit of setup register = 0
	AV_{DD} + 30 mV	V max	
	AGND + 50 mV	V min	BUF bit of setup register = 1
	AV_{DD} − 1.5 V	V max	
AIN DC Input Current[2]	1	nA max	
AIN Sampling Capacitance[2]	10	pF max	BUF = 0
AIN Differential Voltage Range[11, 12]	0 to $+V_{REF}$/gain	V nom	Unipolar input range ($\overline{B}$/U bit of setup register = 1)
	$\pm V_{REF}$/gain	V nom	Bipolar input range ($\overline{B}$/U bit of setup register = 0)
AIN Input Sampling Rate, f_S	Gain × f_{CLKIN}/64	Hz nom	For gains of 1 to 4
	f_{CLKIN}/8		For gains of 8 to 128
Reference Input Range			
REF IN(+) − REF IN(−) Voltage	1/1.75	V min/max	AV_{DD} = 2.7 V to 3.3 V; V_{REF} = 1.225 V ± 1% for specified performance
REF IN(+) − REF IN(−) Voltage	1/3.5	V min/max	AV_{DD} = 4.75 V to 5.25 V; V_{REF} = 2.5 V ± 1% for specified performance
REF IN Input Sampling Rate, f_S	f_{CLKIN}/64		
±100 mV INPUT RANGE			Low level input channels, AIN1 and AIN2; gain = 16, unbuffered mode
INL[2]	±0.003	% of FSR max	Filter notch < 60 Hz
Input Common-Mode Rejection (CMR)[2]	80	dB typ	
Power Supply Rejection (PSR)[2]	90	dB typ	
HIGH LEVEL ANALOG INPUT CHANNEL (AIN3)			AIN3 is with respect to HICOM
AIN3 Voltage Range	+10	V max	
	−10	V min	
Normal Mode 50 Hz Rejection	78	dB typ	For filter notches of 10 Hz, 25 Hz, 50 Hz; $\pm 0.02 \times f_{NOTCH}$
Normal Mode 60 Hz Rejection	78	dB typ	For filter notches of 10 Hz, 20 Hz, 60 Hz; $\pm 0.02 \times f_{NOTCH}$
AIN3 Input Sampling Rate, f_S	Gain × f_{CLKIN}/64	Hz nom	For gains of 1 to 4
	f_{CLKIN}/8	Hz nom	For gains of 8 to 128
AIN3 Input Impedance[2]	27	kΩ min	Typically 30 kΩ ± 10%; typical resistor Tempco is −30 ppm/°C
AIN3 Sampling Capacitance[2]	10	pF max	
VBIAS Input Range	0 V/AV_{DD}	V min/max	Typically REFIN(+) = 2.5 V
LOGIC INPUTS			
Input Current			
All Inputs Except MCLK IN	±1	µA max	Typically ±20 nA
MCLK	±10	µA max	Typically ±2 m A
All Inputs Except SCLK and MCLK IN			
V_{INL}, Input Low Voltage	0.8	V max	DV_{DD} = 5 V
	0.4	V max	DV_{DD} = 3 V
V_{INH}, Input High Voltage	2.0	V max	DV_{DD} = 3 V and 5 V
SCLK Only (Schmitt Triggered Input)			DV_{DD} = 5 V nominal
V_{T+}	1.4/3	V min/V max	
V_{T-}	0.8/1.4	V min/V max	
$V_{T+} - V_{T-}$	0.4/0.8	V min/V max	
SCLK Only (Schmitt Triggered Input)			DV_{DD} = 3 V nominal
V_{T+}	1/2.5	V min/V max	
V_{T-}	0.4/1.1	V min/V max	
$V_{T+} - V_{T-}$	0.375/0.8	V min /V max	

Parameter	B Version[1]	Unit	Conditions/Comments
MCLK IN Only			DV_{DD} = 5 V nominal
V_{INL}, Input Low Voltage	0.8	V max	
V_{INH}, Input High Voltage	3.5	V min	
MCLK IN Only			DV_{DD} = 3 V nominal
V_{INL}, Input Low Voltage	0.4	V max	
V_{INH}, Input High Voltage	2.5	V min	
LOGIC OUTPUTS (Including MCLK OUT)			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 800 μA except for MCLK OUT[13]; DV_{DD} = 5 V
	0.4	V max	I_{SINK} = 100 μA except for MCLK OUT[13]; DV_{DD} = 3 V
V_{OH}, Output High Voltage	4	V min	I_{SOURCE} = 200 μA except for MCLK OUT[13]; DV_{DD} = 5 V
	DV_{DD} − 0.6	V min	I_{SOURCE} = 100 μA except for MCLK OUT[13]; DV_{DD} = 3 V
Floating State Leakage Current	±10	μA max	
Floating State Output Capacitance[14]	9	pF typ	
Data Output Coding	Binary		Unipolar mode
	Offset binary		Bipolar mode
SYSTEM CALIBRATION			
Low Level Input Channels (AIN1 and AIN2)			
Positive Full-Scale Calibration Limit[15]	(1.05 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Negative Full-Scale Calibration Limit[15]	−(1.05 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Offset Calibration Limit[16]	−(1.05 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Input Span[16]	(0.8 × V_{REF})/gain	V min	Gain is the selected PGA gain (1 to 128)
	(2.1 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
High Level Input Channels (AIN3)			
Positive Full-Scale Calibration Limit[15]	(8.4 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Negative Full-Scale Calibration Limit[15]	−(8.4 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Offset Calibration Limit[16]	−(8.4 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
Input Span[16]	(6.4 × V_{REF})/gain	V min	Gain is the selected PGA gain (1 to 128)
	(16.8 × V_{REF})/gain	V max	Gain is the selected PGA gain (1 to 128)
POWER REQUIREMENTS			
Power Supply Voltages			
AV_{DD} Voltage	2.7 to 3.3 or		
	4.75 to 5.25	V min to V max	For specified performance
DV_{DD} Voltage	2.7 to 5.25	V min to V max	For specified performance
Power Supply Currents			
AV_{DD} Current			AV_{DD} = 3 V or 5 V; gain = 1 to 4
	0.27	mA max	Typically 0.22 mA; BUF = 0; $f_{CLK\,IN}$ = 1 MHz or 2.4576 MHz
	0.6	mA max	Typically 0.45 mA; BUF = 1; $f_{CLK\,IN}$ = 1 MHz or 2.4576 MHz
			AV_{DD} = 3 V or 5 V; gain = 8 to 128
	0.5	mA max	Typically 0.38 mA; BUF = 0; $f_{CLK\,IN}$ = 2.4576 MHz
	1.1	mA max	Typically 0.81 mA; BUF = 1; $f_{CLK\,IN}$ = 2.4576 MHz
POWER REQUIREMENTS (Continued)			
DV_{DD} Current[17]			Digital inputs = 0 V or DV_{DD}; external MCLK IN
	0.080	mA max	Typically 0.06 mA; DV_{DD} = 3 V; $f_{CLK\,IN}$ = 1 MHz
	0.15	mA max	Typically 0.13 mA; DV_{DD} = 5 V; $f_{CLK\,IN}$ = 1 MHz
	0.18	mA max	Typically 0.15 mA; DV_{DD} = 3 V; $f_{CLK\,IN}$ = 2.4576 MHz
	0.35	mA max	Typically 0.3 mA; DV_{DD} = 5 V; $f_{CLK\,IN}$ = 2.4576 MHz
Power Supply Rejection[18, 19]		dB typ	

Parameter	B Version[1]	Unit	Conditions/Comments
Normal Mode Power Dissipation[17]			$AV_{DD} = DV_{DD} = 3$ V; digital inputs = 0 V or DV_{DD}; external MCLK IN excluding dissipation in the AIN3 attenuator
	1.05	mW max	Typically 0.84 mW; BUF = 0; $f_{CLK\,IN}$ = 1 MHz, all gains
	2.04	mW max	Typically 1.53 mW; BUF = 1; $f_{CLK\,IN}$ = 1 MHz; all gains
	1.35	mW max	Typically 1.11 mW; BUF = 0; $f_{CLK\,IN}$ = 2.4576 MHz, gain = 1 to 4
	2.34	mW max	Typically 1.9 mW; BUF = 1; $f_{CLK\,IN}$ = 2.457 6 MHz; gain = 1 to 4
Normal Mode Power Dissipation[17]			$AV_{DD} = DV_{DD} = 5$ V; digital inputs = 0 V or DV_{DD}; external MCLKIN
	2.1	mW max	Typically 1.75 mW; BUF = 0; $f_{CLK\,IN}$ = 1 MHz; all gains
	3.75	mW max	Typically 2.9 mW; BUF = 1; $f_{CLK\,IN}$ = 1 MHz; all gains
	3.1	mW max	Typically 2.6 mW; BUF = 0; $f_{CLK\,IN}$ = 2.4576 MHz
	4.75	mW max	Typically 3.75 mW; BUF = 1; $f_{CLK\,IN}$ = 2.4576 MHz
Standby (Power-Down) Current[20]	18	µA max	External MCLK IN = 0 V or DV_{DD}; typically 9 µA; AV_{DD} = 5 V
	8	µA max	External MCLK IN = 0 V or DV_{DD}; typically 4 µA; AV_{DD} = 3 V

[1] Temperature range as follows: B Version, –40°C to +85°C.
[2] These numbers are established from characterization or design at initial product release.
[3] A calibration is effectively a conversion so these errors are of the order of the conversion noise shown in Table 7 and Table 9 for the low level input channels AIN1 and AIN2. This applies after calibration at the temperature of interest.
[4] Recalibration at any temperature removes these drift errors.
[5] Positive full-scale error includes zero-scale errors (unipolar offset error or bipolar zero error) and applies to both unipolar and bipolar input ranges.
[6] Full-scale drift includes zero-scale drift (unipolar offset drift or bipolar zero drift) and applies to both unipolar and bipolar input ranges.
[7] Gain error does not include zero-scale errors. It is calculated as full-scale error—unipolar offset error for unipolar ranges and full-scale error—bipolar zero error for bipolar ranges.
[8] Gain error drift does not include unipolar offset drift/bipolar zero drift. It is effectively the drift of the part if m | jw zero-scale calibrations were performed.
[9] Error is removed following a system calibration.
[10] This common-mode voltage range is allowed provided that the input voltage on analog inputs does not go more positive than AV_{DD} + 30 mV or go more negative than AGND – 100 mV. Parts are functional with voltages down to AGND – 200 mV, but with increased leakage at high temperature.
[11] The analog input voltage range on AIN(+) is given here with respect to the voltage on LCOM on the low level input channels (AIN1 and AIN2) and is given with respect to the HCOM input on the high level input channel, AIN3. The absolute voltage on the low level analog inputs should not go more positive than AV_{DD} + 100 mV, or go more negative than GND – 100 mV for specified performance. Input voltages of AGND – 200 mV can be accommodated, but with increased leakage at high temperature.
[12] V_{REF} = REF IN(+) – REF IN(–).
[13] These logic output levels apply to the MCLK OUT only when it is loaded with one CMOS load.
[14] Sample tested at +25°C to ensure compliance.
[15] After calibration, if the analog input exceeds positive full scale, the converter outputs all 1s. If the analog input is less than negative full scale, the device outputs all 0s.
[16] These calibration and span limits apply provided that the absolute voltage on the analog inputs does not exceed AV_{DD} + 30 mV or go more negative than AGND – 1. mV. The offset calibration limit applies to both the unipolar zero point and the bipolar zero point.
[17] When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the DV_{DD} current and power dissipation varies depending on the crystal or resonator type (see the Clocking and Oscillator Circuit section).
[18] Measured at dc and applies in the selected pass band. PSRR at 50 Hz exceeds 120 dB with filter notches of 25 Hz or 50 Hz. PSRR at 60 Hz exceeds 120 dB with filter notches of 20 Hz or 60 Hz.
[19] PSRR depends on both gain and AV_{DD}. See Table 2 and Table 3.
[20] If the external master clock continues to run in standby mode, the standby current increases to 150 µA typical at 5 V and 75 µA typical at 3 V. When using a crystal or ceramic resonator across the MCLK pins as the clock source for the device, the internal oscillator continues to run in standby mode and the power dissipation depends on the crystal or resonator type (see the Standby Mode section).

Table 2. Low Level Input Channels, AIN1 and AIN2

Gain	1	2	4	8 to 128
AV_{DD} = 3 V	86	78	85	93
AV_{DD} = 5 V	90	78	84	91

Table 3. High Level Input Channel, AIN3

Gain	1	2	4	8 to 128
AV_{DD} = 3 V	68	60	67	75
AV_{DD} = 5 V	72	60	66	73

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = 2.7 V to 5.25 V, AGND = DGND = 0 V; f_{CLKIN} = 2.4576 MHz; input logic = 0, Logic 1 = DV_{DD}, unless otherwise noted.

Table 4.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Conditions/Comments
f_{CLKIN}[3, 4]	400	kHz min	Master clock frequency: crystal oscillator or externally supplied for specified performance
	5	MHz max	
$t_{CLKIN\ LO}$	0.4 × t_{CLKIN}	ns min	Master clock input low time, t_{CLKIN} = 1/f_{CLKIN}
$t_{CLKIN\ HI}$	0.4 × t_{CLKIN}	ns min	Master clock input high time
t_1	500 × t_{CLKIN}	ns nom	$\overline{DRDY}$ high time
t_2	100	ns min	$\overline{RESET}$ pulse width
Read Operation			
t_3	0	ns min	$\overline{DRDY}$ to $\overline{CS}$ setup time
t_4	120	ns min	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_5[5]	0	ns min	SCLK falling edge to data valid delay
	80	ns max	DV_{DD} = 5 V
	100	ns max	DV_{DD} = 3.0 V
t_6	100	ns min	SCLK high pulse width
t_7	100	ns min	SCLK low pulse width
t_8	0	ns min	$\overline{CS}$ rising edge to SCLK rising edge hold time
t_9[6]	10	ns min	Bus relinquish time after SCLK rising edge
	60	ns max	DV_{DD} = 5 V
	100	ns max	DV_{DD} = 3.0 V
t_{10}	100	ns max	SCLK falling edge to $\overline{DRDY}$ high[7]
Write Operation			
t_{11}	120	ns min	$\overline{CS}$ falling edge to SCLK rising edge setup time
t_{12}	30	ns min	Data valid to SCLK rising edge setup time
t_{13}	20	ns min	Data valid to SCLK rising edge hold time
t_{14}	100	ns min	SCLK high pulse width
t_{15}	100	ns min	SCLK low pulse width
t_{16}	0	ns min	$\overline{CS}$ rising edge to SCLK rising edge hold time

[1] Sample tested at +25°C to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V.
[2] See Figure 20 and Figure 21.
[3] f_{CLKIN} duty cycle range is 45% to 55%. f_{CLKIN} must be supplied whenever the AD7707 is not in standby mode. If no clock is present in this case, the device can draw higher current than specified and possibly become uncalibrated.
[4] The AD7707 is production tested with f_{CLKIN} at 2.4576 MHz (1 MHz for some I_{DD} tests). It is guaranteed by characterization to operate at 400 kHz.
[5] These numbers are measured with the load circuit of Figure 2 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[6] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit of Figure 2. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. This means that the times quoted in the timing characteristics are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.
[7] $\overline{DRDY}$ returns high after the first read from the device after an output update. The same data can be read again, if required, while $\overline{DRDY}$ is high, although care should be taken that subsequent reads do not occur close to the next output update.

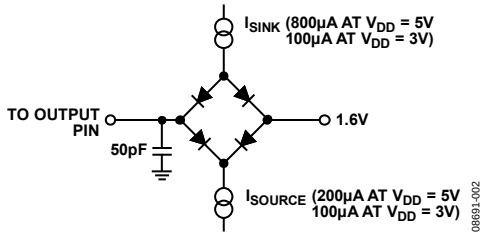


Figure 2. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C, unless otherwise noted.

Table 5.

Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
AV_{DD} to DGND	−0.3 V to +7 V
DV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
AV_{DD} to DV_{DD}	−0.3 V to +7 V
DGND to AGND	−0.3 V to +0.3 V
AIN1, AIN2 Input Voltage to LOCOM	−0.3 V to AV_{DD} + 0.3 V
AIN3 Input Voltage to HICOM	−11 V to +30 V
VBIAS to AGND	−0.3 V to AV_{DD} + 0.3 V
HICOM, LOCOM to AGND	−0.3 V to AV_{DD} + 0.3 V
REF IN(+), REF IN(−) to AGND	−0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOIC Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	75°C/W
Lead Temperature, Soldering	
Reflow	260°C
TSSOP Package, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	139°C/W
Lead Temperature, Soldering	
Reflow	260°C
ESD Rating	2.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

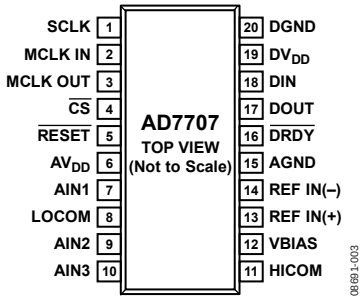


Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	SCLK	Serial Clock, Schmitt-Triggered Logic Input. An external serial clock is applied to this input to access serial data from the AD7707. This serial clock can be a continuous clock with all data transmitted in a continuous train of pulses. Alternatively, it can be a noncontinuous clock with the information being transmitted to the AD7707 in smaller batches of data.
2	MCLK IN	Master Clock Signal for the Device. This can be provided in the form of a crystal/resonator or external clock. A crystal/resonator can be tied across the MCLK IN and MCLK OUT pins. Alternatively, the MCLK IN pin can be driven with a CMOS-compatible clock and MCLK OUT left unconnected. The part can be operated with clock frequencies in the range of 500 kHz to 5 MHz.
3	MCLK OUT	When the master clock for the device is a crystal/resonator, the crystal/resonator is connected between MCLK IN and MCLK OUT. If an external clock is applied to MCLK IN, MCLK OUT provides an inverted clock signal. This clock can be used to provide a clock source for external circuitry and is capable of driving one CMOS load. If the user does not require it, this MCLK OUT can be turned off via the CLKDIS bit of the clock register. This ensures that the part is not wasting unnecessary power driving capacitive loads on MCLK OUT.
4	$\overline{CS}$	Chip Select. This pin is an active low logic input used to select the AD7707. With this input hard-wired low, the AD7707 can operate in its 3-wire interface mode with SCLK, DIN, and DOUT used to interface to the device. $\overline{CS}$ can be used to select the device in systems with more than one device on the serial bus or as a frame synchronization signal in communicating with the AD7707.
5	$\overline{RESET}$	Logic Input. Active low input that resets the control logic, interface logic, calibration coefficients, digital filter, and analog modulator of the part to power-on status.
6	AV_{DD}	Analog Supply Voltage, 2.7 V to 5.25 V Operation.
7	AIN1	Low Level Analog Input Channel 1. This is used as a pseudo differential input with respect to LOCOM.
8	LOCOM	Common Input for Low Level Input Channels. Analog inputs on AIN1 and AIN2 must be referenced to this input.
9	AIN2	Low Level Analog Input Channel 2. This is used as a pseudo differential input with respect to LOCOM.
10	AIN3	Single-Ended High Level Analog Input Channel with respect to HICOM.
11	HICOM	Common Input for High Level Input Channel. Analog input on AIN3 must be referenced to this input.
12	VBIAS	VBIAS is used to level shift the high level input channel signal. This signal is used to ensure that the AIN(+) and AIN(–) signals seen by the internal modulator are within its common-mode range. VBIAS is normally connected to 2.5 V when AV_{DD} = 5 V and 1.225 V when AV_{DD} = 3 V.
13	REF IN(+)	Reference Input. Positive input of the differential reference input to the AD7707. The reference input is differential with the provision that REF IN(+) must be greater than REF IN(–). REF IN(+) can lie anywhere between AV_{DD} and AGND.
14	REF IN(–)	Reference Input. Negative input of the differential reference input to the AD7707. The REF IN(–) can lie anywhere between AV_{DD} and AGND provided that REF IN(+) is greater than REF IN(–).
15	AGND	Analog Ground. Ground reference point for the AD7707's internal analog circuitry.
16	$\overline{DRDY}$	Logic Output. A logic low on this output indicates that a new output word is available from the AD7707 data register. The $\overline{DRDY}$ pin returns high upon completion of a read operation of a full output word. If no data read has taken place between output updates, the $\overline{DRDY}$ line returns high for 500 × $t_{CLK\ IN}$ cycles prior to the next output update. While $\overline{DRDY}$ is high, a read operation should neither be attempted nor in progress to avoid reading from the data register as it is being updated. The $\overline{DRDY}$ line returns low again when the update has taken place. $\overline{DRDY}$ is also used to indicate when the AD7707 has completed its on-chip calibration sequence.
17	DOUT	Serial Data Output with Serial Data Being Read from the Output Shift Register on the Part. This output shift register can contain information from the setup register, communications register, clock register, or data register, depending on the register selection bits of the communications register.

Pin No.	Mnemonic	Description
18	DIN	Serial Data Input with Serial Data Being Written to the Input Shift Register on the Part. Data from this input shift register is transferred to the setup register, clock register, or communications register, depending on the register selection bits of the communications register.
19	DV_{DD}	Digital Supply Voltage, 2.7 V to 5.25 V Operation.
20	DGND	Ground Reference Point for the AD7707's Internal Digital Circuitry.

TYPICAL PERFORMANCE CHARACTERISTICS

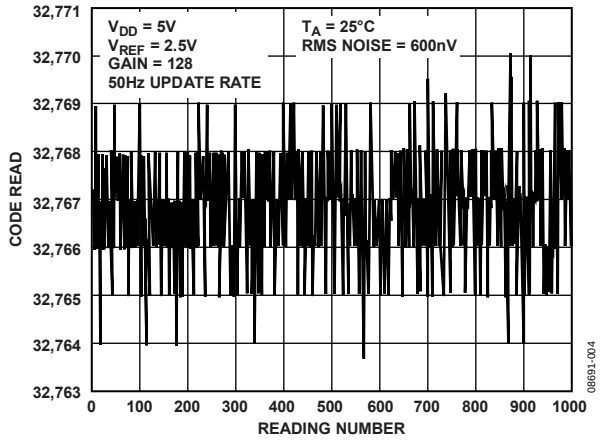


Figure 4. Typical Noise Plot at Gain = 128 with 50 Hz Update Rate for Low Level Input Channel

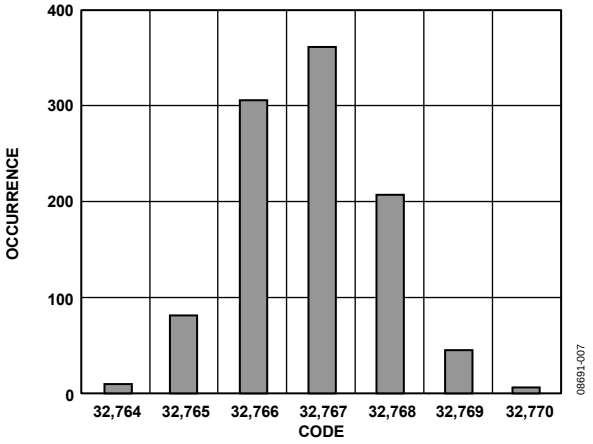


Figure 7. Histogram of Data in Figure 4

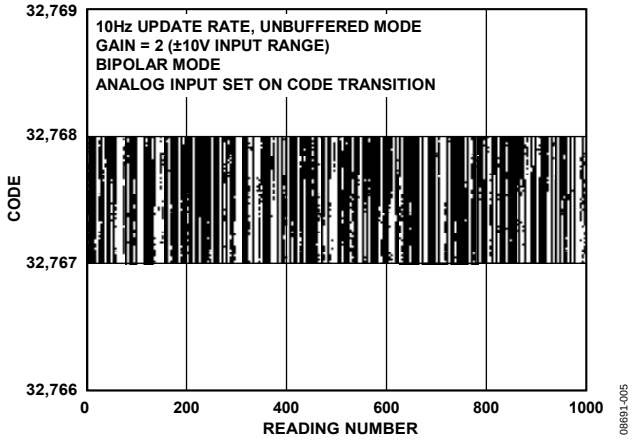


Figure 5. Typical Noise Plot for AIN3, High Level Input Channel

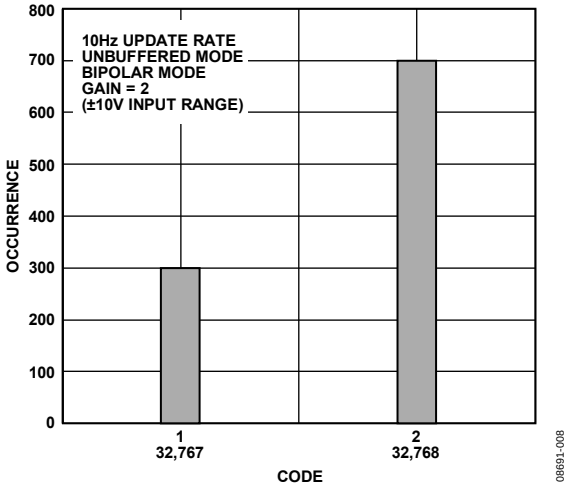


Figure 8. Histogram of Data in Figure 5

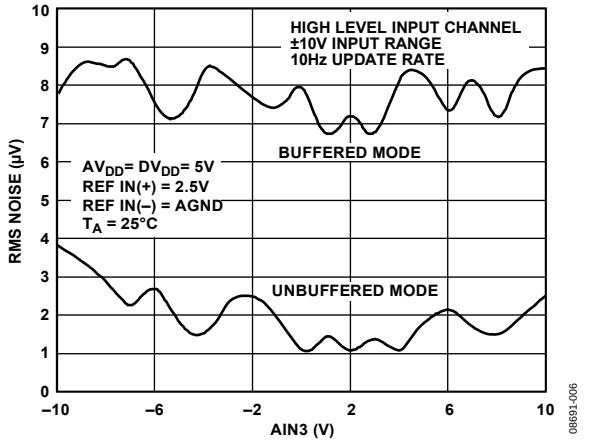


Figure 6. Typical RMS Noise vs. Analog Input Voltage for High Level Input Channel, AIN3

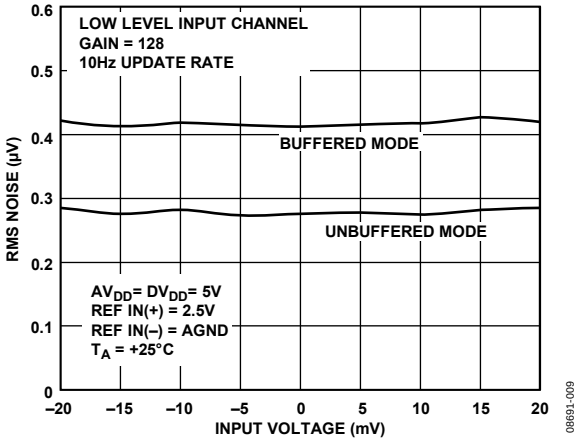


Figure 9. Typical RMS Noise vs. Analog Input Voltage for Low Level Input Channels, AIN1 and AIN2

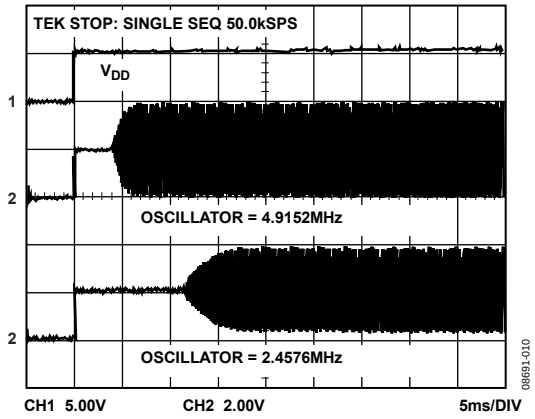


Figure 10. Typical Crystal Oscillator Power-Up Time

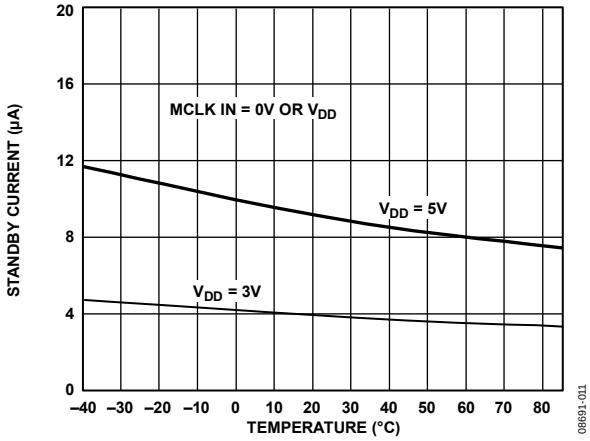


Figure 11. Standby Current vs. Temperature

OUTPUT NOISE

OUTPUT NOISE FOR LOW LEVEL INPUT CHANNELS (5 V OPERATION)

Table 7 shows the AD7707 output rms noise and peak-to-peak resolution in unbuffered mode for the selectable notch and −3 dB frequencies for the part, as selected by FS0, FS1, and FS2 of the clock register. The numbers given are for the bipolar input ranges with a V_{REF} of 2.5 V and AV_{DD} = 5 V. These numbers are typical and are generated at an analog input voltage of 0 V. Table 8 shows the rms noise and peak-to-peak resolution when operating in buffered mode. It is important to note that the peak-to-peak numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. The numbers given are for bipolar input ranges with a V_{REF} of 2.5 V. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLKDIV bit of the clock register set to 0. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in Table 7 and Table 8 are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range but the peak-to-peak resolution is now based on half the signal range, which effectively means losing one bit of resolution.

Table 7. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V AIN1 and AIN2 Unbuffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in µV (Peak-to-Peak Resolution in Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	1.2 (16)	0.7 (16)	0.7 (16)	0.54 (16)	0.28 (16)	0.28 (16)	0.28 (15.5)	0.27 (14.5)
50 Hz	13.1 Hz	3.6 (16)	2.1 (16)	1.25 (16)	0.89 (16)	0.62 (16)	0.60 (15.5)	0.56 (14.5)	0.56 (13.5)
60 Hz	15.72 Hz	4.7 (16)	2.6 (16)	1.5 (16)	0.94 (16)	0.73 (16)	0.68 (15.5)	0.66 (14.5)	0.63 (13.5)
250 Hz	65.5 Hz	95 (13)	65 (13)	23.4 (13)	11.6 (13)	6.5 (13)	3.4 (13)	2.1 (12.5)	1.5 (12)
500 Hz	131 Hz	600 (10.5)	316 (10.5)	138 (10.5)	71 (10.5)	38 (10.5)	18 (10.5)	10 (10)	5.7 (10)
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	1.19 (16)	0.69 (16)	0.71 (16)	0.63 (16)	0.27 (16)	0.27 (16)	0.26 (15.5)	0.24 (15)
20 Hz	5.24 Hz	3.68 (16)	2.18 (16)	1.19 (16)	0.94 (16)	0.6 (16)	0.6 (15.5)	0.56 (14.5)	0.56 (13.5)
25 Hz	6.55 Hz	4.78 (16)	2.66 (16)	1.51 (16)	1.07 (16)	0.7 (16)	0.67 (15.5)	0.66 (14.5)	0.65 (13.5)
100 Hz	26.2 Hz	100 (13)	50.1 (13)	23.5 (13)	11.9 (13)	5.83 (13)	3.64 (13)	2.16 (12.5)	1.5 (12)
200 Hz	52.5 Hz	543 (10.5)	318 (10.5)	132 (10.5)	68.1 (10.5)	33.1 (10.5)	17.6 (10.5)	9.26 (10.5)	6.13 (10)

Table 8. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V AIN1 and AIN2 Buffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Loise in µV (Peak-to-Peak Resolution in Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	1.47 (16)	0.95 (16)	0.88 (16)	0.55 (16)	0.42 (16)	0.42 (16)	0.42 (15)	0.41 (14)
50 Hz	13.1 Hz	4.2 (16)	2.6 (16)	1.6 (16)	1 (16)	0.89 (15.5)	0.94 (15)	0.9 (14)	0.9 (13)
60 Hz	15.72 Hz	4.9 (16)	3 (16)	1.8 (16)	1.1 (16)	1 (15.5)	1 (14.5)	0.94 (14)	0.94 (13)
250 Hz	65.5 Hz	104 (13)	52 (13)	26 (13)	14 (13)	6.5 (13)	4.1 (12.5)	2.7 (12.5)	2.3 (11.5)
500 Hz	131 Hz	572 (10.5)	293 (10.5)	125 (10.5)	69 (10.5)	40 (10.5)	19 (10.5)	10 (10.5)	5.9 (10)
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	1.48 (16)	8.95 (16)	0.87 (16)	0.67 (16)	0.41 (16)	0.40 (16)	0.40 (15)	0.40 (14)
20 Hz	5.24 Hz	3.9 (16)	2.46 (16)	1.77 (16)	1.19 (16)	0.94 (16)	0.93 (15)	0.95 (14)	0.9 (13)
25 Hz	6.55 Hz	5.37 (16)	3.05 (16)	1.89 (16)	1.33 (16)	1.11 (15.5)	1.06 (14.5)	1.04 (13.5)	1.02 (12.5)
100 Hz	26.2 Hz	98.9 (13)	52.4 (13)	26.1 (13)	12.7 (13)	6.08 (13)	4.01 (12.5)	2.62 (12.5)	2.33 (11.5)
200 Hz	52.4 Hz	596 (10.5)	298 (10.5)	133 (10.5)	69.3 (10.5)	34.7 (10.5)	16.9 (10.5)	9.67 (10.5)	6.34 (10)

OUTPUT NOISE FOR LOW LEVEL INPUT CHANNELS (3 V OPERATION)

Table 9 shows the AD7707 output rms noise and peak-to-peak resolution in unbuffered mode for the selectable notch and −3 dB frequencies for the part, as selected by FS0, FS1, and FS2 of the clock register. The numbers given are for the bipolar input ranges with a V_{REF} of 1.225 V and an AV_{DD} = 3 V. These numbers are typical and are generated at an analog input voltage of 0 V. Table 10 shows the rms noise and peak-to-peak resolution when operating in buffered mode. It is important to note that the peak-to-peak numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. The numbers given are for bipolar input ranges with a V_{REF} of 1.225 V and for either buffered or unbuffered mode. These numbers are typical and are rounded to the nearest LSB. The numbers apply for the CLKDIV bit of the clock register set to 0. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in Table 9 and Table 10 are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range but the peak-to-peak resolution is now based on half the signal range, which effectively means losing 1 bit of resolution.

Table 9. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 3 V AIN1 and AIN2 Unbuffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in μV (Peak-to-Peak Resolution in Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	1.60 (16)	0.8 (16)	0.48 (16)	0.29 (16)	0.29 (16)	0.27 (15.5)	0.26 (14.5)	0.26 (13.5)
50 Hz	13.1 Hz	3.8 (16)	1.9 (16)	1.1 (16)	0.64 (16)	0.60 (15.5)	0.6 (14.5)	0.6 (13.5)	0.6 (12.5)
60 Hz	15.72 Hz	4.4 (16)	2.2 (16)	1.35 (16)	0.78 (16)	0.7 (15)	0.68 (14.5)	0.64 (13.5)	0.64 (12.5)
250 Hz	65.5 Hz	53 (13)	24 (13)	15 (13)	6.8 (13)	3.6 (12.5)	2.1 (12.5)	1.5 (12)	1.3 (11)
500 Hz	131 Hz	300 (10.5)	138 (10.5)	80 (10.5)	34 (10.5)	18 (10.5)	8.7 (10.5)	4.8 (10)	3.4 (10)
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	1.56 (16)	0.88 (16)	0.52 (16)	0.3 (16)	0.28 (16)	0.27 (15.5)	0.27 (14.5)	0.26 (13.5)
20 Hz	5.24 Hz	3.85 (16)	2.02 (16)	1.15 (16)	0.74 (16)	0.63 (15.5)	0.57 (14.5)	0.61 (13.5)	0.58 (12.5)
25 Hz	6.55 Hz	4.56 (16)	2.4 (16)	1.4 (16)	0.79 (16)	0.68 (15)	0.66 (14.5)	0.64 (13.5)	0.64 (12.5)
100 Hz	26.2 Hz	45.7 (13)	22 (13)	13.7 (13)	5.27 (13)	2.64 (13)	2 (12.5)	1.59 (12)	1.4 (11)
200 Hz	52.4 Hz	262 (10.5)	125 (10.5)	66 (10.5)	32.4 (10.5)	18.4 (10.5)	8.6 (10.5)	4.64 (10.5)	3.3 (10)

Table 10. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 3 V AIN1 and AIN2 Buffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in μV (Peak-to-Peak Resolution in Bits)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	1.80 (16)	1 (16)	0.7 (16)	0.41 (16)	0.41 (16)	0.41 (15)	0.41 (14)	0.41 (13)
50 Hz	13.1 Hz	4.1 (16)	2.4 (16)	1.5 (16)	1 (15.5)	0.91 (15)	0.89 (14)	0.86 (13)	0.83 (12)
60 Hz	15.72 Hz	5.1 (16)	3 (16)	1.8 (16)	1.1 (15.5)	0.94 (14.5)	0.94 (13.5)	0.99 (13)	0.99 (11.5)
250 Hz	65.5 Hz	50 (13)	27 (13)	12.3 (13)	6.4 (13)	4 (12.5)	2.7 (12.5)	2.2 (11.5)	1.8 (11)
500 Hz	131 Hz	275 (10.5)	125 (10.5)	80 (10.5)	39 (10.5)	16 (10.5)	8.9 (10.5)	5.2 (10)	4.2 (9.5)
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	1.75 (16)	1.18 (16)	0.67 (16)	0.44 (16)	0.41 (16)	0.44 (15)	0.43 (14)	0.43 (13)
20 Hz	5.24 Hz	4.21 (16)	2.5 (16)	1.48 (16)	1 (15.5)	0.94 (15)	0.96 (14)	0.89 (13)	0.86 (12)
25 Hz	6.55 Hz	5.15 (16)	2.8 (16)	1.8 (16)	1.15 (15.5)	1 (14.5)	1.02 (13.5)	0.96 (13)	1.03 (11.5)
100 Hz	26.2 Hz	46.1 (13)	24.3 (13)	13.6 (13)	6.71 (13)	4.1 (12.5)	2.54 (12.5)	2.3 (11.5)	2.15 (10.5)
200 Hz	52.4 Hz	282 (10.5)	123 (10.5)	66 (10.5)	35.3 (10.5)	14.8 (10.5)	9.91 (10.5)	5.48 (10)	4.01 (9.5)

OUTPUT NOISE FOR HIGH LEVEL INPUT CHANNEL AIN3 (5 V OPERATION)

Table 11 shows the AD7707 output rms noise and peak-to-peak resolution in unbuffered mode for the selectable notch and −3 dB frequencies for the part, as selected by FS0, FS1, and FS2 of the clock register. The numbers given are for the ±10 V, ±5 V, 0 to 5 V and 0 V to 10 V ranges with a V_{REF} of 2.5 V, VBIAS = 2.5 V, HICOM = AGND, and AV_{DD} = 5 V. These numbers are typical and are generated at an analog input voltage of 0 V. Table 12 meanwhile shows the output rms noise and peak-to-peak resolution in buffered mode. It is important to note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise, but on peak-to-peak noise. Operating the high level channel with a gain of 2 in bipolar mode gives an operating range of ±10 V. Operating at a gain of 2 in unipolar mode gives a range of 0 V to +10 V. Operating the high level channel with a gain of 4 in bipolar mode gives the ±5 V operating range. Operating at a gain of 4 in unipolar mode gives an operating range of 0 V to 5 V. Noise for all input ranges is shown in Output Noise For High Level Input Channel, AIN3 section. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in Table 11 and Table 12 are given for the bipolar input ranges. For the unipolar ranges the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range, which effectively means losing 1 bit of resolution.

Table 11. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V AIN3 Unbuffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	±10 V Range		±5 V Range		0 V to 10 V Range		0 V to 5 V Range	
		RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	5.10	16	3.52	16	5.10	16	3.52	16
50 Hz	13.1 Hz	15.82	16	9.77	16	15.82	16	9.77	16
60 Hz	15.72 Hz	20.36	16	12.29	16	20.36	16	12.29	16
250 Hz	65.5 Hz	430	13	212	13	430	12	212	12
500 Hz	131 Hz	2350	10	1287	10	2350	9	1287	9
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	5.13	16	3.53	16	5.13	16	3.53	16
20 Hz	5.24 Hz	18.9	16	13.25	16	18.9	16	13.25	16
25 Hz	6.55 Hz	23.7	16	15.3	16	23.7	16	15.3	15.5
100 Hz	26.2 Hz	406	13	174	13	406	12	174	12
200 Hz	52.4 Hz	2184	10.5	1144	10.5	2184	9.5	1144	9.5

Table 12. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ 5 V AIN3 Buffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	±10 V Range		±5 V Range		0 V to 10 V Range		0 to 5 V Range	
		RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	7.4	16	5.2	16	7.4	16	5.2	16
50 Hz	13.1 Hz	22.2	16	14.3	16	22.2	16	14.3	16
60 Hz	15.72 Hz	26.6	16	15.85	16	26.6	16	15.85	16
250 Hz	65.5 Hz	475	13	187	13	475	12	187	12
500 Hz	131 Hz	2423	10.5	1097	10.5	2423	9.5	1097	9.5
MCLK IN = 1 MHz									
4.05 Hz	1.06 Hz	7.63	16	5.45	16	7.63	16	5.45	16
20 Hz	5.24 Hz	20.25	16	13.3	16	20.25	16	13.3	16
25 Hz	6.55 Hz	23.5	16	14.6	16	23.5	16	14.6	15.5
100 Hz	26.2 Hz	377	13	210	13	377	12	210	12
200 Hz	52.4 Hz	2226	10.5	1132	10.5	2226	9.5	1132	9.5

OUTPUT NOISE FOR HIGH LEVEL INPUT CHANNEL AIN3 (3 V OPERATION)

Table 13 shows the AD7707 output rms noise and peak-to-peak resolution for the selectable notch and −3 dB frequencies for the part, as selected by FS0, FS1, and FS2 of the clock register. The numbers given are for the ±5 V, 0 V to 5 V and 0 V to 10 V ranges with a V_{REF} of 1.225 V, VBIAS = 1.225 V, HICOM = AGND, and AV_{DD} = 3 V. These numbers are typical and are generated at an analog input voltage of 0 V for unbuffered mode of operation. The ±5 V, 0 V to 5 V, and 0 V to 10 V operating ranges are only achievable in unbuffered mode when operating at 3 V due to common-mode limitations on the input amplifier. It is important to note that these numbers represent the resolution for which there are no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. Operating at a gain of 1 in unipolar mode provides a range of 0 V to +10 V. Operating the high level channel with a gain of 2 in bipolar mode provides a ±5 V operating range. Operating at a gain of 2 in unipolar mode provides an operating range of 0 V to 5 V. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in Table 13 are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range, which effectively means losing 1 bit of resolution.

Table 13. Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ +3 V AIN3 Unbuffered Mode Only

Filter First Notch and Output Data Rate	−3 dB Frequency	0 V to 10 V Range		±5 V Range		0 to 5 V Range	
		RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution	RMS Noise (μV)	P-P (Bits) Resolution
MCLK IN = 2.4576 MHz							
10 Hz	2.62 Hz	12.4	16	7.02	16	7.02	16
50 Hz	13.1 Hz	30.35	16	16.4	16	16.4	15.5
60 Hz	15.72 Hz	34.55	16	19.13	16	19.13	15
250 Hz	65.5 Hz	498	12.5	204	13	204	12
500 Hz	131 Hz	2266	10.5	1151	10.5	1151	9.5
MCLK IN = 1 MHz							
4.05 Hz	1.06 Hz	13.9	16	7.3	16	7.3	16
20 Hz	5.24 Hz	32.2	16	17.4	16	17.4	15
25 Hz	6.55 Hz	33.4	16	18.57	16	18.57	15
100 Hz	26.2 Hz	430	13	200	13	200	12
200 Hz	52.4 Hz	2207	10.5	1048	10.5	1048	9.5

ON-CHIP REGISTERS

The AD7707 contains eight on-chip registers that can be accessed via the serial port of the part. The first of these is a communications register that controls the channel selection, decides whether the next operation is a read or write operation and selects which register the next read or write operation accesses. All communications to the part must start with a write operation to the communications register. After power-on or RESET, the device expects a write to its communications register. The data written to this register determines whether the next operation to the part is a read or a write operation and determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the communications register followed by a write to the selected register. A read operation from any other register on the part (including the communications register itself and the data register) starts with a write operation to the communications register followed by a read operation from the selected register. The communications register also controls the standby mode and channel selection* and the DRDY status is available by reading from the communications register. The second register is a setup register that determines calibration mode, gain setting, bipolar/unipolar operation, and buffered mode. The third register is the clock register and contains the filter selection bits and clock control bits. The fourth register is the data register from which the output data from the part is accessed. The final registers are the calibration registers, which store channel calibration data. The registers are described in more detail in the following sections.

COMMUNICATIONS REGISTER (RS2, RS1, RS0 = 0, 0, 0)

The communications register is an 8-bit register from which data can either be read or to which data can be written. All communications to the part must start with a write operation to the communications register. The data written to the communications register determines whether the next operation is a read or write operation and to which register this operation takes place. When the subsequent read or write operation to the selected register is complete, the interface returns to where it expects a write operation to the communications register. This is the default state of the interface, and on power-up or after a RESET, the AD7707 is in this default state waiting for a write operation to the communications register. In situations where the interface sequence is lost, if a write operation of sufficient duration (containing at least 32 serial clock cycles) takes place with DIN high, the AD7707 returns to this default state. Table 14 outlines the bit designations for the communications register.

Table 14. Communications Register

0/DRDY (0)	RS2 (0)	RS1 (0)	RS0 (0)	R/W (0)	STBY (0)	CH1 (0)	CH0 (0)

Table 15. Communications Register Bit Descriptions

Bit	Description
0/DRDY	For a write operation, a 0 must be written to this bit so that the write operation to the communications register actually takes place. If a 1 is written to this bit, the part does not clock on to subsequent bits in the register. The serial interface stays at this bit location until a 0 is written to this bit. Once a 0 is written to this bit, the next seven bits are loaded to the communications register. For a read operation, this bit provides the status of the DRDY flag from the part. The status of this bit is the same as the DRDY output pin.
RS2 to RS0	Register selection bits. These three bits select to which one of eight on-chip registers the next read or write operation takes place, as shown in Table 16, along with the register size. When the read or write operation to the selected register is complete, the part waits for a write operation to the communications register. It does not remain in a state where it continues to access the register.
R/W	Read/Write select. This bit selects whether the next operation is a read or write operation to the selected register. A 0 indicates a write cycle for the next operation to the appropriate register, while a 1 indicates a read operation from the appropriate register.
STBY	Standby. Writing a 1 to this bit puts the part into its standby or power-down mode. In this mode, the part consumes only 8 µA of power supply current. The part retains its calibration coefficients and control word information when in standby. Writing a 0 to this bit places the part in its normal operating mode. The serial interface on the AD7707 remains operational when the part is in standby mode.
CH1, CH0	Channel select. These two bits select a channel for conversion or for access to the calibration coefficients as outlined in Table 17. Three pairs of calibration registers on the part are used to store the calibration coefficients following a calibration on a channel. They are shown in Table 17 for the AD7707 to indicate which channel combinations have independent calibration coefficients. With CH1 at Logic 1 and CH0 at a Logic 0, the part looks at the LOCOM input internally shorted to itself. This can be used as a test method to evaluate the noise performance of the part with no external noise sources. In this mode, the LOCOM input should be connected to an external voltage within the allowable common-mode range for the part.

Table 16. Register Selection

RS2	RS1	RS0	Register	Register Size
0	0	0	Communications register	8 bits
0	0	1	Setup register	8 bits
0	1	0	Clock register	8 bits
0	1	1	Data register	16 bits
1	0	0	Test register	8 bits
1	0	1	No operation	
1	1	0	Zero-scale calibration register	24 bits
1	1	1	Full-scale calibration register	24 bits

Table 17. Channel Selection for AD7707

CH1	CH0	AIN	Reference	Calibration Register Pair
0	0	AIN1	LOCOM	Register Pair 0
0	1	AIN2	LOCOM	Register Pair 1
1	0	LOCOM	LOCOM	Register Pair 0
1	1	AIN3	HICOM	Register Pair 2

Setup Register (RS2, RS1, RS0 = 0, 0, 1); Power-On/Reset Status: 0x01

The setup register is an eight-bit register from which data can either be read or to which data can be written. Table 18 outlines the bit designations for the setup register.

Table 18. Setup Register

MD1 (0)	MD0 (0)	G2 (0)	G1 (0)	G0 (0)	$\overline{B}$/U (0)	BUF (0)	FSYNC (1)

Table 19.

Bit	Description
MD1, MD0	Operating mode selection bits.
G2 to G0	Gain selection bits. These bits select the gain setting for the on-chip PGA, as outlined in Table 21.
$\overline{B}$/U	$\overline{Bipolar}$/unipolar operation. A 0 in this bit selects $\overline{Bipolar}$ operation. A 1 in this bit selects unipolar operation.
BUF	Buffer control. With this bit at 0, the on-chip buffer on the analog input is shorted out. With the buffer shorted out, the current flowing in the AV_{DD} line is reduced. When this bit is high, the on-chip buffer is in series with the analog input allowing the input to handle higher source impedances.
FSYNC	Filter synchronization. When this bit is high, the nodes of the digital filter, the filter control logic, and the calibration control logic are held in a reset state, and the analog modulator is held in its reset state. When this bit goes low, the modulator and filter start to process data and a valid word is available in 3 × 1/(output update rate), that is, the settling time of the filter. This FSYNC bit does not affect the digital interface and does not reset the $\overline{DRDY}$ output if it is low.

Table 20. Operating Modes

MD1	MD0	Operating Mode
0	0	Normal mode: this is the normal mode of operation of the device whereby the device is performing normal conversions.
0	1	Self-calibration: this activates self-calibration on the channel selected by CH1 and CH0 of the communications register. This is a one-step calibration sequence and, when complete, the part returns to normal mode with MD1 and MD0 returning to 0, 0. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this self-calibration is complete and a new valid word is available in the data register. The zero-scale calibration is performed at the selected gain on internally shorted (zeroed) inputs and the full-scale calibration is performed at the selected gain on an internally-generated V_{REF}/selected gain.
1	0	Zero-scale (ZS) system calibration: this activates zero-scale system calibration on the channel selected by CH1 and CH0 of the communications register. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this zero-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to l ormal k ode with MD1 and MD0 returning to 0, 0.
1	1	Full-scale (FS) system calibration: this activates full-scale system calibration on the selected input channel. Calibration is performed at the selected gain on the input voltage provided at the analog input during this calibration sequence. This input voltage should remain stable for the duration of the calibration. The $\overline{DRDY}$ output or bit goes high when calibration is initiated and returns low when this full-scale calibration is complete and a new valid word is available in the data register. At the end of the calibration, the part returns to normal mode with MD1 and MD0 returning to 0, 0.

Table 21. Gain Selection

G2	G1	G0	Gain Setting
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Clock Register (RS2, RS1, RS0 = 0, 1, 0); Power-On/Reset Status: 0x05

The clock register is an 8-bit register from which data can either be read or to which data can be written. Table 22 outlines the bit designations for the clock register.

Table 22. Clock Register

Zero (0)	Zero (0)	CLKDIS (0)	CLKDIV (0)	CLK (1)	FS2 (0)	FS1 (0)	FS0 (1)

Table 23. Clock Register Bit Descriptions

Bit	Description
Zero	Zero. A zero must be written to these bits to ensure correct operation of the AD7707. Failure to do so may result in unspecified operation of the device.
CLKDIS	Master clock disable bit. A Logic 1 in this bit disables the master clock from appearing at the MCLK OUT pin. When disabled, the MCLK OUT pin is forced low. This feature allows the user the flexibility of using the MCLK OUT as a clock source for other devices in the system or of turning off the MCLK OUT as a power saving feature. When using an external master clock on the MCLK IN pin, the AD7707 continues to have internal clocks and converts normally with the CLKDIS bit active. When using a crystal oscillator or ceramic resonator across the MCLK IN and MCLK OUT pins, the AD7707 clock is stopped and no conversions take place when the CLKDIS bit is active.
CLKDIV	Clock divider bit. With this bit at a Logic 1, the clock frequency appearing at the MCLK IN pin is divided by two before being used internally by the AD7707. For example, when this bit is set to 1, the user can operate with a 4.9152 MHz crystal between MCLK IN and MCLK OUT, and internally the part operates with the specified 2.4576 MHz. With this bit at a Logic 0, the clock frequency appearing at the MCLK IN pin is the frequency used internally by the part.
CLK	Clock bit. This bit should be set in accordance with the operating frequency of the AD7707. If the device has a master clock frequency of 2.4576 MHz (CLKDIV = 0) or 4.9152 MHz (CLKDIV = 1), then this bit should be set to a 1. If the device has a master clock frequency of 1 MHz (CLKDIV = 0) or 2 MHz (CLKDIV = 1), this bit should be set to a 0. This bit sets up the appropriate scaling currents for a given operating frequency and also chooses (along with FS2, FS1 and FS0) the output update rate for the device. If this bit is not set correctly for the master clock frequency of the device, then the AD7707 may not operate to specification.
FS2, FS1, FS0	Filter selection bits. Along with the CLK bit, FS2, FS1, and FS0 determine the output update rate, filter first notch, and −3 dB frequency as outlined in Table 24. The on-chip digital filter provides a $sinc^3$ (or $Sinx/x^3$) filter response. Placing the first notch at 10 Hz places notches at both 50 Hz and 60 Hz, giving better than 150 dB rejection at these frequencies. In association with the gain selection, the filter cutoff also determines the output noise of the device. Changing the filter notch frequency, as well as the selected gain, impacts resolution. Table 7 to Table 13 show the effect of filter notch frequency and gain on the output noise and effective resolution of the part. The output data rate (or effective conversion time) for the device is equal to the frequency selected for the first notch of the filter. For example, if the first notch of the filter is selected at 50 Hz, a new word is available at a 50 Hz output rate, or every 20 ms. If the first notch is at 500 Hz, a new word is available every 2 ms. A calibration should be initiated when any of these bits are changed. The settling time of the filter to a full-scale step input is worst-case 4 × 1/(output data rate). For example, with the filter first notch at 50 Hz, the settling time of the filter to a full-scale step input is 80 ms maximum. If the first notch is at 500 Hz, the settling time is 8 ms maximum. This settling time can be reduced to 3 × 1/(output data rate) by synchronizing the step input change to a reset of the digital filter. In other words, if the step input takes place with the FSYNC bit high, the settling time is 3 × 1/(output data rate) from when the FSYNC bit returns low. The −3 dB frequency is determined by the programmed first notch frequency according to the following relationship: *filter − 3 dB frequency = 0.262 × filter first notch frequency*

Table 24. Output Update Rates

CLK[1]	FS2	FS1	FS0	Output Update Rate	−3 dB Filter Cutoff
0	0	0	0	20 Hz	5.24 Hz
0	0	0	1	25 Hz	6.55 Hz
0	0	1	0	100 Hz	26.2 Hz
0	0	1	1	200 Hz	52.4 Hz
1	0	0	0	50 Hz	13.1 Hz
1	0	0	1	60 Hz	15.7 Hz
1	0	1	0	250 Hz	65.5 Hz
1	0	1	1	500 Hz	131 Hz
0	1	0	0	4.054 Hz	1.06 Hz
0	1	0	1	4.23 Hz	1.11 Hz
0	1	1	0	4.84 Hz	1.27 Hz
0	1	1	1	4.96 Hz	1.3 Hz
1	1	0	0	10 Hz	2.62 Hz
1	1	0	1	10.34 Hz	2.71 Hz
1	1	1	0	11.90 Hz	3.13 Hz
1	1	1	1	12.2 Hz	3.2 Hz

[1] Assumes correct clock frequency on the MCLK IN pin with the CLKDIV bit set appropriately.

Data Register (RS2, RS1, RS0 = 0, 1, 1)

The data register on the part is a 16-bit read-only register that contains the most up-to-date conversion result from the AD7707. If the communications register sets up the part for a write operation to this register, a write operation must actually take place to return the part to where it is expecting a write operation to the communications register. However, the 16 bits of data written to the part are ignored by the AD7707.

Test Register (RS2, RS1, RS0 = 1, 0, 0); Power-On/Reset Status: 0x00

The part contains a test register that is used when testing the device. The user is advised not to change the status of any of the bits in this register from the default (power-on or $\overline{\text{RESET}}$) status of all 0s because the part will be placed in one of its test modes and will not operate correctly.

Zero-Scale Calibration Register (RS2, RS1, RS0 = 1, 1, 0); Power-On/Reset Status: 0x1F4000

The AD7707 contains independent sets of zero-scale registers, one for each of the input channels. Each of these registers is a 24-bit read/write register; 24 bits of data must be written; otherwise, no data is transferred to the register. This register is used in conjunction with its associated full-scale register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table 17. Although the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking the FSYNC bit in the setup register high before the calibration register operation and taking it low after the operation is complete.

Full-Scale Calibration Register (RS2, RS1, RS0 = 1, 1, 1); Power-On/Reset Status: 0x5761AB

The AD7707 contains independent sets of full-scale registers, one for each of the input channels. Each of these registers is a 24-bit read/write register; 24 bits of data must be written; otherwise, no data is transferred to the register. This register is used in conjunction with its associated zero-scale register to form a register pair. These register pairs are associated with input channel pairs as outlined in Table 17. Although the part is set up to allow access to these registers over the digital interface, the part itself no longer has access to the register coefficients to correctly scale the output data. As a result, there is a possibility that after accessing the calibration registers (either read or write operation) the first output data read from the part may contain incorrect data. In addition, a write to the calibration register should not be attempted while a calibration is in progress. These eventualities can be avoided by taking rfc FSYNC bit in the setup register high before the calibration register operation and taking it low after the operation is complete.

CALIBRATION SEQUENCES

The AD7707 contains a number of calibration options as previously outlined. Table 25 summarizes the calibration types, the operations involved, and the duration of the operations. There are two methods of determining the end of calibration. The first is to monitor when $\overline{\text{DRDY}}$ returns low at the end of the sequence. $\overline{\text{DRDY}}$ not only indicates when the sequence is complete, but also that the part has a valid new sample in its data register. This valid new sample is the result of a normal conversion, which follows the calibration sequence. The second method of determining when calibration is complete is to monitor the MD1 and MD0 bits of the setup register. When these bits return to 0 (0 following a calibration command), it indicates that the calibration sequence is complete. This method does not give any indication of there being a valid new result in the data register. However, it gives an earlier indication than $\overline{\text{DRDY}}$ that calibration is complete. The duration to when the Mode Bits (MD1 and MD0) return to 00 represents the duration of the calibration carried out). The sequence to when $\overline{\text{DRDY}}$ goes low also includes a normal conversion and a pipeline delay, t_P, to correctly scale the results of this first conversion. t_P will never exceed 2000 × t_{CLKIN}. The time for both methods is given in the Table 25.

Table 25. Calibration Sequences

Calibration Type	MD1, MD0	Calibration Sequence	Duration to Mode Bits	Duration to $\overline{\text{DRDY}}$
Self-Calibration	0, 1	Internal ZS calibration at selected gain + Internal FS calibration at selected gain	6 × 1/output rate	9 × 1/output rate + t_P
ZS System Calibration	1, 0	ZS calibration on AIN at selected gain	3 × 1/output rate	4 × 1/output rate + t_P
FS System Calibration	1, 1	FS calibration on AIN at selected gain	3 × 1/output rate	4 × 1/output rate + t_P

CIRCUIT DESCRIPTION

The AD7707 is a Σ-Δ ADC with on-chip digital filtering, intended for the measurement of wide dynamic range, low frequency signals such as those in industrial control or process control applications. It contains a Σ-Δ (or charge balancing) ADC, a calibration microcontroller with on-chip static RAM, a clock oscillator, a digital filter, and a bidirectional serial communications port. The part consumes only 320 μA of power supply current, making it ideal for battery-powered or loop-powered instruments. On-chip thin-film resistors allow ±10 V, ±5 V, 0 V to 10 V, and 0 V to 5 V high level input signals to be directly accommodated on the analog input without requiring split supplies, dc-to-dc converters, or charge pumps. This part operates with a supply voltage of 2.7 V to 3.3 V, or 4.75 V to 5.25 V.

The AD7707 contains two low level (AIN1 and AIN2) programmable-gain pseudo differential analog input channels and one high level (AIN3) single-ended input channel. For the low level input channels, the selectable gains are 1, 2, 4, 8, 16, 32, 64, and 128, allowing the part to accept unipolar signals of between 0 mV to 20 mV and 0 V to 2.5 V, or bipolar signals in the range from ±20 mV to ±2.5 V when the reference input voltage equals 2.5 V. With a reference voltage of 1.225 V, the input ranges are from 0 mV to 10 mV to 0 V to 1.225 V in unipolar mode, and from ±10 mV to ±1.225 V in bipolar mode. Note that the signals are with respect to the LOCOM input.

The high level input channel can directly accept input signals of ±10 V with respect to HICOM when operating with 5 V supplies and a reference of 2.5 V. With 3 V supplies, ±5 V can be accommodated on the AIN3 input.

The input signal to the analog input is continuously sampled at a rate determined by the frequency of the master clock, MCLK IN, and the selected gain. A charge-balancing ADC (Σ-Δ modulator) converts the sampled signal into a digital pulse train whose duty cycle contains the digital information. The programmable gain function on the analog input is also incorporated in this Σ-Δ modulator with the input sampling frequency being modified to give the higher gains. A $sinc^3$ digital low-pass filter processes the output of the Σ-Δ modulator and updates the output register at a rate determined by the first notch frequency of this filter. The output data can be read from the serial port randomly or periodically at any rate up to the output register update rate. The first notch of this digital filter (and therefore its −3 dB frequency) can be programmed via the clock register bits, FS0 to FS2. With a master clock frequency of 2.4576 MHz, the programmable range for this first notch frequency is from 10 Hz to 500 Hz, giving a programmable range for the −3 dB frequency of 2.62 Hz to 131 Hz. With a master clock frequency of 1 MHz, the programmable range for this first notch frequency is from 4 Hz to 200 Hz, giving a programmable range for the −3 dB frequency of 1.06 Hz to 52.4 Hz.

The basic connection diagram for the AD7707 is shown in Figure 12. An AD780 or REF192 precision 2.5 V reference provides the reference source for the part. On the digital side, the part is configured for 3-wire operation with $\overline{CS}$ tied to DGND. A quartz crystal or ceramic resonator provides the master clock source for the part. In most cases, it is necessary to connect capacitors on the crystal or resonator to ensure that it does not oscillate at overtones of its fundamental operating frequency. The values of capacitors can vary, depending on the manufacturer's specifications. A similar circuit is applicable for operation with 3 V supplies; in this case, a 1.225 V reference (AD1580) should be used for specified performance.

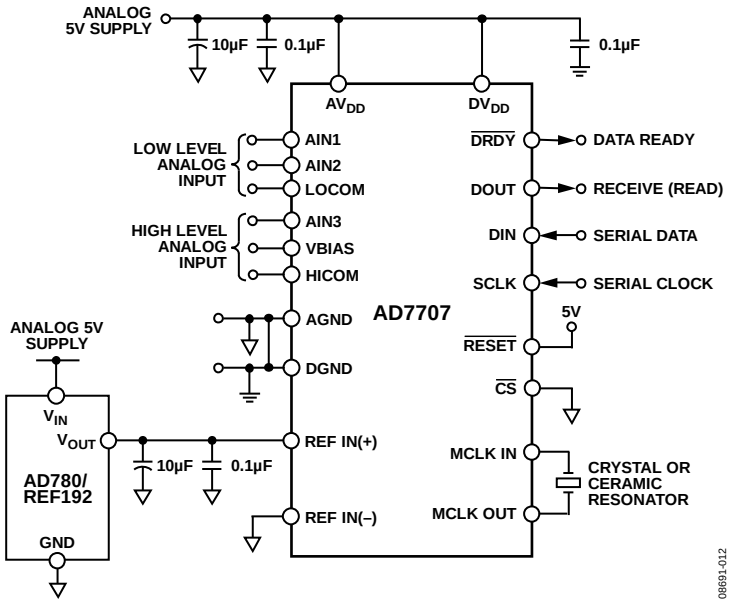


Figure 12. Basic Connection Diagram for 5 V Operation

ANALOG INPUT

ANALOG INPUT RANGES

The AD7707 contains two low level pseudo differential analog input channels, AIN1 and AIN2. These input pairs provide programmable-gain, differential input channels that can handle either unipolar or pseudo bipolar input signals. It should be noted that the bipolar input signals are referenced to the LOCOM input. The AD7707 also has a high level analog input channel AIN3, which is referenced to HICOM. Figure 13 shows the input structure on the high level input channel.

In normal 5 V operation, VBIAS is normally connected to 2.5 V and HICOM is connected to AGND. This arrangement ensures that the voltages seen internally are within the common-mode range of the buffer in buffered mode and within the supply range in unbuffered mode. This device can be programmed to operate in either buffered or unbuffered mode via the BUF bit in the setup register. Note that the signals on AIN3 are with respect to the HICOM input and not with respect to AGND or DGND.

The differential voltage seen by the AD7707 when using the high level input channel is the difference between AIN3(+) and AIN3(−) on the mux as shown in Figure 13.

$$AIN3(+) = (AIN3 + 6 \times VBIAS + V_{HICOM})/8$$

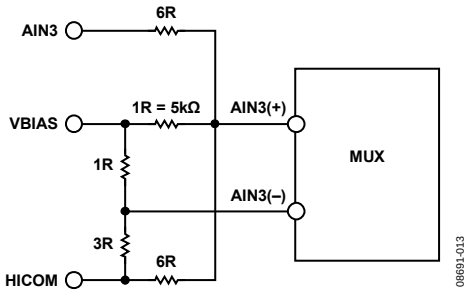


Figure 13. AIN3 Input Structure

$$AIN3(-) = V_{HICOM} + 0.75 \times (VBIAS - V_{HICOM})$$

In unbuffered mode, the common-mode range of the low level input channels is from AGND − 100 mV to AV_{DD} + 30 mV. This means that in unbuffered mode, the part can handle both unipolar and bipolar input ranges for all gains. Absolute voltages of AGND − 100 mV can be accommodated on the analog inputs without degradation in performance, but leakage current increases appreciably with increasing temperature. In buffered mode, the analog inputs can handle much larger source impedances, but the absolute input voltage range is restricted to between AGND + 50 mV to AV_{DD} − 1.5 V, which also places restrictions on the common-mode range. This means that in buffered mode, there are some restrictions on the allowable gains for bipolar input ranges. Care must be taken in setting up the common-mode voltage and input voltage range so that these limits are not exceeded; otherwise, there will be a degradation in linearity performance.

In unbuffered mode, the analog inputs look directly into the 7 pF input sampling capacitor, C_{SAMP}. The dc input leakage current in this unbuffered mode is 1 nA maximum. As a result, the analog inputs see a dynamic load that is switched at the input sample rate (see Figure 14). This sample rate depends on master clock frequency and selected gain. C_{SAMP} is charged to AIN(+) and discharged to AIN(−) every input sample cycle. The effective ml resistance of the switch, R_{SW}, is typically 7 kΩ.

C_{SAMP} must be charged through R_{SW} and any additional source impedances every input sample cycle. Therefore, in unbuffered mode, source impedances mean a longer charge time for C_{SAMP} and this may result in gain errors on the part. Table 26 shows the allowable external resistance/capacitance values, for unbuffered mode, such that no gain error to the 16-bit level is introduced on the part. Note that these capacitances are total capacitances on the analog input. This external capacitance includes 10 pF from the pins and lead frame of the device.

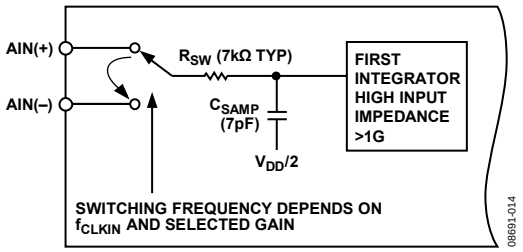


Figure 14. Unbuffered Analog Input Structure

Table 26. External R, C Combination for No 16-Bit Gain Error on Low Level Input Channels (Unbuffered Mode Only)

	External Capacitance (pF)					
Gain	**0**	**50**	**100**	**500**	**1000**	**5000**
1	368 kΩ	90.6 kΩ	54.2 kΩ	14.6 kΩ	8.2 kΩ	2.2 kΩ
2	177.2 kΩ	44.2 kΩ	26.4 kΩ	7.2 kΩ	4 kΩ	1.12 kΩ
4	82.8 kΩ	21.2 kΩ	12.6 kΩ	3.4 kΩ	1.94 kΩ	540 Ω
8 to 128	35.2 kΩ	9.6 kΩ	5.8 kΩ	1.58 Ω	880 Ω	240 Ω

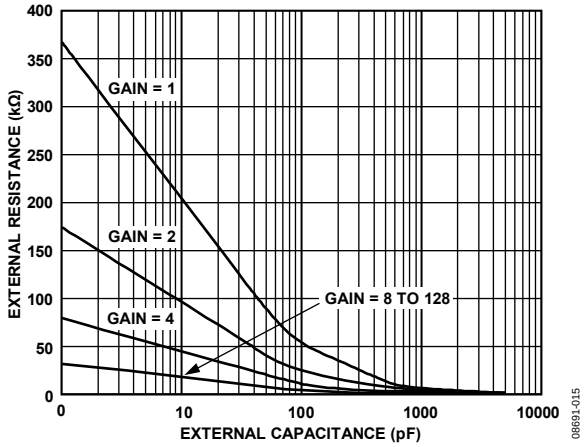


Figure 15. External R, C Combination for No 16-Bit Gain Error on Low Level Input Channels (Unbuffered Mode Only)

In buffered mode, the analog inputs look into the high impedance inputs stage of the on-chip buffer amplifier. C_{SAMP} is charged via this buffer amplifier such that source impedances do not affect the charging of C_{SAMP}. This buffer amplifier has an offset leakage current of 1 nA. In buffered mode, large source impedances result in a small dc offset voltage developed across the source impedance, but not in a gain error.

INPUT SAMPLE RATE

The modulator sample frequency for the AD7707 remains at $f_{CLKIN}/128$ (19.2 kHz at f_{CLKIN} = 2.4576 MHz) regardless of the selected gain. However, gains greater than 1 are achieved by a combination of multiple input samples per modulator cycle and a scaling of the ratio of reference capacitor to input capacitor. As a result of the multiple sampling, the input sample rate of the device varies with the selected gain (see Table 27). In buffered mode, the input impedance is constant. In unbuffered mode, where the analog input looks directly into the sampling capacitor, the effective input impedance is $1/C_{SAMP} \times f_S$ where C_{SAMP} is the input sampling capacitance and f_S is the input sample rate.

Table 27. Input Sampling Frequency vs. Gain

Gain	Input Sampling Frequency (f_S)
1	$f_{CLKIN}/64$ (38.4 kHz at f_{CLKIN} = 2.4576 MHz)
2	$2 \times f_{CLKIN}/64$ (76.8 kHz at f_{CLKIN} =2.4576 MHz)
4	$4 \times f_{CLKIN}/64$ (76.8 kHz at f_{CLKIN} =2.4576 MHz)
8 to 128	$8 \times f_{CLKIN}/64$ (307.2 kHz at f_{CLKIN} = 2.4576 MHz)

BIPOLAR/UNIPOLAR INPUTS

The analog inputs on the low level input channels on the AD7707 can accept either unipolar or bipolar input voltage ranges with respect to LOCOM.

The high level input channel handles true bipolar signals of ±10 V maxg k s k for guaranteed operation.

Bipolar or unipolar options are chosen by programming the $\overline{B}$/U bit of the setup register. This programs the channel for either unipolar or bipolar operation. Programming the channel for either unipolar or bipolar operation does not change any of the channel conditions, it simply changes the data output coding and the points on the transfer function where calibrations occur. In unipolar operation, the output coding is straight binary. In bipolar mode, the output coding is offset binary.

REFERENCE INPUT

The AD7707 reference inputs, REF IN(+) and REF IN(−), provide a differential reference input capability. The common-mode range for these differential inputs is from GND to AV_{DD}. The nominal reference voltage, V_{REF} REF IN(+) − REF IN(−), for specified operation is +2.5 V for the AD7707 operated with an AV_{DD} of 5 V and 1.225 V for the AD7707 operated with an AV_{DD} of 3 V. The part is functional with V_{REF} voltages down to 1 V, but with degraded performance because the LSB size is smaller. REF IN(+) must always be greater than REF IN(−) for correct operation of the AD7707.

Both reference inputs provide a high impedance, dynamic load similar to the analog inputs in unbuffered mode. The maximum dc input leakage current is ±1 nA over temperature, and source resistance may result in gain errors on the part. In this case, the sampling switch resistance is 5 kΩ typical and the reference capacitor (C_{REF}) varies with gain. The sample rate on the reference inputs is $f_{CLKIN}/64$ and does not vary with gain. For gains of 1 and 2, C_{REF} is 8 pF; for a gain of 16, it is 5.5 pF; for a gain of 32, it is 4.25 pF; for a gain of 64, it is 3.625 pF; and for a gain of 128, it is 3.3125 pF.

The output noise performance outlined in Table 7 through Table 13 is for an analog input of 0 V, which effectively removes the effect of noise from the reference. To obtain the same noise performance as shown in the noise tables over the full input range requires a low noise reference source for the AD7707. If the reference noise in the bandwidth of interest is excessive, it degrades the performance of the AD7707. In bridge transducer applications where the reference voltage for the ADC is derived from the excitation voltage, the effect of the noise in the excitation voltage is removed because the application is ratiometric. Recommended reference voltage sources for the AD7707 with an AV_{DD} of 5 V include the AD780, REF43, and REF192, and the recommended reference sources for the AD7707 operated with an AV_{DD} of 3 V include the AD589 and AD1580. It is generally recommended to decouple the output of these references to further reduce the noise level.

DIGITAL FILTERING

The AD7707 contains an on-chip* low-pass digital filter that processes the output of the part's Σ-Δ modulator. Therefore, the part not only provides the analog-to-digital conversion function but also provides a level of filtering. There are a number of system differences when the filtering function is provided in the digital domain rather than the analog domain and the user should be aware of these.

First, because digital filtering occurs after the ADC process, it can remove noise injected during the conversion process. Analog filtering cannot do this. Also, the digital filter can be made programmable far more readily than an analog filter. Depending on the digital filter design, this gives the user the capability of programming cutoff frequency and output update rate.

On the other hand, analog filtering can remove noise superimposed on the analog signal before it reaches the ADC. Digital filtering cannot do this and noise peaks riding on signals near full scale have the potential to saturate the analog modulator and digital filter, even though the average value of the signal is within limits. To alleviate this problem, the AD7707 has overrange headroom built into the Σ-Δ modulator and digital filter, which allows overrange excursions of 5% above the analog input range. If noise signals are larger than this, consideration should be given to analog input filtering, or to reducing the input channel voltage so that its full scale is half that of the analog input channel full scale. This provides an overrange capability greater than 100% at the expense of reducing the dynamic range by one bit (50%).

In addition, the digital filter does not provide any rejection at integer multiples of the digital filter's sample frequency. However, the input sampling on the part provides attenuation at multiples of the digital filter's sampling frequency so that the unattenuated bands actually occur around multiples of the sampling frequency, f_S (as defined in Table 27). Thus, the unattenuated bands occur at $n \times f_S$ (where n = 1, 2, 3…). At these frequencies, there are frequency bands of $\pm f_{3\,dB}$ width ($f_{3\,dB}$ is the cutoff frequency of the digital filter) where noise passes unattenuated to the output.

FILTER CHARACTERISTICS

The AD7707's digital filter is a low-pass filter with a $(\sin x/x)^3$ response (also called sinc^3). The transfer function for this filter is described in the z domain by:

$$H(z) = \left| \frac{1}{N} \times \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3$$

and in the frequency domain by:

$$H(f) - \left| \frac{1}{N} \times \frac{SIN(N \times \pi \times f / f_S)}{SIN(\pi \times f / f_S} \right|^3$$

where N is the ratio of the modulator rate to the output rate.

Phase response:

$$\angle H = -3\,\pi\,(N-2) \times f / f_S \; Rad$$

Figure 16 shows the filter frequency response for a cutoff frequency of 2.62 Hz, which corresponds to a first filter notch frequency of 10 Hz. The plot is shown from dc to 65 Hz. This response is repeated at either side of the digital filter's sample frequency and at either side of multiples of the filter's sample frequency.

The response of the filter is similar to that of an averaging filter, but with a sharper roll-off. The output rate for the digital filter corresponds with the positioning of the first notch of the filter's frequency response. Thus, for the plot of Figure 16 where the output rate is 10 Hz, the first notch of the filter is at 10 Hz. The notches of this $(\sin x/x)^3$ filter are repeated at multiples of the first notch. The filter provides attenuation of better than 100 dB at these notches.

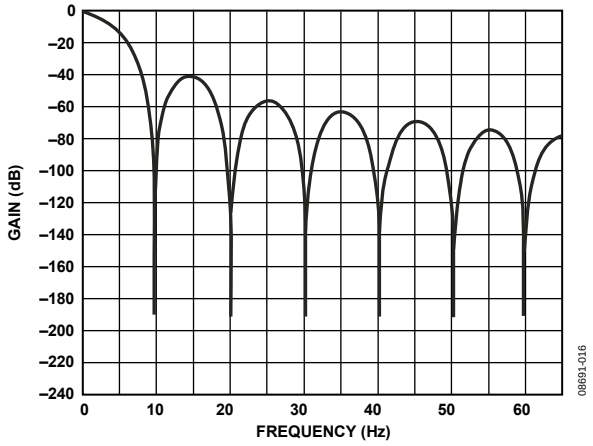


Figure 16. Frequency Response of AD7707 Filter

Simultaneous 50 Hz and 60 Hz rejection is obtained by placing the first notch at 10 Hz. Operating with an update rate of 10 Hz places notches at both 50 Hz and 60 Hz giving better than 100 dB rejection at these frequencies.

The cutoff frequency of the digital filter is determined by the value loaded to Bit FS0 to Bit FS2 in the clock register. Programming a different cutoff frequency via FS0, FS1, and FS2 does not alter the profile of the filter response; it changes the frequency of the notches. The output update of the part and the frequency of the first notch correspond.

Because the AD7707 contains this on-chip, low-pass filtering, a settling time is associated with step function inputs and data on the output will be invalid after a step change until the settling time has elapsed. The settling time depends upon the output rate chosen for the filter. The settling time of the filter to a full-scale step input can be up to four times the output data period. For a synchronized step input (using the FSYNC function), the settling time is three times the output data period.

POSTFILTERING

The on-chip modulator provides samples at a 19.2 kHz output rate with f_{CLKIN} at 2.4576 MHz. The on-chip digital filter decimates these samples to provide data at an output rate that corresponds to the programmed output rate of the filter. Because the output data rate is higher than the Nyquist criterion, the output rate for a given bandwidth satisfies most application requirements. There may, however, be some applications that require a higher data rate for a given bandwidth and noise performance. Applications that need this higher data rate require some postfiltering following the digital filter of the AD7707.

For example, if the required bandwidth is 7.86 Hz, but the required update rate is 100 Hz, the data can be taken from the AD7707 at the 100 Hz rate, giving a −3 dB bandwidth of 26.2 Hz. Postfiltering can be applied to this to reduce the bandwidth and output noise, to the 7.86 Hz bandwidth level, while maintaining an output rate of 100 Hz.

Postfiltering can also be used to reduce the output noise from the device for bandwidths below 2.62 Hz. At a gain of 128 and a bandwidth of 2.62 Hz, the output rms noise is 450 nV. This is essentially device noise or white noise* and because the input is chopped, the noise has a primarily flat frequency response. By reducing the bandwidth below 2.62 Hz, the noise in the resultant pass band can be reduced. A reduction in bandwidth by a factor of 2 results in a reduction of approximately 1.25 in the output rms noise. This additional filtering results in a longer settling time.

ANALOG FILTERING

The digital filter does not provide any rejection at integer multiples of the modulator sample frequency, as previously outlined. However, due to the AD7707's high oversampling ratio, these bands occupy only a small fraction of the spectrum and most broadband noise is filtered. This means that the analog filtering requirements in front of the AD7707 are considerably reduced vs. a conventional converter with no on-chip filtering. In addition, because the part's common-mode rejection performance of 100 dB extends out to several kHz, common-mode noise in this frequency range is substantially reduced.

Depending on the application, however, it may be necessary to provide attenuation prior to the AD7707 to eliminate unwanted frequencies from these bands, which the digital filter will pass. It may also be necessary in some applications to provide analog filtering in front of the AD7707 to ensure that differential noise signals outside the band of interest do not saturate the analog modulator.

If passive components are placed in front of the AD7707 in unbuffered mode, care must be taken to ensure that the source impedance is low enough not to introduce gain errors in the system. This significantly limits the amount of passive antialiasing filtering, which can be provided in front of the AD7707 when it is used in unbuffered mode. However, when the part is used in buffered mode, large source impedances simply result in a small dc offset error (a 10 kΩ source resistance causes an offset error of less than 10 μV). Therefore, if the system requires any qge l gdg+ cant source impedances to provide passive analog dgjrcpg l e g l front of the AD7707, it is recommended that the n_pr `c mncp_rcb in buffered mode.

CALIBRATION

The AD7707 provides a number of calibration options that can be programmed via the MD1 and MD0 bits of the setup register. The different calibration options are outlined in the Setup Register (RS2, RS1, RS0 = 0, 0, 1); Power-On/Reset Status: 0x01 section and the Calibration Sequences section. A calibration cycle can be initiated at any time by writing to these bits of the setup register. Calibration on the AD7707 removes offset and gain errors from the device. A calibration routine should be initiated on the device whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the selected gain, filter notch, or bipolar/unipolar input range.

The AD7707 offers self-calibration and system calibration facilities. For full calibration to occur on the selected channel, the on-chip microcontroller must record the modulator output for two different input conditions. These are zero-scale and full-scale points. These points are derived by performing a conversion on the different input voltages provided to the input of the modulator during calibration. As a result, the accuracy of the calibration can only be as good as the noise level that it provides in normal mode. The result of the zero-scale calibration conversion is stored in the zero-scale calibration register whereas the result of the full-scale calibration conversion is stored in the full-scale calibration register. With these readings, the microcontroller can calculate the offset and the gain slope for the input-to-output transfer function of the converter.

SELF-CALIBRATION

A self-calibration is initiated on the AD7707 by writing the appropriate values (0, 1) to the MD1 and MD0 bits of the setup register. In the self-calibration mode with a unipolar input range, the zero-scale point used in determining the calibration coefficients is with the inputs of the differential pair internally shorted on the part (that is, AIN1 = LOCOM = internal bias voltage in the case of the AD7707. The PGA is set for the selected gain (as per the G2, G1, and G0 bits in the setup register) for this zero-scale calibration conversion. The full-scale calibration conversion is performed at the selected gain on an internally-generated voltage of V_{REF}/selected gain.

The duration time for the calibration is 6 × 1/output rate. This is made up of 3 × 1/output rate for the zero-scale calibration and 3 × 1/output rate for the full-scale calibration. At this time, the MD1 and MD0 bits in the setup register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 9 × 1/output rate. This is made up of 3 × 1/output rate for the zero-scale calibration, 3 × 1/output rate for the full-scale calibration, 3 × 1/output rate for a conversion on the analog input, and some overhead to correctly set up the coefficients. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command write to the setup register, it may take up to one modulator cycle (MCLK IN/ 128) before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit is written to the setup register in the calibration command.

For bipolar input ranges in the self-calibrating mode, the sequence is very similar to that just outlined. In this case, the two points are exactly the same as in the previous case but because the part is configured for bipolar operation, the shorted inputs point is actually midscale of the transfer function.

Errors due to resistor mismatch in the attenuator on the high level input channel AIN3 are not removed by a self-calibration.

SYSTEM CALIBRATION

System calibration allows the AD7707 to compensate for system gain and offset errors as well as its own internal errors. System calibration performs the same slope factor calculations as self-calibration, but uses voltage values presented by the system to the AIN inputs for the zero-scale and full-scale points. Full system calibration requires a two-step process, a ZS system calibration followed by an FS system calibration.

For a full system calibration, the zero-scale point must be presented to the converter first. It must be applied to the converter before the calibration step is initiated, and remain stable until the step is complete. Once the system zero-scale voltage has been set up, a ZS system calibration is then initiated by writing the appropriate values (1, 0) to the MD1 and MD0 bits of the setup register. The zero-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/output rate. At this time, the MD1 and MD0 bits in the setup register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 4 × 1/output rate as the part performs a normal conversion on the analog input voltage before $\overline{\text{DRDY}}$ goes low. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command write to the qetup pegister, it may take up to one modulator cycle (MCLK IN/128) before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit is written to the setup register in the calibration command.

After the zero-scale point is calibrated, the full-scale point is applied to the analog input and the second step of the calibration process is initiated by again writing the appropriate values (1, 1) to MD1 and MD0. Again, the full-scale voltage must be set up before the calibration is initiated and it must remain stable throughout the calibration step. The full-scale system calibration is performed at the selected gain. The duration of the calibration is 3 × 1/output rate. At this time, the MD1 and

MD0 bits in the setup register return to 0, 0. This gives the earliest indication that the calibration sequence is complete. The $\overline{\text{DRDY}}$ line goes high when calibration is initiated and does not return low until there is a valid new word in the data register. The duration time from the calibration command being issued to $\overline{\text{DRDY}}$ going low is 4 × 1/output rate as the part performs a normal conversion on the analog input voltage before $\overline{\text{DRDY}}$ goes low. If $\overline{\text{DRDY}}$ is low before (or goes low during) the calibration command write to the setup register, it may take up to one modulator cycle (MCLK IN/128) before $\overline{\text{DRDY}}$ goes high to indicate that calibration is in progress. Therefore, $\overline{\text{DRDY}}$ should be ignored for up to one modulator cycle after the last bit is written to the setup register in the calibration command.

In the unipolar mode, the system calibration is performed between the two endpoints of the transfer function; in the bipolar mode, it is performed between midscale (zero differential voltage) and positive full scale.

The fact that the system calibration is a two-step calibration offers another feature. After the sequence of a full system calibration has been completed, additional offset or gain calibrations can be performed by themselves to adjust the system zero reference point or the system gain. Calibrating one of the parameters, either system offset or system gain, does not affect the other parameter.

System calibration can also be used to remove any errors from source impedances on the analog input when the part is used in unbuffered mode. A simple R, C antialiasing filter on the front end may introduce a gain error on the analog input voltage, but the system calibration can be used to remove this error.

SPAN AND OFFSET LIMITS ON THE LOW LEVEL INPUT CHANNELS, AIN1 AND AIN2

Whenever a system calibration mode is used, there are limits on the amount of offset and span that can be accommodated. The overriding requirement in determining the amount of offset and gain that can be accommodated by the part is the requirement that the positive full-scale calibration limit is <1.05 × V_{REF}/gain. This allows the input range to go 5% above the nominal range. The built-in headroom in the AD7707's analog modulator ensures that the part will still operate correctly with a positive full-scale voltage that is 5% beyond the nominal.

The input span in both the unipolar and bipolar modes has a minimum value of 0.8 × V_{REF}/gain and a maximum value of 2.1 × V_{REF}/gain. However, the span (which is the difference between the bottom of the AD7707's input range and the top of its input range) has to take into account the limitation on the positive full-scale voltage. The amount of offset that can be accommodated depends on whether the unipolar or bipolar mode is being used. Once again, the offset has to take into account the limitation on the positive full-scale voltage. In unipolar mode, there is considerable flexibility in handling negative offsets. In both unipolar and bipolar modes, the range of positive offsets that can be handled by the part depends on the selected span. Therefore, in determining the limits for system zero-scale and full-scale calibrations, the user must ensure that the offset range plus the span range does exceed 1.05 × V_{REF}/gain. This is best illustrated with the following examples.

If the part is used in unipolar mode with a required span of 0.8 × V_{REF}/gain, the offset range the system calibration can handle is from −1.05 × V_{REF}/gain to +0.25 × V_{REF}/gain. If the part is used in unipolar mode with a required span of V_{REF}/gain, the offset range the system calibration can handle is from −1.05 × V_{REF}/gain to +0.05 × V_{REF}/gain. Similarly, if the part is used in unipolar mode and required to remove an offset of 0.2 × V_{REF}/gain, the span range the system calibration can handle is 0.85 × V_{REF}/gain.

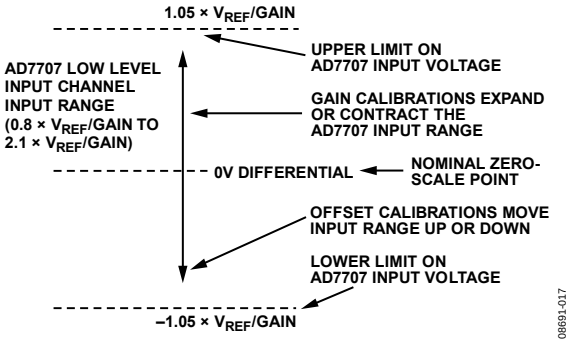


Figure 17. Span and Offset Limits for Low Level Input Channels, AIN1 and AIN2

If the part is used in bipolar mode with a required span of ±0.4 × V_{REF}/gain, the offset range the system calibration can handle is from −0.65 × V_{REF}/gain to +0.65 × V_{REF}/gain. If the part is used in bipolar mode with a required span of ±V_{REF}/gain, then the offset range that the system calibration can handle is from −0.05 × V_{REF}/gain to +0.05 × V_{REF}/gain. Similarly, if the part is used in bipolar mode and required to remove an offset of ±0.2 × V_{REF}/gain, the span range the system calibration can handle is ±0.85 × V_{REF}/gain. Figure 17 shows a graphical representation of the span and offset limits for the low level input channels.

SPAN AND OFFSET LIMITS ON THE HIGH LEVEL INPUT CHANNEL AIN3

The exact same reasoning sqcb for low level input channels can `c applied to the high level input channel. When using the high level channel, the attenuator provides an attenuation factor of 8. All span and offset limits should be multiplied by a factor of 8. Therefore, the range of input span in both the unipolar and bipolar modes has a minimum value of 6.4 × V_{REF}/gain and a maximum value of 16.8 × V_{REF}/gain. The offset range plus the span range cannot exceed 8.4 × V_{REF}/gain.

POWER-UP AND CALIBRATION

On power-up, the AD7707 performs an internal reset that sets the contents of the internal registers to a known state. There are default values loaded to all registers after power-on or reset. The default values contain nominal calibration coefficients for the calibration registers. However, to ensure correct calibration for the device, a calibration routine should be performed after power-up. A calibration should be performed if the update rate or gain are changed.

The power dissipation and temperature drift of the AD7707 are low and no warm-up time is required before the initial calibration is performed. However, if an external reference is being used, this reference must stabilize before calibration is initiated. Similarly, if the clock source for the part is generated from a crystal or resonator across the MCLK pins, the start-up time for the oscillator circuit should elapse before a calibration is initiated on the part (see the Clocking and Oscillator Circuit section).

USING THE AD7707

CLOCKING AND OSCILLATOR CIRCUIT

The AD7707 requires a master clock input, which can be an external CMOS compatible clock signal applied to the MCLK IN pin with the MCLK OUT pin left unconnected. Alternatively, a crystal or ceramic resonator of the correct frequency can be connected between MCLK IN and MCLK OUT* as shown in Figure 18, in which case the clock circuit functions as an oscillator, providing the clock source for the part. The input sampling frequency, the modulator sampling frequency, the −3 dB frequency, output update rate, and calibration time are all directly related to the master clock frequency, f_{CLKIN}. Reducing the master clock frequency by a factor of 2 halves these frequencies and update rate, and doubles the calibration time. The current drawn from the DV_{DD} power supply is also related to f_{CLKIN}. Reducing f_{CLKIN} by a factor of 2 halves the DV_{DD} current but does not affect the current drawn from the AV_{DD}.

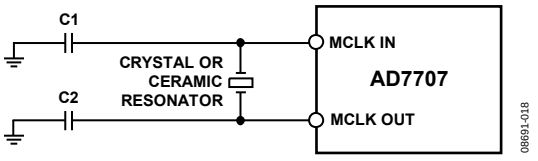


Figure 18. Crystal/Resonator Connection for the AD7707

Using the part with a crystal or ceramic resonator between the MCLK IN and MCLK OUT pins generally causes more current to be drawn from DV_{DD} than when the part is clocked from a driven clock signal at the MCLK IN pin. This is because the on-chip oscillator circuit is active in the case of the crystal or ceramic resonator. Therefore, the lowest possible current on the AD7707 is achieved with an externally applied clock at the MCLK IN pin with MCLK OUT unconnected, unloaded, and disabled.

The amount of additional current taken by the oscillator depends on a number of factors—first, the larger the value of capacitor (C1 and C2) placed on the MCLK IN and MCLK OUT pins, the larger the current consumption on the AD7707. Care should be taken not to exceed the capacitor values recommended by the crystal and ceramic resonator manufacturers to avoid consuming unnecessary current. Typical values for C1 and C2 are recommended by crystal or ceramic resonator manufacturers; these are in the range of 30 pF to 50 pF. If the capacitor values on MCLK IN and MCLK OUT are kept in this range, they do not result in any excessive current. Another factor that influences the current is the effective series resistance (ESR) of the crystal that appears between the MCLK IN and MCLK OUT pins of the AD7707. As a general rule, the lower the ESR value is, the lower the current taken by the oscillator circuit.

When operating with a clock frequency of 2.4576 MHz, there is 50 μA difference in the current between an externally applied clock and a crystal resonator when operating with a DV_{DD} of 3 V. With DV_{DD} = 5 V and f_{CLKIN} = 2.4576 MHz, the typical current increases by 250 μA for a crystal/resonator supplied clock vs. an externally applied clock. The ESR values for crystals and resonators at this frequency tend to be low and, as a result* there tends to be little difference between different crystal and resonator types.

When operating with a clock frequency of 1 MHz, the ESR value for different crystal types varies significantly. As a result, the current drain varies across crystal types. When using a crystal with an ESR of 700 Ω or when using a ceramic resonator, the increase in the typical current over an externally applied clock is 20 μA with DV_{DD} = 3 V and 200 μA with DV_{DD} = 5 V. When using a crystal with an ESR of 3 kΩ, the increase in the typical current over an externally applied clock is again 100 μA with DV_{DD} = 3 V but 400 μA with DV_{DD} = 5 V.

The on-chip oscillator circuit also has a start-up time associated with it before it is oscillating at its correct frequency and correct voltage levels. Typical start-up times with DV_{DD} = 5 V are 6 ms using a 4.9512 MHz crystal, 16 ms with a 2.4576 MHz crystal and 20 ms with a 1 MHz crystal oscillator. Start-up times are typically 20% slower when the power supply voltage is reduced to 3 V. At 3 V supplies, depending on the loading capacitances on the MCLK pins, a 1 MΩ feedback resistor may be required across the crystal or resonator to keep the start-up times around the 20 ms duration.

The AD7707's master clock appears on the MCLK OUT pin of the device. The maximum recommended load on this pin is one CMOS load. When using a crystal or ceramic resonator to generate the AD7707's clock, it may be desirable to use this clock as the clock source for the system. In this case, it is recommended that the MCLK OUT signal is buffered with a CMOS buffer before being applied to the rest of the circuit.

SYSTEM SYNCHRONIZATION

The FSYNC bit of the setup register allows the user to reset the modulator and digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, that is, when the FSYNC `gr is changed from 1 to 0.

With a 1 in the FSYNC bit of the setup register, the digital filter and analog modulator are held in a known reset state and the part is not processing any input samples. When a 0 is then written to the FSYNC bit, the modulator and filter are taken out of this reset state and the part starts to gather samples again on the next master clock edge.

The FSYNC input can also be used as a software start convert command allowing the AD7707 to be operated in a conventional converter fashion. In this mode, writing to the FSYNC bit starts conversion and the falling edge of $\overline{DRDY}$ indicates when conversion is complete. The disadvantage of this scheme is that the settling time of the filter has to be taken into account for every data register update. This means that the rate at which the data register is updated is three times slower in this mode.

Because the FSYNC bit resets the digital filter, the full settling time of 3 × 1/output rate has to elapse before there is a new word loaded to the output register on the part. If the $\overline{\text{DRDY}}$ signal is low when FSYNC goes to a 0, the $\overline{\text{DRDY}}$ signal is not reset high by the FSYNC command. This is because the AD7707 recognizes that there is a word in the data register that has not been read. The $\overline{\text{DRDY}}$ line stays low until an update of the data register takes place, at which time it goes high for 500 × t_{CLKIN} before returning low again. A read from the data register resets the $\overline{\text{DRDY}}$ signal high and it does not return low until the settling time of the filter has elapsed (from the FSYNC command) and there is a valid new word in the data register. If the $\overline{\text{DRDY}}$ line is high when the FSYNC command is issued, the $\overline{\text{DRDY}}$ line does not return low until the settling time of the filter has elapsed.

RESET INPUT

The $\overline{\text{RESET}}$ input on the AD7707 resets all the logic, the digital filter, and the analog modulator, while all on-chip registers are reset to their default state. $\overline{\text{DRDY}}$ is driven high and the AD7707 ignores all communications to any of its registers while the $\overline{\text{RESET}}$ input is low. When the $\overline{\text{RESET}}$ input returns high, the AD7707 starts to process data and $\overline{\text{DRDY}}$ returns low in 3 × 1/output rate, indicating a valid new word in the data register. However, the AD7707 operates with its default setup conditions after a $\overline{\text{RESET}}$ and it is generally necessary to set up all registers and carry out a calibration after a $\overline{\text{RESET}}$ command.

The AD7707's on-chip oscillator circuit continues to function even when the $\overline{\text{RESET}}$ input is low. The master clock signal continues to be available on the MCLK OUT pin. Therefore, in applications where the system clock is provided by the AD7707's clock, the AD7707 produces an uninterrupted master clock during $\overline{\text{RESET}}$ commands.

STANDBY MODE

The STBY bit in the communications register of the AD7707 allows the user to place the part in a power-down mode when it is not required to provide conversion results. The AD7707 retains the contents of all its on-chip registers (including the data register) while in standby mode. When released from standby mode, the part starts to process data and a new word is available in the data register in 3 × 1/output rate from when a 0 is written to the STBY bit.

The STBY bit does not affect the digital interface, nor does it affect the status of the $\overline{\text{DRDY}}$ line. If $\overline{\text{DRDY}}$ is high when the STBY bit is brought low, it remains high until there is a valid new word in the data register. If $\overline{\text{DRDY}}$ is low when the STBY bit is brought low, it remains low until the data register is updated, at which time the $\overline{\text{DRDY}}$ line returns high for 500 × t_{CLKIN} before returning low again. If $\overline{\text{DRDY}}$ is low when the part enters its standby mode (indicating a valid unread word in the data register), the data register can be read while the part is in standby. At the end of this read operation, the $\overline{\text{DRDY}}$ is reset high as normal.

Placing the part in standby mode reduces the total current to 9 μA typical with 5 V supplies and 4 μA with 3 V supplies when the part is operated from an external master clock provided this master clock is stopped. If the external clock continues to drive the MCLK IN pin in standby mode, the standby current increases to 150 μA typical with 5 V supplies and 75 μA typical with 3 V supplies. If a crystal or ceramic resonator is used as the clock source, the total current in standby mode is 400 μA typical with 5 V supplies and 90 μA with 3 V supplies. This is because the on-chip oscillator circuit continues to run when the part is in its standby mode. This is important in applications where the system clock is provided by the AD7707's clock, so that the AD7707 produces an uninterrupted master clock even when it is in its standby mode. The serial interface remains operational when in standby mode so that data can be read from the output register in standby, regardless of whether or not the master clock is stopped.

ACCURACY

Σ-Δ ADCs, like voltage–to-frequency converters (VFCs) and other integrating ADCs, do not contain any source of nonmonotonicity and inherently offer no missing codes performance. The AD7707 achieves excellent linearity by the use of high quality, on-chip capacitors that have a very low capacitance/voltage coefficient. The device also achieves low input drift through the use of chopper-stabilized techniques in its input stage. To ensure excellent performance over time and temperature, the AD7707 uses digital calibration techniques that minimize offset and gain error.

DRIFT CONSIDERATIONS

Charge injection in the analog switches and dc leakage currents at the sampling modes are the primary sources of offset voltage drift in the converter. The dc input leakage current is essentially independent of the selected gain. Gain drift within the converter depends primarily upon the temperature tracking of the internal capacitors. It is not affected by leakage currents.

Measurement errors due to offset drift or gain drift can be eliminated at any time by recalibrating the converter. Using the system calibration mode can also minimize offset and gain errors in the signal conditioning circuitry. Integral and differential linearity errors are not significantly affected by temperature changes.

POWER SUPPLIES

The AD7707 operates with power supplies between 2.7 V and 5.25 V. There is no specific power supply sequence required for the AD7707, either the AV_{DD} or the DV_{DD} supply can come up first. In normal operation, the DV_{DD} must not exceed AV_{DD} by 0.3 V. ?jrfmsef the latch-up performance of the AD7707 is good, gr is important that power is applied to the AD7707 before signals at REF IN, AIN, or the logic input pins to avoid excessive currents. If this is not possible, the current that flows in any of these pins should be limited to less than 100 mA. If separate supplies are used for the AD7707 and the system digital circuitry, the AD7707 should be powered up first. If it is not possible to guarantee this, current limiting resistors should be placed in series with the logic inputs to again limit the current. Latch-up current is greater than 100 mA.

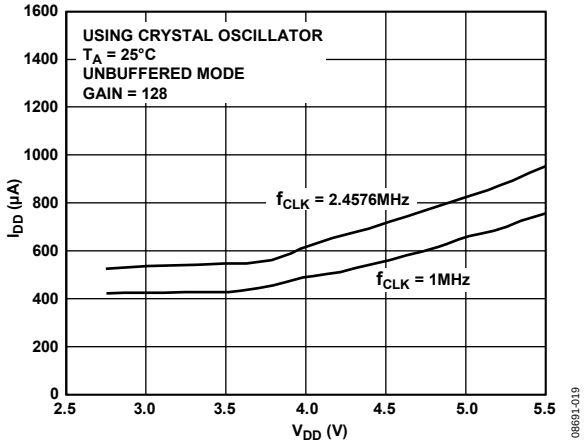


Figure 19. I_{DD} vs. Supply Voltage

SUPPLY CURRENT

The current consumption on the AD7707 is specified for supplies in the range 2.7 V to 3.3 V and in the range 4.75 V to 5.25 V. The part operates over a 2.7 V to 5.25 V supply range and the I_{DD} for the part varies as the supply voltage varies over this range. There is an internal current boost bit on the AD7707 that is set internally in accordance with the operating conditions. This affects the current drawn by the analog circuitry within these devices. Minimum power consumption is achieved when the AD7707 is operated with an f_{CLKIN} of 1 MHz or at gains of 1 to 4 with f_{CLKIN} = 2.4575 MHz as the internal boost bit is off reducing the analog current consumption. Figure 19 shows the variation of the typical I_{DD} with V_{DD} voltage for both a 1 MHz crystal oscillator and a 2.4576 MHz crystal oscillator at 25°C. The AD7707 is operated in unbuffered mode. The relationship shows that the I_{DD} is minimized by operating the part with lower AV_{DD}/DV_{DD} voltages. AI_{DD}/DI_{DD} on the AD7707 is also minimized by using an external master clock or by optimizing external components when using the on-chip oscillator circuit.

GROUNDING AND LAYOUT

Because the analog inputs and reference input are differential, most of the voltages in the analog modulator are common-mode voltages. The excellent common-mode rejection of the part removes common-mode noise on these inputs. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the modulator sampling frequency. The digital filter also removes noise from the analog and reference inputs provided rf_r those noise sources do not saturate the analog modulator. As a result, the AD7707 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7707 is so high, and the noise levels from the AD7707 so low, care must be taken with regard to grounding and layout.

The printed circuit board that houses the AD7707 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes, which can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should only be joined in one place to avoid ground loops. If the AD7707 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point, which should be established as close as possible to the AD7707.

Avoid running digital lines under the device because these may couple noise onto the analog circuitry within the AD7707. The analog ground plane should be allowed to run under the AD7707 to reduce noise coupling. The power supply lines to the AD7707 should use wide traces to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals like clocks should be shielded with digital ground to avoid radiating noise to other sections of the board and clock signals should never be run near the analog inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes while signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. All analog supplies should be decoupled with a 10 µF tantalum capacitor in parallel with 0.1 µF ceramic capacitors to AGND. To achieve the best performance from these decoupling components, they must be placed as close as possible to the device, ideally right up against the device. All logic chips should be decoupled with 0.1 µF disc ceramic capacitors to DGND.

DIGITAL INTERFACE

As previously outlined, the AD7707's programmable functions are controlled using a set of on-chip registers. Data is written to these registers via the part's serial interface and read access to the on-chip registers is also provided by this interface. All communications to the part must start with a write operation to the communications register. After power-on or $\overline{\text{RESET}}$, the device expects a write to its communications register. The data written to this register determines whether the next operation to the part is a read or a write operation and also determines to which register this read or write operation occurs. Therefore, write access to any of the other registers on the part starts with a write operation to the communications register followed by a write to the selected register. A read operation from any other register on the part (including the data register) starts with a write operation to the communications register followed by a read operation from the selected register.

The AD7707 serial interface consists of five signals, $\overline{\text{CS}}$, SCLK, DIN, DOUT, and $\overline{\text{DRDY}}$. The DIN line is used for transferring data into the on-chip registers, and the DOUT line is used for accessing data from the on-chip registers. SCLK is the serial clock input for the device and all data transfers (either on DIN or DOUT) take place with respect to this SCLK signal. The $\overline{\text{DRDY}}$ line is used as a status signal to indicate when data is ready to be read from the AD7707 data register. $\overline{\text{DRDY}}$ goes low when a new data word is available in the output register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. $\overline{\text{CS}}$ is used to select the device. It can be used to decode the AD7707 in systems where a number of parts are connected to the serial bus.

Figure 20 and Figure 21 show timing diagrams for interfacing to the AD7707 with $\overline{\text{CS}}$ used to decode the part. Figure 20 is for a read operation from the AD7707's output shift register whereas Figure 21 shows a write operation to the input shift register. It is possible to read the same data twice from the output register even though the $\overline{\text{DRDY}}$ line returns high after the first read operation. Care must be taken, however, to ensure that the read operations have been completed before the next output update is about to take place.

The AD7707 serial interface can operate in 3-wire mode by tying the $\overline{\text{CS}}$ input low. In this case, the SCLK, DIN, and DOUT lines are used to communicate with the AD7707 and the status of $\overline{\text{DRDY}}$ can be obtained by interrogating the MSB of the communications register. This scheme is suitable for interfacing to microcontrollers. If $\overline{\text{CS}}$ is required as a decoding signal, it can be generated from a port bit. For microcontroller interfaces, it is recommended that SCLK idles high between data transfers.

The AD7707 can also be operated with $\overline{\text{CS}}$ used as a frame synchronization signal. This scheme is suitable for DSP interfaces. In this case, the first bit (MSB) is effectively clocked out by $\overline{\text{CS}}$ because $\overline{\text{CS}}$ normally occurs after the falling edge of SCLK in DSPs. The SCLK can continue to run between data transfers provided rf_r the timing numbers are obeyed.

The serial interface can be reset by exercising the $\overline{\text{RESET}}$ input on the part. It can also be reset by writing a series of 1s on the DIN input. If a Logic 1 is written to the AD7707 DIN line for at least 32 serial clock cycles, the serial interface is reset. This ensures that in 3-wire systems, if the interface is lost either via a software error or by a glitch in the system, it can be reset back to a known state. This state returns the interface to where the AD7707 is expecting a write operation to its communications register. This operation in itself does not reset the contents of any registers but because the interface was lost, the information written to any of the registers is unknown and it is advisable to set up all registers again.

Some microprocessor or microcontroller serial interfaces have a single serial data line. In this case, it is possible to connect the AD7707's DATA OUT and DATA IN lines together and connect them to the single data line of the processor. A 10 kΩ pull-up resistor should be used on this single data line. In this case, if the interface is lost, because the read and write operations share the same line, the procedure to reset it back to a known state is somewhat different than previously described. It requires a read operation of 24 serial clocks followed by a write operation* where a Logic 1 is written for at least 32 serial clock cycles to ensure that the serial interface is back into a known state.

CONFIGURING THE AD7707

The AD7707 contains six on-chip registers that the user can accesses via the serial interface. Communication with any of these registers is initiated by writing to the communications register first. Figure 22 outlines a flow diagram of the sequence used to configure all registers after a power-up or reset on the AD7707. The flowchart also shows two different read options—the first in which the $\overline{\text{DRDY}}$ pin is polled to determine when an update of the data register has taken place, the second in which the $\overline{\text{DRDY}}$ bit of the communications register is interrogated to determine if a data register update has taken place. Also included in the flowing diagram is a series of words that should be written to the registers for a particular set of operating conditions. These conditions are gain of 1, no filter sync, bipolar mode, buffer off, clock of 4.9512 MHz, and an output rate of 50 Hz.

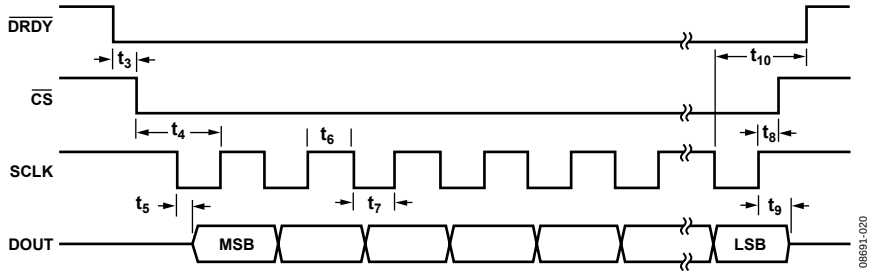


Figure 20. Read Cycle Timing Diagram

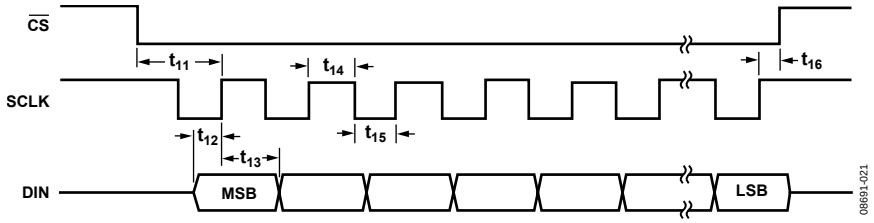


Figure 21. Write Cycle Timing Diagram

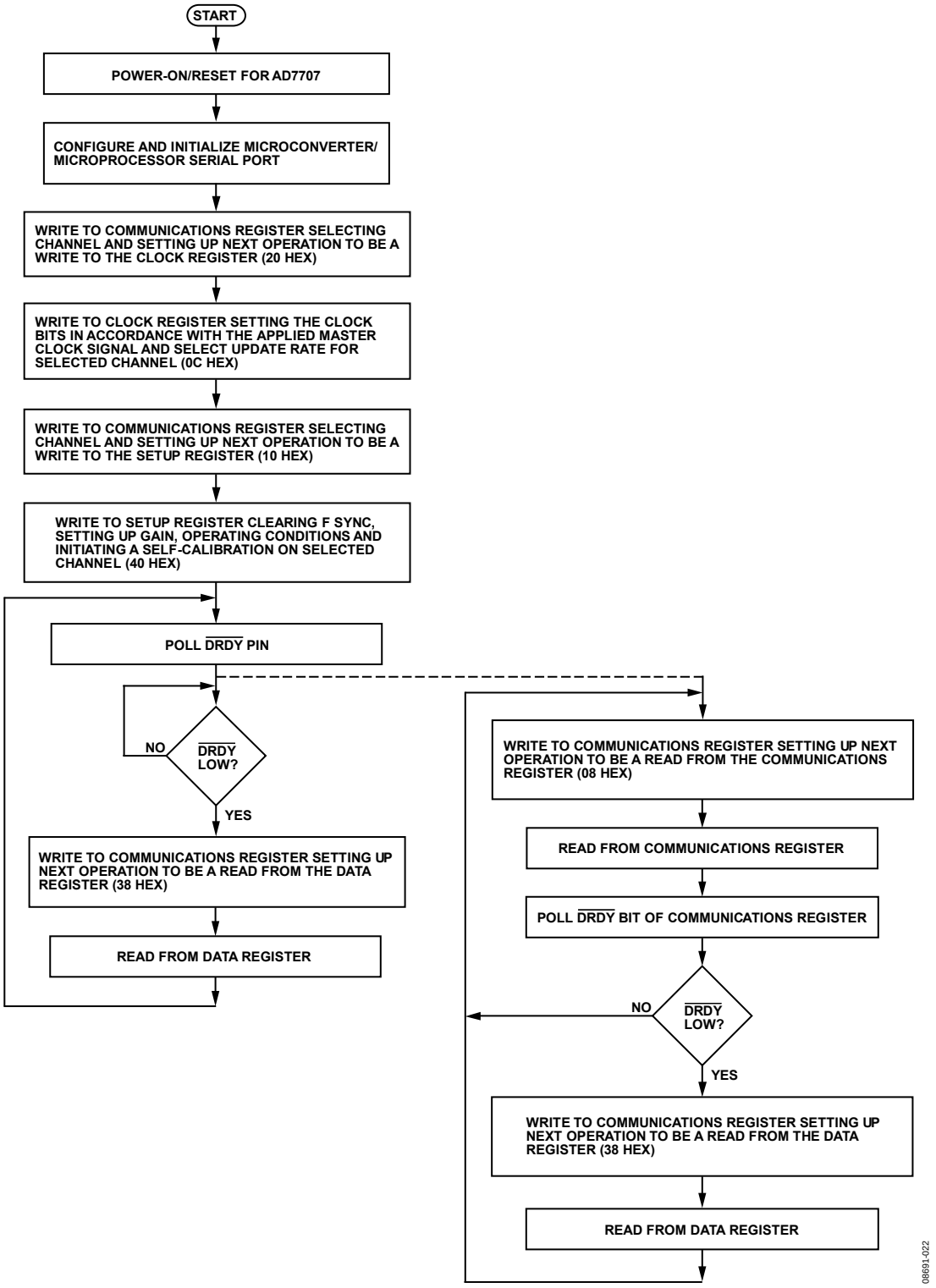


Figure 22. Flowchart for Setting Up and Reading from the AD7707

MICROCOMPUTER/MICROPROCESSOR INTERFACING

The AD7707's flexible serial interface allows for easy interface to most microcomputers and microprocessors. The flowchart of Figure 22 outlines the sequence that should be followed when interfacing a microcontroller or microprocessor to the AD7707. Figure 23 and Figure 24 show some typical interface circuits.

The serial interface on the AD7707 is capable of operating from just three wires and is compatible with SPI interface protocols. The 3-wire operation makes the part ideal for isolated systems in which minimizing the number of interface lines also minimizes the number of opto-isolators required in the system. The serial clock input is a Schmitt-triggered input to accommodate slow edges from optocouplers. The rise and fall times of other digital inputs to the AD7707 should be no longer than 1 µs.

Most of the registers on the AD7707 are 8-bit registers, which facilitates easy interfacing to the 8-bit serial ports of microcontrollers. The data register on the AD7707 is 16 bits, and the zero-scale and full-scale calibration registers are 24-bit registers but data transfers to these registers can consist of multiple 8-bit transfers to the serial port of the microcontroller. DSP processors and microprocessors generally transfer 16 bits of data in a serial data operation. Some of these processors, such as the ADSP-2105, have the facility to program the amount of cycles in a serial transfer. This allows the user to tailor the number of bits in any transfer to match the register length of the required register in the AD7707.

Even though some of the registers on the AD7707 are only eight bits in length, communicating with two of these registers in successive write operations can be handled as a single 16-bit data transfer if required. For example, if the setup register is to be updated, the processor must first write to the communications register (indicating that the next operation is a write to the setup register) and then write eight bits to the setup register. If required, this can all be performed in a single 16-bit transfer because once the eight serial clocks of the write operation to the communications register have been completed, the part immediately sets itself up for a write operation to the setup register.

AD7707+TO+68HC11 INTERFACE

Figure 23 shows an interface between the AD7707 and the 68HC11 microcontroller. The diagram shows the minimum (3-wire) interface with $\overline{CS}$ on the AD7707 hard-wired low. In this scheme, the $\overline{DRDY}$ bit of the communications register is monitored to determine when the data register is updated. An alternative scheme, which increases the number of interface lines to four, is to monitor the $\overline{DRDY}$ output line from the AD7707. The monitoring of the $\overline{DRDY}$ line can be done in two ways. First, $\overline{DRDY}$ can be connected to one of the 68HC11 port bits (such as PC0), which is configured as an input. This port bit is then polled to determine the status of $\overline{DRDY}$. The second scheme is to use an interrupt driven system, in which case the $\overline{DRDY}$ output is connected to the IRQ input of the 68HC11. For interfaces that require control of the $\overline{CS}$ input on the AD7707, one of the port bits of the 68HC11 (such as PC1), which is configured as an output, can be used to drive the $\overline{CS}$ input.

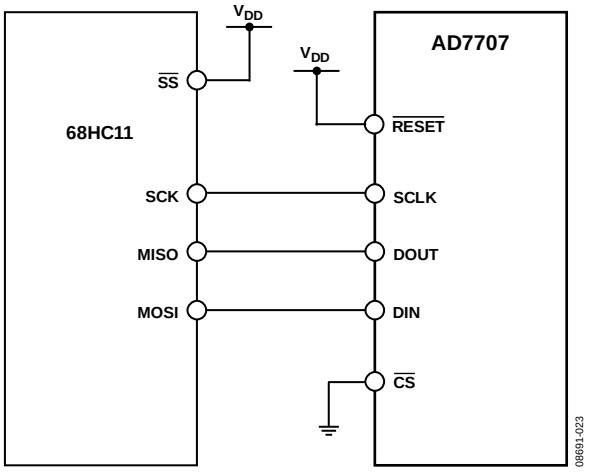


Figure 23. AD7707-to-68HC11 Interface

The 68HC11 is configured in master mode with its CPOL bit set to a Logic 1 and its CPHA bit set to a Logic 1. When the 68HC11 is configured like this, its SCLK line idles high between data transfers. The AD7707 is not capable of full duplex operation. If the AD7707 is configured for a write operation, no data appears on the DATA OUT lines even when the SCLK input is active. Similarly, if the AD7707 is configured for a read operation, data presented to the part on the DATA IN line is ignored even when SCLK is active.

Coding for an interface between the 68HC11 and the AD7707 is given in the C Code for Interfacing AD7707 to 68HC11 section. In this example, the $\overline{DRDY}$ output line of the AD7707 is connected to the PC0 port bit of the 68HC11 and is polled to determine its status.

AD7707+TO 8XC51+INTERFACE

An interface circuit between the AD7707 and the 8XC51 microcontroller is shown in Figure 24. The diagram shows the minimum number of interface connections with $\overline{CS}$ on the AD7707 hard-wired low. In the case of the 8XC51 interface, the minimum number of interconnects is just two. In this scheme, the $\overline{DRDY}$ bit of the communications register is monitored to determine when the data register is updated. The alternative scheme, which increases the number of interface lines to three, is to monitor the $\overline{DRDY}$ output line from the AD7707. The monitoring of the $\overline{DRDY}$ line can be done in two ways. First, $\overline{DRDY}$ can be connected to one of the 8XC51's port bits (such as P1.0), which is configured as an input. This port bit is then polled to determine the status of $\overline{DRDY}$. The second scheme is to use an interrupt-driven system, in which case the $\overline{DRDY}$ output is connected to the INT1 input of the 8XC51. For interfaces that require control of the $\overline{CS}$ input on the AD7707, one of the port bits of the 8XC51 (such as P1.1), which is configured as an output, can be used to drive the $\overline{CS}$ input. The 8XC51 is configured in its Mode 0 serial interface mode. Its serial interface contains a single data line. As a result, the DATA OUT and DATA IN pins of the AD7707 should be connected together with a 10 kΩ pull-up resistor. The serial clock on the 8XC51 idles high between data transfers. The 8XC51 outputs the LSB first in a write operation; however, the AD7707 expects the MSB first so the data to be transmitted must be rearranged before being written to the output serial register. Similarly, the AD7707 outputs the MSB first during a read operation; however, the 8XC51 expects the LSB first. Therefore, the data read into the serial buffer must be rearranged before the correct data word from the AD7707 is available in the accumulator.

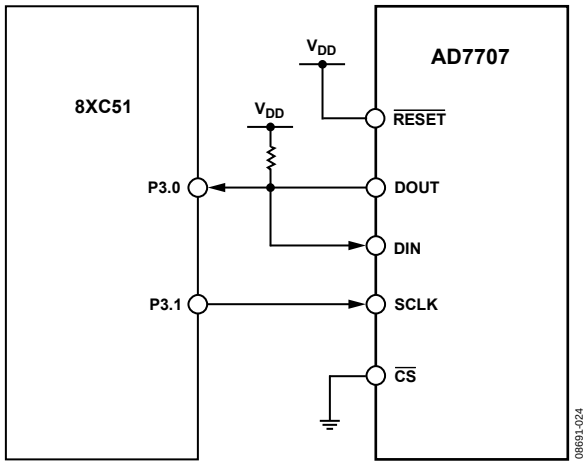


Figure 24. AD7707-to-8XC51 Interface

CODE FOR SETTING UP THE AD7707

The C Code for Interfacing AD7707 to 68HC11 section gives a set of read and write routines in C code for interfacing the 68HC11 microcontroller to the AD7707. The sample program sets up the various registers on the AD7707 and reads 1000 samples from the part into the 68HC11. The setup conditions on the part are exactly the same as those outlined for the flowchart of Figure 22. In the example code given here, the $\overline{\text{DRDY}}$ output is polled to determine if a new valid word is available in the data register.

The sequence of the events in this program are as follows:

1. Write to the communications register, selecting Channel 1 (AIN1) as the active channel and setting the next operation to be a write to the clock register.
2. Write to the clock register setting the CLKDIV bit to 1, which divides the external clock internally by two. This assumes that the external crystal is 4.9512 MHz. The update rate is selected to be 50 Hz.
3. Write to communication register selecting Channel 1 (AIN1) as the active channel and setting the next operation to be a write to the setup register.
4. Write to the setup register, setting the gain to 1, setting bipolar mode, buffer off, clearing the filter synchronization, and initiating a self-calibration.
5. Poll the $\overline{\text{DRDY}}$ output.
6. Read the data from the data register.
7. Repeat Step 5 and Step 6 until the specified number of samples have been taken from the selected channel.

C CODE FOR INTERFACING AD7707 TO 68HC11

```
/* This program has read and write routines for the 68HC11 to interface to the AD7707 and the
sample program sets the various registers and then reads 1000 samples from one channel. */
#include <math.h>
#include <io6811.h>
#define NUM_SAMPLES 1000 /* change the number of data samples */
#define MAX_REG_LENGTH 2 /* this says that the max length of a register is 2 bytes */
Writetoreg (int);
Read (int,char);
char *datapointer = store;
char store[NUM_SAMPLES*MAX_REG_LENGTH + 30];
void main ()
{
  /* the only pin that is programmed here from the 68HC11 is the /CS and this is why the PC2 bit
  of PORTC is made as an output */
char a;
DDRC = 0x04; /* PC2 is an output the rest of the port bits are inputs */
PORTC | = 0x04; /* make the /CS line high */
Writetoreg (0x20); /* Active Channel is AIN1/LOCOM, next operation as write to the clock
register */
Writetoreg (0x18); /* master clock enabled, 4.9512 MHz Clock, set output rate to 50 Hz*/
Writetoreg (0x10); /* Active Channel is AIN1/LOCOM, next operation as write to the setup
register */
Writetoreg (0x40); /* gain = 1, bipolar mode, buffer off, clear FSYNC and perform a Self
Calibration*/
while (PORTC and 0x10); /* wait for /DRDY to go low */
for (a=0;a<NUM_SAMPLES;a++);
  {
  Writetoreg (0x38); /*set the next operation for 16 bit read from the data register */
  Read (NUM_SAMPES,2);
  }
}
```

```
Writetoreg (int byteword);
{
int q;
SPCR = 0x3f;
SPCR = 0X7f; /* this sets the WiredOR mode (DWOM=1), Master mode (MSTR=1), SCK idles high
(CPOL=1), /SS can be low always (CPHA=1), lowest clock speed (slowest speed which is master
clock /32) */
DDRD = 0x18; /* SCK, MOSI outputs */
q = SPSR;
q = SPDR; /* the read of the status register and of the data register is needed to clear the
interrupt which tells the user that the data
transfer is complete */
PORTC &= 0xfb; /* /CS is low */
SPDR = byteword; /* put the byte into data register */
while (! (SPSR & 0x80)); /* wait for /DRDY to go low */
PORTC |= 0x4; /* /CS high */
}
Read (int amount, int reglength)
{
int q;
SPCR = 0x3f;
SPCR = 0x7f; /* clear the interrupt */
DDRD = 0x10; /* MOSI output, MISO input, SCK output */
while (PORTC & 0x10); /* wait for /DRDY to go low */
PORTC & 0xfb ; /* /CS is low */
for (b=0;b<reglength;b++)
  {
  SPDR = 0;
  while (! (SPSR & 0x80)); /* wait until port is ready before reading */
  *datapointer++=SPDR; /* read SPDR into store array via datapointer */
  }
PORTC|=4; /* /CS is high */
}
```

APPLICATIONS INFORMATION

The AD7707 provides a low cost, high resolution analog-to-digital function with two low level input channels and one high level input channel. Because the analog-to-digital function is provided by a Σ-Δ architecture, it makes the part more immune to noisy environments, thus making the part ideal for use in industrial and process control applications. It also provides a programmable gain amplifier, a digital filter and calibration options. Thus, it provides far more system level functionality than off-the-shelf integrating ADCs without the disadvantage of having to supply a high quality integrating capacitor. In addition, using the AD7707 in a system allows the system designer to achieve a much higher level of resolution because noise performance of the AD7707 is better than that of the integrating ADCs.

The on-chip PGA allows the AD7707 to handle an analog input voltage ranges as low as 10 mV full scale with V_{REF} = 1.25 V. The pseudo differential input capability of the low level channel allows this analog input range to have an absolute value anywhere between AGND − 100 mV and AV_{DD} + 30 mV when the part is operated in unbuffered mode. It allows the user to connect the transducer directly to the input of the AD7707.

In addition, the 3-wire digital interface on the AD7707 allows data acquisition front ends to be isolated with just three wires. The AD7707 can be operated from a single 3 V or 5 V, and its low power operation ensures that very little power needs to be brought across the isolation barrier in an isolated application.

DATA ACQUISITION

Figure 25 shows a data acquisition system in which the low level input channel is used to digitize signals from a thermocouple and the high level input channel converts process control signals up to ±10 V in amplitude. This application shows the high level input channel being used to convert a number of input signals provided through an external mux controlled by the system microcontroller. Switching channels on the external multiplexer is equivalent to providing a step change on the AIN3 input. It takes three or four updates before the correct output code corresponding to the new analog input appears at the output. Therefore, when switching between channels on the external mux, the first three outputs should be ignored following the channel change, or the FSYNC bit in the setup register should be used to reset the digital filter, and ensure that the $\overline{DRDY}$ is set high until a valid result is available in the output register.

SMART VALVE/ACTUATOR CONTROL

Another area where the low power, single supply and high voltage input capability is of benefit is in smart valve and actuator control circuits. The AD7707 monitors the signal from the control valve. The controller and the AD7707 form a closed-loop control circuit. Figure 26 shows a block diagram of a smart actuator control circuit, which includes the AD7707. The AD7707 monitors the valve position via a high quality servo potentiometer whose output is ±10 V.

Similar applications for the AD7707 include smart transmitters (see Figure 27). Here, the entire smart transmitter must operate from the 4 mA to 20 mA loop.

Tolerances in the loop mean that the amount of current available to power the transmitter is as low as 3.5 mA. The AD7707 consumes only 280 μA, leaving at least 3 mA available for the rest of the transmitter. Figure 27 shows a block diagram of a smart transmitter, which includes the AD7707.

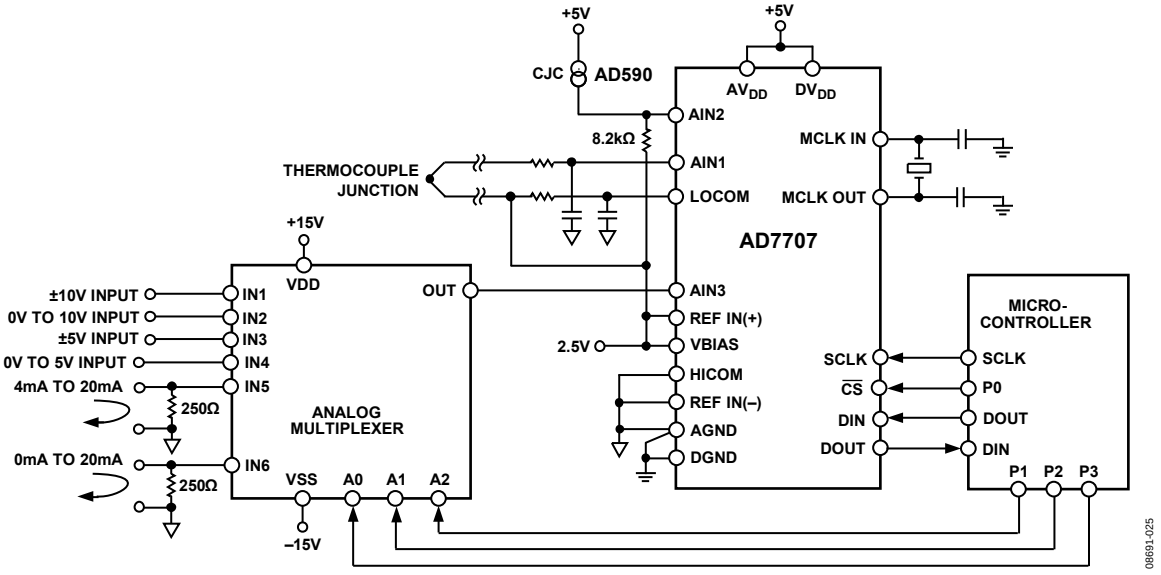


Figure 25. Data Acquisition System Using the AD7707

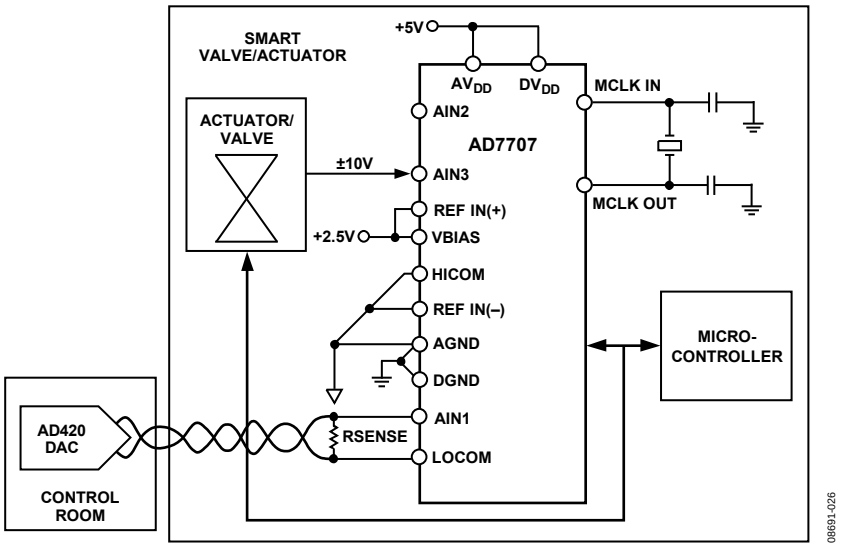


Figure 26. Smart Valve/Actuator Control Using the AD7707

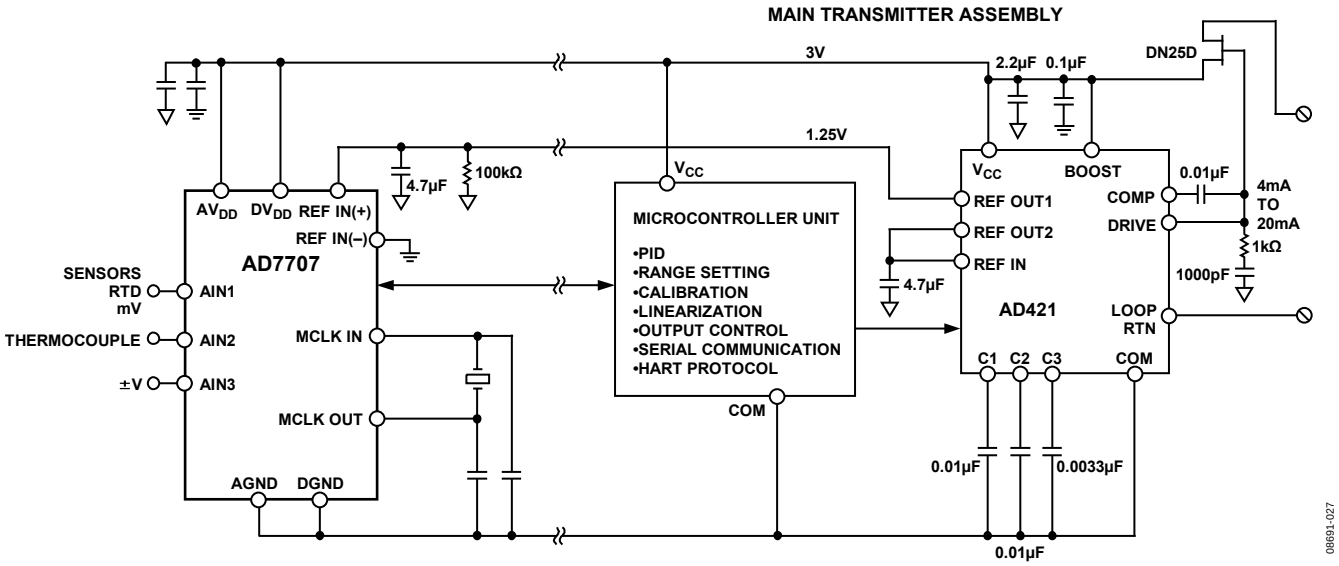


Figure 27. Smart Transmitter Using the AD7707

PRESSURE MEASUREMENT

Other typical applications for the AD7707 include temperature and pressure measurement. Figure 28 shows the AD7707 used with a pressure transducer, the BP01 from Sensym. The pressure transducer is arranged in a bridge network and gives a differential output voltage between its OUT(+) and OUT(−) terminals. With rated full-scale pressure (in this case* 300 mmHg) on the transducer, the differential output voltage is 3 mV/V of the input voltage (that is, the voltage between its IN(+) and IN(−) terminals). Assuming a 5 V excitation voltage, the full-scale output range from the transducer is 15 mV. The low level input channels are ideal for this type of low signal measurement application. The excitation voltage for the bridge is also used to generate the reference voltage for the AD7707. Therefore, variations in the excitation voltage do not introduce errors in the system. Choosing resistor values of 24 kΩ and 15 kΩ, as per Figure 28, gives a 1.92 V reference voltage for the AD7707 when the excitation voltage is 5 V.

Using the part with a programmed gain of 128 results in the full-scale input span of the AD7707 being 15 mV, which corresponds with the output span from the transducer.

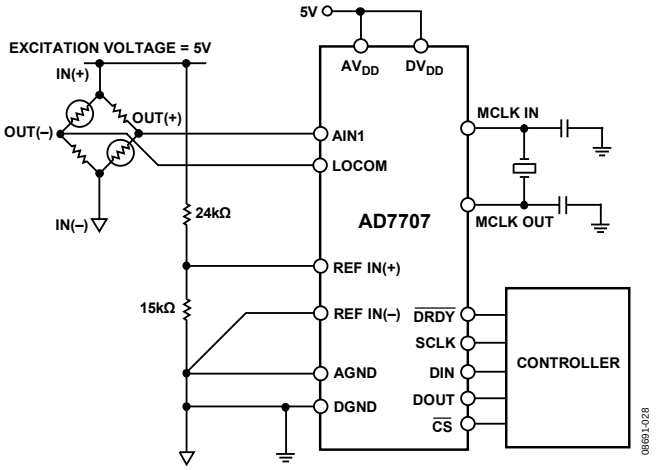


Figure 28. Pressure Measurement Using the AD7707

THERMOCOUPLE MEASUREMENT

Another application area for the AD7707 is in temperature measurement. Figure 29 outlines a connection from a thermocouple to the AD7707. In this application, the AD7707 is operated in its unbuffered mode to accommodate signals of ±100 mV on the front end. Cold conjunction compensation is implemented using the AD590 temperature transducer that produces an output current proportional to absolute temperature.

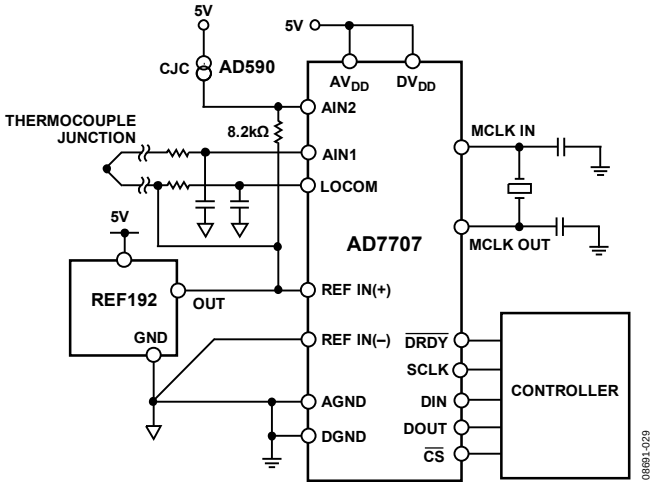


Figure 29. Thermocouple Measurement Using the AD7707

RTD MEASUREMENT

Figure 30 shows another temperature measurement application for the AD7707. In this case, the transducer is an RTD (resistive temperature device), a PT100. The arrangement is a 4-lead RTD configuration. There are voltage drops across the lead resistances, R_{L1} and R_{L4}, but these simply shift the common-mode voltage. There is no voltage drop across lead resistances R_{L2} and R_{L3} because the input current to the AD7707 is very low. The lead resistances present a small source impedance so it is generally not necessary to turn on the buffer on the AD7707.

If the buffer is required, the common-mode voltage should be set accordingly by inserting a small resistance between the bottom end of the RTD and GND of the AD7707. In the application shown, an external 400 μA current source provides the excitation current for the PT100 and generates the reference voltage dmp the AD7707 via the 6.25 kΩ resistor. Variations in the excitation current do not affect the circuit because both the input voltage and the reference voltage vary radiometrically with the excitation current. However, the 6.25 kΩ resistor must have a low temperature coefficient to avoid errors in the reference voltage over temperature.

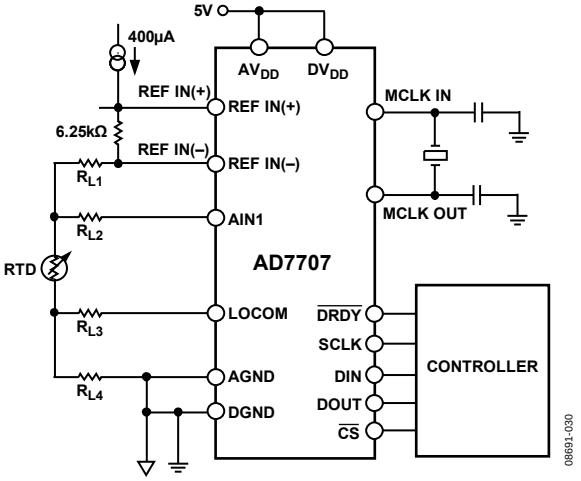


Figure 30. RTD Measurement Using the AD7707

CHART RECORDERS

Another area where both high and low level input channels are usually found is in chart recorder applications. Circular chart recorders generally have two requirements. The first utilizes the low level input channels of the AD7707 to measure inputs from thermocouples, RTDs, and pressure sensors. The second requirement is to be able to measure dc input voltage ranges up to ±10 V. The high level input channel is ideally suited to this measurement because there is no external signal conditioning required to accommodate these high level input signals.

ACCOMMODATING VARIOUS HIGH LEVEL INPUT RANGES

The high level input channel, AIN3* can accommodate input signals from −11 V to +30 V on its input. This is achieved using on-chip thin film resistors that map the signal on AIN3 into a usable range for the AD7707. The input structure is arranged so that the Σ-Δ converter sees the same impedance at its AIN(+) and AIN(−) inputs. The signal on the AIN3 input is referenced to the HICOM input and the VBIAS signal is used to adjust the common-mode voltage at the modulator input. In normal 5 V operation, VBIAS is normally connected to 2.5 V and HICOM is connected to AGND. This arrangement ensures that the voltages seen at the modulator input are within the common-mode range of the buffer.

The differential voltage, AIN, seen by the AD7707 when using the high level input channel is the difference between AIN3(+) and AIN3(−), as shown in Figure 31, and must remain within the absolute common-mode range of the modulator.

$$AIN3(+) = (AIN3 + 6 \times VBIAS + V_{HICOM})/8$$

$$AIN3(-) = 0.75 \times VBIAS + 0.25\ V_{HICOM}$$

$$AIN = (AIN3 - V_{HICOM})/8$$

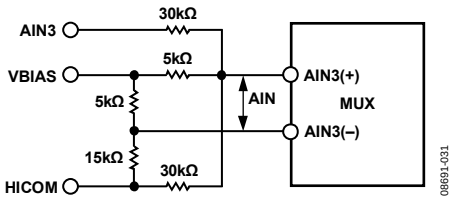


Figure 31. AIN3, High Level Input Channel Structure

The VBIAS and HICOM inputs are used to tailor the input range on the high level input channel to suit a variety of input ranges. Table 28 applies for operation with AV_{DD} = 5 V, and REF(+) − REF(−) = 2.5 V. Table 29 applies for operation with AV_{DD} = 3 V, and REF(+) − REF(−) = 1.25 V.

TYPICAL INPUT CURRENTS

When using the high level input channel, power dissipation is determined by the currents flowing in the AIN3, VBIAS, and HICOM inputs. The voltage level applied to these inputs determines whether the external source driving these inputs needs to sink or source current. Table 30 shows the currents associated with the ±10 V input range. These inputs should be driven from a low impedance source in all applications to prevent significant gain errors being introduced.

Table 28. Configuration of AD7707 vs. Input Range on AIN3 (AV_{DD} = 5 V, V_{REF} = 2.5 V)

AIN3 Range	VBIAS	HICOM	Gain	Buffered/Unbuffered	AIN Range
±10 V	2.5 V	AGND	2	Buffered/Unbuffered	1.875 V ± 1.25 V
±5 V	2.5 V	AGND	4	Buffered/Unbuffered	1.875 V ± 0.625 V
0 V to 10 V	2.5 V	AGND	2	Buffered/Unbuffered	1.875 V to 3.125 V
0 V to 20 V	AGND	AGND	1	Buffered	0 V to 2.5 V
	2.5 V	AGND	1	Buffered	1.875 V to 4.375 V
−5 V to +10 V	2.5 V	2.5 V	2	Buffered/Unbuffered	2.5 V ± 0.9375 V

Table 29. Configuration of AD7707 vs. Input Range on AIN3 (AV_{DD} = 3 V, V_{REF} = 1.25 V)

AIN3 Range	VBIAS	HICOM	Gain	BUF/UNBUF	AIN Range
±5 V	1.25 V	AGND	2	Unbuffered	0.9375 V ± 0.625 V
0 V to 10 V	1.25 V	AGND	1	Unbuffered	0.9375 V to 2.1875 V
−5 V to +10 V	1.25 V	2.5 V	1	Unbuffered	1.5625 V ± 0.9375 V
−7.5 V to +10 V	1.25 V	0 V	1	Unbuffered	0 V to 2.1875 V
±10 V	1.666 V	AGND	1	Unbuffered	1.25 V ± 1.25 V

Table 30. Typical Input Current vs. Voltage on AIN3

AIN3	VBIAS	HICOM	I (AIN3)	I (VBIAS)	I (HICOM)
−10 V	2.5 V	AGND	−354 µA	500 µA	−146 µA
0 V	2.5 V	AGND	−62 µA	250 µA	−188 µA
+10 V	2.5 V	AGND	229 µA	0 µA	−229 µA

OUTPUT NOISE FOR HIGH LEVEL INPUT CHANNEL, AIN3

5 V OPERATION

Specified high level input voltage ranges of ±10 V, ±5 V, 0 V to +10 V, and 0 V to +5 V only utilize two gain different gain settings (gains of 2 and 4) out of the eight possible settings available within the PGA. Table 31 and Table 32 show what the high level channel performance actually is over the complete range of gain settings. Table 31 shows the AD7707 output rms noise and peak-to-peak resolution for the selectable notch and −3 dB frequencies for the part, as selected by FS0, FS1, and FS2 of the clock register. The numbers are given for all input ranges with a V_{REF} of 2.5 V, HBIAS = 2.5 V, HICOM = AGND, and AV_{DD} = 5 V. These numbers are typical and are generated at an analog input voltage of 0 V for buffered mode of operation. Table 32 meanwhile shows the rms and peak-to-peak resolution for buffered mode of operation. It is important to note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in Table 31 and Table 32 are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range, but the peak-to-peak resolution is now based on half the signal range, which effectively means losing one bit of resolution.

Table 31. AIN3, Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ +5 V Unbuffered Mode

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in µV (Peak-to-Peak Resolution)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	10.90 (16)	5.10 (16)	3.52 (16)	2.62 (16)	2.34 (16)	2.34 (16)	2.34 (15)	2.30 (14)
50 Hz	13.1 Hz	31.34 (16)	15.82 (16)	9.77 (16)	6.00 (16)	5.12 (16)	5.36 (15)	4.84 (14)	4.75 (13)
60 Hz	15.72 Hz	36.74 (16)	20.36 (16)	12.29 (16)	7.33 (16)	5.84 (16)	5.65 (15)	5.1 (14)	5.3 (13)
250 Hz	65.5 Hz	690 (13)	430 (13)	212 (13)	100 (13)	42 (13)	30 (13)	18.5 (12)	13.8 (12)
500 Hz	131 Hz	4679 (10)	2350 (10)	1287 (10)	564 (10)	294 (10)	137 (10)	73 (10)	53 (10)

Table 32. AIN3, Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ +5 V Buffered Mode

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in µV (Peak-to-Peak Resolution)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	14.28 (16)	7.4 (16)	5.2 (16)	3.35 (16)	3.35 (16)	3.34 (15.5)	3.34 (15)	2.34 (14.5)
50 Hz	13.1 Hz	37.4 (16)	22.2 (16)	14.3 (16)	8.7 (16)	7.33 (15.5)	7.7 (14.5)	7.6 (13.5)	7.5 (12.5)
60 Hz	15.72 Hz	48.8 (16)	26.6 (16)	15.88 (16)	10.17 (16)	8.78 (15.5)	8.1 (14.5)	8.1 (13.5)	8.1 (12.5)
250 Hz	65.5 Hz	778 (12.5)	475 (13)	187 (13)	98 (13)	60 (12.5)	31.7 (12.5)	23 (12)	18.3 (11.5)
500 Hz	131 Hz	4716 (10.5)	2423 (10.5)	1097 (10.5)	551 (10.5)	288 (10.5)	150 (10)	81 (10)	49 (10)

3 V OPERATION

Table 33 shows the AD7707 output rms noise and peak-to-peak resolution for the selectable notch and −3 dB frequencies for the part, as selected by FS0, FS1, and FS2 of the clock register. The numbers are given for all input ranges with a V_{REF} of 1.25 V, HBIAS = 1.25 V, HICOM = AGND, and AV_{DD} = 3 V. These numbers are typical and are generated at an analog input voltage of 0 V for unbuffered mode of operation. Table 34 meanwhile shows the output rms noise and peak-to-peak resolution for buffered mode of operation with the same operating conditions as for Table 33. It is important to note that these numbers represent the resolution for which there is no code flicker. They are not calculated based on rms noise but on peak-to-peak noise. The output noise comes from two sources. The first is the electrical noise in the semiconductor devices (device noise) used in the implementation of the modulator. Secondly, when the analog input is converted into the digital domain, quantization noise is added. The device noise is at a low level and is independent of frequency. The quantization noise starts at an even lower level but rises rapidly with increasing frequency to become the dominant noise source. The numbers in Table 33 and Table 34 are given for the bipolar input ranges. For the unipolar ranges, the rms noise numbers are the same as the bipolar range but the peak-to-peak resolution is now based on half the signal range, which effectively means losing 1 bit of resolution.

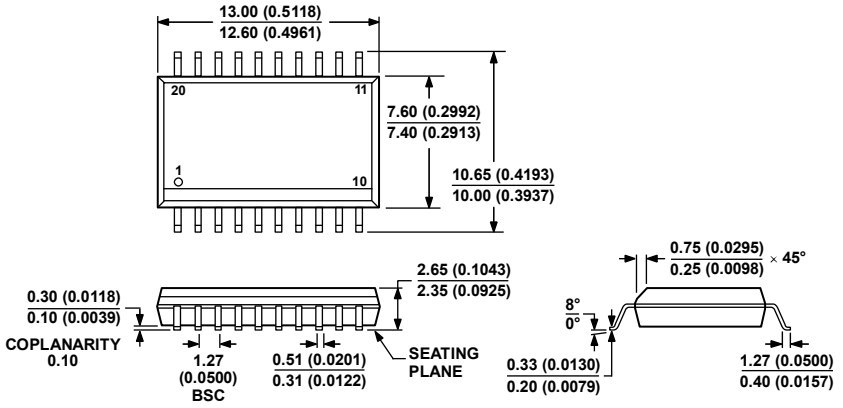
Table 33. AIN3, Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ +3 V Unbuffered Mode

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in μV (Peak-to-Peak Resolution)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	12.4 (16)	7.02 (16)	3.87 (16)	2.41 (16)	2.39 (16)	2.3 (15.5)	2.29 (14.5)	2.13 (13.5)
50 Hz	13.1 Hz	30.35 (16)	16.4 (16)	9.4 (16)	5.85 (16)	5.2 (15)	4.5 (14.5)	4.5 (13.5)	5.09 (12)
60 Hz	15.72 Hz	34.55 (16)	19.13 (16)	10.9 (16)	6 (16)	5.8 (15)	5.62 (14)	5.2 (13)	6.14 (12)
250 Hz	65.5 Hz	498 (13)	204 (13)	105 (13)	57.5 (13)	27.5 (13)	17.4 (12.5)	12.7 (12)	11.42 (11)
500 Hz	131 Hz	2266 (10.5)	1151 (10.5)	554 (10.5)	280 (10.5)	136 (10.5)	83 (10)	39 (10)	27.5 (9.5)

Table 34. AIN3, Output RMS Noise/Peak-to-Peak Resolution vs. Gain and Output Update Rate @ +3 V Buffered Mode

Filter First Notch and Output Data Rate	−3 dB Frequency	Typical Output RMS Noise in μV (Peak-to-Peak Resolution)							
		Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
MCLK IN = 2.4576 MHz									
10 Hz	2.62 Hz	14.84 (16)	8.39 (16)	5.56 (16)	3.45 (16)	3.3 (16)	3.2 (15)	3.2 (14)	3.3 (13)
50 Hz	13.1 Hz	36.1 (16)	18.8 (16)	11.5 (16)	7.5 (15.5)	7.4 (14.5)	7.43 (13.5)	6.8 (12.5)	7 (12)
60 Hz	15.72 Hz	38.8 (16)	21.55 (16)	13.39 (16)	8.5 (15.5)	8.36 (14.5)	8 (13.5)	8.2 (12.5)	7.7 (12)
250 Hz	65.5 Hz	420 (13)	194 (13)	97.6 (13)	54.5 (12.5)	30 (12.5)	22 (12)	18 (11.5)	16.7 (10.5)
500 Hz	131 Hz	2234 (10.5)	1231 (10.5)	534 (10.5)	275 (10.5)	145 (10.5)	71 (10.5)	48 (10)	31 (9.5)

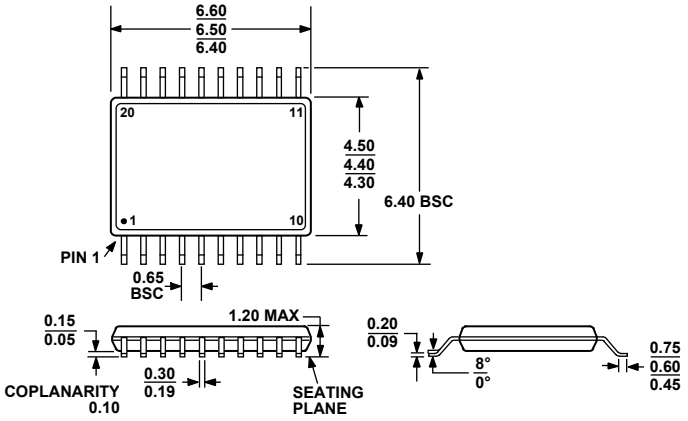
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

06-07-06-A

Figure 32. 20-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-20)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 33. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	V_{DD} Supply	Temperature Range	Package Description	Package Option
AD7707BR	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
AD7707BR-REEL	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
AD7707BRZ	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
AD7707BRZ-REEL	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
AD7707BRZ-REEL7	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Standard Small Outline Package [SOIC_W]	RW-20
AD7707BRU	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD7707BRU-REEL7	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD7707BRUZ	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD7707BRUZ-REEL	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20
AD7707BRUZ-REEL7	2.7 V to 5.25 V	−40°C to +85°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	RU-20

[1] Z = RoHS Compliant Part.

NOTES

NOTES

D08691-0-1/10(B)

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