ANALOG DEVICES

LC^{2}MOS
5 μs 8-Bit ADC with Track/Hold

AD7575

FEATURES
Fast Conversion Time: 5 μs
On-Chip Track/Hold
Low Total Unadjusted Error: 1 LSB
Full Power Signal Bandwidth: 50 kHz
Single +5 V Supply
100 ns Data Access Time
Low Power (15 mW typ)
Low Cost
Standard 18-Lead DIPs or 20-Terminal
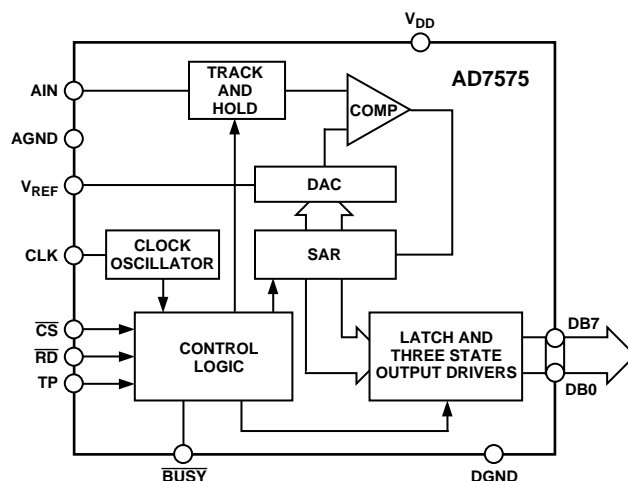 **Surface Mount Packages**

FUNCTIONAL BLOCK DIAGRAM

GENERAL DESCRIPTION
The AD7575 is a high speed 8-bit ADC with a built-in track/hold function. The successive approximation conversion technique is used to achieve a fast conversion time of 5 μs, while the built-in track/hold allows full-scale signals up to 50 kHz (386 mV/μs slew rate) to be digitized. The AD7575 requires only a single +5 V supply and a low cost, 1.23 V bandgap reference in order to convert an input signal range of 0 to 2 V_{REF}.

The AD7575 is designed for easy interfacing to all popular 8-bit microprocessors using standard microprocessor control signals ($\overline{CS}$ and $\overline{RD}$) to control starting of the conversion and reading of the data. The interface logic allows the AD7575 to be easily configured as a memory mapped device, and the part can be interfaced as SLOW-MEMORY or ROM. All data outputs of the AD7575 are latched and three-state buffered to allow direct connection to a microprocessor data bus or I/O port.

The AD7575 is fabricated in an advanced, all ion-implanted high speed Linear Compatible CMOS (LC^{2}MOS) process and is available in a small, 0.3" wide, 18-lead DIP, 18-lead SOIC or in other 20-terminal surface mount packages.

PRODUCT HIGHLIGHTS
1. Fast Conversion Time/Low Power
   The fast, 5 μs, conversion time of the AD7575 makes it suitable for digitizing wideband signals at audio and ultrasonic frequencies while retaining the advantage of low CMOS power consumption.

2. On-Chip Track/Hold
   The on-chip track/hold function is completely self-contained and requires no external hold capacitor. Signals with slew rates up to 386 mV/μs (e.g., 2.46 V peak-to-peak 50 kHz sine waves) can be digitized with full accuracy.

3. Low Total Unadjusted Error
   The zero, full-scale and linearity errors of the AD7575 are so low that the total unadjusted error at any point on the transfer function is less than 1 LSB, and offset and gain adjustments are not required.

4. Single Supply Operation
   Operation from a single +5 V supply with a low cost +1.23 V bandgap reference allows the AD7575 to be used in 5 V microprocessor systems without any additional power supplies.

5. Fast Digital Interface
   Fast interface timing allows the AD7575 to interface easily to the fast versions of most popular microprocessors such as the Z80H, 8085A-2, 6502B, 68B09 and the DSP processor, the TMS32010.

REV. B

AD7575–SPECIFICATIONS

(V_{DD} = +5 V, V_{REF} = +1.23 V, AGND = DGND = 0 V; f_{CLK} = 4 MHz external; all specifications T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	J, A Versions[1]	K, B Versions	S Version	T Version	Units	Conditions/Comments
ACCURACY						
Resolution	8	8	8	8	Bits	
Total Unadjusted Error	±2	±1	±2	±1	LSB max	
Relative Accuracy	±1	±1/2	±1	±1/2	LSB max	
Minimum Resolution for Which						
No Missing Codes Is Guaranteed	8	8	8	8	Bits max	
Full-Scale Error						
+25°C	±1	±1	±1	±1	LSB max	Full-Scale TC Is Typically 5 ppm/°C
T_{MIN} to T_{MAX}	±1	±1	±1	±1	LSB max	
Offset Error[2]						
+25°C	±1/2	±1/2	±1/2	±1/2	LSB max	Offset TC Is Typically 5 ppm/°C
T_{MIN} to T_{MAX}	±1/2	±1/2	±1/2	±1/2	LSB max	
ANALOG INPUT						
Voltage Range	0 to 2 V_{REF}	0 to 2 V_{REF}	0 to 2 V_{REF}	0 to 2 V_{REF}	Volts	1 LSB = 2 V_{REF}/256; See Figure 16
DC Input Impedance	10	10	10	10	MΩ min	
Slew Rate, Tracking	0.386	0.386	0.386	0.386	V/µs max	
SNR[3]	45	45	45	45	dB min	V_{IN} = 2.46 V p-p @ 10 kHz; See Figure 11
REFERENCE INPUT						
V_{REF} (For Specified Performance)	1.23	1.23	1.23	1.23	Volts	±5%
I_{REF}	500	500	500	500	µA max	
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{IN}, Input Current						
+25°C	±1	±1	±1	±1	µA max	V_{IN} = 0 or V_{DD}
T_{MIN} to T_{MAX}	±10	±10	±10	±10	µA max	V_{IN} = 0 or V_{DD}
C_{IN}, Input Capacitance[3]	10	10	10	10	pF max	
CLK						
V_{INL}, Input Low Voltage	0.8	0.8	0.8	0.8	V max	
V_{INH}, Input High Voltage	2.4	2.4	2.4	2.4	V min	
I_{INL}, Input Low Current	700	700	800	800	µA max	V_{INL} = 0 V
I_{INH}, Input High Current	700	700	800	800	µA max	V_{INH} = V_{DD}
LOGIC OUTPUTS						
$\overline{BUSY}$, DB0 to DB7						
V_{OL}, Output Low Voltage	0.4	0.4	0.4	0.4	V max	I_{SINK} = 1.6 mA
V_{OH}, Output High Voltage	4.0	4.0	4.0	4.0	V min	I_{SOURCE} = 40 µA
DB0 to DB7						
Floating State Leakage Current	±1	±1	±10	±10	µA max	V_{OUT} = 0 to V_{DD}
Floating State Output Capacitance[3]	10	10	10	10	pF max	
CONVERSION TIME[4]						
With External Clock	5	5	5	5	µs	f_{CLK} = 4 MHz
With Internal Clock, T_A = +25°C	5	5	5	5	µs min	Using Recommended Clock
	15	15	15	15	µs max	Components Shown in Figure 15
POWER REQUIREMENTS[5]						
V_{DD}	+5	+5	+5	+5	Volts	±5% for Specified Performance
I_{DD}	6	6	7	7	mA max	Typically 3 mA with V_{DD} = +5 V
Power Dissipation	15	15	15	15	mW typ	
Power Supply Rejection	±1/4	±1/4	±1/4	±1/4	LSB max	4.75 V ≤ V_{DD} ≤ 5.25 V

NOTES

[1]Temperature ranges are as follows:

    J, K Versions; 0°C to +70°C

    A, B Versions; –25°C to +85°C

    S, T Versions; –55°C to +125°C

[2]Offset error is measured with respect to an ideal first code transition that occurs at 1/2 LSB.

[3]Sample tested at +25°C to ensure compliance.

[4]Accuracy may degrade at conversion times other than those specified.

[5]Power supply current is measured when AD7575 is inactive i.e., when $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = logic HIGH.

Specifications subject to change without notice.

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TIMING SPECIFICATIONS[1] $(V_{DD} = +5\ V, V_{REF} = +1.23\ V, AGND = DGND = 0\ V)$

Parameter	Limit at +25°C (All Versions)	Limit at T_{MIN}, T_{MAX} (J, K, A, B Versions)	Limit at T_{MIN}, T_{MAX} (S, T Versions)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	100	100	120	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
$t_3{}^2$	100	100	120	ns max	Data Access Time after $\overline{RD}$
t_4	100	100	120	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
$t_6{}^2$	80	80	100	ns max	Data Access Time after $\overline{BUSY}$
$t_7{}^3$	10	10	10	ns min	Data Hold Time
	80	80	100	ns max	
t_8	0	0	0	ns min	$\overline{BUSY}$ to $\overline{CS}$ Delay

NOTES

[1]Timing specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 20 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8 V or 2.4 V.
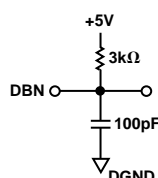
[3]t_7 is defined as the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 2.

Specifications subject to change without notice.
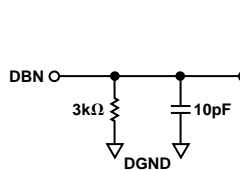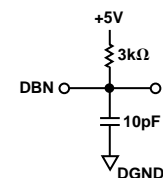
Test Circuits
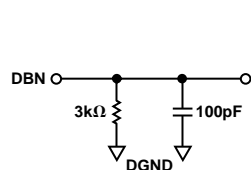
a. High-Z to V_{OH}

b High-Z to V_{OL}

Figure 1. Load Circuits for Data Access Time Test

a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Data Hold Time Test

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to AGND . . . . −0.3 V, +7 V

V_{DD} to DGND . . . . −0.3 V, +7 V

AGND to DGND . . . . −0.3 V, V_{DD}

Digital Input Voltage to DGND . . . . −0.3 V, V_{DD} + 0.3 V

Digital Output Voltage to DGND . . . . . . −0.3 V, V_{DD} + 0.3 V

CLK Input Voltage to DGND . . . . −0.3 V, V_{DD} + 0.3 V

V_{REF} to AGND . . . . −0.3 V, V_{DD}

AIN to AGND . . . . −0.3 V, V_{DD}

Operating Temperature Range

   Commercial (J, K Versions) . . . . 0°C to +70°C

   Industrial (A, B Versions) . . . . −25°C to +85°C

   Extended (S, T Versions) . . . . −55°C to +125°C

Storage Temperature Range . . . . −65°C to +150°C

Lead Temperature (Soldering, 10 sec) . . . . +300°C

Power Dissipation (Any Package) to +75°C . . . . 450 mW

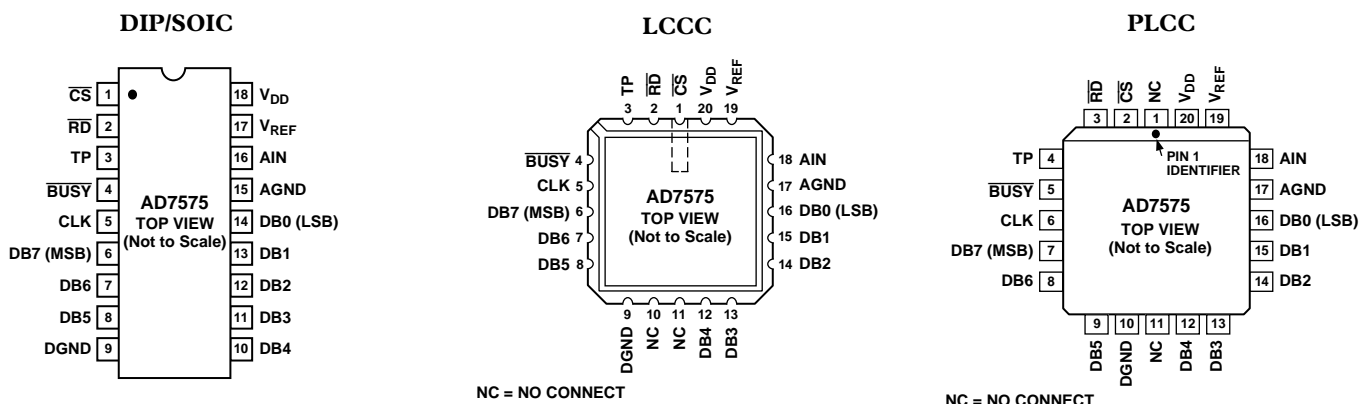Derates above +75°C by . . . . 6 mW/°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AD7575

DIP/SOIC

	AD7575 TOP VIEW (Not to Scale)	
$\overline{CS}$ 1		18 V_{DD}
$\overline{RD}$ 2		17 V_{REF}
TP 3		16 AIN
$\overline{BUSY}$ 4		15 AGND
CLK 5		14 DB0 (LSB)
DB7 (MSB) 6		13 DB1
DB6 7		12 DB2
DB5 8		11 DB3
DGND 9		10 DB4

LCCC

AD7575 TOP VIEW (Not to Scale)

Top pins: TP 3, $\overline{RD}$ 2, $\overline{CS}$ 1, V_{DD} 20, V_{REF} 19

$\overline{BUSY}$ 4 — 18 AIN
CLK 5 — 17 AGND
DB7 (MSB) 6 — 16 DB0 (LSB)
DB6 7 — 15 DB1
DB5 8 — 14 DB2

Bottom pins: DGND 9, NC 10, NC 11, DB4 12, DB3 13

NC = NO CONNECT

PLCC

AD7575 TOP VIEW (Not to Scale)

Top pins: $\overline{RD}$ 3, $\overline{CS}$ 2, NC 1, V_{DD} 20, V_{REF} 19

PIN 1 IDENTIFIER

TP 4 — 18 AIN
$\overline{BUSY}$ 5 — 17 AGND
CLK 6 — 16 DB0 (LSB)
DB7 (MSB) 7 — 15 DB1
DB6 8 — 14 DB2

Bottom pins: DB5 9, DGND 10, NC 11, DB4 12, DB3 13

NC = NO CONNECT

ORDERING GUIDE

Model[1]	Temperature Range	Relative Accuracy (LSB)	Package Options[2]
AD7575JR	0°C to +70°C	±1 max	R-18
AD7575JN	0°C to +70°C	±1 max	N-18
AD7575KN	0°C to +70°C	±1/2 max	N-18
AD7575JP	0°C to +70°C	±1 max	P-20A
AD7575KP	0°C to +70°C	±1/2 max	P-20A
AD7575AQ	–25°C to +85°C	±1 max	Q-18
AD7575BQ	–25°C to +85°C	±1/2 max	Q-18
AD7575SQ	–55°C to +125°C	±1 max	Q-18
AD7575TQ	–55°C to +125°C	±1/2 max	Q-18
AD7575SE	–55°C to +125°C	±1 max	E-20A
AD7575TE	–55°C to +125°C	±1/2 max	E-20A

NOTES
[1]To order MIL-STD-883, Class B process parts, add /883B to part number.
 Contact local sales office for military data sheet. For U.S. Standard Military
 Drawing (SMD), see DESC drawing #5962-87762.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip
 Carrier; Q = Cerdip, R = SOIC.

TERMINOLOGY
LEAST SIGNIFICANT BIT (LSB)
An ADC with 8-bits resolution can resolve 1 part in 2^8 (i.e., 256) of full scale. For the AD7575 with +2.46 V full-scale one LSB is 9.61 mV.

TOTAL UNADJUSTED ERROR
This is a comprehensive specification that includes full-scale error, relative accuracy and offset error.

RELATIVE ACCURACY
Relative Accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices measured first LSB transition point and the measured full-scale transition point.

SNR
Signal-to-Noise Ratio (SNR) is the ratio of the desired signal to the noise produced in the sampled and digitized analog signal. SNR is dependent on the number of quantization levels used in the digitization process; the more levels, the smaller the quantization noise. The theoretical SNR for a sine wave input is given by

$$SNR = (6.02\,N + 1.76)\ dB$$

where N is the number of bits in the ADC.

FULL-SCALE ERROR (GAIN ERROR)
The gain of a unipolar ADC is defined as the difference between the analog input levels required to produce the first and the last digital output code transitions. Gain error is a measure of the deviation of the actual span from the ideal span of FS – 2 LSBs.

ANALOG INPUT RANGE
With V_{REF} = +1.23 V, the maximum analog input voltage range is 0 V to +2.46 V. The output data in LSBs is related to the analog input voltage by the integer value of the following expression:

$$Data\ (LSBs) = \frac{256\,AIN}{2\,V_{REF}} + 0.5$$

SLEW RATE
Slew Rate is the maximum allowable rate of change of input signal such that the digital sample values are not in error. Slew Rate limitations may restrict the analog signal bandwidth for full-scale analog signals below the bandwidth allowed from sampling theorem considerations.
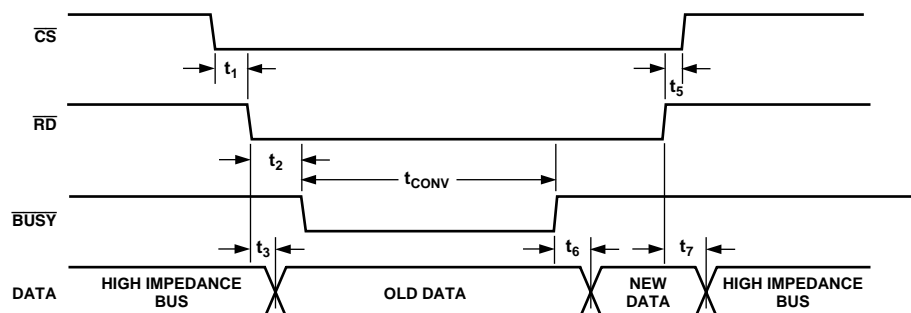
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Figure 3. Slow Memory Interface Timing Diagram

TIMING AND CONTROL OF THE AD7575
The two logic inputs on the AD7575, $\overline{CS}$ and $\overline{RD}$, control both the starting of conversion and the reading of data from the part. A conversion is initiated by bringing both of these control inputs LOW. Two interface options then exist for reading the output data from the AD7575. These are the Slow Memory Interface and ROM Interface, their operation is outlined below. It should be noted that the TP pin of the AD7575 must be hard-wired HIGH to ensure correct operation of the part. This pin is used in testing the device and should not be used as a feedthrough pin in double-sided printed circuit boards.

SLOW MEMORY INTERFACE
The first interface option is intended for use with microprocessors that can be forced into a WAIT STATE for at least 5 μs. The microprocessor (such as the 8085A) starts a conversion and is halted until the result of the conversion is read from the converter. Conversion is initiated by executing a memory READ to the AD7575 address, bringing $\overline{CS}$ and $\overline{RD}$ LOW. $\overline{BUSY}$ subsequently goes LOW (forcing the microprocessor READY input LOW), placing the processor into a WAIT state. The input signal, which had been tracked by the analog input, is held on the third falling clock edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW (see Figure 12). The AD7575 then performs a conversion on this acquired input signal value. When the conversion is complete ($\overline{BUSY}$ goes HIGH), the processor completes the memory READ and acquires the newly converted data. The timing diagram for this interface is shown in Figure 3.

*LINEAR CIRCUITRY OMITTED FOR CLARITY
SO = 0 FOR READ CYCLES
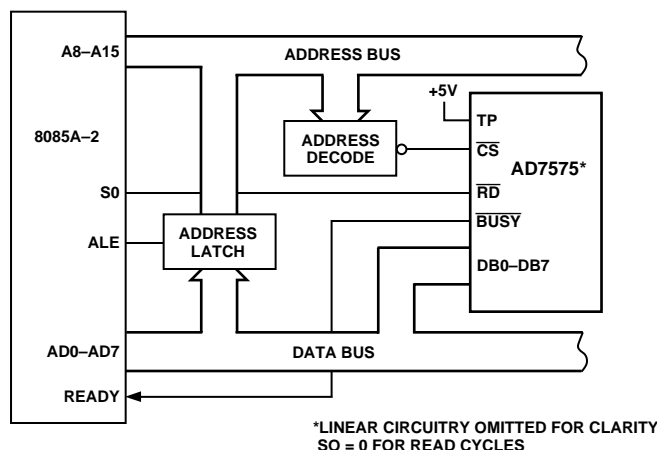
Figure 4. AD7575 to 8085A-2 Slow Memory Interface

The major advantage of this interface is that it allows the microprocessor to start conversion, WAIT, and then READ data with a single READ instruction. The fast conversion time of the AD7575 ensures that the microprocessor is not placed in a WAIT state for an excessive amount of time.

Faster versions of many processors, including the 8085A-2, test the condition of the READY input very soon after the start of an instruction cycle. Therefore, $\overline{BUSY}$ of the AD7575 must go LOW very early in the cycle for the READY input to be effective in forcing the processor into a WAIT state. When using the 8085A-2, the processor S0 status signal provides the earliest possible indication that a READ operation is about to occur. Hence, S0 (which is LOW for a READ cycle) provides the READ signal to the AD7575. The connection diagram for the AD7575 to 8085A-2 Slow Memory interface is shown in Figure 4.

ROM INTERFACE
The alternative interface option on the AD7575 avoids placing the microprocessor into a WAIT state. In this interface, a conversion is started with the first READ instruction, and the second READ instruction accesses the data and starts a second conversion. The timing diagram for this interface is shown in Figure 5. It is possible to avoid starting another conversion on the second READ (see below).

Conversion is initiated by executing a memory READ instruction to the AD7575 address, causing $\overline{CS}$ and $\overline{RD}$ to go LOW. Data is also obtained from the AD7575 during this instruction. This is old data and may be disregarded if not required. $\overline{BUSY}$ goes LOW, indicating that conversion is in progress, and returns HIGH when conversion is complete. Once again, the input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ have gone LOW.

The $\overline{BUSY}$ line may be used to generate an interrupt to the microprocessor or monitored to indicate that conversion is complete. The processor then reads the newly-converted data. Alternatively, the delay between the convert start (first READ instruction) and the data READ (second READ instruction) must be at least as great as the AD7575 conversion time. For the AD7575 to operate correctly in the ROM interface mode, $\overline{CS}$ and $\overline{RD}$ should not go LOW before $\overline{BUSY}$ returns HIGH.

Normally, the second READ instruction starts another conversion as well as accessing the output data. However, if $\overline{CS}$ and $\overline{RD}$ are brought LOW within one external clock period of $\overline{BUSY}$ going HIGH, a second conversion does not occur.
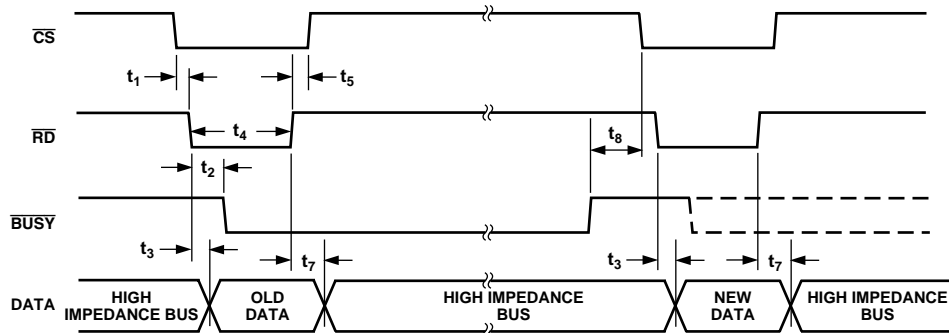
AD7575

Figure 5. ROM Interface Timing Diagram

Figures 6 and 7 show connection diagrams for interfacing the AD7575 in the ROM Interface mode. Figure 6 shows the AD7575 interface to the 6502/6809 microprocessors while the connection diagram for interfacing to the Z-80 is shown in Figure 7.

As a result of its very fast interface timing, the AD7575 can also be interfaced to the DSP processor, the TMS32010. The AD7575 will (within specifications) interface to the TMS32010, running at up to 18 MHz, but will typically work over the full clock frequency range of the TMS32010. Figure 8 shows the connection diagram for this interface. The AD7575 is mapped at a port address. Conversion is initiated using an IN A, PA instruction where PA is the decoded port address for the AD7575. The conversion result is obtained from the part using a second IN A, PA instruction, and the resultant data is placed in the TMS32010 accumulator.

In many applications it is important that the signal sampling occurs at exactly equal intervals to minimize errors due to sampling uncertainty or jitter. The interfaces outlined previously require that for sampling at equidistant intervals, the user must count clock cycles or match software delays. This is especially difficult in interrupt-driven systems where uncertainty in interrupt servicing delays would require that the AD7575 have priority interrupt status and even then redundant software delays may be necessary to equalize loop delays.

This problem can be overcome by using a real time clock to control the starting of conversion. This can be derived from the clock source used to drive the AD7575 CLK pin. Since the sampling instant occurs three clock cycles after $\overline{CS}$ and $\overline{RD}$ go LOW, the input signal sampling intervals are equidistant. The resultant data is placed in a FIFO latch that can be accessed by the microprocessor at its own rate whenever it requires the data. This ensures that data is not READ from the AD7575 during a conversion. If a data READ is performed during a conversion, valid data from the previous conversion will be accessed, but the conversion in progress may be interfered with and an incorrect result is likely.

If $\overline{CS}$ and $\overline{RD}$ go LOW within 20 ns of a falling clock edge, the AD7575 may or may not see that falling edge as the first of the three falling clock edges to the sampling instant. In this case, the sampling instant could vary by one clock period. If it is important to know the exact sampling instant, $\overline{CS}$ and $\overline{RD}$ should not go LOW within 20 ns of a falling clock edge.
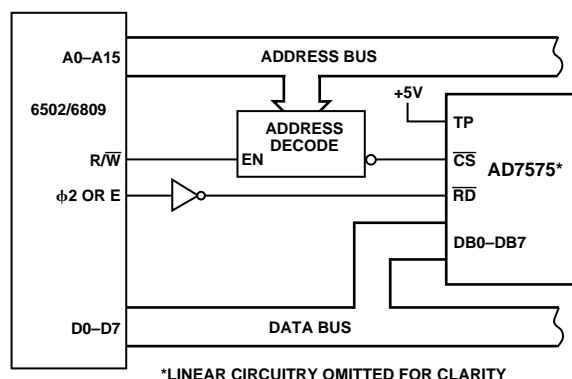

Figure 6. AD7575 to 6502/6809 ROM Interface

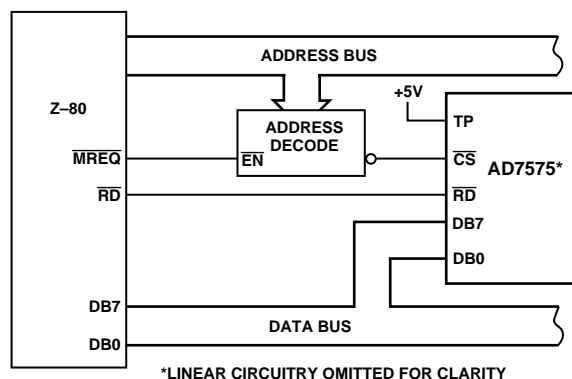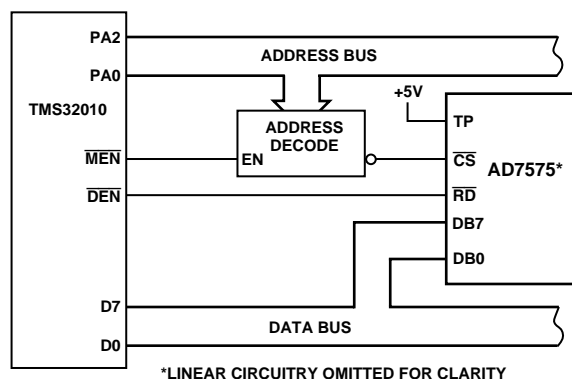Figure 7. AD7575 to Z-80 ROM Interface

Figure 8. AD7575 to TMS32010 ROM Interface

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A SAMPLED-DATA INPUT

The AD7575 makes use of a sampled-data comparator. The equivalent input circuit is shown in Figure 9. When a conversion starts, switch S1 is closed, and the equivalent input capacitance is charged to V_{IN}. With a switch resistance of typically 500 Ω and an input capacitance of typically 2 pF, the input time constant is 1 ns. Thus C_{IN} becomes charged to within ±1/4 LSB in 6.9 time constants or about 7 ns. Since the AD7575 requires two input clock cycles (at a clock frequency of 4 MHz) before going into the compare mode, there is ample time for the input voltage to settle before the first comparator decision is made. Increasing the source resistance increases the settling time required. Input bypass capacitors placed directly at the analog input act to average the input charging currents. The average current flowing through any source impedance can cause full-scale errors.
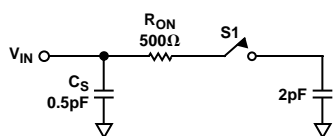
Figure 9. Equivalent Input Circuit

REFERENCE INPUT

The reference input impedance on the AD7575 is code dependent and varies by a ratio of approximately 3-to-1 over the digital code range. The typical resistance range is from 6 kΩ to 18 kΩ. As a result of the code dependent input impedance, the V_{REF} input must be driven from a low impedance source. Figure 10 shows how an AD589 can be configured to produce a nominal reference voltage of +1.23 V.
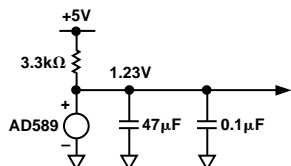
Figure 10. Reference Circuit

TRACK-AND-HOLD

The on-chip track-and-hold on the AD7575 means that input signals with slew rates up to 386 mV/μs can be converted without error. This corresponds to an input signal bandwidth of 50 kHz for a 2.46 V peak-to-peak sine wave. Figure 11 shows a typical plot of signal-to-noise ratio versus input frequency over the input bandwidth of the AD7575. The SNR figures are generated using a 200 kHz sampling frequency, and the reconstructed sine wave passes through a filter with a cutoff frequency of 50 kHz.

The improvement in the SNR figures seen at the higher frequencies is due to the sharp cutoff of the filter (50 kHz, 8th order Chebyshev) used in the test circuit.
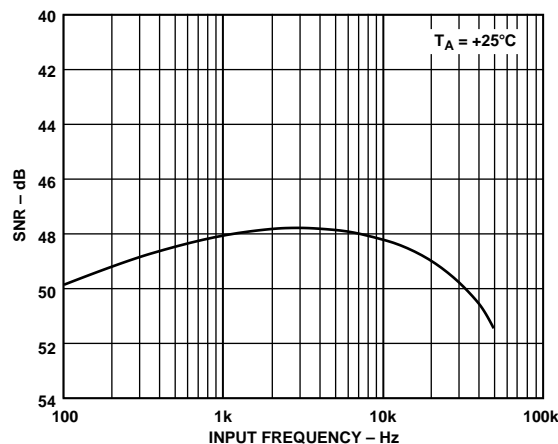
Figure 11. SNR vs. Input Frequency

The input signal is held on the third falling edge of the input clock after $\overline{CS}$ and $\overline{RD}$ go LOW. This is indicated in Figure 12 for the Slow Memory Interface. Between conversions, the input signal is tracked by the AD7575 track-and-hold. Since the sampled signal is held on a small, on-chip capacitor, it is advisable that the data bus be kept as quiet as possible during a conversion.
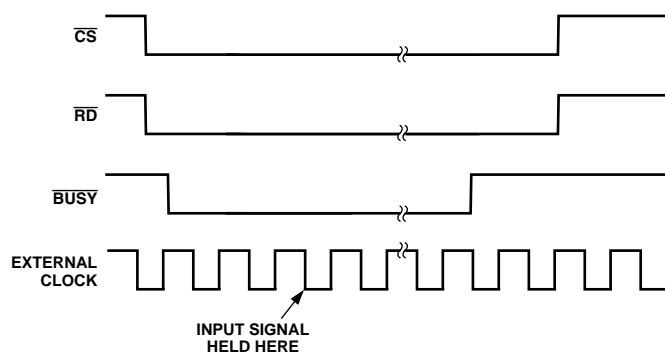
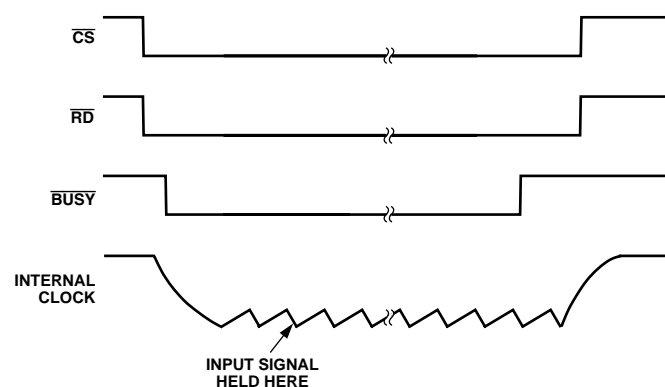Figure 12a. Track-and-Hold (Slow Memory Interface) with External Clock

Figure 12b. Track-and-Hold (Slow Memory Interface) with Internal Clock

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AD7575

INTERNAL/EXTERNAL CLOCK

The AD7575 can be used with its own internal clock or with an externally applied clock. In either case, the clock signal appearing at the CLK pin is divided internally by two to provide an internal clock signal for the AD7575. A single conversion lasts for 20 input clock cycles (10 internal clock cycles).

INTERNAL CLOCK

Clock pulses are generated by the action of the external capacitor (C_{CLK}) charging through an external resistor (R_{CLK}) and discharging through an internal switch. When a conversion is complete, the internal clock stops operating. In addition to conversion, the internal clock also controls the automatic internal reset of the SAR. This reset occurs at the start of each conversion cycle during the first internal clock pulse.

Nominal conversion times versus temperature for the recommended R_{CLK} and C_{CLK} combination are shown in Figure 13.
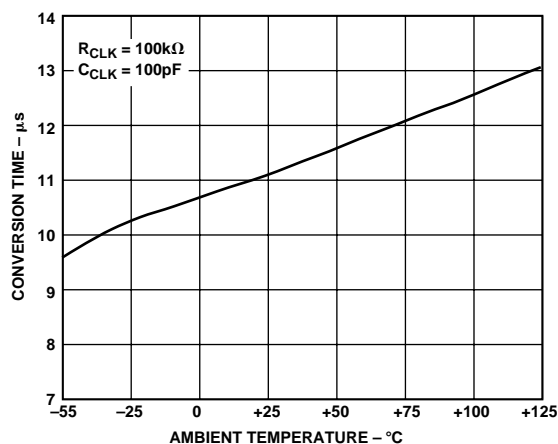

Figure 13. Typical Conversion Times vs. Temperature Using Internal Clock

The internal clock is useful because it provides a convenient clock source for the AD7575. Due to process variations, the actual operating frequency for this R_{CLK}/C_{CLK} combination can vary from device to device by up to ±50%. For this reason it is recommended that an external clock be used in the following situations:

1. Applications requiring a conversion time that is within 50% of 5 μs, the minimum conversion time for specified accuracy. A clock frequency of 4 MHz at the CLK pin gives a conversion time of 5 μs.

2. Applications where time related software constraints cannot accommodate time differences that may occur due to unit to unit clock frequency variations or temperature.

EXTERNAL CLOCK

The CLK input of the AD7575 may be driven directly from 74 HC, 4000B series buffers (such as 4049) or from LS TTL with a 5.6 kΩ pull-up resistor. When conversion is complete, the internal clock is disabled even if the external clock is still applied. This means that the external clock can continue to run between conversions without being disabled. The mark/space ratio of the external clock can vary from 70/30 to 30/70.

The AD7575 is specified for operation at a 5 μs conversion rate; with a 4 MHz input clock frequency. If the part is operated at slower clock frequencies, it may result in slightly degraded accuracy performance from the part. This is a result of leakage effects on the hold capacitor. Figure 14 shows a typical plot of accuracy versus conversion time for the AD7575.
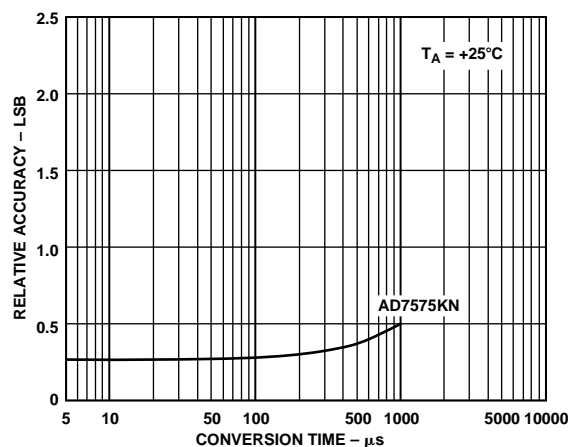

Figure 14. Accuracy vs. Conversion Time

REV. B

UNIPOLAR OPERATION

The basic operation for the AD7575 is in the unipolar single supply mode. Figure 15 shows the circuit connections to achieve this, while the nominal transfer characteristic for unipolar operation is given in Figure 16. Since the offset and full-scale errors on the AD7575 are very small, in many cases it will not be necessary to adjust out these errors. If calibration is required, the procedure is as follows:

Offset Adjust

Offset error adjustment in single-supply systems is easily achievable by means of the offset null facility of an op amp when used as a voltage follower for the analog input signal, AIN. The op amp chosen should be able to operate from a single supply and allow a common-mode input voltage range that includes 0 V (e.g., TLC271). To adjust for zero offset, the input signal source is set to +4.8 mV (i.e., 1/2 LSB) while the op amp offset is varied until the ADC output code flickers between 000 . . . 00 and 000 . . . 01.

Full-Scale Adjust

The full scale or gain adjustment is made by forcing the analog input AIN to +2.445 V (i.e., Full-Scale Voltage −3/2 LSB). The magnitude of the reference voltage is then adjusted until the ADC output code flickers between 111 . . . 10 and 111. . . 11.
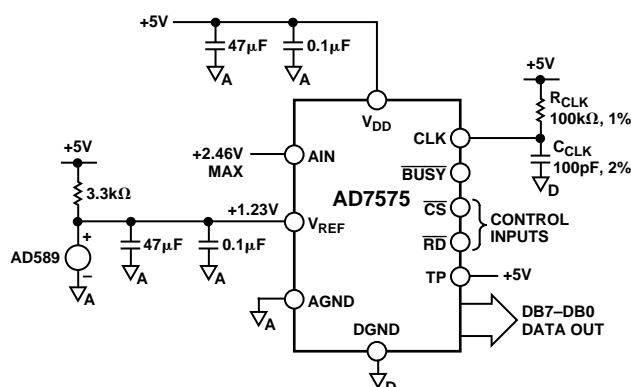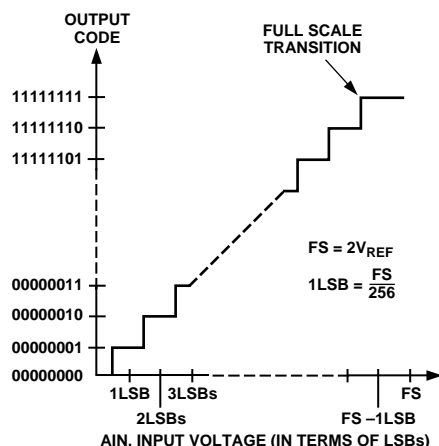
BIPOLAR OPERATION

The circuit of Figure 17 shows how the AD7575 can be configured for bipolar operation. The output code provided by the AD7575 is offset binary. The analog input voltage range is ±5 V, although the voltage appearing at the AIN pin of the AD7575 is in the range 0 V to +2.46 V. Figure 18 shows the transfer function for bipolar operation. The LSB size is now 39.06 mV. Calibration of the bipolar operation is outlined below. Once again, because the errors are small, it may not be necessary to adjust them. To maintain specified performance without the calibration, all resistors should be 0.1% tolerance with R4 and R5 replaced by one 3.3 kΩ resistor and R2 and R3 replaced by one 2.5 kΩ resistor.

Offset Adjust

Offset error adjustment is achieved by applying an analog input voltage of −4.9805 V (−FS +1/2 LSB). Resistor R3 is then adjusted until the output code flickers between 000 . . . 00 and 000 . . . 01.

Full-Scale Adjust

Full-scale or gain adjustment is made by applying an analog input voltage of +4.9414 V (+FS −3/2 LSB). Resistor R4 is then adjusted until the output code flickers between 111 . . . 10 and 111. . . 11.
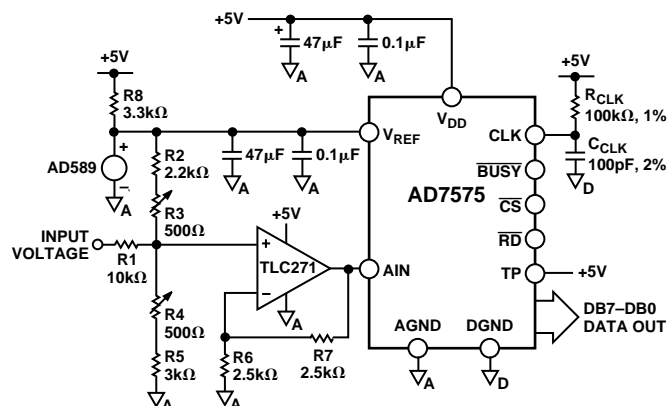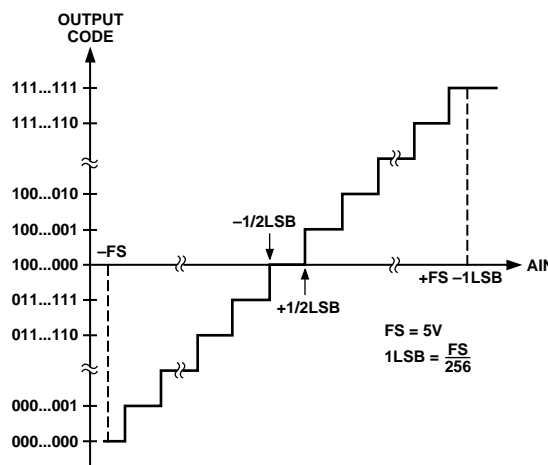

Figure 15. Unipolar Configuration

Figure 17. Bipolar Configuration

Figure 16. Nominal Transfer Characteristic for Unipolar Operation

Figure 18. Nominal Transfer Characteristic for Bipolar Operation

AD7575

APPLICATION HINTS

1. NOISE: Both the input signal lead to AIN and the signal return lead from AGND should be kept as short as possible to minimize input-noise coupling. In applications where this is not possible, either a shielded cable or a twisted pair transmission line between source and ADC is recommended. Also, since any potential difference in grounds between the signal source and ADC appears as an error voltage in series with the input signal, attention should be paid to reducing the ground circuit impedance as much as possible. In general, the source resistance should be kept below 2 kΩ. Larger values of source resistance can cause undesired system noise pickup.

2. PROPER LAYOUT: Layout for a printed circuit board should ensure that digital and analog lines are kept separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track. Both the analog input and the reference input should be screened by AGND. A single point analog ground separate from the logic system ground, should be established at or near the AD7575. This single point analog ground subsystem should be connected to the digital system ground by a single-track connection only. Any reference bypass capacitors, analog input filter capacitors or input signal shielding should be returned to the analog ground point.

AD7575 WITH AD589 REFERENCE

The AD7575 8-bit A/D converter features a total unadjusted error specification over its entire operating temperature range. This total unadjusted error includes all errors in the A/D converter—offset, full scale and linearity. The one feature not provided on the AD7575 is a voltage reference. This section discusses the use of the AD589 bandgap reference with the AD7575, and gives the combined reference and ADC error budget over the full operating temperature range. This allows the user to compare the combined AD589/AD7575 errors to ADCs whose specifications include on-chip references.

Two distinct application areas exist. The first is where the reference voltage and the analog input voltage are derived from the same source. In other words, if the reference voltage varies, the analog input voltage range varies by a ratioed amount. In this case, the user is not worried about the absolute value of the reference voltage. The second case is where changes in the reference voltage are not matched by changes in the analog input voltage range. Here, the absolute value of the reference voltage, and its drift over temperature, are of prime importance. Both applications are discussed below.

If the analog input range varies with the reference voltage, the part is said to be operating ratiometrically. This is representative of many applications. If the reference is on-chip, and the user does not have access to it, it is not possible to get ratiometric operation. Since the AD7575 uses an external reference, it can be used in ratiometric applications. However, because the part is specified with a reference of +1.23 V ± 5%, then the voltage range for ratiometric operation is limited.

The error analysis over temperature of ratiometric applications is different from nonratiometric ones. Since the reference and analog input voltage range are ratioed to each other, temperature variations in the reference are matched by variations in the analog input range. Therefore, the AD589 contributes no additional errors over temperature to the system errors, and the combined total unadjusted error specification for the AD589 and AD7575 is as per the total unadjusted error specification in this data sheet.

With nonratiometric applications, however, the analog input range stays the same if the reference varies and a full-scale error is introduced. The amount by which the reference varies determines the amount of error introduced. The AD589 is graded on temperature coefficient; therefore, selection of different grades allows the user to tailor the amount of error introduced to suit the system requirements. The reference voltage from the AD589 can lie between 1.2 V and 1.25 V. This reference voltage can be adjusted for the desired full-scale voltage range using the circuit outlined in Figure 19. For example, if an analog input voltage range of 0 V to +2.46 V is required, the reference should be adjusted to +1.23 V. Once the reference is adjusted to the desired value at 25°C, the total error is as per the total unadjusted error specification on the AD7575 specification pages. (To reduce this still further, offset and full-scale errors of the AD7575 can be adjusted out using the calibration procedure outlined in this data sheet.)
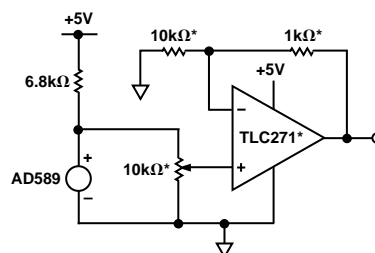
*ONLY REQUIRED IF IT IS NECESSARY TO ADJUST THE ABSOLUTE VALUE OF REFERENCE VOLTAGE.

Figure 19. Reference Adjust Circuit

However, it is as the temperature varies from 25°C that the AD589 starts to introduce errors. The typical temperature characteristics of the AD589 are shown in Figure 20. The temperature coefficients (TCs) represent the slopes of the diagonals of the error band from +25°C to T_{MIN} and +25°C to T_{MAX}. The AD589 TC is specified in ppm/°C max and is offered in four different grades.
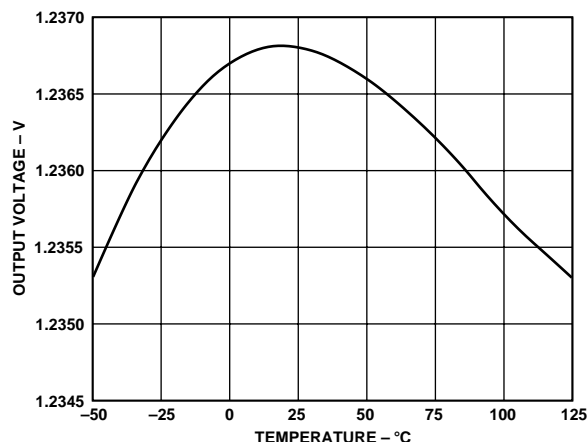
–10–

Figure 20. Typical AD589 Temperature Characteristics

The effect the TC has on the system error is that it introduces a full-scale error in the ADC. This, in turn, affects the total unadjusted error specification. For example, using the AD589KH with a 50 ppm/°C max TC the change in reference voltage from 25°C to 70°C will be from 1.23 V to 1.22724 V, a change of –2.76 mV. This results in a change in the full-scale range of the ADC of –5.52 mV, since the full-scale range on the AD7575 is 2 V_{REF}. Because the LSB size for the AD7575 is 9.61 mV, the AD589 introduces an additional full-scale error of –0.57 LSBs on top of the existing full-scale error specification for the ADC. Since the total unadjusted error specification for the ADC includes the full-scale error, there is also a corresponding increase in the total unadjusted error of –0.57 LSBs. The change in reference voltage at 0°C is –1.5 mV, resulting in a full-scale change of –3 mV or –0.31 LSBs worth of full-scale error. Table I shows the amount of additional total unadjusted error, which is introduced by the temperature variation of the AD589, for different grades and for different temperature ranges. This table applies only to nonratiometric applications, because the temperature variation of the reference does not affect the system error in ratiometric applications as outlined earlier. It shows the amount of error introduced over T_{MIN} to T_{MAX} for a system in which the reference has been adjusted to the desired value at 25°C. The final or right-most column of the table gives the total combined error for the AD589 and the top grade AD7575.

Taking the 25°C measurement as the starting point, the full-scale error introduced is always in the negative direction whether the temperature goes to T_{MIN} or T_{MAX}. This can be seen from the AD589 temperature characteristic shown in Figure 20. If the reference voltage is adjusted for 1.23 V at 45°C (for the 0°C to +70°C range) and 75°C (for the –55°C to +125°C range) the magnitude of the error introduced is reduced since it is distributed in both the positive and negative directions. Alternatively, this can be achieved not by adjusting at these temperatures, which would be impractical, but by adjusting the reference to 1.231 V instead of 1.23 V (for the extended temperature range) at 25°C. This has the required effect of distributing the plot of Figure 20 more evenly about the desired value.

An additional error source is the mismatch between the temperature coefficients (TCs) of the 10 kΩ and 1 kΩ resistors in the feedback loop of the TLC271. If these resistors have ±50 ppm/°C absolute TCs, the worst case difference in drift between both resistors is 100 ppm/°C. From +25°C to +125°C, this introduces a worst case shift of 1.22 mV, which results in an additional full-scale error of 0.25 LSB. If ±25 ppm/°C resistors are used, then the worst case error is 0.13 LSB. Over the 0°C to +70°C range, the ±50 ppm/°C resistors introduce an additional full-scale error of 0.11 LSB. All these errors are worst case and assume that the resistance values drift in opposite directions. In practice, resistors of the same type, and from the same manufacturer, would drift in the same direction and hence the above error would be considerably reduced. An additional error source is the offset drift of the TLC271. This is significant only over the –55°C to +125°C range and, even in this case, it contributes <0.1 LSB worth of full-scale error.

The error outlined in the right-hand column of Table I is a total unadjusted error specification, excluding resistor and offset drift (the effect of these can be controlled by the user). It consists of errors from two error sources: a ±1 LSB contribution from the AD7575 (including full-scale, offset and relative accuracy errors), and the remainder is a full-scale error introduced by the AD589. It is important to note that the variation of the AD589 voltage only introduces a full-scale error; the relative accuracy (or endpoint nonlinearity) of the system, with a top grade AD7575, is still ±1/2 LSB (i.e., 8-bits accurate).

**Table I. AD589/AD7575 Error over Temperature (Nonratiometric Applications)**

| AD589 Grade	Temperature Range	Full-Scale Error Introduced by AD589 @ T_{MAX} (Worst Case)	Combined Worst Case AD589/AD7575 T.U.E. @ T_{MAX}
AD589JH	0°C to +70°C	–1.15 LSB	–2.15 LSB
AD589KH	0°C to +70°C	–0.57 LSB	–1.57 LSB
AD589LH	0°C to +70°C	–0.29 LSB	–1.29 LSB
AD589MH	0°C to +70°C	–0.115 LSB	–1.115 LSB
AD589SH	–55°C to +125°C	–2.56 LSB	–3.56 LSB
AD589TH	–55°C to +125°C	–1.28 LSB	–2.28 LSB
AD589UH	–55°C to +125°C	–0.64 LSB	–1.64 LSB

*Excluding resistor and offset drift.

AD7575

OUTLINE DIMENSIONS
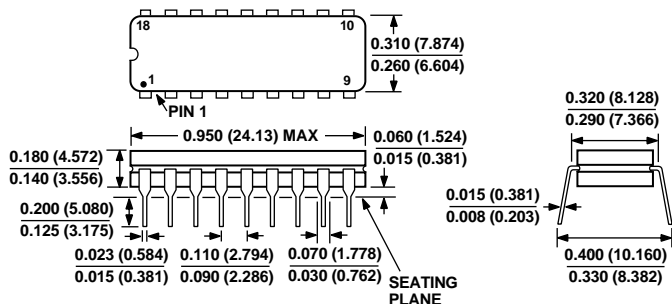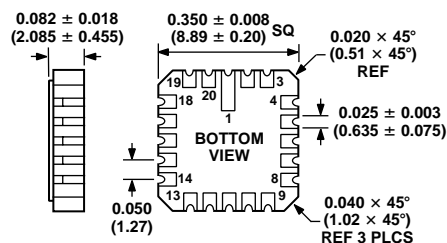Dimensions shown in inches and (mm).

18-Lead Plastic DIP
(N-18)
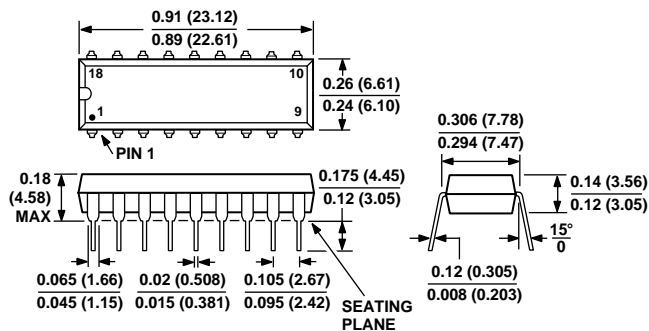
20-Lead PLCC
(P-20A)
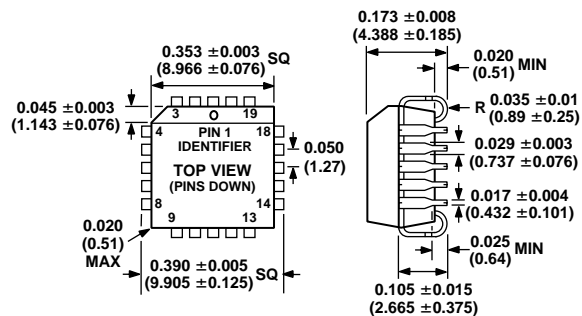
18-Lead Cerdip
(Q-18)

20-Terminal LCCC
(E-20A)

18-Lead SOIC
(R-18)

REV. B
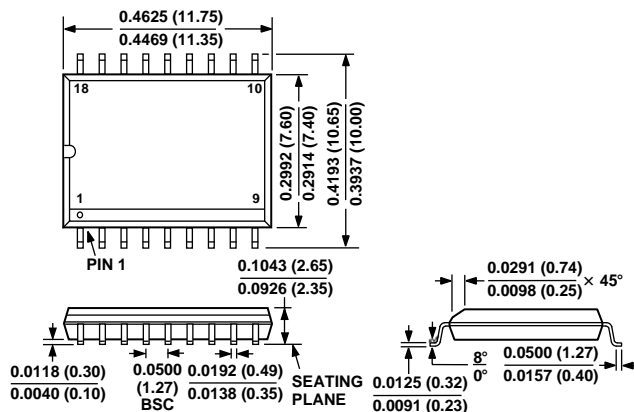
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