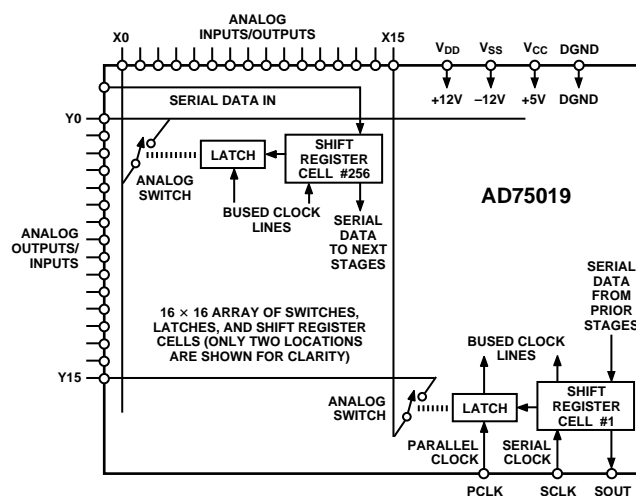


### FEATURES

**256 Switches in a 16 × 16 Array**  
**Wide Signal Range: to Supply Rails of 24 V or ±12 V**  
**Low On-Resistance: 200 Ω Typ**  
**TTL/CMOS/Microprocessor-Compatible Control Lines**  
**Serial Input Simplifies Interface**  
**Serial Output Allows Cascading for More Channels**  
**Low Power Consumption: 2 mW Quiescent**  
**Compact 44-Lead PLCC**

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT DESCRIPTION

The AD75019 contains 256 analog switches in a 16 × 16 array. Any of the X or Y pins may serve as an input or output. Any or all of the X terminals may be programmed to connect to any or all of the Y terminals. The switches can accommodate signals with amplitudes up to the supply rails and have a typical on-resistance of 150 Ω.

Data is loaded serially via the SIN input and clocked into an on-board 256-bit shift register via SCLK. When all the switch settings have been programmed, data is transferred into a set of 256 latches via PCLK. The serial shift register is dynamic, so there is a minimum clock rate of 20 kHz. The maximum clock rate of 5 MHz allows loading times as short as 52 μs. The switch control latches are static and will hold their data as long as power is applied.

To extend the number of switches in the array, you may cascade multiple AD75019s. The SOUT output is the end of the shift register, and may be connected to the SIN input of the next AD75019.

The AD75019 is fabricated in Analog Devices' BiMOS II process. This epitaxial BiCMOS process features CMOS devices for low distortion switches and bipolar devices for ESD protection.

REV. D

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# AD75019—SPECIFICATIONS<sup>1</sup> (T<sub>A</sub> = +25°C, V<sub>DD</sub> and V<sub>SS</sub> = ±12 V, V<sub>CC</sub> = +5 V unless otherwise noted)

AD75019	Symbol	Min	Typ	Max	Units
<b>MULTIPLEXER</b>					
Input Signal Range	V <sub>IN</sub>	V <sub>SS</sub> – 0.5		V <sub>DD</sub> + 0.5	V
Switch ON Resistance, V <sub>DD</sub> and V <sub>SS</sub> = ±12 V, V <sub>SIGNAL</sub> = ±12 V	R <sub>ON</sub>		150	<b>300</b>	Ω
Switch ON Resistance, V <sub>DD</sub> and V <sub>SS</sub> = ±5 V, V <sub>SIGNAL</sub> = ±5 V	R <sub>ON</sub>		300	500	Ω
Switch ON Resistance Matching <sup>2</sup> , V <sub>SIGNAL</sub> = ±12 V	ΔR <sub>ON</sub>		20	<b>30</b>	Ω
Leakage Current, V <sub>SIGNAL</sub> = ±10 V			2	10	nA
Input/Output Capacitance	C <sub>IN</sub>			25	pF
Isolation Between Any Two Channels					
R <sub>S</sub> = 600 Ω, R <sub>L</sub> = 10 kΩ, V <sub>SIGNAL</sub> = 2 V p-p					
f <sub>SIGNAL</sub> = 1 kHz		92			dB
f <sub>SIGNAL</sub> = 20 kHz		69			dB
f <sub>SIGNAL</sub> = 1 MHz		38			dB
Total Harmonic Distortion				0.01	%
R <sub>S</sub> = 600 Ω, R <sub>L</sub> = 10 kΩ, V <sub>SIGNAL</sub> = 2 V p-p					
Switch Frequency Response, –3 dB					
R <sub>S</sub> = 600 Ω, R <sub>L</sub> = 10 kΩ, V <sub>SIGNAL</sub> = 2 V p-p		20			MHz
Propagation Delay			4	8	ns
<b>DIGITAL INPUTS (SIN, SCLK, PCLK)</b>					
Logic Levels (TTL Compatible)					
Input Voltage, Logic “1”	V <sub>IH</sub>	<b>2.4</b>		5.5	V
Input Voltage, Logic “0”	V <sub>IL</sub>	0		<b>0.8</b>	V
Input Current, V <sub>IH</sub> = 5.5 V	I <sub>IH</sub>			±1	μA
Input Current, V <sub>IL</sub> = 0.8 V	I <sub>IL</sub>			±1	μA
Input Capacitance	C <sub>IN</sub>			10	pF
<b>DIGITAL OUTPUTS (SOUT)</b>					
Logic Levels (TTL Compatible)					
Output Voltage, Logic “1”	V <sub>OH</sub>	2.8			V
Output Voltage, Logic “0”	V <sub>OL</sub>			0.4	V
Output Current, V <sub>OH</sub> = 2.8 V	I <sub>OH</sub>	3.2			mA
Output Current, V <sub>OL</sub> = 0.4 V	I <sub>OL</sub>	3.2			mA
<b>POWER SUPPLY REQUIREMENTS</b>					
Voltage Range, Total Analog	V <sub>DD</sub> – V <sub>SS</sub>	9.0		25.2	V
Voltage Range, Positive Analog	V <sub>DD</sub> – V <sub>DGND</sub>	(V <sub>CC</sub> – 0.5)		25.2	V
Voltage Range, Negative Analog	V <sub>SS</sub> – V <sub>DGND</sub>	–20.7		0	V
Voltage Range, Digital	V <sub>CC</sub> – V <sub>DGND</sub>	4.5	5	5.5	V
Supply Current, SCLK = 5 MHz,	I <sub>DD</sub> , I <sub>SS</sub>			±70	mA
V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.4 V	I <sub>CC</sub>			800	μA
Supply Current, Quiescent,	I <sub>DD</sub> , I <sub>SS</sub>		–	<b>±400</b>	μA
V <sub>IL</sub> = 0.8 V, V <sub>IH</sub> = 2.4 V	I <sub>CC</sub>		–	<b>100</b>	μA

## NOTES

<sup>1</sup>All minimum and maximum specifications are guaranteed, and specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

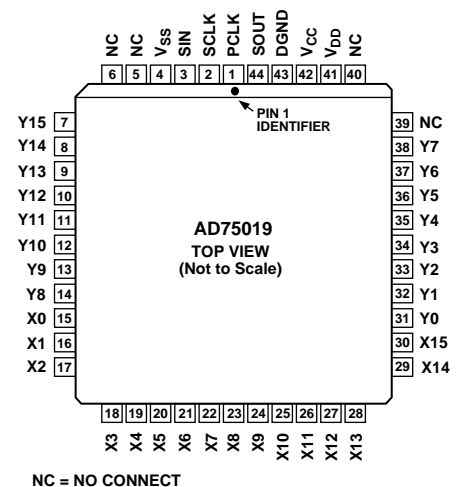
<sup>2</sup>Switch resistance matching is measured with zero volts at each analog input and refers to the difference between the maximum and minimum values.

Specifications subject to change without notice.

## PIN FUNCTION DESCRIPTIONS

Pin	Name	Description	Pin	Name	Description
1	PCLK	Parallel Clock Input	23	X8	Analog Input (or Output)
2	SCLK	Serial Clock Input	24	X9	Analog Input (or Output)
3	SIN	Serial Data Input	25	X10	Analog Input (or Output)
4	V <sub>SS</sub>	Negative Analog Power Supply	26	X11	Analog Input (or Output)
5	NC	No Internal Connection	27	X12	Analog Input (or Output)
6	NC	No Internal Connection	28	X13	Analog Input (or Output)
7	Y15	Analog Output (or Input)	29	X14	Analog Output (or Input)
8	Y14	Analog Output (or Input)	30	X15	Analog Output (or Input)
9	Y13	Analog Output (or Input)	31	Y0	Analog Output (or Input)
10	Y12	Analog Output (or Input)	32	Y1	Analog Output (or Input)
11	Y11	Analog Output (or Input)	33	Y2	Analog Output (or Input)
12	Y10	Analog Output (or Input)	34	Y3	Analog Output (or Input)
13	Y9	Analog Output (or Input)	35	Y4	Analog Output (or Input)
14	Y8	Analog Output (or Input)	36	Y5	Analog Output (or Input)
15	X0	Analog Input (or Output)	37	Y6	Analog Output (or Input)
16	X1	Analog Input (or Output)	38	Y7	Analog Output (or Input)
17	X2	Analog Input (or Output)	39	NC	No Internal Connection
18	X3	Analog Input (or Output)	40	NC	No Internal Connection
19	X4	Analog Input (or Output)	41	V <sub>DD</sub>	Positive Analog Power Supply
20	X5	Analog Input (or Output)	42	V <sub>CC</sub>	Digital Power Supply
21	X6	Analog Input (or Output)	43	DGND	Digital Ground
22	X7	Analog Input (or Output)	44	SOUT	Serial Data Output: Positive True

## PIN CONFIGURATION



## TIMING CHARACTERISTICS<sup>1</sup> ( $T_A = T_{MIN}$ to $T_{MAX}$ , rated power supplies unless otherwise noted)

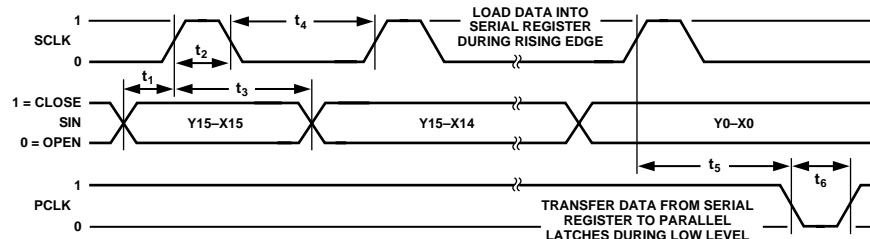
Parameter	Symbol	Value	Units	Condition
Data Setup Time	$t_1$	20	ns	min
SCLK Pulsewidth	$t_2$	100	ns	min
Data Hold Time	$t_3$	40	ns	min
SCLK Pulse Separation	$t_4$	100	ns	min
SCLK to PCLK Delay	$t_5$	65	ns	min
SCLK to PCLK Delay and Release	$(t_5 + t_6)$	5	ms	max
PCLK Pulsewidth	$t_6$	65	ns	min
Propagation Delay, PCLK to Switches On or Off	—	70	ns	max
Data Load Time	—	52	$\mu$ s	SCLK = 5 MHz
SCLK Frequency	—	20	kHz	min
SCLK, PCLK Rise and Fall Times	—	1	$\mu$ s	max

### NOTES

<sup>1</sup>Timing measurement reference level is 1.5 V.

Specifications subject to change without notice.

### TIMING DIAGRAM



### OPERATION TRUTH TABLE

Control Lines				Operation/Comment
PCLK	SCLK	SIN	SOUT	
1	0	X	X	No operation.
1	1	Data <sub>i</sub>	Data <sub>i-256</sub>	The data on the SIN line is loaded into the serial register; data clocked into the serial register 256 clocks ago appears at the SOUT output.
0	X	X	X	Data in the serial shift register transfers into the parallel latches which control the switch array.

### APPLICATIONS INFORMATION

#### Loading Data

Data to control the switches is clocked serially into a 256-bit shift register and then transferred in parallel to 256 bits of memory. The rising edge of SCLK, the serial clock input, loads data into the shift register. The first bit loaded via SIN, the serial data input, controls the switch at the intersection of row Y15 and column X15. The next bits control the remaining columns (down to X0) of row Y15, and are followed by the bits for row Y14, and so on down to the data for the switch at the intersection of row Y0 and column X0. The shift register is dynamic, so there is a minimum clock rate, specified as 20 kHz.

After the shift register is filled with the new 256 bits of control data, PCLK is activated (pulsed low) to transfer the data to the parallel latches. Since the shift register is dynamic, there is a maximum time delay specified before the data is lost: PCLK must be activated and brought back high within 5 ms after filling the shift register. The switch control latches are static and will hold their data as long as power is applied.

To extend the number of switches in the array, you may cascade multiple AD75019s. The SOUT output is the end of the shift register, and may be directly connected to the SIN input of the next AD75019.

#### Power Supply Sequencing and Bypassing

All junction-isolated parts operating on multiple power supplies require proper attention to supply sequencing. Because BiMOS II is a junction-isolated process, parasitic diodes exist between  $V_{DD}$  and  $V_{CC}$ , and between  $V_{SS}$  and DGND. As a result,  $V_{DD}$  must always be greater than ( $V_{CC} - 0.5$  V), and  $V_{SS}$  must always be less than ( $DGND + 0.5$  V).

If you can't ensure that system power supplies will sequence to meet these conditions, external Schottky (e.g., 1N5818) or silicon (e.g., 1N4001) diodes may be used. To protect the positive side, the anode would connect to  $V_{CC}$  (Pin 42) and the cathode to  $V_{DD}$  (Pin 41). For the negative side, connect the anode to  $V_{SS}$  (Pin 4) and the cathode to DGND (Pin 43).

Each of the three power supply pins [ $V_{DD}$  (Pin 41),  $V_{CC}$  (Pin 42) and  $V_{SS}$  (Pin 4)] should be bypassed to DGND (Pin 43) through a 0.1  $\mu$ F ceramic capacitor located close to the package pins.

#### Transistor Count

AD75019 contains 5,472 transistors. This number may be used for calculating projected reliability.

# AD75019

## ABSOLUTE MAXIMUM RATINGS\*

	Min	Max	Units	Conditions
$V_{DD}$ to DGND	-0.5	+25.2	V	$T_A \leq 75^\circ\text{C}$
$V_{SS}$ to DGND	-25.2	+0.5	V	
$V_{CC}$ to DGND	-0.5	+7.0	V	
$V_{DD}$ to $V_{SS}$	-0.5	+25.2	V	
$V_{CC}$ to $V_{SS}$	-0.5	+25.2	V	
Digital Inputs to DGND	-0.3	$V_{CC} + 0.5$	V	
Power Dissipation		1.0	W	
Operating Temperature Range	0	+70	$^\circ\text{C}$	Soldering, 10 sec
Storage Temperature	-65	+150	$^\circ\text{C}$	
Lead Temperature		+300	$^\circ\text{C}$	

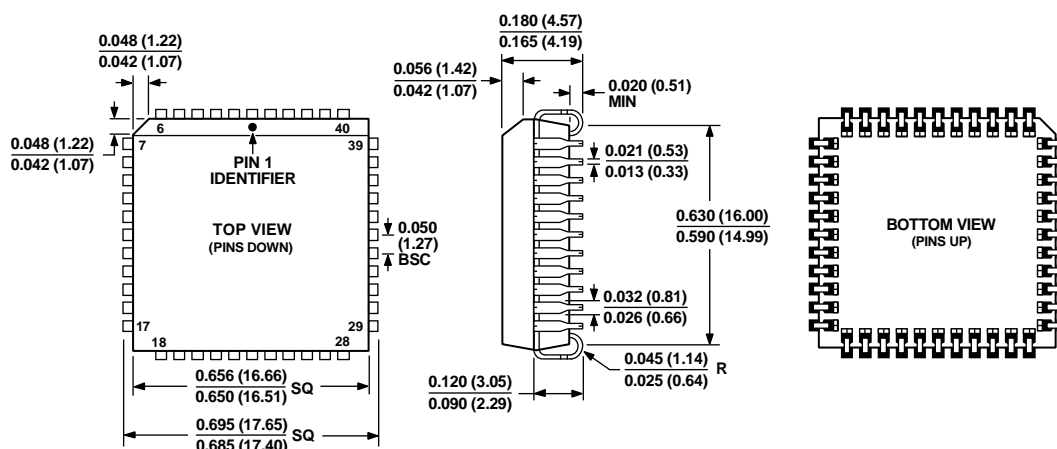
\*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-047-AC  
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS  
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR  
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 1. 44-Lead Plastic Leaded Chip Carrier [PLCC]  
(P-44)

Dimensions shown in inches and (millimeters)

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD75019JPZ	0°C to 70°C	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44
AD75019JPZ-REEL	0°C to 70°C	44-Lead Plastic Leaded Chip Carrier [PLCC]	P-44

<sup>1</sup> Z = RoHS Compliant Part.

## REVISION HISTORY

10/2018—Rev. C to Rev. D

Changes to Temperature Range Parameter,

AD75019—Specifications Table .....2

Moved Outline Dimensions and Ordering Guide .....5

Updated Outline Dimensions.....5

Changes to Ordering Guide.....5

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