

### FEATURES

Specified for  $V_{DD}$  of 2.35 V to 5.25 V

Low power

3.6 mW at 600 kSPS with 3 V supplies

15 mW at 600 kSPS with 5 V supplies

Wide input bandwidth

70 dB SNR at 100 kHz input frequency

High speed serial interface

SPI/QSPI™/MICROWIRE™/DSP compatible

Standby mode: 1  $\mu$ A maximum

6-lead SOT-23 package

### ENHANCED PRODUCT FEATURES

Military temperature range ( $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ )

Controlled manufacturing baseline

One assembly/test site

One fabrication site

Enhanced product change notification

Qualification data available upon request

### APPLICATIONS

Battery-powered systems

Personal digital assistants

Medical instruments

Mobile communications

Instrumentation and control systems

Data acquisition systems

### GENERAL DESCRIPTION

The AD7476<sup>1</sup> is a 12-bit, high speed, low power, successive approximation ADC. The part operates from a single 2.35 V to 5.25 V power supply and features throughput rates up to 600 kSPS. The part contains a low noise, wide bandwidth, track-and-hold amplifier that can handle input frequencies in excess of 6 MHz.

The conversion process and data acquisition are controlled using  $\overline{\text{CS}}$  and the serial clock, allowing the device to interface with microprocessors or DSPs. The input signal is sampled on the falling edge of  $\overline{\text{CS}}$  and the conversion is initiated at this point. There are no pipeline delays associated with this part.

The AD7476 uses advanced design techniques to achieve very low power dissipation at high throughput rates.

<sup>1</sup> Protected by U.S. Patent No. 6,681,332.

#### Rev. 0

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### FUNCTIONAL BLOCK DIAGRAM

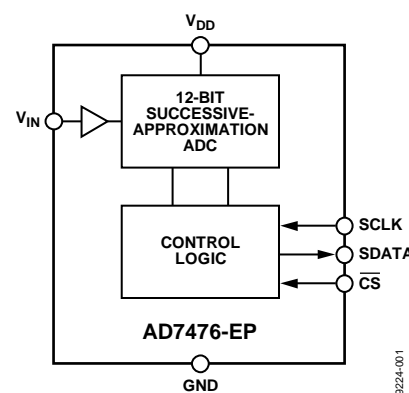


Figure 1.

The reference for the part is taken internally from  $V_{DD}$ . This allows the widest dynamic input range to the ADC. Thus, the analog input range for the part is 0 V to  $V_{DD}$ . The conversion rate is determined by the SCLK pin.

Additional application and technical information can be found in the [AD7476](#) data sheet.

### PRODUCT HIGHLIGHTS

1. First 12-Bit ADC in a SOT-23 Package.
2. High Throughput with Low Power Consumption.
3. Flexible Power/Serial Clock Speed Management. The conversion rate is determined by the serial clock, allowing the conversion time to be reduced through the serial clock speed increase. This allows the average power consumption to be reduced while not converting. The part also features a shutdown mode to maximize power efficiency at lower throughput rates. Current consumption is 1  $\mu$ A maximum when in shutdown mode.
4. Reference Derived from the Power Supply.
5. No Pipeline Delay. The part features a standard successive-approximation ADC with accurate control of the sampling instant via a  $\overline{\text{CS}}$  input and once-off conversion control.

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REVISION HISTORY

8/10—Revision 0: Initial Version

## SPECIFICATIONS

$V_{DD} = 2.35\text{ V to }5.25\text{ V}$ ,  $f_{SCLK} = 12\text{ MHz}$ ,  $f_{SAMPLE} = 600\text{ kSPS}$ , unless otherwise noted;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	S Version	Unit	Test Conditions/Comments
<b>DYNAMIC PERFORMANCE</b>			
Signal-to-(Noise + Distortion) (SINAD)	69 70	dB min dB min	$f_{IN} = 100\text{ kHz sine wave}$ $T_A = 25^\circ\text{C}$
Signal-to-Noise Ratio (SNR)	70	dB min	
Total Harmonic Distortion (THD)	−78	dB typ	
Peak Harmonic or Spurious Noise (SFDR)	−80	dB typ	
Intermodulation Distortion (IMD)			
Second-Order Terms	−78	dB typ	$f_a = 103.5\text{ kHz}$ , $f_b = 113.5\text{ kHz}$
Third-Order Terms	−78	dB typ	$f_a = 103.5\text{ kHz}$ , $f_b = 113.5\text{ kHz}$
Aperture Delay	10	ns typ	
Aperture Jitter	30	ps typ	
Full Power Bandwidth	6.5	MHz typ	At 3 dB
<b>DC ACCURACY</b>			
Resolution	12	Bits	$V_{DD} = (2.35\text{ V to }3.6\text{ V})^1$
Integral Nonlinearity	±1.5 ±0.6	LSB max LSB typ	
Differential Nonlinearity	−0.9/+1.5 ±0.75	LSB max LSB typ	Guaranteed no missed codes to 12 bits
Offset Error	±2	LSB max	
Gain Error	±2	LSB typ LSB max LSB typ	
<b>ANALOG INPUT</b>			
Input Voltage Ranges	0 to $V_{DD}$	V	
DC Leakage Current	±1	μA max	
Input Capacitance	30	pF typ	
<b>LOGIC INPUT</b>			
Input High Voltage, $V_{INH}$	2.4 1.8	V min V min	$V_{DD} = 2.35\text{ V}$
Input Low Voltage, $V_{INL}$	0.4 0.8	V max V max	$V_{DD} = 3\text{ V}$ $V_{DD} = 5\text{ V}$
Input Current, $I_{IN}$ , SCLK Pin	±1	μA max	Typically 10 nA, $V_{IN} = 0\text{ V or }V_{DD}$
Input Current, $I_{IN}$ , $\overline{CS}$ Pin	±1	μA typ	
Input Capacitance, $C_{IN}^2$	10	pF max	
<b>LOGIC OUTPUT</b>			
Output High Voltage, $V_{OH}$	$V_{DD} - 0.2$	V min	$I_{SOURCE} = 200\text{ μA}$ ; $V_{DD} = 2.35\text{ V to }5.25\text{ V}$
Output Low Voltage, $V_{OL}$	0.4	V max	$I_{SINK} = 200\text{ μA}$
Floating-State Leakage Current	±10	μA max	
Floating-State Output Capacitance <sup>2</sup>	10	pF max	
Output Coding	Straight (natural) binary		
<b>CONVERSION RATE</b>			
Conversion Time	1.33	μs max	16 SCLK cycles
Track-and-Hold Acquisition Time	500	ns max	Full-scale step input
	400	ns max	Sine wave input ≤ 100 kHz
Throughput Rate	600	kSPS max	

# AD7476-EP

Parameter	S Version	Unit	Test Conditions/Comments
POWER REQUIREMENTS			
$V_{DD}$	2.35/5.25	V min/max	Digital I/Ps = 0 V or $V_{DD}$
$I_{DD}$			
Normal Mode (Static)	2	mA typ	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$ , SCLK on or off
	1	mA typ	$V_{DD} = 2.35\text{ V to }3.6\text{ V}$ , SCLK on or off
Normal Mode (Operational)	3	mA max	$V_{DD} = 4.75\text{ V to }5.25\text{ V}$ , $f_{SAMPLE} = f_{SAMPLEMAX}^3$
	1.4	mA max	$V_{DD} = 2.35\text{ V to }3.6\text{ V}$ , $f_{SAMPLE} = f_{SAMPLEMAX}^4$
Full Power-Down Mode	1	$\mu\text{A max}$	SCLK off
	80	$\mu\text{A max}$	SCLK on
Power Dissipation			
Normal Mode (Operational)	15	mW max	$V_{DD} = 5\text{ V}$ , $f_{SAMPLE} = f_{SAMPLEMAX}^4$
	4.2	mW max	$V_{DD} = 3\text{ V}$ , $f_{SAMPLE} = f_{SAMPLEMAX}^4$
Full Power-Down	5	$\mu\text{W max}$	$V_{DD} = 5\text{ V}$ , SCLK off
	3	$\mu\text{W max}$	$V_{DD} = 3\text{ V}$ , SCLK off

<sup>1</sup> S version specifications apply as typical figures when  $V_{DD} = 5.25\text{ V}$ .

<sup>2</sup> Guaranteed by characterization.

<sup>3</sup>  $f_{SAMPLEMAX} = 600\text{ kSPS}$ .

## TIMING SPECIFICATIONS

$V_{DD} = 2.35 \text{ V}$  to  $5.25 \text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 2.

Parameter <sup>2</sup>	Limit at $T_{MIN}$ , $T_{MAX}$ <sup>1</sup>		Unit	Description
	3 V	5 V		
$f_{SCLK}$ <sup>3</sup>	10	10	kHz min	
	12	12	MHz max	
$t_{CONVERT}$	$16 \times t_{SCLK}$	$16 \times t_{SCLK}$		
$t_{QUIET}$	50	50	ns min	Minimum quiet time required between bus relinquish and start of next conversion
$t_1$	10	10	ns min	Minimum $\overline{CS}$ pulse width
$t_2$	10	10	ns min	$\overline{CS}$ to SCLK setup time
$t_3$ <sup>4</sup>	20	20	ns max	Delay from $\overline{CS}$ until SDATA three-state disabled
$t_4$ <sup>4</sup>	40	20	ns max	Data access time after SCLK falling edge, A version
	70	20	ns max	Data access time after SCLK falling edge, B version
$t_5$	$0.4 \times t_{SCLK}$	$0.4 \times t_{SCLK}$	ns min	SCLK low pulse width
$t_6$	$0.4 \times t_{SCLK}$	$0.4 \times t_{SCLK}$	ns min	SCLK high pulse width
$t_7$	10	10	ns min	SCLK to data valid hold time
$t_8$ <sup>5</sup>	10	10	ns min	SCLK falling edge to SDATA high impedance
	25	25	ns max	SCLK falling edge to SDATA high impedance
$t_{POWER-UP}$	1	1	$\mu\text{s typ}$	Power-up time from full power-down

<sup>1</sup> 3 V specifications apply from  $V_{DD} = 2.35 \text{ V}$  to  $3.6 \text{ V}$ ; 5 V specifications apply from  $V_{DD} = 4.75 \text{ V}$  to  $5.25 \text{ V}$ .

<sup>2</sup> Guaranteed by characterization. All input signals are specified with  $t_r = t_f = 5 \text{ ns}$  (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of  $1.6 \text{ V}$ .

<sup>3</sup> Mark/space ratio for the SCLK input is 40/60 to 60/40.

<sup>4</sup> Measured with the load circuit of Figure 2 and defined as the time required for the output to cross  $0.8 \text{ V}$  or  $2.0 \text{ V}$ .

<sup>5</sup>  $t_8$  is derived from the measured time taken by the data output to change  $0.5 \text{ V}$  when loaded with the circuit in Figure 2. The measured number is then extrapolated to remove the effects of charging or discharging the  $50 \text{ pF}$  capacitor. This means that the time,  $t_8$ , is the true bus relinquish time of the part and is independent of the bus loading.

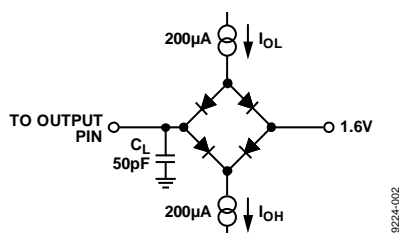


Figure 2. Load Circuit for Digital Output Timing Specifications

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Rating
$V_{DD}$ to GND	−0.3 V to +7 V
Analog Input Voltage to GND	−0.3 V to $V_{DD} + 0.3$ V
Digital Input Voltage to GND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to $V_{DD} + 0.3$ V
Input Current to Any Pin Except Supplies <sup>1</sup>	±10 mA
Operating Temperature Range	
Enhanced Plastic (EP Version)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SOT-23 Package	
$\theta_{JA}$ Thermal Impedance	230°C/W
$\theta_{JC}$ Thermal Impedance	92°C/W
Lead Temperature, Soldering Reflow	
(10 sec to 30 sec)	235 (0/+5)°C
Pb-free Temperature Soldering Reflow	255 (0/+5)°C
ESD	3.5 kV

<sup>1</sup> Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

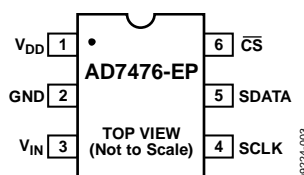


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD</sub>	Power Supply Input. The V <sub>DD</sub> range for the AD7476-EP is from 2.35 V to 5.25 V.
2	GND	Analog Ground. Ground reference point for all circuitry on the part. All analog input signals should be referred to this GND voltage.
3	V <sub>IN</sub>	Analog Input. Single-ended analog input channel. The input range is 0 V to V <sub>DD</sub> .
4	SCLK	Serial Clock. Logic input. SCLK provides the serial clock for accessing data from the part. This clock input is also used as the clock source for the AD7476-EP conversion process.
5	SDATA	Data Out. Logic output. The conversion result is provided on this output as a serial data stream. The bits are clocked out on the falling edge of the SCLK input. The data stream from the AD7476-EP consists of four leading zeros followed by the 12 bits of conversion data; this is provided MSB first.
6	$\overline{\text{CS}}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7476-EP and framing the serial data transfer.

TYPICAL PERFORMANCE CHARACTERISTICS

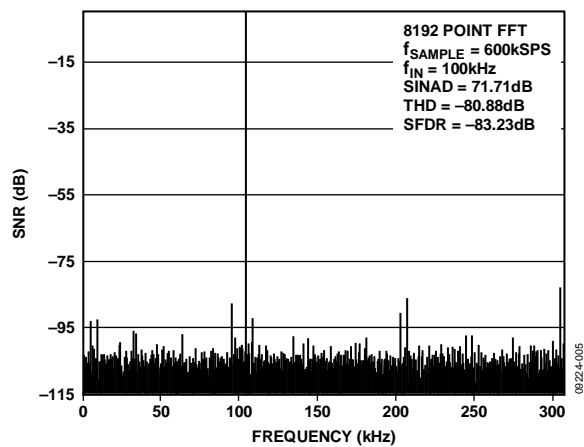


Figure 4. AD7476-EP Dynamic Performance at 600 kSPS

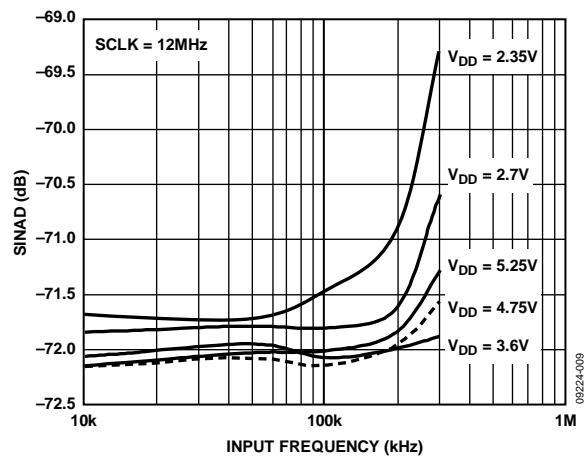
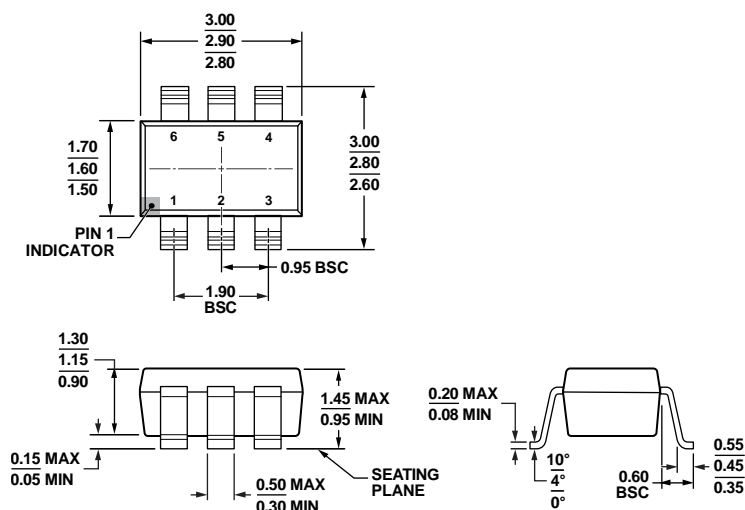


Figure 5. AD7476-EP SINAD vs. Input Frequency at 605 kSPS



## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 6. 6-Lead Small Outline Transistor Package [SOT-23]  
(RJ-6)

Dimensions shown in millimeters

121608-A

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Linearity Error (LSB) <sup>2</sup>	Package Description	Package Option	Branding
AD7476SRTZ-EP-RL7	−55°C to +125°C	±1.5 maximum	6-Lead SOT-23	RJ-6	C73#

<sup>1</sup> Z = RoHS Compliant Part, # denotes RoHS compliant part maybe top or bottom marked.

<sup>2</sup> Linearity error refers to integral linearity error.

**AD7476-EP**

**NOTES**

## **NOTES**

## NOTES

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