24-Bit, 250 kSPS Sigma-Delta ADC with 20 µs Settling

Data Sheet

AD7176-2

FEATURES

- Fast and flexible output rate—5 SPS to 250 kSPS
- Fast settling time—20 µs
- Channel scan data rate of 50 kSPS/channel
- Performance specifications
  - 17 noise free bits at 250 kSPS
  - 20 noise free bits at 2.5 kSPS
  - 22 noise free bits at 5 SPS
  - INL ±2.5 ppm of FSR
- 85 dB rejection of 50 Hz and 60 Hz with 50 ms settling
- User-configurable input channels
  - 2 fully differential or 4 pseudo differential
  - Crosspoint multiplexer
- On-chip 2.5 V reference (drift 2 ppm/°C)
- Internal oscillator, external crystal, or external clock
- Power supply
  - Single supply: 5 V AVDD1, 2 V to 5 V AVDD2 and IOVDD
  - Optional split supply: AVDD1 and AVSS ± 2.5 V
- Current: 7.8 mA
- Temperature range: −40°C to +105°C
- 3- or 4-wire serial digital interface (Schmitt trigger on SCLK)
  - CRC error checking
  - SPI, QSPI, MICROWIRE, and DSP compatible

APPLICATIONS

- Process control: PLC/DCS modules
  - Temperature and pressure measurement
- Medical and scientific multichannel instrumentation
- Chromatography

GENERAL DESCRIPTION

The AD7176-2 is a fast settling, highly accurate, high resolution, multiplexed Σ-Δ analog-to-digital converter (ADC) for low bandwidth input signals. Its inputs can be configured as two fully differential or four pseudo differential inputs via the integrated crosspoint multiplexer. An integrated precision, 2.5 V, low drift (2 ppm/°C), band gap internal reference (with an output reference buffer) adds functionality and reduces the external component count.

The maximum channel scan data rate is 50 kSPS/channel (settling time of 20 µs), resulting in fully settled data with 17 noise free bits. User-selectable output data rates range from 5 SPS to 250 kSPS. The resolution increases at lower speeds.

The AD7176-2 offers three key digital filters. The fast settling sinc5 + sinc1 filter maximizes the channel scan rate. The sinc3 filter maximizes the resolution for single-channel, low speed applications. For 50 Hz and 60 Hz environments, the AD7176-2 specific filter minimizes the settling times or maximizes the rejection of the line frequency. These enhanced filters enable simultaneous 50 Hz and 60 Hz rejection with a 27 SPS output data rate (with a settling time of 36 ms).

System offset and gain errors can be corrected on a per channel basis. This per channel configurability extends to the output data rate used for each channel when using a sinc5 + sinc1 filter. All switching of the crosspoint multiplexer is controlled by the ADC and can be configured to automatically control an external multiplexer via the GPIO pins.

The specified operating temperature range is −40°C to +105°C. The AD7176-2 is housed in a 24-lead TSSOP package.

FUNCTIONAL BLOCK DIAGRAM

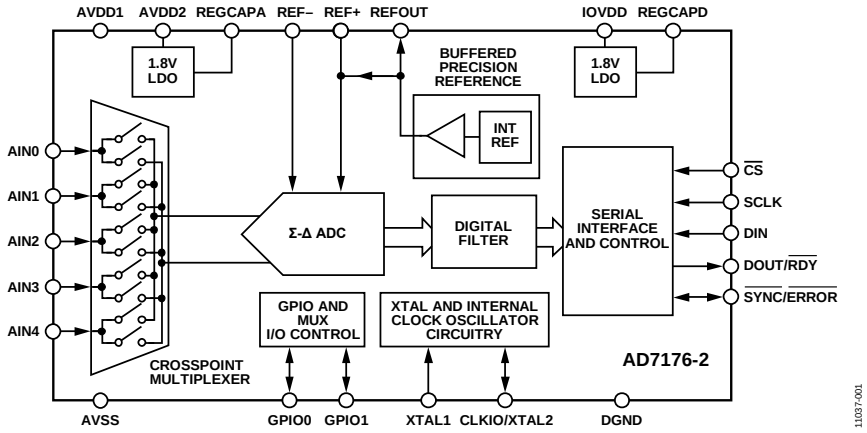

Figure 1.

Rev. D

Document Feedback

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SPECIFICATIONS

AVDD1 = 4.5 V to 5.5 V, AVDD2 = 2 V to 5.5 V, IOVDD = 2 V to 5.5 V, AVSS = DGND = 0 V, REF+ = 2.5 V, REF− = AVSS, internal master clock = 16 MHz, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPEED AND PERFORMANCE					
Output Data Rate (ODR)		5		250,000	SPS
No Missing Codes[1]	Excluding sinc3 filter ≥125 kSPS	24			Bits
Resolution	See Table 6				
Noise	See Table 6				
Noise Free Resolution	Sinc5 + sinc1 filter (default)				
	250 kSPS, REF+ = 5 V		17.3		Bits
	2.5 kSPS, REF+ = 5 V		20.1		Bits
	5 SPS, REF+ = 5 V		22.4		Bits
ACCURACY					
Integral Nonlinearity (INL)	2.5 V reference		±2.5	±7	ppm of FSR
	5 V reference		±7		ppm of FSR
Offset Error[2]	Internal short		±40		µV
Offset Drift	Internal short		±110		nV/°C
Offset Drift vs. Time[3]			±450		nV/1000 hours
Gain Error[2]	25°C		±10	±50	ppm/FSR
Gain Drift vs. Temperature[1]			±0.5	±1	ppm/FSR/°C
Gain Drift vs. Time[3]			±3		ppm/FSR/ 1000 hours
REJECTION					
Power Supply Rejection	AVDD1, AVDD2 V_{IN} = 1 V		90		dB
Common-Mode Rejection	V_{IN} = 0.1 V				
At DC		95			dB
At 50 Hz and 60 Hz[1]	20 SPS ODR (post filter) (50 Hz ± 1 Hz and 60 Hz ± 1 Hz)	130			dB
Normal Mode Rejection[1]	50 Hz ± 1 Hz and 60 Hz ± 1 Hz				
	Internal clock, 20 SPS ODR (post filter)	71	90		dB
	External clock, 20 SPS ODR (post filter)	85	90		dB
ANALOG INPUTS					
Differential Input Voltage Range			$\pm V_{REF}$		V
Absolute AIN Voltage Limits[1]		AVSS − 0.050		AVDD1 + 0.05	V
Analog Input Current					
Input Current			±48		µA/V
Input Current Drift	External clock		±0.75		nA/V/°C
	Internal clock (±2.5 % clock)		±4		nA/V/°C
Crosstalk	1 kHz input		−120		dB
INTERNAL REFERENCE	100 nF external capacitor on REFOUT to AVSS				
Output Voltage	REFOUT with respect to AVSS		2.5		V
Initial Accuracy[1]	T_A = 25°C[4]	−0.16%		+0.16%	V
Temperature Coefficient					
	0°C to +105°C		±2	±5	ppm/°C
	−40°C to +105°C		±3	±10	ppm/°C
Reference Load Current, I_{LOAD}	I_L	−10		+10	mA
Power Supply Rejection (Line Regulation)	AVDD1 and AVDD2		93		dB
Load Regulation	$\Delta V_{OUT}/\Delta I_L$		32		ppm/mA
Voltage Noise	e_N, 0.1 Hz to 10 Hz		4.5		µV rms
Voltage Noise Density	e_N, 1 kHz		215		nV/√Hz
Turn-On Settling Time	100 nF capacitor		60		µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Long-Term Stability[3]	1000 hours		460		ppm
Short Circuit	I_{SC}		25		mA
EXTERNAL REFERENCE					
Reference Input Voltage	Reference input = (REF+) − (REF−)	1	2.5	AVDD1	V
Absolute Reference Input Voltage Limits[1]		AVSS − 0.05		AVDD1 + 0.05	V
Average Reference Input Current			±72		µA/V
Average Reference Input Current Drift	External clock		±1.2		nA/V/°C
	Internal clock		±6		nA/V/°C
Normal Mode Rejection[1]	See the Rejection parameter section of this table				
Common-Mode Rejection			83		dB
GENERAL-PURPOSE I/O (GPIO 0, GPIO 1)	With respect to AVSS				
Output High Voltage, V_{OH}[1]	I_{SOURCE} = 200 µA	AVSS + 4			V
Output Low Voltage, V_{OL}[1]	I_{SINK} = 800 µA			AVSS + 0.4	V
Input Mode Leakage Current[1]		−10		+10	µA
Floating-State Output Capacitance			5		pF
Input High Voltage, V_{IH}[1]		AVSS + 3			V
Input Low Voltage, V_{IL}[1]				AVSS + 0.7	V
CLOCK					
Internal Clock					
Frequency			16		MHz
Accuracy		−2.5		+2.5	%
Duty Cycle			50:50		%
Output Low Voltage, V_{OL}				0.4	V
Output High Voltage, V_{OH}		0.8 × IOVDD			V
Crystal					
Frequency		14	16	16.384	MHz
Start-Up Time			10		µs
External Clock (CLKIO)			16	16.384	MHz
Duty Cycle[1]	Typical duty cycle 50:50 (max:min)	30	50:50	70	%
LOGIC INPUTS					
Input High Voltage, V_{INH}[1]	2 V ≤ IOVDD ≤ 2.3 V	0.65 × IOVDD			V
	2.3 V ≤ IOVDD ≤ 5.5 V	0.7 × IOVDD			V
Input Low Voltage, V_{INL}[1]	2 V ≤ IOVDD ≤ 2.3 V			0.35 × IOVDD	V
	2.3 V ≤ IOVDD ≤ 5.5 V			0.7	V
Hysteresis[1]	IOVDD > 2.7 V	0.08		0.25	V
	IOVDD < 2.7 V	0.04		0.2	V
Leakage Currents		−10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output High Voltage, V_{OH}[1]	IOVDD ≥ 4.5 V, I_{SOURCE} = 1 mA	0.8 × IOVDD			V
	2.7 V ≤ IOVDD < 4.5 V, I_{SOURCE} = 500 µA	0.8 × IOVDD			V
	IOVDD < 2.7 V, I_{SOURCE} = 200 µA	0.8 × IOVDD			V
Output Low Voltage, V_{OL}[1]	IOVDD ≥ 4.5 V, I_{SINK} = 2 mA			0.4	V
	2.7 V ≤ IOVDD < 4.5 V, I_{SINK} = 1 mA			0.4	V
	IOVDD < 2.7 V, I_{SINK} = 400 µA			0.4	V
Leakage Current	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
SYSTEM CALIBRATION[1]					
Full-Scale Calibration Limit				1.05 × FS	V
Zero-Scale Calibration Limit		−1.05 × FS			V
Input Span		0.8 × FS		2.1 × FS	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD1 − AVSS		4.5		5.5	V
AVDD2 − AVSS		2		5.5	V
AVSS − DGND		−2.75		0	V
IOVDD − DGND		2		5.5	V
IOVDD − AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS	All outputs unloaded, digital inputs connected to IOVDD or DGND				
Full Operating Mode					
AVDD1 Current	External reference		1.5	1.8	mA
	Internal reference		1.8	2.1	mA
AVDD2 Current	External reference		4.3	4.9	mA
	Internal reference		4.5	5.1	mA
IOVDD Current	External clock		2	2.3	mA
	Internal clock		2.3	2.6	mA
	External crystal		2.5		mA
Standby Mode					
Standby (LDO On)	Internal reference off, total current consumption		22		µA
	Internal reference on, total current consumption		415		µA
Power-Down Mode	Full power-down, LDO, Internal reference		0.5	10	µA
POWER DISSIPATION					
Full Operating Mode	AVDD2 = 2 V, IOVDD = 2 V, external clock and reference		20.1	23.2	mW
	AVDD2 = 5 V, IOVDD = 5 V, external clock and reference		39	44.8	mW
	AVDD2 = 2 V, IOVDD = 2 V, internal clock and reference		22.3	25.9	mW
	AVDD2 = 5 V, IOVDD = 5 V, internal clock and reference		42.5	49	mW
Standby Mode	Internal reference off, all supplies = 5 V		110		µW
	Internal reference on, all supplies = 5 V		2.1		mW
Power-Down Mode	Full power-down		2.5	50	µW

[1] Specification is not production tested but is supported by characterization data at the initial product release.
[2] Following a system or internal zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected. A system full-scale calibration reduces the gain error to the order of the noise for the programmed output data rate.
[3] This specification is noncumulative and includes the effects of preconditioning.
[4] This specification includes MSL preconditioning effects.

TIMING CHARACTERISTICS

IOVDD = 2 V to 5.5 V, DGND = 0 V, Input Logic 0 = 0 V, Input Logic 1 = IOVDD, C_{LOAD} = 20 pF, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX} (B Version)	Unit	Test Conditions/Comments[1, 2]
t_3	25	ns min	SCLK high pulse width
t_4	25	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns max	IOVDD = 4.5 V to 5.5 V
	40	ns max	IOVDD = 2 V to 3.6 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	12	ns max	IOVDD = 4.5 V to 5.5 V
	25	ns max	IOVDD = 2 V to 3.6 V
t_5[5]	2.5	ns min	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns max	
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns min	SCLK inactive edge to DOUT/$\overline{RDY}$ high/low
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	5	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] The time required for the output to cross the V_{OL} or V_{OH} limits.
[4] The SCLK active edge is the falling edge of SCLK.
[5] $\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while $\overline{RDY}$ is high, although care should be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

TIMING DIAGRAMS

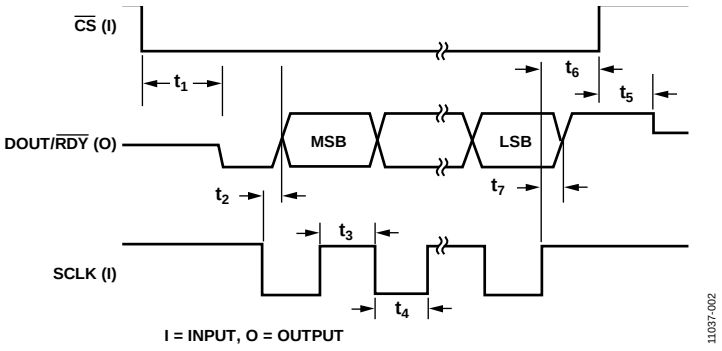


Figure 2. Read Cycle Timing Diagram

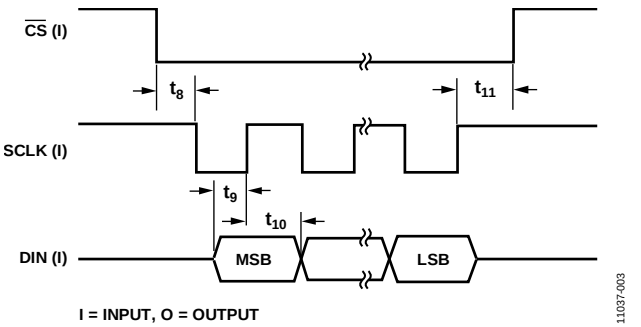


Figure 3. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD1, AVDD2 to AVSS	−0.3 V to +6.5 V
AVDD1 to DGND	−0.3 V to +6.5 V
IOVDD to DGND	−0.3 V to +6.5 V
IOVDD to AVSS	−0.3 V to +7.5 V
AVSS to DGND	−3.25 V to +0.3 V
Analog Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Reference Input Voltage to AVSS	−0.3 V to AVDD1 + 0.3 V
Digital Input Voltage to DGND	−0.3 V to IOVDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to IOVDD + 0.3 V
AIN[4:0] or Digital Input Current	10 mA
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Soldering, Reflow Temperature	260°C
ESD Rating (HBM)	3.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for a device soldered on a JEDEC test board for surface-mount packages. The values listed in Table 4 are based on simulated data.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead TSSOP		
JEDEC 1 Layer Board	149	°C/W
JEDEC 2 Layer Board	81	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

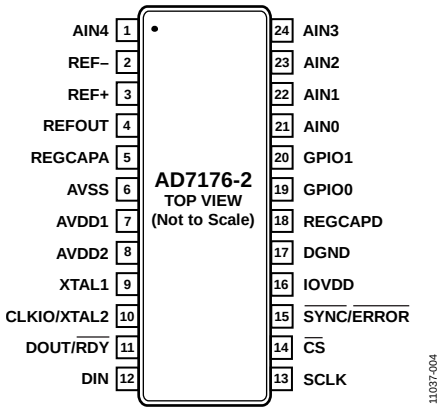


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AIN4	Analog Input 4. Selectable through crosspoint multiplexer.
2	REF−	Reference Input Negative Terminal. REF− can span from AVSS to AVDD1 − 1 V.
3	REF+	Reference Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVDD1 to AVSS + 1 V. The part functions with a reference from 1 V to AVDD1.
4	REFOUT	Buffered Output of Internal Reference. The output is 2.5 V with respect to AVSS.
5	REGCAPA	Analog LDO Regulator Output. Decouple this pin to AVSS using a 1 µF capacitor.
6	AVSS	Negative Analog Supply. This supply ranges from 0 V to −2.75 V and is nominally set to 0 V.
7	AVDD1	Analog Supply Voltage 1. This voltage is 5 V ± 10% with respect to AVSS.
8	AVDD2	Analog Supply Voltage 2. This voltage ranges from 2 V to AVDD1 with respect to AVSS.
9	XTAL1	Input 1 for Crystal.
10	CLKIO/XTAL2	Clock Input or Output (Based on the CLOCKSEL Bits in the ADCMODE Register)/Input 2 for Crystal. There are four options available: Internal oscillator—no output. Internal oscillator—output to CLKIO/XTAL2. Operates at IOVDD logic level. External clock—input to CLKIO/XTAL2. Input should be at IOVDD logic level. External crystal—connected between XTAL1 and CLKIO/XTAL2.
11	DOUT/$\overline{\text{RDY}}$	Serial Data Output/Data Ready Output. DOUT/$\overline{\text{RDY}}$ serves a dual purpose. It functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data-word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.
12	DIN	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK.
13	SCLK	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. The SCLK has a Schmitt-triggered input, making the interface suitable for opto-isolated applications.
14	$\overline{\text{CS}}$	Chip Select Input. This is an active low logic input used to select the ADC. $\overline{\text{CS}}$ can be used to select the ADC in systems with more than one device on the serial bus. $\overline{\text{CS}}$ can be hardwired low, allowing the ADC to operate in 3-wire mode with SCLK, DIN, and DOUT used to interface with the device. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated.

Pin No.	Mnemonic	Description
15	$\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$	Can be switched between a logic input and a logic output in the GPIOCON register. When synchronization input is enabled, this pin allows for synchronization of the digital filters and analog modulators when using multiple AD7176-2 devices. When synchronization input is disabled, this pin can be used in one of three modes: Active low error input mode: this mode sets the ADC_ERROR bit in the STATUS register. Active low, open-drain error output mode: the STATUS register error bits are mapped to the $\overline{\text{ERROR}}$ pin. The $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. General-purpose output mode: the status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the GPIO pins. The pin has an active pull-up in this case.
16	IOVDD	Digital I/O Supply Voltage. IOVDD voltage ranges from 2 V to 5 V. IOVDD is independent of AVDD2. For example, IOVDD can be operated at 3 V when AVDD2 equals 5 V, or vice versa. If AVSS is set to −2.5 V, the voltage on IOVDD must not exceed 3.6 V.
17	DGND	Digital Ground.
18	REGCAPD	Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1 µF capacitor.
19	GPIO0	General-Purpose Input/Output. The pin is referenced between AVDD1 and AVSS levels.
20	GPIO1	General-Purpose Input/Output. The pin is referenced between AVDD1 and AVSS levels.
21	AIN0	Analog Input 0. Selectable through the crosspoint multiplexer.
22	AIN1	Analog Input 1. Selectable through the crosspoint multiplexer.
23	AIN2	Analog Input 2. Selectable through the crosspoint multiplexer.
24	AIN3	Analog Input 3. Selectable through the crosspoint multiplexer.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD1 = 5 V, AVDD2 = 5 V, IOVDD = 3.3 V, unless otherwise noted.

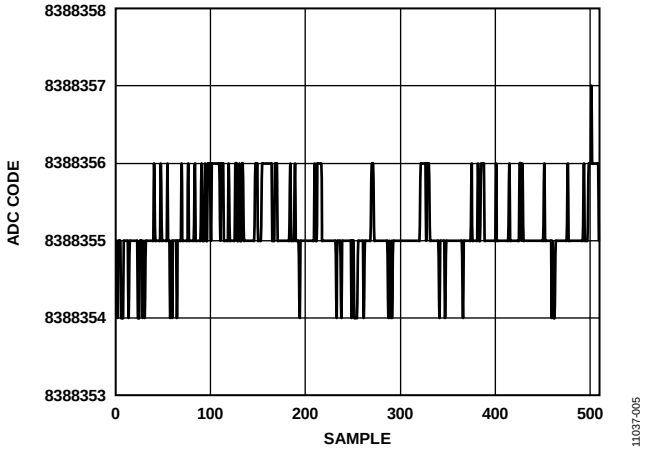


Figure 5. Noise (V_{REF} = 5 V, Output Data Rate = 5 SPS)

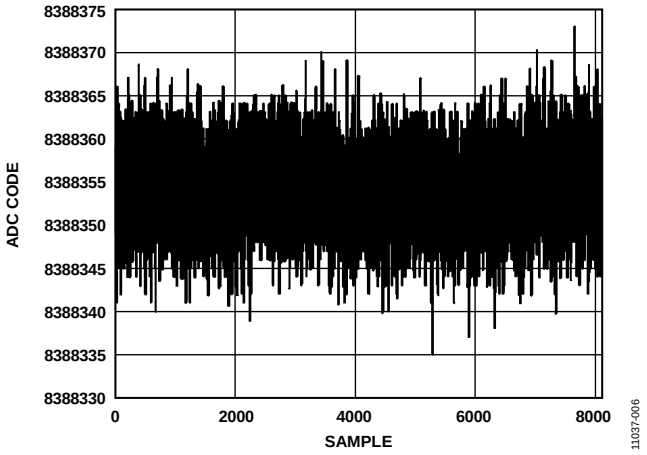


Figure 6. Noise (V_{REF} = 5 V, Output Data Rate = 10 kSPS)

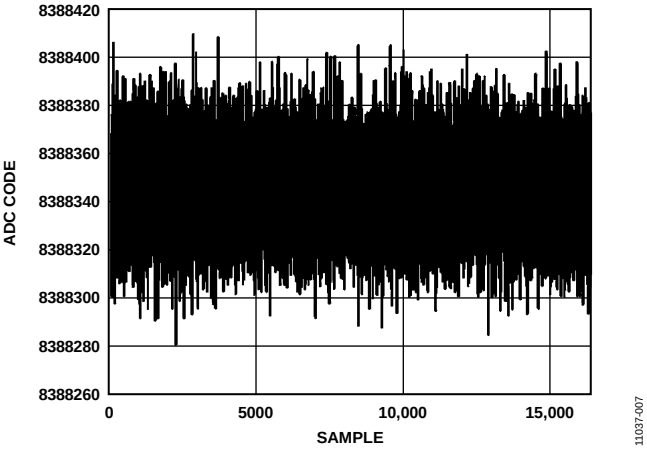


Figure 7. Noise (V_{REF} = 5 V, Output Data Rate = 250 kSPS)

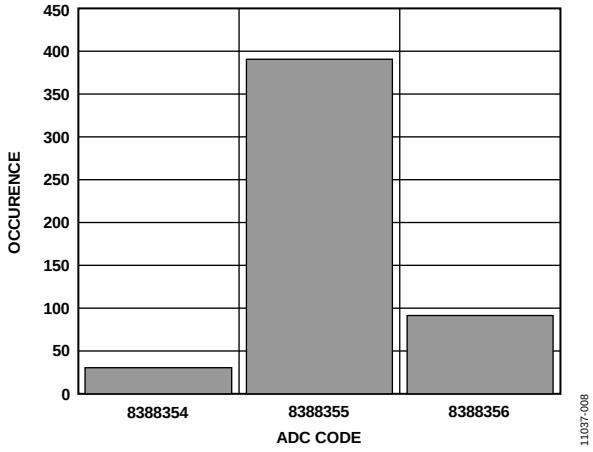


Figure 8. Noise Distribution Histogram (V_{REF} = 5 V, Output Data Rate = 5 SPS)

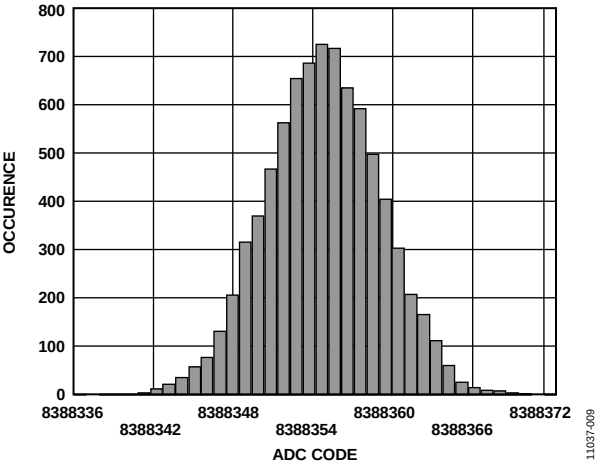


Figure 9. Noise Distribution Histogram (V_{REF} = 5 V Output Data Rate = 10 kSPS)

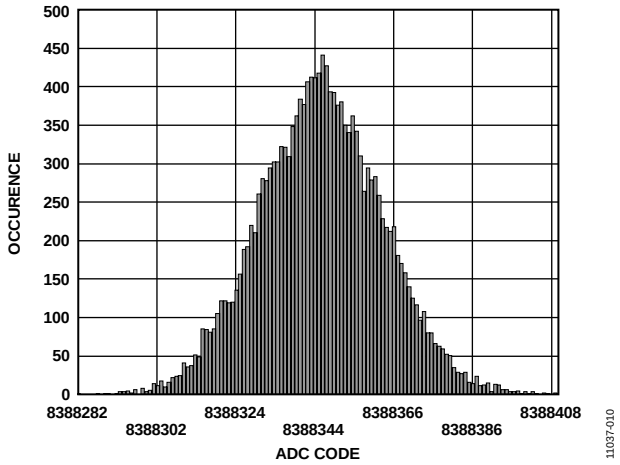


Figure 10. Noise Distribution Histogram (V_{REF} = 5 V, Output Data Rate = 250 kSPS)

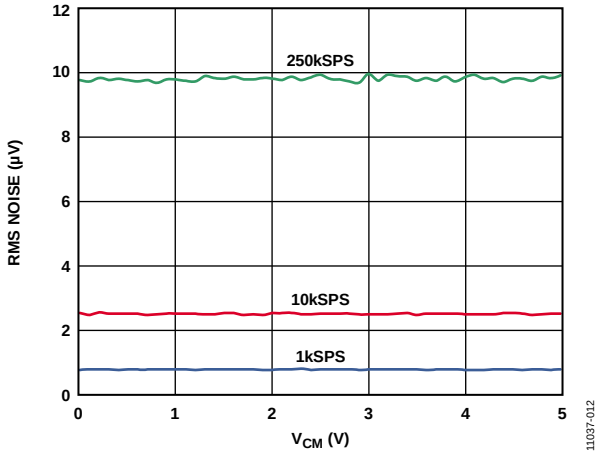


Figure 11. Noise vs. Common-Mode Input Voltage (V_{REF} = 2.5 V)

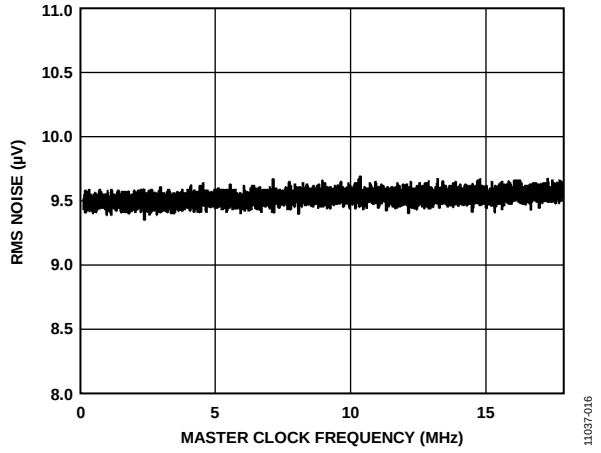


Figure 12. Noise vs. Master Clock (V_{REF} = 2.5 V)

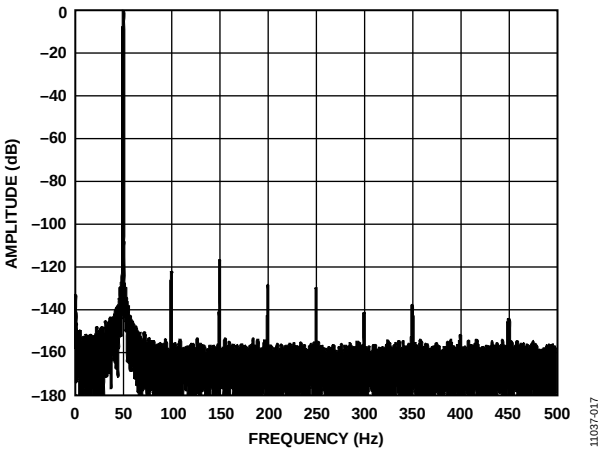


Figure 13. 50 Hz Input Tone, −0.5 dBFS Input FFT (V_{REF} = 2.5 V, Output Data Rate = 1 kSPS)

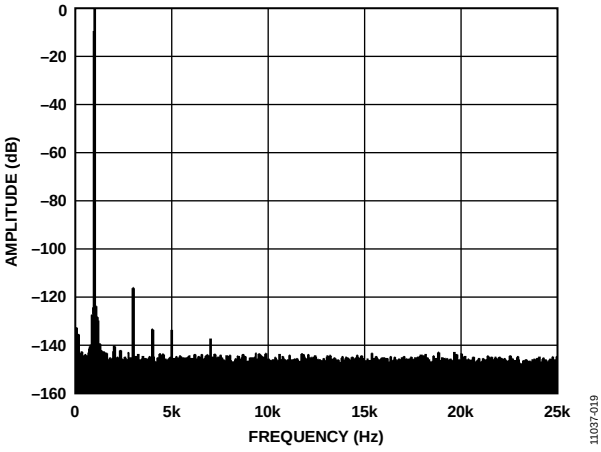


Figure 14. 1 kHz Input Tone, −0.5 dBFS Input FFT (V_{REF} = 2.5 V, Output Data Rate = 50 kSPS)

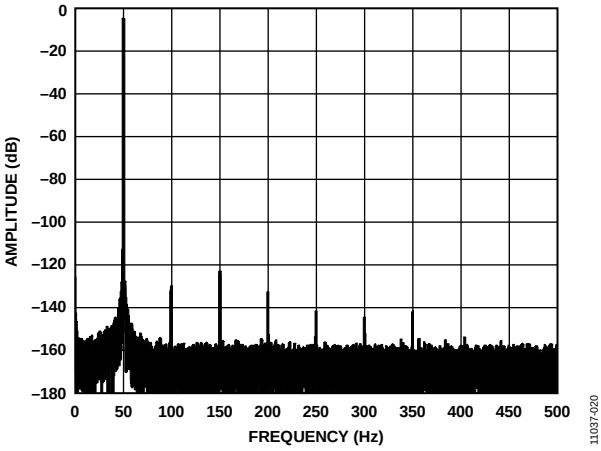


Figure 15. 50 Hz Input Tone, −6 dBFS Input FFT (V_{REF} = 2.5 V Output Data Rate = 1 kSPS)

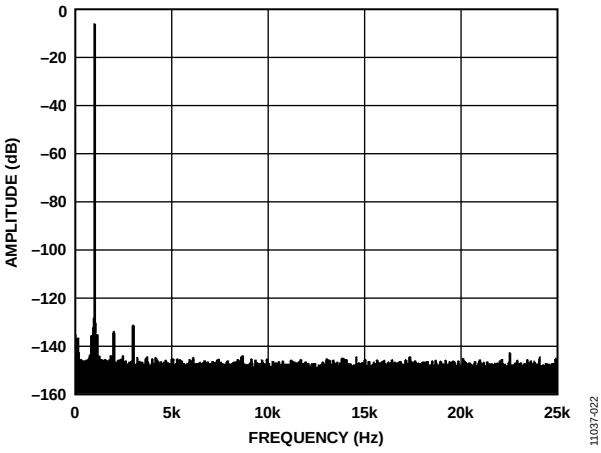


Figure 16. 1 kHz Input Tone, −6 dBFS Input FFT (V_{REF} = 2.5 V, Output Data Rate = 50 kSPS)

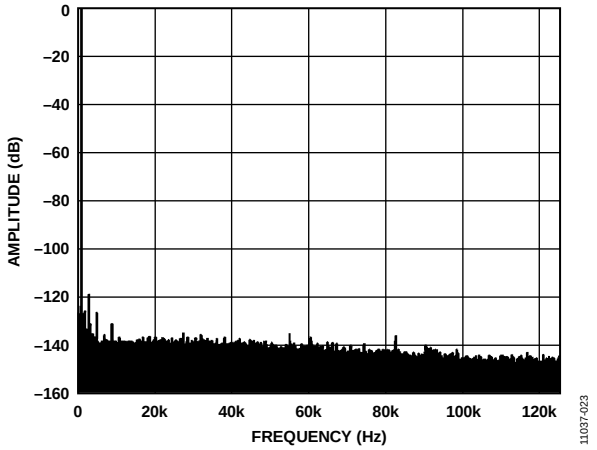


Figure 17. 1 kHz Input Tone, –0.5 dBFS Input FFT (V_{REF} = 2.5 V, Output Data Rate = 250 kSPS)

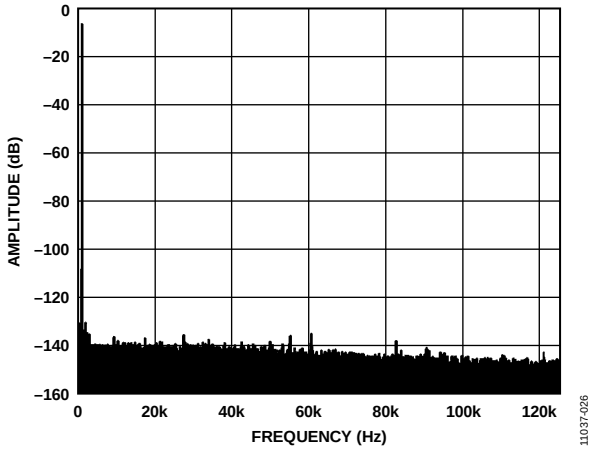


Figure 18. 1 kHz Input Tone, –6 dBFS Input FFT (V_{REF} = 2.5 V, Output Data Rate = 250 kSPS)

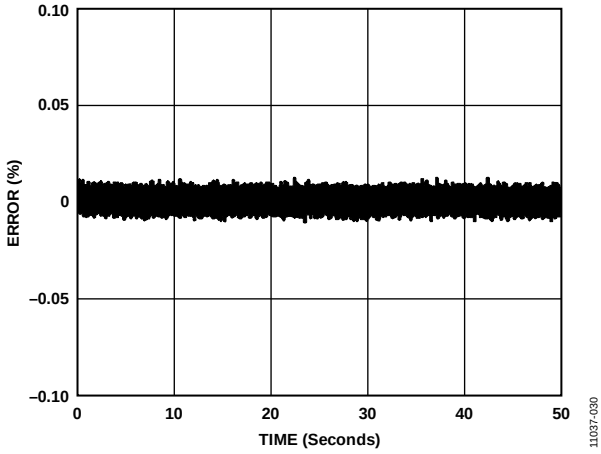


Figure 19. Internal Reference Settling Time (Extended)

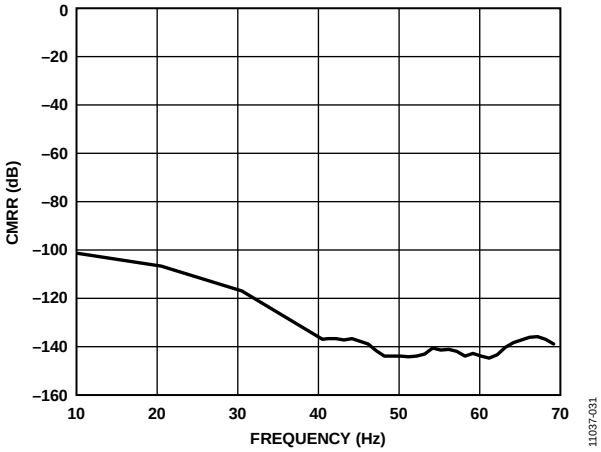


Figure 20. Common-Mode Rejection Ratio (10 Hz to 70 Hz) (20 SPS Enhanced Filter)

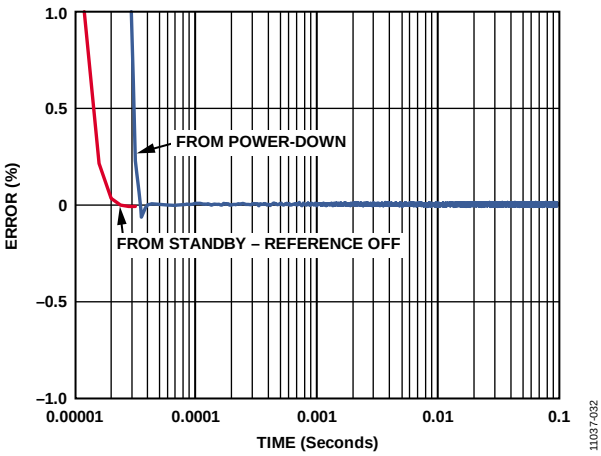


Figure 21. Internal Reference Settling Time

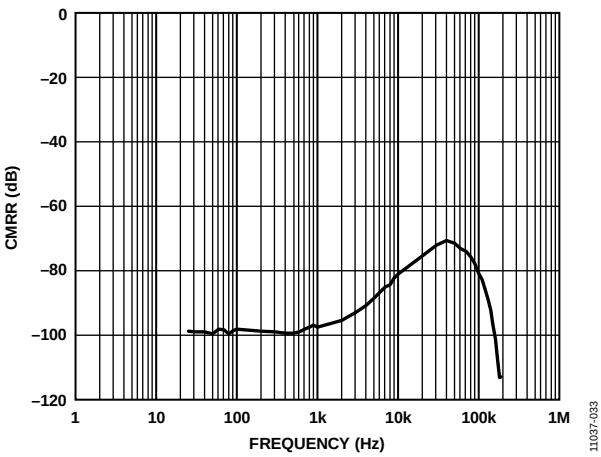


Figure 22. Common-Mode Rejection Ratio vs. Frequency (Output Data Rate = 250 kSPS)

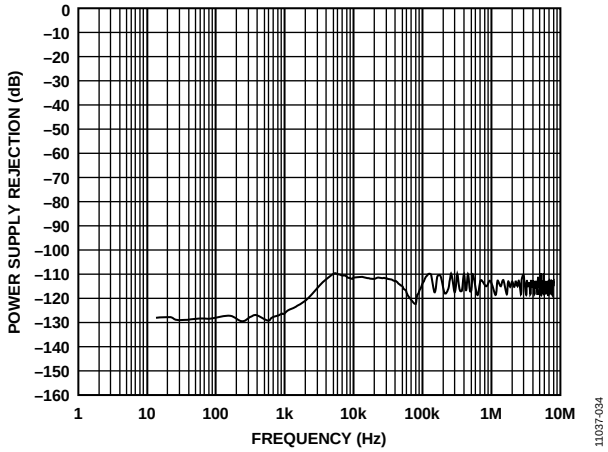


Figure 23. Power Supply Rejection Ratio vs. Frequency

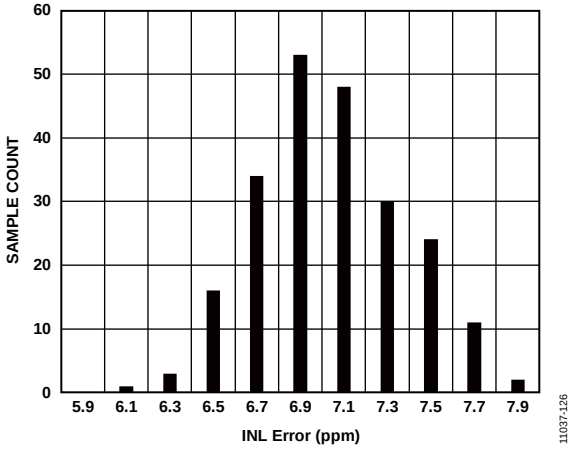


Figure 26. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 5 V External)

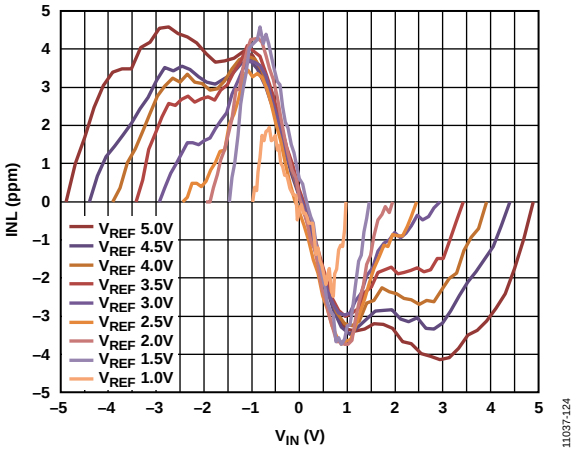


Figure 24. Integral Nonlinearity (INL) vs. Reference Voltage (Differential Input, External Reference)

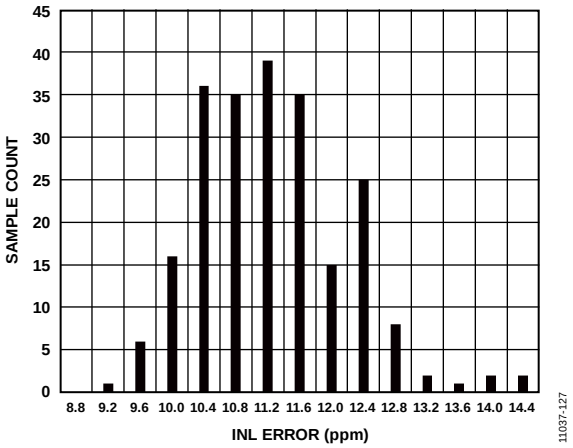


Figure 27. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 2.5 V Internal)

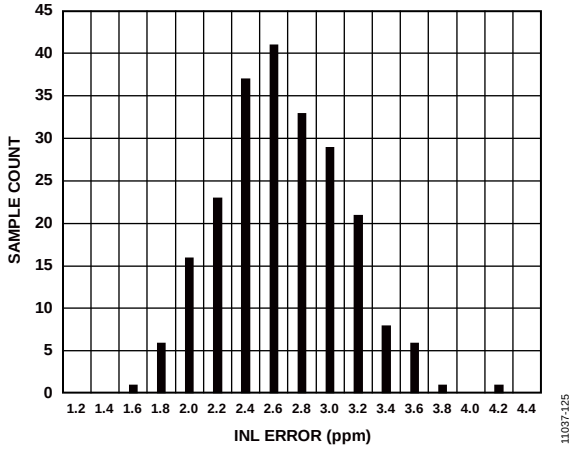


Figure 25. Integral Nonlinearity (INL) Distribution Histogram (Differential Input, V_{REF} = 2.5V External)

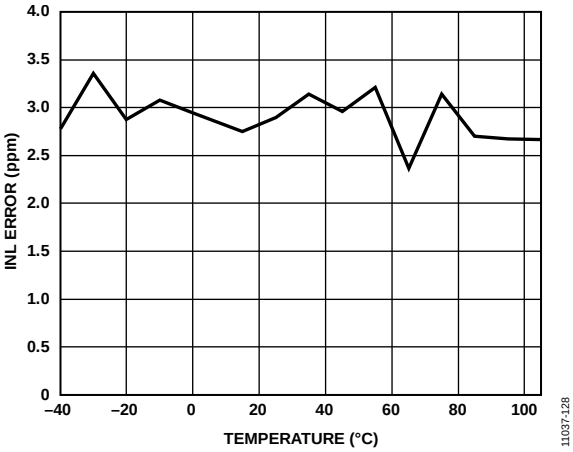


Figure 28. Integral Nonlinearity (INL) vs. Temperature (Differential Input, V_{REF} = 2.5 V)

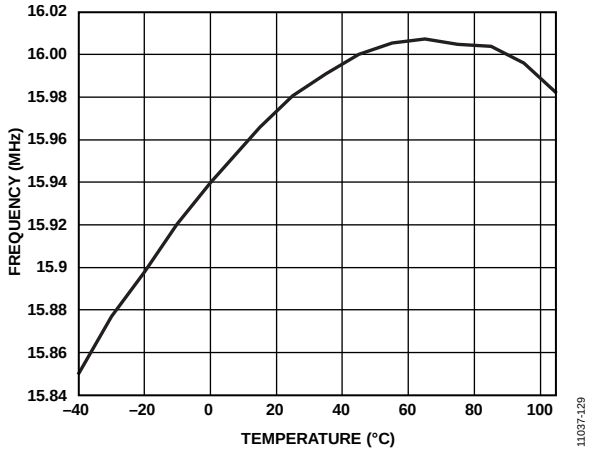


Figure 29. Internal Oscillator Frequency vs. Temperature

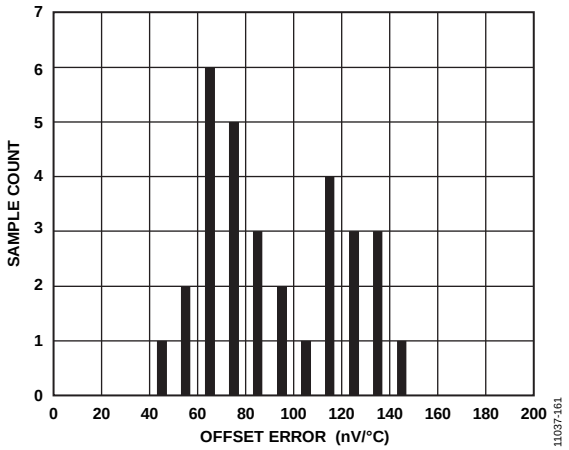


Figure 32. Offset Error Drift Distribution Histogram (Internal Short)

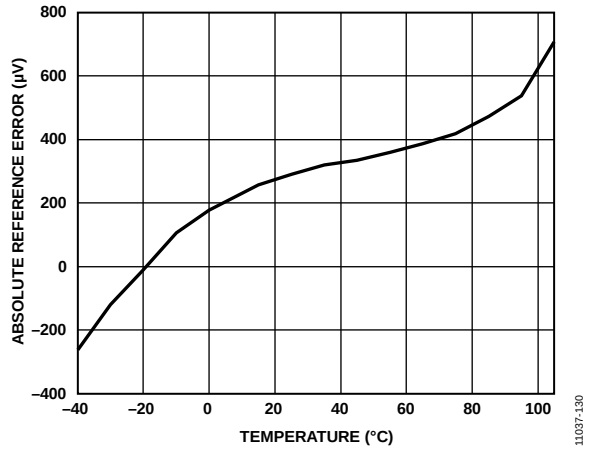


Figure 30. Absolute Reference Error vs. Temperature

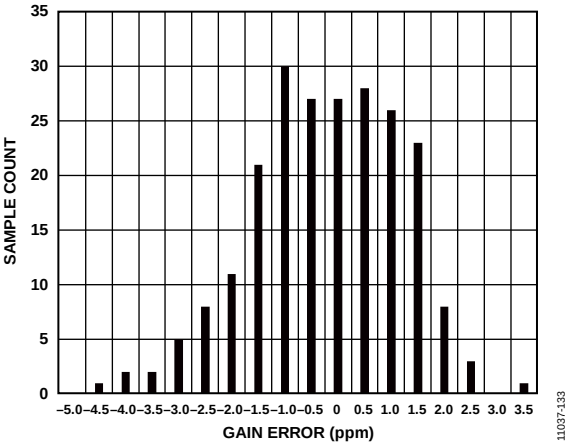


Figure 33. Gain Error Distribution Histogram

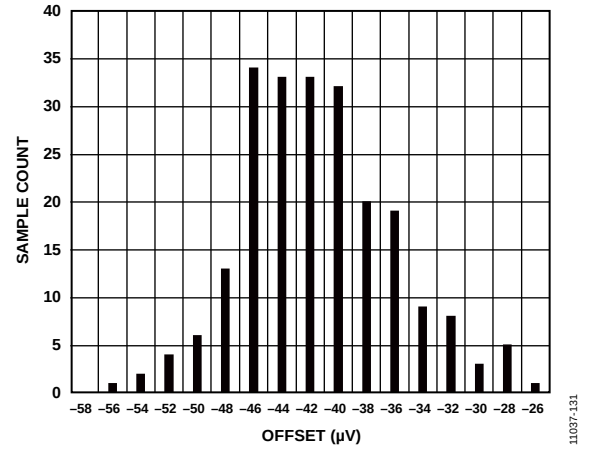


Figure 31. Offset Error Distribution Histogram (Internal Short)

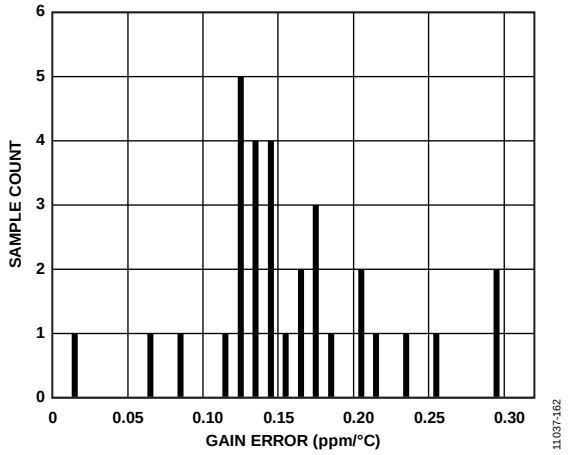


Figure 34. Gain Error Drift Distribution Histogram

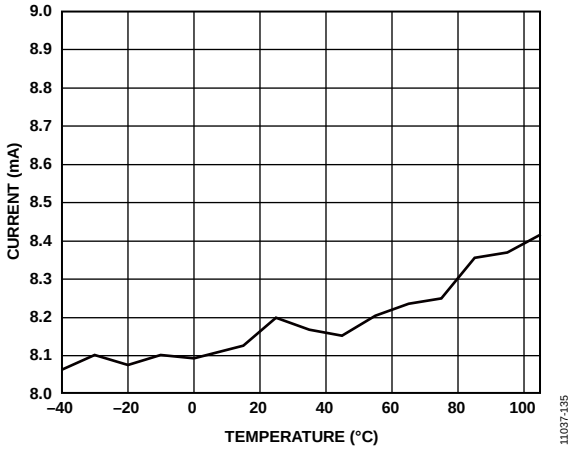


Figure 35. Current Consumption vs Temperature (Continous Conversion Mode)

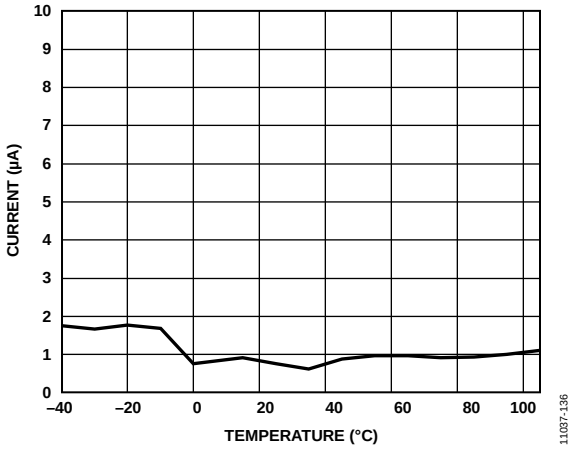


Figure 36. Current Consumption vs Temperature (Power Down Mode)

NOISE PERFORMANCE AND RESOLUTION

Table 6 shows the rms noise, peak-to-peak noise, effective resolution and the noise free (peak-to-peak) resolution of the AD7176-2 for various output data rates and filters. The numbers given are for the bipolar input range with an external 5 V reference.

These numbers are typical and are generated with a differential input voltage of 0 V when the ADC is continuously converting on a single channel. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

Table 6. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate Using Sinc5 + Sinc1 Filter (Default)[1]

	Sinc5 + Sinc1 Filter (Default)			
Output Data Rate (SPS)	**RMS Noise (μV rms)**	**Effective Resolution (Bits)**	**Peak-to-Peak Noise (μV rms)**	**Peak-to-Peak Resolution (Bits)**
250,000	9.7	20	66	17.3
62,500	5.4	20.8	35	18.1
10,000	2.6	21.9	16	19.2
1000	0.87	23.5	5.4	20.8
59.98	0.36	24.7	2.4	22
49.96	0.35	24.8	2.4	22
16.66	0.31	24.9	1.8	22.4
5	0.28	25.1	1.8	22.4

[1] Selected rates only, 1000 samples.

Table 7. RMS Noise and Peak-to-Peak Resolution vs. Output Data Rate Using Sinc3 Filter[1]

	Sinc3 Filter			
Output Data Rate (SPS)	**RMS Noise (μV rms)**	**Effective Resolution (Bits)**	**Peak-to-Peak Noise (μV rms)**	**Peak-to-Peak Resolution (Bits)**
250,000	220	15.5	1200	13
62,500	5.1	20.9	32	18.3
10,000	1.8	22.4	11	19.8
1000	0.62	24	4.8	21
60	0.31	25	2.4	22
50	0.31	25	2.4	22
16.66	0.28	25.1	1.8	22.4
5	0.28	25.1	1.8	22.4

[1] Selected rates only, 1000 samples.

GETTING STARTED

The AD7176-2 offers the user a fast settling, high resolution, multiplexed ADC with high levels of configurability.

- Two fully differential or four single-ended analog inputs.
- Crosspoint multiplexer selects any analog input combination as the input signals to be converted, routing them to the modulator positive or negative input.
- Fully differential input, single-ended relative to any analog input and pseudo differential configuration available.
- Per channel configurability—up to four different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure:
  - Gain and offset correction
  - Filter type
  - Output data rate when using sinc5 + sinc1 filter
  - Reference source selection (internal/external)

The AD7176-2 includes a precision 2.5 V low drift (2 ppm/°C) band gap internal reference. This reference can be selected to be used for the ADC conversions, reducing the external component count. Alternatively, the reference can be output to the REFOUT pin to be used as a low noise biasing voltage for the external circuitry. An example of this is using the REFOUT signal to set the input common mode for an external driving amplifier.

The AD7176-2 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulates the AVDD2 supply to 1.8 V supplying the ADC core. The user can tie the AVDD1 and AVDD2 supplies together for easiest connection. If there is already a clean analog supply rail in the system in the range of 2 V to 5 V, the user can also choose to connect this to the AVDD2 input, allowing for lower power dissipation.

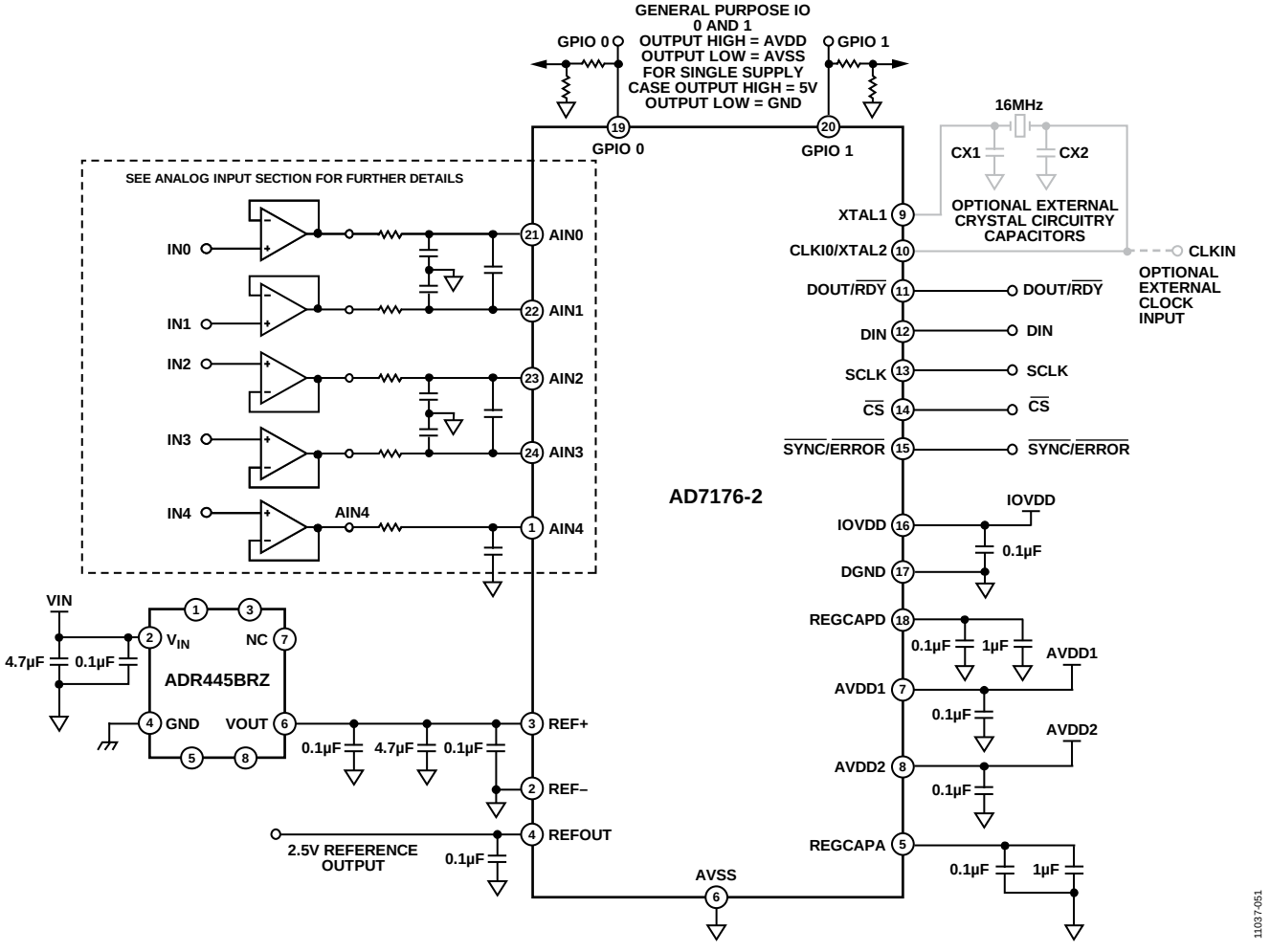


Figure 37. Typical Connection Diagram

The linear regulator for the digital IOVDD supply performs a similar function, regulating the input voltage applied at the IOVDD pin to 2 V for the internal digital filtering. The serial interface signals always operate from the IOVDD supply seen at the pin. This means that if 3.3 V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD7176-2 can be used across a wide variety of applications, providing high resolution and accuracy. A sample of these scenarios is as follows:

- Fast scanning of analog input channels using the internal multiplexer.
- Fast scanning of analog input channels using an external multiplexer.
- High resolution at lower speeds in either channel scanning or ADC per channel applications.
- Single ADC per channel: the fast low latency output allows further application specific filtering in an external microcontroller, DSP, or FPGA.

POWER SUPPLIES

The AD7176-2 has three independent power supply pins: AVDD1, AVDD2, and IOVDD.

AVDD1 powers the front-end circuitry, including the crosspoint multiplexer. AVDD1 is referenced to AVSS and AVDD1 − AVSS = 5 V only. This can be a single 5 V supply or a ±2.5 V split supply. The split supply operation allows for true bipolar inputs. When using split supplies, the absolute maximum ratings (see the Absolute Maximum Ratings section) must be kept in mind.

AVDD2 powers the internal 1.8 V analog LDO regulator. This regulator powers the ADC core. AVDD2 is referenced to AVSS, and AVDD2 – AVSS can range from 5 V to 2 V.

IOVDD powers the internal 1.8 V digital LDO regulator. This regulator powers the digital logic of the ADC. IOVDD sets the voltage levels for the SPI interface of the ADC. IOVDD is referenced to DGND, and IOVDD − DGND can vary from 5 V to 2 V.

There is no specific requirement for a power supply sequence on the AD7176-2. When all power supplies are stable, a device reset is required; see the AD7176-2 Reset section for details on how to reset the device.

DIGITAL COMMUNICATION

The AD7176-2 has a 3- or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ tied low. In SPI Mode 3, the SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

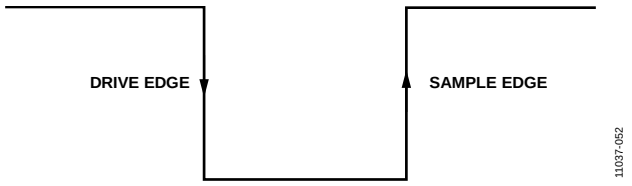


Figure 38. SPI Mode 3 SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expected a write to the communications register; therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The register address bits (RA[5:0]) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its defaults state, where it expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire part, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to its default state and aborts any current operation.

Figure 39 and Figure 40 illustrate writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for that register.

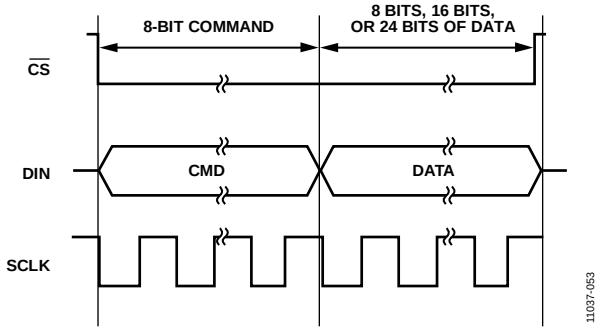


Figure 39. Writing to a Register
(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length Is Dependent on the Register Selected)

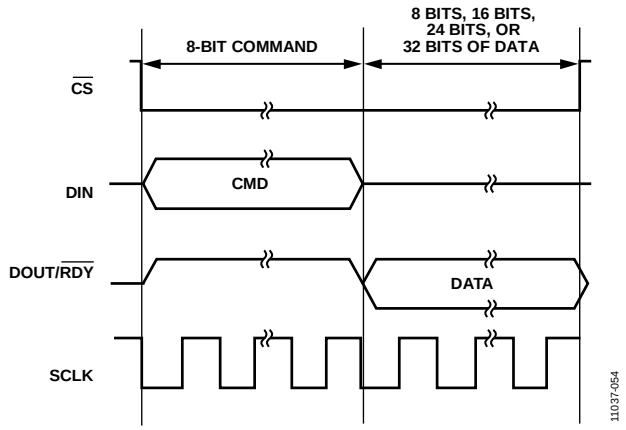


Figure 40. Reading from a Register
(8-Bit Command with Register Address Followed by Data of 8, 16, or 24 Bits; Data Length on DOUT Is Dependent on the Register Selected)

Reading the ID register is the recommended method for verifying correct communication with the part. The ID registers is a read only register and contains the value 0x0C9X for the AD7176-2. The communication register and ID register details are described in Table 8 and Table 9.

AD7176-2 RESET

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire part, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to its default state and aborts any current operation.

Table 8. Communications Register

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W

Table 9. ID Register

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x07	ID	[15:8]	ID[15:8]								0x0C9X	R
		[7:0]	ID[7:0]									

CONFIGURATION OVERVIEW

After power on-or reset, the AD7176-2 default configuration is as follows:

- Channel configuration. CH0 is enabled, AIN0 is selected as the positive input, and AIN1 is selected as the negative input. Setup 0 is selected.
- Setup configuration. The internal reference is selected.
- ADC mode. Continuous conversion mode and the internal oscillator are enabled.
- Interface mode. CRC is disabled, and data + status output is disabled.

Note that only a few of the register setting options are shown; this list is just an example. For full register information, see the Register Details section.

Figure 41 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 41).
- Setup configuration (see Box B in Figure 41).
- ADC mode and interface mode configuration (see Box C in Figure 41).

Channel Configuration

The AD7176-2 has four independent channels and four independent setups. The user can select any of the analog input pairs on any channel, as well as any of the four setups for any channel, giving the user full flexibility in the channel configuration. This also allows per channel configuration when using differential inputs and single-ended inputs because each channel can have its own dedicated setup.

Channel Registers

The channel registers are used to select which of the five analog input pins (AIN0 to AIN4) are used as either the positive analog input or the negative analog input for that channel. This register also contains a channel enable/disable bit and the setup selection bits, which are used to pick which of the eight available setups are used for this channel.

When the AD7176-2 operates with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 3. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 10.

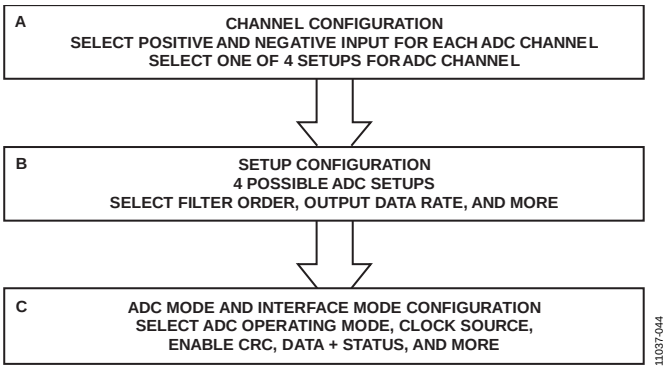


Figure 41. Suggested ADC Configuration Flow

Table 10. Channel 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL[2:0]			RESERVED		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]				AINNEG0					

ADC Setups

The AD7176-2 has four independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Offset register
- Gain register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Offset Register 0, and Gain Register 0. Figure 42 shows the grouping of these registers The setup is selectable from the channel registers detailed in the Channel Configuration section. This allows each channel to be assigned to one of four separate setups. Table 11 through Table 14 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 3.

Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar and unipolar. In bipolar mode, the ADC accepts negative differential input voltages, and the output coding is offset binary. In unipolar mode, the ADC accepts only positive differential voltages, and the coding is straight binary. In either case, the input voltage must be within the AVDD1/AVSS supply voltages. The user can also select the reference source using this register. Three options are available: an internal 2.5 V reference, an external reference connected between the REF+ and REF− pins, or AVDD1 − AVSS.

Filter Configuration Registers

The filter configuration register selects which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate is selected by setting the bits in this register. For more information, see the Digital Filters section.

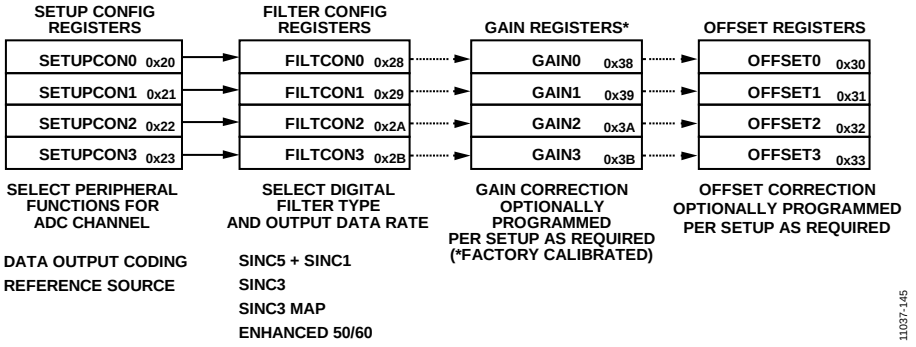


Figure 42. ADC Setup Register Grouping

Table 11. Setup Configuration 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	RESERVED				0x1000	RW
		[7:0]	RESERVED		REF_SEL0		RESERVED					

Table 12. Filter Configuration 0 Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x28	FILTCON0		SINC3_MAP0	RESERVED			ENHFILTEN0	ENHFILT0			0x0000	RW
				ORDER0		ODR0						

Table 13. Offset Configuration 0 Register Bit Map

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x30	OFFSET0	[23:0]	OFFSET0[23:0]	0x800000	RW

Table 14. Gain Configuration 0 Register Bit Map

Reg	Name	Bits	Bit[23:0]	Reset	RW
0x38	GAIN0	[23:0]	GAIN0[23:0]	0x5XXXX0	RW

Offset Registers

The offset register holds the offset calibration coefficient for the ADC. The power-on reset value of the offset register is 0x800000. The offset register is a 24-bit read/write register. The power-on reset value is automatically overwritten if an internal or system zero-scale calibration is initiated by the user or if the offset register is written to by the user.

Gain Registers

The gain register is a 24-bit register that holds the gain calibration coefficient for the ADC. The gain registers are read/write registers. These registers are configured at power-on with factory calibrated coefficients. Therefore, every device has different default coefficients. The default value is automatically overwritten if a system full-scale calibration is initiated by the user or if the gain register is written to by the user. For more information on calibration, see the Operating Modes section.

ADC Mode and Interface Mode Configuration

The ADC mode register and the interface mode register configure the core peripherals for use by the AD7176-2 and the mode for the digital interface.

ADC Mode Register

The ADC mode register is used primarily to set the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and the internal reference enable bits. The reference select bits are contained in the setup configuration registers (see the ADC Setups section for more information).

Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data + status read and continuous read mode. The details of both registers are shown in Table 15 and Table 16. For more information, see the Digital Interface section.

Table 15. ADC Mode Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x8000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			

Table 16. Interface Mode Register Bit Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	IOSTRENGTH	$\overline{\text{HIDE\_DELAY}}$	RESERVED	DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		

Understanding Configuration Flexibility

The most straightforward implementation of the AD7176-2 is to use two differential inputs with adjacent analog inputs and run both of them with the same setup, gain correction, and offset correction register. In this case, the user selects the following differential inputs: AIN0/AIN1 and AIN2/AIN3. In Figure 43, the registers shown in black font must be programmed for such a configuration. The registers that are shown in gray font are redundant in this configuration.

Programming the gain and offset registers is optional for any use case, as indicated by the dashed lines between the register blocks.

An alternative way to implement these two fully differential inputs is by taking advantage of the four available setups. Motivation for doing this includes having is a different speed/noise requirement on each of the two differential inputs vs. other inputs, or there may be a specific offset or gain correction for each channel. Figure 44 shows how each of the differential inputs may use a separate setup, allowing full flexibility in the configuration of each channel.

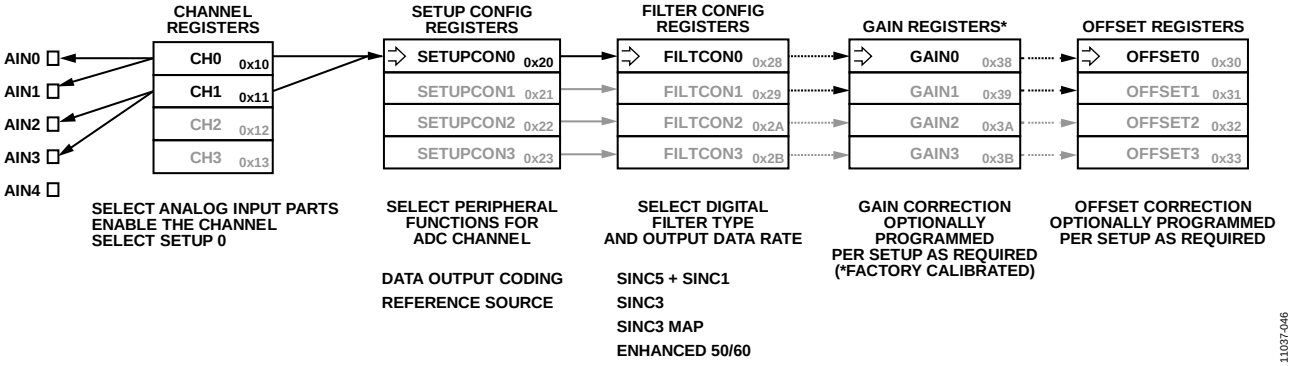


Figure 43. Two Fully Differential Inputs, Both Using a Single Setup (SETUPCON0; FILTCON0; GAIN0; OFFSET0)

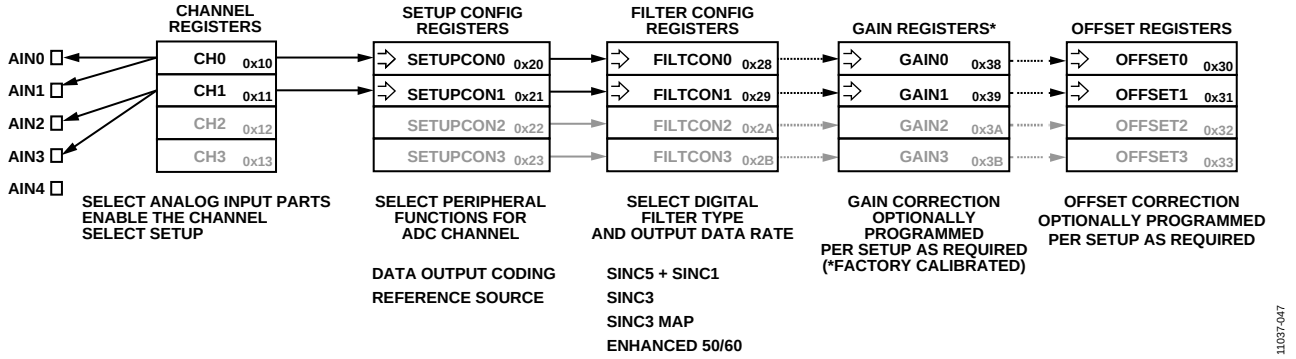


Figure 44. Two Fully Differential Inputs with a Setup per Channel

Figure 45 shows an example of how the channel registers span between the analog input pins and the setup configurations downstream. In this example, one differential input and two single-ended inputs are required. The single-ended inputs are the AIN2/AIN4 and AIN3/AIN4 combinations. The differential input pairs is AIN0/AIN1and uses setup 0. The two single-ended input pairs are set up as a diagnostics; therefore, use a separate setup from the differential input but share a setup between them, setup 1. Given that two setups are selected for use, the SETUPCON0 and SETUPCON1 registers are programmed as required, and the FILTCON0 and FILTCON1 registers are also programmed as desired. Optional gain and offset correction can be employed on a per setup basis by programming the GAIN0 and GAIN1 registers and the OFFSET0 and OFFSET1 registers.

In the example shown in Figure 45, the CH0 to CH2 registers are used. Setting the MSB in each of these registers, the CH_EN0 to CH_EN2 bits enable the 3 combinations via the cross point mux. When the AD7176-2 converts, the sequencer transitions in ascending sequential order from CH0 to CH1 to CH2 before looping back to CH0 to repeat the sequence.

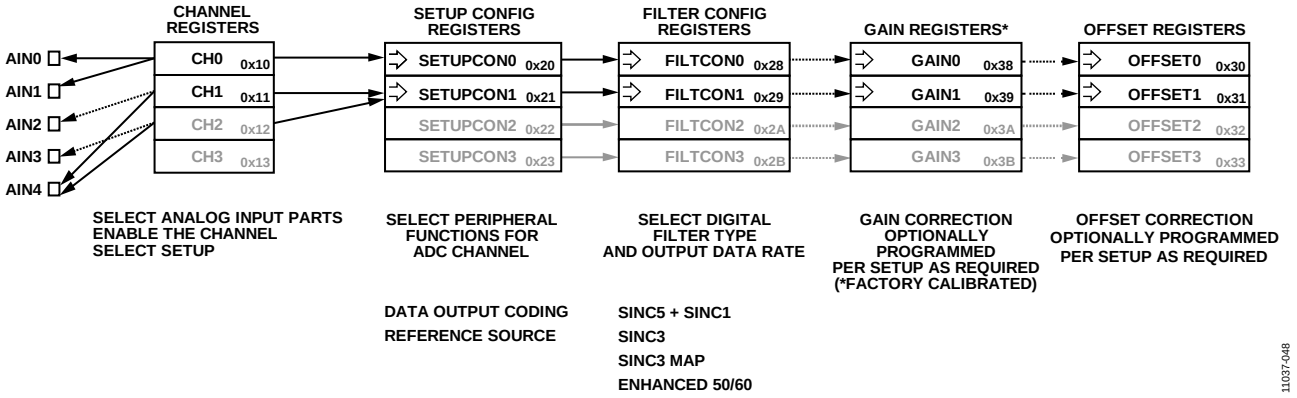


Figure 45. Mixed Differential and Single-Ended Configuration Using Multiple Shared Setups

CIRCUIT DESCRIPTION

ANALOG INPUT

The AD7176-2 has five analog input pins: AIN0, AIN1, AIN2, AIN3, and AIN4. Each of these pins connects to the internal crosspoint multiplexer. The crosspoint multiplexer enables any of these inputs to be configured as an input pair, either pseudo differential or fully differential. The AD7176-2 can have up to four active channels. When more than one channel is enabled, the channels are automatically sequenced in order. The output of the multiplexer is connected directly to the switched-capacitor input of the ADC. The simplified analog input circuit is shown in Figure 46.

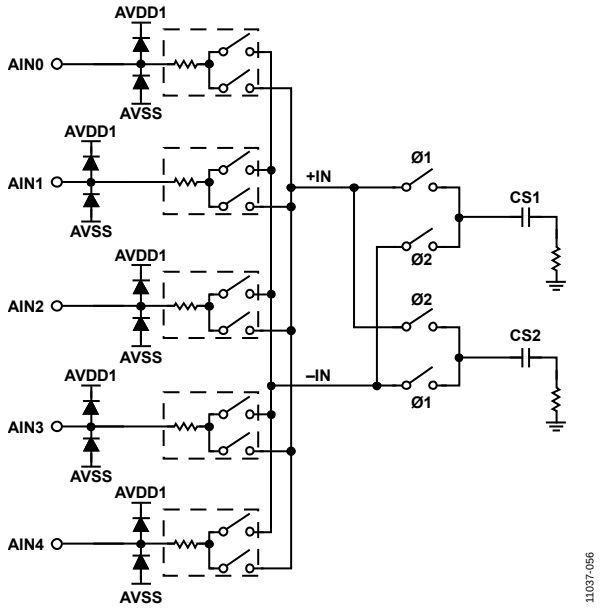


Figure 46. Simplified Analog Input Circuit

The CS1 and CS2 capacitors have a magnitude in the order of a number of picofarads each. This capacitance is the combination of both the sampling capacitance and the parasitic capacitance. The average input current to the AD7176-2 changes linearly with the differential input voltage at a rate of 48 µA/V. Each of the analog inputs must be buffered externally not only to provide the varying input current with differential input amplitude but also to settle the switched-capacitor input to allow for accurate sampling.

Recommended amplifiers for this purpose are discussed in the Driver Amplifiers section.

Fully Differential Inputs

Because the AIN0 to AIN4 analog inputs are connected to a crosspoint multiplexer, any combination of signals can be used to create an analog input pair. This allows the user to select two fully differential inputs or four pseudo differential inputs.

If two fully differential input paths are connected to the AD7176-2, using AIN0/AIN1 as one differential input pair and AIN2/AIN3 as the second differential input pair is recommended. This is due to the relative locations of these pins to each other. All analog inputs should be decoupled to AVSS.

Pseudo Differential Inputs

The user can also choose to measure four different single-ended analog inputs. In this case, each of the analog inputs is converted as being the difference between the single-ended input to be measured and a set analog input common pin. Because there is a crosspoint multiplexer, the user can set any of the analog inputs as the common pin. An example of such a scenario is to connect the AIN4 pin to AVSS or to the REFOUT voltage (that is, AVSS + 2.5 V) and select this input when configuring the crosspoint multiplexer. When using the AD7176-2 with pseudo differential inputs, the INL specification is degraded.

DRIVER AMPLIFIERS

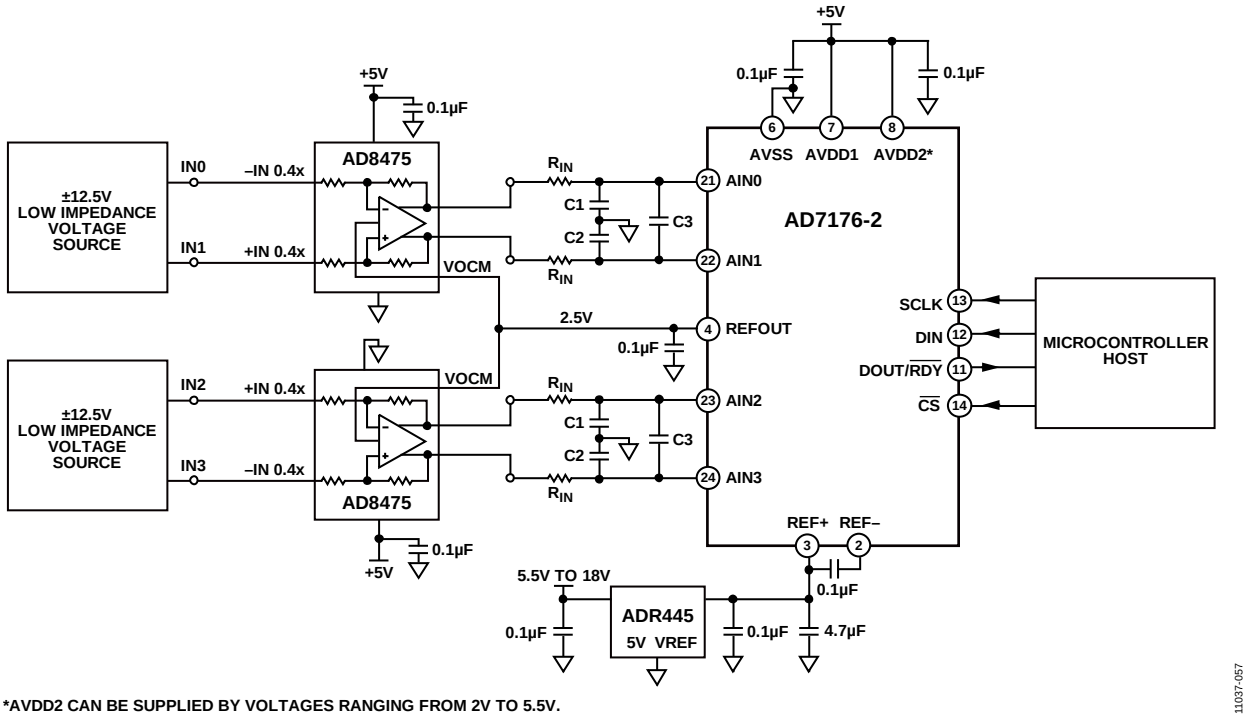
To drive the analog input switch capacitor, an external amplifier is required. Details of three recommended amplifiers for the AD7176-2 are shown in the Driver Amplifiers section. Each of the amplifiers can run from a single 5 V voltage rail.

AD8475

The AD8475 features an attenuating input stage of 0.8× or 0.4× (using integrated precision resistors), allowing inputs in the ±10 V range with a single 5 V supply and a 3 mA current consumption to be used. The AD8475 performs single-ended to differential conversions, allows easy setting of the common-mode output, and drives the AD7176-2 with a differential input.

Figure 47 shows a typical connection to the AD7176-2, where two AD8475 amplifiers attenuate two differential inputs and then drive the AD7176-2 inputs. The common-mode output of the AD8475 is set by connecting the internal, buffered 2.5 V reference of the AD7176-2 to the VOCM pin of the AD8475. The output of the AD8475 to the AD7176-2 is fully differential with a fixed common mode of 2.5 V. The output of the AD8475 amplifier is connected to an RC network. The RC network, as shown in Figure 47, includes R_{IN} = 10 Ω; C1, C2 = 270 pF; and C3 = 680 pF. The RC circuit acts to provide the dynamic charge required by the AD7176-2 switched sampling capacitors while isolating the amplifier output from any kickback from the dynamic switched capacitor input. The configuration of the AD8475 in Figure 47 shows a fully differential signal source with a gain of 0.4×.

The AD8475 can also be set up to convert single-ended signals to fully differential inputs. Ground the −IN 0.4× input and apply the single-ended input to the +IN 0.4× input.



*AVDD2 CAN BE SUPPLIED BY VOLTAGES RANGING FROM 2V TO 5.5V.

Figure 47. AD8475 Driving Two Differential Inputs of the AD7176-2

AD8656

The AD8656 is a low noise, dual precision CMOS amplifier. The AD8656 allows the user to connect a signal of interest directly to a high impedance, low noise, low offset amplifier input that can drive the AD7176-2 switched capacitor input. The AD8656 can operate from a single 5 V supply. When using an external 5 V reference such as the ADR445 in conjunction with the AD7176-2, the AD8656 output can swing to within −1 dBFS (which equates to a differential input of ±4.45 V) of the ADC input range.

A simple configuration for use of the AD8656 is to connect the amplifiers in a configuration for a gain of more than 1. Each of the AD7176-2 analog inputs has its own amplifier. This allows the user to connect either fully differential inputs or single-ended inputs to the AD7176-2. The example shown in Figure 48 is configured with two fully differential inputs connecting to the AIN0/AIN1 pair and the AIN2/AIN3 pair.

The high impedance input to the amplifier allows the user to band-limit the input with a suitable passive filter RC combination. The gain of the configuration used is set by the R_G and R_F resistors.

To improve accuracy, use precision resistors for R_G and R_F. Setting $R_G = R_F = 1\ k\Omega$ results in a gain of 2 for the circuit. The matching of the RG and RF resistors directly affects the gain error of the circuit. The drift and matching of these resistors affect the gain error drift of the circuit. A 10 Ω source resistor (R_S) is placed between the feedback resistor (R_F) and the amplifier output. This resistor acts to isolate the amplifier from any kickback from the ADC input and does not directly affect the gain error of the circuit.

The output of each of the amplifier pairs is connected directly to a network of decoupling and differential capacitors prior to being connected to the AD7176-2 analog inputs. The capacitor network shown in Figure 48 includes C1, C2 = 270 pF and C3 = 680 pF. The capacitor network acts to provide the dynamic charge required by the AD7176-2 switched sampling capacitors.

The circuit example in Figure 48 requires inclusion of two precision gain resistors per amplifier (R_G and R_F). Choose the value, precision, and matching of such resistors according to the requirements of the application.

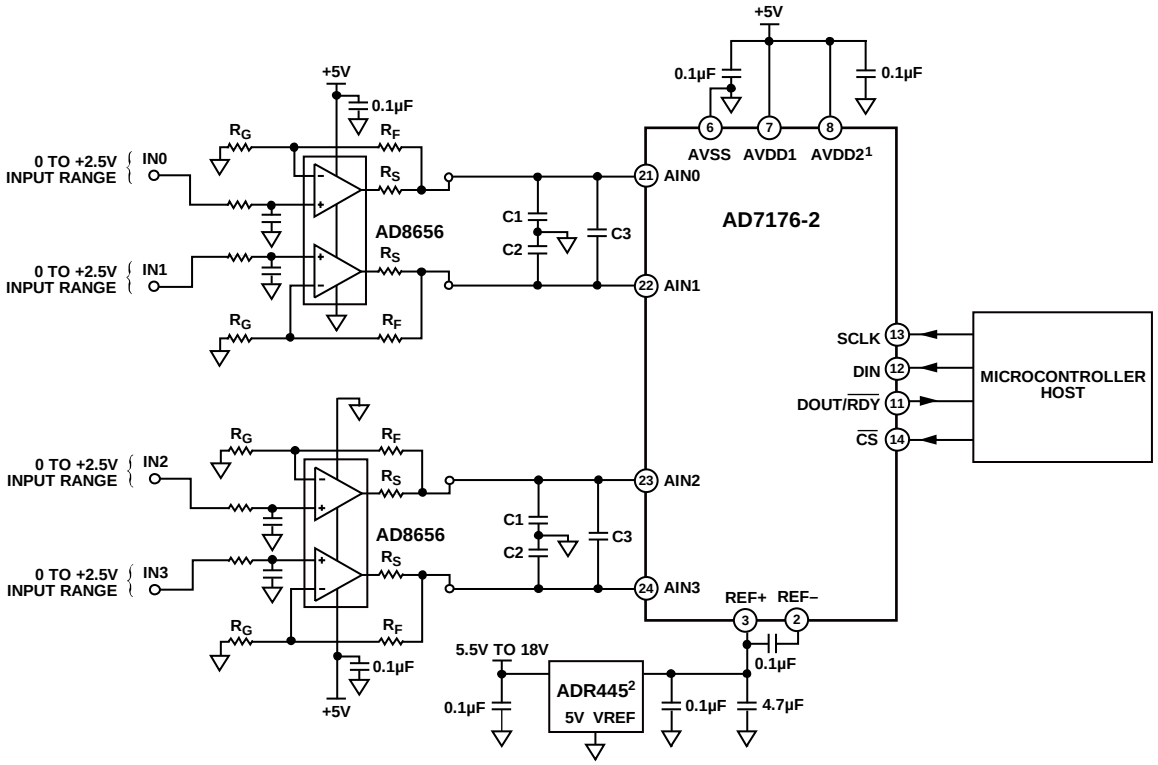


Figure 48. Dual AD8656 Amplifiers Driving the AD7176-2

ADA4940-1/ADA4940-2

The ADA4940-1/ADA4940-2 is an alternate option to drive the AD7176-2. It is a low noise, low distortion fully differential amplifier with very low power consumption (1.25 mA of quiescent current). The AD7176-2 REFOUT pin can be used to connect to the ADA4940-1/ADA4940-2 to set the common-mode output to 2.5 V. This option requires the use of external resistors to set the gain of the amplifier.

AD7176-2 REFERENCE

The AD7176-2 offers the user the option of either supplying an external reference to the REF+ and REF− pins of the device or allowing the use of the internal 2.5 V, low noise, low drift reference. Select the reference source to be used by the analog input by setting the REF_SELx bits (Bits[5:4]) in the setup configuration registers appropriately. The structure of the Setup Configuration 0 register is shown in Table 17. The AD7176-2 defaults on power-up to use the internal 2.5 V reference.

External Reference

The AD7176-2 has a fully differential reference input applied through the REF+ and REF− pins. Standard low noise, low drift voltage references, such as the ADR445, ADR444, and ADR441, are recommended for use. The external reference should be applied to the AD7176-2 reference pins as shown in Figure 49. The output of any external reference should be decoupled to AVSS. As shown in Figure 49, the ADR445 output is decoupled with a 0.1 µF capacitor at its output for stability purposes. The output is then connected to a 4.7 µF capacitor, which acts as a reservoir for any dynamic charge required by the ADC, and followed by a 0.1 µF decoupling capacitor at the REF+ input. This capacitor is placed as close as possible to the REF+ and REF− pins. The REF− pin is connected directly to the AVSS potential. On power-up of the AD7176-2, the internal reference is enabled by default and is output on the REFOUT pin. When an external reference is used instead of the internal reference to supply the AD7176-2, attention must be paid to the output of the REFOUT pin. If the internal reference is not being used elsewhere in the application, ensure that the REFOUT pin is not hardwired to AVSS because this will draw a large current on power-up. On power-up if the internal reference is not being used, write to the ADC mode register, disabling the internal reference. This is controlled by the REF_EN bit (Bit 15) in the ADC mode register and is shown in Table 18.

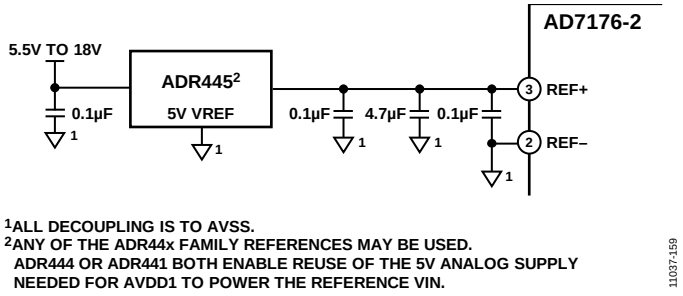


Figure 49. External Reference ADR445 Connected to AD7176-2 Reference Pins

Table 17. Setup Configuration 0 Register

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	RESERVED				0x1020	RW
		[7:0]	RESERVED		REF_SEL0		RESERVED					

Table 18. ADC Mode Register

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x01	ADCMODE	[15:8]	REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x8000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL	RESERVED				

Internal Reference

The AD7176-2 includes its own low noise, low drift voltage reference. The internal reference has a 2.5 V output. The internal reference is output on the REFOUT pin after the REF_EN bit in the ADC mode register is set and is decoupled to AVSS with a 0.1 µF capacitor. The AD7176-2 internal reference is enabled by default on power-up and is selected as the reference source for the ADC.

The REFOUT signal is buffered prior to being output to the pin. The signal can be used externally in the circuit as a common-mode source for external amplifier configurations. This is shown in Figure 47 in the Driver Amplifiers section, where the REFOUT pin supplies the VOCM input of the AD8475 amplifier.

AD7176-2 CLOCK SOURCE

The AD7176-2 requires a master clock of 16 MHz. The AD7176-2 can source its sampling clock from one of three scenarios:

- Internal oscillator
- External crystal
- External clock source

All output data rates listed in the data sheet relate to a master clock rate of 16 MHz. Using a lower clock frequency from, for instance, an external source will scale any listed data rate proportionally. To achieve the specified data rates, particularly rates for rejection of 50 Hz and 60 Hz, a 16 MHz clock should be used. The source of the master clock is selected by setting the CLOCKSEL bits (Bits[3:2]) in the ADC mode register as shown in Table 18. The default operation on power-up and reset of the AD7176-2 is to operate with the internal oscillator.

Internal Oscillator

The internal oscillator runs at 16 MHz and can be used as the ADC master clock. It is the default clock source for the AD7176-2 and is specified with an accuracy of ±2.5%.

There is an option to allow the internal clock oscillator to be output on the AD7176-2 CLKIO/XTAL2 pin. The clock output is driven to the IOVDD logic level. Use of this option can affect the dc performance of the AD7176-2 due to the disturbance introduced by the output driver. The extent to which the performance is affected depends on the IOVDD voltage supply. Higher IOVDD voltages create a wider logic output swing from the driver and affect performance to a greater extent. This is further exaggerated if the IOSTRENGTH bit is set at higher IOVDD levels (see Table 26 for more information).

External Crystal

If higher precision, lower jitter clock sources are required, the AD7176-2 has the ability to use an external crystal to generate the master clock. The crystal is connected to the XTAL1 and XTAL2 pins. A recommended crystal for use is the FA-20H—a 16 MHz, 10 ppm, 9 pF crystal from Epson-Toyocom—which is available in a surface-mounted package. As shown in Figure 50, allow for two capacitors to be inserted from the traces connecting the crystal to the XTAL1 and XTAL2 pins. These capacitors allow for circuit tuning. Connect these capacitors to the DGND pin. The value for these capacitors depends on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2 pins. Therefore, the values of these capacitors differ depending on the PCB layout and the crystal employed. As a result, empirical testing of the circuit is required.

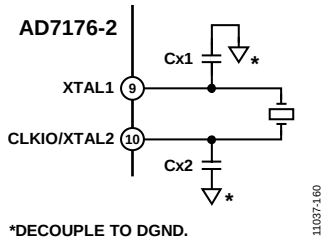


Figure 50. External Crystal Connections

External Clock

The AD7176-2 can also use an externally supplied clock. In systems where this is desirable, the external clock is routed to the CLKIO pin. In this configuration, the CLKIO pin accepts the externally sourced clock and routes it to the modulator. The logic level of this clock input is defined by the voltage applied to the IOVDD pin.

DIGITAL FILTERS

The AD7176-2 has three flexible filter options to allow for optimization of noise, settling time, and rejection:

- Sinc5 + sinc1 filter
- Sinc3 filter
- Enhanced 50 Hz and 60 Hz rejection filters

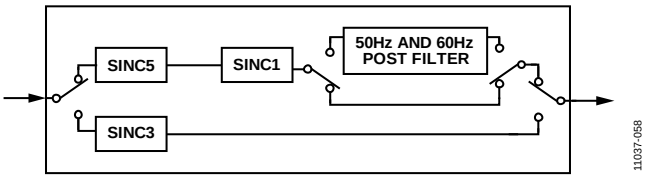


Figure 51. Digital Filter Block Diagram

The filter and output data rate is configured by setting the appropriate bits in the filter configuration register for the selected setup. When using the sinc5 + sinc1 filter, the user can select different output data rates per channel. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels. See the Register Details section for more information.

SINC5 + SINC1 FILTER

The sinc5 + sinc1 filter is targeted at fast switching multiplexed applications and achieves single cycle settling at output data rates of 10 kSPS and lower. The sinc5 block output is fixed at the maximum rate of 250 kSPS, and the sinc1 block output data rate can be varied to control the final ADC output data rate. Figure 52 shows the frequency domain response of the sinc5 + sinc1 filter at a 50 SPS output data rate. The sinc5 + sinc1 filter has a slow roll-off over frequency and narrow notches.

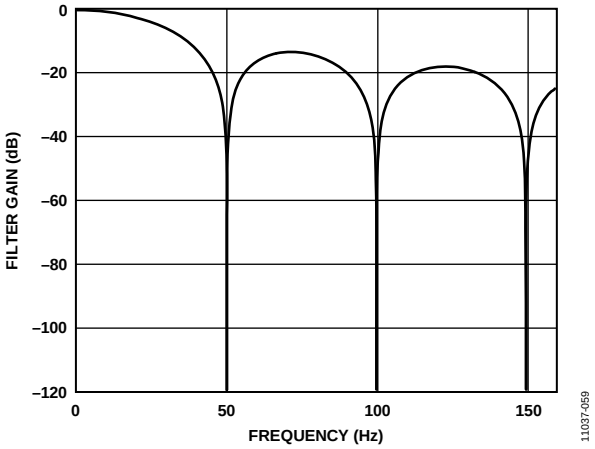


Figure 52. Sinc5 + Sinc1 Filter Response at 50 SPS ODR

The output data rates with the accompanying settling time and rms noise for the sinc5 + sinc1 filter are shown in Table 19.

Table 19. AD7176-2 Output Data Rate (ODR), Settling Time (t_{SETTLE}), and Noise Using the Sinc5 + Sinc1 Filter

Default Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled[1]	Output Data Rate (SPS/Channel); SING_CYC = 1 or with Multiple Channels Enabled[1]	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)	Noise (µV p-p)[2]	Effective Resolution with 5 V Reference (Bits)	Peak-to-Peak Resolution with 5 V Reference (Bits)
250,000	50,000	20 µs	250,000	9.7	66	20	17.3
125,000	41,667	24 µs	125,000	7.4	50	20.4	17.6
62,500	31,250	32 µs	62,500	5.4	35	20.8	18.1
50,000	27,778	36 µs	50,000	5	33	20.9	18.2
31,250	20,833	48 µs	31,250	4	26	21.3	18.5
25,000	17,857	56 µs	25,000	3.6	24	21.4	18.7
15,625	12,500	80 µs	15,625	2.9	17	21.7	19.1
10,000	10,000	100 µs	11,905	2.6	16	21.9	19.2
5000	5000	200 µs	5435	1.8	12	22.4	19.7
2500	2500	400 µs	2604	1.3	8.9	22.8	20.1
1000	1000	1.0 ms	1016	0.87	5.4	23.5	20.8
500	500.0	2.0 ms	504	0.7	4.8	23.8	21
397.5	397.5	2.516 ms	400.00	0.62	4.8	23.9	21
200	200.0	5.0 ms	200.64	0.49	3.6	24	21.4
100.2	100.2	9.976 ms	100.4	0.4	3	24	21.7
59.98	59.98	16.67 ms	59.98	0.36	2.4	24	22
49.96	49.96	20.016 ms	50.00	0.35	2.4	24	22
20	20.00	50.0 ms	20.01	0.31	2.4	24	22
16.66	16.66	60.02 ms	16.66	0.31	1.8	24	22.4
10	10.00	100 ms	10.00	0.29	1.8	24	22.4
5	5.00	200 ms	5.00	0.28	1.8	24	22.4

[1] The settling time has been rounded to the nearest microsecond. This is reflected in the output data rate and switching rate. Switching rate = 1 ÷ t_{SETTLE}.
[2] 1000 samples.

SINC3 FILTER

The sinc3 filter achieves the best single-channel noise performance at lower rates and is, therefore, most suitable for single-channel applications. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels. The sinc3 filter always has a settling time equal to

$$t_{SETTLE} = 3/Output\ Data\ Rate$$

Figure 53 shows the frequency domain filter response for the sinc3 filter. The sinc3 filter has good roll-off over frequency and has wide notches for good notch frequency rejection.

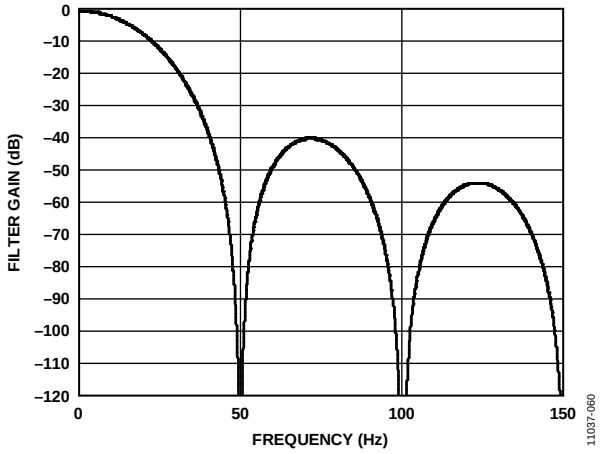


Figure 53. Sinc3 Filter Response

The output data rates with the accompanying settling time and rms noise for the sinc3 filter are shown in Table 20.

It is possible to finely tune the output data rate for the sinc3 filter by setting the SINC3_MAP bit in the filter configuration register. If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the sinc3 filter. All other options are eliminated. The data rate when on a single channel can be calculated using the following equation:

$$Output\ Data\ Rate = \frac{f_{MOD}}{32 \times FILTCONx[14:0]}$$

where:
f_{MOD} is the modulator rate and is 8 MHz.
FILTCONx[14:0] are the contents on the filter configuration register excluding the MSB.

For example, an output data rate of 50 SPS can be achieved with SINC3_MAP enabled by setting the FILTCONx[14:0] bits to a value of 5000.

SINGLE CYCLE SETTLING

The AD7176-2 can be configured by setting the SING_CYC bit in the ADC mode register so that only fully settled data is output, thus effectively putting the ADC into a single cycle settling mode. This mode achieves single cycle settling by reducing the output data rate to be equal to the settling time of the ADC for the selected output data rate. This bit has no effect with the sinc5 + sinc1 at output data rates of 10 kSPS and lower.

Figure 54 shows a step on the analog input with this mode disabled and the sinc3 filter selected. It takes at least three cycles after the step change for the output to reach the final settled value.

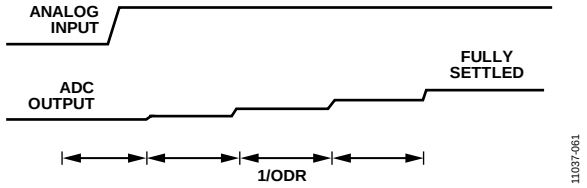


Figure 54. Step Input Without Single Cycle Settling

Figure 55 shows the same step on the analog input but with single cycle settling enabled. It takes at least a single cycle for the output to be fully settled. The output data rate is now reduced to equal the settling time of the filter at the selected output data rate.

Figure 55. Step Input with Single Cycle Settling

Table 20. AD7176-2 Output Data Rate (ODR), Settling Time (t_{SETTLE}), and Noise Using the Sinc3 Filter

Default Output Data Rate (SPS); SING_CYC = 0 and Single Channel Enabled[1]	Output Data Rate (SPS/Channel); SING_CYC = 1 or with Multiple Channels Enabled[1]	Settling Time (ms)[1]	Notch Frequency (Hz)	Noise (µV rms)	Noise (µV p-p)	Effective Resolution with 5V Reference (Bits)	Peak-to-Peak Resolution with 5 V Reference (Bits)
250,000	83,333	0.012	250,000	220	1200	15.5	13
125,000	41,667	0.024	125,000	28	170	18.4	15.9
62,500	20,833	0.048	62,500	5.1	32	20.9	18.3
50,000	16,667	0.060	50,000	4.2	27	21.2	18.5
31,250	10,417	0.096	31,250	3.2	21	21.6	18.8
25,000	8333	0.120	25,000	2.7	18	21.8	19
15,625	5208	0.192	15,625	2.3	15	22.1	19.4
10,000	3333	0.300	10,000	1.8	11	22.4	19.8
5000	1667	0.600	5000	1.3	8.3	22.9	20.2
2500	833	1.200	2500	0.91	6.6	23.4	20.5
1000	333.3	3.000	1000	0.62	4.8	24	21
500	166.7	6.000	500	0.49	3.6	24	21.4
400	133.3	7.500	400	0.45	3	24	21.7
200	66.7	15.000	200	0.37	2.4	24	22
100.2	33.41	29.928	100.2	0.31	2.4	24	22
60	19.99	50.016	59.98	0.31	2.4	24	22
50	16.67	60.000	50	0.31	2.4	24	22
20	6.67	150.000	20	0.28	1.8	24	22.4
16.67	5.56	180.000	16.67	0.28	1.8	24	22.4
10	3.33	300.000	10	0.28	1.8	24	22.4
5	1.67	600.000	5	0.28	1.8	24	22.4

[1] The settling time has been rounded to the nearest microsecond. This is reflected in the output data rate and switching rate. Switching rate = 1 ÷ t_{SETTLE}.

ENHANCED 50 HZ AND 60 HZ REJECTION FILTERS

The enhanced filters are designed to provide rejection of 50 Hz and 60 Hz simultaneously and to allow the user to trade off settling time and rejection. These filters can operate up to 27.27 SPS or can reject up to 90 dB of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz interference. These filters are realized by post filtering the output of the sinc5 + sinc1 filter. For this reason, the sinc5 + sinc1 filter must be selected when using the enhanced filters. Table 21 shows the output data rates with the accompanying settling time, rejection, and rms noise. Figure 56 to Figure 63 show the frequency domain plots of the responses from the enhanced filters.

Table 21. AD7176-2 Enhanced Filters Output Data Rate, Noise, Settling Time (t_{SETTLE}), and Rejection Using the Enhanced Filters

Output Data Rate (SPS)	Settling Time (ms)	Simultaneous Rejection of 50 Hz ± 1 Hz and 60 Hz ± 1 Hz (dB)[1]	Noise (µV rms)	Peak-to-Peak Resolution (Bits)	Comments
27.27	36.67	47	0.45	21.7	See Figure 56 and Figure 59
25	40.0	62	0.45	21.7	See Figure 57 and Figure 60
20	50.0	85	0.44	22	See Figure 58 and Figure 61
16.667	60.0	90	0.44	22	See Figure 62 and Figure 63

[1] Master clock = 16 MHz.

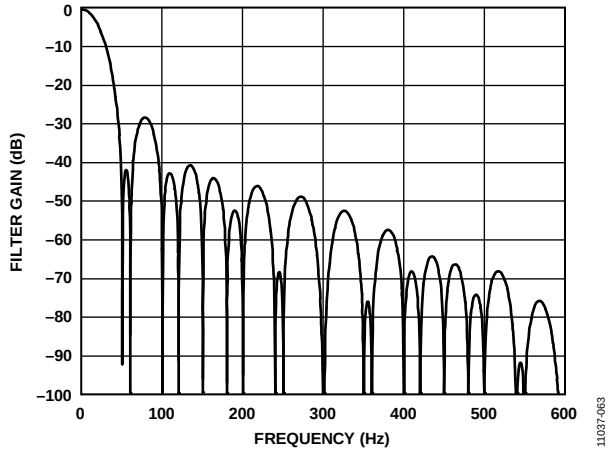


Figure 56. 27.27 SPS ODR, 36.67 ms Settling Time

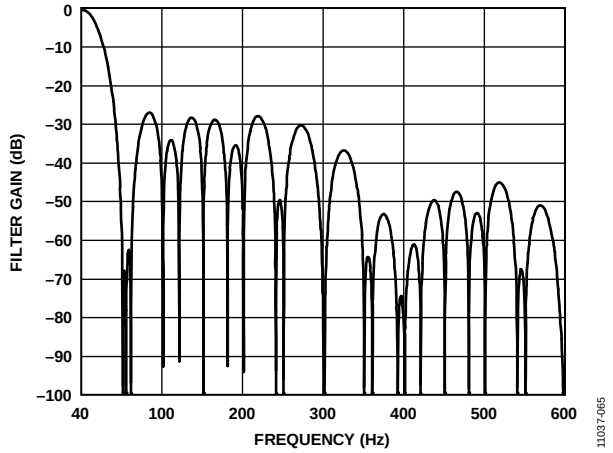


Figure 57. 25 SPS ODR, 40 ms Settling Time

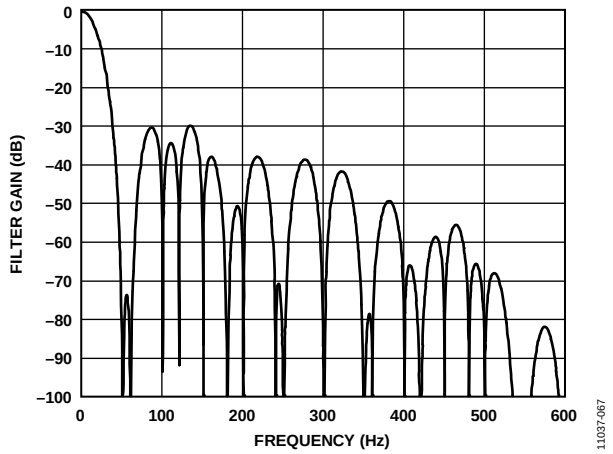


Figure 58. 20 SPS ODR, 50 ms Settling Time

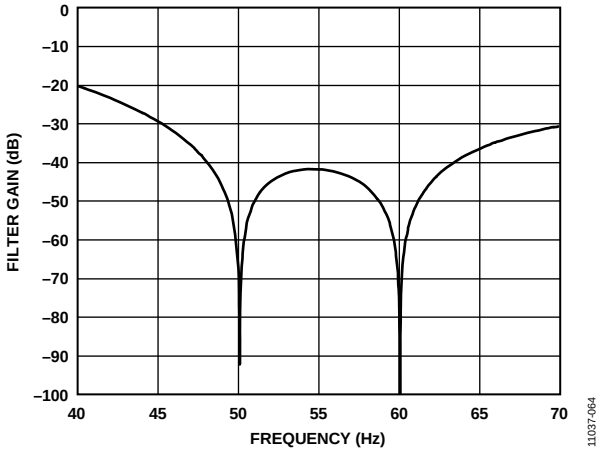


Figure 59. 27.27 SPS ODR, 36.67 ms Settling Time

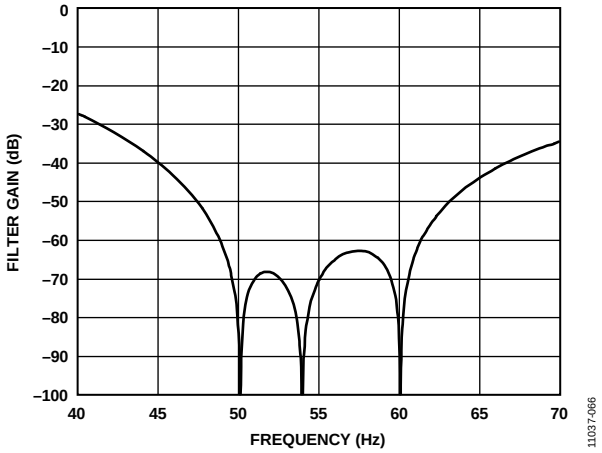


Figure 60. 25 SPS ODR, 40 ms Settling Time

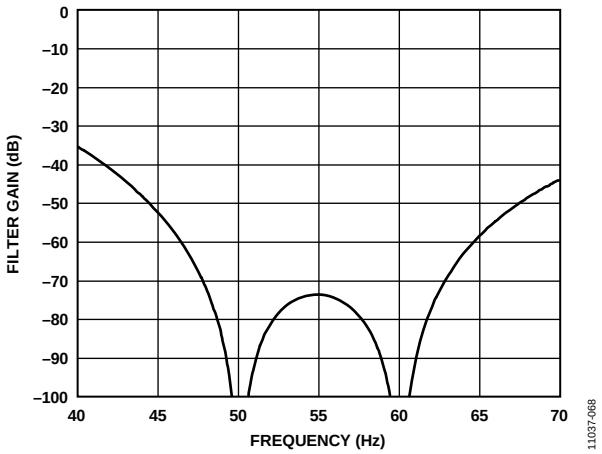


Figure 61. 20 SPS ODR, 50 ms Settling Time

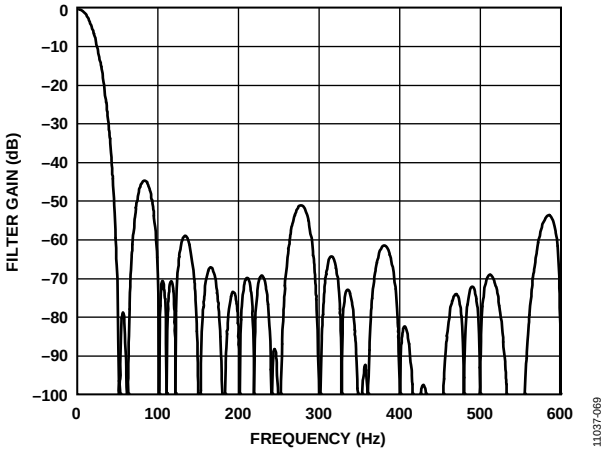


Figure 62. 16.667 SPS ODR, 60 ms Settling Time

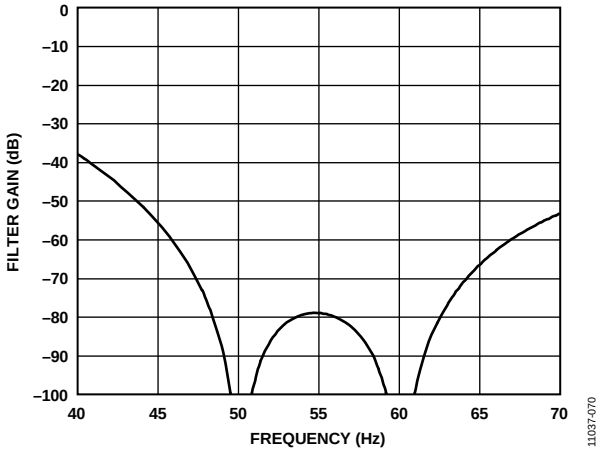


Figure 63. 16.667 SPS ODR, 60 ms Settling Time

OPERATING MODES

CONTINUOUS CONVERSION MODE

Continuous conversion is the default power-up mode. The AD7176-2 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register, indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The user can read this register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion; otherwise the new conversion word will be lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all channels have been converted, the sequence starts again with the first channel. The channels are converted in order from lowest enabled channel to highest enabled channel. The data register is updated as soon as each conversion is available. The DOUT/$\overline{RDY}$ pin pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The status register indicates the channel to which the conversion corresponds.

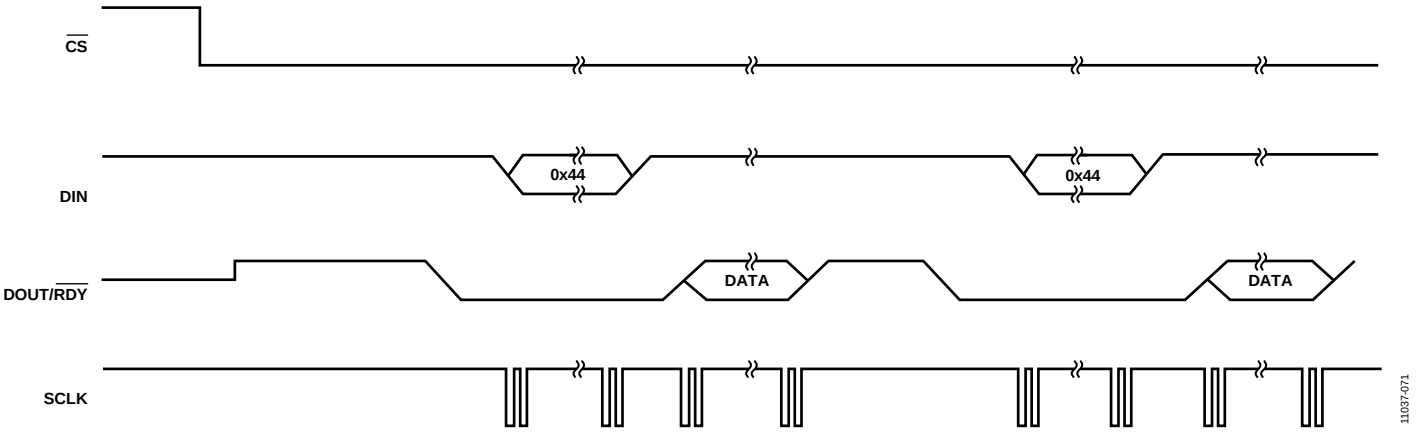


Figure 64. Continuous Conversion Mode

CONTINUOUS READ MODE

In continuous read mode, it is not required to write to the communications register before reading ADC data; just apply the required number of SCLKs after DOUT/$\overline{\text{RDY}}$ goes low to indicate the end of a conversion. When the conversion is read, DOUT/$\overline{\text{RDY}}$ returns high until the next conversion is available. In this mode, the data can be read only once. The user must also ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD7176-2 to read the word, the serial output register is reset when the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode.

To enable continuous read mode, set the CONTREAD bit in the interface mode register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while $\overline{\text{RDY}}$ is low. Alternatively, apply a software reset, that is, 64 SCLKs with $\overline{\text{CS}}$ = 0 and DIN = 1. This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. DIN should be held low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if DATA_STAT is set in the interface mode register. The status register indicates the channel to which the conversion corresponds.

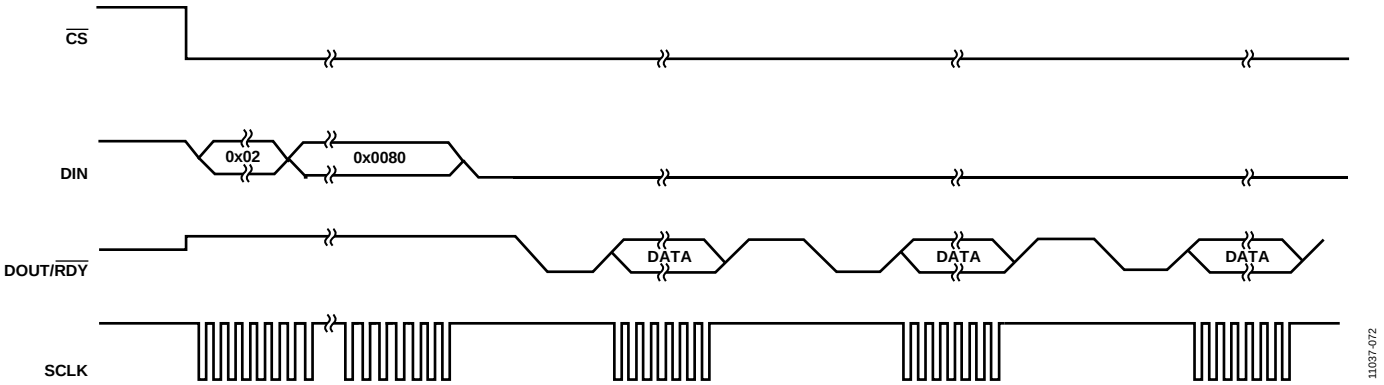


Figure 65. Continuous Read Mode

SINGLE CONVERSION MODE

In single conversion mode, the AD7176-2 performs a single conversion and is placed in standby mode after the conversion is complete. DOUT/$\overline{RDY}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{RDY}$ has gone high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{RDY}$ goes high and remains high until a valid conversion is available and $\overline{CS}$ is low. As soon as the conversion is available, DOUT/$\overline{RDY}$ goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. As soon as the next conversion is complete, the data register is updated; therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to standby mode.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion, are output each time the data register is read. The two LSBs of the status register indicate the channel to which the conversion corresponds.

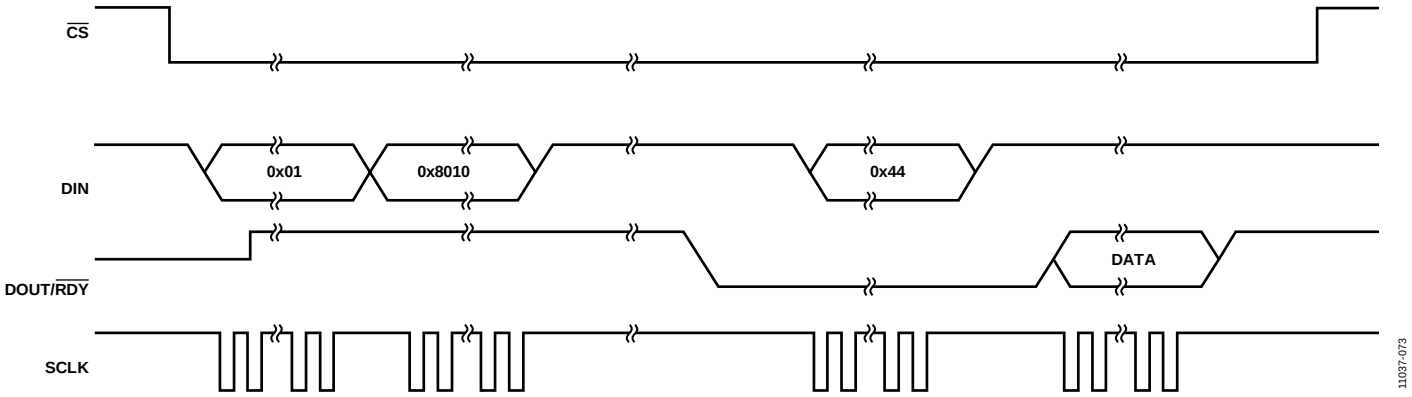


Figure 66. Single Conversion Mode

STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDOs remain active so that registers maintain their contents. The internal reference remains active if enabled, and the crystal oscillator remains active if selected. To power down the reference in standby mode, set the REF_EN bit in the ADC mode register to 0. To power down the clock in standby mode, set the CLOCKSEL bits in the ADC mode register to 00 (internal oscillator).

In power-down mode, all blocks are powered down, including the LDOs. All registers lose their contents, and the GPIO outputs are placed in tristate. To prevent accidental entry to power-down mode, the ADC must first be placed into standby mode. Exiting power-down mode requires 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1, that is, a serial interface reset. A delay of 500 µs is recommended before issuing a subsequent serial interface command to allow the LDO to power up.

Figure 21 shows the internal reference settling time after returning from the standby (setting REF_EN = 0 and then 1) and power down modes.

CALIBRATION MODES

The AD7176-2 provides three calibration modes that can be used to eliminate the offset and gain errors on a per setup basis:

- Internal zero-scale calibration mode
- System zero-scale calibration mode
- System full-scale calibration mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x800000, and the nominal value of the gain register is 0x555555. The calibration range of the ADC gain is from 0.4 × V_{REF} to 1.05 × V_{REF}. The following equations show the calculations that are used. In unipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left[\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right] \times \frac{Gain}{0x400000} \times 2$$

In bipolar mode, the ideal relationship—that is, not taking into account the ADC gain error and offset error—is as follows:

$$Data = \left[\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right] \times \frac{Gain}{0x400000} + 0x800000$$

To start a calibration, write the relevant value to the MODE bits in the ADC mode register. The DOUT/$\overline{RDY}$ pin and the RDY bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is reset, the DOUT/$\overline{RDY}$ pin returns low (if $\overline{CS}$ is low), and the AD7176-2 reverts to standby mode.

During an internal offset calibration, the selected positive analog input pin is disconnected, and both modulator inputs are connected internally to the selected negative analog input pin. For this reason, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference.

System calibrations, however, expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the ADC are removed.

From an operational point of view, treat a calibration like another ADC conversion. An offset calibration, if required, must always be performed before a full-scale calibration. Set the system software to monitor the RDY bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of a calibration via a polling sequence or an interrupt-driven routine. All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed.

An internal offset calibration, system zero-scale calibration, and system full-scale calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new calibration is required for a given channel if the reference source for that channel is changed.

The offset error is typically ±40 µV and an offset calibration reduces the offset error to the order of the noise. The gain error is factory calibrated at ambient temperature. Following this calibration, the gain error is typically ±0.001%.

The AD7176-2 provides the user with access to the on-chip calibration registers, allowing the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during an internal or self-calibration.

DIGITAL INTERFACE

The programmable functions of the AD7176-2 are via the SPI serial interface. The serial interface of the AD7176-2 consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line is used to transfer data into the on-chip registers, and DOUT/$\overline{RDY}$ is used to access data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or on DOUT/$\overline{RDY}$) occur with respect to the SCLK signal.

The DOUT/$\overline{RDY}$ pin also functions as a data-ready signal, with the line going low if $\overline{CS}$ is low when a new data-word is available in the data register. The pin is reset high when a read operation from the data register is complete. The DOUT/$\overline{RDY}$ pin also goes high before updating the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. Take care to avoid reading from the data register when DOUT/$\overline{RDY}$ is about to go low. The best method to ensure that no data read occurs is to always monitor the DOUT/$\overline{RDY}$ line; start reading the data register as soon as DOUT/$\overline{RDY}$ goes low; and ensure a sufficient SCLK rate, such that the read is completed before the next conversion result. $\overline{CS}$ is used to select a device. It can be used to decode the AD7176-2 in systems where several components are connected to the serial bus.

Figure 2 and Figure 3 show timing diagrams for interfacing to the AD7176-2 using $\overline{CS}$ to decode the part. Figure 2 shows the timing for a read operation from the AD7176-2, and Figure 3 shows the timing for a write operation to the AD7176-2. It is possible to read from the data register several times even though the DOUT/$\overline{RDY}$ line returns high after the first read operation. However, care must be taken to ensure that the read operations are completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by tying $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD7176-2. The end of the conversion can also be monitored using the $\overline{RDY}$ bit in the status register.

The serial interface can be reset by writing 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1. A reset returns the interface to the state in which it expects a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, allow a period of 500 µs before addressing the serial interface.

CHECKSUM PROTECTION

The AD7176-2 has a checksum mode, which can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERROR bit is set in the status register. However, to ensure that the register write was successful, the register should be read back and checksum verified.

For CRC checksum calculations during a write operation, the following polynomial is always used:

$$x^8 + x^2 + x + 1$$

During read operations, the user can select between this polynomial and a similar XOR function. The XOR function requires less time to process on the host microcontroller than the polynomial-based checksum. The CRC_EN bits in the interface mode register enable and disable the checksum and allow the user to select between the polynomial check and the simple XOR check.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8- to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8- to 32-bit data output. Figure 67 and Figure 68 show SPI write and read transactions, respectively.

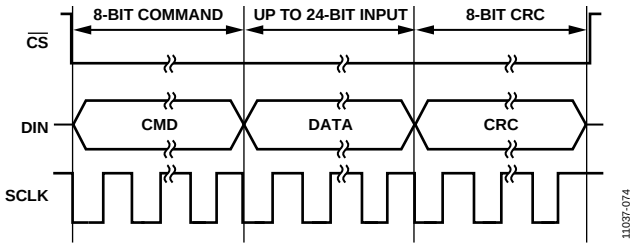


Figure 67. SPI Write Transaction with CRC

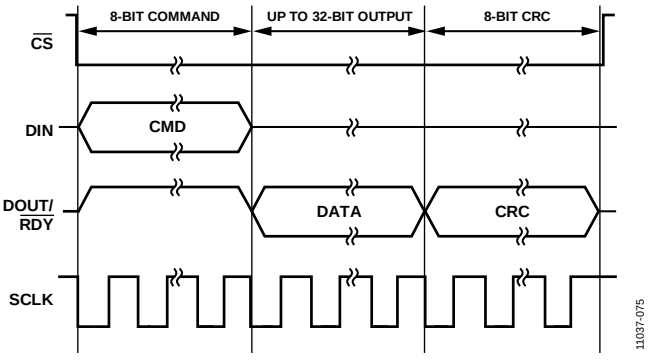


Figure 68. SPI Read Transaction with CRC

If checksum protection is enabled when continuous read mode is active, there is an implied read data command of 0x44 before every data transmission that needs to be accounted for when calculating the checksum value. This ensures a nonzero checksum value even if the ADC data equals 0x000000.

CRC CALCULATION

Polynomial

The checksum, which is 8-bits wide, is generated using the polynomial

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR (exclusive OR) function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

```
Initial value          011001010100001100100001
                       011001010100001100100001100000000      left shifted eight bits
x^8 + x^2 + x + 1  =       100000111                          polynomial
   100100100000110010000100000000          XOR result
   100000111                               polynomial
      100011000110010000100000000          XOR result
      100000111                            polynomial
         111111100100001000000000          XOR result
         100000111                         polynomial value
          11111011100001000000000          XOR result
          100000111                        polynomial value
           11110000000100000000            XOR result
           100000111                       polynomial value
            1110011100010000000            XOR result
            100000111                      polynomial value
             110010010010000000            XOR result
             100000111                     polynomial value
              10010101010000000            XOR result
              100000111                    polynomial value
                  1011011000000            XOR result
                  100000111                polynomial value
                   101010110000            XOR result
                   100000111               polynomial value
                     1010001000            XOR result
                     100000111             polynomial value
                       10000110            checksum = 0x86.
```

XOR Calculation

The checksum, which is 8-bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

Example of an XOR Calculation—24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

Using the previous example,

Divide into three bytes: 0x65, 0x43, and 0x21

01100101	0x65
01000011	0x43
00100110	XOR result
00100001	0x21
00000111	CRC

INTEGRATED FUNCTIONS

The AD7176-2 has a number of integrated functions that can be used to improve usefulness in a number of applications as well as for diagnostic purposes in safety conscious applications.

GENERAL-PURPOSE I/O

The AD7176-2 has two general-purpose digital input/output pins: GPIO0 and GPIO1. These are enabled using the IP_EN0/IP_EN1 or OP_EN0/OP_EN1 bits in the GPIOCON register. When the GPIO0 or GPIO1 pin is enabled as an input, the logic level at the pin is contained in the DATA0 or DATA1 bit, respectively. When the GPIO0 or GPIO1 pin is enabled as an output, the GP_DATA0 or GP_DATA1 bits, respectively, determine the logic level output at the pin. The logic levels for these pins are referenced to AVDD1 and AVSS; therefore, outputs have an amplitude of 5 V.

The $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin can also be used as a general-purpose output. When ERR_EN bits in the GPIOCON register are set to 11, the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin operates as a general-purpose output. In this configuration, the ERR_DAT bit in the GPIOCON register determines the logic level output at the pin. The logic level for the pin is referenced to IOVDD and DGND, and the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin has an active pull-up.

EXTERNAL MULTIPLEXER CONTROL

If an external multiplexer is used to increase the channel count, the multiplexer logic pins can be controlled via the AD7176-2 GPIO pins. With the MUX_IO bit, the GPIOs timing is controlled by the ADC; therefore, the channel change is synchronized with the ADC, eliminating any need for external synchronization.

DELAY

It is possible to insert a programmable delay before the AD7176-2 begins taking samples when using the sinc5 + sinc1 filter. This allows for an external amplifier or multiplexer to settle and can also relax the specification requirements for the external amplifier or multiplexer. There are eight programmable settings ranging from 0 µs to 1 ms which can be set using the DELAY bits in the ADC Mode Register (Address 0x01, Bits[10:8]).

If a delay greater than 0 µs is selected and $\overline{\text{HIDE\_DELAY}}$ in the Interface Mode Register (Address 0x02, Bit 10) is set to 1 then this delay is added to the conversion time for each sample regardless of selected output data rate.

If $\overline{\text{HIDE\_DELAY}}$ is set to 0 and the selected delay is less than half of the conversion time then the delay can be absorbed by reducing the number of averages performed which keeps the conversion time the same but can affect the noise performance depending on how long the delay is compared to the conversion time. It is only possible to absorb the delay for output data rates less than 10 kSPS with the exception of the following four rates which cannot absorb any delay: 397.5 SPS, 59.94 SPS, 49.96 SPS, and 16.66 SPS.

16-BIT/24-BIT CONVERSIONS

By default, the AD7176-2 generates 24-bit conversions. However, the width of the conversions can be reduced to 16 bits. Setting Bit WL16 in the interface mode register to 1 rounds all data conversions to 16 bits. Clearing this bit sets the width of the data conversions to 24 bits.

SERIAL INTERFACE RESET (DOUT_RESET)

The serial interface is reset when each read operation is complete. The instant at which the serial interface is reset is programmable. By default, the serial interface is reset after a period of time following the last SCLK rising edge, the SCLK edge on which the LSB is read by the processor. By setting Bit DOUT_RESET in the interface mode register to 1, the instant at which the interface is reset is controlled by the $\overline{\text{CS}}$ rising edge. In this case, the DOUT/$\overline{\text{RDY}}$ pin continues to output the LSB of the register being read until $\overline{\text{CS}}$ is taken high. Only on the $\overline{\text{CS}}$ rising edge is the interface reset. This configuration is useful if the $\overline{\text{CS}}$ signal is used to frame all read operations. If $\overline{\text{CS}}$ is not used to frame all read operations, DOUT_RESET should be set to 0 so that the interface is reset following the last SCLK edge in the read operation.

SYNCHRONIZATION ($\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$)

Normal Synchronization

When the SYNC_EN bit in the GPIOCON register is set to 1, the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin functions as a synchronization pin. The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the part. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{\text{SYNC}}$. This pin must be low for at least one master clock cycle to ensure that synchronization occurs.

If multiple AD7176-2 devices are operated from a common master clock, they can be synchronized so that their data registers are updated simultaneously. This is normally done after each AD7176-2 has performed its own calibration or has calibration coefficients loaded into its calibration registers. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD7176-2 into a consistent known state. While the $\overline{\text{SYNC}}$ pin is low, the AD7176-2 is maintained in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter are taken out of this reset state, and on the next master clock edge, the part starts to gather input samples again.

The part is taken out of reset on the master clock falling edge following the $\overline{\text{SYNC}}$ low-to-high transition. Therefore, when multiple devices are being synchronized, the $\overline{\text{SYNC}}$ pin should be taken high on the master clock rising edge to ensure that all devices begin sampling on the master clock falling edge. If the $\overline{\text{SYNC}}$ pin is not taken high in sufficient time, it is possible to have a difference of one master clock cycle between the devices;

that is, the instant at which conversions are available differs from part to part by a maximum of one master clock cycle.

The $\overline{\text{SYNC}}$ pin can also be used as a start conversion command. In this mode, the rising edge of $\overline{\text{SYNC}}$ starts a conversion, and the falling edge of $\overline{\text{RDY}}$ indicates when the conversion is complete. The settling time of the filter has to be allowed for each data register update.

Alternate Synchronization

Setting Bit ALT_SYNC in the interface mode register to 1 enables an alternate synchronization scheme. The SYNC_EN bit in the GPIOCON register must be set to 1 to enable this alternate scheme. In this mode, the $\overline{\text{SYNC}}$ pin operates as a start conversion command when several channels of the AD7176-2 are enabled. When $\overline{\text{SYNC}}$ is taken low, the ADC completes the conversion on the current channel, selects the next channel in the sequence, and then waits until $\overline{\text{SYNC}}$ is taken high to commence the conversion. The $\overline{\text{RDY}}$ pin goes low when the conversion is complete on the current channel, and the data register is updated with the corresponding conversion. Therefore, the $\overline{\text{SYNC}}$ command does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence.

This mode can be used only when several channels are enabled. It is not recommended to use this mode when a single channel is enabled.

ERROR FLAGS

The status register contains three error bits—ADC_ERROR, CRC_ERROR, and REG_ERROR—that flag errors with the ADC conversion, errors with the CRC check, and errors due to changes in the registers, respectively. In addition, the $\overline{\text{ERROR}}$ pin can indicate that an error has occurred.

ADC_ERROR

The ADC_ERROR bit in the status register flags any errors that occur during the conversion process. The flag is set when an overvoltage or undervoltage occurs on the analog inputs. The ADC also outputs all 0s or all 1s when an undervoltage or overvoltage occurs. This flag is reset only when the overvoltage/undervoltage is removed. It is not reset by a read of the data register.

CRC_ERROR

If the CRC value that accompanies a write operation does not correspond with the information sent, the CRC_ERROR flag is set. The flag is reset as soon as the status register is explicitly read.

REG_ERROR

This flag is used in conjunction with the REG_CHECK bit in the interface mode register. When the REG_CHECK bit is set, the AD7176-2 monitors the values in the on-chip registers. If a bit changes, the REG_ERROR bit is set. Therefore, for writes to the on-chip registers, REG_CHECK should be set to 0. When the registers have been updated, the REF_CHK bit can be set to 1. The AD7176-2 calculates a checksum of the on-chip registers. If one of the register values has changed, the REG_ERROR bit is set. If an error is flagged, the REG_CHECK bit must be set to 0 to clear the REG_ERROR bit in the status register. The register check function does not monitor the data register, status register, or interface mode register.

$\overline{\text{ERROR}}$ Pin

When the SYNC_EN bit in the GPIOCON register is set to 1 and Bit ALT_SYNC in the interface mode register is set to 0, the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin functions as an error input/output pin or a general-purpose output pin. The ERR_EN bits in the GPIOCON register determine the function of the pin.

With ERR_EN bits are set to 10, the pin functions as an open-drain error output pin. The three error bits in the status register (ADC_ERROR, CRC_ERROR, and REG_ERROR) are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ pin. Therefore, the $\overline{\text{ERROR}}$ pin indicates that an error has occurred. The status register must be read to identify the error source.

When ERR_EN bits are set to 01, the $\overline{\text{ERROR}}$ pin functions as an error input pin. The error pin of another component can be connected to the AD7176-2 $\overline{\text{ERROR}}$ pin so that the AD7176-2 indicates when an error occurs on either itself or the external component. The value on the $\overline{\text{ERROR}}$ pin is inverted and OR'ed with the errors from the ADC conversion, and the result is indicated via the ADC_ERROR bit in the status register. The value of the $\overline{\text{ERROR}}$ pin is reflected in the ERR_DAT bit in the status register.

The $\overline{\text{ERROR}}$ pin is disabled when the ERR_EN bits are set to 00. When the ERR_EN1 bits are set to 11, the $\overline{\text{ERROR}}$ pin operates as a general-purpose output.

DATA_STAT

The contents of the status register can be appended to each conversion on the AD7176-2. This is a useful function if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The two LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged by the error bits.

IOSTRENTGH

The serial interface can operate with a power supply as low as 2 V. However, at this low voltage, the DOUT/$\overline{\text{RDY}}$ pin may not have sufficient drive strength if there is moderate parasitic capacitance on the board or the SCLK frequency is high. The IOSTRENGTH bit in the interface mode register increases the drive strength of the DOUT/$\overline{\text{RDY}}$ pin.

GROUNDING AND LAYOUT

The analog inputs and reference inputs are differential and, therefore, most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the part removes common-mode noise on these inputs. The analog and digital supplies to the AD7176-2 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the master clock frequency.

The digital filter also removes noise from the analog and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD7176-2 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD7176-2 is high and the noise levels from the converter are so low, care must be taken with regard to grounding and layout.

The printed circuit board (PCB) that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is generally best for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, ensuring that the paths for all return currents are as close as possible to the paths the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD7176-2 to prevent noise coupling. The power supply lines to the AD7176-2 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough on the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Good decoupling is important when using high resolution ADCs. The AD7176-2 has three power supply pins—AVDD1, AVDD2, and IOVDD. The AVDD1 and AVDD2 pins are referenced to AVSS, and the IOVDD pin is referenced to DGND. AVDD1 and AVDD2 should be decoupled with a 10 µF tantalum capacitor in parallel with a 0.1 µF capacitor to AVSS on each pin. The 0.1 µF capacitor should be placed as close as possible to the device on each supply, ideally right up against the device. IOVDD should be decoupled with a 10 µF tantalum capacitor in parallel with a 0.1 µF capacitor to DGND. All analog inputs should be decoupled to AVSS. If an external reference is used, the REF+ and REF− pins should be decoupled to AVSS.

The AD7176-2 also has two on-board LDO regulators—one that regulates the AVDD2 supply and one that regulates the IOVDD supply. For the REGCAPA pin, it is recommended that 1 µF and 0.1 µF capacitors to AVSS be used. Similarly, for the REGCAPD pin, it is recommended that 1 µF and 0.1 µF capacitors to DGND be used.

If using the AD7176-2 for split supply operation, a separate plane must be used for AVSS.

REGISTER SUMMARY

Table 22. AD7176-2 Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W
0x00	STATUS	[7:0]	$\overline{RDY}$	ADC_ERROR	CRC_ERROR	REG_ERROR	RESERVED		CHANNEL		0x80	R
0x01	ADCMODE	[15:8]	REF_EN	RESERVED	SING_CYC	RESERVED		DELAY			0x8000	RW
		[7:0]	RESERVED	MODE			CLOCKSEL		RESERVED			
0x02	IFMODE	[15:8]	RESERVED			ALT_SYNC	IOSTRENGTH	$\overline{HIDE\_DELAY}$		DOUT_RESET	0x0000	RW
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	RESERVED	CRC_EN		RESERVED	WL16		
0x03	REGCHECK	[23:16]	REGISTER_CHECK[23:16]								0x000000	R
		[15:8]	REGISTER_CHECK[15:8]									
		[7:0]	REGISTER_CHECK[7:0]									
0x04	DATA	[23:16]	DATA[23:16]								0x000000	R
		[15:8]	DATA[15:8]									
		[7:0]	DATA[7:0]									
0x06	GPIOCON	[15:8]	RESERVED			MUX_IO	SYNC_EN	ERR_EN		ERR_DAT	0x0800	RW
		[7:0]	RESERVED		IP_EN1	IP_EN0	OP_EN1	OP_EN0	GP_DATA1	GP_DATA0		
0x07	ID	[15:8]	ID[15:8]								0x0C9X	R
		[7:0]	ID[7:0]									
0x10	CHMAP0	[15:8]	CH_EN0	RESERVED	SETUP_SEL0		RESERVED		AINPOS0[4:3]		0x8001	RW
		[7:0]	AINPOS0[2:0]			AINNEG0						
0x11	CHMAP1	[15:8]	CH_EN1	RESERVED	SETUP_SEL1		RESERVED		AINPOS1[4:3]		0x0001	RW
		[7:0]	AINPOS1[2:0]			AINNEG1						
0x12	CHMAP2	[15:8]	CH_EN2	RESERVED	SETUP_SEL2		RESERVED		AINPOS2[4:3]		0x0001	RW
		[7:0]	AINPOS2[2:0]			AINNEG2						
0x13	CHMAP3	[15:8]	CH_EN3	RESERVED	SETUP_SEL3		RESERVED		AINPOS3[4:3]		0x0001	RW
		[7:0]	AINPOS3[2:0]			AINNEG3						
0x20	SETUPCON0	[15:8]	RESERVED			BI_UNIPOLAR0	RESERVED				0x1020	RW
		[7:0]	RESERVED		REF_SEL0		RESERVED					
0x21	SETUPCON1	[15:8]	RESERVED			BI_UNIPOLAR1	RESERVED				0x1020	RW
		[7:0]	RESERVED		REF_SEL1		RESERVED					
0x22	SETUPCON2	[15:8]	RESERVED			BI_UNIPOLAR2	RESERVED				0x1020	RW
		[7:0]	RESERVED		REF_SEL2		RESERVED					
0x23	SETUPCON3	[15:8]	RESERVED			BI_UNIPOLAR3	RESERVED				0x1020	RW
		[7:0]	RESERVED		REF_SEL3		RESERVED					
0x28	FILTCON0	[15:8]	SINC3_MAP0	RESERVED			ENHFILTEN0	ENHFILT0			0x0000	RW
		[7:0]	RESERVED	ORDER0		ODR0						
0x29	FILTCON1	[15:8]	SINC3_MAP1	RESERVED			ENHFILTEN1	ENHFILT1			0x0000	RW
		[7:0]	RESERVED	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	RESERVED			ENHFILTEN2	ENHFILT2			0x0000	RW
		[7:0]	RESERVED	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	RESERVED			ENHFILTEN3	ENHFILT3			0x0000	RW
		[7:0]	RESERVED	ORDER3		ODR3						
0x30	OFFSET0	[23:16]	OFFSET0[23:16]								0x800000	RW
		[15:8]	OFFSET0[15:8]									
		[7:0]	OFFSET0[7:0]									
0x31	OFFSET1	[23:16]	OFFSET1[23:16]								0x800000	RW
		[15:8]	OFFSET1[15:8]									
		[7:0]	OFFSET1[7:0]									
0x32	OFFSET2	[23:16]	OFFSET2[23:16]								0x800000	RW
		[15:8]	OFFSET2[15:8]									
		[7:0]	OFFSET2[7:0]									
0x33	OFFSET3	[23:16]	OFFSET3[23:16]								0x800000	RW
		[15:8]	OFFSET3[15:8]									
		[7:0]	OFFSET3[7:0]									

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x38	GAIN0	[23:16]	GAIN0[23:16]								0x5XXXX0	RW
		[15:8]	GAIN0[15:8]									
		[7:0]	GAIN0[7:0]									
0x39	GAIN1	[23:16]	GAIN1[23:16]								0x5XXXX0	RW
		[15:8]	GAIN1[15:8]									
		[7:0]	GAIN1[7:0]									
0x3A	GAIN2	[23:16]	GAIN2[23:16]								0x5XXXX0	RW
		[15:8]	GAIN2[15:8]									
		[7:0]	GAIN2[7:0]									
0x3B	GAIN3	[23:16]	GAIN3[23:16]								0x5XXXX0	RW
		[15:8]	GAIN3[15:8]									
		[7:0]	GAIN3[7:0]									

REGISTER DETAILS

COMMUNICATIONS REGISTER

Address: 0x00, Reset: 0x00, Name: COMMS

Table 23. Bit Descriptions for COMMS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{WEN}$		This bit must be low to begin communications with the ADC.	0x0	W
6	R/$\overline{W}$		This bit determines if the command is a read or write operation.	0x0	W
		0	Write command		
		1	Read command		
[5:0]	RA		The register address bits determine which register is to be read from or written to as part of the current communication.	0x00	W
		000000	Status Register		
		000001	ADC Mode Register		
		000010	Interface Mode Register		
		000011	Register Checksum Register		
		000100	Data Register		
		000110	GPIO Configuration Register		
		000111	ID Register		
		010000	Channel 0 Register		
		010001	Channel 1 Register		
		010010	Channel 2 Register		
		010011	Channel 3 Register		
		100000	Setup Configuration 0 Register		
		100001	Setup Configuration 1 Register		
		100010	Setup Configuration 2 Register		
		100011	Setup Configuration 3 Register		
		101000	Filter Configuration 0 Register		
		101001	Filter Configuration 1 Register		
		101010	Filter Configuration 2 Register		
		101011	Filter Configuration 3 Register		
		110000	Offset 0 Register		
		110001	Offset 1 Register		
		110010	Offset 2 Register		
		110011	Offset 3 Register		
		111000	Gain 0 Register		
		111001	Gain 1 Register		
		111010	Gain 2 Register		
		111011	Gain 3 Register		

STATUS REGISTER

Address: 0x00, Reset: 0x80, Name: STATUS

The Status Register is an 8-bit register that contains ADC and serial interface status information. It can optionally be appended to the Data Register by setting the DATA_STAT bit in the Interface Mode Register.

Table 24. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{\text{RDY}}$		The status of $\overline{\text{RDY}}$ is output to the DOUT/$\overline{\text{RDY}}$ pin whenever $\overline{\text{CS}}$ is low and a register is not being read. This bit goes low when the ADC has written a new result to the Data Register. In ADC calibration modes, this bit goes low when the ADC has written the calibration result. $\overline{\text{RDY}}$ is brought high automatically by a read of the Data Register.	0x1	R
		0	New data result available		
		1	Awaiting new data result		
6	ADC_ERROR		This bit by default indicates if an ADC overrange or underrange has occurred. The ADC result will be clamped to ±full scale if this happens. This bit is updated when the ADC result is written and is cleared by removing the overrange or underrange condition on the analog inputs.	0x0	R
		0	No Error		
		1	Error		
5	CRC_ERROR		This bit indicates if a CRC error has taken place during a register write. For register reads, the host microcontroller determines if a CRC error has occurred. This bit is cleared by a read of this register.	0x0	R
		0	No Error		
		1	CRC Error		
4	REG_ERROR		This bit indicates if the content of one of the internal registers has changed from the value calculated when the register integrity check was activated. The check is activated by setting the REG_CHECK bit in the Interface Mode Register. This bit is cleared by clearing the REG_CHECK bit.	0x0	R
		0	No Error		
		1	Error		
[3:2]	RESERVED		These bits are reserved.	0x0	R
[1:0]	CHANNEL		These bits indicate which channel was active for the ADC conversion whose result is currently in the Data Register. This may be different from the channel currently being converted. The mapping is a direct map from the Channel Map Register; therefore, Channel 0 results in 0x0 and Channel 3 results in 0x3.	0x0	R
		00	Channel 0		
		01	Channel 1		
		10	Channel 2		
		11	Channel 3		

ADC MODE REGISTER

Address: 0x01, Reset: 0x8000, Name: ADCMODE

The ADC Mode Register controls the operating mode of the ADC and the master clock selection. A write to the ADC Mode Register resets the filter and the $\overline{RDY}$ bits and starts a new conversion or calibration.

Table 25. Bit Descriptions for ADCMODE

Bits	Bit Name	Settings	Description	Reset	Access
15	REF_EN		Enables internal reference and outputs a buffered 2.5 V to the REFOUT pin.	0x1	RW
		0	Disabled		
		1	Enabled		
14	RESERVED		This bit is reserved and should be set to 0.	0x0	R
13	SING_CYC		This bit can be used when only a single channel is active to set the ADC to only output at the settled filter data rate.	0x0	RW
		0	Disabled		
		1	Enabled		
[12:11]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
[10:8]	DELAY		These bits allow a programmable delay to be added after a channel switch to allow for settling of external circuitry before the ADC starts processing its input.	0x0	RW
		000	0		
		001	4 µs		
		010	16 µs		
		011	40 µs		
		100	100 µs		
		101	200 µs		
		110	500 µs		
		111	1 ms		
7	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[6:4]	MODE		These bits control the operating mode of the ADC. Details can be found in the Operating Modes section.	0x0	RW
		000	Continuous Conversion Mode		
		001	Single Conversion Mode		
		010	Standby Mode		
		011	Power-Down Mode		
		100	Internal Offset Calibration		
		110	System Offset Calibration		
		111	System Gain Calibration		
[3:2]	CLOCKSEL		This bit is used to select the ADC clock source. Selecting internal oscillator also enables the internal oscillator.	0x0	RW
		00	Internal oscillator		
		01	Internal oscillator output on XTAL2 pin		
		10	External clock input on XTAL2 pin		
		11	External crystal on XTAL1 and XTAL2 pins		
[1:0]	RESERVED		These bits are reserved and should be set to 0.	0x0	R

INTERFACE MODE REGISTER

Address: 0x02, Reset: 0x0000, Name: IFMODE

The Interface Mode Register configures various serial interface options.

Table 26. Bit Descriptions for IFMODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
12	ALT_SYNC		This bit enables a different behavior of the $\overline{\text{ERROR}}$\$\overline{\text{SYNC}}$ pin to allow the use of $\overline{\text{ERROR}}$\$\overline{\text{SYNC}}$ as a control for conversions when cycling channels (see the description of the SYNC_EN bit in the GPIO Configuration Register for details).	0x0	RW
		0	Disabled		
		1	Enabled		
11	IOSTRENGTH		This bit controls the drive strength of the DOUT pin. This bit should be set when reading from the serial interface at high speed with low IOVDD supply and moderate capacitance.	0x0	RW
		0	Disabled (default)		
		1	Enabled		
10	$\overline{\text{HIDE\_DELAY}}$		If a programmable delay has been set using the DELAY bits in the ADC Mode Register then this bit allows for the delay to be hidden by absorbing the delay into the conversion time for selected data rates. See the Delay section for more details.	0x0	RW
		0	Enabled		
		1	Disabled		
9	RESERVED		These bits are reserved and should be set to 0.	0x0	R
8	DOUT_RESET		This bit prevents the DOUT/$\overline{\text{RDY}}$ pin from switching from outputting DOUT to outputting $\overline{\text{RDY}}$ soon after the last rising edge of SCLK during a read operation. Instead, the DOUT/$\overline{\text{RDY}}$ pin will continue to output the LSB of the data until $\overline{\text{CS}}$ goes high. This allows for longer hold times for the SPI master to sample the LSB of the data. When this bit is set, $\overline{\text{CS}}$ must not be tied low.	0x0	RW
		0	Disabled		
		1	Enabled		
7	CONTREAD		This enables continuous read of the ADC data register. The ADC should be configured in continuous conversion mode to use continuous read. For more details, see the Operating Modes section.	0x0	RW
		0	Disabled		
		1	Enabled		
6	DATA_STAT		This enables the Status Register to be appended to the Data Register when read so that channel and status information are transmitted with the data. This is the only way to be sure that the channel bits read from the Status Register correspond to the data in the Data Register.	0x0	RW
		0	Disabled		
		1	Enabled		
5	REG_CHECK		This bit enables a register integrity checker, which can be used to monitor any change in the value of the user registers. To use this feature, all other registers should be configured as desired, with this bit cleared. Then write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the Status Register. To clear the error, the REG_CHECK bit should be set to 0. Neither the Interface Mode Register nor the ADC Data or Status Register is included in the registers that are checked. If a register needs to have a new value written, this bit should first be cleared; otherwise, an error will be flagged falsely when the new register contents are written.	0x0	RW
		0	Disabled		
		1	Enabled		
4	RESERVED		This bit is reserved and should be set to 0.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[3:2]	CRC_EN		Enables CRC protection of register reads/writes. CRC increases the number of bytes in a serial interface transfer by one. See the CRC Calculation section for more details.	0x00	RW
		00	Disabled.		
		01	XOR checksum enabled for register read transactions. Register writes will still use CRC with these bits set.		
		10	CRC checksum enabled for read and write transactions.		
1	RESERVED		This bit is reserved and should be set to 0.	0x0	R
0	WL16		Changes the ADC Data Register to 16 bits. The ADC is not reset by a write to the Interface Mode Register; therefore, the ADC result will not be rounded to the correct word length immediately after writing to these bits. The first new ADC result will be correct.	0x0	RW
		0	24-bit data		
		1	16-bit data		

REGISTER CHECK

Address: 0x03, Reset: 0x000000, Name: REGCHECK

This Register Check Register is a 24-bit checksum calculated by exclusively OR'ing the contents of the user registers. The REG_CHECK bit in the Interface Mode Register must be set for this to operate; otherwise, the register reads 0.

Table 27. Bit Descriptions for REGCHECK

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	REGISTER_CHECK		This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the Interface Mode Register.	0x000000	R

DATA REGISTER

Address: 0x04, Reset: 0x000000, Name: DATA

The Data Register contains the ADC conversion result. The encoding is offset binary, or it can be changed to unipolar by the BI_UNIPOLAR bit in the Setup Configuration Register. Reading the Data Register brings the $\overline{\text{RDY}}$ bit and pin high if they had been low. The ADC result can be read multiple times; however, because $\overline{\text{RDY}}$ has been brought high, it is not possible to know if another ADC result is imminent. The ADC will not write a new result into the data register if the register is currently being read.

Table 28. Bit Descriptions for DATA

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	DATA		This register contains the ADC conversion result. If DATA_STAT is set in the Interface Mode Register, then the Status Register is appended to this register when read, making this a 32-bit register. If WL16 is set in the Interface Mode Register, then this register is rounded to 16 bits.	0x000000	R

GPIO CONFIGURATION REGISTER

Address: 0x06, Reset: 0x0800, Name: GPIOCON

The GPIO Configuration Register controls the general-purpose I/O pins of the ADC.

Table 29. Bit Descriptions for GPIOCON

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
12	MUX_IO		This bit allows the ADC to control an external multiplexer, using GPIO0/GPIO1 in sync with the internal channel sequencing. The analog input pins used for a channel can still be selected on a per channel basis. Therefore, it is possible to have a 4-channel multiplexer in front of AIN0/AIN1 and another in front of AIN2/AIN3, giving a total of eight differential channels with the AD7175-2. However, only four channels at a time can be automatically sequenced. A delay can be inserted after switching an external multiplexer (see the DELAY bits in the ADC Mode Register section).	0x0	RW
11	SYNC_EN		This bit enables the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin as a sync input. When the pin is low, this holds the ADC and filter in reset until $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin goes high. An alternative operation of the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin is available when the ALT_SYNC bit in the Interface Mode Register is set. This mode only works when multiple channels are enabled. In this case, a low on the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin does not immediately reset the filter/modulator. Instead, if the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ high begins the next conversion. This alternative sync mode allows $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ to be used while cycling through channels.	0x1	RW
		0	Disabled		
		1	Enabled		
[10:9]	ERR_EN		These bits enable the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin as an error input/output.	0x0	RW
		00	Disabled		
		01	$\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ is an error input. The (inverted) readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the Status Register. The $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin state can also be read from the ERR_DAT bit in this register.		
		10	$\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ is an open-drain error output. The Status Register error bits are OR'ed, inverted, and mapped to the $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pin. $\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.		
		11	$\overline{\text{SYNC}}$/$\overline{\text{ERROR}}$ is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This is referenced between IOVDD and DGND, as opposed to the AVDD1 and AVSS levels used by the general-purpose I/O pins. It has an active pull-up in this case.		
8	ERR_DAT		This bit determines the logic level at the $\overline{\text{ERROR}}$ pin if the pin is enabled as a general-purpose output. It reflects the readback status of the pin if the pin is enabled as an input.	0x0	RW
[7:6]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
5	IP_EN1		This bit turns GPIO1 into an input. Input should equal AVDD5 or AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		
4	IP_EN0		This bit turns GPIO0 into an input. Input should equal AVDD5 or AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		
3	OP_EN1		This bit turns GPIO1 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		

Bits	Bit Name	Settings	Description	Reset	Access
2	OP_EN0		This bit turns GPIO0 into an output. Outputs are referenced between AVDD1 and AVSS.	0x0	RW
		0	Disabled		
		1	Enabled		
1	GP_DATA1		This bit is the readback or write data for GPIO1.	0x0	RW
0	GP_DATA0		This bit is the readback or write data for GPIO0.	0x0	RW

ID REGISTER

Address: 0x07, Reset: 0x0C9X, Name: ID

The ID register returns a 16-bit ID. For the AD7176-2, this should be 0x0C94.

Table 30. Bit Descriptions for ID

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ID		The ID register returns a 16-bit ID code that is specific to the ADC.	0x0C9X	R
		0x0C9X	AD7176-2		

CHANNEL MAP REGISTER 0

Address: 0x10, Reset: 0x8001, Name: CHMAP0

The Channel Map Registers are 16-bit registers that are used to select which channels are currently active, which inputs are selected for each channel, and which setup should be used to configure the ADC for that channel.

Table 31. Bit Descriptions for CHMAP0

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_EN0		This bit enables Channel 0. If more than one channel is enabled, the ADC will automatically sequence between them.	0x1	RW
		0	Disabled		
		1	Enabled (default)		
14	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[13:12]	SETUP_SEL0		These bits identify which of the four setups are used to configure the ADC for this channel. A setup comprises a set of four registers: Setup Configuration Register, Filter Configuration Register, Offset Register, Gain Register. All channels can use the same setup, in which case the same 3-bit value should be written to these bits on all active channels, or up to four channels can be configured differently.	0x0	RW
		00	Setup 0		
		01	Setup 1		
		10	Setup 2		
		11	Setup 3		
[11:10]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
[9:5]	AINPOS0		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel.	0x0	RW
		00000	AIN0 (default)		
		00001	AIN1		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		
[4:0]	AINNEG0		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
		00000	AIN0		
		00001	AIN1 (default)		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		

CHANNEL MAP REGISTER 1

Address: 0x11, Reset: 0x0001, Name: CHMAP1

The Channel Map Registers are 16-bit registers that are used to select which channels are currently active, which inputs are selected for each channel, and which setup should be used to configure the ADC for that channel.

Table 32. Bit Descriptions for CHMAP1

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_EN1		This bit enables Channel 1. If more than one channel is enabled, the ADC will automatically sequence between them.	0x0	RW
		0	Disabled (default)		
		1	Enabled		
14	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[13:12]	SETUP_SEL1		These bits identify which of the four setups are used to configure the ADC for this channel. A setup comprises a set of four registers: Setup Configuration Register, Filter Configuration Register, Offset Register, Gain Register. All channels can use the same setup, in which case the same 3-bit value should be written to these bits on all active channels, or up to four channels can be configured differently.	0x0	RW
		00	Setup 0		
		01	Setup 1		
		10	Setup 2		
		11	Setup 3		
[11:10]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
[9:5]	AINPOS1		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel.	0x0	RW
		00000	AIN0 (default)		
		00001	AIN1		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		
[4:0]	AINNEG1		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
		00000	AIN0		
		00001	AIN1 (default)		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		

CHANNEL MAP REGISTER 2

Address: 0x12, Reset: 0x0001, Name: CHMAP2

The Channel Map Registers are 16-bit registers that are used to select which channels are currently active, which inputs are selected for each channel, and which setup should be used to configure the ADC for that channel.

Table 33. Bit Descriptions for CHMAP2

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_EN2		This bit enables Channel 2. If more than one channel is enabled, the ADC will automatically sequence between them.	0x0	RW
		0	Disabled (default)		
		1	Enabled		
14	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[13:12]	SETUP_SEL2		These bits identify which of the four setups are used to configure the ADC for this channel. A setup comprises a set of four registers: Setup Configuration Register, Filter Configuration Register, Offset Register, Gain Register. All channels can use the same setup, in which case the same 3-bit value should be written to these bits on all active channels, or up to four channels can be configured differently.	0x0	RW
		00	Setup 0		
		01	Setup 1		
		10	Setup 2		
		11	Setup 3		
[11:10]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
[9:5]	AINPOS2		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel.	0x0	RW
		00000	AIN0 (default)		
		00001	AIN1		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		
[4:0]	AINNEG2		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
		00000	AIN0		
		00001	AIN1 (default)		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		

CHANNEL MAP REGISTER 3

Address: 0x13, Reset: 0x0001, Name: CHMAP3

The Channel Map Registers are 16-bit registers that are used to select which channels are currently active, which inputs are selected for each channel, and which setup should be used to configure the ADC for that channel.

Table 34. Bit Descriptions for CHMAP3

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_EN3		This bit enables Channel 3. If more than one channel is enabled, the ADC will automatically sequence between them.	0x0	RW
		0	Disabled (default)		
		1	Enabled		
14	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[13:12]	SETUP_SEL3		These bits identify which of the four setups are used to configure the ADC for this channel. A setup comprises a set of four registers: Setup Configuration Register, Filter Configuration Register, Offset Register, Gain Register. All channels can use the same setup, in which case the same 3-bit value should be written to these bits on all active channels, or up to four channels can be configured differently.	0x0	RW
		00	Setup 0		
		01	Setup 1		
		10	Setup 2		
		11	Setup 3		
[11:10]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
[9:5]	AINPOS3		These bits select which of the analog inputs is connected to the positive input of the ADC for this channel.	0x0	RW
		00000	AIN0 (default)		
		00001	AIN1		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		
[4:0]	AINNEG3		These bits select which of the analog inputs is connected to the negative input of the ADC for this channel.	0x1	RW
		00000	AIN0		
		00001	AIN1 (default)		
		00010	AIN2		
		00011	AIN3		
		00100	AIN4		
		10101	REF+		
		10110	REF−		

SETUP CONFIGURATION REGISTER 0

Address: 0x20, Reset: 0x1020, Name: SETUPCON0

The Setup Configuration Registers are 16-bit registers that configure the reference selection and output coding of the ADC.

Table 35. Bit Descriptions for SETUPCON0

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
12	BI_UNIPOLAR0		This bit sets the output coding of the ADC for Setup 0.	0x1	RW
		0	Unipolar coded output		
		1	Offset binary coded output		
[11:6]	RESERVED		These bits are reserved and should be set to 0.	0x00	R
[5:4]	REF_SEL0		These bits allow you to select the reference source for ADC conversion on Setup 0.	0x2	RW
		00	External Reference.		
		10	Internal 2.5 V Reference. This must also be enabled in the ADC Mode Register.		
		11	AVDD1 − AVSS. This can be used to as a diagnostic to validate other reference values.		
[3:0]	RESERVED		These bits are reserved and should be set to 0.	0x0	R

SETUP CONFIGURATION REGISTER 1

Address: 0x21, Reset: 0x1020, Name: SETUPCON1

The Setup Configuration Registers are 16-bit registers that configure the reference selection and output coding of the ADC.

Table 36. Bit Descriptions for SETUPCON1

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
12	BI_UNIPOLAR1		This bit sets the output coding of the ADC for Setup 1.	0x1	RW
		0	Unipolar coded output		
		1	Offset binary coded output		
[11:6]	RESERVED		These bits are reserved and should be set to 0.	0x00	R
[5:4]	REF_SEL1		These bits allow you to select the reference source for ADC conversion on Setup 1.	0x2	RW
		00	External Reference		
		10	Internal 2.5 V Reference. This must also be enabled in the ADC Mode Register.		
		11	AVDD1 − AVSS. This can be used to as a diagnostic to validate other reference values.		
[3:0]	RESERVED		These bits are reserved and should be set to 0.	0x0	R

SETUP CONFIGURATION REGISTER 2

Address: 0x22, Reset: 0x1020, Name: SETUPCON2

The Setup Configuration Registers are 16-bit registers that configure the reference selection and output coding of the ADC.

Table 37. Bit Descriptions for SETUPCON2

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
12	BI_UNIPOLAR2		This bit sets the output coding of the ADC for Setup 2.	0x1	RW
		0	Unipolar coded output		
		1	Offset binary coded output		
[11:6]	RESERVED		These bits are reserved and should be set to 0.	0x00	R
[5:4]	REF_SEL2		These bits allow you to select the reference source for ADC conversion on Setup 2.	0x2	RW
		00	External Reference		
		10	Internal 2.5 V Reference. This must also be enabled in the ADC Mode Register.		
		11	AVDD1 − AVSS. This can be used to as a diagnostic to validate other reference values.		
[3:0]	RESERVED		These bits are reserved and should be set to 0.	0x0	R

SETUP CONFIGURATION REGISTER 3

Address: 0x23, Reset: 0x1020, Name: SETUPCON3

The Setup Configuration Registers are 16-bit registers that configure the reference selection and output coding of the ADC.

Table 38. Bit Descriptions for SETUPCON3

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
12	BI_UNIPOLAR3		This bit sets the output coding of the ADC for Setup 3.	0x1	RW
		0	Unipolar coded output		
		1	Offset binary coded output		
[11:6]	RESERVED		These bits are reserved and should be set to 0.	0x00	R
[5:4]	REF_SEL3		These bits allow you to select the reference source for ADC conversion on Setup 3.	0x2	RW
		00	External Reference		
		10	Internal 2.5 V Reference. This must also be enabled in the ADC Mode Register.		
		11	AVDD1 − AVSS. This can be used to as a diagnostic to validate other reference values.		
[3:0]	RESERVED		These bits are reserved and should be set to 0.	0x0	R

FILTER CONFIGURATION REGISTER 0

Address: 0x28, Reset: 0x0000, Name: FILTCON0

The Filter Configuration Registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 39. Bit Descriptions for FILTCON0

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAP0		If this bit is set, the mapping of the Filter Register changes to directly program the decimation rate of the sinc3 filter for Setup 0. All other options are eliminated. This allows for fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals FMOD/(32 × FILTCON0[14:0]).	0x0	RW
[14:12]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
11	ENHFILTEN0		This bit enables various post filters for enhanced 50 Hz/60 Hz rejection for Setup 0. The ORDER bits must be set to 00 to select the sinc5 + sinc1 filter for this to work.	0x0	RW
		0	Disabled		
		1	Enabled		
[10:8]	ENHFILT0		These bits select between various post filters for enhanced 50 Hz/60 Hz rejection for Setup 0.	0x0	RW
		010	27 SPS, 47 dB rejection, 36.7 ms settling		
		011	25 SPS, 62 dB rejection, 40 ms settling		
		101	20 SPS, 86 dB rejection, 50 ms settling		
		110	16.67 SPS, 92 dB rejection, 60 ms settling		
7	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[6:5]	ORDER0		These bits control the order of the digital filter that processes the modulator data for Setup 0.	0x0	RW
		00	Sinc5 + sinc1 (default)		
		11	Sinc3. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels.		
[4:0]	ODR0		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 0.	0x0	RW
		00000	250,000		
		00001	125,000		
		00010	62,500		
		00011	50,000		
		00100	31,250		
		00101	25,000		
		00110	15,625		
		00111	10,000		
		01000	5000		
		01001	2500		
		01010	1000		
		01011	500		
		01100	397.5		
		01101	200		
		01110	100		
		01111	59.94		
		10000	49.96		
		10001	20		
		10010	16.667		
		10011	10		
		10100	5		

FILTER CONFIGURATION REGISTER 1

Address: 0x29, Reset: 0x0000, Name: FILTCON1

The Filter Configuration Registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 40. Bit Descriptions for FILTCON1

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAP1		If this bit is set, the mapping of the Filter Register changes to directly program the decimation rate of the sinc3 filter for Setup 1. All other options are eliminated. This allows for fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals FMOD/(32 × FILTCON1[14:0]).	0x0	RW
[14:12]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
11	ENHFILTEN1		This bit enables various post filters for enhanced 50 Hz/60 Hz rejection for Setup 1. The ORDER bits must be set to 00 to select the sinc5 + sinc1 filter for this to work.	0x0	RW
		0	Disabled		
		1	Enabled		
[10:8]	ENHFILT1		These bits select between various post filters for enhanced 50 Hz/60 Hz rejection for Setup 1.	0x0	RW
		010	27 SPS, 47 dB rejection, 36.7 ms settling		
		011	25 SPS, 62 dB rejection, 40 ms settling		
		101	20 SPS, 86 dB rejection, 50 ms settling		
		110	16.67 SPS, 92 dB rejection, 60 ms settling		
7	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[6:5]	ORDER1		These bits control the order of the digital filter that processes the modulator data for Setup 1.	0x0	RW
		00	Sinc5 + sinc1 (default)		
		11	Sinc3. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels.		
[4:0]	ODR1		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 1.	0x0	RW
		00000	250,000		
		00001	125,000		
		00010	62,500		
		00011	50,000		
		00100	31,250		
		00101	25,000		
		00110	15,625		
		00111	10,000		
		01000	5000		
		01001	2500		
		01010	1000		
		01011	500		
		01100	397.5		
		01101	200		
		01110	100		
		01111	59.94		
		10000	49.96		
		10001	20		
		10010	16.667		
		10011	10		
		10100	5		

FILTER CONFIGURATION REGISTER 2

Address: 0x2A, Reset: 0x0000, Name: FILTCON2

The Filter Configuration Registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 41. Bit Descriptions for FILTCON2

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAP2		If this bit is set, the mapping of the Filter Register changes to directly program the decimation rate of the sinc3 filter for Setup 2. All other options are eliminated. This allows for fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals FMOD/(32 × FILTCON2[14:0]).	0x0	RW
[14:12]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
11	ENHFILTEN2		This bit enables various post filters for enhanced 50 Hz/60 Hz rejection for Setup 2. The ORDER bits must be set to 00 to select the sinc5 + sinc1 filter for this to work.	0x0	RW
		0	Disabled		
		1	Enabled		
[10:8]	ENHFILT2		These bits select between various post filters for enhanced 50 Hz/60 Hz rejection for Setup 2.	0x0	RW
		010	27 SPS, 47dB rejection, 36.7 ms settling		
		011	25 SPS, 62 dB rejection, 40 ms settling		
		101	20 SPS, 86 dB rejection, 50 ms settling		
		110	16.67 SPS, 92 dB rejection, 60 ms settling		
7	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[6:5]	ORDER2		These bits control the order of the digital filter that processes the modulator data for Setup 2.	0x0	RW
		00	Sinc5 + sinc1 (default)		
		11	Sinc3. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels.		
[4:0]	ODR2		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 2.	0x0	RW
		00000	250,000		
		00001	125,000		
		00010	62,500		
		00011	50,000		
		00100	31,250		
		00101	25,000		
		00110	15,625		
		00111	10,000		
		01000	5000		
		01001	2500		
		01010	1000		
		01011	500		
		01100	397.5		
		01101	200		
		01110	100		
		01111	59.94		
		10000	49.96		
		10001	20		
		10010	16.667		
		10011	10		
		10100	5		

FILTER CONFIGURATION REGISTER 3

Address: 0x2B, Reset: 0x0000, Name: FILTCON3

The Filter Configuration Registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence.

Table 42. Bit Descriptions for FILTCON3

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAP3		If this bit is set, the mapping of the Filter Register changes to directly program the decimation rate of the sinc3 filter for Setup 3. All other options are eliminated. This allows for fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals FMOD/(32 × FILTCON3[14:0]).	0x0	RW
[14:12]	RESERVED		These bits are reserved and should be set to 0.	0x0	R
11	ENHFILTEN3		This bit enables various post filters for enhanced 50 Hz/60 Hz rejection for Setup 3. The ORDER bits must be set to 00 to select the sinc5 + sinc1 filter for this to work.	0x0	RW
		0	Disabled		
		1	Enabled		
[10:8]	ENHFILT3		These bits select between various post filters for enhanced 50 Hz/60 Hz rejection for Setup 3.	0x0	RW
		010	27 SPS, 47 dB rejection, 36.7 ms settling		
		011	25 SPS, 62 dB rejection, 40 ms settling		
		101	20 SPS, 86 dB rejection, 50 ms settling		
		110	16.67 SPS, 92 dB rejection, 60 ms settling		
7	RESERVED		This bit is reserved and should be set to 0.	0x0	R
[6:5]	ORDER3		These bits control the order of the digital filter that processes the modulator data for Setup 3.	0x0	RW
		00	Sinc5 + sinc1 (default)		
		11	Sinc3. When using the sinc3 filter, the user must select the sinc3 filter and use the same output data rate for all enabled channels.		
[4:0]	ODR3		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup 3.	0x0	RW
		00000	250,000		
		00001	125,000		
		00010	62,500		
		00011	50,000		
		00100	31,250		
		00101	25,000		
		00110	15,625		
		00111	10,000		
		01000	5000		
		01001	2500		
		01010	1000		
		01011	500		
		01100	397.5		
		01101	200		
		01110	100		
		01111	59.94		
		10000	49.96		
		10001	20		
		10010	16.667		
		10011	10		
		10100	5		

OFFSET REGISTER 0

Address: 0x30, Reset: 0x800000, Name: OFFSET0

The Offset (Zero-Scale) Registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Table 43. Bit Descriptions for OFFSET0

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET0		Offset calibration coefficient for Setup 0.	0x800000	RW

OFFSET REGISTER 1

Address: 0x31, Reset: 0x800000, Name: OFFSET1

The Offset (Zero-Scale) Registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Table 44. Bit Descriptions for OFFSET1

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET1		Offset calibration coefficient for Setup 1.	0x800000	RW

OFFSET REGISTER 2

Address: 0x32, Reset: 0x800000, Name: OFFSET2

The Offset (Zero-Scale) Registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Table 45. Bit Descriptions for OFFSET2

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET2		Offset calibration coefficient for Setup 2.	0x800000	RW

OFFSET REGISTER 3

Address: 0x33, Reset: 0x800000, Name: OFFSET3

The Offset (Zero-Scale) Registers are 24-bit registers that can be used to compensate for any offset error in the ADC or in the system.

Table 46. Bit Descriptions for OFFSET3

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET3		Offset calibration coefficient for Setup 3.	0x800000	RW

GAIN REGISTER 0

Address: 0x38, Reset: 0x5xxxx0, Name: GAIN0

The Gain (Full-Scale) Registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Table 47. Bit Descriptions for GAIN0

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN0		Gain calibration coefficient for Setup 0.	0x5XXXX0	RW

GAIN REGISTER 1

Address: 0x39, Reset: 0x5xxxx0, Name: GAIN1

The Gain (Full-Scale) Registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Table 48. Bit Descriptions for GAIN1

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN1		Gain calibration coefficient for Setup 1.	0x5XXXX0	RW

GAIN REGISTER 2

Address: 0x3A, Reset: 0x5xxxx0, Name: GAIN2

The Gain (Full-Scale) Registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Table 49. Bit Descriptions for GAIN2

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN2		Gain calibration coefficient for Setup 2.	0x5XXXX0	RW

GAIN REGISTER 3

Address: 0x3B, Reset: 0x5xxxx0, Name: GAIN3

The Gain (Full-Scale) Registers are 24-bit registers that can be used to compensate for any gain error in the ADC or in the system.

Table 50. Bit Descriptions for GAIN3

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN3		Gain calibration coefficient for Setup 3.	0x5XXXX0	RW

OUTLINE DIMENSIONS

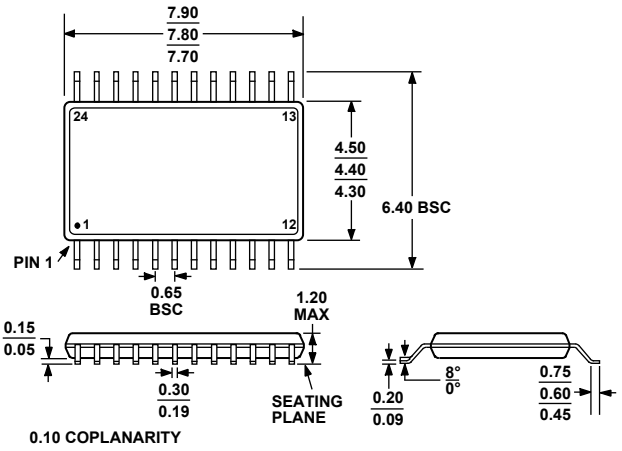


Figure 69. 24-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-24)
Dimensions shown in millimeters

ORDERING GUIDE

Models[1]	Temperature Range	Package Description	Package Option
AD7176-2BRUZ	–40°C to +105°C	24-Lead TSSOP	RU-24
AD7176-2BRUZ-RL	–40°C to +105°C	24-Lead TSSOP	RU-24
EVAL-AD7176-2SDZ		Evaluation Board	
EVAL-SDP-CB1Z		Evaluation Controller Board	

[1] Z = RoHS Compliant Part.

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