Universal Input Analog Front End with 24-Bit ADC for Industrial Process Control Systems

Data Sheet

AD4110-1

FEATURES

- 2 software programmable input terminals
  - Current up to ±20 mA
  - Voltage up to ±10 V
  - Thermocouple
  - RTD
- Replaces existing 3-terminal solutions
- Field power supply for loop powered current sensors
- HV input overvoltage protected up to ±30 V
- Internal current sense resistor
- Option to use external current sense resistor
- Current limited input even with no power supply
- Diagnostic functions for overrange and open wire detect
- Fast and flexible output data rates: 5 SPS to 125 kSPS
  - 16 noise free bits at 62 kSPS
  - 18 noise free bits at 2.5 kSPS
  - 20 noise free bits at 50 SPS/60 SPS
- Simultaneous 50 Hz and 60 Hz rejection
- Serial interface for configuration and diagnostics
  - 4-wire interface compatible with SPI®, QSPI™, MICROWIRE®, and DSP
- Power supply: ±12 V to ±20 V, +5 V
- Operating temperature: −40°C to +105°C
- Package: 40-lead, 6 mm × 6 mm LFCSP

APPLICATIONS

- Process control and industrial automation
- Remote and distributed control systems
- Instrumentation and measurement
- Sensor and data acquisition

GENERAL DESCRIPTION

The AD4110-1 is a complete, single-channel, universal input analog-to-digital front end for industrial process control systems where sensor type flexibility is required.

The high voltage input is fully software configurable for current or voltage signals and allows direct interface to all standard industrial analog signal sources such as ±20 mA, ±4 mA to ±20 mA, ±10 V, and all thermocouple types. Field power can be supplied for loop powered current output sensors. A range of excitation current sources for resistance temperature detector (RTD) sensors and other resistive sensors are included. The integrated, fully differential programmable gain amplifier (PGA) offers 16 gain settings from 0.2 to 24.

The high voltage input can be programmed to power up in either voltage mode or current mode. When programmed to current mode, the unique input circuit architecture provides a path for the loop current, even in the absence of the system module power supply.

The AD4110-1 provides internal, front-end diagnostic functions to indicate overvoltage, undervoltage, open wire, overcurrent, and overtemperature conditions. The high voltage input is thermally protected, overcurrent limited, and overvoltage protected.

The AD4110-1 incorporates a precision 24-bit, Σ-Δ, analog-to-digital converter (ADC) offering conversion rates from 5 SPS to 125 kSPS with simultaneous 50 Hz and 60 Hz noise rejection.

FUNCTIONAL BLOCK DIAGRAM

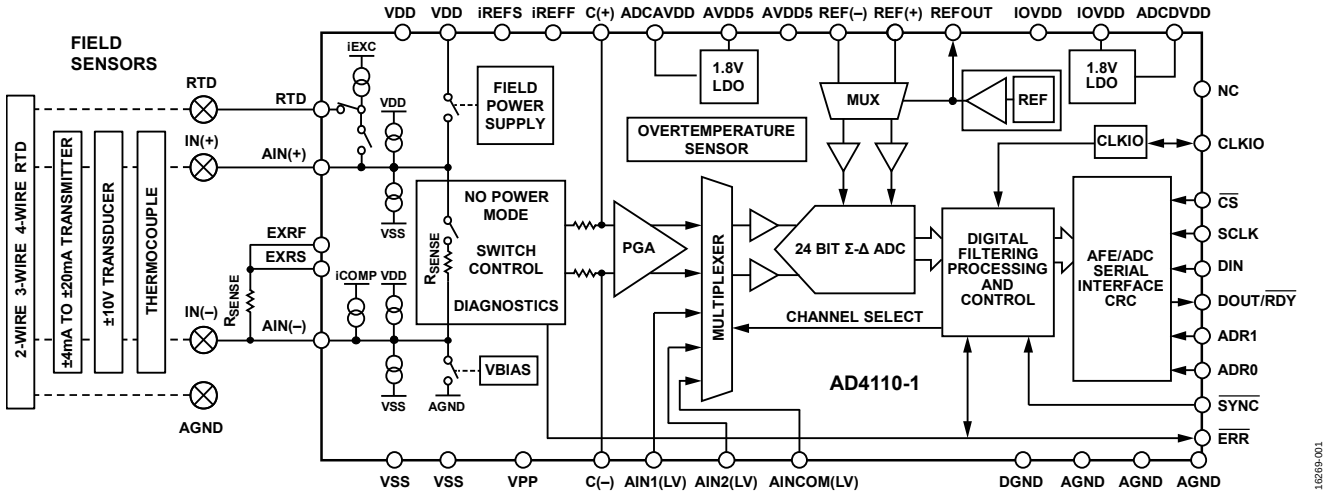


Figure 1. Functional Block Diagram

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

3/2019—Revision 0: Initial Version

SPECIFICATIONS

VDD = +12 V to 20 V, VSS = −12 V to −20 V, AVDD5 = +5 V, IOVDD = +5 V, AGND = DGND = 0 V, VBIAS function = off, REFIN(+) = 2.5 V (external reference), REFIN(−) = 0 V, MCLK = 8 MHz (internal ADC clock), T_A = −40°C to +105°C, all gains, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIGH VOLTAGE ANALOG INPUTS, AIN(±) Pins					
Differential Input Voltage Range, Reference Voltage (V_{REF}) ≤ 2.5 V	−V_{REF}/Gain		+V_{REF}/Gain	V	For specified performance, gain > 0.2
	−10		+10	V	For specified performance, gain = 0.2
	−12.5		+12.5	V	Functional range, gain = 0.2
Absolute AIN Voltage	VSS + 3		VDD − 3	V	For specified performance
Overvoltage Protection[1, 2]					
AIN(+) – AGND, AIN(–) – AGND, AIN(+) – AIN(–) Pins			±30	V	Using input resistor-capacitor (RC) low-pass filter with resistor (R) = 10 Ω, 0.5 W and capacitor (C) = 47 nF 50 V, VDD/VSS ≤ ±15 V
VOLTAGE INPUT MODE					
Gain Error					
Before Calibration[3]	−1		+1	%	T_A = 25°C
Using Calibration Coefficient[4]	−0.03		+0.03	%	T_A = 25°C, VDD/VSS = ±15 V
Gain Drift vs. Temperature[2]	−3		+3	ppm/°C	All gains except gain = 1
	−8		+8	ppm/°C	Gain = 1
Gain Drift vs. Time[5]		±30		ppm	Over 1000 hours
Input Offset Error[6]	−350/Gain		+350/Gain	µV	Gain = 0.2 to 3
	−100		+100	µV	Gain = 4 to 24
Input Offset Drift vs. Temperature[2]		2	14	µV/°C	Gain = 0.2, referred to input
		0.2	0.5	µV/°C	Gain = 24, referred to input
Input Offset Drift vs. Time[5]		±50		µV	Gain = 0.2, over 1000 hours
		±25		µV	Gain = 1, over 1000 hours
		±4		µV	Gain = 24, over 1000 hours
Integral Nonlinearity		6		ppm/FSR	Gain = 0.2, full-scale range (FSR) = 2 × full scale (FS)
		25	75	ppm/FSR	Gain = 24
Input Bias Current, AIN(+), AIN(–) Pins[2]	−0.5		+0.5	µA	
Input Bias Current, AIN(+) Pin	−0.25	−0.15	−0.05	µA	AIN(+) − AIN(−) < ±100 mV, AIN(−) = 0 V, VBIAS on/off, gain = 24, source impedance < 5 kΩ
Input Bias Current Drift[2]		1	2.5	nA/°C	AIN(+) and AIN(−)
Input Offset Current[2]	−100		+100	nA	
Input Impedance[7]		>1		GΩ	$\Delta V_{IN} \div \Delta I_{IN}$
Input Voltage Noise and Resolution[2]					See Table 16 to Table 21
Input Common-Mode Rejection, DC		125		dB	Gain = 24
		100		dB	Gain = 0.2
Input Common-Mode Rejection, AC		130		dB	50 Hz/60 Hz
Power Supply Rejection, DC[8]		120		dB	Related to VSS and VDD
		83		dB	Related to AVDD5, gain = 1, V_{IN} = 1 V
Normal Mode Rejection, 50 Hz/60 Hz		40		dB	Sinc5 + sinc1 filter, ±0.5 Hz, external clock
		100		dB	Sinc3 filter, ±1 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT INPUT MODE USING INTERNAL SENSE RESISTOR[9]					Gain = 4
Input Current Range[10]	−20		+20	mA	Specified performance range
	−24		+24	mA	Functional range
Transimpedance Gain		96		mV/mA	Gain = 4, sense resistor (R_{SENSE}) = 24 Ω
Gain Error					
Before Calibration[3]		±30		%	
Using Calibration Coefficient[4]	−0.1		+0.1	%	T_A = 25°C, I_{IN} = 20 mA
Gain Drift vs. Temperature[2]	−50		+50	ppm/°C	Excludes reference drift, includes R_{SENSE} resistor drift
Gain Drift vs. Time[5]		250		ppm	Over 1000 hours
Input Offset Error	−5		+5	µA	
Input Offset Drift vs. Temperature[2]			50	nA/°C	
Input Offset Drift vs. Time[5]		±200		nA	Over 1000 hours
Integral Nonlinearity		25	75	ppm/FSR	FSR = 2 × FS
Input Overcurrent Detection		±35		mA	
Input Current Internal Limit[10]		±40		mA	Overcurrent self-protection
Input Impedance[2, 11]	30	45	60	Ω	Input current <±24 mA
Input Current Noise and Resolution					See Table 16 to Table 21
Input Common-Mode Rejection, DC		0.15		µA/V	
Power Supply Rejection, DC[8]		0.01		µA/V	Related to VDD and VSS
CURRENT INPUT MODE USING EXTERNAL SENSE RESISTOR[12, 13]					External sense resistor (R_{EXT}) = 200 Ω, gain = 0.5
Input Current Range[7]	−20		+20	mA	Specified performance range
	−24		+24	mA	Functional range
Input Overcurrent Detection		±35		mA	
Input Current Internal Limit[7]		±40		mA	Overcurrent self-protection
Gain Drift vs. Temperature[2]			2.5	ppm/°C	Excludes reference drift and drift of external sense resistor
ADC SPEED AND PERFORMANCE					
Output Data Rate[2]	5		125,000	SPS	
No Missing Codes[2]	24			Bits	Sinc5 + sinc1 filter setting
Resolution					See Table 16 to Table 21
NO POWER SUPPLY MODE					
Input Voltage Drop		5		V	Current mode, input current = 24 mA
Input Current Internal Limit[2]		±55	±70	mA	Current mode, overcurrent self-protection
Input Current Loss		70		µA	Current mode, 24 mA, GND connected
Input Current in Voltage Mode		±0.5		mA	Voltage mode
FIELD POWER SUPPLY MODE					
Output Voltage, AIN(+) Pin[2]	VDD − 2.5	VDD − 1.5		V	Output current = 24 mA
		VDD − 0.1	VDD	V	No load
Output Current, AIN(+) Pin			−24	mA	
Output Current Limit, AIN(+) Pin[2]	−35	−45	−55	mA	Overcurrent self-protection
Voltage, AIN(−) Pin[2]		VSS + 3.6	VSS + 4.2	V	AIN(−) with 24 mA, no VSS diode
	VSS + 2.2	VSS + 2.7		V	No load, no VSS diode
Input Current Limit, AIN(−) Pin		+40		mA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RTD EXCITATION CURRENTS[14]					External reference voltage (V_{REF}) = 2.5 V ± 0%
Current Outputs		0.1 to 1		mA	Programmable (see Table 30)
Initial Error, Internal Reference Resistor	−0.3		+0.3	%	Current ≥ 400 µA, T_A = 25°C
	−1		+1	%	Current = 100 µA, T_A = 25°C
Initial Drift		130		ppm	See Figure 44 and Figure 45
Drift vs. Temperature[2]	−45		+45	ppm/°C	Internal reference resistor (including reference resistor drift)
	−18		+18	ppm/°C	External reference resistor (excluding reference resistor drift)
Drift vs. Time[5, 15]		150		ppm	Internal resistor, over 1000 hours
		150		ppm	External resistor, over 1000 hours
Load Regulation[2]			0.01	%/V	
Line Regulation[2]		4		ppm/V	Related to VSS and VDD
Noise[2]	See Table 22 and Table 23				T_A = 25°C
Current Matching[15]		0.05		%	AIN(+) and AIN(−) pins, excludes 100 µA
Current Matching Drift		0.0002		%/°C	AIN(+) and AIN(−) pins, excludes 100 µA
Compliance			VDD − 5	V	
REFERENCE VOLTAGE (INPUT)					
Reference Voltage Input, V_{REF}[2, 14]	1	2.5	AVDD5 − 1.6	V	REFIN(+) − REFIN(−) = V_{REF} RTD mode disabled
	2.45	2.5	2.55	V	RTD mode enabled
V_{REF} Input Current		200		nA	V_{REF}+ reference buffer on
		100		µA	V_{REF}− reference buffer on
		36		µA/V	V_{REF}+ reference buffer off
		75		µA/V	V_{REF}− reference buffer off
V_{REF} Input Current Drift		1.3		nA/°C	V_{REF}+ reference buffer on
		−3.5		nA/°C	V_{REF}− reference buffer on
		10		nA/V/°C	V_{REF}+ reference buffer off
		10		nA/V/°C	V_{REF}− reference buffer off
Absolute REFIN Voltage Limits	AGND − 0.05		AVDD5 + 0.05	V	
	AGND		AVDD5	V	Reference buffer on
Common-Mode Rejection		95		dB	
REFERENCE VOLTAGE (OUTPUT)					
Output Voltage		2.5		V	REFOUT pin
Initial Accuracy[2]	−0.16		+0.16	V	T_A = 25°C
Temperature Coefficient[2]		10	50	ppm/°C	
Long Term Stability[5]		600		ppm	Over 1000 hours
Reference Load Current, I_{LOAD}			10	mA	
Power Supply Rejection		93		dB	
Load Regulation		75		µV/mA	
VBIAS					
Voltage		AGND		V	
Output Current Limit		±50		µA	Source or sink, depending on the AIN(−) pin potential referenced to AGND
OPEN WIRE DETECTION CURRENTS					
Current Output	±0.71	±1	±1.45	µA	
		±100		µA	
Compliance	VSS + 2		VDD − 2	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT OVERVOLTAGE DETECTION					
Positive Overvoltage Threshold		VDD − 2.0	VDD − 2.8	V	
Negative Overvoltage Threshold		VSS + 2.0	VSS + 2.8	V	
OVERTEMPERATURE PROTECTION					
Overtemperature Detection Threshold		120		°C	Junction temperature
Thermal Shutdown Threshold		145		°C	Junction temperature
Thermal Shutdown Hysteresis		30		°C	
ANTIALIASING FILTER RESISTOR					
AIN(±) to C(±) Resistance		1600		Ω	Includes internal switch resistance
Resistance Variation[2]			±35	%	
Mismatch		0.2		%	Resistor pair per channel
LOW VOLTAGE ANALOG INPUTS, AIN1(LV), AIN2(LV), AND AINCOM(LV)					
Differential Input Range		$\pm V_{REF}$		V	
Absolute Voltage Limit	AGND		AVDD5	V	
Input Current		±65		nA	
Input Current Drift		±75		pA/°C	AGND + 0.2 V to AVDD5 − 0.2 V
		±1		nA/°C	AGND to AVDD5
High Voltage (HV) to Low Voltage (LV) Channel Crosstalk[16]		−120		dB	Input frequency (f_{IN}) = 1 kHz, Gain (HV Channel) = 1
Input Common-Mode Rejection, DC		95		dB	
Input Common-Mode Rejection, AC		120		dB	50 Hz/60 Hz, V_{IN} = 1 V
DIGITAL INPUTS					
Input High Voltage, V_{IH}[2]	0.7 × IOVDD			V	IOVDD = 2 V to 5.5 V
Input Low Voltage, V_{IL}[2]			0.8	V	IOVDD = 3.3 V to 5.5 V
			0.4	V	IOVDD = 2 V
Hysteresis		100		mV	
Input Leakage Current	−10		+10	µA	
Input Pin Capacitance		10		pF	
DIGITAL OUTPUTS					
V_{OH}[2]	0.8 × IOVDD			V	IOVDD = 5 V, source current (I_{SOURCE}) = 1 mA
	0.8 × IOVDD			V	IOVDD = 3.3 V, I_{SOURCE} = 500 µA
	0.8 × IOVDD			V	IOVDD = 2 V, I_{SOURCE} = 500 µA
V_{OL}[2]			0.4	V	IOVDD = 5 V, sink current (I_{SINK}) = 2 mA
			0.4	V	IOVDD = 3.3 V, I_{SINK} = 1 mA
			0.4	V	IOVDD = 2 V, I_{SINK} = 1 mA
Floating State Leakage Current	−10		+10	µA	
Floating State Output Capacitance		12		pF	
ERROR OUTPUT (OPEN DRAIN)					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = −100 µA
Output High Leakage Current, I_{OH}	−10		+10	µA	Output voltage (V_{OUT}) = 5 V
CLOCK INPUT/OUTPUT					
Internal Oscillator		8		MHz	
Internal Oscillator Accuracy	−3.5		+3.5	%	ADC clock
Clock Input Frequency		8		MHz	
Duty Cycle, External Clock[2]	45	50	55	%	
V_{IH}[2]	0.8 × IOVDD			V	
V_{OH}	0.8 × IOVDD			V	
V_{OL}			0.4	V	
V_{IL}[2]			0.4	V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Input Leakage Current	−10		+10	µA	
Pin Capacitance		12		pF	
Duty Cycle, Internal Clock		50		%	
POWER REQUIREMENTS					See the Power Supply Sequence section
VDD − VSS Voltage	24	30	40	V	
AGND Voltage		(VDD − VSS)/2		V	
AVDD5 − AGND Voltage	4.5	5	5.5	V	
DGND Voltage		AGND		V	
IOVDD − DGND Voltage	2.0	5	5.5	V	
VDD Supply Current					
Field Power Supply Off		5.5	8	mA	All current sources off and disabled
		7.5	10	mA	RTD current sources on, other current sources off, VBIAS off
Field Power Supply On[2]		29.5		mA	Field power supply current = 24 mA to AGND, all current sources off and disabled, VBIAS off
VSS Supply Current					
Field Power Supply Off		−5.5	−8	mA	All current sources off and disabled
		−5.5	−10	mA	RTD current sources on, other current sources off, VBIAS off
Field Power Supply On[2]		−5.8		mA	Field power supply current = 24 mA to AGND, all current sources off and disabled, VBIAS off
AVDD5 Supply Current		10	12	mA	
IOVDD Supply Current		2.5	3.5	mA	

[1] The device is specified to operate with an input voltage from VSS + 3 V to VDD − 3 V on any AIN(±) pin. The device is protected against overvoltage on the AIN(+) and AIN(−) pins up to ±30 V (referred to the AGND supply). The limitation of VDD = VSS ≤ ± 15 V only applies when field power supply mode is enabled. Applying a voltage to a high voltage pin that is more negative than the potential of the system negative power supply can only be accomplished by connecting an external diode from the VSS pin to the system negative power supply (see Figure 29). The absolute maximum ratings must not be exceeded at any time (see Table 3).
[2] Specification is not production tested, but is supported by characterization data at initial product release.
[3] Gain error prior to applying software error correction algorithm. See the Gain Calibration Data Register section.
[4] Gain error after applying software error correction algorithm. See the Gain Calibration Application Examples section.
[5] Data based on the following test methods: - Moisture/Reflow Sensitivity (MSL) Classification for nonhermetic Solid State Surface Mount Devices and High Temperature Operating Life (HTOL).
[6] Offset voltage seen at the inputs in voltage mode. Note that RTD currents can cause an additional I × R offset voltage (±V) due to any mismatch in IC or PCB trace resistance. System calibration may be required when changing RTD excitation and compensation current levels.
[7] DC input impedance is derived from measuring the change in input current for a change in input voltage, ($\Delta V_{IN} \div \Delta I_{IN}$).
[8] Referred to input.
[9] PGA gain = 4 for all specifications related to the current input mode with internal sense resistor.
[10] Input current in current input mode must be within ±20 mA for fully specified performance. The device is functional up to ±24 mA. The internal protection limits the input overcurrent to approximately 40 mA.
[11] Current mode input impedance is the total impedance between the AIN(+) and AIN(−) pins, which includes the on-chip sense resistor, on-chip current mode switches, and other on-chip circuits. The relationship between the analog input current and the analog output voltage is represented by the gain and offset specifications.
[12] R_{EXT} = 200 Ω and gain = 0.5 for all specifications related to the current input mode with external sense resistor.
[13] The external resistor transfers the input current to a voltage for additional signal processing in this mode. The AD4110-1 specifications exclude the effect of any changes in the external resistor resistance. Performance of the external resistor must be considered to assess system performance in this mode.
[14] The AD4110-1 RTD excitation currents are designed to operate with a 2.5 V reference voltage. The AD4110-1 RTD excitation current value scales proportionally to small changes in the V_{REF} input voltage. The AD4110-1 RTD excitation current specifications exclude the effect of any changes in the V_{REF} input voltage.
[15] RTD current source enabled and current flowing continuously.
[16] This specification relates to the worst high voltage and low voltage channel pair. A 20 V p-p, 1 kHz sine wave input on the HV channel is attenuated by this amount on the other LV channels. The interferer signal is applied to an unselected channel. The filter network connected to C(+) and C(−) is implemented as shown in Figure 29. There is no filter network implemented on the input terminals.

TIMING SPECIFICATIONS

IOVDD = 2 V to 5.5 V, AGND = DGND = 0 V, C_{LOAD} = 20 pF, T_A = −40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description[1, 2]
t_3	50	ns min	SCLK high pulse width
t_4	50	ns min	SCLK low pulse width
READ OPERATION			
t_1	0	ns min	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns max	IOVDD = 4.5 V to 5.5 V
	20	ns max	IOVDD = 3.0 V to 3.6 V
	40	ns max	IOVDD = 2.0 V
t_2[3]	0	ns min	SCLK active edge to data valid delay[4]
	15	ns max	IOVDD = 4.5 V to 5.5 V
	20	ns max	IOVDD = 3.0 V to 3.6 V
	40	ns max	IOVDD = 2.0 V
t_5[5]	20	ns max	Bus relinquish time after $\overline{CS}$ inactive edge
t_6	0	ns min	SCLK inactive edge to $\overline{CS}$ inactive edge
WRITE OPERATION			
t_8	0	ns min	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns min	Data valid to SCLK edge setup time
t_{10}	8	ns min	Data valid to SCLK edge hold time
t_{11}	10	ns min	$\overline{CS}$ rising edge to SCLK edge hold time

[1] Sample tested during initial release to ensure compliance.
[2] See Figure 2 and Figure 3.
[3] t_2 is the time required for the output to cross the V_{OL} or V_{OH} limit.
[4] The SCLK active edge is the falling edge of SCLK.
[5] DOUT/$\overline{RDY}$ returns high after a read of the data register. In single conversion mode and continuous conversion mode, the same data can be read again, if required, while DOUT/$\overline{RDY}$ is high, although care must be taken to ensure that subsequent reads do not occur close to the next output update.

Timing Diagrams

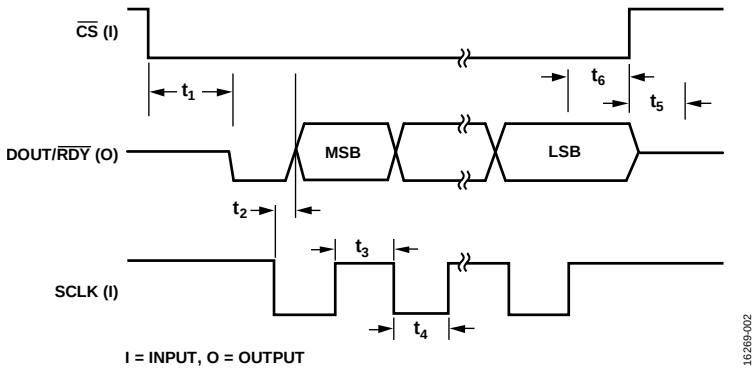


Figure 2. Data Read Timing Diagram

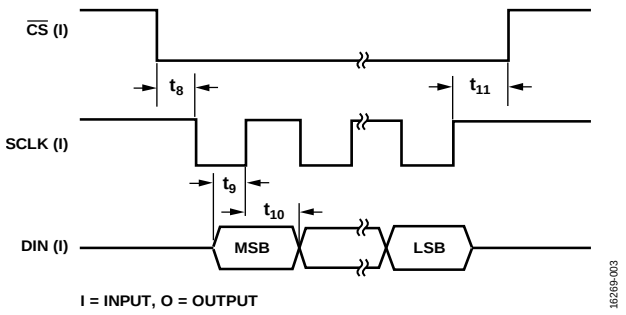


Figure 3. Data Write Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
Any HV Pin to VSS[1, 2]	−0.3 V to +60 V
VDD to VSS[3]	−0.3 V to +50 V
AIN(+) to AIN(−)[4]	±50 V
AVDD5 to AGND, DGND[3, 5]	−0.3 V to +6.5 V
IOVDD to AGND, DGND[3, 5]	−0.3 V to +6.5 V
AGND to DGND[5]	−0.3 V to +0.3 V
AGND to VSS	AGND ≥ VSS − 0.3 V
AVDD5 to VDD	AVDD5 ≤ VDD + 0.3 V
REFIN(+), REFIN(−), AIN1(LV), AIN2(LV), AINCOM(LV) to AGND	−0.3 V to AVDD5 + 0.3 V
Digital Inputs and Outputs to DGND	−0.3 V to IOVDD + 0.3 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Electrostatic Discharge (ESD), Human Body Model	700 V
Field Induced Charge Device Model (FICDM)	1250 V
Reflow Soldering (Pb-Free)	JEDEC J-STD-020
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec

[1] HV pins are AIN(+), AIN(−), RTD, EXRS, and EXRF.
[2] Applying a voltage to an HV pin that is more negative than the potential of the system negative power supply can only be accomplished by connecting an external diode from the VSS pin to the system negative power supply (see Figure 29).
[3] Pins with the same name must be shorted together.
[4] Using an input RC low-pass filter with R = 10 Ω, 0.5 W and C = 47 nF, 50 V.
[5] It is recommended to short AGND and DGND pins together as close to the device as possible.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-40-15[1]	35	°C/W

[1] θ_{JA} is specified for a device soldered on a JEDEC 4-layer test board for surface-mount packages with 16 thermal vias. The values listed in Table 4 are based on simulated data.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

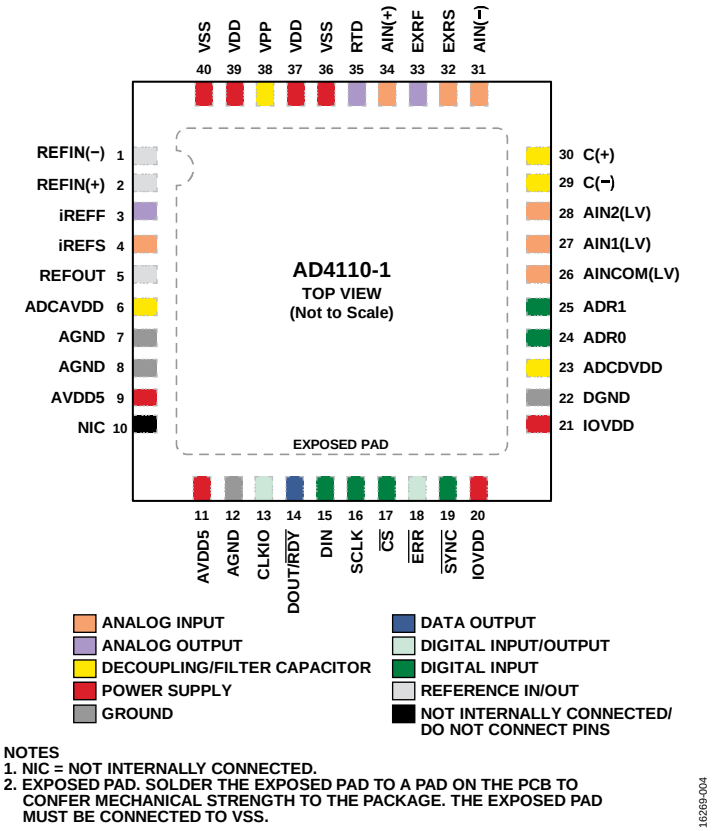


Figure 4. Pin Configuration

Table 5. Pin Function Descriptions[1]

Pin No.	Mnemonic	Description
1	REFIN(−)	Reference Input Negative. This pin works with the REFIN(+) pin. Connect to AGND.
2	REFIN(+)	Reference Input Positive. Connect an external reference voltage between the REFIN(+) and REFIN(−) pins. The RTD excitation current functionality operates with a 2.5 V reference only.
3	iREFF	RTD Excitation Current External Reference Resistor Force Pin. This pin is used when an external precision resistor is required as the reference for generating the RTD excitation currents. This pin forces the REFIN(+) voltage across the external resistor. Connect this pin and the iREFS pin in a star point to the top of the external precision resistor. Minimize the pin capacitance by placing the precision resistor as close as possible to the iREFS and iREFF pins. For more information, see the RTD Mode section. No other circuit connections are allowed.
4	iREFS	RTD Excitation Current External Reference Resistor Sense Pin. This pin is used when an external precision resistor is required as the reference for generating the RTD excitation currents. This pin senses the RTD reference current flowing through the external resistor. Connect this pin and the iREFF pin in a star point to the top of the external precision resistor. Minimize the pin capacitance by placing the precision resistor as close as possible to the iREFS and iREFF pins. For more information, see the RTD Mode section. No other circuit connections are allowed.
5	REFOUT	Internal 2.5 V Reference Output Pin. Decouple this pin to GND using a 100 nF capacitor when the internal reference is selected. Leave this pin open circuit when operating the device with an external reference applied to the REFIN(+) and REFIN(−) pins.
6	ADCAVDD	Decoupling Node for the Internal Linear Regulator Output. Decouple this pin using a 1 µF capacitor to AGND (Pin 7).
7	AGND	Analog Ground (0 V). Ground for the ADC core. It is recommended to short the AGND and DGND pins together, as close to the device as possible.
8	AGND	Analog Ground (0 V). Ground for the analog front end (AFE). It is recommended to short the AGND and DGND pins together as close to the device as possible.
9	AVDD5	Analog Power Supply (5 V). Power supply for the ADC core.
10	NIC	Not internally connected.
11	AVDD5	Analog Power Supply (5 V). Power supply for the AFE.
12	AGND	Analog Ground (0 V). Ground for the AFE. It is recommended to short the AGND and DGND pins together as close to the device as possible.

Pin No.	Mnemonic	Description
13	CLKIO	Clock Input/Output. This pin is the input for an external clock or the output of the on-chip clock.
14	DOUT/$\overline{\text{RDY}}$	Serial Interface Data Output (DOUT). This pin functions as a serial data output to access the output register of the ADC. The data is placed on the DOUT/$\overline{\text{RDY}}$ pin after the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. Data Ready Output ($\overline{\text{RDY}}$). When $\overline{\text{CS}}$ is low, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.
15	DIN	Serial Interface Data Input. Digital input.
16	SCLK	Serial Interface Clock. Digital input.
17	$\overline{\text{CS}}$	Serial Interface Chip Select/Frame. Digital input.
18	$\overline{\text{ERR}}$	Error Input/Output. Open-drain digital output.
19	$\overline{\text{SYNC}}$	ADC Synchronization Input. When $\overline{\text{SYNC}}$ is brought low, the ADC aborts any active ADC conversion, and brings $\overline{\text{RDY}}$ high if it is low. When $\overline{\text{SYNC}}$ is brought high, the ADC starts a new conversion within a number of clock cycles. If multiple ADC channels are enabled the conversions restart with the first channel in the sequence.
20, 21	IOVDD	Digital Power Supply (2 V to 5 V). Power supply for digital inputs and outputs.
22	DGND	Digital Ground (0 V). Reference ground for the digital inputs and outputs. It is recommended to short the AGND and DGND pins together as close to the device as possible.
23	ADCDVDD	Decoupling Node for the Internal Linear Regulator Output. Decouple this pin using a 1 µF capacitor to DGND (Pin 22).
24, 25	ADR0, ADR1	Serial Interface Address. Digital input.
26	AINCOM(LV)	Low Voltage Analog Input. AIN1(LV) and AIN2(LV) are referenced to this pin when the device is configured in pseudo differential mode.
27	AIN1(LV)	Low Voltage Analog Input. This input can be configured as a fully differential input with AIN2(LV) or as a single-ended or pseudo differential input when configured for use with AINCOM(LV).
28	AIN2(LV)	Low Voltage Analog Input. This input can be configured as a fully differential input with AIN1(LV) or as a single-ended or pseudo differential input when configured for use with AINCOM(LV).
29	C(–)	Capacitor Terminal Negative. Filter capacitors can be connected between this pin and C(+) and/or between this pin and analog ground (AGND). No other circuit connections are allowed.
30	C(+)	Capacitor Terminal Positive. Filter capacitors can be connected between this pin and C(–) and/or between this pin and analog ground (AGND). No other circuit connections are allowed.
31	AIN(–)	Analog Input Negative. In voltage mode, this pin is the negative input. In a 3-wire RTD connection, RTD compensation current flows out of this terminal. This pin also functions as the negative sense voltage terminal for the external sense resistor in current mode.
32	EXRS	External Resistor Sense. Sense (voltage) terminal for an external sense resistor in current mode.
33	EXRF	External Resistor Force. Force (current) terminal for an external sense resistor in current mode. If an external sense resistor is not used in the application, this pin must be connected to the AIN(–) pin for current mode operation; that is, the external resistor must be replaced by a short connection or a 0 Ω resistor.
34	AIN(+)	Analog Input Positive. In voltage and current modes, this pin is the positive input. In a 3-wire RTD connection, RTD excitation current flows out of this terminal. This pin also functions as a positive field power supply output in field power supply mode.
35	RTD	Resistance Temperature Detector Pin. In a 4-wire RTD connection, RTD excitation current flows out of this terminal.
36	VSS[2]	Negative Power Supply (−12 V to −20 V). A 10 µF decoupling capacitor is recommended.
37	VDD	Positive Power Supply (12 V to 20 V). A 10 µF decoupling capacitor is recommended.
38	VPP	Internal 5 V node. A decoupling capacitor must be connected to this pin; no other circuit connections are allowed. Connect a 0.1 µF ceramic capacitor between the VPP and the VSS pins.
39	VDD	Positive Power Supply (12 V to 20 V).
40	VSS[2]	Negative Power Supply (−12 V to −20 V).
EPAD	VSS[2]	Exposed Pad. Solder the exposed pad to a pad on the PCB to confer mechanical strength to the package. The exposed pad must be connected to VSS.

[1] Pins with the same name must be shorted together.
[2] Applying a voltage to an HV pin that is more negative than the potential of the system negative power supply can only be accomplished by connecting an external diode from the VSS pin to the system negative power supply. See Figure 29 for the connection diagram.

TYPICAL PERFORMANCE CHARACTERISTICS

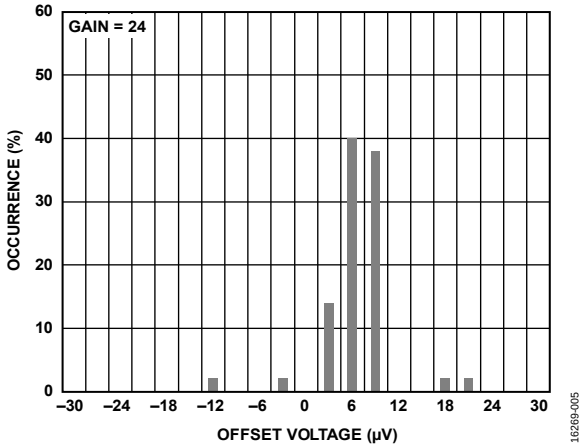


Figure 5. Voltage Mode, Offset Voltage Distribution (Gain = 24)

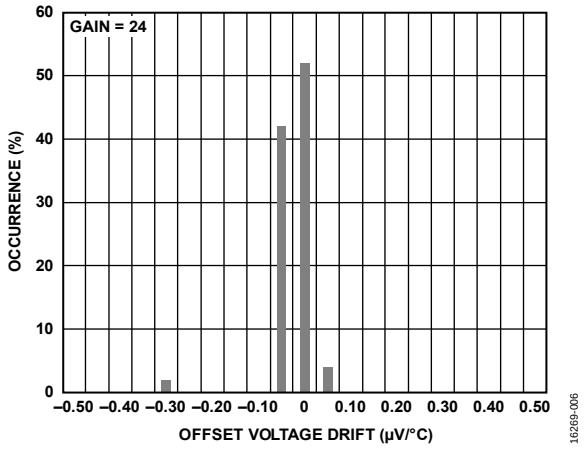


Figure 6. Voltage Mode, Offset Voltage Drift Distribution (Gain = 24)

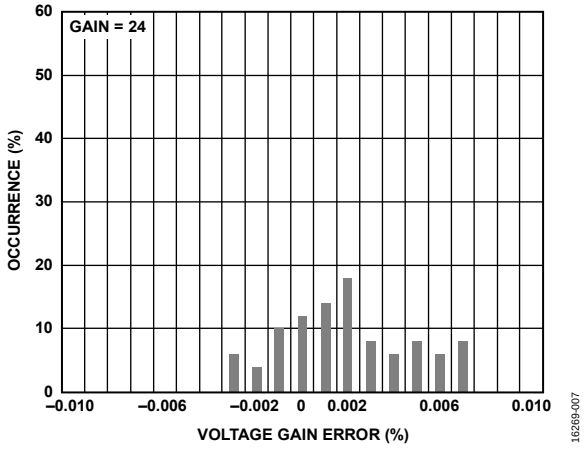


Figure 7. Voltage Mode, Gain Error Distribution (Gain = 24)

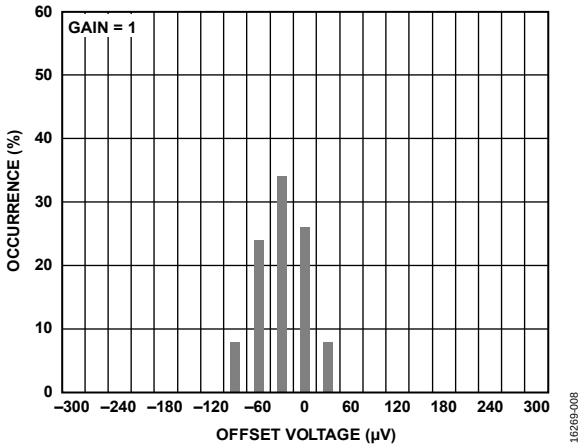


Figure 8. Voltage Mode, Offset Voltage Distribution (Gain = 1)

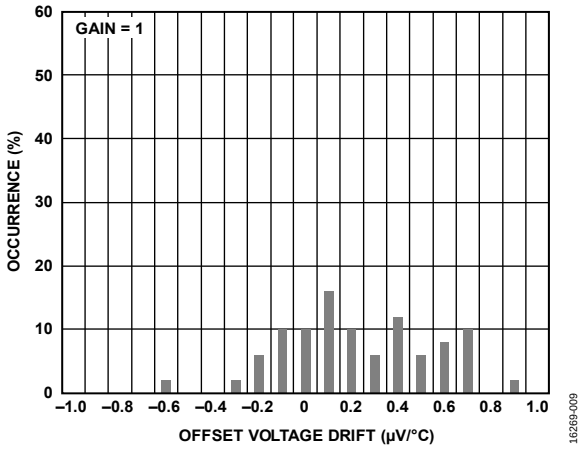


Figure 9. Voltage Mode, Offset Voltage Drift Distribution (Gain = 1)

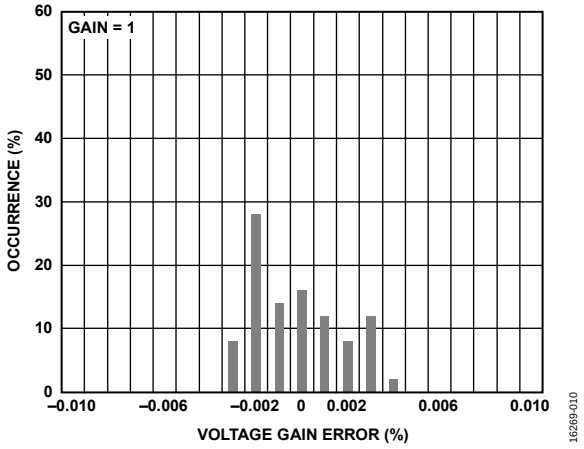


Figure 10. Voltage Mode, Gain Error Distribution (Gain = 1)

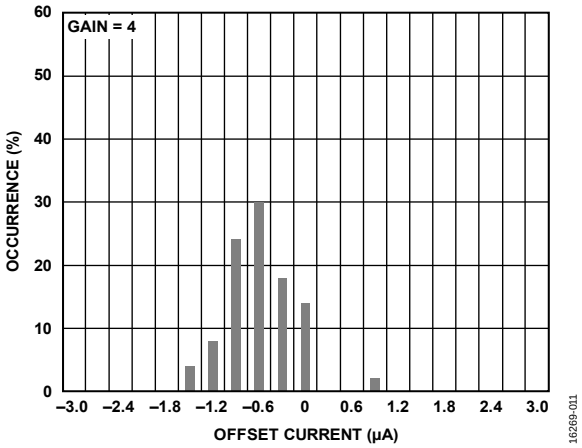


Figure 11. Current Mode, Offset Current Distribution (Gain = 4)

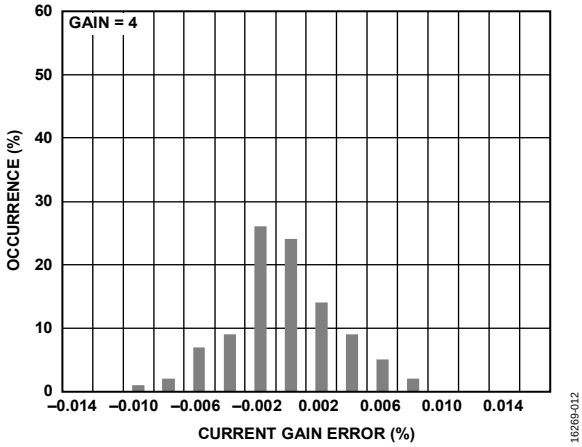


Figure 12. Current Mode, Gain Error Distribution (Gain = 4)

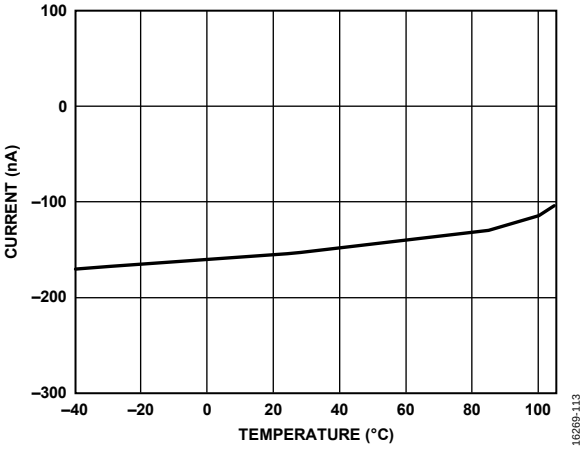


Figure 13. Input Bias Current (Gain = 24)

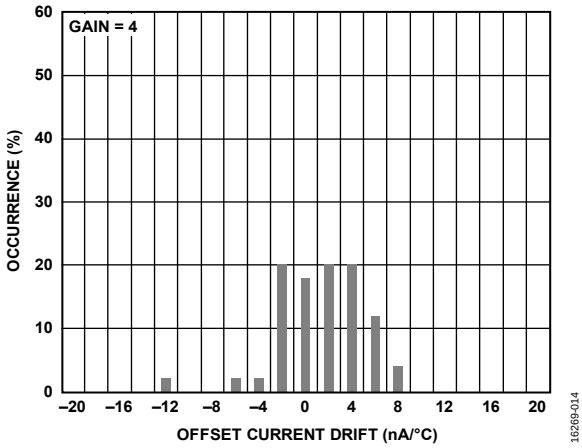


Figure 14. Current Mode, Offset Current Drift Distribution (Gain = 4)

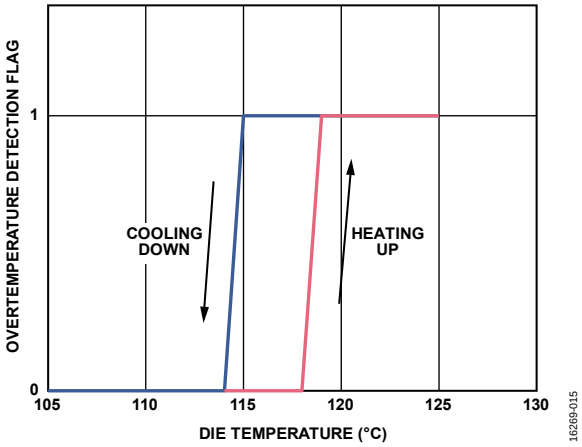


Figure 15. Overtemperature Detection

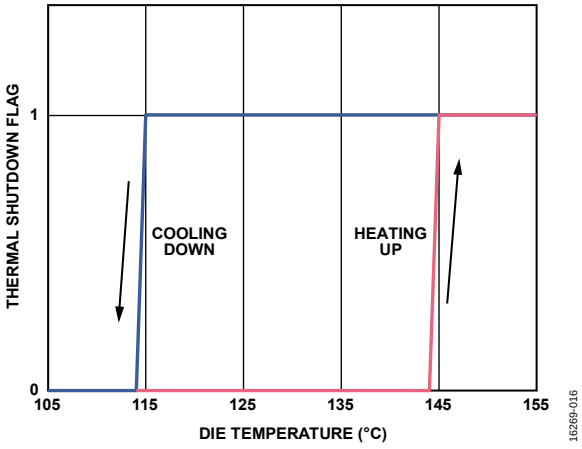


Figure 16. Thermal Shutdown

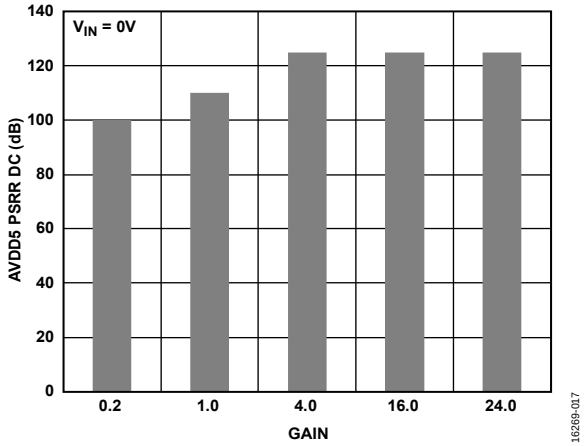


Figure 17. DC Power Supply Rejection Ratio (PSRR), AVDD5 Only

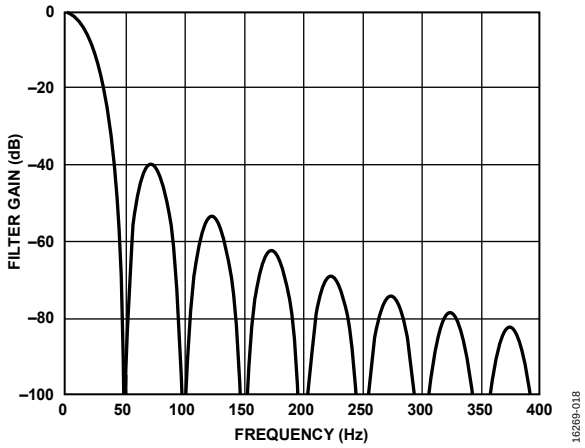


Figure 18. Normal Mode Rejection, Sinc3 Filter, Output Data Rate = 50 SPS

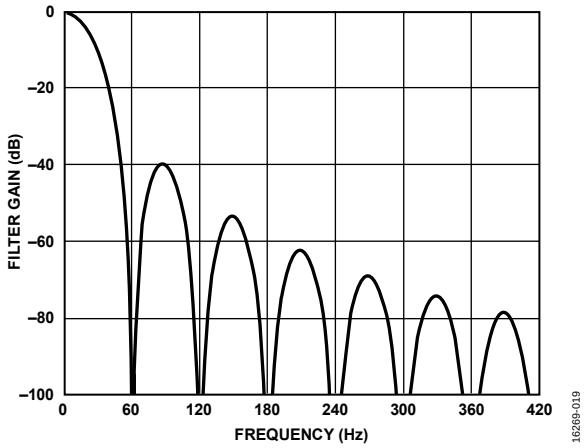


Figure 19. Normal Mode Rejection, Sinc3 Filter, Output Data Rate = 60 SPS

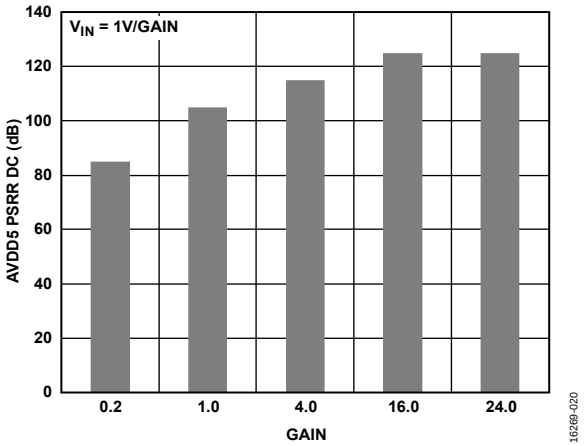


Figure 20. DC PSRR (AVDD5 Only)

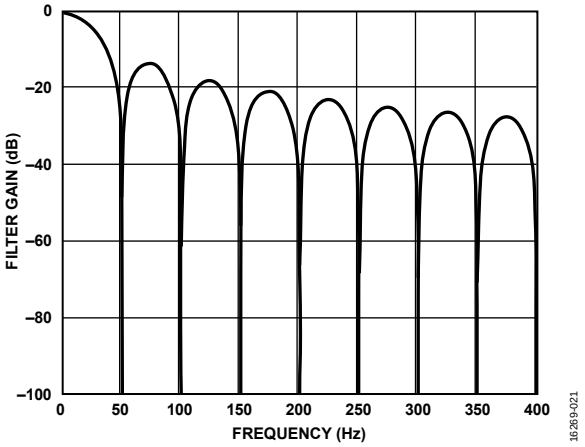


Figure 21. Normal Mode Rejection, Sinc5 + Sinc1 Filter, Output Data Rate = 49.92 SPS

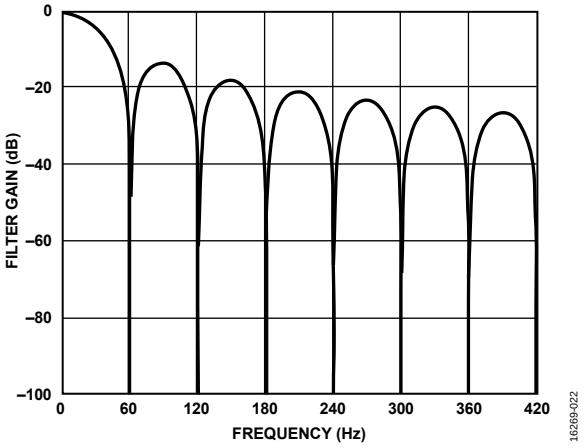


Figure 22. Normal Mode Rejection, Sinc5 + Sinc1 Filter, Output Data Rate = 59.9 SPS

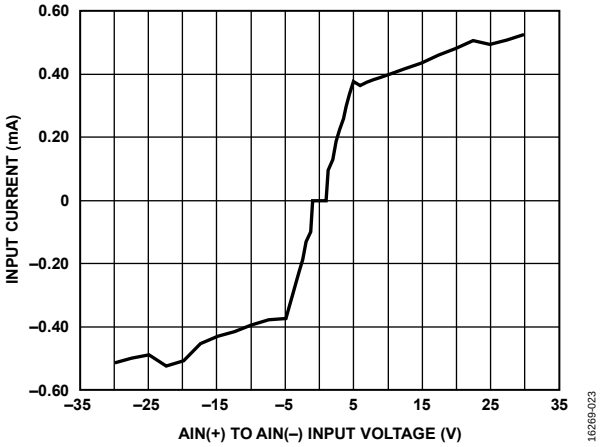


Figure 23. No Supply Mode, Input Current in Voltage Mode

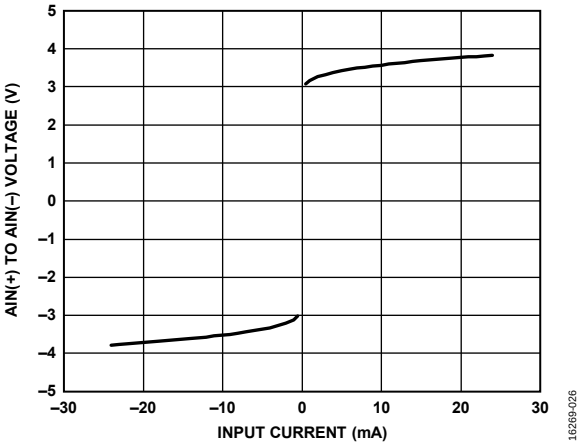


Figure 26. No Supply Mode, AIN(+) to AIN(–) Voltage Drop in Current Mode

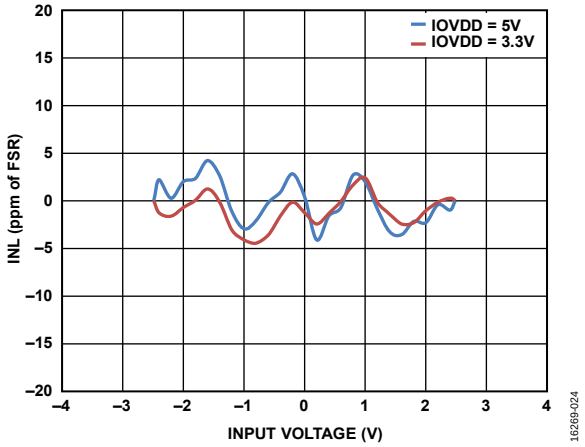


Figure 24. Integral Nonlinearityl (INL), Voltage Mode, Gain = 1

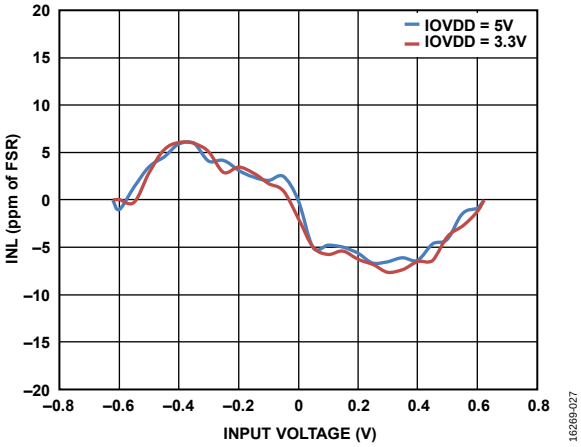


Figure 27. INL, Voltage Mode, Gain = 4

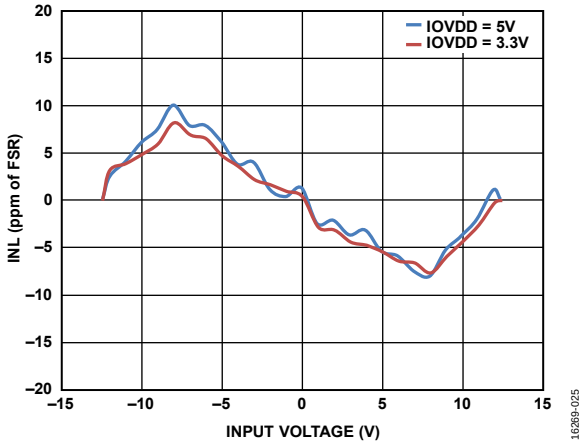


Figure 25. INL, Voltage Mode, Gain = 0.2

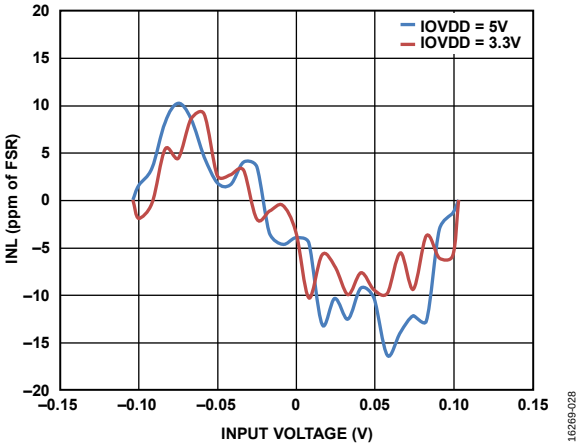


Figure 28. INL, Voltage Mode, Gain = 24

THEORY OF OPERATION

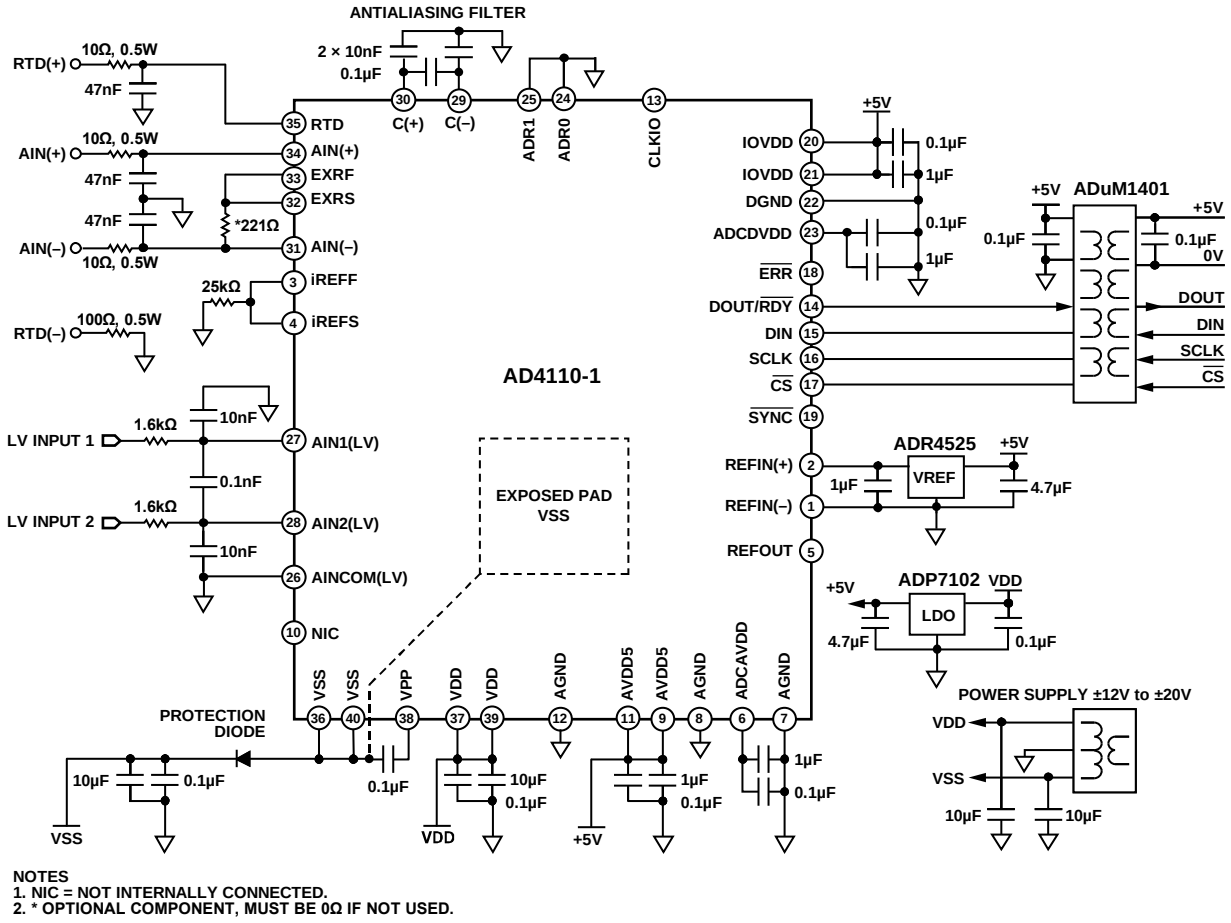


Figure 29. Typical Application Diagram

The AD4110-1 is a complete analog front end for industrial process control systems. The AD4110-1 provides a single, high voltage protected analog input channel that accepts either a voltage or current signal on two input terminals.

The high voltage input is fully software configurable for current or voltage ranges and allows a direct interface to all standard industrial analog signal sources such as ±4 mA to ±20 mA loops, voltage output sensors, thermocouples, and RTDs. Excitation current sources for RTD and other resistive sensors are also included in the device.

Figure 29 shows the basic connections required to operate the device. When the device is configured for current input, the unique circuit architecture provides a path for the loop current, even when the module power supply is absent.

The design features a PGA. The PGA removes potentially large common-mode signals and then applies gain or attenuates the input signal. This conditioned signal is converted by a fully buffered, 24-bit, Σ-Δ ADC with a maximum output data rate of 125 kSPS.

The low voltage inputs, AINCOM(LV), AIN1(LV), and AIN2(LV), allow the user to route signals directly to the ADC input multiplexer. These low voltage input channels are not high voltage protected and have different maximum ratings than the AIN(+) and AIN(–) high voltage inputs. The low voltage input channels are useful for applications where cold junction compensation is required for a thermocouple input.

Key features of the AD4110-1 include the internal front-end diagnostic functions and protection mechanisms for current and voltage modes. These features include the indication of overcurrent, overvoltage, and overtemperature conditions with automatic shutdown. System level diagnostics enable open wire detection and out of compliance current sources. The AD4110-1 provides enhanced digital filter modes of operation for 50 Hz/60 Hz noise rejection and a precision on-chip voltage reference, as well as fully buffered analog and reference inputs to the ADC.

POWER SUPPLY SEQUENCE

A power supply sequence is recommended for the AD4110-1, please see Table 6. After all power supplies are stable, a device reset is required. See the Resetting the AD4110-1 section.

PROTECTION DIODE

Applying a voltage to an HV pin that is more negative than the potential of the system negative power supply can only be accomplished by connecting an external diode from the VSS pin to the system negative power supply. A diode with a very low reverse leakage current should be considered. See Figure 29 for the connection diagram.

ANALOG INPUT

The AD4110-1 has one high voltage differential input, which can be configured to accept a voltage or current. When the input is a current, the internal resistor (R_{SENSE}) can be used to convert the current to a voltage. Alternatively, a high precision external resistor can be used.

PULL-UP/PULL-DOWN CURRENTS

Each AD4110-1 high voltage input pin can use a pull-up or pull-down current. These currents can have a value of 1 µA or 100 µA and are used to detect the presence of an open wire.

ANTIALIASING FILTER

The AD4110-1 input pins are linked to the inputs of the internal PGA by a nominal series resistance of 1.6 kΩ. Using external capacitors on the C(±) pins, a first-order antialiasing filter can be implemented. A 0.1 µF capacitor is recommended because the differential capacitor and 0.01 µF capacitors to ground provide a −3 dB cutoff frequency at approximately 500 Hz.

RTD EXCITATION CURRENTS

The AD4110-1 high voltage input can connect to 2-wire, 3-wire, and 4-wire RTD sensors. The device includes two matched excitation currents that can be programmed to 100 µA, 400 µA, 500 µA, or any combination of these values.

FIELD POWER SUPPLY MODE

The AD4110-1 provides an option to power an external current output sensor connected between the AIN(+) and AIN(−) terminals with up to 24 mA.

NO POWER SUPPLY MODE

When the AD4110-1 is configured to power up in current mode and there is no power supply connected to VDD/VSS, the AD4110-1 can power itself from the ±4 mA to ±20 mA loop with limited functionality. Both the current path through the loop and the loop overcurrent protection are maintained.

BIAS VOLTAGE GENERATOR

The AD4110-1 incorporates a bias voltage generator (VBIAS) that can be used to connect the AIN(−) pin to AGND. See Figure 34 for an equivalent circuit diagram. This feature is software selectable and is included for applications where the sensor output signal is floating.

PGA

The PGA removes potentially large common-mode signals and subsequently applies gain or attenuates the input signal to maximize the resolution of the conversions from the ADC.

CALIBRATION REGISTERS

The AD4110-1 provides gain calibration registers that contain gain correction coefficients for all 16 gain settings in voltage mode. For current mode, there is one gain calibration register containing the gain correction coefficient for a gain of 4.

SERIAL INTERFACE

The AD4110-1 has a 4-wire serial peripheral interface (SPI). The on-chip registers are accessed via the serial interface. Up to four devices can be connected on the same SPI bus. The AD4110-1 has two address pins (ADR0 and ADR1) to set the address of each device.

CLOCK

The AD4110-1 has two internal 8 MHz clocks. For specified performance, it is recommended that the AFE be driven with the ADC clock. The internal clock can be made available on the CLKIO pin and an external clock can be supplied to the CLKIO pin.

ADC

The output of the high voltage analog front end is applied to the ADC input multiplexer. The 24-bit ADC is fully buffered (analog inputs and reference inputs) with a maximum output data rate of 125 kSPS.

The Σ-Δ modulator output is digitally filtered. The AD4110-1 provides three separate types of digital filtering. The application selects one of these filter responses:

- Sinc5 + sinc1 averager for fast channel switching
- Sinc3 filter response to maximize rejection of interferers
- Enhanced filter set to maximize the simultaneous rejection of 50 Hz and 60 Hz while minimizing the settling time

ADC FILTER REGISTERS

The AD4110-1 provides four filter registers that allow different output data rates to be selected for the high voltage channel and the three low voltage channels. The filter registers share the same memory address. Therefore, when the filter register is written to, the contents are copied to the filter register for each channel enabled in the ADC_CONFIG register.

ADC GAIN AND OFFSET REGISTERS

The AD4110-1 provides four sets of gain and offset registers for each of the four channels, the high voltage channel and the three low voltage channels.

NOISE PERFORMANCE AND RESOLUTION

Figure 30 to Figure 33 show the typical rms noise and the noise free (peak-to-peak) resolution of the AD4110-1 for various output data rates and filter settings taken over 1000 samples. The values given are for the bipolar input range with an external 2.5 V reference. These typical values are generated with a differential input voltage of 0 V when the ADC is continuously converting.

Both inputs are shorted together at the device pins with VBIAS turned on. Note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

For more information about noise performance and resolution, see the Noise, Settling Time, and Digital Filtering section.

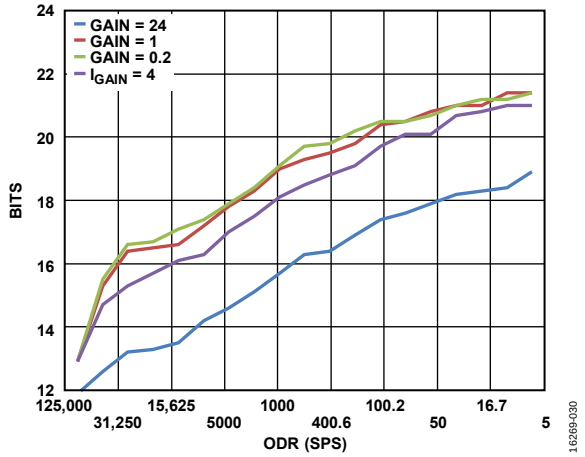


Figure 30. Noise Free Resolution for sinc3 Filter

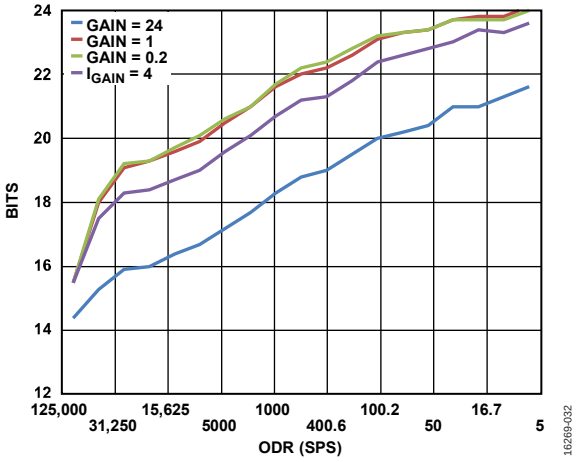


Figure 32. RMS Noise Resolution for sinc3 Filter

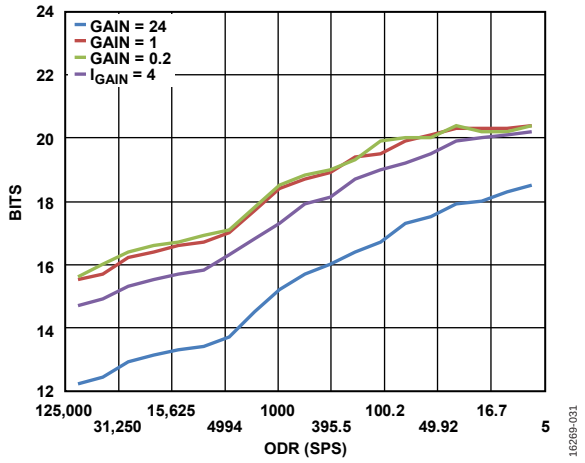


Figure 31. Noise Free Resolution for sinc5 + sinc1 Filter

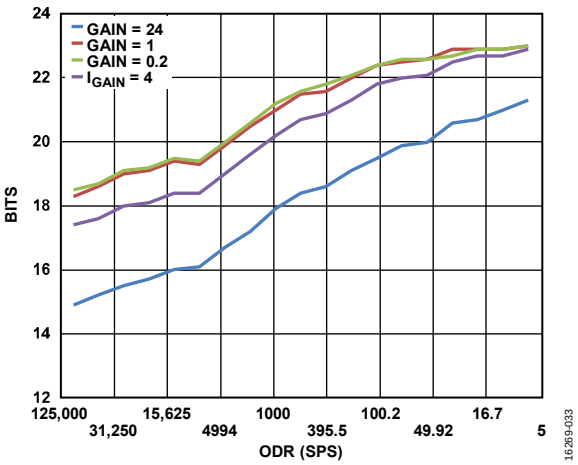


Figure 33. RMS Noise Resolution for sinc5 + sinc1 Filter

MODES OF OPERATION

DEFAULT MODE OF OPERATION ON POWER-UP

The input pins of the AD4110-1, AIN(+) and AIN(−), can be configured for voltage or current input. The factory default mode of operation for the AD4110-1 is current mode. On power-up, the device accepts an input current routing it through a low impedance sense resistor for measurement.

The default mode on power-up is also the mode of operation used in a no power supply mode condition (see the No Power Supply Mode section). The power-up mode for the high voltage channel can be programmed.

CHANGING THE DEFAULT MODE OF OPERATION FOR FUTURE POWER-UP CYCLES

The factory default mode of operation is stored in memory and can be reprogrammed by the application so that the device powers up the high voltage channel in either current mode or voltage mode after the next power cycle.

An advantage of setting the power-up default to current mode is when dealing with ±4 mA to ±20 mA current loops. If the AD4110-1 is connected to the ±4 mA to ±20 mA loop and a power supply failure to the AD4110-1 occurs, the current loop continuity and input protection are both maintained due to the unique design of the AD4110-1. Alternatively, the advantage of setting the power-up default to voltage mode is that the inputs operate as high impedance inputs.

To change the default mode of operation, take the following steps:

1. Set the IMODE bit (Bit 1) in the AFE_CNTRL2 register (Address 0x4). A value of 1 selects current mode; a value of 0 selects voltage mode (see Table 7 and Table 29).
2. Write the value 0x00B1 to the NO_PWR_DEFAULT_SEL register (Address 0xE, see Table 8).
3. Issue the refresh command (0x00A1) immediately to the NO_PWR_DEFAULT_SEL register to ensure that the new count value is loaded correctly.

Table 7 and Table 8 show the bit descriptions of the registers required to change the default mode of operation on power-up. Additionally this power-up default mode is the mode of operation that the device reverts to if the power supply to AD4110-1 is disconnected for some reason.

The application can read the programmed default mode of operation from the NO_PWR_DEFAULT_STATUS register. An even value in this register means that the default power-up mode is voltage mode, and an odd value in this register means that the default power-up mode is current mode.

The default mode of operation can be changed only 100 times. Bits[7:0] in the NO_PWR_DEFAULT_STATUS register contain the number of remaining changes allowed to the default mode of operation.

POWER SUPPLY REQUIREMENTS

Any one of the following power supply sequences are recommended (see Table 6). After all power supplies are stable, a device reset is required (see the Resetting the AD4110-1 section).

Table 6. Power Supply Sequence

Sequence	1st	2nd	3rd	4th
1	VSS	VDD	AVDD5	IOVDD
2	VDD	VSS	AVDD5	IOVDD
3	VDD	AVDD5	VSS	IOVDD
4	VDD	AVDD5	IOVDD	VSS

SYSTEM CLOCK REQUIREMENTS

The AD4110-1 has two internal 8 MHz clocks. For specified performance, it is recommended that the AFE be driven with the ADC clock. By default on power-up, the AFE and the ADC run on their own internal clocks; therefore, it is necessary for the application software to reconfigure the ADC clock to be output to the CLKIO pin and to reconfigure the AFE clock to use the CLKIO pin as its source (see Table 28 and Table 39).

- Set Bits[3:2] = 01 in the ADC_MODE register.
- Set Bits[4:3] = 10 in the AFE_CLK_CTRL register.

When an external clock source is used, it is necessary to reconfigure the ADC clock to use the CLKIO pin as its source.

- Set Bits[3:2] = 10 in the ADC_MODE register.

Table 7. Bit Descriptions for the AFE_CNTRL2 Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x4	AFE_CNTRL2	[15:8]	AINN_DN100	AINN_DN1	AINN_UP100	AINN_UP1	AINP_DN100	AINP_DN1	AINP_UP100	AINP_UP1
		[7:0]	VBIAS		Reserved		EN_FLD_PWR	EXT_R_SEL	IMODE	Reserved

Table 8. Bit Descriptions for the NO_PWR_DEFAULT_SEL and NO_PWR_DEFAULT_STATUS Registers

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0xE	NO_PWR_DEFAULT_SEL	[15:8]	Reserved							
		[7:0]	D_MODE							
0xF	NO_PWR_DEFAULT_STATUS	[15:8]	Reserved							COMM_ERR
		[7:0]	Count							

BIPOLAR AND UNIPOLAR OUTPUT

The AD4110-1 accepts fully differential, pseudo differential and single-ended input signals. The ADC_CONFIG register allows the application to select the output coding of the ADC by selecting between bipolar and unipolar. The default output mode is bipolar (see Table 41).

The voltage seen at the ADC inputs is,

$$(AIN(+) - AIN(-)) \times PGA\ Gain$$

In bipolar mode, the ADC accepts both positive and negative differential input voltages. The output coding is offset binary and the LSB size is,

$$LSB = ((2 \times V_{REF}) \div 2^{24}) \div PGA\ Gain$$

In unipolar mode, the ADC accepts only positive differential voltages. The coding is straight binary and the LSB size is,

$$LSB = (V_{REF} \div 2^{24}) \div PGA\ Gain$$

Before using unipolar mode, consider that a negative ADC differential input voltage can result due to a negative PGA input offset voltage, and is converted by the ADC as 0 V.

AUXILIARY LOW VOLTAGE INPUTS

The AD4110-1 has three auxiliary low voltage input channels available to the application. These low voltage channels connect directly to the ADC input multiplexer and can be selected as part of a conversion sequence with the main high voltage channel (Channel 0).

- Channel 1: AIN1(LV) – AIN2(LV)
- Channel 2: AIN1(LV) – AINCOM(LV)
- Channel 3: AIN2(LV) – AINCOM(LV)

By default, these auxiliary channels are disabled. To enable the auxiliary channels, set Bits[3:1] of the ADC_CONFIG register (see Table 41). A set of gain, offset, and filter registers is available for each channel. These registers can be programmed separately from the registers for the main high voltage channel.

DIGITAL FILTER

Four digital filter registers on the AD4110-1 allow different output data rates to be selected for the high voltage channel and the three low voltage channels (see Table 43). The filter registers share the same memory address, therefore, when the filter register is written to, the contents are copied to the filter register for each channel enabled in the ADC_CONFIG register.

CONTINUOUS CONVERSION MODE

Continuous conversion mode on the high voltage channel is the default mode of operation for the ADC after power-up.

The AD4110-1 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the DOUT/$\overline{RDY}$ line also goes low when a conversion is complete. To read a conversion, the user writes to the communications register indicating that the next operation is a read of the data register. When the data-word has been read from the data register, DOUT/$\overline{RDY}$ goes high. The application can read the data register additional times, if required. However, the user must ensure that the data register is not being accessed at the completion of the next conversion; otherwise, the new conversion word is lost.

Because he ADC conversion control logic and the SPI interface are not synchronized, take care when reading the ADC result register after $\overline{CS}$ is brought low (see the DOUT/$\overline{RDY}$ pin description in the Serial Peripheral Interface section for further details).

INPUT AUTO SEQUENCING

When more than one channel is enabled, the ADC automatically sequences through each channel and generate a conversion result. When all channels have been converted, the sequence starts again with the first channel. The channels are converted in order from lowest enabled channel to highest enabled channel. The data register is updated as soon as each conversion is available. The DOUT/$\overline{RDY}$pin pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

The ADC data register conversion result contains no channel identification. Therefore, when more than one channel is enabled, it is necessary to append the contents of the ADC status register to the ADC data register. This is configured by setting Bit 6 of the ADC_INTERFACE register (see Table 9 and Table 40).

A filter settling time is associated with switching channels. Therefore, the output data rate of the AD4110-1 is reduced, depending on the number of channels selected. See Table 16 to Table 21 for the channel filter settling time and switching rates.

Because the input channels are multiplexed, an input settling time can be required before the ADC starts the conversion process. The AD4110-1 provides an ADC conversion delay feature, see the ADC Conversion Delay section.

Table 9. Bit Descriptions for the ADC_INTERFACE Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x2	ADC_INTERFACE	[15:8]	Reserved							
		[7:0]	Reserved	DATA_STAT	Reserved		CRC_EN		Reserved	WL16

SINGLE CONVERSION MODE

In single conversion mode, the AD4110-1 performs a single conversion, and is then placed in standby mode after the conversion is complete. DOUT/$\overline{\text{RDY}}$ goes low to indicate the completion of a conversion. When the data-word has been read from the data register, DOUT/$\overline{\text{RDY}}$ goes high. The data register can be read several times, if required, even when DOUT/$\overline{\text{RDY}}$ has gone high.

To enable single conversion mode, set the MODE bits of the ADC_MODE register to 001, see Table 10 and Table 39 for details of the MODE bits

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion is started, DOUT/$\overline{\text{RDY}}$ goes high and remains high until a valid conversion is available and $\overline{\text{CS}}$ is low. When the conversion is available, DOUT/$\overline{\text{RDY}}$ goes low. The ADC then selects the next channel and begins a conversion. The application can read the present conversion while the next conversion is being performed. When the next conversion is complete, the data register is updated. Therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to standby mode.

ADC CONVERSION DELAY

When the AFE configuration is changed or more than one channel is enabled and the ADC is programmed to automatically sequence through each channel, an input signal settling time can be required before the ADC starts the conversion process. The AD4110-1 provides the capability to program a conversion delay from 8 µs to 2 ms (see Table 39 for programming options).

For output data rates of 10.39 kSPS or less, the delay allows the data rate of the ADC to remain at the required update rate with only a minor impact on the resolution of the conversion result. The delay is effectively absorbed by the filter by reducing the amount of averaging performed. The correct delay selection vs. the output data rate minimizes any effect on resolution. This delay can only be absorbed when the requested delay is less than half the original settling time. For output data rates of greater than 10.39 kSPS, the delay time is added to the overall conversion time.

This delay function is not valid when using the sinc3 filter or when rejecting 16.7 Hz, 50 Hz, 60 Hz, and 400 Hz interferers.

BIAS VOLTAGE GENERATOR

The AD4110-1 incorporates a bias voltage generator (VBIAS) that can be used to connect the AIN(−) pin to AGND. This feature is software selectable and is included for applications where the sensor output signal is floating.

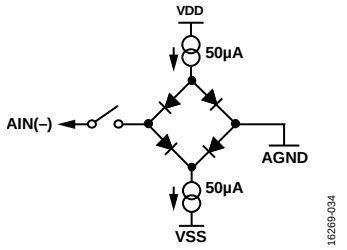


Figure 34. VBIAS Equivalent Circuit Diagram

The VBIAS generator acts as a 0 V voltage source with respect to AGND, see Figure 34 for the equivalent circuit diagram. It can source or sink up to a maximum of 50 µA from the sensor device connected to the AIN(+) and AIN(−) pins.

If a sensor output connected to the input of the AD4110-1 is floating, the VBIAS function is used to bias the sensor output so that the sensor and AD4110-1 measuring system share the same ground. A typical example of a sensor that has a floating output is a thermocouple (see Figure 35).

The VBIAS function is controlled by Bits[7:6] in the AFE_CNTRL2 register (see Table 7 and Table 29). By default, the VBIAS function is disabled.

Table 10. Bit Descriptions for the ADC_MODE Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1	ADC_MODE	[15:8]	REF_EN	Reserved				DELAY		
		[7:0]	Reserved	MODE			CLK_SEL		Reserved	

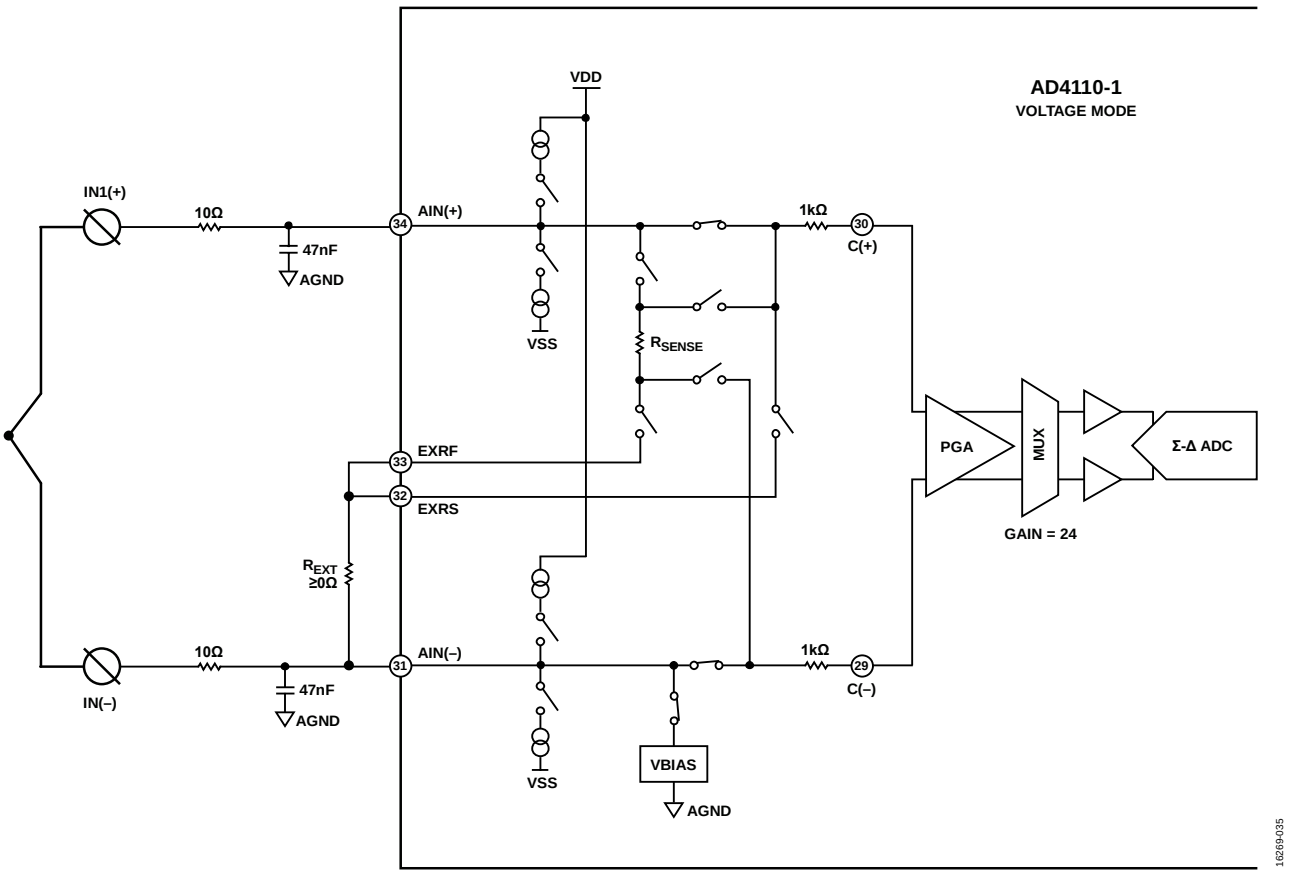


Figure 35. Thermocouple Connections

ANTIALIASING FILTER CIRCUIT

A general-purpose approach to antialiasing filtering for device level applications using amplifiers is shown in Figure 36.

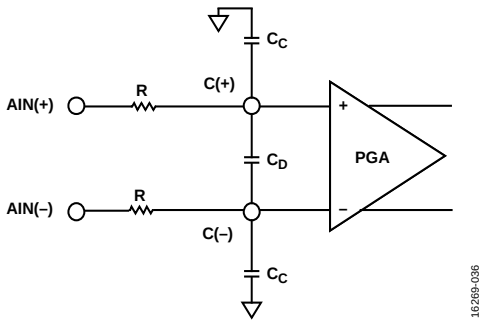


Figure 36. Antialiasing Filter, C_C and C_D are External Components

On the AD4110-1, the AIN(+) and AIN(−) input pins are linked to the inputs of the internal PGA by a nominal series resistance of 1.6 kΩ. Using external capacitors, a first-order antialiasing filter can be implemented by connecting capacitors to the C(+) and C(−) pins.

In this type of filter, choose C_D to be at least ten times larger than C_C to suppress spurious differential signals due to common-mode to differential mode conversion. These spurious signals can occur due to the mismatch between the two time constants (RC_C). For further information on filtering techniques, see the MT-070 Tutorial.

The low pass filter corner frequency for common mode signals (Filter Frequency$_{CM}$) is calculated using the following equation:

$$Filter\ Frequency_{CM} = \frac{1}{2\pi RC_C}$$

The low pass filter corner frequency for differential mode signals (Filter Frequency$_{DIFF}$) is calculated using the following equation:

$$Filter\ Frequency_{DIFF} = \frac{1}{2\pi R\left(2C_D + C_C\right)}$$

where $C_D \geq 10\ C_C$ is recommended.

The calculation is as follows:

R = 1.6 kΩ
C_C = 0.01 µF
C_D = 0.1 µF
Filter Frequency$_{DIFF} \approx$ 500 Hz

CURRENT MODE

Current mode is selected by setting the IMODE bit to 1 in the AFE_CNTRL2 register (see Table 7 and Table 29).

The analog inputs of the AD4110-1, AIN(+) and AIN(−), can interface directly to standard industrial analog sensors operating as current loops with 0 mA to +20 mA, ±4 mA to ±20 mA, or ±20 mA output.

The current loop of the transmitter module terminals is connected directly to the differential analog inputs of the AD4110-1. The loop current flows through the internal switches, through the internal sense resistor, R_{SENSE}, and then through the external sense resistor, R_{EXT}, as shown in Figure 37.

The voltage drop across R_{SENSE}, which is proportional to the input current, is then filtered by an analog RC filter. The AIN(+) and AIN(−) input pins are linked to the inputs of the internal PGA by a nominal series resistance of 1.6 kΩ. Using external capacitors, a first-order antialiasing filter can be implemented by connecting capacitors to the C(+) and C(−) pins. A 0.1 µF capacitor is recommended as the differential capacitor, and 0.01 µF capacitors to ground give a −3 dB cutoff frequency at approximately 500 Hz (see the Antialiasing Filter section).

The resulting voltage is amplified by the on-chip PGA, and the analog output of the PGA is then routed to the buffered input of the ADC through a multiplexer. Set the gain of the PGA so that the PGA output voltage is within ±2.5 V to maximize the resolution of the 24-bit Σ-Δ ADC.

When using the internal R_{SENSE} resistor, the path from the EXRF pin to the AIN(−) pin must be connected. This connection can be implemented by shorting these pins externally or by populating the resistor R_{EXT} as a 0 Ω link.

The current flowing through the R_{SENSE} resistor is continuously monitored by the AD4110-1. If the current reaches the specified limit, the overcurrent flag (AIN_OC) is set in the AFE_DETAIL_STATUS register (see Table 32).

The AD4110-1 has built in self protection circuitry that limits the maximum current flowing through the device.

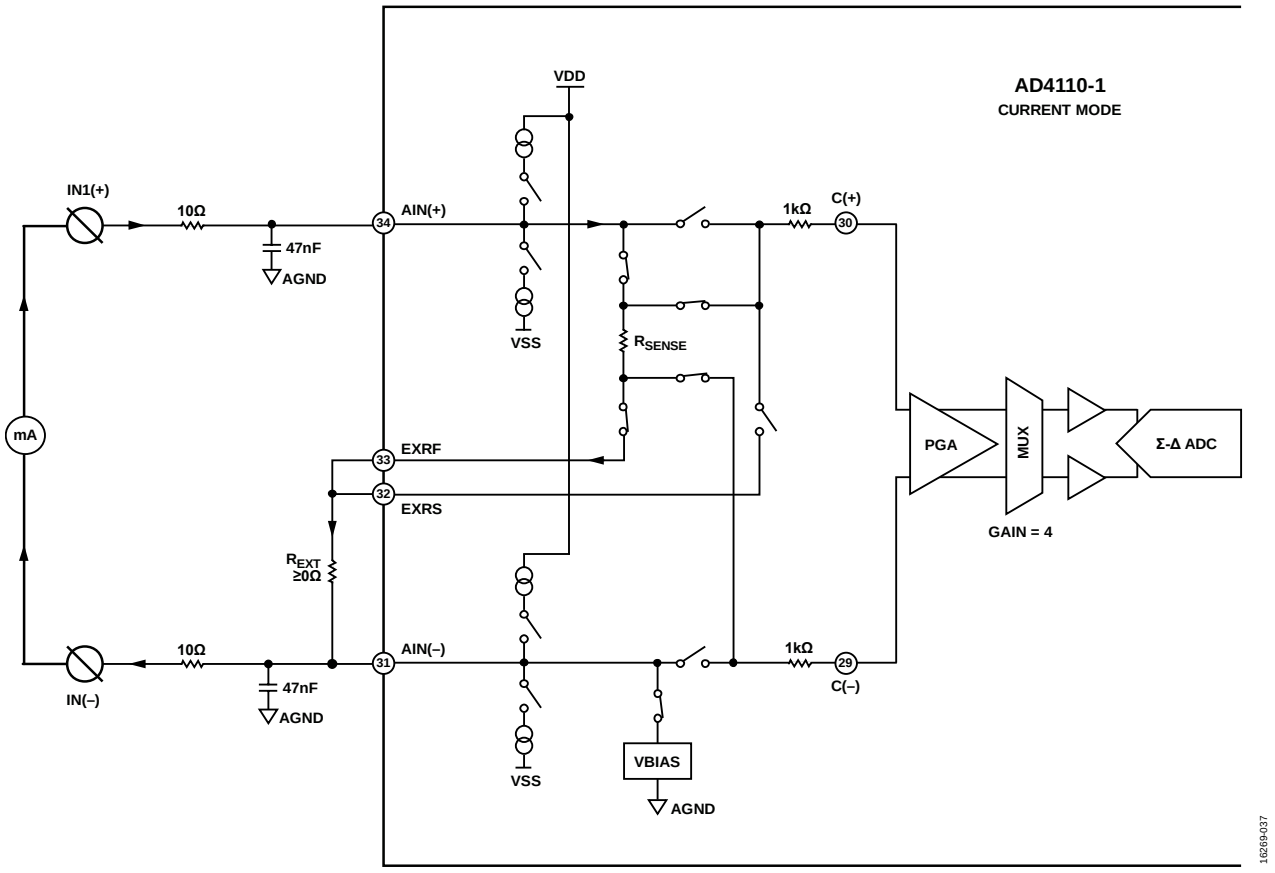


Figure 37. Current Input Mode, Internal Sense Resistor, Gain = 4

Transimpedance Gain

When using the internal sense resistor, the transimpedance gain is set by the resistance value of the internal R_{SENSE} resistor and the gain selected for the PGA.

The internal R_{SENSE} resistor is typically 24 Ω. The current input mode specifications of the AD4110-1 are specified for a gain of 4 only. Multiplying the gain of 4 by R_{SENSE} = 24 Ω gives a value of 96 Ω, which means that for each milliamp applied to R_{SENSE}, the output of the PGA equals 96 mV.

Figure 38 shows the scaling from the output of the PGA to the ADC and the output range of the ADC codes with a ±20 mA input and the internal R_{SENSE} selected with a gain of 4.

For specified performance as shown in Table 1, the input range is ±20 mA and the functional range is ±24 mA.

Using an External Sense Resistor

If a specific current sense resistor is required, the AD4110-1 allows an external resistor to be connected to the device (see Figure 39). When changing from the internal 25 Ω sense resistor to an external sense resistor of a higher value, note the increase in common mode voltage such that the absolute input voltage as specified in Table 1 is not exceeded. To configure the device to use an external resistor, set the EXT_R_SEL bit in the AFE_CNTRL2 register.

The loop current continues to flow through the internal R_{SENSE} resistor so that the overcurrent detection flag and the current limit circuitry operate in the same way as when the internal sense resistor is used. Only the voltage generated across the external sense resistor is amplified by the PGA.

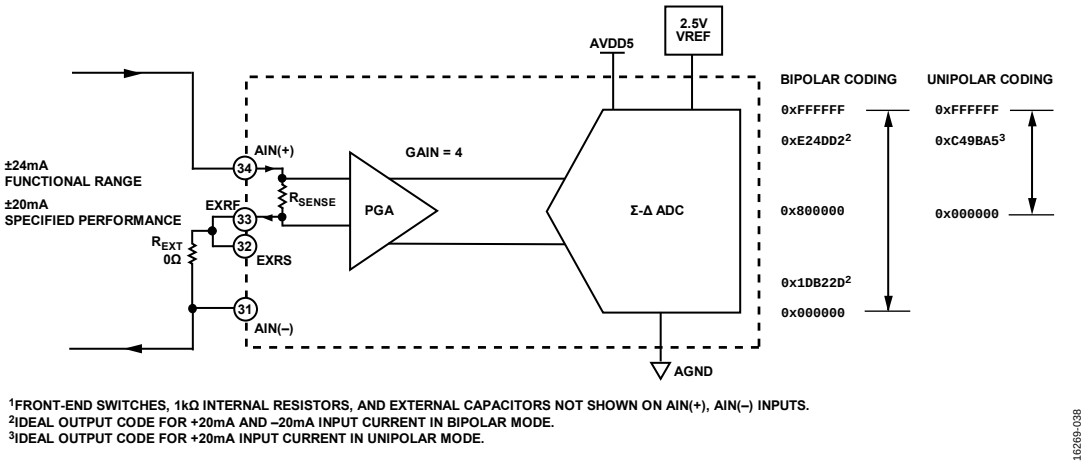


Figure 38. Current Input Mode Scaling, R_{SENSE} Resistor, Gain = 4

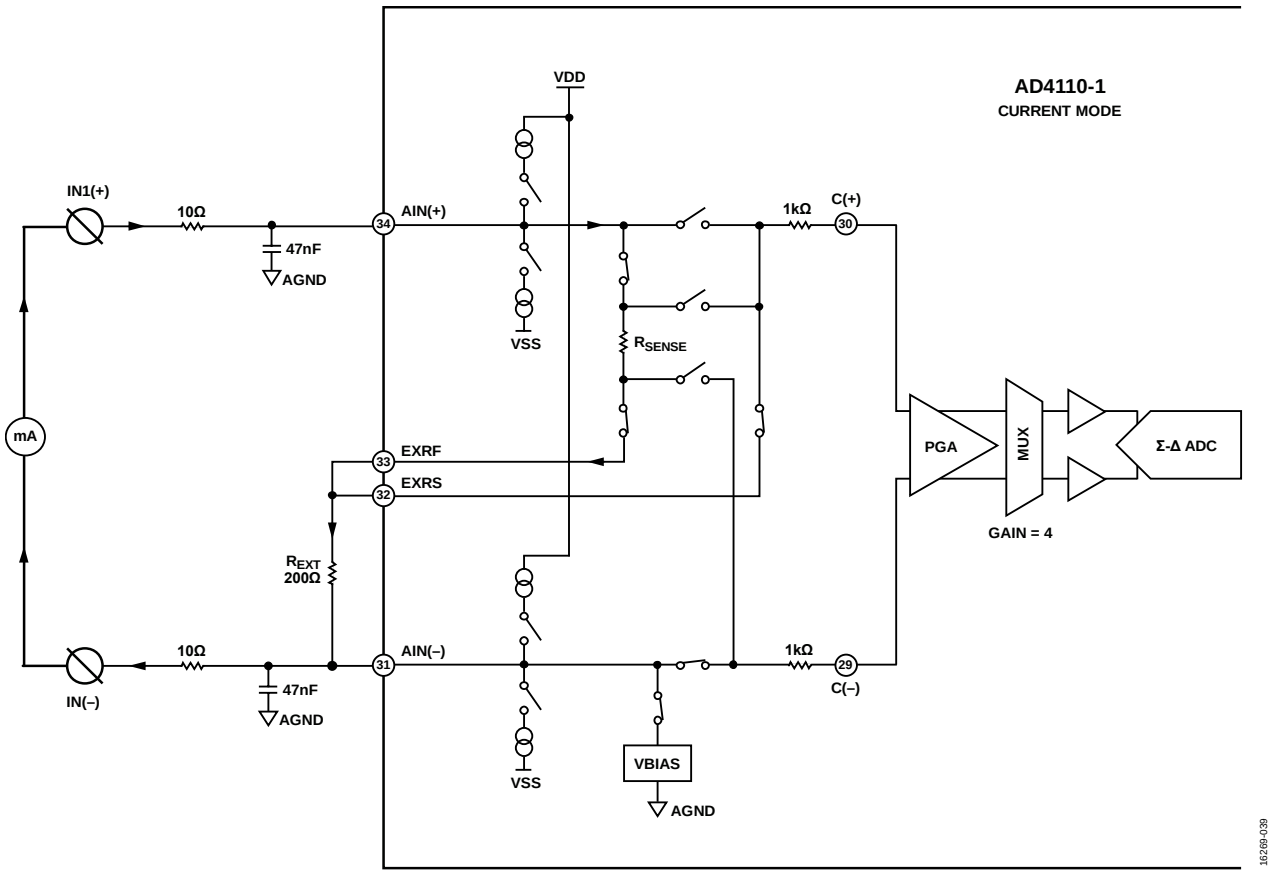


Figure 39. Current Input Mode, R_{EXT} Resistor

VOLTAGE AND THERMOCOUPLE MODE

The factory default mode of operation for the AD4110-1 is current mode. Voltage mode is selected by clearing the IMODE bit in the AFE_CNTRL2 register (see Table 7 and Table 29).

After a power cycle, the AD4110-1 reverts to current mode unless the default mode of operation is changed as described in the Default Mode of Operation on Power-Up section.

Figure 40 shows the architecture of the internal switches of the AD4110-1 when the device is configured for voltage input mode. The AD4110-1 converts the difference in voltage between the analog input pins, AIN(+) and AIN(−).

The AIN(+) and AIN(−) input pins are linked to the inputs of the internal PGA by a nominal series resistance of 1.6 kΩ. Using external capacitors, a first-order antialiasing filter can be implemented by connecting capacitors to the C(+) and C(−) pins.

A 0.1 µF capacitor is recommended as the differential capacitor, and 0.01 µF capacitors to ground give a −3 dB cutoff frequency at approximately 500 Hz (see the Antialiasing Filter section).

A total of 16 gain settings are available on the AD4110-1 in the range of 0.2 to 24. These gain settings allow for an input voltage range from ±12.5 V to ±0.104 V. Therefore, the analog inputs can connect directly to standard industrial voltage output sensors with a unipolar or bipolar output topology. Note that for specified performance, the input voltage range must be restricted to that as specified in Table 1.

To program the gain, set the GAIN_CH bits in the PGA_RTD_CTRL register (Address 0x5). For more information, see the PGA_RTD_CTRL Register section.

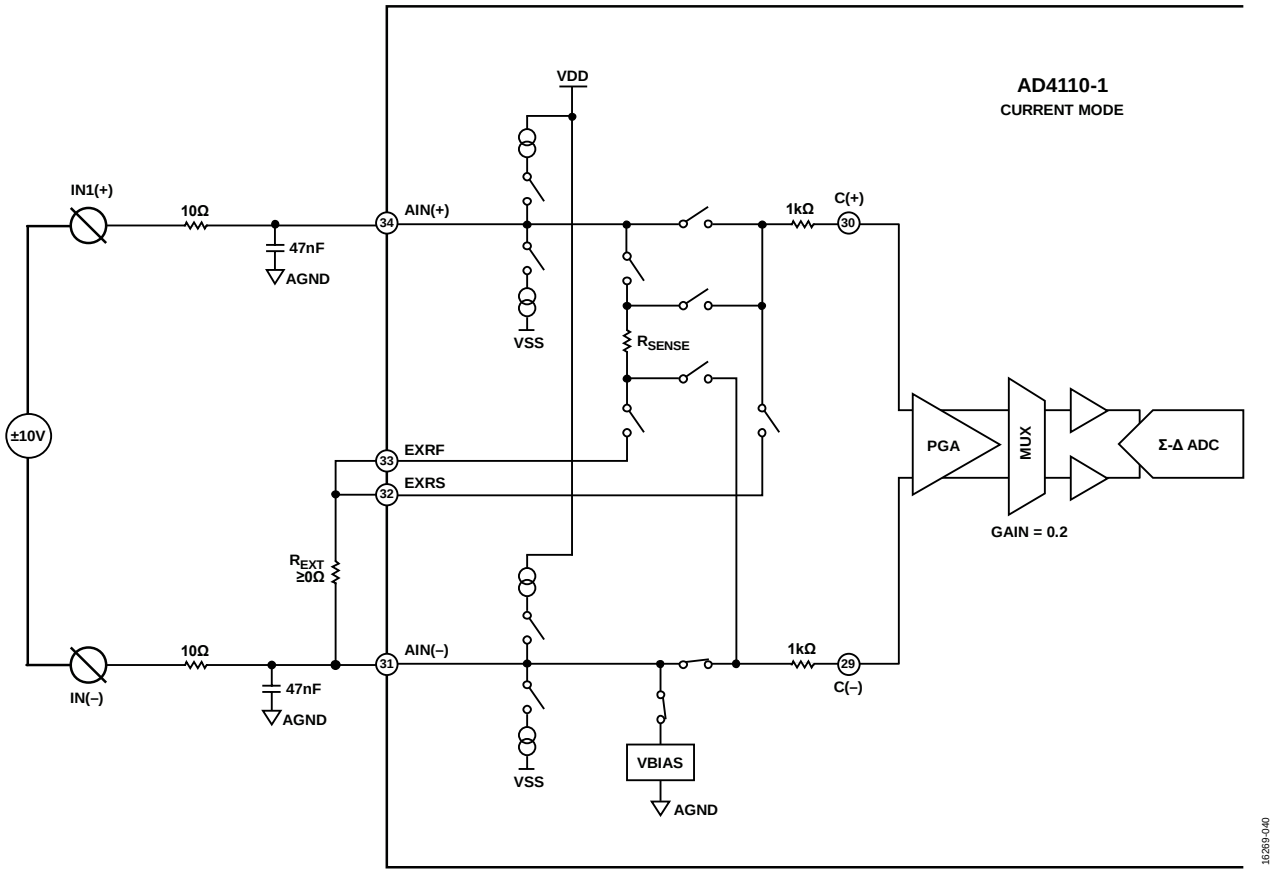


Figure 40. Voltage Input Mode

Input Scaling for Voltage Mode

Figure 41 shows the scaling of the voltage mode. The output of the front-end PGA is routed to the buffered input of the ADC through a multiplexer. To maximize the resolution of the 24-bit Σ-Δ ADC, the gain or attenuation of the PGA is selected so that the analog output voltage is within the range of ±2.5 V. Figure 41 shows the maximum input of ±12.5 V, which can be converted when the gain of 0.2 is selected. For specified performance as shown in Table 1, the input range is ±10 V and the functional range is ±12.5 V.

If an overvoltage or undervoltage condition occurs on the AIN(+) or AIN(−) input, the corresponding error flag is set in the AFE_DETAIL_STATUS register. For more information, see the Overvoltage and Undervoltage Detection section.

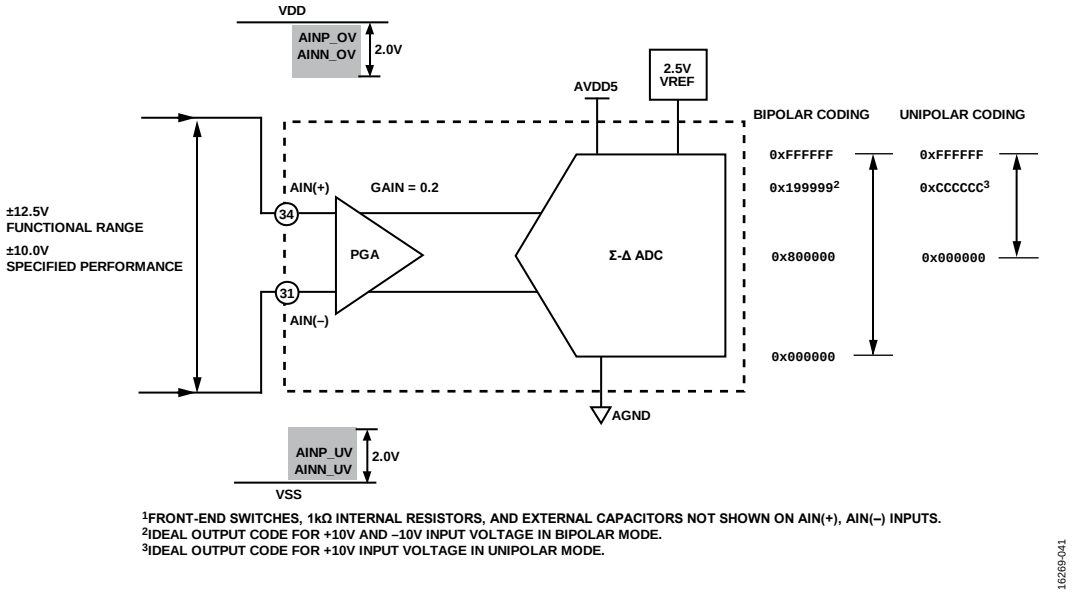


Figure 41. Voltage Input Mode Scaling

Thermocouple Inputs

The analog inputs of the AD4110-1, AIN(+) and AIN(−), can directly interface to standard industrial thermocouples. The voltage mode of operation is used when connecting to thermocouples.

Figure 42 shows the architecture of the internal switches of the AD4110-1 when the device is configured for a thermocouple input. The thermocouple terminals are connected directly to the differential input pins of the AD4110-1, AIN(+) and AIN(−).

The AIN(+) and AIN(−)input pins are linked to the inputs of the internal PGA by a nominal series resistance of 1.6 kΩ. Using external capacitors, a first-order antialiasing filter can be implemented by connecting capacitors to the C(+) and C(−) pins. A 0.1 µF capacitor is recommended as the differential capacitor, and 0.01 µF capacitors to ground give a −3 dB cutoff frequency at approximately 500 Hz (see the Antialiasing Filter section).

In most cases, a thermocouple is not referenced to or biased toward any system power supply voltage. Therefore, the VBIAS function must be used when connecting a thermocouple to the AD4110-1. Enabling VBIAS effectively grounds the AIN(−) side of the thermocouple to the ground of the AD4110-1 power supply. For more information, see the section.

Select the gain of the PGA so that the output voltage of the PGA as seen by the ADC is as close to ±2.5 V as possible. Using the gain of 24, which is the maximum gain of the PGA, allows for an input range of ±0.104166 V at the inputs of the AD4110-1.

When measuring temperature with a thermocouple, cold junction compensation must be incorporated. The AD4110-1 includes three low voltage channels that can be used for this purpose: AIN1(LV), AIN2(LV), and AINCOM(LV).

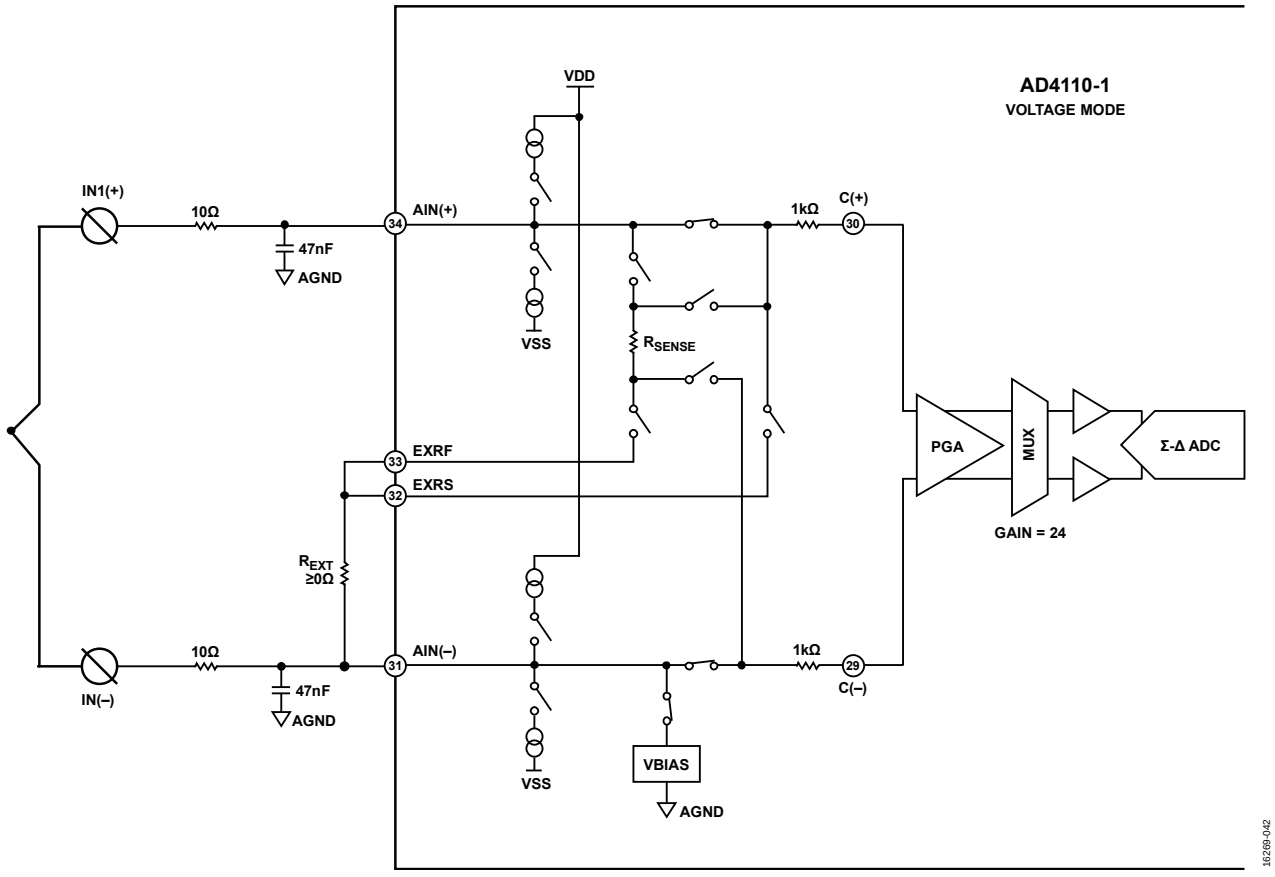


Figure 42. Thermocouple Connections

RTD MODE

The AD4110-1 includes on-chip functions that support applications where RTD sensors are required. The voltage mode of operation is used when connecting the device to RTD sensors.

The AD4110-1 provides a range of matched precision excitation currents on the AIN(+) and AIN(−) pins for 3-wire RTD measurements. For 4-wire RTD measurements, the precision excitation current is switched from the AIN(+) pin to the RTD pin. Six programmable current levels are available; 100µA, 400 µA, 500 µA, 600 µA, 900 µA and 1000 µA.

The RTD measurement mode (2-wire, 3-wire, or 4-wire) and the magnitude of the excitation currents are programmed using the PGA_RTD_CTRL register (see Table 11 and Table 30).

The RTD excitation currents are generated by routing the reference input across an internal, precision, thin film resistor of 25 kΩ. In this way, the RTD currents are always ratiometric to the reference voltage applied to the AD4110-1. Alternatively, an external, high precision, 25 kΩ resistor can be used when the application requires a lower drift resistor specification (see the Generating RTD Currents with an External Resistor section).

The typical configuration when using the RTD functionality is to supply the REFIN(+) and REFIN(−) pins of the AD4110-1 from an external precision 2.5 V reference, such as the ADR4525.

Generating RTD Currents with an External Resistor

The AD4110-1 also allows the application to generate RTD excitation currents with a reduced drift, external precision 25 kΩ resistor. By default, the internal resistor is used to generate the RTD currents. If an external resistor is required, set the EXT_RTD_RES bit in the PGA_RTD_CTRL register (see Table 11 and Table 30).

When the AD4110-1 is used in RTD mode with an external resistor, the PCB layout must include a star point connection of the iREFS and iREFF pins to one side of the external precision resistor (see Figure 43). Connect the ground side of the resistor as close as possible to the ground of the external reference and to the ground connection at the REFIN(−) pin. Minimize the pin capacitance by placing the precision resistor as close as possible to the iREFS and iREFF pins.

In applications where the RTD function is not required, it is recommended that a non-precision, 25 kΩ ± 15% resistor be connected in the same way as shown in Figure 43.

The RTD excitation currents (I_{EXC}) are derived from a reference current, which is generated by forcing an external reference voltage (V_{REF}) across an external reference resistor (R_{REF}) by means of an amplifier. The reference current, (nominally 100 µA), is mirrored and multiplied (Ratio) to make up the individual current sources.

The nominal value of the RTD excitation current using an external resistor is:

$$I_{EXC}\,(nominal) = (V_{REF}/R_{REF}) \times Ratio$$

where *Ratio* = {1, 4, 5, 6, 9, 10}.

An error band of ± 0.3% (typical) must be applied to the I_{EXC} (nominal) to account for an error made up of the internal amplifier offset error and the ratio error.

The worst case RTD excitation current temperature drift can be approximated to:

$$TC(I_{EXC}) = TC(I_{RTD}) + TC(V_{REF}) + TC(R_{REF})$$

where *TC* is typically specified in ppm/°C.

Table 1 specifies TC(I_{RTD}). Refer to the relevant data sheets for the temperature coefficients of the voltage reference and the reference resistor used.

Table 11. Bit Descriptions for the PGA_RTD_CTRL Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x5	PGA_RTD_CNTRL	[15:8]	RTD_3W4W	I_COM_SEL			I_EXC_SEL			EXT_RTD_RES
		[7:0]	GAIN_CH				Reserved			

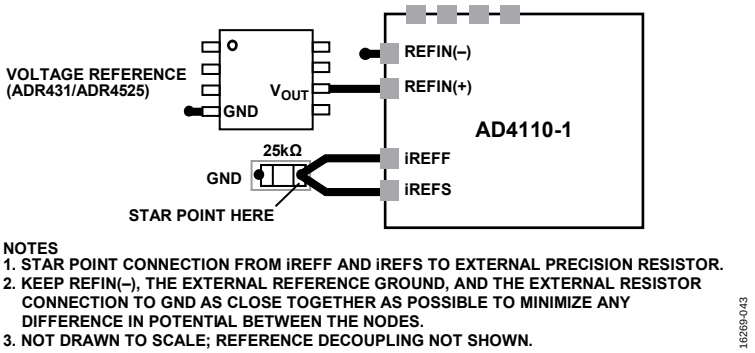


Figure 43. Connecting an External Reference Resistor to Generate RTD Excitation Currents

Excitation Currents

The AD4110-1 provides two precision current sources for use with RTD sensors. The RTD function is enabled by default and can be disabled by setting the DISRTD bit in the AFE_CNTRL1 register (see Table 12 and Table 27).

By default, the AD4110-1 is configured to operate in 4-wire RTD mode, see Figure 46 for the connection diagram. If 3-wire or 2-wire RTD mode is required, set the RTD_3W4W bit in the PGA_RTD_CTRL register (see Table 11 and Table 30).

In 3-wire RTD mode, two current sources are required and are available on the AIN(+) and AIN(−) pins. The RTD excitation current is available on the AIN(+) pin, and the RTD compensation current is available on the AIN(−) pin. See Figure 47 for the connection diagram.

The levels for the excitation and compensation currents are set to zero by default and are programmed by the I_EXC_SEL and I_COM_SEL bits of the PGA_RTD_CTRL register (see Table 11). Six programmable current levels from 100 µA to 1 mA are available (see Table 30). For proper 3-wire RTD measurements, program the excitation current and the compensation current to the same level.

By default, the AD4110-1 is configured to operate in 4-wire RTD mode (the RTD_3W4W bit in the PGA_RTD_CTRL register is cleared to 0).

In 4-wire RTD mode, only the excitation current is required and this current is available on the RTD pin (see Figure 46 for the connection diagram). When using 4-wire mode, the level of the compensation current must be disabled.

An external 2.5 V reference (for example, the ADR4525) is required when the excitation currents are used. The external reference is connected to the REFIN(+) and REFIN(−) pins and is used to generate the excitation currents (see the RTD Mode section). The AD4110-1 ADC should also use this reference when converting the RTD signals. Therefore, the absolute accuracy and temperature drift of the voltage reference do not directly affect the accuracy of the measured resistance.

Note that the voltage mode input offset specification as shown in Table 1 is specified for voltage mode only. RTD currents may cause an additional input offset voltage (±V) due to an I × R error voltage caused by a mismatch in IC or PCB trace resistance.

RTD Initial Drift

When either or both of the RTD excitation and compensation currents are set and enabled, the output current increases over time, as shown in Figure 44 and Figure 45. This initial drift resets when the current level is changed to another value or disabled and reenabled.

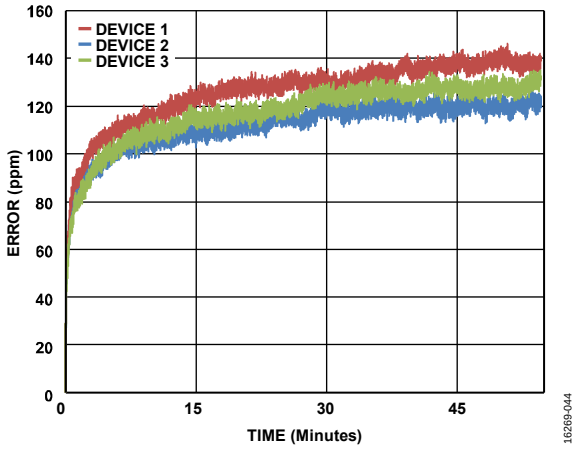


Figure 44. RTD Current, Initial Long Term Drift

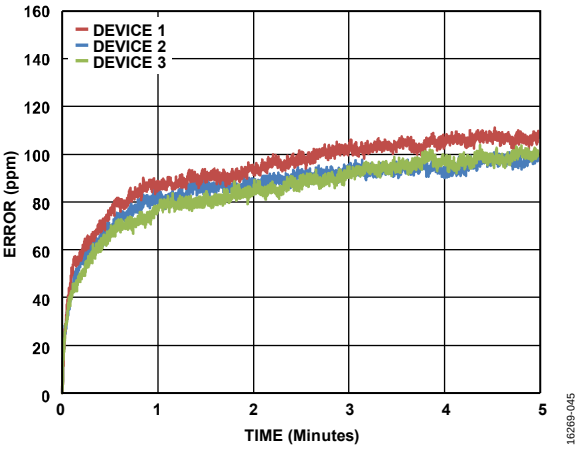


Figure 45. RTD Current, Initial Short Term Drift

4-Wire RTD

Figure 46 shows the connection diagram for a 4-wire sensor. Configure the AD4110-1 to operate in voltage mode by clearing the IMODE bit in the AFE_CNTRL2 register (see Table 7).

The AD4110-1 provides a programmable precision current source on the high voltage channel for use with a 4-wire RTD sensor. By default, the AD4110-1 is configured to operate in 4-wire RTD mode (the RTD_3W4W bit in the PGA_ RTD_CTRL register is cleared to 0; see Table 11and Table 30).

In 4-wire mode, a single excitation current is required; this current is available on the RTD pin. Six programmable current levels from 100 μA to 1 mA are available, see Table 30. When using 4-wire mode, set the level of the compensation current must be disabled.

The excitation current flows through the RL1 and RL4 lead resistances only (see Figure 46). Ideally, no current flows through RL2 and RL3. The voltage generated across the RTD sensor corresponds to the voltage sensed between AIN(+) and AIN(−).

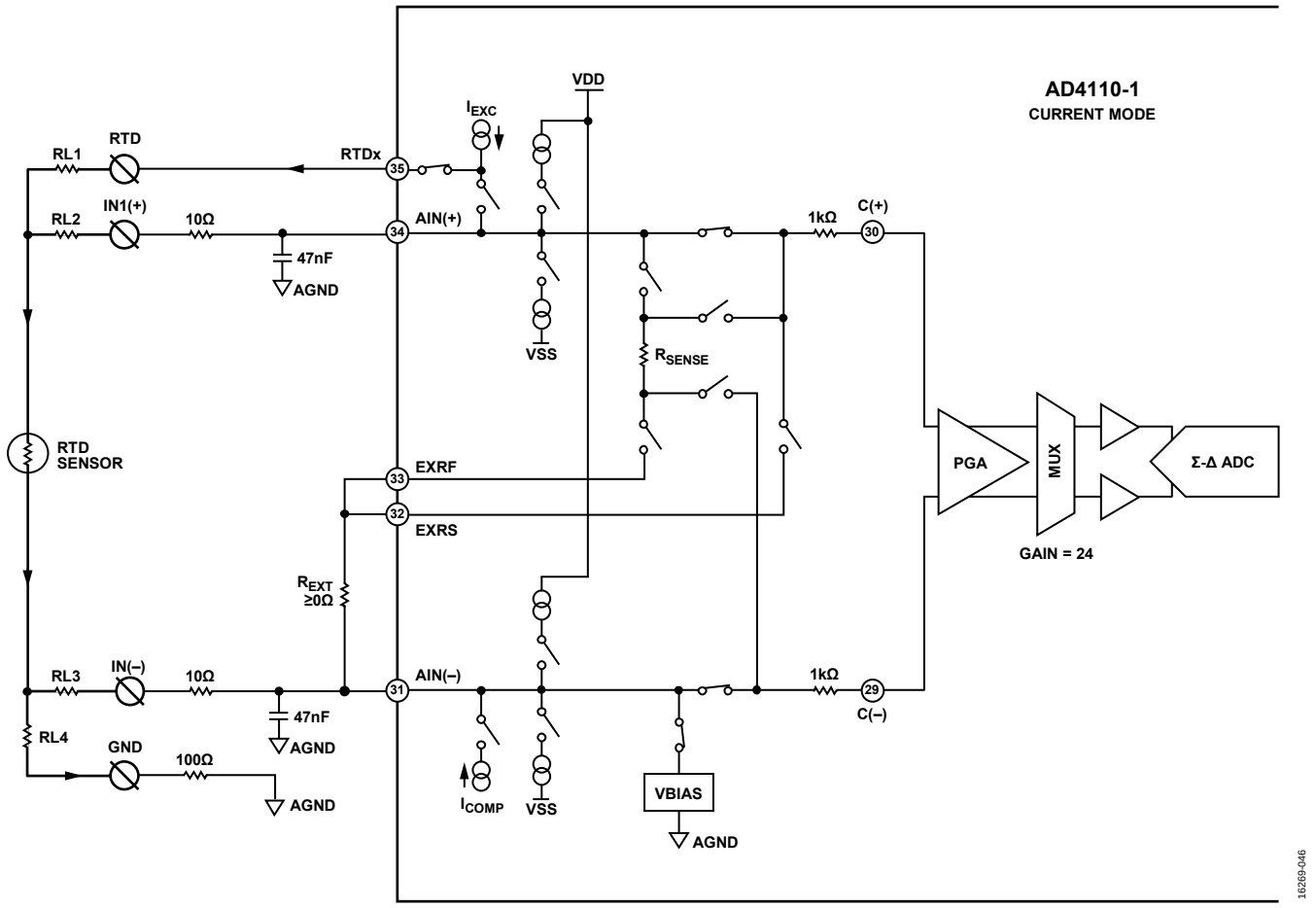


Figure 46. 4-Wire RTD

Table 12. Bit Descriptions for the AFE_CNTRL1 Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x1	AFE_CNTRL1	[15:8]	Reserved	CRC_EN		Reserved			DISRTD	Reserved
		[7:0]	Reserved							

3-Wire RTD

Figure 47 shows the connection diagram for a 3-wire sensor. Configure the AD4110-1 to operate in voltage mode by clearing the IMODE bit in the AFE_CNTRL2 register (see Table 7).

The AD4110-1 provides two precision current sources on the high voltage channel for use with 3-wire RTD sensors. By default, the AD4110-1 is configured to operate in 4-wire RTD mode. If 3-wire RTD mode is required, set the RTD_3W4W bit in the PGA_RTD_CTRL register (see Table 11 and Table 30).

The RTD excitation current is available on the AIN(+) pin, and the RTD compensation current is available on the AIN(−) pin. Six programmable current levels from 100 µA to 1 mA are available, see Table 30. For correct 3-wire RTD measurement, program the excitation current and the compensation current to the same level.

The excitation current flows through the RL1 and RL3 lead resistances (see Figure 47). The compensation current flows through the RL2 and RL3 lead resistances.

Because the lead resistances are similar (the leads are normally of the same material and the same length) and the excitation currents are well matched, the voltage generated across RL2 equals the voltage generated across RL1. Therefore, the voltage generated between AIN(+) and AIN(−) corresponds to the voltage generated across the RTD but with the lead resistance error removed.

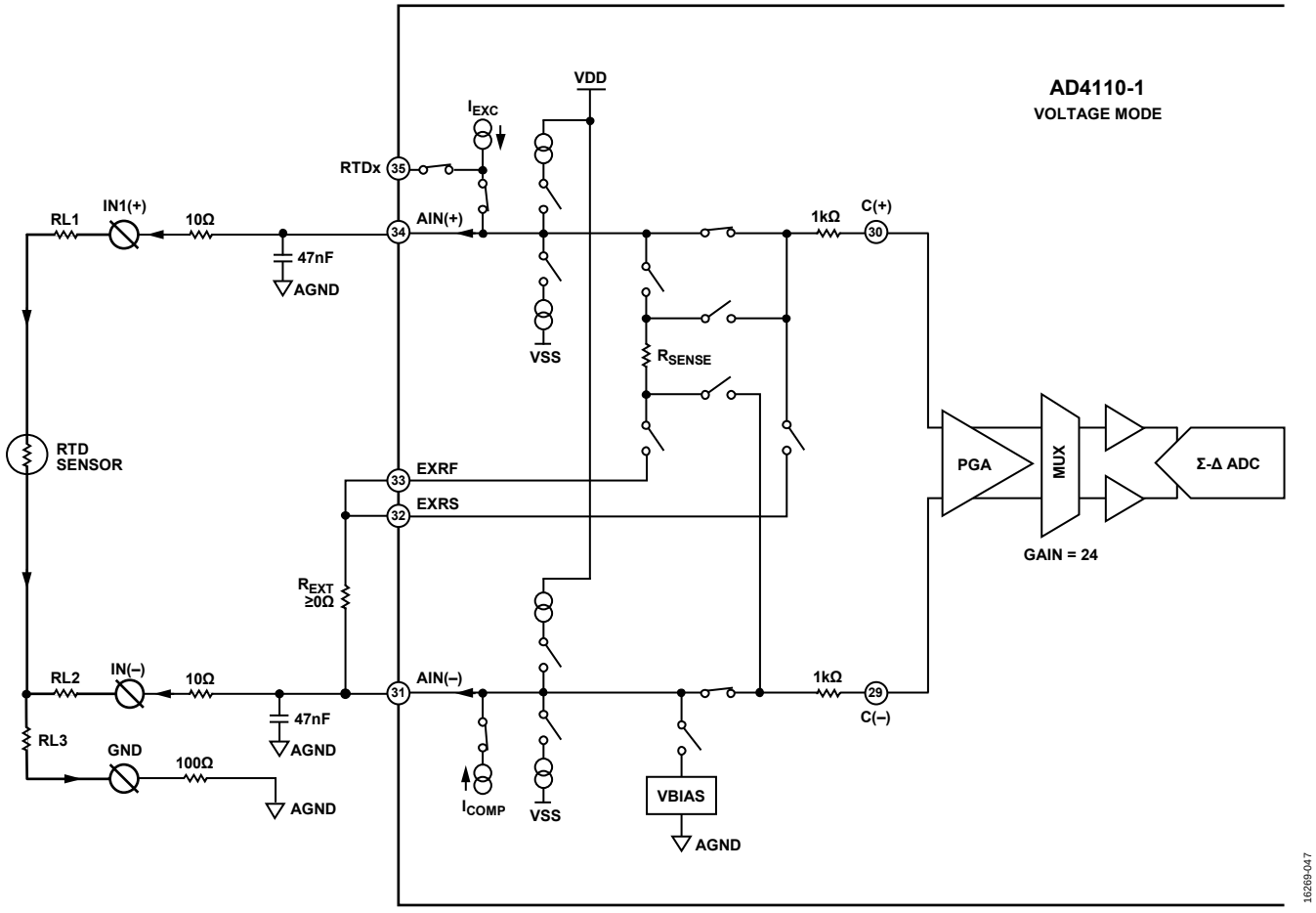


Figure 47. 3-Wire RTD

2-Wire RTD

Figure 48 shows the connection diagram for a 2-wire sensor. Configure the AD4110-1 to operate in voltage mode by clearing the IMODE bit in the AFE_CNTRL2 register (see Table 7).

The AD4110-1 provides a single precision current source on the high voltage channel for use with 2-wire RTD sensors. By default, the AD4110-1 is configured to operate in 4-wire RTD mode. When 2-wire RTD mode is required, set the RTD_3W4W bit in the PGA_RTD_CTRL register (see Table 11 and Table 30).

In 2-wire mode, only the 100 µA excitation current can be used and this current is available on the AIN(+) pin. When using 2-wire mode, the compensation current must be disabled (see Table 30).

When using a 2-wire RTD sensor, enable the VBIAS function (see the Bias Voltage Generator section). Enable the 100 µA pull-down current source on the AIN(−) input by setting the AINN_DN100 bit in the AFE_CNTRL2 register (see Table 7).

The excitation current flows through the RL1 and RL2 lead resistances and through the sensor. In 2-wire mode, it is not possible to compensate for the lead resistance. Therefore, the voltage generated between AIN(+) and AIN(−) equals the sum of the voltage generated across the RTD and the voltage generated by the lead resistance.

Alternative 3-Wire Configuration

An alternative 3-wire configuration is possible using a link wire between the AIN(−) and AGND, and is usually mounted on the module screw terminals. With this configuration, 3-wire RTD mode operation is possible. However, the excitation current flows through the RL1 and RL2 lead resistances, so the voltage generated between AIN(+) and AIN(−) equals the sum of the voltage generated across the RTD and the voltage generated by the lead resistance.

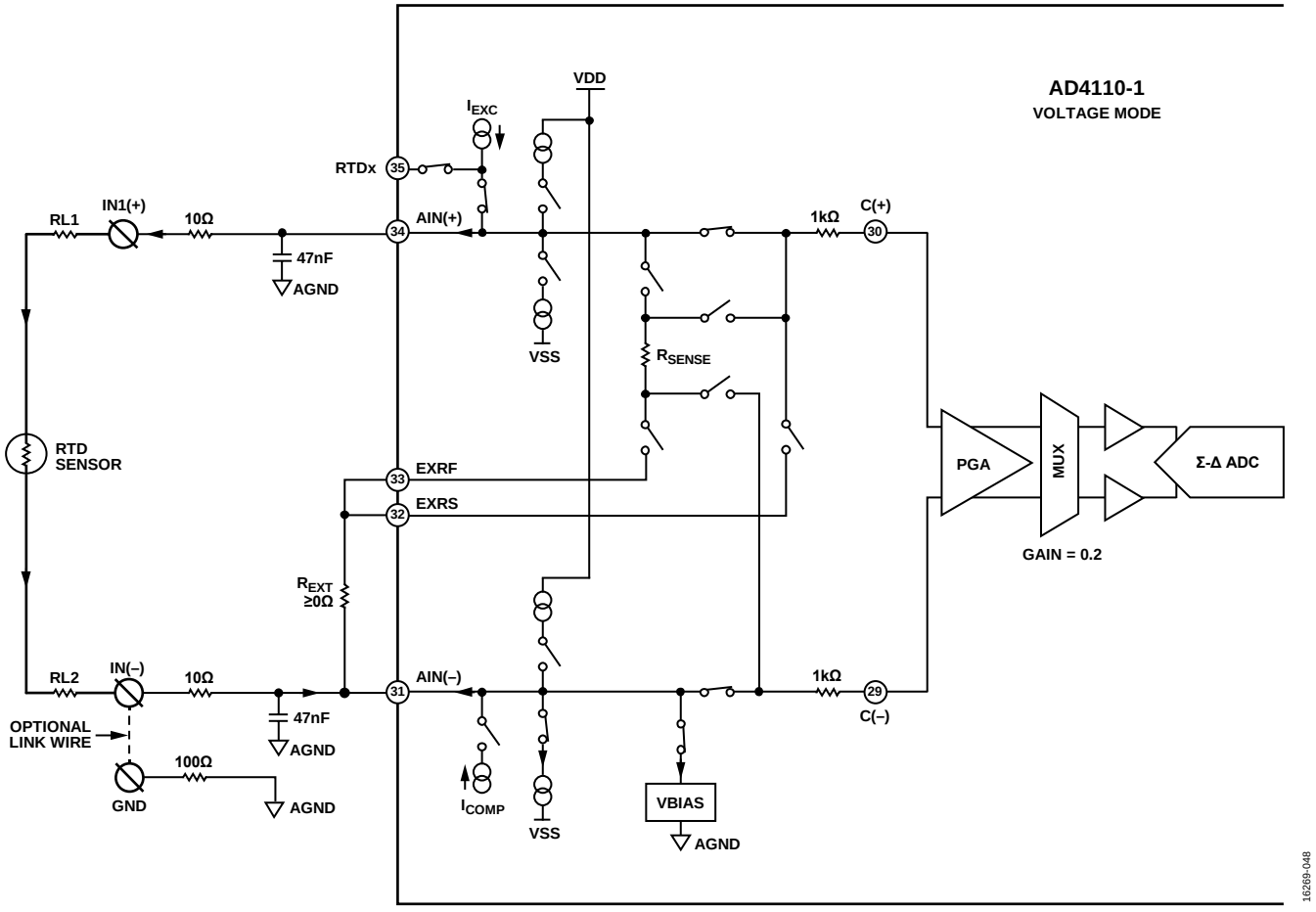


Figure 48. 2-Wire RTD

FIELD POWER SUPPLY MODE

The AD4110-1 provides an option to supply power to a current output sensor connected between the AIN(+) and AIN(−) pins with up to 24 mA.

When Bit 3, EN_FLD_PWR, in the AFE_CNTRL2 register is set to 1, the voltage at the VDD pin –1.5V is routed through internal circuitry to the AIN(+) pin. The voltage drop of 1.5V is a typical value based on the specified maximum output current of 24 mA. The sensor return current flows from the AIN(−) pin through internal circuitry to the VSS pin via a 2.5 V regulator, see Figure 49 below. The voltage seen at the AIN(−) pin is typically VSS + 3.6 V. It is also necessary to set the mode of operation to current mode by setting the IMODE bit to 1 in the AFE_CNTRL2 register.

The internal self-protection circuitry of the AD4110-1 limits the supply current from the AIN(+) pin to typically 55 mA, and the return current into the AIN(−) pin to typically 40 mA. If the supply current limit is exceeded, the overcurrent flag (FLD_PWR_OC) is set in the AFE_DETAIL_STATUS register. If the return current limit is exceeded, the overcurrent flag (AIN_OC) is set in the AFE_DETAIL_STATUS register (see Table 32).

Using external capacitors on C(+) and C(−), combined with the nominal 1.6 kΩ series resistance, a first-order, low-pass anti-aliasing filter can be implemented at the PGA input. A 0.1 µF capacitor is recommended as the differential capacitor, and 0.01 µF capacitors to ground give a -3dB cutoff frequency at approximately 500 Hz (see the Antialiasing Filter section).

To maximize the supply voltage to a current output field transmitter, select the internal current sense resistor. Apply a 0 Ω link in place of the R_{EXT} resistor, as shown in Figure 49.

Since the voltage at VDD is routed through internal circuitry to provide a voltage of VDD − 1.5 V at the AIN(+) pin and the AIN(−) is typically 3.6 V above VSS, both the overvoltage flag on AIN(+) and the undervoltage flag on AIN(−) can be set. This is expected behavior and these flags can be ignored in this case. Alternatively, these flags can be masked out using the AFE error disable register (see Table 31).

Overvoltage Protection

When field power supply mode is enabled, the power supply (VDD/VSS) must be limited to ± 15 V. This requirement is to prevent exceeding the absolute maximum rating for any high voltage pin to VSS, as shown in Table 3.

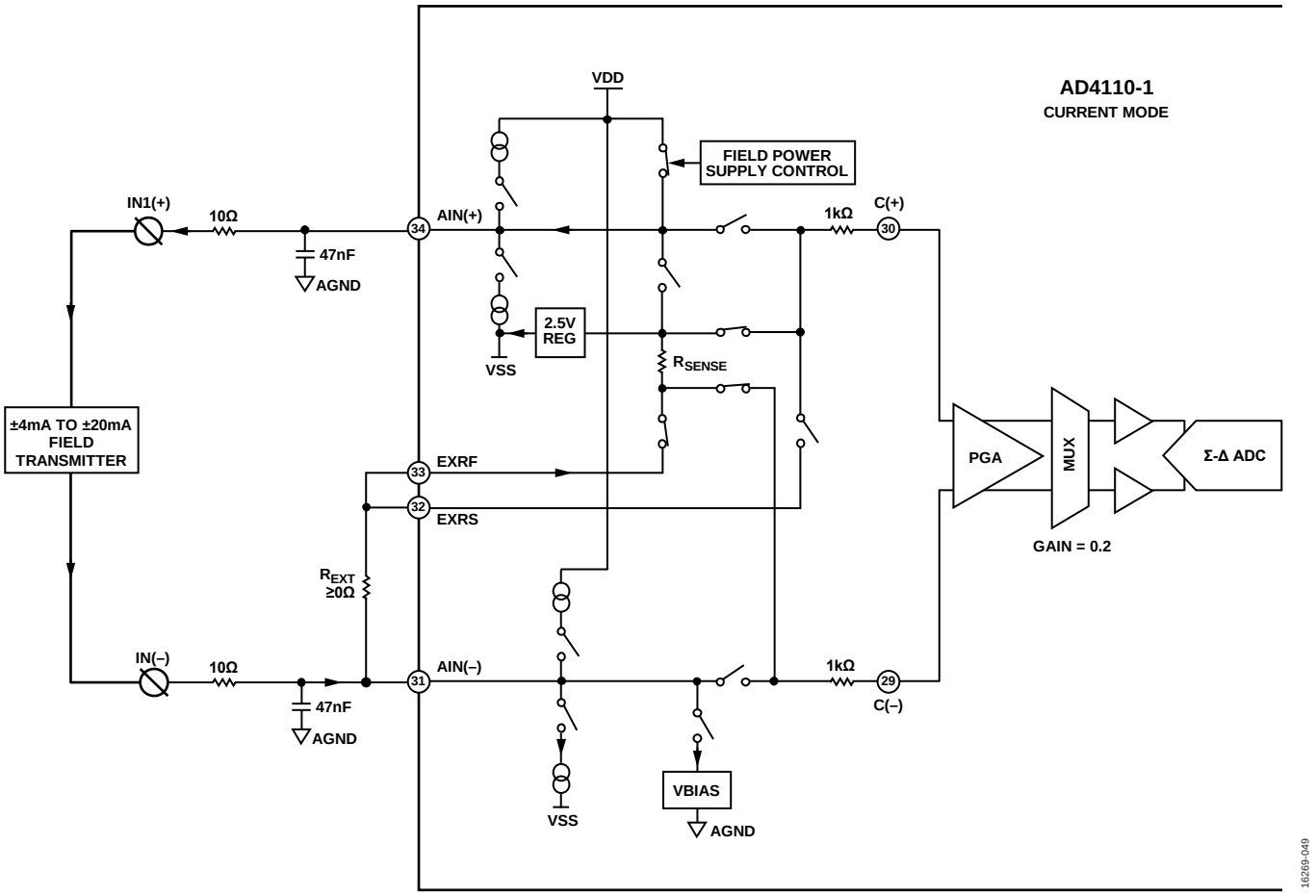


Figure 49. Field Power Supply Mode, R_{EXT} = 0 Ω

NO POWER SUPPLY MODE

When the AD4110-1 has no power supply connected on the VDD and VSS pins, the high voltage analog input of the AD4110-1 defaults to its preprogrammed input mode, either voltage mode or current mode, (see the Default Mode of Operation on Power-Up section).

Voltage Mode

If voltage mode is configured as the default mode of operation, the high voltage inputs operate as high impedance inputs. Typically, in this mode, there is a current flowing between the AIN(+) and AIN(−) pins of ±0.5 mA, see Figure 23.

Current Mode

If current mode is configured as the default mode of operation, the loop is not broken and the ±4 mA to ±20 mA loop current continues to pass through the analog inputs. The AD4110-1 monitors the loop current, and its selfprotection circuitry limits the maximum current through the high voltage inputs to ±55 mA (typical). In this mode, the voltage drop across the AIN(+) and AIN(−) pins is typically 5V, see Figure 26.

System Redundancy

Because the ±4 to ±20 mA loop is not broken when the device has no power supply connected, a second system connected in the loop can continue to operate and provide system redundancy. An example connection diagram is shown in Figure 50.

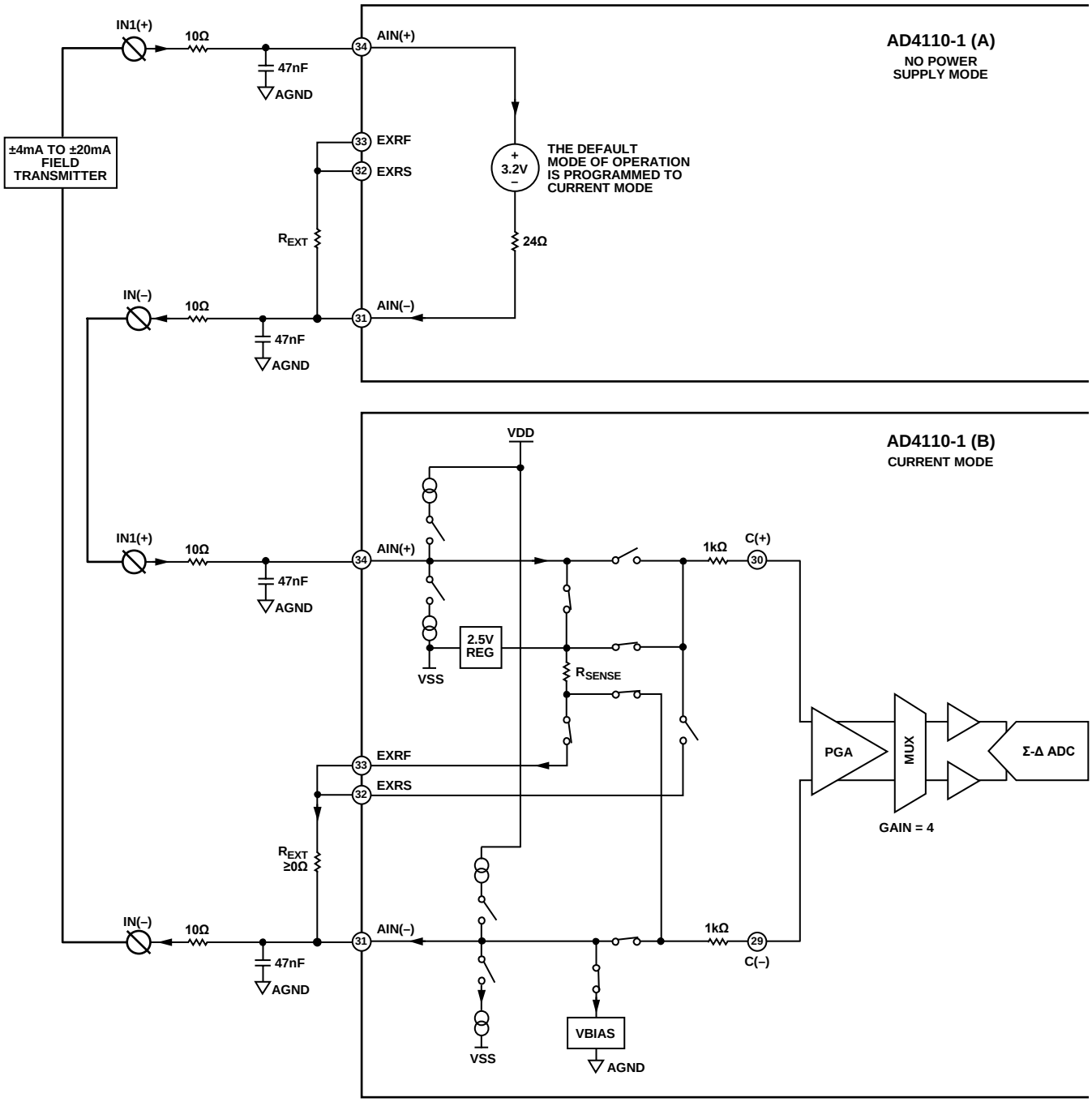


Figure 50. No Power Supply Mode in Redundancy Configuration

GAIN CALIBRATION DATA REGISTER

The AD4110-1 has a set of gain calibration data registers that store the gain correction coefficient for all gain settings in voltage mode and for a gain setting of 4 in current mode. The gain calibration data is stored for the high voltage channel only.

The AFE_CAL_DATA register (Address 0xC) stores the 16 coefficients for voltage mode, and the AFE_RSENSE_DATA register (Address 0xD) stores the coefficient for current mode.

GAIN CALIBRATION IN VOLTAGE MODE

The gain error for voltage mode is measured at each gain setting during device production test, and the corresponding correction coefficient is stored. Only one coefficient can be accessed at a time when the AFE_CAL_DATA register (Address 0xC) is used to access the data value. The coefficient for each gain is accessed by first setting the gain bits to the required gain in the PGA_RTD_CTRL register (Address 0x5) and then reading the AFE_CAL_DATA register (Address 0xC).

The calibration data register value is binary coded and stored in a 10-bit straight binary format. The MSB is an odd parity bit. The available codes are 0 to 511 and can be decoded to reveal the actual coefficient value using the following equation:

$$Coefficient = (Register\ Code_{DEC} - 2^8 + 2^{14})/2^{14}$$

The following equation is used to generate the gain coefficient that is stored and represents the correction factor required to compensate for any measured gain error.

$$Register = ((Nominal\ Gain/Actual\ Gain) \times 2^{14}) - 2^{14} + 2^8$$

The AD4110-1 does not use these coefficients during the ADC conversion process. The AFE_CAL_DATA register is a read-only memory location.

Table 13. Coefficient Examples

Stored Code	Corrective Coefficient	Measured AFE Gain Error (%)
0	0.984375000	+1.5625
1	0.984436035	+1.5564
2	0.984497070	+1.5503
…	…	…
255	0.999938965	+0.0061
256	1.000000000	0.0000
257	1.000061035	−0.0061
…	…	…
510	1.015502930	−1.5503
511	1.015563965	−1.5564

GAIN CALIBRATION IN CURRENT MODE

The gain error for current mode is measured for a gain setting of 4 during device production test, and the corresponding correction coefficient is stored.

The coefficient is accessed by first setting the gain bits to a gain of 4 in the PGA_RTD_CTRL register (Address 0x5) and then reading the AFE_RSENSE_DATA register (Address 0xD).

The calibration data register value is binary coded and stored in a 16-bit straight binary format. The MSB is an odd parity bit. The calibration data register is programmed with the correction coefficient using the following equation:

$$Register = (Nominal\ Gain/Actual\ Gain) \times 2^{14}$$

The current mode calibration data register value is relevant only for applications that use the internal current sense resistor. In applications that use the external current sense resistor, use the voltage mode correction coefficient for the required gain setting.

SCALING FACTOR

For voltage mode, the scaling factor of 2^{14} is chosen to cover an appropriate calibration range vs. device resolution. The step size is approximately 0.0061% in the context of a 0.1% maximum calibrated system error. The calibration range is just above 1.56% in the context of a maximum PGA gain error requirement of ±1%.

The scaling factor of two is chosen because division can be performed as a shift operation rather than a division operation in a microcontroller- or microprocessor- based implementation. This approach can save significant resources in the application, specifically where gain correction is performed in software for every data sample read from the ADC.

For current mode, the step size is approximately 0.0061% in the context of a 0.1% maximum calibrated system error, and the calibration range is well above ±30% in the context of a maximum thin film resistor estimated at ±20%.

AUTOCALIBRATION MODES

After each conversion, the ADC conversion result is scaled using the channel ADC offset and gain registers before being written to the data register.

In unipolar mode,

$$Data = \left[\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right] \times \frac{Gain}{0x400000} \times 2$$

In bipolar mode,

$$Data = \left[\frac{0.75 \times V_{IN}}{V_{REF}} \times 2^{23} - (Offset - 0x800000) \right] \times \frac{Gain}{0x400000} + 0x800000$$

The default value of the offset register is 0x800000 and means that there is no offset to be added or subtracted. The nominal value of the gain register is 0x555555 and means that the ADC gain error is zero. However, during factory calibration of the ADC, the default value is adjusted so that any ADC gain error is compensated for.

The AD4110-1 provides two calibration modes within the ADC that can be used to eliminate the system offset and gain errors on a per setup basis (see Table 39):

- System offset (zero-scale) calibration.
- System gain (full-scale) calibration.

To start a calibration, write the relevant value to the MODE bits in the ADC_MODE register, see Table 39. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register are updated, the $\overline{RDY}$ bit in the status register is reset, the DOUT/$\overline{RDY}$ pin returns low and the AD4110-1 reverts to standby mode. Only one channel can be active during either calibration mode.

System calibrations expect the system zero-scale (offset) and system full-scale (gain) voltages to be applied to the AIN(+) and AIN(−) pins before initiating the calibration mode. As a result, errors external to the ADC are removed. The calibration range of the ADC gain is from 0.4 × V_{REF} to 1.05 × V_{REF}.

A zero-scale (offset) calibration, if required, must always be performed before a full-scale (gain) calibration. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the DOUT/$\overline{RDY}$ pin to determine the end of a calibration via a polling sequence or an interrupt-driven routine. All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed. Calibration can be performed at any output data rate. Using lower output data rates results in improved calibration accuracy and is then accurate for all higher output data rates.

The AD4110-1 provides the application with access to the on-chip gain calibration registers, allowing the microprocessor to read the gain correction coefficients of the device and to write calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during a selfcalibration.

This calibration method is only valid for one PGA gain setting at a time. If the PGA gain is changed, this process must be repeated. Alternatively, the application software retrieves previously stored calibration data and reprograms the gain and offset registers directly. After a power cycle, these registers return to their default values.

APPLICATION EXAMPLES

Example 1

The following example demonstrates how to read the AFE gain calibration register data, calculate the gain correction coefficient, and then apply the gain correction coefficient to the ADC conversion result within the application software.

This example uses the following settings:

- Voltage mode with PGA gain set to 0.2
- Input signal applied is 5.00 V
- ADC result = 5.05 V (this result is within ±1%)
- AFE_CAL_DATA register = 94 (for gain = 0.2)

The calculations are

$$PGA\_GAIN_{COEFFICIENT} = (94 - 2^8 + 2^{14})/2^{14}$$

$$PGA\_GAIN_{COEFFICIENT} = 0.9901123047$$

Multiply ADC Result × $PGA\_GAIN_{COEFFICIENT}$

New ADC Result = 5.000067 V

This result is within ±0.03%.

Example 2

The following example demonstrates how to use the AFE gain calibration register data, calculate the gain correction coefficient, and then reprogram the ADC gain register so that the gain correction coefficient is automatically applied to the ADC conversion result. With this method, it is necessary to combine the factory stored ADC gain correction coefficient with the PGA gain correction coefficient, and then reprogram the ADC gain register.

This example uses the following settings:

- Voltage mode with PGA gain set to 0.2
- AFE_CAL_DATA Register = 94 (for gain = 0.2)
- $PGA\_GAIN_{COEFFICIENT}$ = 0.9901123047
- $ADC\_GAIN_{REGISTER}$ = $0x5556B0_{HEX}$ (5592752 (dec))
- $ADC\_GAIN_{NOMINAL}$ = $0x555555_{HEX}$ (5592405 (dec))

The calculations are

$PGA\_GAIN_{ACTUAL} = PGA\_GAIN_{NOMINAL}/PGA\_GAIN_{COEFFICIENT}$ = 0.2019972876

$ADC\_GAIN_{ACTUAL} = ADC\_GAIN_{NOMINAL}/ADC\_GAIN_{REGISTER}$ = 0.9999379554

$SYS\_GAIN_{ACTUAL} = PGA\_GAIN_{ACTUAL} \times ADC\_GAIN_{ACTUAL}$ = 0.2019847548

$ADC\_GAIN_{MODIFY} = SYS\_GAIN_{NOMINAL}/SYS\_GAIN_{ACTUAL}$ = 0.9901737398

$ADC\_GAIN_{REGISTER} = ADC\_GAIN_{NOMINAL} \times ADC\_GAIN_{MODIFY}$ = 5592405 × 0.9901737398 = 5537453

Reprogram as

$ADC\_GAIN_{REGISTER}$ = 0x547EAD

DIAGNOSTICS AND PROTECTION

DIAGNOSTIC FLAGS

Through the use of diagnostic flags, the AD4110-1 provides diagnostic functions for the high voltage channel to indicate overvoltage, undervoltage, open wire, overcurrent and over-temperature conditions. The status of any AFE diagnostic flag can be checked by reading either or both the AFE_TOP_STATUS and the AFE_DETAIL_STATUS registers. The status of any ADC diagnostic flag can be checked by reading the ADC_STATUS register.

The specified performance as outlined in Table 1 can only be guaranteed when no diagnostic flags are set. An exception is when the field power supply mode is activated. Both the over-voltage flag on AIN(+) and the undervoltage flag on AIN(−) may be set for that channel. This exception is expected behavior and the diagnostic flag can be ignored for that case.

Note that it is recommended to avoid floating inputs and tie them to AGND.

ERROR PIN

The AD4110-1 has an open-drain, active low $\overline{\text{ERR}}$ pin available to indicate an error condition from the high voltage channel of the AFE and an error condition from the ADC. Because this is an open-drain output, it is necessary to connect a pull-up resistor between this pin and the required power supply rail. Refer to the specifications in Table 1 when choosing this resistor value.

The AFE_TOP_ STATUS register and AFE_DETAIL_STATUS register error bits are OR'ed together, inverted, and mapped to the error pin. The error status reporting functionality of the ADC is programmable based on the setting of the ERR_EN bits of the ADC_GPIO_CONFIG register (see Table 44).

When The ERR_EN bits are set to 10, the ADC connects an open-drain, active low output to the $\overline{\text{ERR}}$ pin, and the ADC status register error bits are OR'ed together, inverted, and mapped to the error pin. When the ERR_EN bits are set to 01, the ADC logically OR's the $\overline{\text{ERR}}$ pin input status and the internal ADC error bits with the result available in the ADC_ERR bit of the ADC_STATUS register. This mode combines the AFE and ADC errors into the ADC_ERR bit. Note that when the ERR pin is configured as an input, it is treated as a digital input and its state is not latched. Because the ADC_ERR bit of the ADC_STATUS register is updated only when the ADC result is written, keep the $\overline{\text{ERR}}$ pin active for a time longer than the selected output data rate settling time.

OVERTEMPERATURE DETECTION AND THERMAL SHUTDOWN

An on-chip temperature sensor monitors the die temperature of the AD4110-1. The device has two temperature detection thresholds.

- Overtemperature detection threshold. If the temperature exceeds the overtemperature detection threshold, the TEMPHI bit in the AFE_TOP_STATUS register is set (see Table 14). This error bit is latched. A read of this register is required to clear the error bit status.
- Thermal shutdown threshold. If the temperature exceeds the thermal shutdown threshold, the input channel is forced into voltage input mode, all on-chip current sources are disabled, the field power supply is disabled, and parts of the PGA are shut down. The digital interface remains functional so that the flags can be accessed. The TEMPSD bit in the AFE_TOP_STATUS register is set (see Table 14). This error bit is latched. A read of this register is required to clear the error bit status.
- When the temperature falls below either threshold, the AFE_ERROR flag in the AFE_TOP_STATUS register is cleared and the device powers up again.

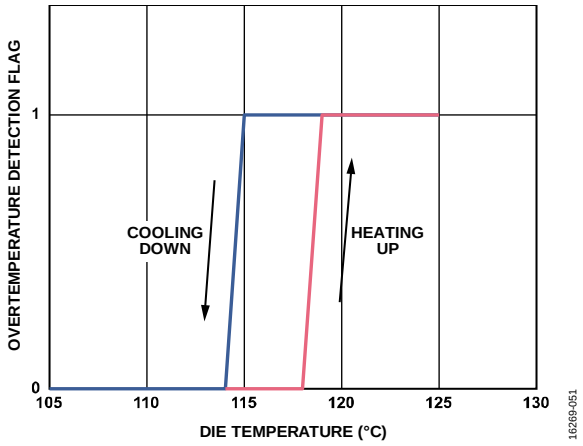


Figure 51. Overtemperature Detection

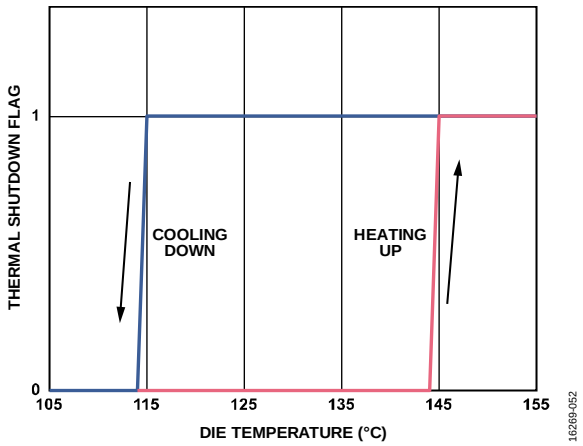


Figure 52. Thermal Shutdown

OVERVOLTAGE AND UNDERVOLTAGE DETECTION

When an overvoltage or undervoltage condition is present on the high voltage inputs of the AD4110-1, the associated error flags (Bits[11:8] in the AFE_DETAIL_STATUS register) are set to indicate that a fault condition is present.

When any error flag is set in the AFE_DETAIL_STATUS register, the AFE_ERROR bit (Bit 0) in the AFE_TOP_STATUS register is also set (see Table 26).

The AIN_OV and AIN_UV error flags are set to 1 when the analog input is within 2 V (typical) of VSS or VDD. These error flags are enabled by default and can be disabled by setting the associated bits in the AFE_ERR_DISABLE register (see Table 15).

Note that the AINP_OV and AINN_UV bits may be set when field power supply mode is active. In this mode, the AIN(+) pin is effectively connected to the VDD power rail and can be at a voltage of VDD − 1.5 V (typical), which is within the overvoltage detection range. The AIN(−) pin is effectively connected to the VSS power rail via a 2.5 V regulator and can be at a voltage of VSS + 2.7 V (typical), which is within the undervoltage detection range.

OVERVOLTAGE PROTECTION

The AD4110-1 operates from a power supply of ±12 V to ±20 V. However, the device can protect against higher voltages on the analog inputs.

Applying a voltage to an HV pin that is more negative than the potential of the system negative power supply can only be accomplished by connecting an external diode from the VSS pin to the system negative power supply, see Figure 29 for the connection diagram.

When the voltage on the analog input exceeds VDD, the performance of the AD4110-1 is degraded, but the device remains functional. The device meets the specifications again as soon as the analog input voltage is within the specified range.

Table 14. Bit Descriptions for the AFE_TOP_STATUS and AFE_DETAIL_STATUS Registers

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0	AFE_TOP_STATUS	[15:8]	Reserved							
		[7:0]	Reserved		ERRCH	ERRCRC	TEMPSD	TEMPHI	Reserved	AFE_ERROR
0x7	AFE_DETAIL_STATUS	[15:8]	Reserved				AINN_UV	AINP_UV	AINN_OV	AINP_OV
		[7:0]	I_EXC	I_COM	Reserved			FLD_PWR_OC	AIN_OC	Error

Table 15. Bit Descriptions for the AFE_ERR_DISABLE Register

Addr.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x6	AFE_ERR_DISABLE	[15:8]	Reserved				AINN_UV	AINP_UV	AINN_OV	AINP_OV
		[7:0]	I_EXC	I_COM	Reserved			FLD_PWR_OC	AIN_OC	Reserved

DIAGNOSING OVERVOLTAGE AND UNDERVOLTAGE CONDITIONS

The overvoltage and undervoltage flags in the AD4110-1 are set when the voltage on the high voltage input is within 2 V (typical) of either the VSS or VDD supply rail. The flags indicate that the input is not within the usable input range (see Table 14).

Figure 53 and Figure 54 show two examples where the AIN(+) input is 13 V greater than the AIN(−) input but with different VDD and VSS power supplies.

In Example 1, Figure 53, the VDD/VSS supply voltage is ±15 V (referenced to AGND). The AINP_OV flag is set to indicate that the input to the AIN(+) pin is within 2 V of VDD.

In Example 2, Figure 54, the VDD/VSS supply voltage is greater than ±15 V (referenced to AGND). The AIN(+) input is also 13 V greater than the AIN(−) input. The voltage on the AIN(+) input is not within 2 V of the VDD rail. Therefore, no overvoltage flag is set, but the output of the ADC is at positive full scale (0xFFFFFF).

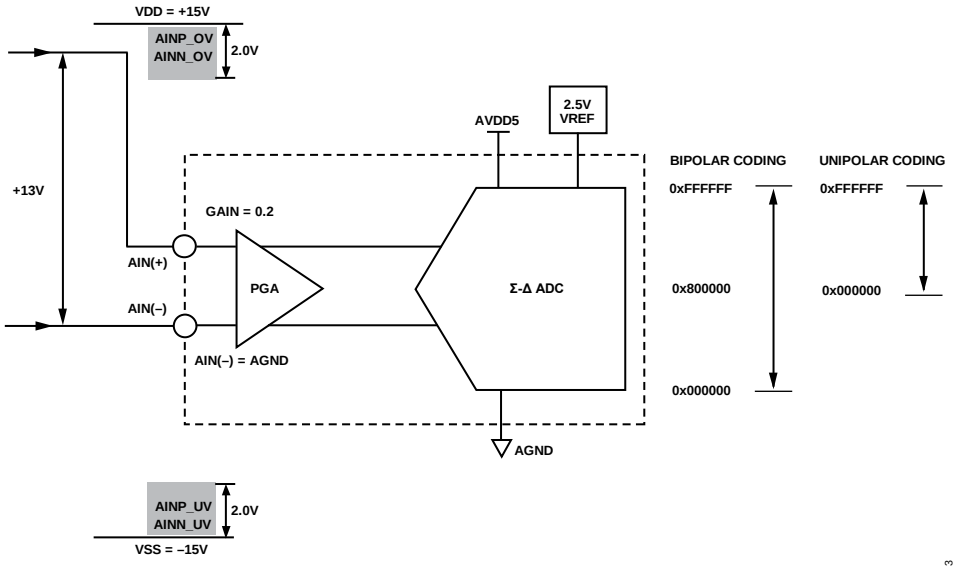


Figure 53. Example 1: 13 V Difference Between the Voltages at the AIN(+) and AIN(−) Pins, (AIN(+) Pin is Within 2 V of VDD)

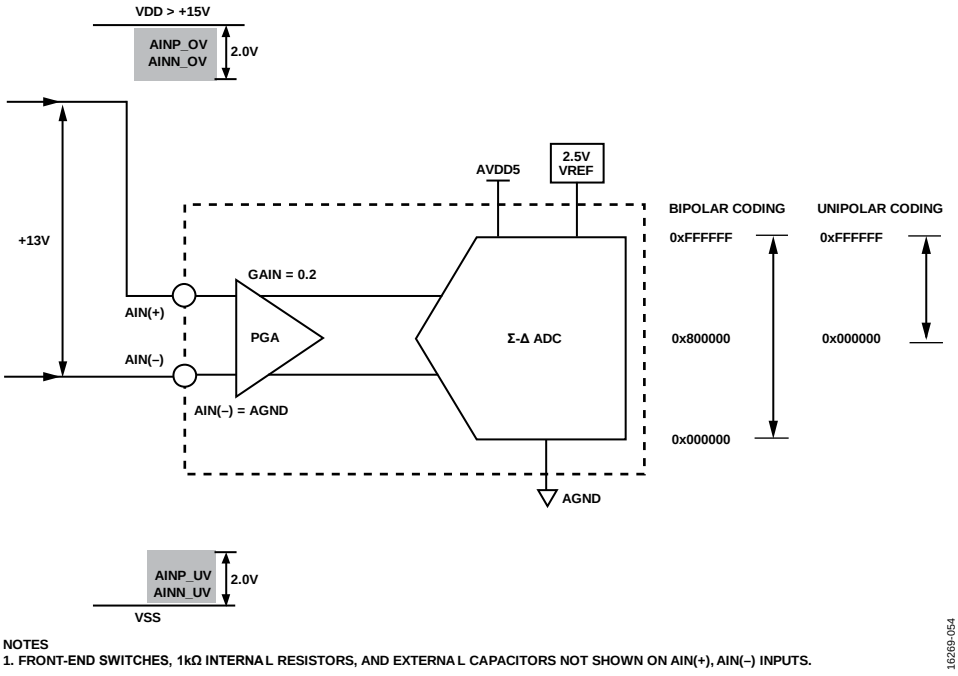


Figure 54. Example 2: 13 V Difference Between the Voltages at the AIN(+) and AIN(−) Pins, (AIN(+) Pin is not Within 2 V of VDD)

OPEN WIRE DETECTION

When the AD4110-1 is configured for the voltage mode of operation, open wire detection currents can be used to detect a broken wire in the connection from the voltage source to the AD4110-1 inputs. Two constant current generators are available on the AIN(+) and AIN(−) inputs. These nonprecision current sources can be programmed to source or sink 1 µA or 100 µA and are disabled by default. See Figure 55 for the configuration diagram. For programming options, see the AFE_CNTRL2 Register section.

These currents can be used to verify that an external transducer remains connected before attempting to take measurements. After the open wire detection currents are turned on, the current flows in the external transducer circuit, and a measurement of the input voltage on the analog input channel can be taken. If a sensor wire is broken, either the overvoltage flag or the undervoltage flag is set.

Because the open wire detection currents can produce an error voltage due to sensor lead resistance, use them only periodically to check for an open wire prior to a measurement.

It can take some time for the open wire detection current to detect an open circuit condition because the currents must charge any external capacitance. The strength of the open wire detection current can be selected as either 1 µA or 100 µA, depending on the amount of external capacitance in the circuit vs. the response time required to diagnose an external open circuit.

DIAGNOSTICS FOR RTD MEASUREMENTS AND RTD FLAGS

The RTD excitation and compensation currents have an output compliance of VDD − 5 V. Therefore, for correct operation, the voltage generated at the RTD pin or at the AIN(+) and AIN(−) pins must be less than VDD − 5 V. Out of compliance flags are available in the AFE_DETAIL_STATUS register (see Table 32).

The AD4110-1 can monitor the voltages on the RTD, AIN(+), and AIN(−) pins. The voltage on the RTD or AIN(+) pin is monitored when the excitation current is active. When the output compliance is exceeded, the I_EXC bit in the AFE_DETAIL_STATUS register is set to 1. For example, this bit is set to 1 if a wire is broken, preventing the excitation current from flowing to ground.

Similarly, the voltage on the AIN(−) pin is monitored when the compensation current is active. When the output compliance is exceeded, the I_COM bit in the AFE_DETAIL_STATUS register is set to 1. For example, this bit is set to 1 if a wire is broken, preventing the compensation current from flowing to ground.

Note that in 4-wire RTD mode, no current flows from the AIN(+) and AIN(−) pins. Therefore, the open wire detection currents described in the Open Wire Detection section must also be used. In 4-wire RTD mode, only the excitation current is used. The out-of-compliance flag is set only when the RTD pin wire or the GND wire is broken (see Figure 46).

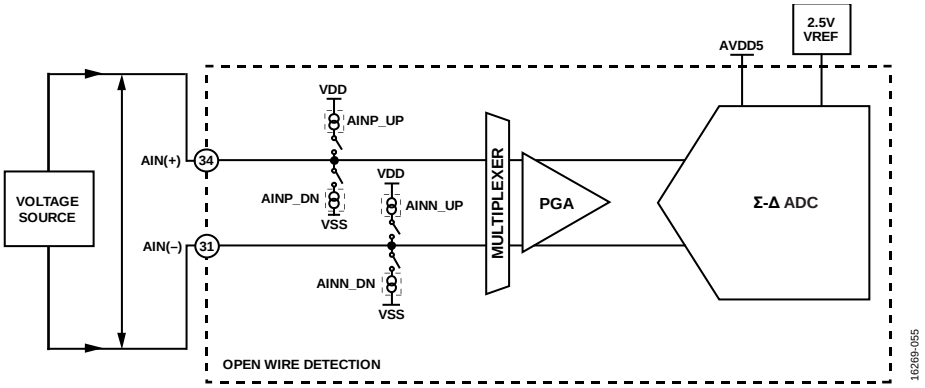


Figure 55. Voltage Input Mode, Open Wire Detection Options

NOISE, SETTLING TIME, AND DIGITAL FILTERING

DIGITAL FILTER

The AD4110-1 has three flexible filter options to allow the optimization of noise, settling time, and rejection.

- Sinc5 + sinc1 filter
- Sinc3 filter
- Enhanced rejection filters for 50 Hz and 60 Hz

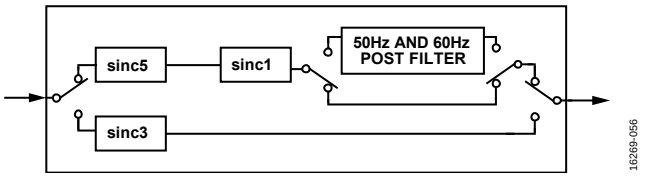


Figure 56. Digital Filter Block Diagram

The filter and output data rate are configured by setting the appropriate bits in the filter configuration register for the selected channels. For more information, see the Filter Register section.

SINC5 + SINC1 FILTER

The sinc5 + sinc1 filter is targeted at fast switching multiplexed applications and achieves single cycle settling at output data rates of 10 kSPS and lower. The sinc5 block output is fixed at the maximum rate of 125 kSPS.

Selecting the fast settling filter (sinc1) as the response of the AD4110-1 digital filter in the ADC filter register (Address 0x5) gives 40 dB rejection of 50 Hz or 60 Hz (±0.5 Hz).

Figure 57 shows the frequency domain response of the sinc5 + sinc1 filter at a 50 SPS output data rate. The sinc5 + sinc1 filter has slow roll-off over frequency and narrow notches.

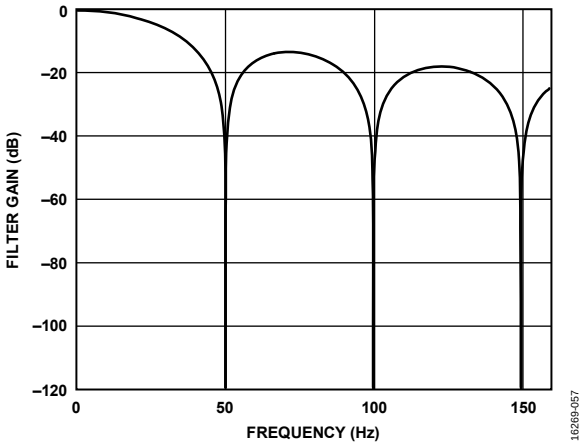


Figure 57. Sinc5 + Sinc1 Filter Response, Output Data Rate = 50 SPS

Table 16 and Table 17 provide the output data rates, settling times, peak-to-peak noise, and rms noise for the sinc5 + sinc1 filter.

SINC3 FILTER

The sinc3 filter achieves the best single-channel noise performance at lower output data rates and is, therefore, most suitable for single-channel applications. The settling time of the sinc3 filter is equal to

$$t_{SETTLE} = 3/Output\ Data\ Rate$$

Figure 58 shows the frequency domain response for the sinc3 filter at a 50 SPS output data rate. The sinc3 filter has good roll-off over frequency and wide notches for good notch frequency rejection. Selecting the sinc3 filter as the response of the AD4110-1 digital filter in the ADC filter register (Address 0x5) gives 100 dB rejection of 50 Hz or 60 Hz (±1 Hz).

Table 18 and Table 19 provide the output data rates, settling times, peak-to-peak noise, and rms noise for the sinc3 filter.

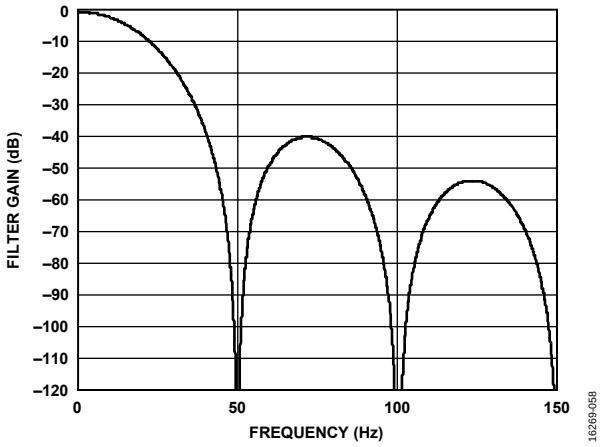


Figure 58. Sinc3 Filter Response, Output Data Rate = 50 SPS

Table 16. Sinc5 + Sinc1 Filter Response—Peak-to-Peak Noise and Resolution (Data Based on 1000 Samples, 500 Samples for Output Data Rate (ODR) < 50 SPS)

Output Data Rate (SPS)	Settling Time (ms)	Switching Rate (Hz)	−3 dB BW (Hz)	Notch Filter (Hz)	Peak-to-Peak Noise				Peak-to-Peak Resolution (Bits)			
					Voltage Mode (μV)			Current Mode (nA)	Voltage Mode			Current Mode
					G = 24	G = 1	G = 0.2	G = 4	G = 24	G = 1	G = 0.2	G = 4
125,000	0.040	24,814	27,000	125,000	44.0	110.0	490.0	2000.0	12.2	15.5	15.6	14.7
62,500	0.048	20,704	20,600	62,500	38.0	92.0	390.0	1708.3	12.4	15.7	16.0	14.9
31,250	0.064	15,552	12,500	31,250	28.0	66.0	300.0	1333.3	12.9	16.2	16.4	15.3
25,000	0.072	13,831	10,280	25,000	24.0	60.0	250.0	1166.7	13.1	16.4	16.6	15.5
15,625	0.096	10,384	6650	15,625	20.0	50.0	230.0	958.3	13.3	16.6	16.7	15.7
10,390	0.096	10,384	6650	15,625	19.0	49.0	210.0	916.7	13.4	16.7	16.9	15.8
4994	0.20	4994	2581	5952	15.0	38.0	180.0	625.0	13.7	17.0	17.1	16.3
2498	0.40	2498	1178	2717	8.9	23.0	110.0	458.3	14.5	17.7	17.8	16.8
1000	1.00	1000	450	1033	5.7	15.0	67.0	320.8	15.2	18.4	18.5	17.3
500	2.00	500	221	508	4.0	12.0	57.0	212.5	15.7	18.7	18.8	17.9
395.5	2.53	395.5	174	400.6	3.2	10.0	46.0	187.5	16.0	18.9	19.0	18.1
200	5.00	200	88	201	2.4	7.5	39.0	120.8	16.4	19.4	19.3	18.7
100.2	10.0	100.2	44	100.5	1.9	6.9	25.0	104.2	16.7	19.5	19.9	19.0
59.87[1]	16.7	59.9	26	60	1.30	5.1	24.0	83.3	17.3	19.9	20.0	19.2
49.92[2]	20.0	49.9	22	50	1.20	4.5	24.0	70.8	17.5	20.1	20.0	19.5
20	50.0	20	9	20	0.87	3.9	18.0	54.2	17.9	20.3	20.4	19.9
16.7[3]	60.0	16.7	7.3	16.7	0.78	3.9	21.0	50.0	18.0	20.3	20.2	20.0
10	100	10	4.3	10	0.66	3.9	21.0	45.8	18.3	20.3	20.2	20.1
5	200	5	2.2	5	0.56	3.6	18.0	41.7	18.5	20.4	20.4	20.2

[1] Rejects 60 Hz.
[2] Rejects 50 Hz.
[3] Rejects 50 Hz and 60 Hz.

Table 17. Sinc5 + Sinc1 Filter Response—RMS Noise and Resolution (Data Based on 1000 Samples, 500 Samples for ODR < 50 SPS)

Output Data Rate (SPS)	Settling Time (ms)	Switching Rate (Hz)	−3 dB BW (Hz)	Notch Filter (Hz)	RMS Noise				RMS Resolution (Bits)			
					Voltage Mode (μV)			Current Mode (nA)	Voltage Mode			Current Mode
					G = 24	G = 1	G = 0.2	G = 4	G = 24	G = 1	G = 0.2	G = 4
125,000	0.040	24,814	27,000	125,000	7.0	15.0	69.0	312.5	14.9	18.3	18.5	17.4
62,500	0.048	20,704	20,600	62,500	5.7	13.0	58.0	258.3	15.2	18.6	18.7	17.6
31,250	0.064	15,552	12,500	31,250	4.4	9.9	44.0	204.2	15.5	19.0	19.1	18.0
25,000	0.072	13,831	10,280	25,000	3.9	9.0	41.0	179.2	15.7	19.1	19.2	18.1
15,625	0.096	10,384	6650	15,625	3.2	7.3	34.0	150.0	16.0	19.4	19.5	18.4
10,390	0.096	10,384	6650	15,625	3.0	7.9	36.0	150.0	16.1	19.3	19.4	18.4
4994	0.20	4994	2581	5952	2.0	5.2	24.0	100.0	16.7	19.9	20.0	19.0
2498	0.40	2498	1178	2717	1.4	3.4	16.0	66.7	17.2	20.5	20.6	19.6
1000	1.00	1000	450	1033	0.9	2.3	10.0	45.8	17.9	21.0	21.2	20.2
500	2.00	500	221	508	0.6	1.7	7.9	30.0	18.4	21.5	21.6	20.7
395.5	2.53	395.5	174	400.6	0.5	1.5	6.8	26.7	18.6	21.6	21.8	20.9
200	5.00	200	88	201	0.4	1.2	5.4	19.6	19.1	22.0	22.1	21.3
100.2	10.0	100.2	44	100.5	0.3	0.9	4.7	14.2	19.5	22.4	22.4	21.8
59.87[1]	16.7	59.9	26	60	0.2	0.8	4.0	12.1	19.9	22.5	22.6	22.0
49.92[2]	20.0	49.9	22	50	0.2	0.8	3.9	11.3	20.0	22.6	22.6	22.1
20	50.0	20	9	20	0.1	0.7	3.6	8.3	20.6	22.9	22.7	22.5
16.7[3]	60.0	16.7	7.3	16.7	0.1	0.6	3.2	7.5	20.7	22.9	22.9	22.7
10	100	10	4.3	10	0.1	0.6	3.2	7.5	21.0	22.9	22.9	22.7
5	200	5	2.2	5	0.1	0.6	3.0	6.7	21.3	23.0	23.0	22.9

[1] Rejects 60 Hz.
[2] Rejects 50 Hz.
[3] Rejects 50 Hz and 60 Hz.

Table 18. Sinc3 Filter Response—Peak-to-Peak Noise and Resolution (Data Based on 1000 Samples, 500 Samples for ODR < 50 SPS)

Output Data Rate (SPS)	Settling Time (ms)	Switching Rate (Hz)	−3 dB BW (Hz)	Notch Filter (Hz)	Peak-to-Peak Noise				Peak-to-Peak Resolution (Bits)			
					Voltage Mode (µV)			Current Mode (nA)	Voltage Mode			Current Mode
					G = 24	G = 1	G = 0.2	G = 4	G = 24	G = 1	G = 0.2	G = 4
125,000	0.024	41,152	37,000	125,000	62.0	690.0	3200.0	7500.0	11.9	12.9	12.9	12.9
62,500	0.048	20,704	18,500	62,500	35.0	120.0	590.0	1875.0	12.6	15.3	15.5	14.7
31,250	0.096	10,384	8650	31,250	20.0	60.0	280.0	1166.7	13.2	16.4	16.6	15.3
25,000	0.120	8313	6840	25,000	19.0	55.0	250.0	916.7	13.3	16.5	16.7	15.7
15,625	0.192	5200	4175	15,625	16.0	41.0	180.0	750.0	13.5	16.6	17.1	16.1
10,417	0.288	3469	2750	10,417	11.0	30.0	140.0	500.0	14.2	17.2	17.4	16.3
5000	0.6	1666	1296	5000	7.7	20.0	98.0	383.3	14.6	17.8	17.9	17.0
2500	1.2	833	644	2500	5.5	14.0	75.0	279.2	15.1	18.3	18.4	17.5
1000	3.0	333	258	1000	3.7	9.5	42.0	175.0	15.7	19.0	19.1	18.1
500	6.0	167	128	500	2.7	7.2	34.0	137.5	16.3	19.3	19.7	18.5
400.6	7.5	134	103	400.6	2.7	6.9	28.0	112.5	16.4	19.5	19.8	18.8
200	15	67	51	200	2.0	5.4	21.0	91.7	16.9	19.8	20.2	19.1
100.2	30	33	26	100.2	1.4	3.9	16.0	70.8	17.4	20.4	20.5	19.7
60[1]	50	20	15	60	1.10	3.0	16.0	54.2	17.6	20.5	20.5	20.1
50[2]	60	17	13	50	0.93	2.7	15.0	45.8	17.9	20.8	20.7	20.1
20	150	7	5.1	20	0.68	2.1	12.0	37.1	18.2	21.0	21.0	20.7
16.7[3]	180	6	4.3	16.7	0.65	1.8	10.0	29.2	18.3	21.0	21.2	20.8
10	300	3	2.7	10	0.58	1.7	8.9	25.0	18.4	21.4	21.2	21.0
5	600	2	1.3	5	0.43	1.6	8.9	25.0	18.9	21.4	21.4	21.0

[1] Rejects 60 Hz.
[2] Rejects 50 Hz.
[3] Rejects 50 Hz and 60 Hz.

Table 19. Sinc3 Filter Response—RMS Noise and Resolution (Data Based on 1000 Samples, 500 Samples for ODR < 50 SPS)

Output Data Rate (SPS)	Settling Time (ms)	Switching Rate (Hz)	−3 dB BW (Hz)	Notch Filter (Hz)	RMS Noise				RMS Resolution (Bits)			
					Voltage Mode (µV)			Current Mode (nA)	Voltage Mode			Current Mode
					G = 24	G = 1	G = 0.2	G = 4	G = 24	G = 1	G = 0.2	G = 4
125,000	0.024	41,152	37,000	125,000	9.6	110.0	530.0	1208.3	14.4	15.5	15.5	15.5
62,500	0.048	20,704	18,500	62,500	5.6	19.0	90.0	291.7	15.3	18.0	18.1	17.5
31,250	0.096	10,384	8650	31,250	3.5	9.3	40.0	179.2	15.9	19.1	19.2	18.3
25,000	0.120	8313	6840	25,000	3.2	8.0	38.0	150.0	16.0	19.3	19.3	18.4
15,625	0.192	5200	4175	15,625	2.4	6.6	30.0	125.0	16.4	19.6	19.7	18.7
10,417	0.288	3469	2750	10,417	1.9	5.2	23.0	91.7	16.7	19.9	20.1	19.0
5000	0.6	1666	1296	5000	1.4	3.4	16.0	66.7	17.2	20.5	20.6	19.6
2500	1.2	833	644	2500	1.0	2.5	11.0	45.8	17.7	21.0	21.0	20.1
1000	3.0	333	258	1000	0.6	1.6	7.3	30.0	18.3	21.6	21.7	20.7
500	6.0	167	128	500	0.4	1.2	5.2	21.7	18.8	22.0	22.2	21.2
400.6	7.5	134	103	400.6	0.4	1.0	4.8	18.8	19.0	22.2	22.4	21.3
200	15	67	51	200	0.3	0.8	3.5	13.8	19.5	22.6	22.8	21.8
100.2	30	33	26	100.2	0.2	0.6	2.8	10.0	20.0	23.1	23.2	22.4
60[1]	50	20	15	60	0.2	0.5	2.5	8.8	20.2	23.3	23.3	22.6
50[2]	60	17	13	50	0.1	0.4	2.2	7.5	20.4	23.4	23.4	22.8
20	150	7	5.1	20	0.1	0.4	1.8	5.8	21.0	23.7	23.7	23.0
16.7[3]	180	6	4.3	16.7	0.1	0.3	1.8	4.7	21.0	23.8	23.7	23.4
10	300	3	2.7	10	0.1	0.3	1.7	5.0	21.3	23.8	23.7	23.3
5	600	2	1.3	5	0.1	0.3	1.5	4.2	21.6	24.0	24.0	23.6

[1] Rejects 60 Hz.
[2] Rejects 50 Hz.
[3] Rejects 50 Hz and 60 Hz.

ENHANCED 50 HZ AND 60 HZ REJECTION FILTERS

The enhanced filters are designed to provide rejection of 50 Hz and 60 Hz simultaneously and to allow the application to trade off settling time and rejection. The enhanced filters can operate at up to 27.27 SPS or can reject interference up to 90 dB at 50 Hz ± 1 Hz and 60 Hz ± 1 Hz.

The enhanced filters are realized by postfiltering the output of the sinc5 + sinc1 filter. Therefore, the sinc5 + sinc1 filter must be selected when using the enhanced filters.

Table 20 and Table 21 provide the output data rates, settling times, rejection of 50 Hz/60 Hz, peak-to-peak noise, and rms noise for the enhanced filters. Figure 59 to Figure 66 are frequency domain plots of the responses from the enhanced filters.

Table 20. Enhanced Filter Response—Peak-to-Peak Noise and Resolution (Data Based on 500 Samples)

Output Data Rate (SPS)	Settling Time (ms)	Switching Rate (Hz)[1]	Simultaneous Rejection of 50 Hz/60 Hz (± 1 Hz) (dB)	Peak-to-Peak Noise				Peak-to-Peak Resolution (Bits)			
				Voltage Mode (µV)			Current Mode (nA)	Voltage Mode			Current Mode
				G = 24	G = 1	G = 0.2	G = 4	G = 24	G = 1	G = 0.2	G = 4
27.27	36.7	27.27	47	1.1	3.3	15.0	66.7	17.5	20.5	20.7	19.5
25	40.0	25	62	1.1	2.7	16.0	54.2	17.6	20.8	20.5	19.8
20	50.0	20	86	1.1	3.0	12.0	50.0	17.6	20.7	21.0	20.0
16.67	60.0	16.667	92	0.93	3.0	13.0	45.8	17.8	20.7	20.8	20.1

[1] The switching rate = $1/t_{SETTLE}$.

Table 21. Enhanced Filter Response—RMS Noise and Resolution (Data Based on 500 Samples)

Output Data Rate (SPS)	Settling Time (ms)	Switching Rate (Hz)[1]	Simultaneous Rejection of 50 Hz/60 Hz (± 1 Hz) (dB)	RMS Noise				RMS (Bits)			
				Voltage Mode (µV)			Current Mode (nA)	Voltage Mode			Current Mode
				G = 24	G = 1	G = 0.2	G = 4	G = 24	G = 1	G = 0.2	G = 4
27.27	36.7	27.27	47	0.18	0.52	2.4	9.2	20.1	23.2	23.3	22.4
25	40.0	25	62	0.17	0.49	2.4	8.3	20.2	23.3	23.3	22.6
20	50.0	20	86	0.16	0.49	2.2	8.3	20.3	23.3	23.5	22.6
16.67	60.0	16.667	92	0.15	0.48	2.2	7.5	20.4	23.3	23.5	22.7

[1] The switching rate = $1/t_{SETTLE}$.

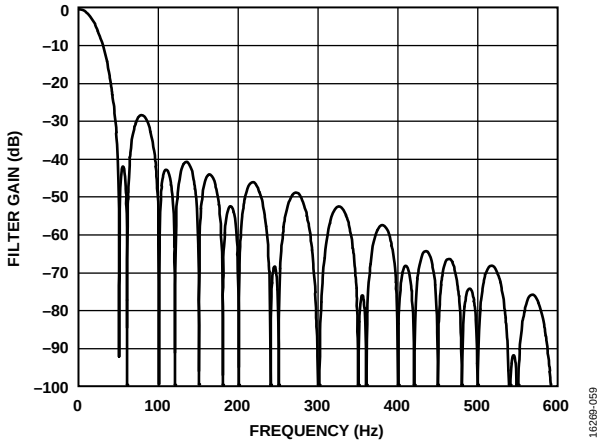


Figure 59. DC to 600 Hz, Output Data Rate = 27.27 SPS, Settling Time = 36.7 ms

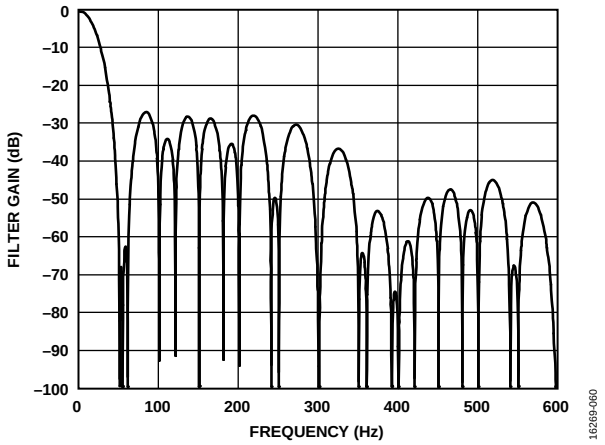


Figure 60. DC to 600 Hz, Output Data Rate = 25 SPS, Settling Time = 40 ms

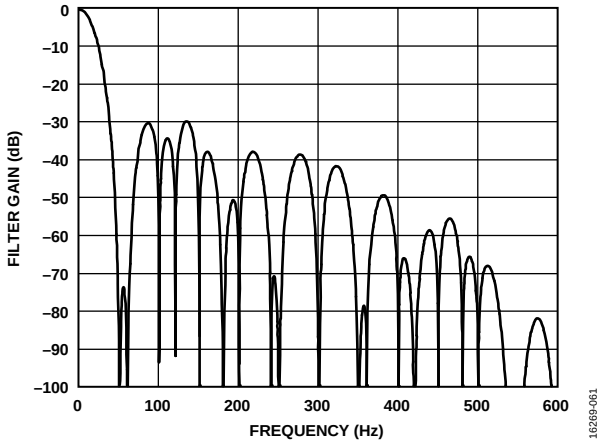


Figure 61. DC to 600 Hz, Output Data Rate = 20 SPS, Settling Time = 50 ms

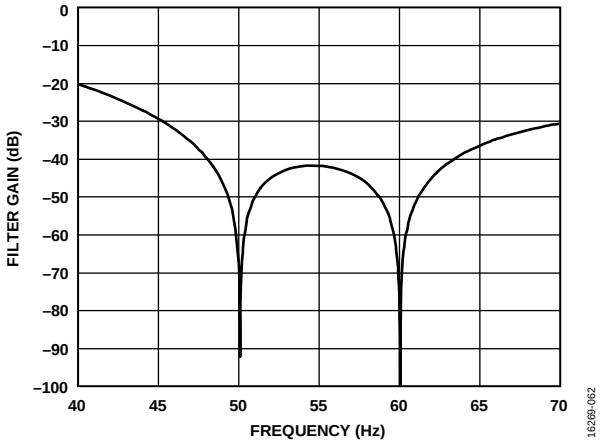


Figure 62. Zoom In, 40 Hz to 70 Hz, Output Data Rate = 27.27 SPS, Settling Time = 36.7 ms

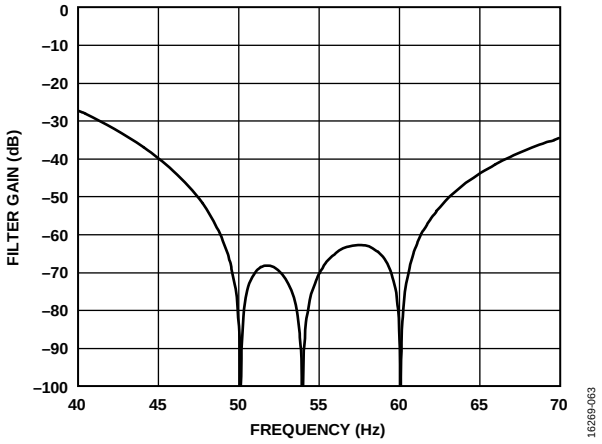


Figure 63. Zoom In, 40 Hz to 70 Hz, Output Data Rate = 25 SPS, Settling Time = 40 ms

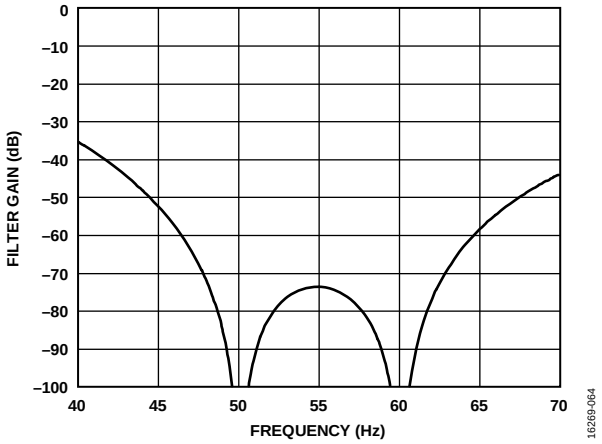


Figure 64. Zoom In, 40 Hz to 70 Hz, Output Data Rate = 20 SPS, Settling Time = 50 ms

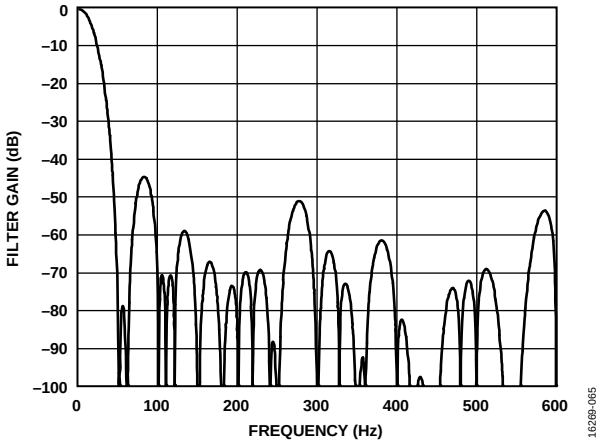


Figure 65. DC to 600 Hz, Output Data Rate = 16.67 SPS, Settling Time = 60 ms

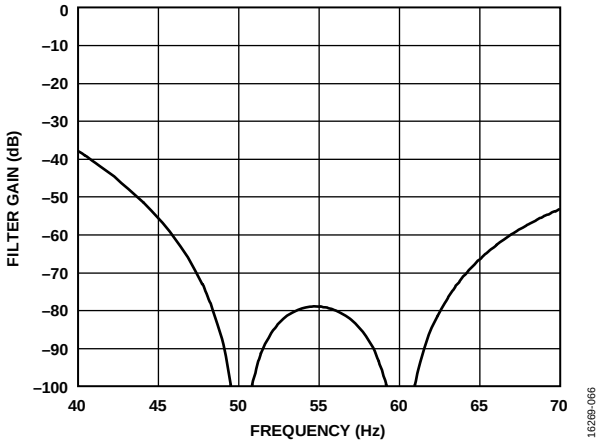


Figure 66. Zoom In, 40 Hz to 70 Hz, Output Data Rate = 16.67 SPS, Settling Time = 60 ms

RTD MODE NOISE PERFORMANCE

Table 22 and Table 23 show the typical rms noise and the noise free (peak-to-peak) resolution of the AD4110-1 for various output data rates and filter settings taken over 500 samples when the ADC is continuously converting.

The values given are for the bipolar input range with an external 2.5 V reference.

These typical values are generated with a 0.01%, 500 Ω, 3 ppm resistor connected to the AIN(+) and AIN(−) pins, and with the device configured in either 3-wire or 4-wire RTD mode. See Figure 46 and Figure 47 for the configuration diagrams.

Note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no output code flicker.

Table 22. 3-Wire and 4-Wire RTD Mode—Peak-to-Peak Resolution Using a 500 Ω Resistor (Data Based on 500 Samples)

Output Data Rate (SPS)	Digital Filter Type	Peak-to-Peak Resolution (Bits)					
		G = 4, 1000 µA	G = 4, 900 µA	G = 8, 600 µA	G = 8, 500 µA	G = 12, 400 µA	G = 24, 100 µA
59.87	Sinc5 + Sinc1	18.1	18.3	17.6	18.0	17.7	17.2
49.92	Sinc5 + Sinc1	18.1	18.3	17.6	18.0	17.7	17.2
60	Sinc3	18.5	18.5	18.2	18.2	17.9	17.7
50	Sinc3	18.5	18.5	18.2	18.2	17.9	17.7

Table 23. 3-Wire and 4-Wire RTD Mode—RMS Resolution Using a 500 Ω Resistor (Data Based on 500 Samples)

Output Data Rate (SPS)	Digital Filter Type	RMS Resolution (Bits)					
		G = 4, 1000 µA	G = 4, 900 µA	G = 8, 600 µA	G = 8, 500 µA	G = 12, 400 µA	G = 24, 100 µA
59.87	Sinc5 + Sinc1	20.8	20.9	20.4	20.5	20.3	19.7
49.92	Sinc5 + Sinc1	20.8	20.9	20.4	20.5	20.3	19.7
60	Sinc3	21.0	21.0	20.6	20.9	20.5	20.3
50	Sinc3	21.0	21.0	20.6	20.9	20.5	20.3

SERIAL PERIPHERAL INTERFACE

The AD4110-1 is programmed using a 4-wire serial peripheral interface (SPI). The serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT/$\overline{RDY}$.

The chip select ($\overline{CS}$) signal selects the device and is also used as a frame for the communication sequence. Each sequence begins with the $\overline{CS}$ falling edge and ends with the $\overline{CS}$ rising edge. The Timing Specifications section includes timing diagrams for interfacing to the AD4110-1.

SCLK is the serial clock input for the device. All data transfers (either on DIN or on DOUT/$\overline{RDY}$) occur with respect to the SCLK signal.

The DIN line transfers data into the on-chip registers and must be valid on the rising edge of SCLK. The DOUT/$\overline{RDY}$ line accesses data from the on-chip registers. DOUT/$\overline{RDY}$ changes on the falling edge of SCLK. The last DOUT/$\overline{RDY}$ bit is valid until the end of the chip select frame.

The AD4110-1 is always a slave in the system. Set the device address for the AD4110-1 by hardwiring the address pins, ADR0 and ADR1. Using these pins, up to four AD4110-1 devices can share the 4-wire serial interface connection to the master. The integrity of the serial communication can be further secured using the 8-bit cyclic redundancy check (CRC). For more information about the CRC, see the CRC Checksum section.

RESETTING THE AD4110-1

After a power-up cycle and when the power supplies are stable, a device reset is required. A wait time of 1 ms is recommended after a device reset before reading or writing to registers.

The AD4110-1 can be reset by writing a series of 1s to the DIN input. If a Logic 1 is written to the DIN line for at least 64 serial clock cycles, the device is reset. The reset returns the serial interface to a state where it expects a write to the communications register. After a device reset, the contents of all registers revert to their power-on values.

SPI COMMAND TO COMMUNICATIONS REGISTER

All communication with the AD4110-1 is initiated by writing an 8-bit command to the communications register, which is the key register in the AD4110-1. The command selects the register map, whether the communication is a read or write, and the register address that is written to or read from. The $\overline{CS}$ pin must be continuously low throughout the 8-bit command write and the subsequent read or write of the selected register.

The MSB of the command word (AFE/$\overline{ADC}$ bit) addresses the write to either the analog front end (AFE) or the ADC registers. The R/$\overline{W}$ bit is set to 0 (write) or 1 (read). The ADR[1:0] bits specify the AD4110-1 device address. If the value of the ADR[1:0] bits does not match the combination of logic levels on the ADR0 and ADR1 pins, the command sequence is ignored by the AD4110-1, and the device waits for a new command at the next chip select frame. The last four bits in the command, R[3:0], specify the AD4110-1 register address to access in the AFE or ADC register map.

The 8-bit command is followed by an 8-/16-/24-bit data read or by a 16-bit/24-bit data write, depending on the register selected.

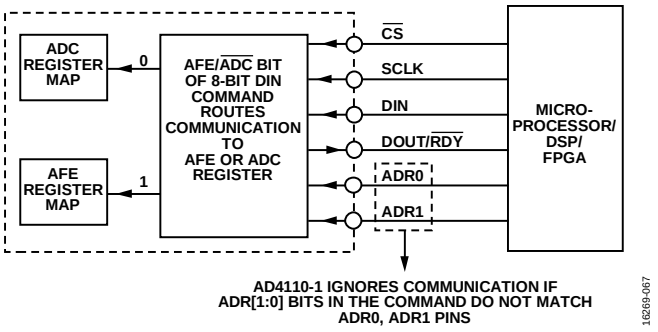


Figure 67. AFE/$\overline{ADC}$ Bit Used to Address the Two AD4110-1 Register Maps

Table 24. Communications Register (Write Only Register)

Bits	Bit Name	Settings	Description
7	AFE/$\overline{ADC}$		The AFE/ADC bit routes the communication write to either the AFE register map or the ADC register map.
		0	ADC register map selected.
		1	AFE register map selected.
6	R/$\overline{W}$		Read/write enable. This bit enables a read or write of the selected register.
		0	Write to selected register.
		1	Read selected register.
[5:4]	ADR[1:0]		Device address bits. Up to four AD4110-1 devices can share the same serial bus. Commands sent on the serial bus are decoded to the correct device when these bits match the state of the ADR1 and ADR0 pins.
[3:0]	R[3:0]		Register address bits. These bits map to the register addresses on both the AFE and ADC register maps.

DOUT/$\overline{\text{RDY}}$ PIN

The DOUT/$\overline{\text{RDY}}$ pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the AD4110-1, and it functions as an indication of the completion of an ADC conversion.

The output shift register can contain data from any on-chip data or control register. The data word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated.

When $\overline{\text{CS}}$ is low and a register is not being read, the DOUT/$\overline{\text{RDY}}$ pin functions as an ADC data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, indicating that valid data is available.

If the ADC data result register is not read after a conversion and the ADC is continuously converting, the DOUT/$\overline{\text{RDY}}$ pin is brought high approximately 2.2 µs before the next conversion result is written to indicate that the data register is about to be updated, and that the register cannot be read at this time. If the data register is being read when an ADC result is written to it, the write is aborted and the conversion result is lost.

ADC conversion control and the SPI interface are not synchronized. Therefore, it is possible for the ADC to be in the process of updating the data result register while the SPI interface is reading the MSB of the same register, thus causing an MSB read error. With an SCLK initial state high, this read error can only happen on the ninth SCLK falling edge after $\overline{\text{CS}}$ goes low.

To avoid a possible MSB error, check the logic state of the DOUT/$\overline{\text{RDY}}$ signal just after the eighth SCLK rising edge, after $\overline{\text{CS}}$ goes low. If the DOUT/$\overline{\text{RDY}}$ signal is at a logic high, the application should wait until it goes low before the ninth SCLK falling edge. If the DOUT/$\overline{\text{RDY}}$ signal is at a logic low, the application must ensure that the time taken before the ninth SCLK falling edge is less than 2.2 µs.

WRITE OPERATION

Figure 68 shows the SPI write operation sequence. The sequence consists of an 8-bit command, 16-bit data, and optional 8-bit CRC. The MSB of the command word (AFE/$\overline{\text{ADC}}$) addresses the write to either the AFE register map or the ADC register map. The R/$\overline{\text{W}}$ bit is set to 0 to specify a write operation. The last four bits in the command, R[3:0], specify the AD4110-1 register address to access in the AFE or ADC register map.

This 8-bit command is followed by the 16-/24-bit data to be written to the specified register. All AFE registers have 16 bits. The optional CRC is enabled on all register writes and reads by setting the CRC_EN bits in both the AFE and ADC register maps.

- AFE_CNTRL1 register (Address 0x1), Bits[14:13]
- ADC_INTERFACE register (Address 0x2), Bits[3:2]

With the CRC enabled, the write operation must continue with an 8-bit CRC calculated by the master device. The AD4110-1 calculates its own CRC based on the bits received on the DIN line, incorporating both the 8-bit command and the data to be written. If the CRC calculated by the AD4110-1 matches the CRC received from the master device, the data is accepted and written to the specified register. If the CRC does not match, the data is not written to the register, and the appropriate CRC error bit (Bit 4 in the AFE_TOP_STATUS register or Bit 5 in the ADC_STATUS register) is set.

If the write operation sequence is terminated (that is, the chip select frame transitions to logic high before the correct number of SCLK cycles), no data is written to any register, and the AD4110-1 waits for a new command at the next chip select frame.

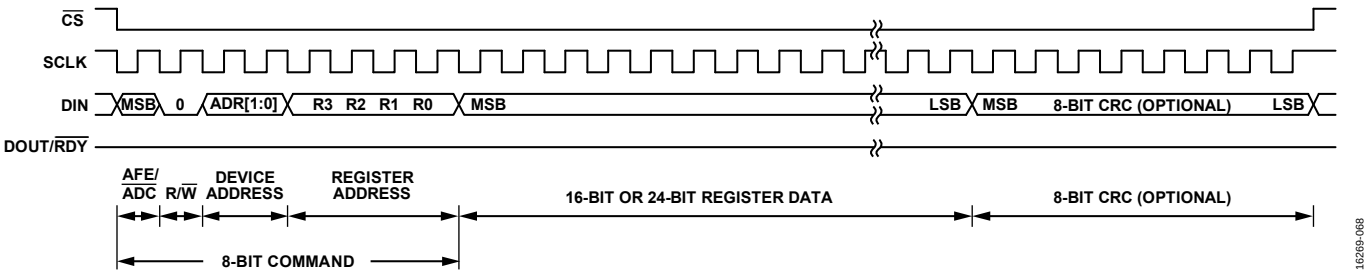


Figure 68. Serial Interface Write Sequence

READ OPERATION

Figure 69 shows the SPI read operation sequence for all registers except the ADC data register. The sequence consists of an 8-bit command to select the AFE or ADC register map and to address the required register. This command is followed by an 8-, 16-, or 24-bit data output and the optional 8-bit CRC from the register being accessed.

The MSB of the command word (AFE/$\overline{\text{ADC}}$) addresses the read to either the AFE register map or the ADC register map. The R/$\overline{\text{W}}$ bit is set to 1 to specify a read operation. The last four bits in the command, R[3:0], specify the AD4110-1 register address to access in the AFE or ADC register map.

At the next falling edge of SCLK after the 8-bit command, the DOUT/$\overline{\text{RDY}}$ pin is switched from its $\overline{\text{RDY}}$ state to its function as the serial data output for the specified register. The data is sent via the DOUT/$\overline{\text{RDY}}$ pin in the following SCLK cycles. The master can send any dummy data via the DIN pin. This dummy data is ignored.

The ADC data register contains the ADC conversion result. The readback from the ADC data register differs from other register reads in that the DOUT/$\overline{\text{RDY}}$ signal is used to signal that a new ADC conversion is ready to be read (see Figure 70).

The DOUT/$\overline{\text{RDY}}$ line transitions from high to low to indicate that a new data conversion is available. When the data is read and $\overline{\text{CS}}$ returns to logic high, the DOUT/$\overline{\text{RDY}}$ pin reverts to a high impedance state.

The optional CRC is enabled on all register writes and reads by setting the CRC_EN bits in both the AFE and ADC register maps.

- AFE_CNTRL1 register (Address 0x1), Bits[14:13]
- ADC_INTERFACE register (Address 0x2), Bits[3:2]

The AD4110-1 calculates and transmits a CRC based on the 8-bit data command received on DIN and the transmitted register data. The data is transmitted to the master on DOUT/$\overline{\text{RDY}}$. This CRC can be used by the master device to implement an error check on the received data.

If the read operation sequence is terminated (that is, the chip select frame transitions to logic high before the correct number of SCLK cycles), the AD4110-1 waits for a new command at the next chip select frame. The DOUT/$\overline{\text{RDY}}$ pin reverts to a high impedance state at the end of the chip select frame.

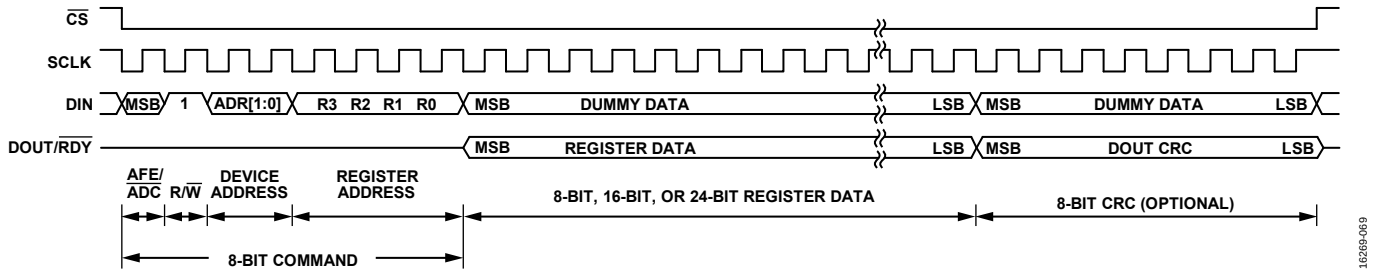


Figure 69. Serial Interface Read Sequence for All Registers Except the ADC_DATA Register

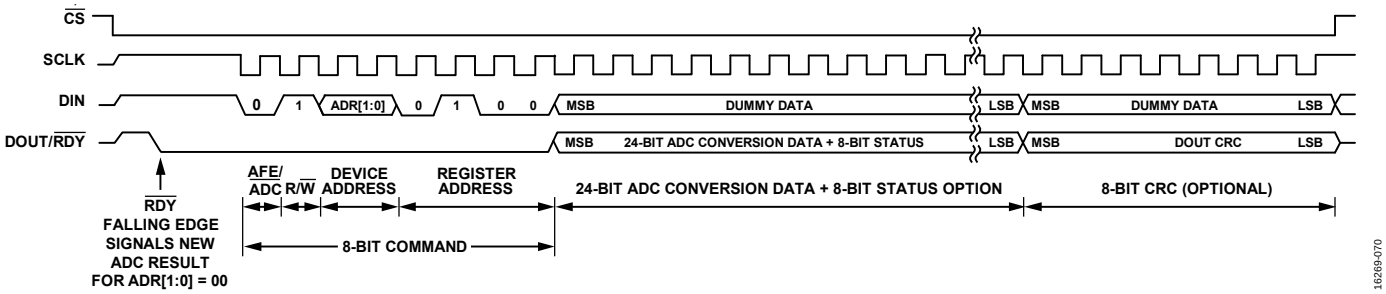


Figure 70. Serial Interface Read Sequence for the ADC_DATA Register (Conversion Result)

MULTIPLE DEVICES ON THE SPI BUS

Up to four AD4110-1 devices can be connected together on a single SPI bus. The two device address pins, ADR0 and ADR1, set the address of each device. Pull these pins up to IOVDD or pull them down to DGND. Each device on the bus requires the address pins to be set differently to each other and a wiring example is shown in Figure 71. In this example, resistors are used to allow easy address reconfiguration, but a hard wire connection to IOVDD or DGND is also possible.

Communication with a device is established when the device address bits of the SPI command byte matches the device address pin setting. Only one device can communicate on the SPI bus during a $\overline{CS}$ frame, that is, the $\overline{CS}$ signal must go low to address one device at a time and then go high again before addressing the next device. The command byte device address bits cannot be changed during a $\overline{CS}$ frame.

The DOUT/$\overline{RDY}$ pin serves a dual purpose. It functions as a serial data output pin to access the output shift register of the AD4110-1, and it functions as an indication of the completion of an ADC conversion.

Only one device can take control of the DOUT/$\overline{RDY}$ signal at any one time. When the $\overline{CS}$ pin is high, all DOUT/$\overline{RDY}$ outputs are tristated. When the $\overline{CS}$ signal goes low, the device with its address pins set to ADR0 = 0 and ADR1 = 0 takes control of the DOUT/$\overline{RDY}$ signal. Control of the DOUT/$\overline{RDY}$ signal passes to the addressed device only after a command byte with a nonzero device address is received. This happens on the eighth rising SCLK edge, see Figure 72.

Since the DOUT/$\overline{RDY}$ signal and the SPI communication signals are not synchronized, the DOUT/$\overline{RDY}$ signal from the device with address pins set to 00 may or may not be active when the $\overline{CS}$ signal is brought low. The DOUT/$\overline{RDY}$ signal may also transition sometime after the $\overline{CS}$ signal is brought low if the device is in continuous conversion mode. Therefore, it is suggested that the DOUT/$\overline{RDY}$ pins be connected to a microcontroller falling edge triggered interrupt pin which is disabled before the $\overline{CS}$ signal goes low and only enabled after the 8th SCLK rising edge. The SCLK should also stop after the 8th rising edge. When the next falling edge of the DOUT/$\overline{RDY}$ signal triggers the microcontroller interrupt, data is ready for the addressed device and SCLK is started again to read out the data.

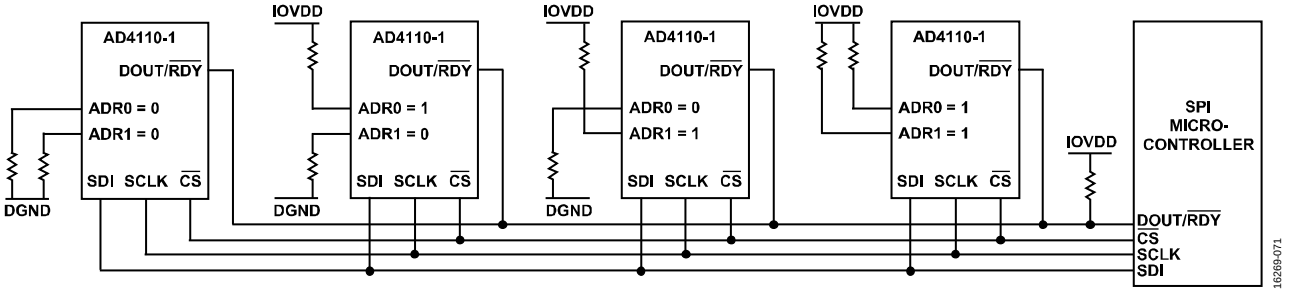


Figure 71. SPI Wiring Connections for Multiple Devices

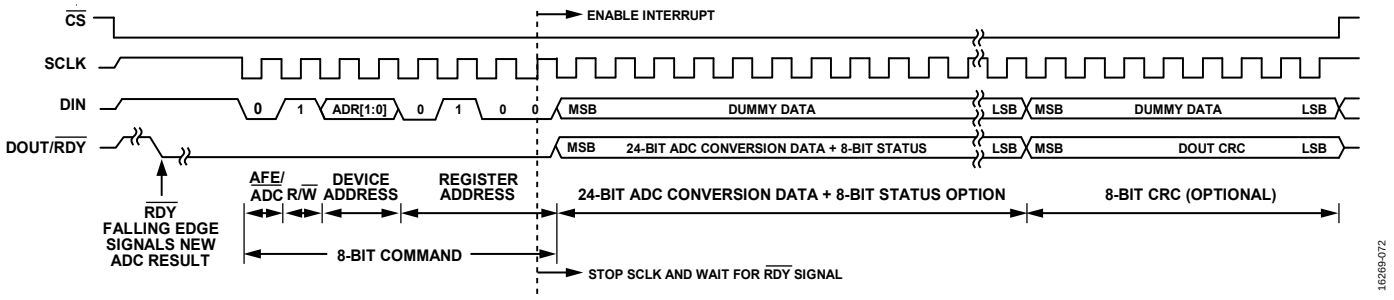


Figure 72. Serial Interface Read Sequence for the ADC_DATA Register with Multiple Devices on the SPI bus

CRC CHECKSUM

The AD4110-1 has a cyclic redundancy check (CRC) that can be used to improve the SPI interface communication robustness during reads and writes to the device.

Using the CRC ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the corresponding CRC error bit is set in either the AFE_TOP_STATUS register or the ADC_STATUS register.

Using the CRC ensures that only valid writes take place but the CRC cannot detect whether a write operation completed successfully. This inability to detect completion is because the CRC error bits are not set when an SPI read transaction occurs instead of an SPI write transaction, due to an error in communication. To verify that a write to a register has taken place, the same register contents must be read back. The data that is read back includes a CRC checksum to allow for validation of the data.

For the AFE, the following polynomial is the CRC checksum calculation that is used during a read or write operation:

$$x^8 + x^2 + x + 1$$

The same polynomial is used for ADC writes. During ADC read operations, the application can select between the polynomial type and a similar exclusive OR (XOR) function.

The XOR function requires less time to process on the host microcontroller than the polynomial based checksum. The CRC_EN bits in the ADC_INTERFACE register enable and disable the checksum and allow the application to select between the polynomial and the XOR implementation.

The 8-bit CRC checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8- to 24-bit data. For a read transaction, the checksum is calculated using the command word and the 8- to 32-bit data output.

A register is modified only if a correct CRC checksum is received as part of the SPI write transaction. A CRC checksum is sent by the AD4110-1 as part of a read transaction. Figure 73 and Figure 74 show an SPI write and read transaction, respectively, using the CRC.

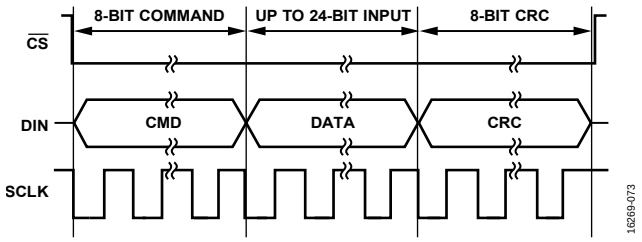


Figure 73. SPI Write Transaction with CRC

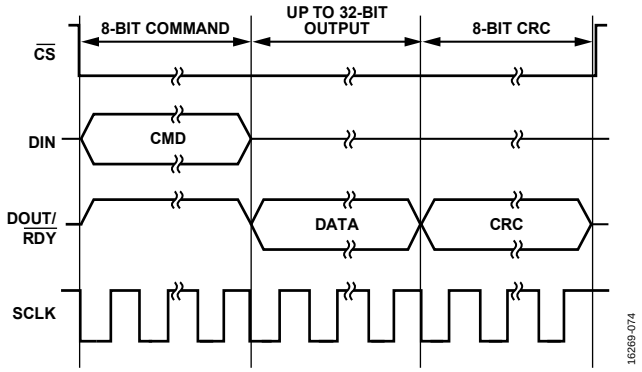


Figure 74. SPI Read Transaction with CRC

CRC CHECKSUM METHODS

Polynomial Calculation

The checksum, which is 8 bits wide, is generated using the polynomial:

$$x^8 + x^2 + x + 1$$

To generate the checksum, the data is left shifted by eight bits to create a number ending in eight Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An XOR function is applied to the data to produce a new, shorter number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This polynomial is the 8-bit checksum.

Polynomial CRC Calculation of a 24-Bit Word: 0x654321 (Eight Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

	6 5 4 3 2 1
Initial value:	0110 0101 0100 0011 0010 0001
Left shifted eight bits:	0110 0101 0100 0011 0010 0001 0000 0000
Polynomial:	100 0001 11
XOR 1	10 0100 1000 0011 0010 0001 0000 0000
	10 0000 111
XOR 2	100 0110 0011 0010 0001 0000 0000
	100 0001 11
XOR 3	111 1111 0010 0001 0000 0000
	100 0001 11
XOR 4	11 1110 1110 0001 0000 0000
	10 0000 111
XOR 5	1 1110 0000 0001 0000 0000
	1 0000 0111
XOR 6	1110 0111 0001 0000 0000
	1000 0011 1
XOR 7	110 0100 1001 0000 0000
	100 0001 11
XOR 8	10 0101 0101 0000 0000
	10 0000 111
XOR 9	101 1011 0000 0000
	100 0001 11
XOR 10	1 1010 1100 0000
	1 0000 0111
XOR 11	1010 1011 0000
	1000 0011 1
XOR 12	10 1000 1000
	10 0000 111
CRC Checksum (0x86)	1000 0110

XOR Calculation

The checksum, which is eight bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

XOR CRC calculation of a 24-bit word:

0x654321 (eight command bits and 16-bit data)

An example of generating the 8-bit checksum using the polynomial-based checksum is as follows:

Divide into three bytes: 0x65, 0x43, and 0x21

0x65	0110 0101
0x43	0100 0011
XOR Result	0010 0110
0x21	0010 0001
CRC Checksum (0x07)	0000 0111

REGISTER DETAILS

Throughout this section, RW means read and write, R means read only, and W means write only.

AFE REGISTER MAP

Table 25. AFE Register Map

Reg	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0	AFE_TOP_STATUS	[15:8]	Reserved								0xD000	R
		[7:0]	Reserved		ERRCH	ERRCRC	TEMPSD	TEMPHI	Reserved	AFE_ERROR		
0x1	AFE_CNTRL1	[15:8]	Reserved	CRC_EN			Reserved		DISRTD	Reserved	0x0000	RW
		[7:0]	Reserved									
0x2	Reserved	[15:8]	Reserved								0x0000	R
		[7:0]	Reserved									
0x3	AFE_CLK_CTRL	[15:8]	Reserved								0x0000	RW
		[7:0]	Reserved			CLK_CFG		Reserved				
0x4	AFE_CNTRL2	[15:8]	AINN_DN100	AINN_DN1	AINN_UP100	AINN_UP1	AINP_DN100	AINP_DN1	AINP_UP100	AINP_UP1	0x0082	RW
		[7:0]	VBIAS		Reserved		EN_FLD_PWR	EXT_R_SEL	IMODE	Reserved		
0x5	PGA_RTD_CTRL	[15:8]	RTD_3W4W	I_COM_SEL			I_EXC_SEL			EXT_RTD_RES	0x0000	RW
		[7:0]	GAIN_CH				Reserved					
0x6	AFE_ERR_DISABLE	[15:8]	Reserved				AINN_UV	AINP_UV	AINN_OV	AINP_OV	0x0000	RW
		[7:0]	I_EXC	I_COM	Reserved			FLD_PWR_OC	AIN_OC	Reserved		
0x7	AFE_DETAIL_STATUS	[15:8]	Reserved				AINN_UV	AINP_UV	AINN_OV	AINP_OV	0x0000	R
		[7:0]	I_EXC	I_COM	Reserved			FLD_PWR_OC	AIN_OC	Error		
0x8	Reserved	[15:8]	Reserved								0x0000	R
		[7:0]	Reserved									
0x9	Reserved	[15:8]	Reserved								0x0000	R
		[7:0]	Reserved									
0xA	Reserved	[15:8]	Reserved								0x0000	R
		[7:0]	Reserved									
0xB	Reserved	[15:8]	Reserved								0x0000	R
		[7:0]	Reserved									
0xC	AFE_CAL_DATA	[15:8]	Reserved						Parity	GAIN_CAL[8]	0x0XXX	R
		[7:0]	GAIN_CAL[7:0]									
0xD	AFE_RSENSE_DATA	[15:8]	Parity	RSEN_CAL[14:8]							0xXXXX	R
		[7:0]	RSEN_CAL[7:0]									
0xE	NO_PWR_ DEFAULT_SEL	[15:8]	Reserved								0x0000	W
		[7:0]	D_MODE									
0xF	NO_PWR_ DEFAULT_STATUS	[15:8]	Reserved							COMM_ERR	0x00XX	R
		[7:0]	Count									

AFE REGISTER DESCRIPTIONS

AFE_TOP_STATUS Register

Address: 0x0, Reset: 0xD000, Name: AFE_TOP_STATUS

The read only AFE_TOP_STATUS register indicates the status of the AFE. The register can be read via the serial interface to verify that the internal temperature of the chip is within limits and to check whether an error condition in the analog input channel was detected. All individual error bits (Bits[5:2]) are latched. Therefore, if an error condition occurs for even a short period of time, the error condition is captured by the error logic and indicated by the relevant error bit until this register is read. The overall error bit (Bit 0, AFE_ERROR) is not latched and reflects the sum of all unmasked errors at the time of reading. The AFE_ERROR bit is not cleared by reading the AFE status register, but individual error bits can be prevented (masked) from driving the AFE_ERROR bit by setting the appropriate bits in the AFE_ERR_DISABLE register (Address 0x6).

Table 26. Bit Descriptions for the AFE_TOP_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Silicon Revision ID.	0xD	R
[7:6]	Reserved		Reserved.	0x0	R
5	ERRCH		Error on channel.	0x0	R
		0	No error.		
		1	Indicates one or more errors detected on the high voltage channel.		
4	ERRCRC		CRC check failed. This bit is set when a CRC error occurs during a register write to any AFE register.	0x0	R
		0	No error.		
		1	Indicates an error during SPI communication.		
3	TEMPSD		Thermal shutdown.	0x0	R
		0	No error.		
		1	Indicates that the chip temperature exceeded the thermal shutdown threshold, as specified in Table 1. To minimize power dissipation, the high voltage channel is forced into voltage input mode, all on-chip current sources are shut down, the field power supply is shut down, and parts of the PGA are shut down. The SPI interface remains functional.		
2	TEMPHI		Overtemperature detection.	0x0	R
		0	No error.		
		1	Indicates that the chip temperature exceeded the overtemperature detection threshold, as specified in Table 1. The system controller must take the appropriate actions to lower the device power dissipation.		
1	Reserved		Reserved.	0x0	R
0	AFE_ERROR		Error on channel.	0x0	R
		0	No error.		
		1	Indicates an error condition that is not masked by the AFE_ERR_DISABLE register. The state of this bit is directly reflected by the status of the $\overline{\text{ERR}}$ output pin, in reversed polarity. That is, when this bit is set to 1, the open-drain, active low $\overline{\text{ERR}}$ output pin is driven low to indicate an error.		

AFE_CNTRL1 Register

Address: 0x1, Reset: 0x0000, Name: AFE_CNTRL1

The AFE_CNTRL1 register is used to enable RTD excitation and compensation currents and to enable the CRC checksum mode on the AFE interface. To enable CRC checksum mode, Bits[14:13] in this register must be set, as well as Bits[3:2] in the ADC_INTERFACE register (see Table 40).

Table 27. Bit Descriptions for the AFE_CNTRL1 Register

Bits	Bit Name	Settings	Description	Reset	Access
15	Reserved		Reserved.	0x0	R
[14:13]	CRC_EN		CRC checksum enable.	0x0	RW
		00	CRC checksum disabled.		
		01	Reserved.		
		10	8-bit CRC enabled on reads and writes.		
		11	Reserved.		
[12:10]	Reserved		Reserved.	0x0	R
9	DISRTD		Disable all RTD excitation and compensation currents.	0x0	RW
		0	RTD currents are on.		
		1	RTD currents are off.		
8	Reserved		Reserved.	0x0	R
[7:0]	Reserved		Reserved.	0x00	R

AFE_CLK_CTRL Register

Address: 0x3, Reset: 0x0000, Name: AFE_CLK_CTRL

The application software must write to this register during the device initialization routine to set Bits[4:3] to 10. This write is required to ensure that the AFE and ADC are synchronized with the same clock.

Table 28. Bit Descriptions for the AFE_CLK_CTRL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:5]	Reserved		Reserved.	0x0	R
[4:3]	CLK_CFG		CLKIO pin configuration.	0x0	RW
		00	Internal.		
		01	Reserved.		
		10	AFE clocked by ADC (required setting).		
		11	Reserved.		
[2:0]	Reserved		Reserved.	0x0	R

AFE_CNTRL2 Register

Address: 0x4, Reset: 0x0082, Name: AFE_CNTRL2

The AFE_CNTRL2 register is used to enable open wire detection, VBIAS, and field power supply mode. This register is also used to select the external sense resistor for current input mode and to select the voltage mode or current mode of operation.

Table 29. Bit Descriptions for the AFE_CNTRL2 Register

Bits	Bit Name	Settings	Description	Reset	Access
15	AINN_DN100		Enable open wire detection on AIN(−) with the detection current = −100 µA.	0x0	RW
		0	Off.		
		1	On.		
14	AINN_DN1		Enable open wire detection on AIN(−) with the detection current = −1 µA.	0x0	RW
		0	Off.		
		1	On.		
13	AINN_UP100		Enable open wire detection on AIN(−) with the detection current = +100 µA.	0x0	RW
		0	Off.		
		1	On.		
12	AINN_UP1		Enable open wire detection on AIN(−) with the detection current = +1 µA.	0x0	RW
		0	Off.		
		1	On.		
11	AINP_DN100		Enable open wire detection on AIN(+) with the detection current = −100 µA.	0x0	RW
		0	Off.		
		1	On.		
10	AINP_DN1		Enable open wire detection on AIN(+) with the detection current = −1 µA.	0x0	RW
		0	Off.		
		1	On.		
9	AINP_UP100		Enable open wire detection on AIN(+) with the detection current = +100 µA.	0x0	RW
		0	Off.		
		1	On.		
8	AINP_UP1		Enable open wire detection on AIN(+) with the detection current = +1 µA.	0x0	RW
		0	Off.		
		1	On.		
[7:6]	VBIAS		Common-mode bias to GND.	0x2	RW
		00	Reserved.		
		01	50 µA bias on.		
		10	Off (default).		
		11	Off.		
[5:4]	Reserved		Reserved.	0x0	R
3	EN_FLD_PWR		Enable field power supply mode.	0x0	RW
		0	Field power supply is off.		
		1	Field power supply is on.		
2	EXT_R_SEL		Select external current sense resistor for use in current mode.	0x0	RW
		0	Internal sense resistor selected.		
		1	External sense resistor selected.		
1	IMODE		Enable current mode. The power-on default setting of this bit can be programmed by the application.	0x1	RW
		0	Voltage mode selected.		
		1	Current mode selected.		
0	Reserved		Reserved.	0x0	R

PGA_RTD_CTRL Register

Address: 0x5, Reset: 0x0000, Name: PGA_RTD_CTRL

The PGA_RTD_CTRL register is used to enable RTD measurement mode (4-wire, 3-wire, or 2-wire) and to configure the magnitude of the excitation and compensation currents. This register is also used to set the channel gain.

Table 30. Bit Descriptions for the PGA_RTD_CTRL Register

Bits	Bit Name	Settings	Description	Reset	Access
15	RTD_3W4W		Configure the device for 2-wire, 3-wire, or 4-wire RTD connection.	0x0	RW
		0	4-wire (current via RTD pin).		
		1	2-wire or 3-wire (currents via AIN(+) and AIN(−) pins).		
[14:12]	I_COM_SEL		RTD compensation current.	0x0	RW
		000	Disabled.		
		001	100 µA.		
		010	400 µA.		
		011	500 µA.		
		100	500 µA.		
		101	600 µA.		
		110	900 µA.		
		111	1000 µA.		
[11:9]	I_EXC_SEL		RTD excitation current.	0x0	RW
		000	Disabled.		
		001	100 µA.		
		010	400 µA.		
		011	500 µA.		
		100	500 µA.		
		101	600 µA.		
		110	900 µA.		
		111	1000 µA.		
8	EXT_RTD_RES		Select the external RTD resistor.	0x0	RW
		0	Internal RTD resistor selected.		
		1	External RTD resistor selected.		
[7:4]	GAIN_CH		Set the channel gain.	0x0	RW
		0000	Gain = 0.2.		
		0001	Gain = 0.25.		
		0010	Gain = 0.3.		
		0011	Gain = 0.375.		
		0100	Gain = 0.5.		
		0101	Gain = 0.75.		
		0110	Gain = 1.		
		0111	Gain = 1.5.		
		1000	Gain = 2.		
		1001	Gain = 3.		
		1010	Gain = 4.		
		1011	Gain = 6.		
		1100	Gain = 8.		
		1101	Gain = 12.		
		1110	Gain = 16.		
		1111	Gain = 24.		
[3:0]	Reserved		Reserved.	0x0	R

AFE_ERR_DISABLE Register

Address: 0x6, Reset: 0x0000, Name: AFE_ERR_DISABLE

The bits in the AFE_ERR_DISABLE register can be set to mask (disable) error events. When any bit in this register is set to 1 (error is masked), the specified error is not included in the sum of errors that is represented by the AFE_ERROR bit in the AFE_TOP_STATUS register (Address 0x0). The application can use the AFE_ERR_DISABLE register to select the errors that are reported in real time by the $\overline{\text{ERR}}$ pin and by the AFE_ERROR bit to customize the system diagnostics for the requirements of the application.

Table 31. Bit Descriptions for the AFE_ERR_DISABLE Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	Reserved		Reserved.	0x0	R
11	AINN_UV		Undervoltage on AIN(–).	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
10	AINP_UV		Undervoltage on AIN(+).	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
9	AINN_OV		Overvoltage on AIN(–).	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
8	AINP_OV		Overvoltage on AIN(+).	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
7	I_EXC		RTD excitation current out of compliance.	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
6	I_COM		RTD compensation current out of compliance.	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
[5:3]	Reserved		Reserved.	0x0	R
2	FLD_PWR_OC		Output overcurrent in field power supply mode.	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
1	AIN_OC		Input overcurrent.	0x0	RW
		0	Alert flag is on.		
		1	Alert flag is off.		
0	Reserved		Reserved.	0x0	R

AFE_DETAIL_STATUS Register

Address: 0x7, Reset: 0x0000, Name: AFE_DETAIL_STATUS

The read only AFE_DETAIL_STATUS register can be used for detailed diagnostics and to monitor all error conditions in the high voltage analog input channel. Each error bit in this register is latched. Therefore, if an error condition occurs for even a short period of time, the error condition is captured by the error logic and indicated by the appropriate error bit until this register is read.

Table 32. Bit Descriptions for the AFE_DETAIL_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	Reserved		Reserved.	0x0	R
11	AINN_UV		Undervoltage on AIN(−).	0x0	R
		0	No error.		
		1	Error flag is set.		
10	AINP_UV		Undervoltage on AIN(+).	0x0	R
		0	No error.		
		1	Error flag is set.		
9	AINN_OV		Overvoltage on AIN(−).	0x0	R
		0	No error.		
		1	Error flag is set.		
8	AINP_OV		Overvoltage on AIN(+).	0x0	R
		0	No error.		
		1	Error flag is set.		
7	I_EXC		RTD excitation current out of compliance.	0x0	R
		0	No error.		
		1	Error flag is set.		
6	I_COM		RTD compensation current out of compliance.	0x0	R
		0	No error.		
		1	Error flag is set.		
[5:3]	Reserved		Reserved.	0x0	R
2	FLD_PWR_OC		Output overcurrent in field power supply mode.	0x0	R
		0	No error.		
		1	Error flag is set.		
1	AIN_OC		Input overcurrent.	0x0	R
		0	No error.		
		1	Error flag is set.		
0	Error		Error on high voltage channel.	0x0	R
		0	No error.		
		1	Error flag is set.		

AFE_CAL_DATA Register

Address: 0xC, Reset: 0x0XXX, Name: AFE_CAL_DATA

The read only AFE_CAL_DATA register contains the value of the gain correction coefficients for voltage mode. The gain coefficient is nine bits wide and uses offset binary coding. Bit 9 is a parity bit that is set so that the overall number of 1s in the register is an odd number. The gain error at each gain is measured during device production test, and the corresponding correction coefficient is stored in this register. The coefficient for each gain is accessed by first setting the gain bits to the required gain in the PGA_RTD_CTRL register (Address 0x5) and then reading this register.

Table 33. Bit Descriptions for the AFE_CAL_DATA Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:10]	Reserved		Reserved.	0x0	R
9	Parity		Parity bit.	0xX	R
		0	Even parity.		
		1	Odd parity.		
[8:0]	GAIN_CAL		Gain calibration data for voltage mode.	0xX	R

AFE_RSENSE_DATA Register

Address: 0xD, Reset: 0xXXXX, Name: AFE_RSENSE_DATA

The read only AFE_RSENSE_DATA register contains the value of the gain correction coefficient for current mode. The gain coefficient is 15 bits wide and uses offset binary coding. Bit 15 is a parity bit that is set so that the overall number of 1s in the register is an odd number. The gain error at a gain setting of 4 is measured during device production test, and the corresponding correction coefficient is stored in this register. The coefficient is accessed by first setting the GAIN_CH bits for a gain of 4 in the PGA_RTD_CTRL register (Address 0x5) and then reading this register.

Table 34. Bit Descriptions for the AFE_RSENSE_DATA Register

Bits	Bit Name	Settings	Description	Reset	Access
15	Parity		Parity bit.	0xX	R
		0	Even parity.		
		1	Odd parity.		
[14:0]	RSEN_CAL		Gain calibration data for current mode.	0xX	R

NO_PWR_DEFAULT_SEL Register

Address: 0xE, Reset: 0x0000, Name: NO_PWR_DEFAULT_SEL

When power is initially applied to the AD4110-1, the device operates in current input mode by default. The default mode of operation can be changed, as described in the Default Mode of Operation on Power-Up section.

Table 35. Bit Descriptions for the NO_PWR_DEFAULT_SEL Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
[7:0]	D_MODE		Change the default power-up mode (after setting the IMODE bit (Bit 1) in the AFE_CNTRL2 register at Address 0x4).	0x0	W

NO_PWR_DEFAULT_STATUS Register

Address: 0xF, Reset: 0x00XX, Name: NO_PWR_DEFAULT_STATUS

A read of the NO_PWR_DEFAULT_STATUS register indicates whether current mode or voltage mode is selected as the default mode of operation. If this register contains an even value, the default mode of operation is voltage mode. If the register contains an odd value, the default mode of operation is current mode. The default mode of operation of the AD4110-1 can be changed up to 100 times. The number of remaining changes to the default mode of operation is provided by the count bits (Bits[7:0]).

Table 36. Bit Descriptions for the NO_PWR_DEFAULT_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:9]	Reserved		Reserved.	0x0	R
8	COMM_ERR		Error when reading this register.	0x0	R
		0	No error.		
		1	This error flag is set if there was an error in the communication while reading this register. If this bit is set to 1, an error occurred, and the data read must be repeated to ensure that the read is accurate.		
[7:0]	Count		Remaining writes to set the default power-up mode. The default mode of operation of the AD4110-1 can be changed up to 100 times.	0xXX	R

ADC REGISTER MAP

Table 37. ADC Register Map

Reg	Register Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x0	ADC_STATUS	[7:0]	$\overline{\text{RDY}}$	ADC_ERR	CRC_ERR	Reserved			CHAN_ID		0x80	R
0x1	ADC_MODE	[15:8]	REF_EN	Reserved				Delay			0x0000	RW
		[7:0]	Reserved	Mode			CLK_SEL		Reserved			
0x2	ADC_INTERFACE	[15:8]	Reserved								0x0000	RW
		[7:0]	Reserved	DATA_STAT	Reserved		CRC_EN		Reserved	WL16		
0x3	ADC_CONFIG	[15:8]	Reserved			BI_UNIPOLAR	REFIN_BUFF		AIN_BUFF		0x1340	RW
		[7:0]	Reserved	BIT_6	REF_SEL		CHAN_EN_3	CHAN_EN_2	CHAN_EN_1	CHAN_EN_0		
0x4	Data	[23:16]	DATA[23:16]								0x000000	R
		[15:8]	DATA[15:8]									
		[7:0]	DATA[7:0]									
0x5	Filter	[15:8]	Reserved				EN_ENHANCEFILT	SEL_ENHANCEFILT			0x0500	RW
		[7:0]	Reserved	Order		ODR						
0x6	ADC_GPIO_CONFIG	[15:8]	Reserved				SYNC_EN	ERR_EN		Reserved	0x0800	RW
		[7:0]	Reserved									
0x7	ID	[15:8]	ID[15:8]								0x98DX	R
		[7:0]	ID[7:0]									
0x8	ADC_OFFSET0	[23:16]	OFFSET0[23:16]								0x800000	RW
		[15:8]	OFFSET0[15:8]									
		[7:0]	OFFSET0[7:0]									
0x9	ADC_OFFSET1	[23:16]	OFFSET1[23:16]								0x800000	RW
		[15:8]	OFFSET1[15:8]									
		[7:0]	OFFSET1[7:0]									
0xA	ADC_OFFSET2	[23:16]	OFFSET2[23:16]								0x800000	RW
		[15:8]	OFFSET2[15:8]									
		[7:0]	OFFSET2[7:0]									
0xB	ADC_OFFSET3	[23:16]	OFFSET3[23:16]								0x800000	RW
		[15:8]	OFFSET3[15:8]									
		[7:0]	OFFSET3[7:0]									
0xC	ADC_GAIN0	[23:16]	GAIN0[23:16]								0x5XXXX0	RW
		[15:8]	GAIN0[15:8]									
		[7:0]	GAIN0[7:0]									
0xD	ADC_GAIN1	[23:16]	GAIN1[23:16]								0x5XXXX0	RW
		[15:8]	GAIN1[15:8]									
		[7:0]	GAIN1[7:0]									
0xE	ADC_GAIN2	[23:16]	GAIN2[23:16]								0x5XXXX0	RW
		[15:8]	GAIN2[15:8]									
		[7:0]	GAIN2[7:0]									
0xF	ADC_GAIN3	[23:16]	GAIN3[23:16]								0x5XXXX0	RW
		[15:8]	GAIN3[15:8]									
		[7:0]	GAIN3[7:0]									

ADC REGISTER DESCRIPTIONS

ADC_STATUS Register

Address: 0x0, Reset: 0x80, Name: ADC_STATUS

The ADC_STATUS register is an 8-bit, read-only register that contains ADC and serial interface status information. The application can append the contents of this register to the data register by setting Bit 6 in the ADC_INTERFACE register (Address 0x2). When this option is selected, the contents of the ADC_STATUS register are read automatically with each ADC conversion result.

Table 38. Bit Descriptions for the ADC_STATUS Register

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{\text{RDY}}$		Data ready. The status of the $\overline{\text{RDY}}$ bit is output to the DOUT/$\overline{\text{RDY}}$ pin when $\overline{\text{CS}}$ is low and a register is not being read. This bit goes low after the ADC writes a new result to the data register. In ADC calibration modes, this bit goes low after the ADC writes the calibration result. $\overline{\text{RDY}}$ is brought high automatically by a read of the data register.	0x1	R
		0	New ADC data result is available.		
		1	Waiting for new data result.		
6	ADC_ERR		This bit by default indicates if an ADC overrange or underrange has occurred. The ADC result is clamped to 0xFFFFFF for overrange errors and 0x000000 for underrange errors. This bit is updated when the ADC result is written and is cleared at the next update after removing the overrange or underrange condition. Writing to the ADC_MODE register or asserting $\overline{\text{SYNC}}$ pin also clears this bit. This bit can also be used to indicate the status on the error pin if configured as an input (see the Error Pin section).	0x0	R
		0	No error.		
		1	Error.		
5	CRC_ERR		CRC checksum error. This bit is set when a CRC error occurs during a register write to the ADC Register Map. (For register reads, the host microcontroller determines whether a CRC error has occurred.) This bit is cleared by a read of this register.	0x0	R
		0	No error.		
		1	An error occurred during communication.		
[4:2]	Reserved		Reserved.	0x0	R
[1:0]	CHAN_ID		Channel ID of the last ADC result. These bits indicate the channel that was active for the ADC conversion whose result is currently in the data register. This value may differ from the channel that is currently being converted.	0x0	R
		00	Channel 0 (high voltage channel): AIN(+) − AIN(−).		
		01	Channel 1 (low voltage channel): AIN1(LV) − AIN2(LV).		
		10	Channel 2 (low voltage channel): AIN1(LV) − AINCOM(LV).		
		11	Channel 3 (low voltage channel): AIN2(LV) − AINCOM(LV).		

ADC_MODE Register

Address: 0x1, Reset: 0x0000, Name: ADC_MODE

The ADC_MODE register controls the conversion mode of the ADC, turns on the internal voltage reference, and selects the clock source for the ADC sampling. A write to this register resets the digital filter and the $\overline{\text{RDY}}$ bit in the ADC_STATUS register and starts a new conversion.

The application software must write to this register during the device initialization routine to set Bits[3:2] to 01. This write is required to ensure that the AFE and ADC are synchronized with the same clock.

Table 39. Bit Descriptions for the ADC_MODE Register

Bits	Bit Name	Settings	Description	Reset	Access
15	REF_EN		Internal voltage reference enable.	0x0	RW
		0	Disabled.		
		1	Enabled, buffered output to REFOUT pin.		
[14:11]	Reserved		Reserved.	0x0	R

Bits	Bit Name	Settings	Description	Reset	Access
[10:8]	Delay		Conversion delay. If the application switches through a sequence of channels for conversion by the ADC, a settling time is associated with each switched analog input. These bits allow the user to configure a delay that is added after a channel switch. This delay allows settling of the external circuitry before the ADC starts processing its input. The delay allows the data rate of the ADC to remain at the required update rate with only a minor impact on the resolution of the conversion result. The correct delay selection vs. the output data rate minimizes any effect on resolution. This function is not valid when rejecting 50 Hz/60 Hz interferers.	0x0	RW
		000	Off (no delay).		
		001	1 cycle (1 cycle = 8 µs).		
		010	4 cycles.		
		011	10 cycles.		
		100	25 cycles.		
		101	50 cycles.		
		110	125 cycles.		
		111	250 cycles.		
7	Reserved		Reserved.	0x0	R
[6:4]	Mode		ADC conversion mode. These bits control the operating mode of the ADC.	0x0	RW
		000	Continuous conversion. The ADC continually converts the selected input channel at the selected conversion rate, or sequences around channels if more than one channel is enabled.		
		001	Single conversion. This performs a single conversion of the selected channel or channels. The ADC returns to Standby mode on completion of the sequence.		
		010	Standby mode.		
		011	Power-down mode. All ADC blocks are powered down and registers lose their contents. The ADC can only enter power-down mode if the previous mode was set to standby mode. To exit power-down mode it is necessary to reset the SPI interface, see the Resetting the AD4110-1 section.		
		100	Reserved		
		101	Reserved		
		110	System offset (zero-scale) calibration. This mode performs an offset calibration using the applied analog input as the zero scale point. The calibration result is stored in the appropriate offset register for the channel and the ADC then enters standby mode. This calibration allows any offset error present in the full channel to be removed. Select only one channel at a time for an offset calibration. See the Autocalibration Modes section for a detailed description. Note that this calibration method is valid for one PGA gain setting and must be repeated if the PGA gain is changed.		
		111	System gain (full-scale) calibration. This mode performs a gain calibration using the applied analog input as the full-scale point. The calibration result is stored in the appropriate gain register for the channel and the ADC then enters standby mode. This calibration allows any gain error present in the full channel to be removed. Select only one channe at a time for a gain calibration. See the Autocalibration Modes section for a detailed description. Note that this calibration method is valid for one PGA gain setting and must be repeated if the PGA gain is changed.		
[3:2]	CLK_SEL		Clock source select. These bits select the ADC clock source.	0x0	RW
		00	Internal clock.		
		01	Internal clock connected to CLKIO pin (required for AFE).		
		10	External clock from CLKIO pin.		
		11	Reserved.		
[1:0]	Reserved		Reserved.	0x0	R

ADC_INTERFACE Register

Address: 0x2, Reset: 0x0000, Name: ADC_INTERFACE

The ADC_INTERFACE register is used to enable the CRC checksum mode on the ADC. To enable CRC checksum mode, Bits[3:2] in this register must be set, as well as Bits[14:13] in the AFE_CNTRL1 register (see Table 27). The ADC_INTERFACE register is also used to enable the appending of the ADC_STATUS register contents to the ADC conversion result and to set the conversion data length to 16 bits instead of the default 24 bits.

Table 40. Bit Descriptions for the ADC_INTERFACE Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:8]	Reserved		Reserved.	0x0	R
7	Reserved		Reserved.	0x0	R
6	DATA_STAT		Append status register contents to conversion result. When this bit is set, the contents of the ADC_STATUS register are appended to the data register when a conversion result is read. In this way, channel and status information is transmitted with the data. Using this option is the only way to ensure that the channel bits that are read from the status register correspond to the data in the data register.	0x0	RW
		0	Disabled.		
		1	Enabled.		
[5:4]	Reserved		Reserved.	0x0	R
[3:2]	CRC_EN		CRC checksum enable. These bits enable CRC protection of register reads and writes. CRC increases the number of bytes in the serial interface transfer by 1.	0x0	RW
		00	Disabled.		
		01	8-bit XOR checksum on reads, 8-bit CRC on writes.		
		10	8-bit CRC on reads and writes.		
		11	Reserved.		
1	Reserved		Reserved.	0x0	R
0	WL16		Data word length (24 or 16 bits). By default, the AD4110-1 generates 24-bit conversions. When this bit is set, the width of the data register is reduced to 16 bits, and all data conversions are rounded to 16 bits. After this bit is set to 1, the ADC result is not rounded to the correct word length immediately (the ADC is not reset by a write to the ADC_INTERFACE register). The first new ADC result is 16 bits wide.	0x0	RW
		0	Conversion result is 24 bits long.		
		1	Conversion result is 16 bits long.		

ADC_CONFIG Register

Address: 0x3, Reset: 0x1340, Name: ADC_CONFIG

The ADC_CONFIG register configures output coding of the ADC, as well as the reference and analog input buffers, and selects the reference source. This register is also used to enable and disable the channels. It is recommended to enable or disable the positive and negative REFIN_BUFF and AIN_BUFF buffers as a pair.

Table 41. Bit Descriptions for the ADC_CONFIG Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	Reserved		Reserved.	0x0	R
12	BI_UNIPOLAR		Unipolar or bipolar output coding.	0x1	RW
		0	Unipolar coded output (straight binary).		
		1	Bipolar coded output (offset binary).		
[11:10]	REFIN_BUFF		Reference input buffer configuration.	0x0	RW
		00	Disable input buffer.		
		01	Enable negative input buffer only.		
		10	Enable positive input buffer only.		
		11	Full buffer enabled.		

Bits	Bit Name	Settings	Description	Reset	Access
[9:8]	AIN_BUFF		Analog input buffer configuration.	0x3	RW
		00	Disable input buffer.		
		01	Enable negative input buffer only.		
		10	Enable positive input buffer only.		
		11	Full buffer enabled.		
7	Reserved		Reserved.	0x0	R
6	BIT_6		Set this bit to 1.	0x1	RW
[5:4]	REF_SEL		Reference source select. If the internal voltage reference is selected, the REF_EN bit (Bit 15) in the ADC_MODE register (Address 0x1) must also be set.	0x0	RW
		00	External voltage reference connected to REFIN(+)/REFIN(−) pins.		
		01	Reserved.		
		10	Internal 2.5 V reference.		
		11	AVDD5 and AGND.		
3	CHAN_EN_3		Enable Channel 3 (low voltage channel): AIN2(LV) − AINCOM(LV).	0x0	RW
		0	Disabled.		
		1	Enabled.		
2	CHAN_EN_2		Enable Channel 2 (low voltage channel): AIN1(LV) − AINCOM(LV).	0x0	RW
		0	Disabled.		
		1	Enabled.		
1	CHAN_EN_1		Enable Channel 1 (low voltage channel): AIN1(LV) − AIN2(LV).	0x0	RW
		0	Disabled.		
		1	Enabled.		
0	CHAN_EN_0		Enable Channel 0 (high voltage channel): AIN(+) − AIN(−). Channel 0 is enabled automatically when Bits[3:0] = 00.	0x0	RW
		0	Disabled.		
		1	Enabled.		

Data Register

Address: 0x4, Reset: 0x000000, Name: Data

The read-only data register contains the ADC conversion result. Reading the data register takes the $\overline{\text{RDY}}$ bit and the DOUT/$\overline{\text{RDY}}$ pin high. The ADC result can be read multiple times. However, after the $\overline{\text{RDY}}$ bit and the DOUT/$\overline{\text{RDY}}$ pin are brought high, it is not possible to determine whether another ADC result is imminent. The ADC does not write a new result to the data register if the data register is currently being read.

Table 42. Bit Descriptions for the Data Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	Data		ADC conversion result. If the DATA_STAT bit is set in the ADC_INTERFACE register, the contents of the ADC_STATUS register are appended to this register when it is read, making this a 32-bit register. If the WL16 bit is set in the ADC_INTERFACE register, this register is rounded to 16 bits.	0x0	R

Filter Register

Address: 0x5, Reset: 0x0500, Name: Filter

The filter register configures the ADC data rate and filter options. Writing to the filter register resets any active ADC conversion and restarts conversion at the first channel in the sequence. The AD4110-1 provides four filter registers that allow different output data rates to be selected for the high voltage channel and the three low voltage channels. These filter registers share the same memory address. Therefore, when the filter register is written to, the contents are copied to the filter register for each active channel selected by Bits[3:0] of the ADC_CONFIG register (see Table 41).

Table 43. Bit Descriptions for the Filter Register

Bits	Bit Name	Settings	Description		Reset	Access
[15:12]	Reserved		Reserved.		0x0	R
11	EN_ENHANCEFILT		Enable enhanced filters. Allows the application to optimize the rejection of 50 Hz and 60 Hz simultaneously while also reducing the settling time.		0x0	RW
		0	Disable enhanced 50 Hz/60 Hz filter.			
		1	Enable enhanced 50 Hz/60 Hz filter.			
[10:8]	SEL_ENHANCEFILT		Select enhanced filter mode for 50 Hz/60 Hz rejection.		0x5	RW
		000	Reserved.			
		001	Reserved.			
		010	ODR = 27.27 SPS, settling time = 36.7 ms.			
		011	ODR = 25 SPS, settling time = 40 ms.			
		100	ODR = 20.67 SPS, settling time = 48.4 ms.			
		101	ODR = 20 SPS, settling time = 50 ms.			
		110	ODR = 16.67 SPS, settling time = 60 ms.			
		111	Reserved.			
7	Reserved		Reserved.		0x0	R
[6:5]	Order		Filter order.		0x0	RW
		00	Sinc5 + sinc1 (fast settling filter).			
		01	Reserved.			
		10	Reserved.			
		11	Sinc3 filter.			
[4:0]	ODR		Output data rate.		0x0	RW
			Sinc3 Filter	**Sinc5 + Sinc1 Filter**		
		00000	125.0 kSPS (default setting)	125.0 kSPS (default setting)		
		00001	125.0 kSPS	125.0 kSPS		
		00010	62.5 kSPS	62.5 kSPS		
		00011	62.5 kSPS	62.5 kSPS		
		00100	31.25 kSPS	31.25 kSPS		
		00101	25.0 kSPS	25.0 kSPS		
		00110	15.625 kSPS	15.625 kSPS		
		00111	10.417 kSPS	10.390 kSPS		
		01000	5.0 kSPS	4.994 kSPS		
		01001	2.5 kSPS	2.498 kSPS		
		01010	1.0 kSPS	1.0 kSPS		
		01011	500 SPS	500 SPS		
		01100	400.6 SPS	395.5 SPS		
		01101	200 SPS	200 SPS		
		01110	100.2 SPS	100.2 SPS		
		01111	60 SPS	59.87 SPS		
		10000	50 SPS	49.92 SPS		
		10001	20.0 SPS	20.0 SPS		
		10010	16.7 SPS	16.7 SPS		
		10011	10.0 SPS	10.0 SPS		
		10100	5.0 SPS	5.0 SPS		

ADC_GPIO_CONFIG Register

Address: 0x6, Reset: 0x0800, Name: ADC_GPIO_CONFIG

The ADC_GPIO_CONFIG register controls the general-purpose I/O pins of the ADC: $\overline{\text{SYNC}}$ and $\overline{\text{ERR}}$.

Table 44. Bit Descriptions for the ADC_GPIO_CONFIG Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	Reserved		Reserved.	0x0	R
11	SYNC_EN		$\overline{\text{SYNC}}$ pin enable. Setting this bit allows the $\overline{\text{SYNC}}$ pin to hold the ADC or filter in reset. This pin can be used to synchronize the conversion start on multiple devices.	0x1	RW
		0	Disabled.		
		1	Enabled.		
[10:9]	ERR_EN		$\overline{\text{ERR}}$ pin mode select.	0x0	RW
		00	Disabled.		
		01	Input. Logic OR of the $\overline{\text{ERR}}$ pin and the internal ADC error bits with the result available in the ADC_ERR bit of the ADC_STATUS register. This mode can be used to combine the AFE and ADC errors into the ADC_ERR bit.		
		10	Output (open-drain, active low).		
		11	Reserved.		
8	Reserved		Reserved.	0x0	R
[7:0]	Reserved		Reserved.	0x0	R

ID Register

Address: 0x7, Reset: 0x98DX, Name: ID

The read only ID register returns the 16-bit device ID. For the AD4110-1, this value is 0x98DX.

Table 45. Bit Descriptions for the ID Register

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ID		Device product identification number.	0x98DX	R
		0x98DX	AD4110-1. (where X is the ADC silicon revision).		

ADC_OFFSET0 Register

Address: 0x8, Reset: 0x800000, Name: ADC_OFFSET0

The ADC_OFFSET0 register configures the offset for Channel 0 (high voltage channel, AIN(+) − AIN(−) inputs).

Table 46. Bit Descriptions for the ADC_OFFSET0 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET0		Offset data value.	0x800000	RW

ADC_OFFSET1 Register

Address: 0x9, Reset: 0x800000, Name: ADC_OFFSET1

The ADC_OFFSET1 register configures the offset for Channel 1 (low voltage channel, AIN1(LV) − AIN2(LV) inputs).

Table 47. Bit Descriptions for the ADC_OFFSET1 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET1		Offset data value.	0x800000	RW

ADC_OFFSET2 Register

Address: 0xA, Reset: 0x800000, Name: ADC_OFFSET2

The ADC_OFFSET2 register configures the offset for Channel 2 (low voltage channel, AIN1(LV) − AINCOM(LV) inputs).

Table 48. Bit Descriptions for the ADC_OFFSET2 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET2		Offset data value.	0x800000	RW

ADC_OFFSET3 Register

Address: 0xB, Reset: 0x800000, Name: ADC_OFFSET3

The ADC_OFFSET3 register configures the offset for Channel 3 (low voltage channel, AIN2(LV) − AINCOM(LV) inputs).

Table 49. Bit Descriptions for the ADC_OFFSET3 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	OFFSET3		Offset data value.	0x800000	RW

ADC_GAIN0 Register

Address: 0xC, Reset: 0x5XXXX0, Name: ADC_GAIN0

The ADC_GAIN0 register configures the gain for Channel 0 (high voltage channel, AIN(+) − AIN(−) input).

Table 50. Bit Descriptions for the ADC_GAIN0 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN0		Gain data value.	0x5XXXX0	RW

ADC_GAIN1 Register

Address: 0xD, Reset: 0x5XXXX0, Name: ADC_GAIN1

The ADC_GAIN1 register configures the gain for Channel 1 (low voltage channel, AIN1(LV) − AIN2(LV) input).

Table 51. Bit Descriptions for the ADC_GAIN1 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN1		Gain data value.	0x5XXXX0	RW

ADC_GAIN2 Register

Address: 0xE, Reset: 0x5XXXX0, Name: ADC_GAIN2

The ADC_GAIN2 register configures the gain for Channel 2 (low voltage channel, AIN1(LV) − AINCOM(LV) input).

Table 52. Bit Descriptions for the ADC_GAIN2 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN2		Gain data value.	0x5XXXX0	RW

ADC_GAIN3 Register

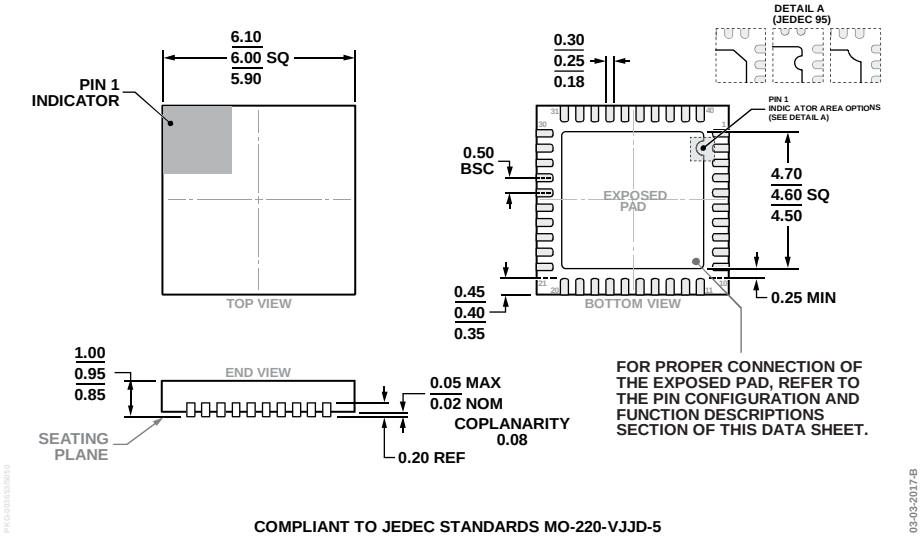
Address: 0xF, Reset: 0x5XXXX0, Name: ADC_GAIN3

The ADC_GAIN3 register configures the gain for Channel 3 (low voltage channel, AIN2(LV) − AINCOM(LV) input).

Table 53. Bit Descriptions for the ADC_GAIN3 Register

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	GAIN3		Gain data value.	0x5XXXX0	RW

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-5

Figure 75. 40-Lead Lead Frame Chip Scale Package [LFCSP]
6 mm × 6 mm Body and 0.95 mm Package Height
(CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD4110-1BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
AD4110-1BCPZ-RL	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15
AD4110-1BCPZ-RL7	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP]	CP-40-15

[1] Z = RoHS Compliant Part.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

EVAL-AD4110-1SDZ AD4110-1BCPZ AD4110-1BCPZ-RL AD4110-1BCPZ-RL7