3.1V_{IN} to 32V_{IN} Isolated µModule DC/DC Converter

FEATURES

- **Complete Switch Mode Power Supply**
- **725VDC Isolation**
- **Wide Input Voltage Range: 3.1V to 32V**
- **Up to 440mA Output Current (V_{OUT} = 2.5V)**
- **2.5V to 12V Output Voltage**
- Current Mode Control
- Programmable Soft-Start
- User Configurable Undervoltage Lockout
- SnPb or RoHS Compliant Finish
- Low Profile (11.25mm × 9mm × 4.92mm) Surface Mount BGA Package

APPLICATIONS

- Industrial Sensors
- Industrial Switches
- Ground Loop Mitigation

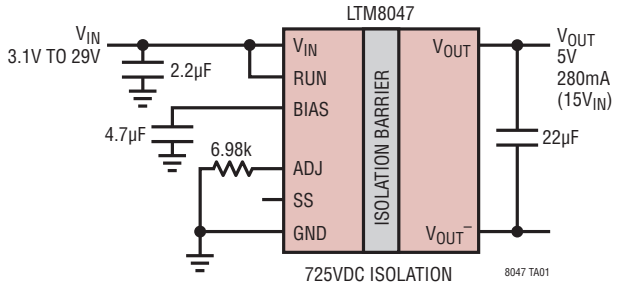
DESCRIPTION

The LTM®8047 is an isolated flyback µModule DC/DC converter. The LTM8047 has an isolation rating of 725VDC. For a similar product with LDO post regulator, see the LTM8048. Included in the package are the switching controller, power switches, transformer, and all support components. Operating over an input voltage range of 3.1V to 32V, the LTM8047 supports an output voltage range of 2.5V to 12V, set by a single resistor. Only output, input, and bypass capacitors are needed to finish the design. Other components may be used to control the soft-start control and biasing.

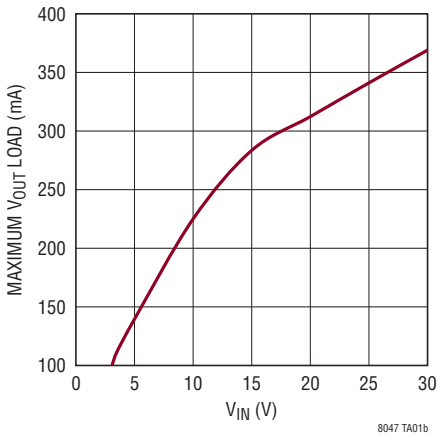
The LTM8047 is packaged in a thermally enhanced, compact (11.25mm × 9mm × 4.92mm) over-molded ball grid array (BGA) package suitable for automated assembly by standard surface mount equipment. The LTM8047 is available with SnPb (BGA) or RoHS compliant terminal finish.

TYPICAL APPLICATION

725V DC Isolated Low Noise µModule Regulator



Maximum Load vs V_{IN}

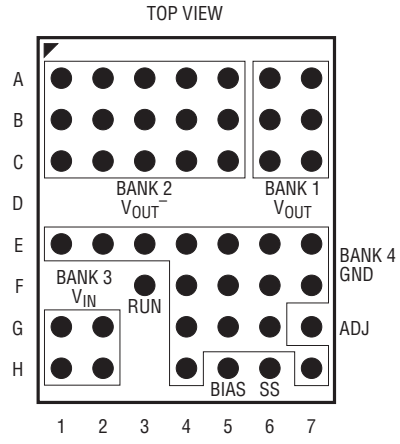


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, RUN, BIAS 32V
ADJ, SS 5V
V_{OUT} Relative to V_{OUT}^- 16V
(V_{IN} – GND) + (V_{OUT} – V_{OUT}^-) 36V
BIAS Above V_{IN} 0.1V
GND to V_{OUT}^- Isolation (Note 2) 725VDC
Maximum Internal Temperature (Note 3) ..... 125°C
Maximum Solder Temperature ..... 250°C

PIN CONFIGURATION



BGA PACKAGE
45-LEAD (11.25mm × 9mm × 4.92mm)

T_{JMAX} = 125°C, θ_{JA} = 16°C/W, $\theta_{JCbottom}$ = 4.1°C/W, θ_{JCtop} = 15°C/W, θ_{JB} = 4°C/W
WEIGHT = 1.1g, θ VALUES DETERMINED PER JEDEC 51-9, 51-12

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 3)
		DEVICE	CODE			
LTM8047EY#PBF	SAC305 (RoHS)	LTM8047Y	e1	BGA	3	–40°C to 125°C
LTM8047IY#PBF	SAC305 (RoHS)	LTM8047Y	e1	BGA	3	–40°C to 125°C
LTM8047MPY#PBF	SAC305 (RoHS)	LTM8047Y	e1	BGA	3	–55°C to 125°C
LTM8047MPY	SnPb (63/37)	LTM8047Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, RUN = 12V (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input DC Voltage	BIAS = V_{IN}	●			3.1	V
V_{OUT} DC Voltage	R_{ADJ} = 12.4k R_{ADJ} = 6.98k R_{ADJ} = 3.16k	 ● 	 4.75 	2.5 5 12	 5.25 	V V V
V_{IN} Quiescent Current	V_{RUN} = 0V Not Switching	 	 	 850	1 	µA µA
V_{OUT} Line Regulation	6V ≤ V_{IN} ≤ 31V, I_{OUT} = 0.15A			1.7		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, RUN = 12V (Note 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT} Load Regulation	0.05A ≤ I_{OUT} ≤ 0.2A			1.5		%
V_{OUT} Ripple (RMS)	I_{OUT} = 0.1A			20		mV
Input Short Circuit Current	V_{OUT} Shorted			30		mA
RUN Pin Input Threshold	RUN Pin Rising		1.18	1.24	1.30	V
RUN Pin Current	V_{RUN} = 1V V_{RUN} = 1.3V			2.5 0.1		µA µA
SS Threshold				0.7		V
SS Sourcing Current	SS = 0V			–10		µA
BIAS Current	V_{IN} = 12V, BIAS = 5V, I_{LOAD1} = 100mA			8		mA
Minimum BIAS Voltage (Note 4)	I_{LOAD1} = 100mA				3.1	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

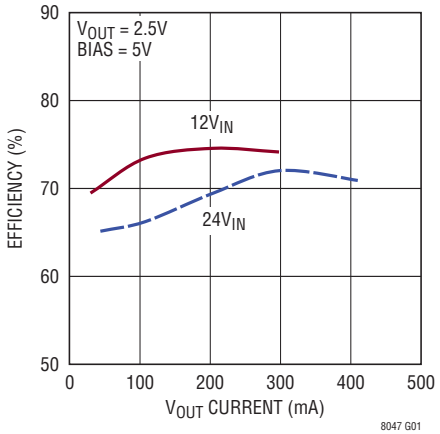
Note 2: The LTM8047 isolation is tested at 725VDC for one second in each polarity.

Note 3: The LTM8047E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C internal temperature range are assured by design, characterization and correlation with statistical process controls. LTM8047I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. The LTM8047MP is guaranteed to meet specifications over the full –55°C to 125°C internal operating temperature range. Note that the maximum internal temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

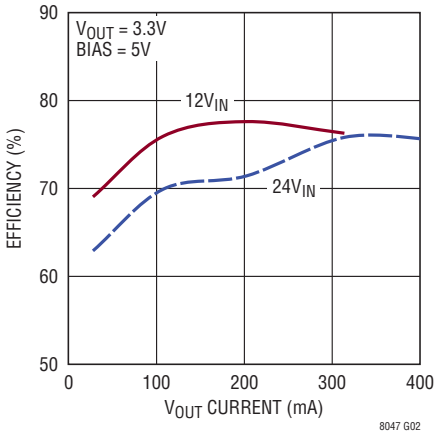
Note 4: This is the BIAS pin voltage at which the internal circuitry is powered through the BIAS pin and not the integrated regulator. See BIAS Pin Considerations for details.

TYPICAL PERFORMANCE CHARACTERISTICS

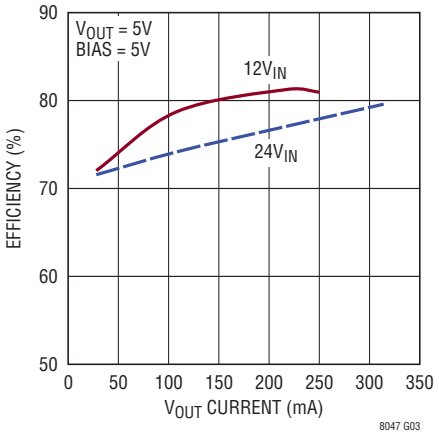
Efficiency vs Load



Efficiency vs Load

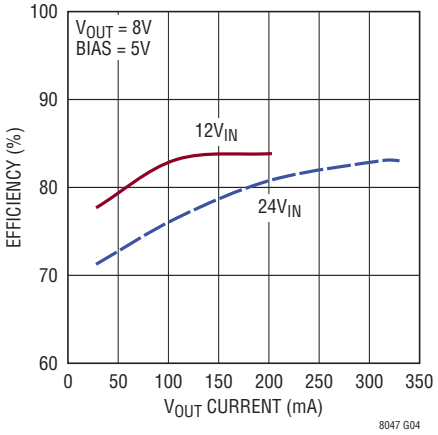


Efficiency vs Load

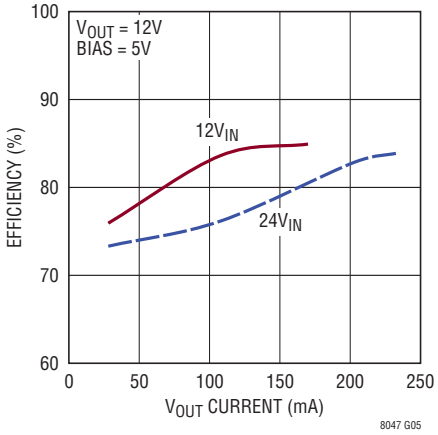


TYPICAL PERFORMANCE CHARACTERISTICS

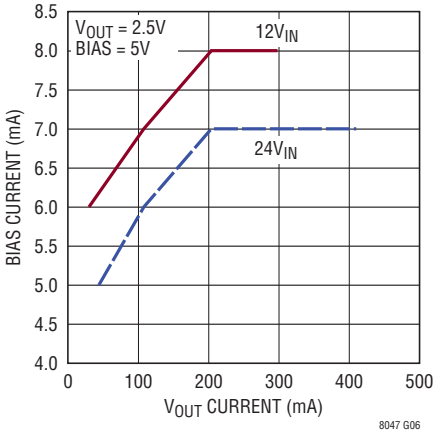
Efficiency vs Load



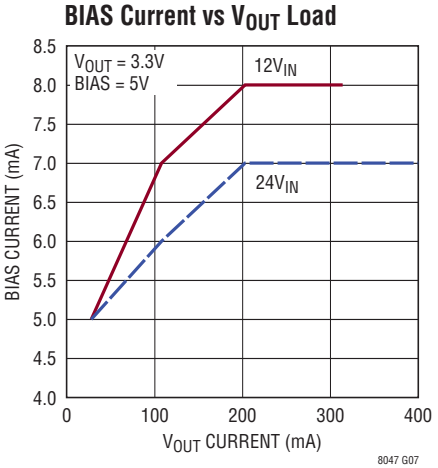
Efficiency vs Load



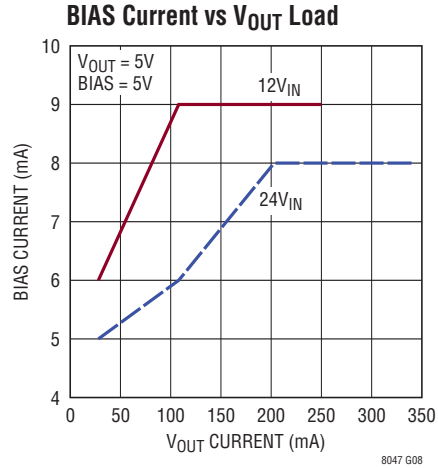
BIAS Current vs V_{OUT} Load



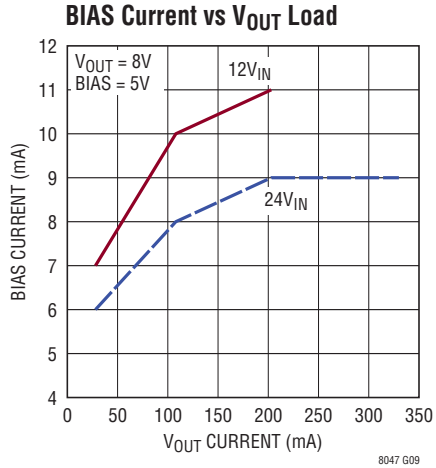
BIAS Current vs V_{OUT} Load



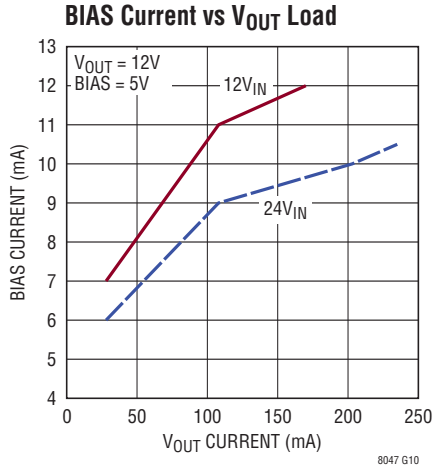
BIAS Current vs V_{OUT} Load



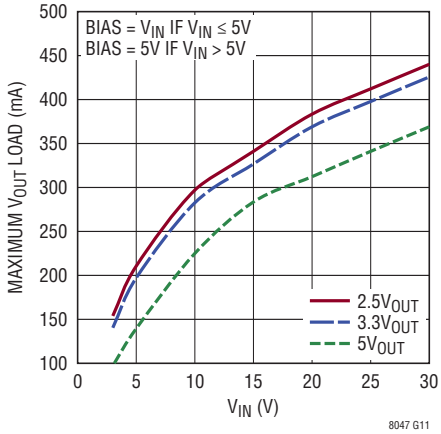
BIAS Current vs V_{OUT} Load



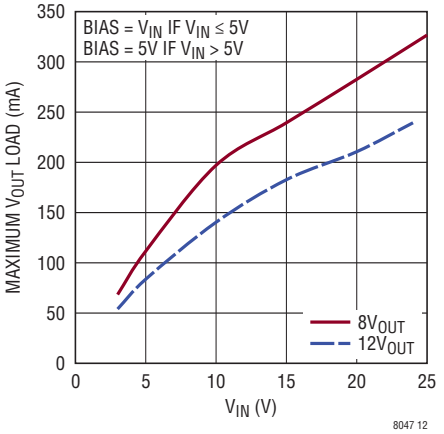
BIAS Current vs V_{OUT} Load



Maximum Load vs V_{IN}

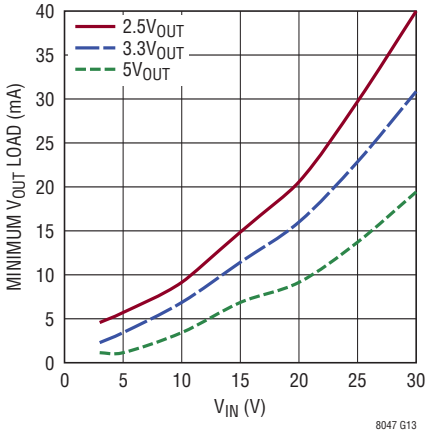


Maximum Load vs V_{IN}

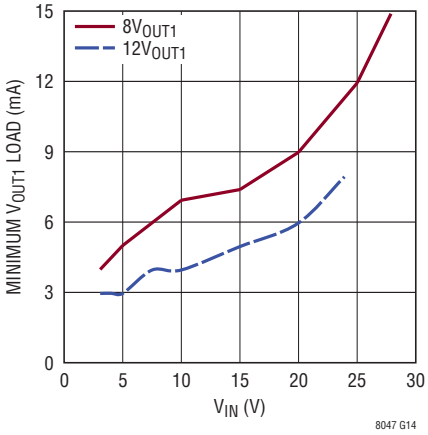


TYPICAL PERFORMANCE CHARACTERISTICS

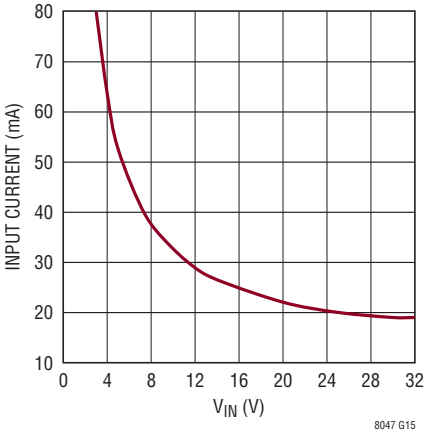
Minimum Load vs V_{IN}



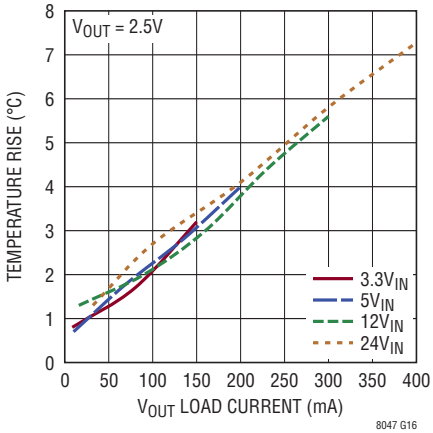
Minimum Load vs V_{IN}



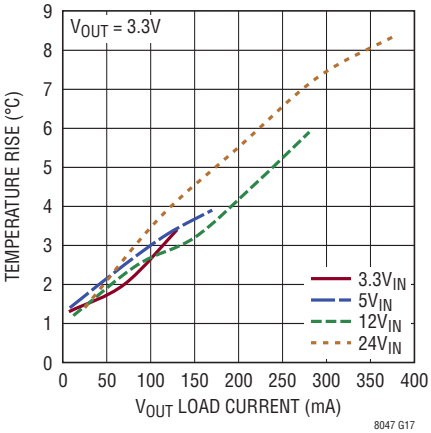
Input Current vs V_{IN} V_{OUT} Shorted



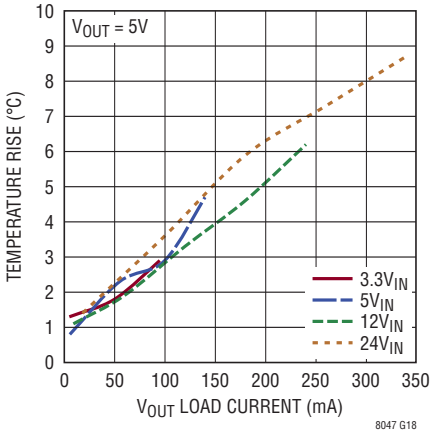
Junction Temperature Rise vs Load Current



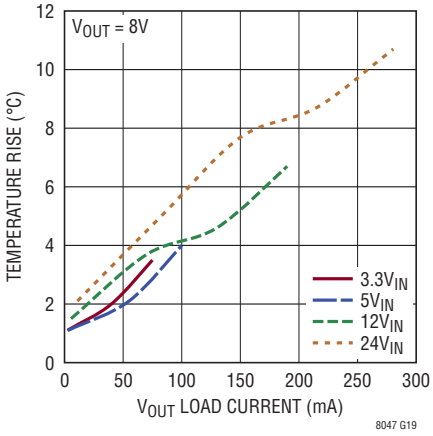
Junction Temperature Rise vs Load Current



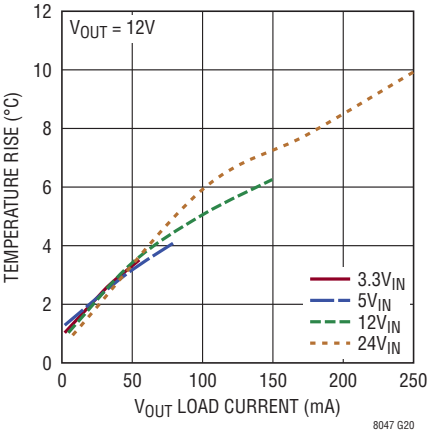
Junction Temperature Rise vs Load Current



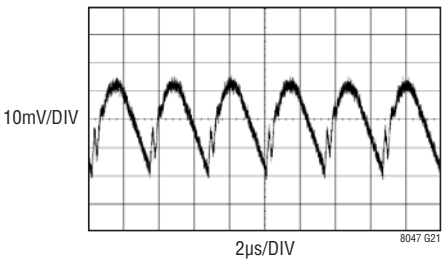
Junction Temperature Rise vs Load Current



Junction Temperature Rise vs Load Current



Output Noise and Ripple



$12V_{IN}$, $5V_{OUT}$ at 250mA
0.1µF 250V SAFETY CAPACITOR APPLIED
BETWEEN GND AND V_{OUT}^-

PIN FUNCTIONS

V_{OUT} (Bank 1): V_{OUT} and V_{OUT}^- comprise the isolated output of the LTM8047 flyback stage. Apply an external capacitor between V_{OUT} and V_{OUT}^-. Do not allow V_{OUT}^- to exceed V_{OUT}.

V_{OUT}^- (Bank 2): V_{OUT}^- is the return for V_{OUT}. V_{OUT} and V_{OUT}^- comprise the isolated output of the LTM8047. In most applications, the bulk of the heat flow out of the LTM8047 is through the GND and V_{OUT}^- pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details. Apply an external capacitor between V_{OUT} and V_{OUT}^-.

GND (Bank 4): This is the primary side local ground of the LTM8047 primary. In most applications, the bulk of the heat flow out of the LTM8047 is through the GND and V_{OUT}^- pads, so the printed circuit design has a large impact on the thermal performance of the part. See the PCB Layout and Thermal Considerations sections for more details.

V_{IN} (Bank 3): V_{IN} supplies current to the LTM8047's internal regulator and to the integrated power switch. These pins must be locally bypassed with an external, low ESR capacitor.

RUN (Pin F3): A resistive divider connected to V_{IN} and this pin programs the minimum voltage at which the LTM8047 will operate. Below 1.24V, the LTM8047 does not deliver power to the secondary. Above 1.24V, power will be delivered to the secondary and 10µA will be fed into the SS pin. When RUN is less than 1.24V, the pin draws 2.5µA, allowing for a programmable hysteresis. Do not allow a negative voltage (relative to GND) on this pin.

ADJ (Pin G7): Apply a resistor from this pin to GND to set the output voltage, using the recommended value given in Table 1. If Table 1 does not list the desired V_{OUT} value, the equation

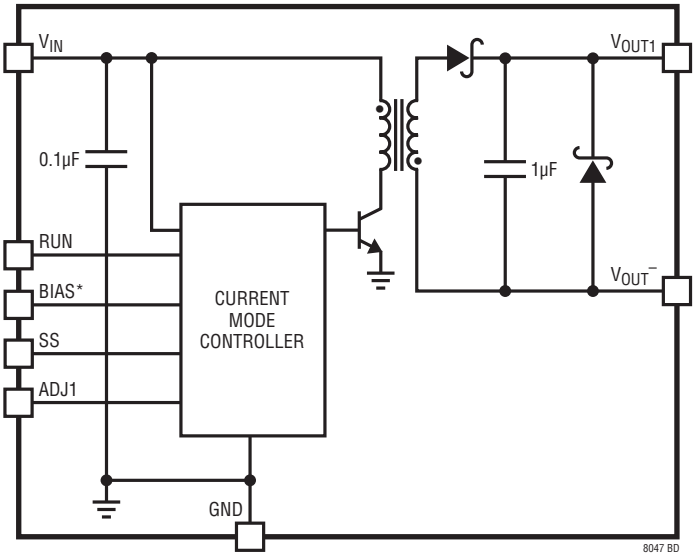
$$R_{ADJ} = 28.4\left(V_{OUT}^{-0.879}\right)k\Omega$$

may be used to approximate the value. To the seasoned designer, this exponential equation may seem unusual. The equation is exponential due to non-linear current sources that are used to temperature compensate the output regulation.

BIAS (Pin H5): This pin supplies the power necessary to operate the LTM8047. It must be locally bypassed with a low ESR capacitor of at least 4.7µF. Do not allow this pin voltage to rise above V_{IN}.

SS (Pin H6): Place a soft-start capacitor here to limit inrush current and the output voltage ramp rate. Do not allow a negative voltage (relative to GND) on this pin.

BLOCK DIAGRAM



*DO NOT ALLOW BIAS VOLTAGE TO BE ABOVE V_{IN}

OPERATION

The LTM8047 is a stand-alone isolated flyback switching DC/DC power supply that can deliver up to 440mA of output current. This module provides a regulated output voltage programmable via one external resistor from 2.5V to 12V. The input voltage range of the LTM8047 is 3.1V to 32V. Given that the LTM8047 is a flyback converter, the output current depends upon the input and output voltages, so make sure that the input voltage is high enough to support the desired output voltage and load current. The Typical Performance Characteristics section gives several graphs of the maximum load versus V_{IN} for several output voltages.

A simplified block diagram is given. The LTM8047 contains a current mode controller, power switching element, power transformer, power Schottky diode, a modest amount of input and output capacitance.

The LTM8047 has a galvanic primary to secondary isolation rating of 725VDC. This is verified by applying 725VDC between the primary to secondary for 1 second and then applying –725VDC for 1 second. For details please refer to the Isolation and Working Voltage section.

An internal regulator provides power to the control circuitry. The bias regulator normally draws power from the V_{IN} pin, but if the BIAS pin is connected to an external voltage higher than 3.1V, bias power will be drawn from the external source, improving efficiency. V_{BIAS} must not exceed V_{IN}. The RUN pin is used to turn on or off the LTM8047, disconnecting the output and reducing the input current to 1µA or less.

The LTM8047 is a variable frequency device. For a fixed input and output voltage, the frequency increases as the load increases. For light loads, the current through the internal transformer may be discontinuous.

APPLICATIONS INFORMATION

For most applications, the design process is straightforward, summarized as follows:

1. Look at Table 1 and find the row that has the desired input range and output voltage.
2. Apply the recommended C_{IN}, C_{OUT} and R_{ADJ}.
3. Connect BIAS as indicated, or tie to an external source up to 15V or V_{IN}, whichever is less.

While these component combinations have been tested for proper operation, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions. Bear in mind that the maximum output current may be limited by junction temperature, the relationship between the input and output voltage magnitude and polarity and other factors. Please refer to the graphs in the Typical Performance Characteristics section for guidance.

Capacitor Selection Considerations

The C_{IN} and C_{OUT} capacitor values in Table 1 are the minimum recommended values for the associated operating conditions. Applying capacitor values below those indicated in Table 1 is not recommended, and may result in undesirable operation. Using larger values is generally acceptable, and can yield improved dynamic response, if it is necessary. Again, it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental conditions.

Ceramic capacitors are small, robust and have very low ESR. However, not all ceramic capacitors are suitable. X5R and X7R types are stable over temperature and applied voltage and give dependable service. Other types, including Y5V and Z5U have very large temperature and voltage coefficients of capacitance. In an application circuit they may have only a small fraction of their nominal capacitance resulting in much higher output voltage ripple than expected.

A final precaution regarding ceramic capacitors concerns the maximum input voltage rating of the LTM8047. A ceramic input capacitor combined with trace or cable inductance forms a high-Q (underdamped) tank circuit. If the LTM8047 circuit is plugged into a live supply, the input voltage can ring to much higher than its nominal value, possibly exceeding the device's rating. This situation is easily avoided; see the Hot-Plugging Safely section.

LTM8047 Table 1. Recommended Component Values and Configuration for Specific V_{OUT} Voltages (T_A = 25°C)

V_{IN}	V_{OUT}	V_{BIAS}	C_{IN}	C_{OUT}	R_{ADJ}
3.1V to 32V	2.5V	3.1V to 15V or Open	2.2µF, 50V, 1206	100µF, 6.3V, 1210	12.4k
3.1V to 32V	3.3V	3.1V to 15V or Open	2.2µF, 50V, 1206	100µF, 6.3V, 1210	10k
3.1V to 29V	5V	3.1V to 15V or Open	2.2µF, 50V, 1206	22µF, 16V, 1210	6.98k
3.1V to 26V	8V	3.1V to 15V or Open	2.2µF, 50V, 1206	22µF, 10V, 1206	4.53k
3.1V to 24V	12V	3.1V to 15V or Open	2.2µF, 25V, 0805	10µF, 16V, 1210	3.16k/12pF*
9V to 15V	2.5V	V_{IN}	2.2µF, 50V, 1206	100µF, 6.3V, 1210	12.4k
9V to 15V	3.3V	V_{IN}	2.2µF, 50V, 1206	47µF, 6.3V, 1210	10k
9V to 15V	5V	V_{IN}	2.2µF, 50V, 1206	22µF, 16V, 1210	6.98k
9V to 15V	8V	V_{IN}	2.2µF, 50V, 1206	22µF, 10V, 1206	4.53k
9V to 15V	12V	V_{IN}	2.2µF, 25V, 0805	10µF, 16V, 1210	3.16k
18V to 32V	2.5V	3.1V to 15V or Open	2.2µF, 50V, 1206	100µF, 6.3V, 1210	12.4k
18V to 32V	3.3V	3.1V to 15V or Open	2.2µF, 50V, 1206	47µF, 6.3V, 1210	10k
18V to 29V	5V	3.1V to 15V or Open	2.2µF, 50V, 1206	22µF, 16V, 1210	6.98k
18V to 26V	8V	3.1V to 15V or Open	2.2µF, 50V, 1206	22µF, 10V, 1206	4.53k
18V to 24V	12V	3.1V to 15V or Open	2.2µF, 50V, 1206	10µF, 16V, 1210	3.16k/12pF*

Note: Do not allow BIAS to exceed V_{IN}, a bulk input capacitor is required.
*Connect 3.16k in parallel with 12pF from ADJ to GND.

APPLICATIONS INFORMATION

BIAS Pin Considerations

The BIAS pin is the output of an internal linear regulator that powers the LTM8047's internal circuitry. It is set to 3V and must be decoupled with a low ESR capacitor of at least 4.7µF. The LTM8047 will run properly without applying a voltage to this pin, but will operate more efficiently and dissipate less power if a voltage greater than 3.1V is applied. At low V_{IN}, the LTM8047 will be able to deliver more output current if BIAS is 3.1V or greater. Up to 40V may be applied to this pin, but a high BIAS voltage will cause excessive power dissipation in the internal circuitry. For applications with an input voltage less than 15V, the BIAS pin is typically connected directly to the V_{IN} pin. For input voltages greater than 15V, it is preferred to leave the BIAS pin separate from the V_{IN} pin, either powered from a separate voltage source or left running from the internal regulator. This has the added advantage of keeping the physical size of the BIAS capacitor small. Do not allow BIAS to rise above V_{IN}.

Soft-Start

For many applications, it is necessary to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot by applying a capacitor from SS to GND. When the LTM8047 is enabled, whether from V_{IN} reaching a sufficiently high voltage or RUN being pulled high, the LTM8047 will source approximately 10µA out of the SS pin. As this current gradually charges the capacitor from SS to GND, the LTM8047 will correspondingly increase the power delivered to the output, allowing for a graceful turn-on ramp.

Isolation and Working Voltage

The LTM8047 isolation is 100% hi-pot tested by tying all of the primary pins together, all of the secondary pins together and subjecting the two resultant circuits to a differential of 725VDC for one second and then –725VDC for one second. This establishes the isolation voltage rating of the LTM8047 component, and is most often used to satisfy component safety specifications issued by agencies such as UL, TUV, CSA and others.

The isolation rating of the LTM8047 is not the same as the working or operational voltage that the application will experience. This is subject to the application's power source, operating conditions, the industry where the end product is used and other factors that dictate design requirements such as the gap between copper planes, traces and component pins on the printed circuit board, as well as the type of connector that may be used. To maximize the allowable working voltage, the LTM8047 has a row of solder balls removed to facilitate the printed circuit board design. The ball to ball pitch is 1.27mm, and the typical ball diameter is 0.78mm. Accounting for the missing row and the ball diameter, the printed circuit board may be designed for a metal-to-metal separation of up to 1.76mm. This may have to be reduced somewhat to allow for tolerances in solder mask or other printed circuit board design rules.

To reiterate, the manufacturer's isolation voltage rating and the required operational voltage are often different numbers. In the case of the LTM8047, the isolation voltage rating is established by 100% hi-pot testing. The working or operational voltage is a function of the end product and its system level specifications. The actual required operational voltage is often smaller than the manufacturer's isolation rating.

For those situations where information about the spacing of LTM8047 internal circuitry is required, the minimum metal to metal separation of the primary and secondary is 0.44mm.

ADJ and Line Regulation

For V_{OUT} greater than 8V, a capacitor connected from ADJ to GND improves line regulation. Figure 1 shows the effect of three capacitance values applied to ADJ for a load of 15mA. No capacitance has poor line regulation, while 12pF has improved line regulation. As the capacitance increases, the line regulation begins to degrade again, but in the opposite direction as having too little capacitance. Furthermore, too much capacitance from ADJ to GND may increase the minimum load required for proper regulation.

APPLICATIONS INFORMATION

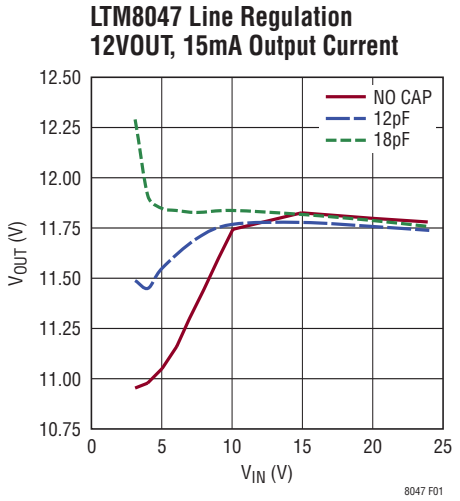


Figure 1. For higher output voltages, the LTM8047 requires some capacitance from ADJ to GND for proper line regulation

V_{OUT} to V_{OUT}^- Reverse Voltage

The LTM8047 cannot tolerate a reverse voltage from V_{OUT} to V_{OUT}^- during operation. If V_{OUT}^- raises above V_{OUT} during operation, the LTM8047 may be damaged. To protect against this condition, a low forward drop power Schottky diode has been integrated into the LTM8047, anti-parallel to V_{OUT}/V_{OUT}^-. This can protect the output against many reverse voltage faults. Reverse voltage faults can be both steady state and transient. An example of a steady state voltage reversal is accidentally misconnecting a powered LTM8047 to a negative voltage source. An example of transient voltage reversals is a momentary connection to a negative voltage. It is also possible to achieve a V_{OUT} reversal if the load is short-circuited through a long cable. The inductance of the long cable forms an LC tank circuit with the V_{OUT} capacitance, which drives V_{OUT} negative. Avoid these conditions.

PCB Layout

Most of the headaches associated with PCB layout have been alleviated or even eliminated by the high level of integration of the LTM8047. The LTM8047 is nevertheless a switching power supply, and care must be taken to minimize electrical noise to ensure proper operation. Even with the high level of integration, you may fail to achieve specified operation with a haphazard or poor layout. See Figure 2 for a suggested layout. Ensure that the grounding and heat sinking are acceptable.

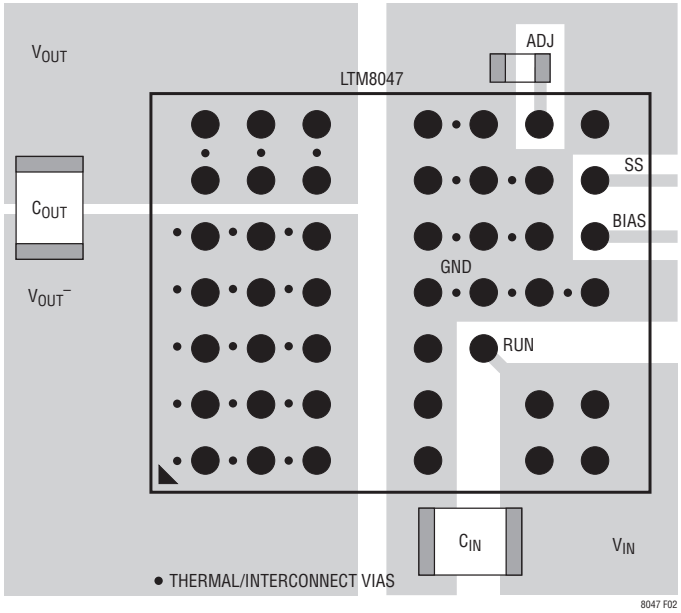


Figure 2. Layout Showing Suggested External Components, Planes and Thermal Vias

A few rules to keep in mind are:

1. Place the R_{ADJ} resistor as close as possible to its respective pin.
2. Place the C_{IN} capacitor as close as possible to the V_{IN} and GND connections of the LTM8047.
3. Place the C_{OUT} capacitor as close as possible to V_{OUT} and V_{OUT}^-.
4. Place the C_{IN} and C_{OUT} capacitors such that their ground current flow directly adjacent or underneath the LTM8047.
5. Connect all of the GND connections to as large a copper pour or plane area as possible on the top layer. Avoid breaking the ground connection between the external components and the LTM8047.
6. Use vias to connect the GND copper area to the board's internal ground planes. Liberally distribute these GND vias to provide both a good ground connection and thermal path to the internal planes of the printed circuit board. Pay attention to the location and density of the thermal vias in Figure 2. The LTM8047 can benefit from the heat sinking afforded by vias that connect to internal GND planes at these locations, due to their proximity to internal power handling components. The optimum

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number of thermal vias depends upon the printed circuit board design. For example, a board might use very small via holes. It should employ more thermal vias than a board that uses larger holes.

The printed circuit board construction has an impact on the isolation performance of the end product. For example, increased trace and layer spacing, as well as the choice of core and prepreg materials (such as using polyimide versus FR4) can significantly affect the isolation withstand of the end product.

Hot-Plugging Safely

The small size, robustness and low impedance of ceramic capacitors make them an attractive option for the input bypass capacitor of the LTM8047. However, these capacitors can cause problems if the LTM8047 is plugged into a live supply (see Linear Technology Application Note 88 for a complete discussion). The low loss ceramic capacitor combined with stray inductance in series with the power source forms an underdamped tank circuit, and the voltage at the V_{IN} pin of the LTM8047 can ring to more than twice the nominal input voltage, possibly exceeding the LTM8047's rating and damaging the part. If the input supply is poorly controlled or the user will be plugging the LTM8047 into an energized supply, the input network should be designed to prevent this overshoot. This can be accomplished by installing a small resistor in series to V_{IN}, but the most popular method of controlling input voltage overshoot is adding an electrolytic bulk capacitor to V_{IN}. This capacitor's relatively high equivalent series resistance damps the circuit and eliminates the voltage overshoot. The extra capacitor improves low frequency ripple filtering and can slightly improve the efficiency of the circuit, though it can be a large component in the circuit.

Thermal Considerations

The LTM8047 output current may need to be derated if it is required to operate in a high ambient temperature. The amount of current derating is dependent upon the input voltage, output power and ambient temperature. The temperature rise curves given in the Typical Performance Characteristics section can be used as a guide. These curves were generated by the LTM8047 mounted to a 58cm^2 4-layer FR4 printed circuit board. Boards of other sizes and layer count can exhibit different thermal behavior, so it is incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

For increased accuracy and fidelity to the actual application, many designers use FEA to predict thermal performance. To that end, the Pin Configuration section of the data sheet typically gives four thermal coefficients:

θ_{JA}: Thermal resistance from junction to ambient

$\theta_{JCbottom}$: Thermal resistance from junction to the bottom of the product case

θ_{JCtop}: Thermal resistance from junction to top of the product case

θ_{JB}: Thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased as follows:

θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as still air although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

$\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule converter, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient envi-

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ronment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule converter are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule converter and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two-sided, two-layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule converter. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature vs load graphs given in the product's data sheet. The only appropriate way to use the coefficients is when running a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 3.

The blue resistances are contained within the µModule converter, and the green are outside.

The die temperature of the LTM8047 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM8047. The bulk of the heat flow out of the LTM8047 is through the bottom of the module and the BGA pads into the printed circuit board. Consequently a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions.

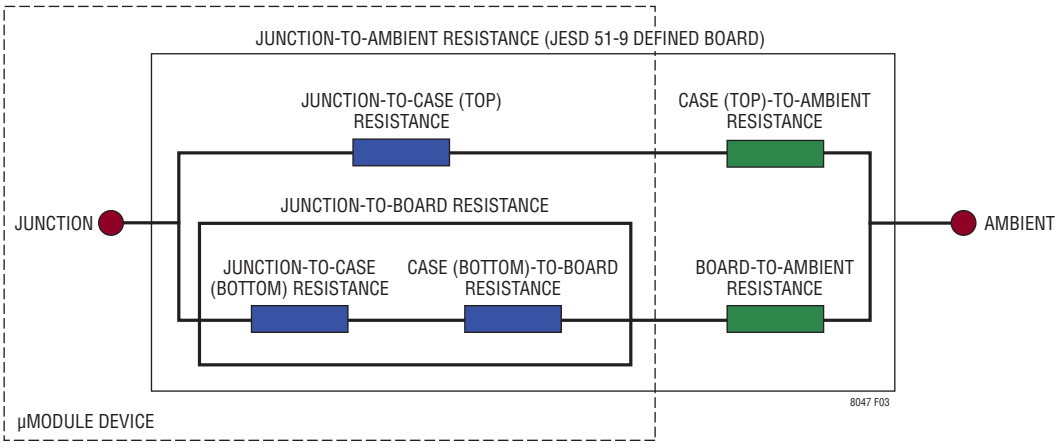
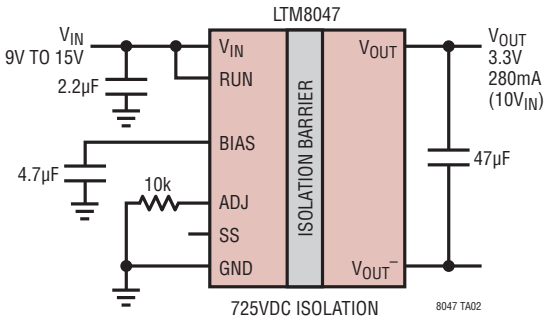


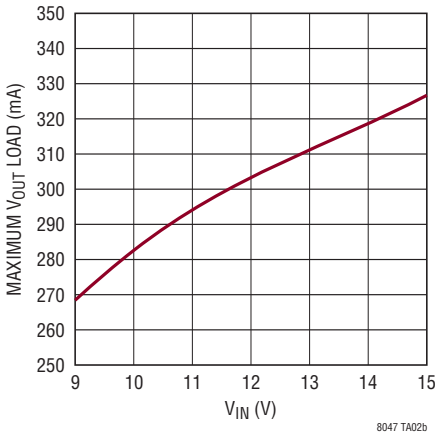
Figure 3.

TYPICAL APPLICATIONS

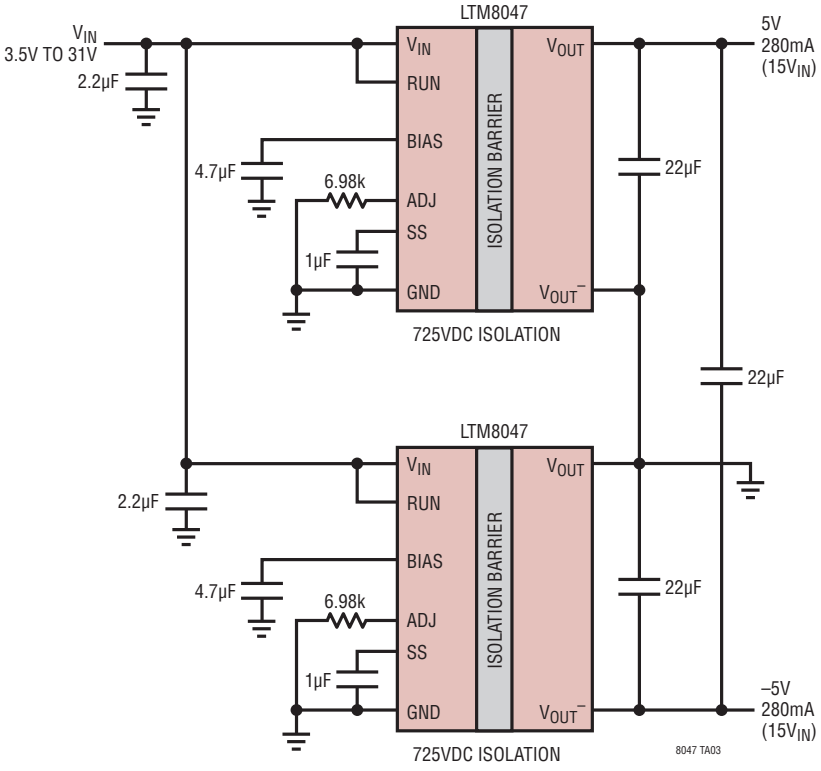
3.3V Isolated Flyback Converter



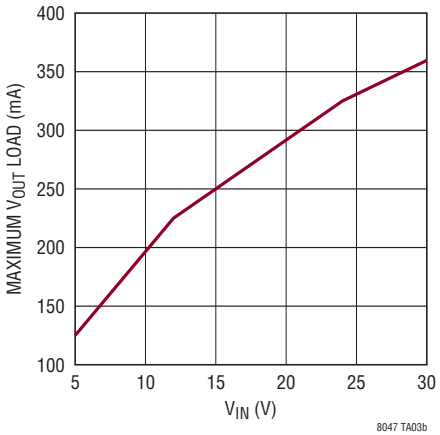
Maximum Load vs V_{IN}



Use Two LTM8047 Flyback Converters to Generate ±5V



Maximum Load Current vs V_{IN}

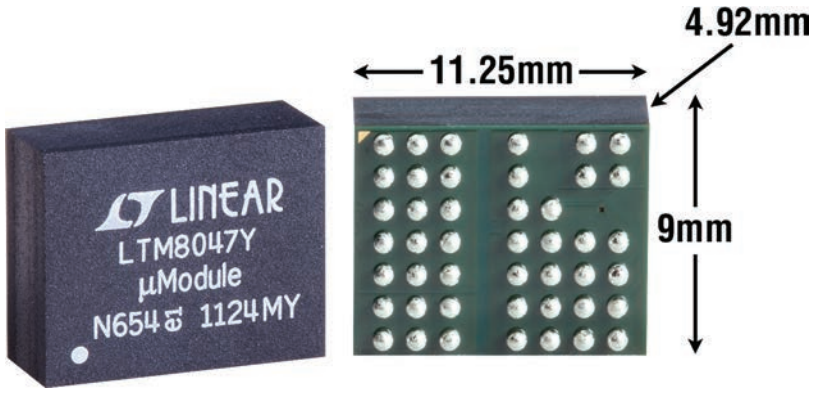


PACKAGE DESCRIPTION

Pin Assignment Table
(Arranged by Pin Number)

PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME
A1 V_{OUT}^-	B1 V_{OUT}^-	C1 V_{OUT}^-	D1 -	E1 GND	F1 -	G1 V_{IN}	H1 V_{IN}
A2 V_{OUT}^-	B2 V_{OUT}^-	C2 V_{OUT}^-	D2 -	E2 GND	F2 -	G2 V_{IN}	H2 V_{IN}
A3 V_{OUT}^-	B3 V_{OUT}^-	C3 V_{OUT}^-	D3 -	E3 GND	F3 RUN	G3 -	H3 -
A4 V_{OUT}^-	B4 V_{OUT}^-	C4 V_{OUT}^-	D4 -	E4 GND	F4 GND	G4 GND	H4 GND
A5 V_{OUT}^-	B5 V_{OUT}^-	C5 V_{OUT}^-	D5 -	E5 GND	F5 GND	G5 GND	H5 BIAS
A6 V_{OUT}	B6 V_{OUT}	C6 V_{OUT}	D6 -	E6 GND	F6 GND	G6 GND	H6 SS
A7 V_{OUT}	B7 V_{OUT}	C7 V_{OUT}	D7 -	E7 GND	F7 GND	G7 ADJ	H7 GND

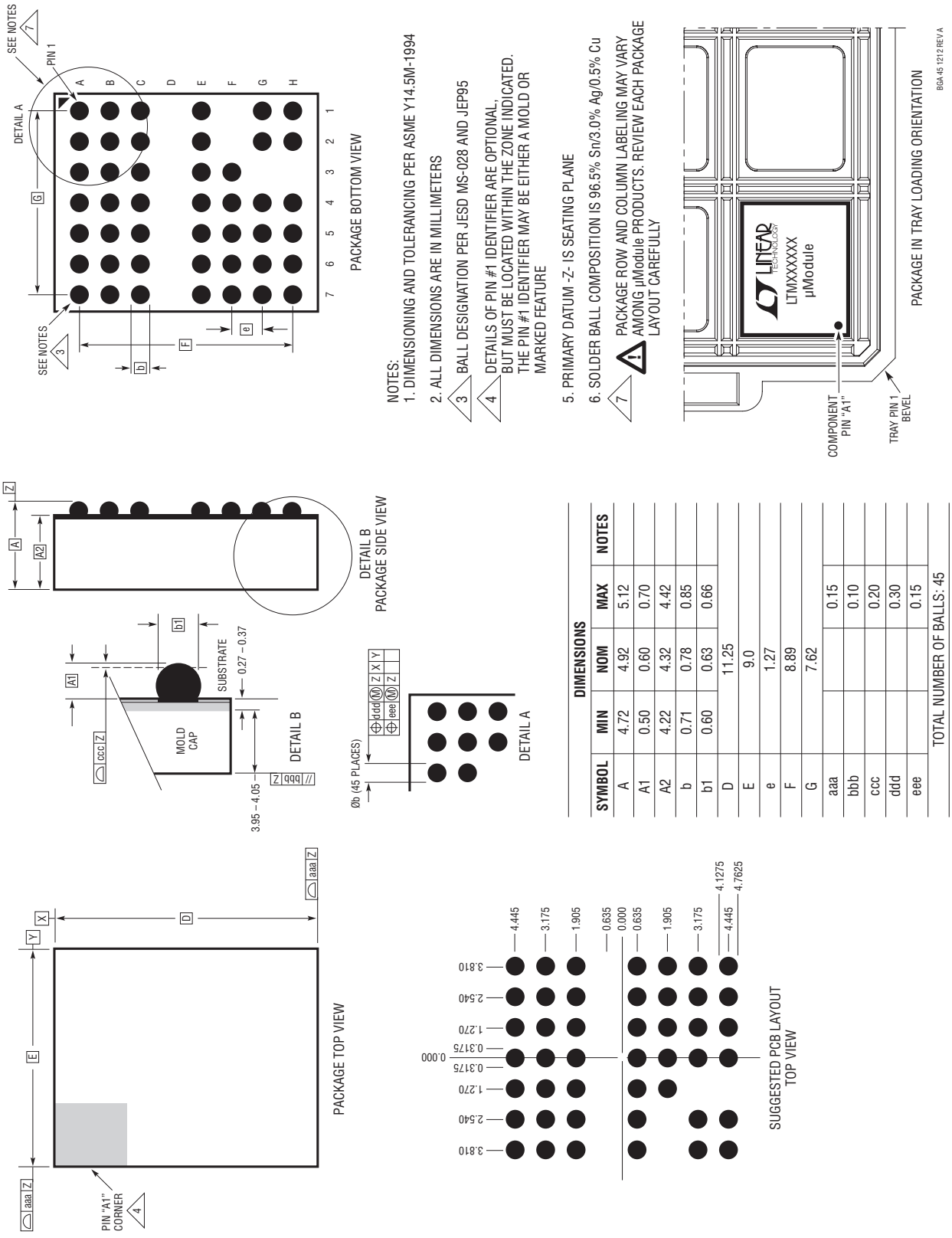
PACKAGE PHOTO



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

BGA Package
45-Lead (11.25mm × 9.00mm × 4.92mm)
(Reference LTC DWG # 05-08-1869 Rev A)



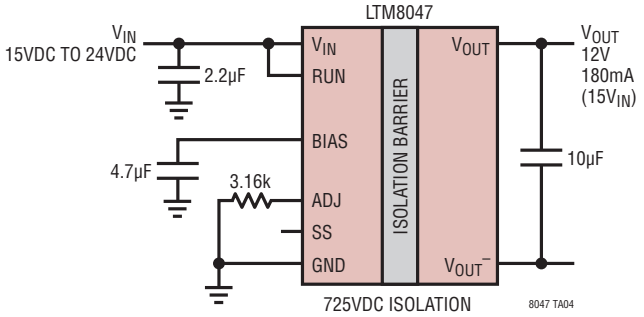
DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.71	0.78	0.85	
b1	0.60	0.63	0.66	
D		11.25		
E		9.0		
e		1.27		
F		8.89		
G		7.62		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 45				

REVISION HISTORY

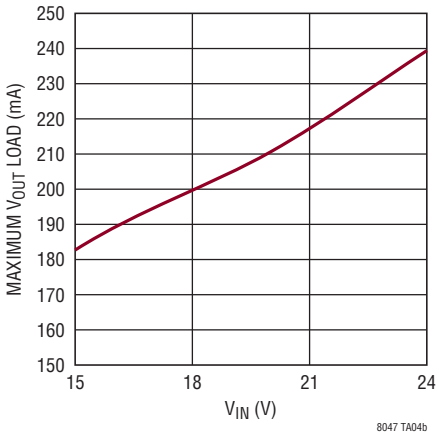
REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/14	Correct ADJ resistor on Typical Application schematic.	1
		Add Min/Max limits to Output Voltage parameter.	2
		Correct the $5V_{OUT}$ R_{ADJ} value in Table 1.	9
		Correct the $5V_{OUT}$ R_{ADJ} value in schematic.	14
B	1/14	Added SnPb terminal finish product option.	1, 2
C	7/15	Added a new section: ADJ and Line Regulation.	10, 11

TYPICAL APPLICATION

12V Isolated Flyback Converter



Maximum Load vs V_{IN}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8031	Ultralow Noise EMC 1A µModule Regulator	EN55022 Class B Compliant, 3.6V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 10V
LTM8032	Ultralow Noise EMC 2A µModule Regulator	EN55022 Class B Compliant, 3.6V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 10V
LTM8033	Ultralow Noise EMC 3A µModule Regulator	EN55022 Class B Compliant, 3.6V ≤ V_{IN} ≤ 36V; 0.8V ≤ V_{OUT} ≤ 24V
LTM4612	Ultralow Noise EMC 5A µModule Regulator	EN55022 Class B Compliant, 5V ≤ V_{IN} ≤ 36V; 3.3V ≤ V_{OUT} ≤ 15V
LTM8061	Li-Ion/Polymer µModule Battery Charger	4.95V ≤ V_{IN} ≤ 32V, 2A, 1-Cell and 2-Cell, 4.1V or 4.2V per Cell
LTM8048	Isolated DC/DC µModule Regulator with LDO Post Regulator	Low Noise LDO Post Regulator, Similar to the LTM8047

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