# 2GHz, 3.5mA Gain of 7 Stable Rail-to-Rail I/O Dual Op Amp

## FEATURES

- **Gain Bandwidth Product: 2GHz**
- **–3dB Frequency ($A_V$ = 7): 160MHz**
- **Low Quiescent Current: 3.5mA Max**
- **High Slew Rate: 500V/µs**
- **Input Common Mode Range Includes Both Rails**
- **Output Swings Rail-to-Rail**
- Low Broadband Voltage Noise: 2.75nV/√Hz
- Fast Output Recovery
- Supply Voltage Range: 2.5V to 5.25V
- Input Offset Voltage: 350µV Max
- Large Output Current: 90mA
- CMRR: 105dB
- Open Loop Gain: 60V/mV
- Operating Temperature Range: –40°C to 125°C
- MS10 Package with Independent Shutdown Pins

## APPLICATIONS

- Low Voltage, High Frequency Signal Processing
- Driving A/D Converters
- Rail-to-Rail Buffer Amplifiers
- Active Filters
- Battery Powered Equipment

## DESCRIPTION

The LTC®6253-7 is a dual high speed, low power, rail-to-rail input/output operational amplifier. On only 3.5mA of supply current, it features a 2GHz gain-bandwidth product, 500V/µs slew rate and a low 2.75nV/√Hz of input-referred noise. The combination of high bandwidth, high slew rate, low power consumption and low broadband noise makes the LTC6253-7 ideal for lower supply voltage, high speed signal conditioning systems. The device is stable for closed loop noise gains of 7 or higher.

The LTC6253-7 maintains high efficiency performance from supply voltage levels of 2.5V to 5.25V and is fully specified at supplies of 2.7V and 5.0V.

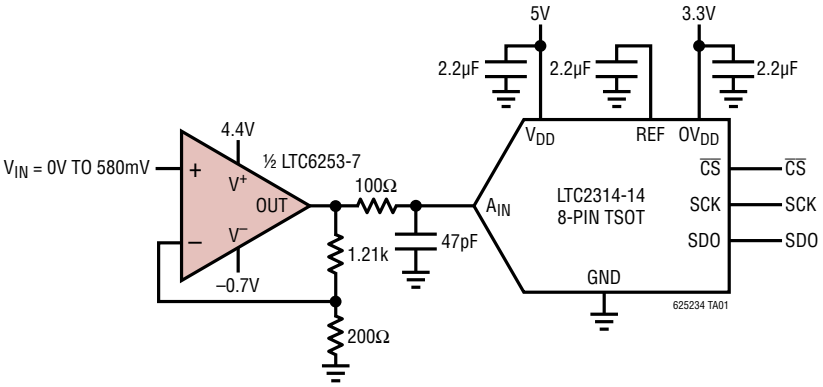
For applications that require power-down, the LTC6253-7 offers a shutdown pin which disables the amplifier and reduces current consumption to 42µA.

The LTC6253-7 can be used as a plug-in replacement for many commercially available op amps to reduce power or to improve input/output range and performance.

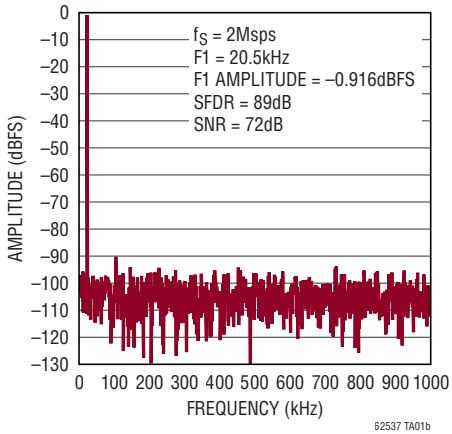


## TYPICAL APPLICATION

**ADC Driver with Gain**




**LTC6253–7 Driving LTC2314–14 1024 Point FFT**

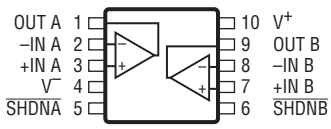


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Total Supply Voltage ($V^+$ to $V^-$) ..... 5.5V
Input Current (+IN, –IN, $\overline{SHDN}$) (Note 2) ..... ±10mA
Output Current (Note 3) ..... ±100mA
Operating Temperature Range (Note 4) .. –40°C to 125°C
Specified Temperature Range (Note 5) .. –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




MS PACKAGE
10-LEAD PLASTIC MSOP

$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 160°C/W (NOTE 9)

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC6253IMS-7#PBF | LTC6253IMS-7#TRPBF | LTGWS | 10-Lead Plastic MSOP | –40°C to 85°C |
| LTC6253HMS-7#PBF | LTC6253HMS-7#TRPBF | LTGWS | 10-Lead Plastic MSOP | –40°C to 125°C |

*Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**($V_S$ = 5V) The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at $T_A$ = 25°C. For each amplifier $V_S$ = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; $V_{CM}$ = $V_{OUT}$ = 2.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = Half Supply | | –350 | 50 | 350 | µV |
| | | | ● | –1000 | | 1000 | µV |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | | –2.2 | 0.1 | 2.2 | mV |
| | | | ● | –3.3 | | –3.3 | mV |
| $\Delta V_{OS}$ | Input Offset Voltage Match (Channel-to-Channel) (Note 7) | $V_{CM}$ = Half Supply | | –350 | 50 | 350 | µV |
| | | | ● | –550 | | 550 | µV |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | | –2.75 | 0.1 | 2.75 | mV |
| | | | ● | –4 | | 4 | mV |
| $V_{OS}$ $T_C$ | Input Offset Voltage Drift | | ● | | –3.5 | | µV/°C |
| $I_B$ | Input Bias Current (Note 6) | $V_{CM}$ = Half Supply | | –0.75 | –0.1 | 0.75 | µA |
| | | | ● | –1.15 | | 1.15 | µA |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | | 0.8 | 1.4 | 3.0 | µA |
| | | | ● | 0.4 | | 5.0 | µA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = Half Supply | | –0.5 | –0.03 | 0.5 | µA |
| | | | ● | –0.6 | | 0.6 | µA |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | | –0.5 | –0.03 | 0.5 | µA |
| | | | ● | –0.6 | | 0.6 | µA |
| $e_n$ | Input Noise Voltage Density | f = 1MHz | | | 2.75 | | nV/√Hz |
| | Input 1/f Noise Voltage | f = 0.1Hz to 10Hz | | | 2 | | $\mu V_{P-P}$ |
| $i_n$ | Input Noise Current Density | f = 1MHz | | | 4 | | pA/√Hz |

## ELECTRICAL CHARACTERISTICS

**($V_S$ = 5V) The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at $T_A$ = 25°C. For each amplifier $V_S$ = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; $V_{CM}$ = $V_{OUT}$ = 2.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | Differential Mode<br>Common Mode | | | 2.5<br>0.8 | | pF<br>pF |
| $R_{IN}$ | Input Resistance | Differential Mode<br>Common Mode | | | 7.2<br>3 | | kΩ<br>MΩ |
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L$ = 1k to Half Supply (Note 9) | <br>● | 35<br>16 | 60 | | V/mV<br>V/mV |
| | | $R_L$ = 100Ω to Half Supply (Note 9) | <br>● | 5<br>2.4 | 13 | | V/mV<br>V/mV |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = 0V to 3.5V | <br>● | 85<br>82 | 105 | | dB<br>dB |
| $V_{CMR}$ | Input Common Mode Range | | ● | 0 | | $V_S$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5V to 5.25V, $V_{CM}$ = 1V | <br>● | 66.5<br>62 | 70 | | dB<br>dB |
| | Supply Voltage Range (Note 5) | | ● | 2.5 | | 5.25 | V |
| $V_{OL}$ | Output Swing Low ($V_{OUT}$ – $V^-$) | No Load | <br>● | | 25 | 40<br>65 | mV<br>mV |
| | | $I_{SINK}$ = 5mA | <br>● | | 60 | 90<br>120 | mV<br>mV |
| | | $I_{SINK}$ = 25mA | <br>● | | 150 | 200<br>320 | mV<br>mV |
| $V_{OH}$ | Output Swing High ($V^+$ – $V_{OUT}$) | No Load | <br>● | | 65 | 100<br>120 | mV<br>mV |
| | | $I_{SOURCE}$ = 5mA | <br>● | | 115 | 170<br>210 | mV<br>mV |
| | | $I_{SOURCE}$ = 25mA | <br>● | | 270 | 330<br>450 | mV<br>mV |
| $I_{SC}$ | Output Short-Circuit Current | Sourcing | <br>● | | –90 | –40<br>–32 | mA<br>mA |
| | | Sinking | <br>● | 60<br>40 | 100 | | mA<br>mA |
| $I_S$ | Supply Current per Amplifier | $V_{CM}$ = Half Supply | <br>● | | 3.3 | 3.5<br>4.8 | mA<br>mA |
| | | $V_{CM}$ = $V^+$ – 0.5V | <br>● | | 4.25 | 4.85<br>5.9 | mA<br>mA |
| $I_{SD}$ | Disable Supply Current | $V_{\overline{SHDN}}$ = 0.8V | <br>● | | 42 | 55<br>75 | µA<br>µA |
| $I_{\overline{SHDNL}}$ | $\overline{SHDN}$ Pin Current Low | $V_{\overline{SHDN}}$ = 0.8V | <br>● | –3<br>–4 | –1.6 | 0<br>0 | µA<br>µA |
| $I_{\overline{SHDNH}}$ | $\overline{SHDN}$ Pin Current High | $V_{\overline{SHDN}}$ = 2V | <br>● | –300<br>–600 | 35 | 300<br>600 | nA<br>nA |
| $V_L$ | $\overline{SHDN}$ Pin Input Voltage Low | | ● | | | 0.8 | V |
| $V_H$ | $\overline{SHDN}$ Pin Input Voltage High | | ● | 2 | | | V |
| $I_{OSD}$ | Output Leakage Current in Shutdown | $V_{\overline{SHDN}}$ = 0.8V, Output Shorted to Either Supply | | | 100 | | nA |
| $t_{ON}$ | Turn-On Time | $V_{\overline{SHDN}}$ = 0.8V to 2V | | | 3.5 | | µs |
| $t_{OFF}$ | Turn-Off Time | $V_{\overline{SHDN}}$ = 2V to 0.8V | | | 2 | | µs |

## ELECTRICAL CHARACTERISTICS

**($V_S$ = 5V) The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at $T_A$ = 25°C. For each amplifier $V_S$ = 5V, 0V; $V_{\overline{SHDN}}$ = 2V; $V_{CM}$ = $V_{OUT}$ = 2.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| BW | –3dB Closed Loop Bandwidth | $A_V$ = 7, $R_L$ = 1k to Half Supply | | | 160 | | MHz |
| GBW | Gain-Bandwidth Product | f = 10MHz, $R_L$ = 1k to Half Supply | <br>● | 0.9<br>0.67 | 2 | | GHz<br>GHz |
| $t_S$, 0.1% | Settling Time to 0.1% | $A_V$ = 7, 2V Output Step $R_L$ = 1k, $V_{CC}$ = 4.5V, $V_{EE}$ = 0.5V | | | 32 | | ns |
| SR | Slew Rate | $A_V$ = –6, 4V Output Step (Note 10) | <br>● | 300<br>250 | 500 | | V/µs<br>V/µs |
| FPBW | Full Power Bandwidth | $V_{OUT}$ = $4V_{P-P}$ (Note 12) | | | 13 | | MHz |
| HD2/HD3 | Harmonic Distortion<br>$R_L$ = 1k to Half Supply, $A_V$ = +7,<br>$R_F$ = 499Ω | $f_C$ = 100kHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 1MHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 5MHz, $V_O$ = $2V_{P-P}$ | | | 99/94<br>73/71<br>60/56 | | dBc<br>dBc<br>dBc |
| | $R_L$ = 1kΩ to Half Supply, $A_V$ = +7,<br>$R_F$ = 3kΩ | $f_C$ = 100kHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 1MHz, $V_O$ = $2V_{P-P}$<br>$f_C$ = 5MHz, $V_O$ = $2V_{P-P}$ | | | 105/109<br>82/87<br>66/67 | | dBc<br>dBc<br>dBc |
| | Crosstalk | $A_V$ = 7, $R_L$ = 1k to Half Supply, $V_{OUT}$ = $2V_{P-P}$, f = 2.5MHz | | | –79 | | dB |

**($V_S$ = 2.7V) The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at $T_A$ = 25°C. For each amplifier $V_S$ = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; $V_{CM}$ = $V_{OUT}$ = 1.35V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{OS}$ | Input Offset Voltage | $V_{CM}$ = Half Supply | <br>● | 0<br>–300 | 700 | 1250<br>1500 | µV<br>µV |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | <br>● | –1.6<br>–2.0 | 0.9 | 3.2<br>3.4 | mV<br>mV |
| $\Delta V_{OS}$ | Input Offset Voltage Match (Channel-to-Channel) (Note 8) | $V_{CM}$ = Half Supply | <br>● | –350<br>–750 | 10 | 350<br>750 | µV<br>µV |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | <br>● | –2.8<br>–4 | 0.1 | 2.8<br>4 | mV<br>mV |
| $V_{OS}$ $T_C$ | Input Offset Voltage Drift | | ● | | 2.75 | | µV/°C |
| $I_B$ | Input Bias Current (Note 7) | $V_{CM}$ = Half Supply | <br>● | –1000<br>–1500 | –275 | 600<br>900 | nA<br>nA |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | <br>● | 0.6<br>0 | 1.175 | 2.5<br>4.0 | µA<br>µA |
| $I_{OS}$ | Input Offset Current | $V_{CM}$ = Half Supply | <br>● | –500<br>–600 | –150 | 500<br>600 | nA<br>nA |
| | | $V_{CM}$ = $V^+$ – 0.5V, NPN Mode | <br>● | –500<br>–600 | –30 | 500<br>600 | nA<br>nA |
| $e_n$ | Input Noise Voltage Density | f = 1MHz | | | 2.9 | | $nV/\sqrt{Hz}$ |
| | Input 1/f Noise Voltage | f = 0.1Hz to 10Hz | | | 2 | | $\mu V_{P-P}$ |
| $i_n$ | Input Noise Current Density | f = 1MHz | | | 3.6 | | $pA/\sqrt{Hz}$ |
| $C_{IN}$ | Input Capacitance | Differential Mode<br>Common Mode | | | 2.5<br>0.8 | | pF<br>pF |
| $R_{IN}$ | Input Resistance | Differential Mode<br>Common Mode | | | 7.2<br>3 | | kΩ<br>MΩ |

## ELECTRICAL CHARACTERISTICS

**($V_S$ = 2.7V) The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at $T_A$ = 25°C. For each amplifier $V_S$ = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; $V_{CM}$ = $V_{OUT}$ = 1.35V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $A_{VOL}$ | Large Signal Voltage Gain | $R_L$ = 1k to Half Supply (Note 11) | ● | 16.5<br>7 | 36 | | V/mV<br>V/mV |
| | | $R_L$ = 100Ω to Half Supply (Note 11) | ● | 2.3<br>1.8 | 6.9 | | V/mV<br>V/mV |
| CMRR | Common Mode Rejection Ratio | $V_{CM}$ = 0V to 1.2V | ● | 80<br>77 | 105 | | dB<br>dB |
| $V_{CMR}$ | Input Common Mode Range | | ● | 0 | | $V_S$ | V |
| PSRR | Power Supply Rejection Ratio | $V_S$ = 2.5V to 5.25V, $V_{CM}$ = 1V | ● | 66.5<br>62 | 70 | | dB<br>dB |
| | Supply Voltage Range (Note 5) | | ● | 2.5 | | 5.25 | V |
| $V_{OL}$ | Output Swing Low ($V_{OUT}$ – $V^-$) | No Load | ● | | 22 | 28<br>40 | mV<br>mV |
| | | $I_{SINK}$ = 5mA | ● | | 80 | 100<br>140 | mV<br>mV |
| | | $I_{SINK}$ = 10mA | ● | | 110 | 150<br>190 | mV<br>mV |
| $V_{OH}$ | Output Swing High ($V^+$ – $V_{OUT}$) | No Load | ● | | 55 | 75<br>95 | mV<br>mV |
| | | $I_{SOURCE}$ = 5mA | ● | | 125 | 150<br>200 | mV<br>mV |
| | | $I_{SOURCE}$ = 10mA | ● | | 165 | 200<br>275 | mV<br>mV |
| $I_{SC}$ | Short-Circuit Current | Sourcing | ● | | –35 | –18<br>–14 | mA<br>mA |
| | | Sinking | ● | 20<br>17 | 40 | | mA<br>mA |
| $I_S$ | Supply Current per Amplifier | $V_{CM}$ = Half Supply | ● | | 2.9 | 3.5<br>4.5 | mA<br>mA |
| | | $V_{CM}$ = $V^+$ – 0.5V | ● | | 3.7 | 4.6<br>5.5 | mA<br>mA |
| $I_{SD}$ | Disable Supply Current | $V_{\overline{SHDN}}$ = 0.8V | ● | | 24 | 35<br>50 | µA<br>µA |
| $I_{\overline{SHDN}L}$ | $\overline{SHDN}$ Pin Current Low | $V_{\overline{SHDN}}$ = 0.8V | ● | –1<br>–1.5 | –0.5 | 0<br>0 | µA<br>µA |
| $I_{\overline{SHDN}H}$ | $\overline{SHDN}$ Pin Current High | $V_{\overline{SHDN}}$ = 2V | ● | –300<br>–600 | 45 | 300<br>600 | nA<br>nA |
| $V_L$ | $\overline{SHDN}$ Pin Input Voltage | | ● | | | 0.8 | V |
| $V_H$ | $\overline{SHDN}$ Pin Input Voltage | | ● | 2.0 | | | V |
| $I_{OSD}$ | Output Leakage Current Magnitude in Shutdown | $V_{\overline{SHDN}}$ = 0.8V, Output Shorted to Either Supply | | | 100 | | nA |
| $t_{ON}$ | Turn-On Time | $V_{\overline{SHDN}}$ = 0.8V to 2V | | | 5 | | µs |
| $t_{OFF}$ | Turn-Off Time | $V_{\overline{SHDN}}$ = 2V to 0.8V | | | 2 | | µs |
| BW | –3dB Closed Loop Bandwidth | $A_V$ = +7, $R_L$ = 1k to Half Supply | | | 130 | | MHz |
| GBW | Gain-Bandwidth Product | f = 10MHz, $R_L$ = 1k to Half Supply | ● | 0.8<br>0.5 | 1.3 | | GHz<br>GHz |

## ELECTRICAL CHARACTERISTICS

**($V_S$ = 2.7V) The ● denotes the specifications which apply across the specified temperature range, otherwise specifications are at $T_A$ = 25°C. For each amplifier $V_S$ = 2.7V, 0V; $V_{\overline{SHDN}}$ = 2V; $V_{CM}$ = $V_{OUT}$ = 1.35V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_S$, 0.1 | Settling Time to 0.1% | $A_V$ = +7, 2V Output Step $R_L$ = 1k, $V_{CC}$ = 2.35V, $V_{EE}$ = –0.35V | | | 25 | | ns |
| SR | Slew Rate | $A_V$ = –6, 2V Output Step (Note 10) | | | 300 | | V/µs |
| FPBW | Full Power Bandwidth | $V_{OUT}$ = $2V_{P-P}$ (Note 12) | | | 11 | | MHz |
| | Crosstalk | $A_V$ = +7, $R_L$ = 1k to Half Supply, $V_{OUT}$ = $2V_{P-P}$, f = 2.5MHz | | | –88 | | dB |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by back-to-back diodes. If any of the input or shutdown pins goes 300mV beyond either supply or the differential input voltage exceeds 1.4V the input current should be limited to less than 10mA. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output current is high. This parameter is guaranteed to meet specified performance through design and/or characterization. It is not production tested.

**Note 4:** The LTC6253-7I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6253-7H is guaranteed to meet specified performance from –40°C to 125°C.

**Note 5:** Supply voltage range is guaranteed by power supply rejection ratio test.

**Note 6:** The input bias current is the average of the average of the currents at the positive and negative input pins.

**Note 7:** Matching parameters are the difference between the two amplifiers on the LTC6253-7.

**Note 8:** Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are with short traces connected to the leads with minimal metal area.

**Note 9:** The output voltage is varied from 0.5V to 4.5V during measurement.

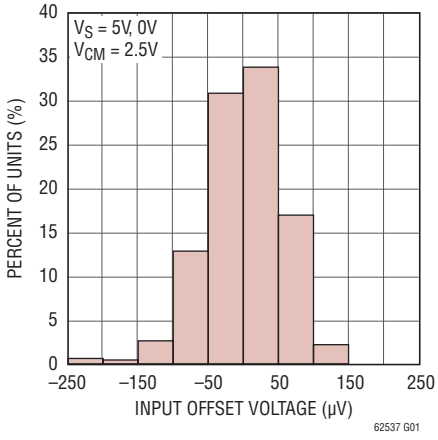
**Note 10:** Middle 2/3 of the output waveform is observed. $R_L$ = 1k to half supply.

**Note 11:** The output voltage is varied from 0.5V to 2.2V during measurement.

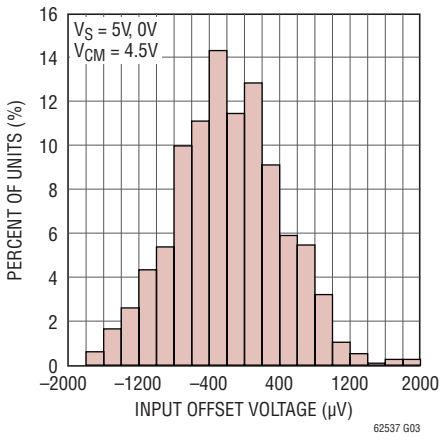
**Note 12:** FPBW is determined from distortion performance in a gain of +7 configuration with HD2, HD3 < –40dBc as the criteria for a valid output.

## TYPICAL PERFORMANCE CHARACTERISTICS

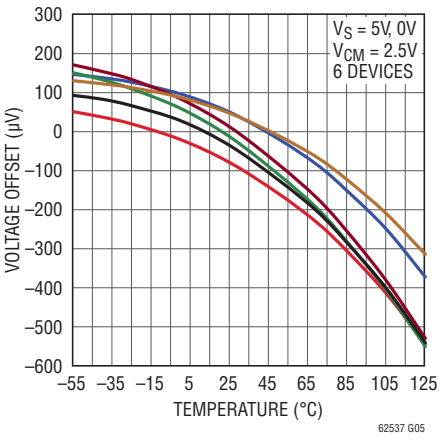
**$V_{OS}$ Distribution, $V_{CM}$ = $V_S$/2 (MS, PNP Stage)**




**$V_{OS}$ Distribution, $V_{CM}$ = $V^+$ – 0.5V (NPN Stage)**

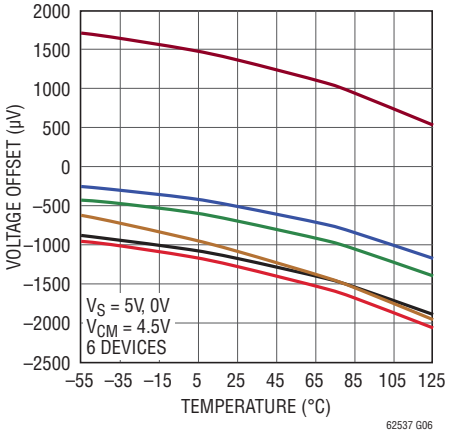



**$V_{OS}$ vs Temperature, $V_S$ = 5V, 0V (PNP Stage)**

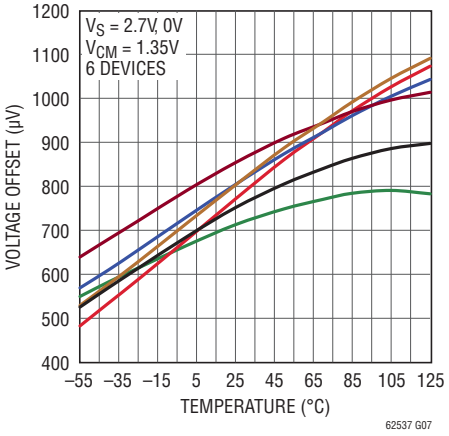


## TYPICAL PERFORMANCE CHARACTERISTICS

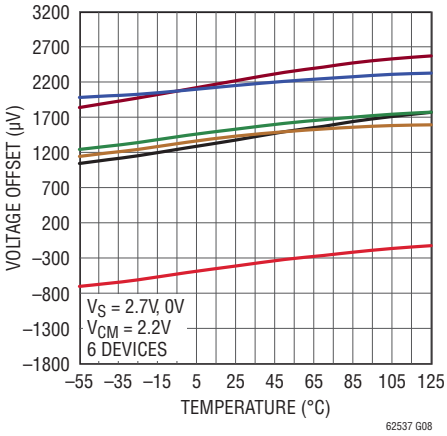
**$V_{OS}$ vs Temperature, $V_S$ = 5V, 0V (NPN Stage)**



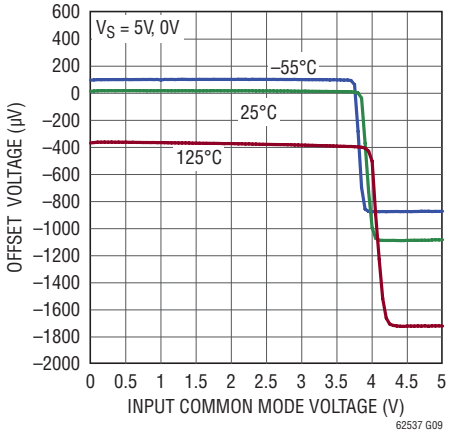

**$V_{OS}$ vs Temperature, $V_S$ = 2.7V, 0V (PNP Stage)**



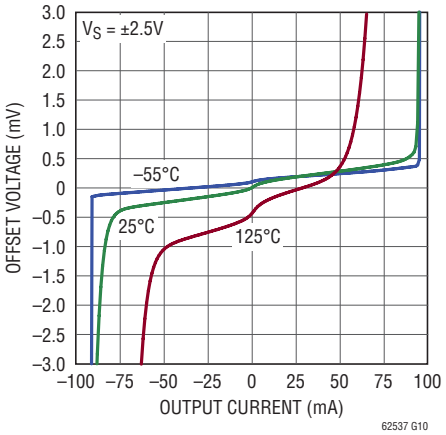

**$V_{OS}$ vs Temperature, $V_S$ = 2.7V, 0V (NPN Stage)**



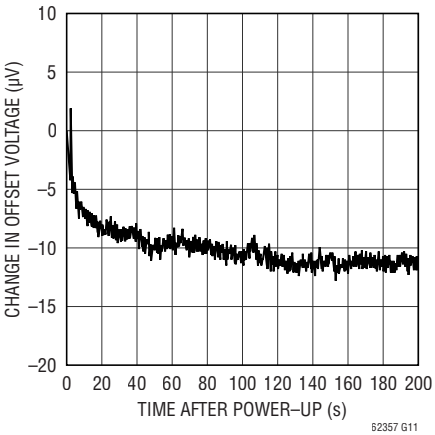

**Offset Voltage vs Input Common Mode Voltage**



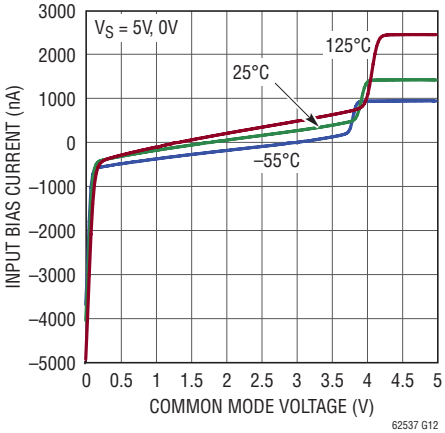

**Offset Voltage vs Output Current**



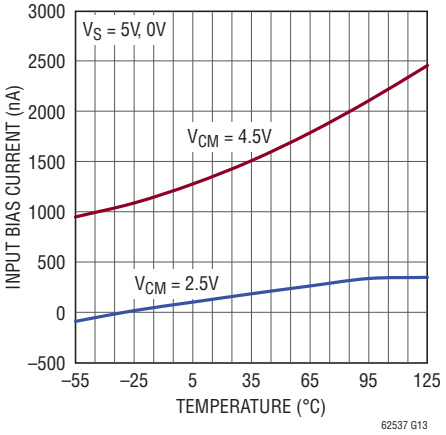

**Warm-Up Drift vs Time**



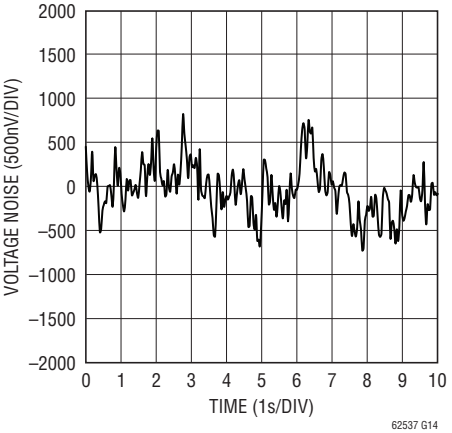

**Input Bias Current vs Common Mode Voltage**




**Input Bias Current vs Temperature**

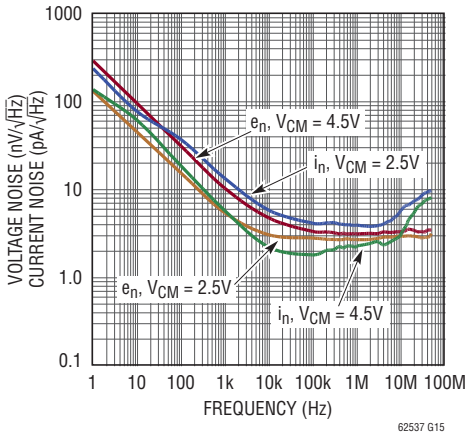



**0.1Hz to 10Hz Voltage Noise**

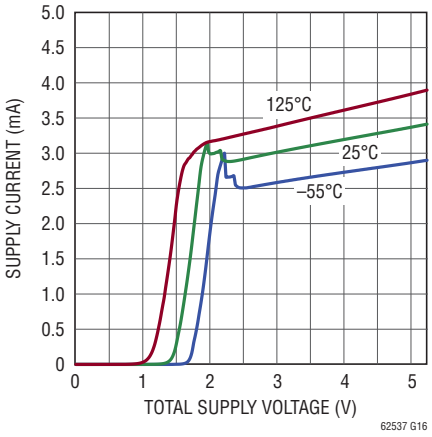


## TYPICAL PERFORMANCE CHARACTERISTICS

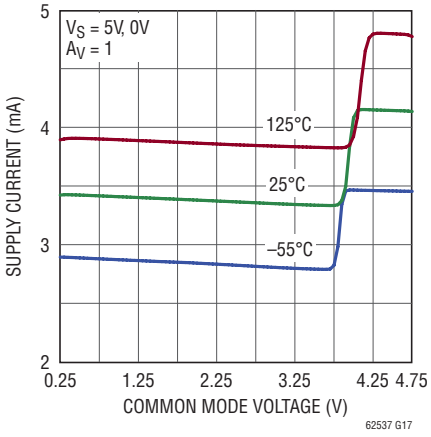
### Input Noise Voltage and Noise Current vs Frequency



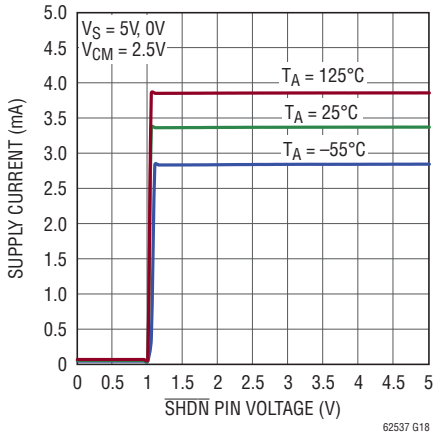

### Supply Current vs Supply Voltage (Per Amplifier)



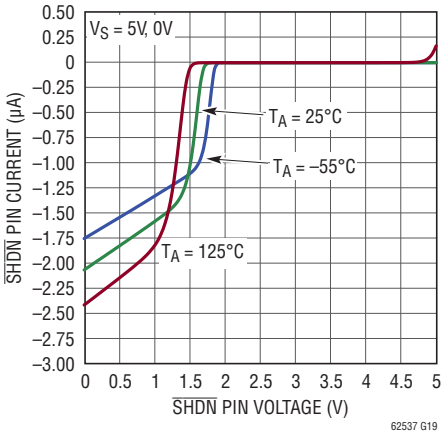

### Supply Current vs Input Common Mode Voltage (Per Amplifier)



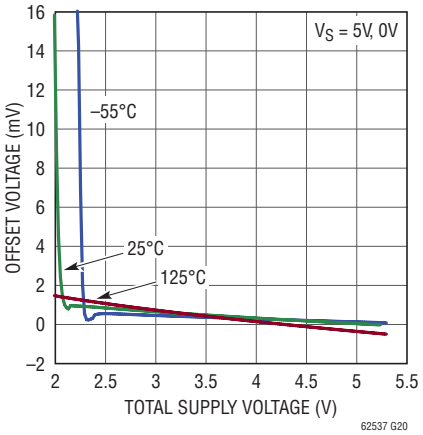

### Supply Current Per Amplifier vs $\overline{SHDN}$ Pin Voltage



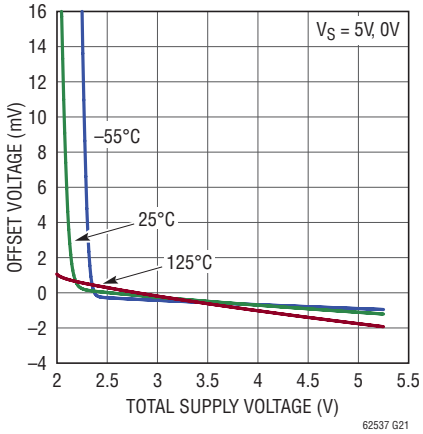

### $\overline{SHDN}$ Pin Current vs $\overline{SHDN}$ Pin Voltage



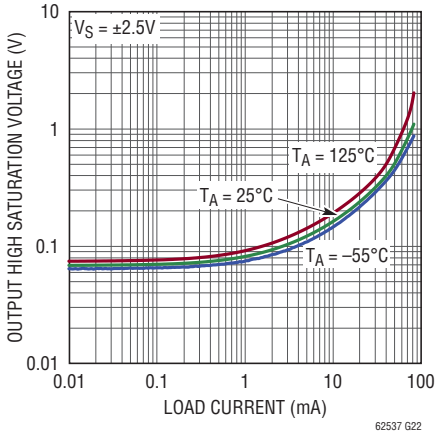

### Minimum Supply Voltage, $V_{CM} = V_S/2$ (PNP Operation)



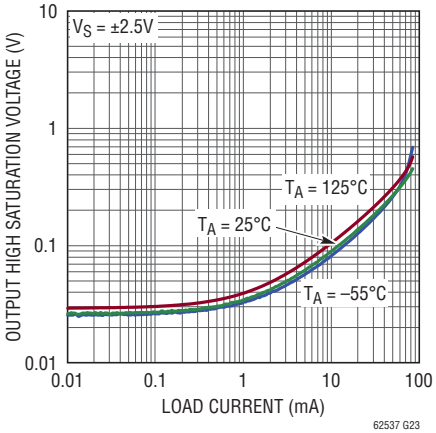

### Minimum Supply Voltage, $V_{CM} = V^+ – 0.5V$ (NPN Operation)




### Output Saturation Voltage vs Load Current (Output High)

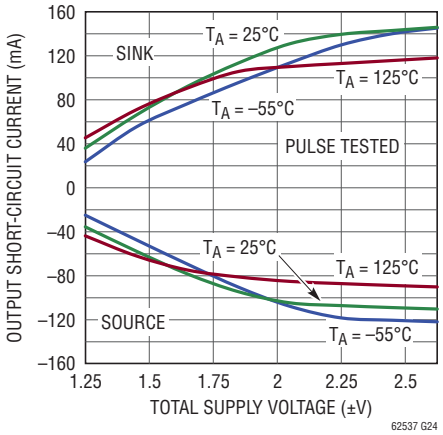



### Output Saturation Voltage vs Load Current (Output Low)

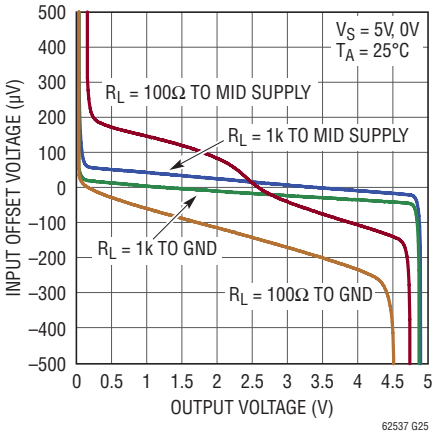


# TYPICAL PERFORMANCE CHARACTERISTICS

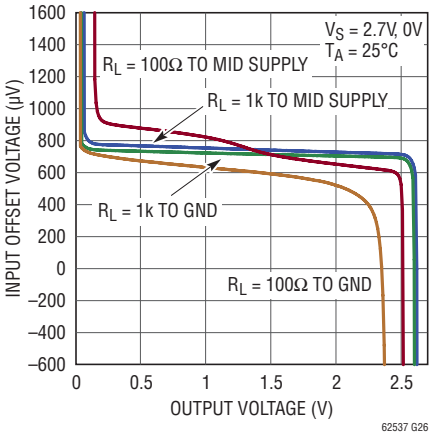
### Output Short-Circuit Current vs Supply Voltage



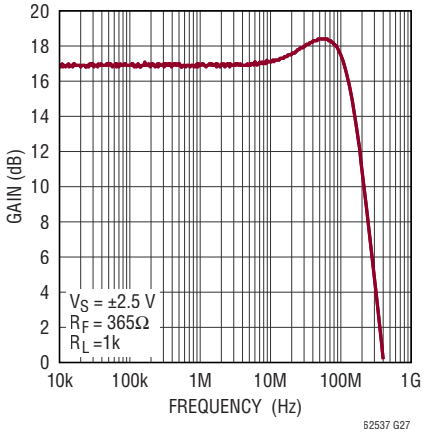

### Open Loop Gain



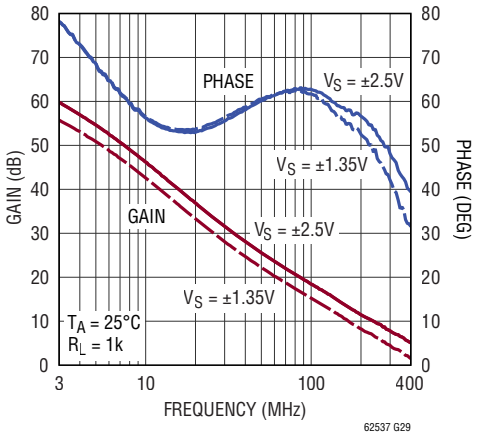

### Open Loop Gain



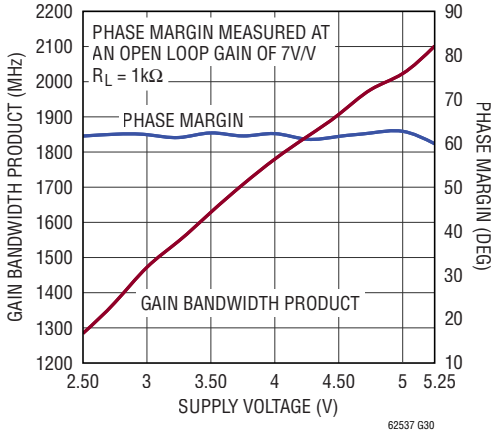

### Gain vs Frequency ($A_V$ = 7)



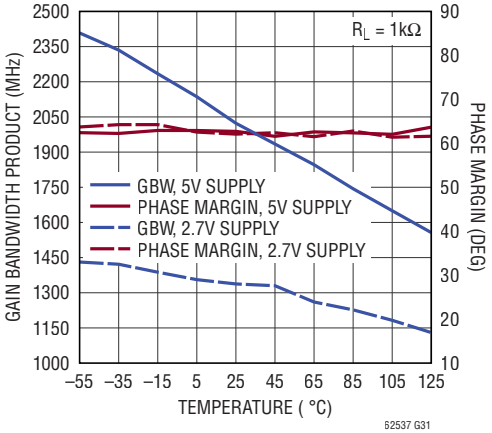

### Open Loop Gain and Phase vs Frequency




### Gain Bandwidth and Phase Margin vs Supply Voltage

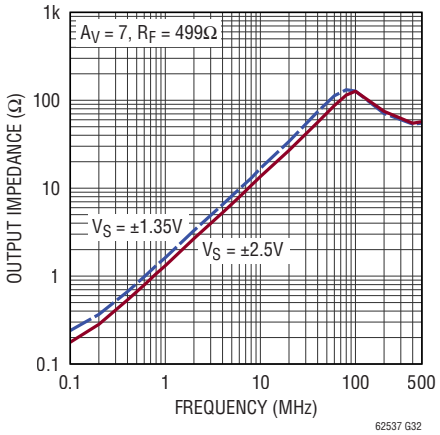



### Gain Bandwidth and Phase Margin vs Temperature

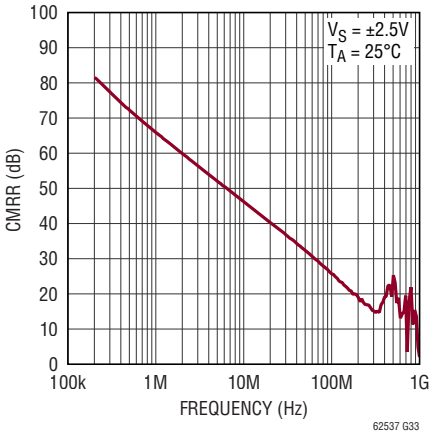


## TYPICAL PERFORMANCE CHARACTERISTICS

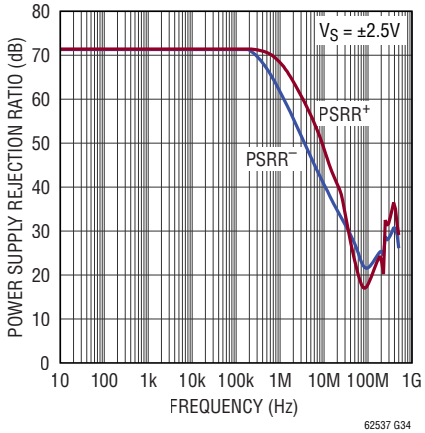
### Output Impedance vs Frequency



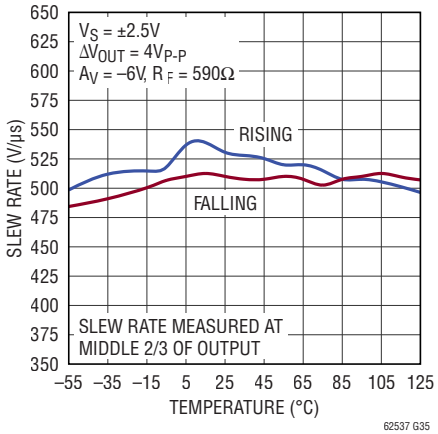

### Common Mode Rejection Ratio vs Frequency



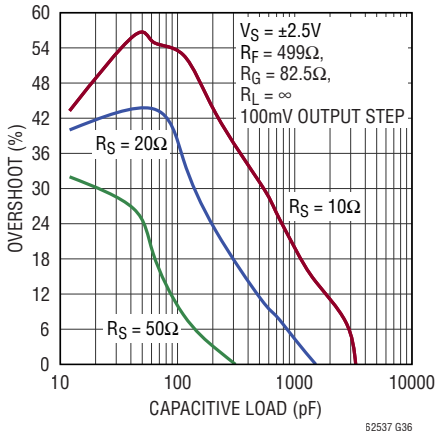

### Power Supply Rejection Ratio vs Frequency



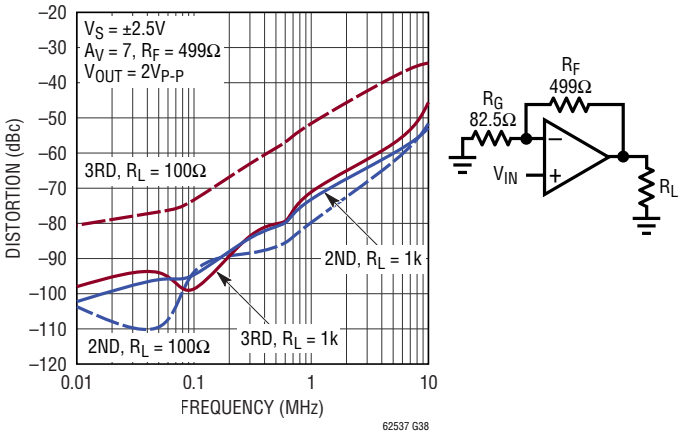

### Slew Rate vs Temperature




### Series Output Resistor vs Capacitive Load ($A_V$ = 7)

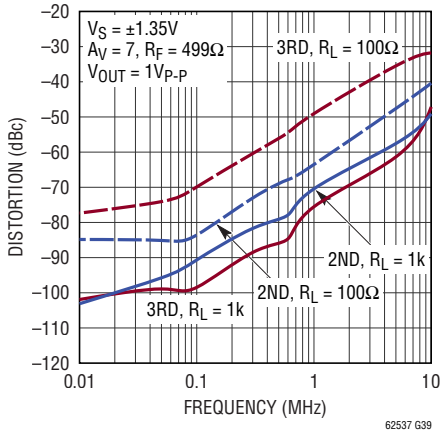


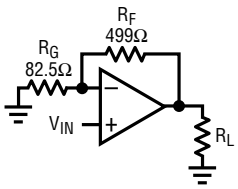

### Distortion vs Frequency, 5V Supply



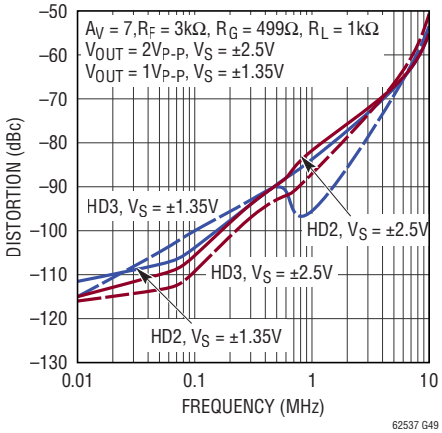
# TYPICAL PERFORMANCE CHARACTERISTICS

### Distortion vs Frequency, 2.7V Supply

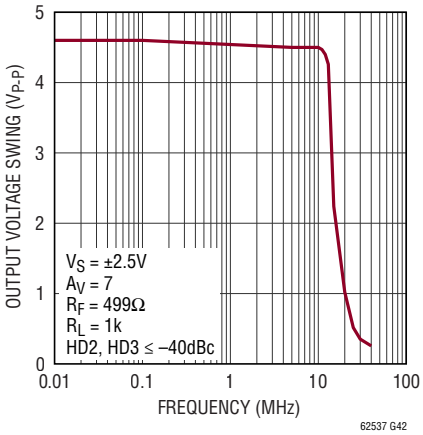


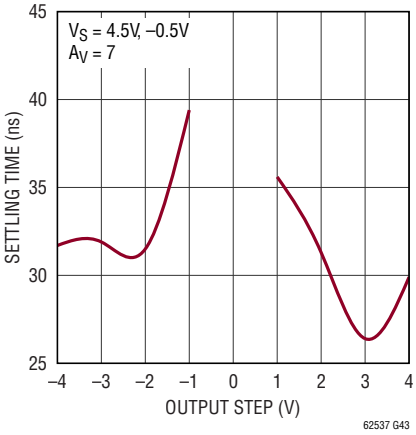

### Distortion vs Frequency, (Moderate Loading, $A_V$ = 7)



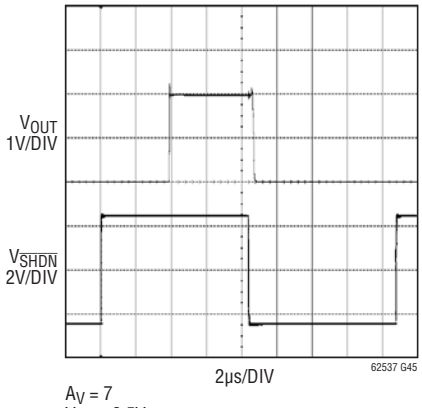

### Maximum Undistorted Output Signal vs Frequency




### 0.1% Settling Time vs Output Step

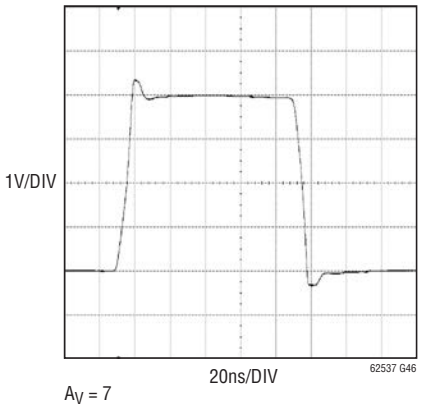



### $\overline{SHDN}$ Pin Response Time



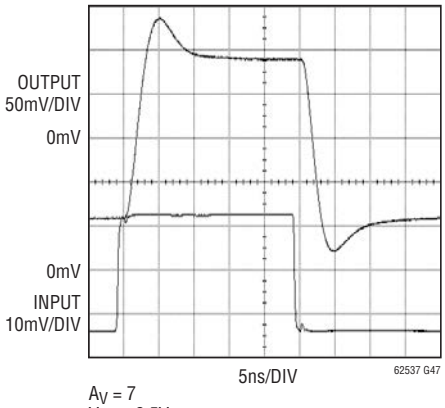

AV = 7
VS = ±2.5V
RL = 1k
VIN = 280mV

### Large Signal Response



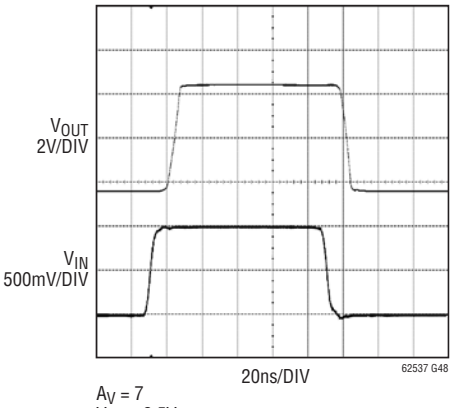

AV = 7
VS = ±2.5V
TA = 25°C
RL = 1k

### Small Signal Response




AV = 7
VS = ±2.5V
TA = 25°C
RL = 1k

### Output Overdriven Recovery




AV = 7
VS = ±2.5V
TA = 25°C
VIN = 1VP-P

## PIN FUNCTIONS

**–IN:** Inverting Input of Amplifier. Input range from $V^-$ to $V^+$.

**+IN:** Non-Inverting Input of Amplifier. Input range from $V^-$ to $V^+$.

**$V^+$ :** Positive Supply Voltage. Total supply voltage ranges from 2.5V to 5.25V.

**$V^-$ :** Negative Supply Voltage. Typically 0V. This can be made a negative voltage as long as $2.5V \leq (V^+ – V^-) \leq 5.25V$.

**$\overline{SHDN}$:** Active Low Shutdown. Threshold is typically 1.1V referenced to $V^-$. Floating this pin will turn the part on.

**OUT:** Amplifier Output. Swings rail-to-rail and can typically source/sink over 90mA of current at a total supply of 5V.

## APPLICATIONS INFORMATION

### Circuit Description

The LTC6253-7 has an input and output signal range that extends from the negative power supply to the positive power supply. Figure 1 depicts a simplified schematic of the amplifier. The input stage is comprised of two differential amplifiers, a PNP stage, Q1/Q2, and an NPN stage, Q3/Q4 that are active over different common mode input voltages. The PNP stage is active between the negative supply to nominally 1.2V below the positive supply. As the input voltage approaches the positive supply, the transistor Q5 will steer the tail current, $I_1$, to the current mirror, Q6/Q7, activating the NPN differential pair and the PNP pair becomes inactive for the remaining input common mode range. Also, at the input stage, devices Q17 to Q19 act to cancel the bias current of the PNP input pair. When Q1/Q2 are active, the current in Q16 is controlled to be the same as the current in Q1 and Q2. Thus, the base current of Q16 is nominally equal to the base current of the input devices. The base current of Q16 is then mirrored by devices Q17 to Q19 to cancel the base current of the input devices Q1/Q2. A pair of complementary common emitter stages, Q14/Q15, enable the output to swing from rail-to-rail.

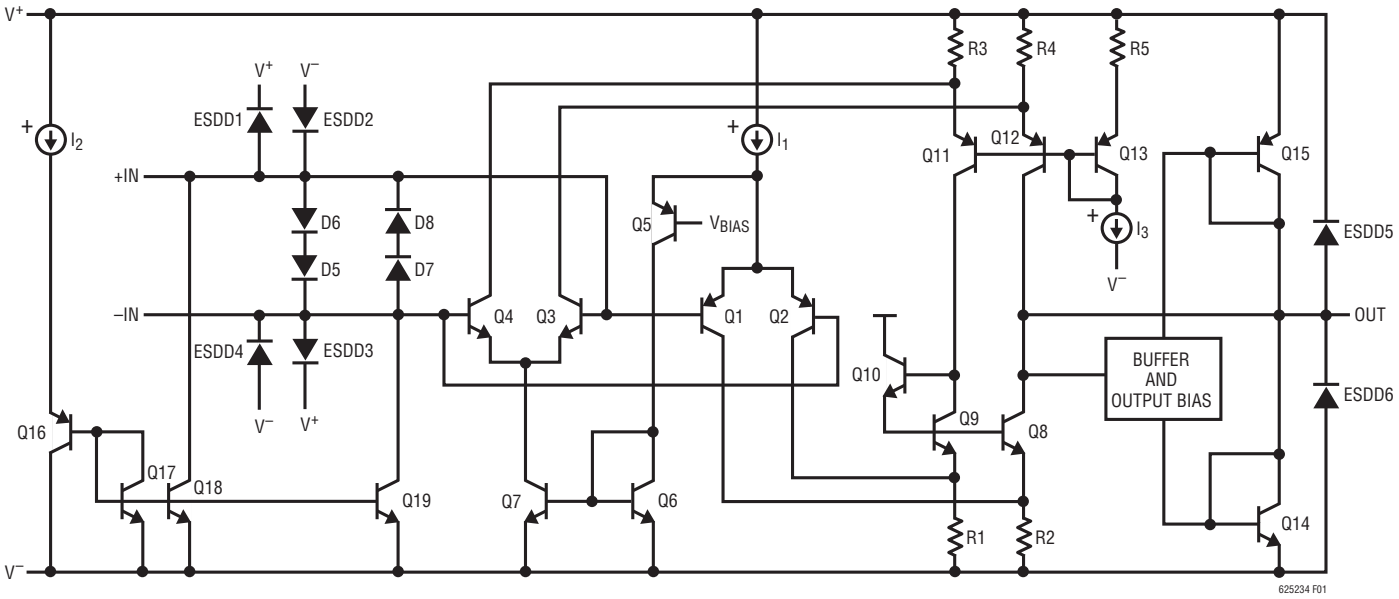



**Figure 1. LTC6253-7 Simplified Schematic Diagram**

## APPLICATIONS INFORMATION

### Input Offset Voltage

The offset voltage will change depending upon which input stage is active. The PNP input stage is active from the negative supply rail to approximately 1.2V below the positive supply rail, then the NPN input stage is activated for the remaining input range up to the positive supply rail with the PNP stage inactive. The offset voltage magnitude for the PNP input stage is trimmed to less than 350µV with 5V total supply at room temperature, and is typically less than 150µV. The offset voltage for the NPN input stage is less than 2.2mV with 5V total supply at room temperature.

### Input Bias Current

The LTC6253-7 uses a bias current cancellation circuit to compensate for the base current of the PNP input pair. This results in a typical $I_B$ of about 100nA. When the input common mode voltage is less than 200mV, the bias cancellation circuit is no longer effective and the input bias current magnitude can reach a value above 4µA. For common mode voltages ranging from 0.2V above the negative supply to 1.2V below the positive supply, the low input bias current allows the amplifiers to be used in applications with high source resistances where errors due to voltage drops must be minimized.

### Output

The LTC6253-7 has excellent output drive capability. The amplifiers can typically deliver 90mA of output drive current at a total supply of 5V. The maximum output current is a function of the total supply voltage. As the supply voltage to the amplifier decreases, the output current capability also decreases. Attention must be paid to keep the junction temperature of the IC below 150°C (refer to the Power Dissipation Section) when the output is in continuous short-circuit. The output of the amplifier has reverse-biased diodes connected to each supply. If the output is forced beyond either supply, extremely high current will flow through these diodes which can result in damage to the device. Forcing the output to even 1V beyond either supply could result in several hundred milliamps of current through either diode.

### Input Protection

The LTC6253-7's input stages are protected against a large differential input voltage of 1.4V or higher by 2 pairs of back-to-back diodes to prevent the emitter-base breakdown of the input transistors. In addition, the input and shutdown pins have reverse biased diodes connected to the supplies. The current in these diodes must be limited to less than 10mA. The amplifiers should not be used as comparators or in other open loop applications.

### ESD

The LTC6253-7 has reverse-biased ESD protection diodes on all inputs and outputs as shown in Figure 1.

There is an additional clamp between the positive and negative supplies that further protects the device during ESD strikes. Hot plugging of the device into a powered socket must be avoided since this can trigger the clamp resulting in larger currents flowing between the supply pins.

### Capacitive Loads

The LTC6253-7 has been optimized for speed and should not be used to drive large capacitors without resistive isolation. Increased capacitance at the output creates an additional pole in the open loop frequency response, worsening the phase margin. When driving capacitive loads, a resistor of 10Ω to 100Ω should be connected between the amplifier output and the capacitive load to avoid ringing or oscillation. The feedback should be taken directly from the amplifier output. Higher voltage gain configurations tend to have better capacitive drive capability than lower gain configurations due to lower closed loop bandwidth and hence higher phase margin. The graphs titled Series Output Resistor vs Capacitive Load demonstrate the transient response of the amplifier when driving capacitive loads with various series resistors.

## APPLICATIONS INFORMATION

### Feedback Components

When feedback resistors are used to set up gain, care must be taken to ensure that the pole formed by the feedback resistors and the parasitic capacitance at the inverting input does not degrade stability. For example if the amplifier is set up in a gain of +11 configuration with a gain resistor of 1k and a feedback resistor of 10k, a parasitic capacitance of 7pF (device + PC board) at the amplifier's inverting input will cause the part to oscillate, due to a pole formed at 25MHz. An additional capacitor of 0.7pF across the feedback resistor as shown in Figure 2 will eliminate any ringing or oscillation. In general, if the resistive feedback network results in a pole whose frequency lies within the closed loop bandwidth of the amplifier, a capacitor can be added in parallel with the feedback resistor to introduce a zero whose frequency is close to the frequency of the pole, improving stability.

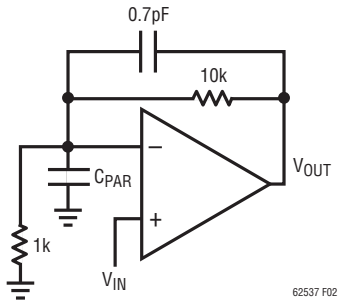



**Figure 2. 0.7pF Feedback Cancels Parasitic Pole**

### Shutdown

The LTC6253-7 has $\overline{SHDN}$ pins that can shut down the amplifier to 42µA typical supply current. The $\overline{SHDN}$ pin needs to be taken within 0.8V of the negative supply for the amplifier to shut down. When left floating, the $\overline{SHDN}$ pin is internally pulled up to the positive supply and the amplifier remains on.

### Power Dissipation

The LTC6253-7 is housed in a small 10-lead MS package and typically has a thermal resistance ($\theta_{JA}$) of 160°C/W. It is necessary to ensure that the die's junction temperature does not exceed 150°C. The junction temperature, $T_J$, is calculated from the ambient temperature, $T_A$, power dissipation, PD, and thermal resistance, $\theta_{JA}$:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

The power dissipation in the IC is a function of the supply voltage, output voltage and load resistance. For a given supply voltage with output connected to ground or supply, the worst-case power dissipation $P_{D(MAX)}$ occurs when the supply current is maximum and the output voltage at half of either supply voltage for a given load resistance. $P_{D(MAX)}$ is approximately (since $I_S$ actually changes with output load current) given by:

$$P_{D(MAX)} = (V_S \bullet I_{S(MAX)}) + \left(\frac{V_S}{2}\right)^2 / R_L$$

Example: For an LTC6253-7 operating on ±2.5V supplies and driving a 100Ω load to ground, the worst-case power dissipation is approximately given by

$$P_{D(MAX)}/Amp = (5 \bullet 4.8mA) + (1.25)^2/100 = 39.6mW$$

If both amplifiers are loaded simultaneously then the total power dissipation is 79.2mW.

At the Absolute Maximum ambient operating temperature, the junction temperature under these conditions will be:

$$T_J = T_A + P_D \bullet 160°C/W$$

$$= 125 + (0.079W \bullet 160°C/W) = 137°C$$

which is less than the absolute maximum junction temperature for the LTC6253-7 (150°C).

# TYPICAL APPLICATIONS

## ADC Driver with Gain

Figure 3 shows the LTC6253-7 acting as a gain of 7 stage driving the LTC2314-14 14-bit A/D converter. With a gain of 7V/V, for a 20.5kHz signal a handsome SFDR of 89dB can be obtained at a –1dBFS input signal, with an SNR of 72dB, at a sampling frequency of 2Msps. Figure 4 shows the FFT of the ADC's output.

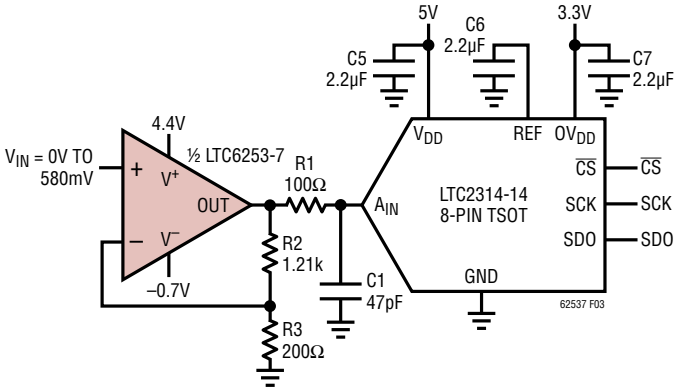



**Figure 3. ADC Driver with Gain**

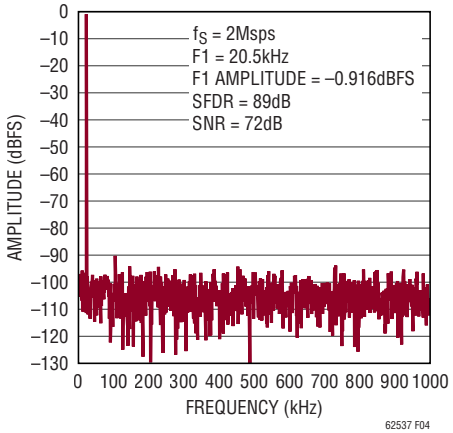



**Figure 4. Dynamic Performance, LTC6253-7 Driving LTC2314-14**

## High Speed Low Voltage Instrumentation Amplifier

Figure 5 shows a high speed three op amp instrumentation amplifier with a gain of 41V/V and bandwidth of 47MHz, operating from a total supply of 3.3V. Op amps U1 and U2

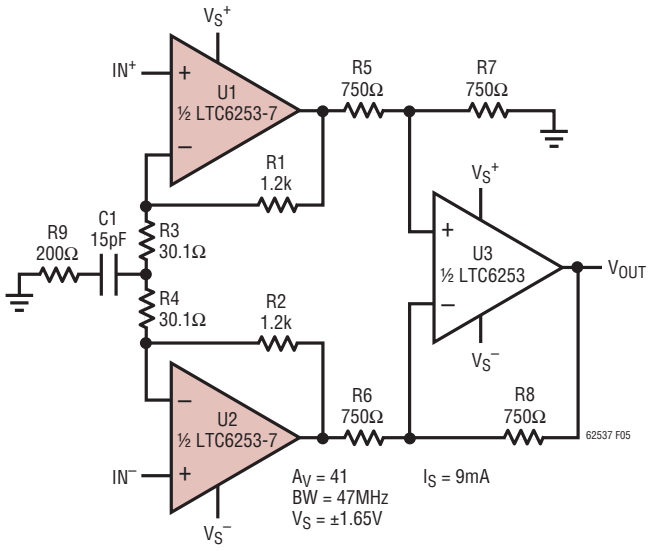



**Figure 5. High Speed Low Voltage Instrumentation Amplifier**

are channels from an LTC6253-7. Op amp U3 can be an LTC6252 or one channel of an LTC6253. An RC snubber is used at the common terminal of the 30Ω gain setting resistors to eliminate the effects of any board layout induced coupling from the output of an amplifier to the negative input of the other amplifier. Figure 6 shows the measured frequency response of the instrumentation amplifier for

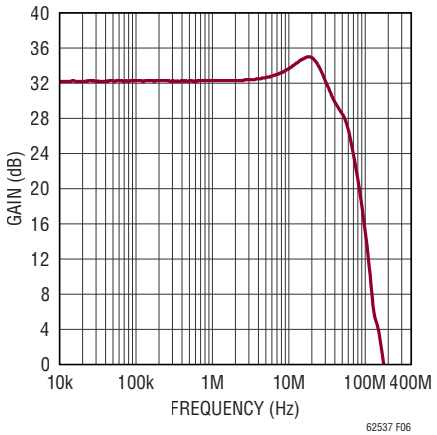



**Figure 6. Instrumentation Amplifier Frequency Response**

## TYPICAL APPLICATIONS

a load of 1k. Figure 7 shows the measured CMRR across frequency. Figure 8 shows the transient response with a 1.6$V_{P-P}$ output step, with the input applied to the positive input of the instrumentation amplifier, with the negative input grounded.

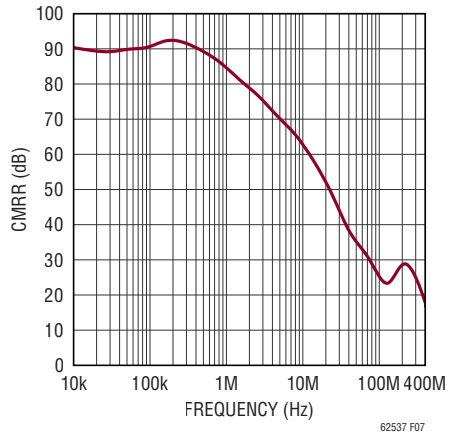



**Figure 7. Instrumentation Amplifier CMRR**

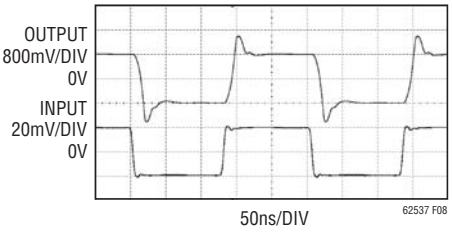



**Figure 8. Instrumentation Amplifier Transient Response**

### Using a Gain-of-7 Stable Op Amp to Achieve Low Closed Loop Gains

Many applications may demand higher slew rates and bandwidths associated with decompensated op amps like the LTC6253-7, but with lower closed loop gains. Any circuit using the LTC6253-7 will be stable as long as the noise gain (gain for any noise referred to the inputs of the operational amplifier) is 7 or higher. Figure 9 shows how such a circuit can be implemented. The overall signal gain is 1 + $R_F/R_G$, however the noise gain is 1 + $R_F/(R_G||R_C)$. Figure 10 shows the measured frequency response of such a circuit. The low frequency gain is 9.5dB (~3V/V) and is

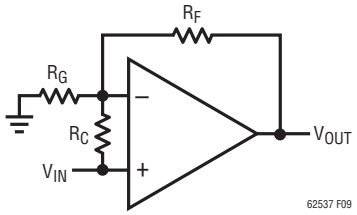



**Figure 9. Low Gain Stage with Higher Noise Gain**

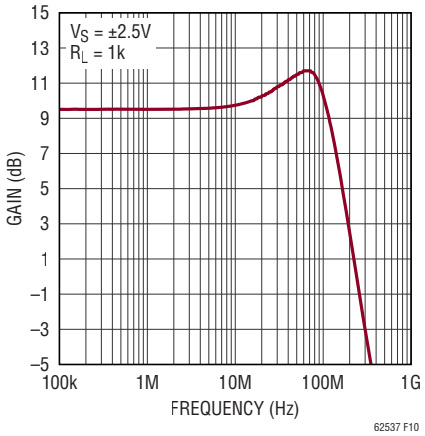



**Figure 10. Frequency Response, Low Gain Stage Using the LTC6253-7**

achieved by making $R_F$ = 499Ω and $R_G$ = 249Ω. Resistor $R_C$ is chosen to be 124Ω, leading to a noise gain of approximately 7V/V. The measured bandwidth of the circuit is an impressive 147MHz. Figure 11 shows a 4$V_{P-P}$ output at a frequency of 13MHz.

Note that for $R_G$ = ∞, $R_C$ = 82.5Ω, a closed loop gain of +1 can be obtained, with a noise gain of 7V/V, and such a circuit can be implemented with the LTC6253-7.

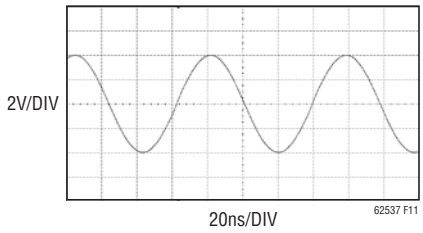
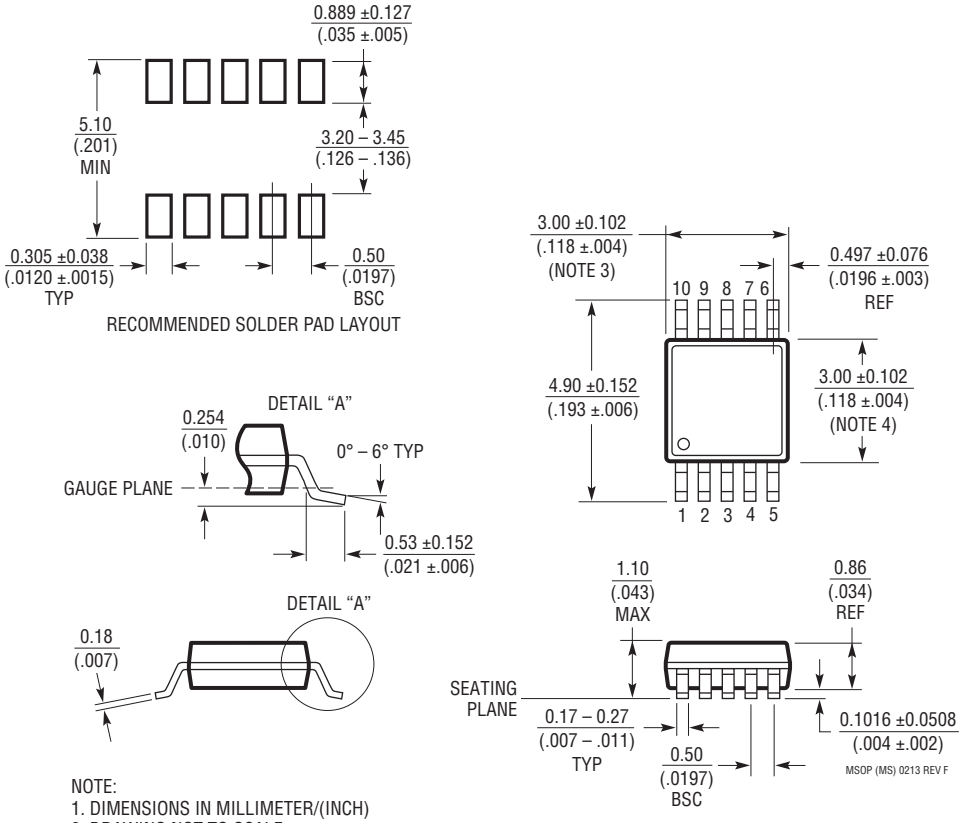



**Figure 11. Transient Response, Sinusoidal Input**

# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC6253-7#packaging for the most recent package drawings.**

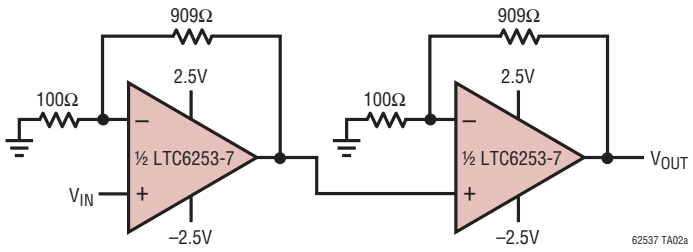
**MS Package**
**10-Lead Plastic MSOP**
(Reference LTC DWG # 05-08-1661 Rev F)



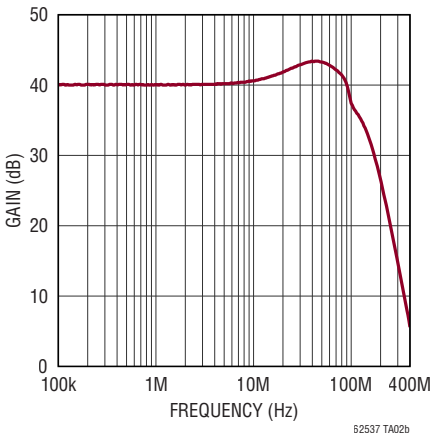

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

## TYPICAL APPLICATION

**101V/V 100MHz Gain Block**




**Frequency Response**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| **Operational Amplifiers** | | |
| LTC6252/LTC6253/ LTC6254 | Single/Dual/Quad High Speed Rail-to-Rail Input and Output Op Amps | 720MHz, 3.5mA, 2.75nV/√Hz, 280V/µs, 0.35mV, Unity Gain Stable |
| LTC6268-10/ LTC6269-10 | Single/Dual High Speed FET Input Op Amp | 4GHz, 4nV/√Hz, ±3$f_A$ Input Bias Current |
| LT1818/LT1819 | Single/Dual Wide Bandwidth, High Slew Rate Low Noise and Distortion Op Amps | 400MHz, 9mA, 6nV/√Hz, 2500V/µs, 1.5mV –85dBc at 5MHz |
| LT1806/LT1807 | Single/Dual Low Noise Rail-to-Rail Input and Output Op Amps | 325MHz, 13mA, 3.5nV/√Hz, 140V/µs, 550µV, 85mA Output Drive |
| LTC6246/LTC6247/ LTC6248 | Single/Dual/Quad High Speed Rail-to-Rail Input and Output Op Amps | 180MHz, 1mA, 4.2nV/√Hz, 90V/µs, 0.5mV |
| LT6230/LT6231/ LT6232 | Single/Dual/Quad Low Noise Rail-to-Rail Output Op Amps | 215MHz, 3.5mA, 1.1nV/√Hz, 70V/µs, 350µV |
| LT6200/LT6201 | Single/Dual Ultralow Noise Rail-to-Rail Input/Output Op Amps | 165MHz, 20mA, 0.95nV/√Hz, 44V/µs, 1mV |
| LT6202/LT6203/ LT6204 | Single/Dual/Quad Ultralow Noise Rail-to-Rail Op Amp | 100MHz, 3mA, 1.9nV/√Hz, 25V/µs, 0.5mV |
| LT1468 | 16-Bit Accurate Precision High Speed Op Amp | 90MHz, 3.9mA, 5nV/√Hz, 22V/µs, 175µV, –96.5dB THD at 10$V_{P-P}$, 100kHz |
| LT1801/LT1802 | Dual/Quad Low Power High Speed Rail-to-Rail Input and Output Op Amps | 80MHz, 2mA, 8.5nV√Hz, 25V/µs, 350µV |
| LT1028 | Ultralow Noise, Precision High Speed Op Amps | 75MHz, 9.5mA, 0.85nV/√Hz, 11V/µs, 40µV |
| LTC6350 | Low Noise Single-Ended to Differential Converter/ADC Driver | 33MHz (–3dB), 4.8mA, 1.9nV/√Hz, 240ns Settling to 0.01% 8$V_{P-P}$ |
| **ADCs** | | |
| LTC2393-16 | 1Msps 16-Bit SAR ADC | 94dB SNR |
| LTC2366 | 3Msps, 12-Bit ADC Serial I/O | 72dB SNR, 7.8mW No Data Latency TSOT-23 Package |
| LTC2365 | 1Msps, 12-Bit ADC Serial I/O | 73dB SNR, 7.8mW No Data Latency TSOT-23 Package |


Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com/LTC6253-7
LT 0216 • PRINTED IN USA

# Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

LTC6253HMS-7#PBF LTC6253IMS-7#PBF