

## FEATURES

- 155Mbps to 3.2Gbps Laser Diode Driver for VCSELs\*
- 60ps Rise and Fall Times, 10ps Deterministic Jitter
- Eye Diagram is Stable and Consistent Across Modulation Range and Temperature
- 1mA to 12mA Modulation Current
- Easy Board Layout, Laser can be Remotely Located if Desired
- No Input Matching or AC Coupling Components Needed
- On-Chip ADC for Monitoring Critical Parameters
- Digital Setup and Control with I<sup>2</sup>C™ Serial Interface
- Emulation and Set-Up Software Available\*\*
- Operates Standalone or with a Microprocessor
- On-Chip DACs Eliminate External Potentiometers
- Constant Current or Automatic Power Control
- First and Second Order Temperature Compensation
- On-Chip Temperature Sensor
- Extensive Eye Safety Features
- Single 3.3V Supply
- 4mm × 4mm QFN Package

## APPLICATIONS

- Gigabit Ethernet and Fibre Channel Transceivers
- SFF and SFP Transceiver Modules
- Proprietary Fiber Optic Links

## DESCRIPTION

The LTC<sup>®</sup>5100 is a 3.2Gbps VCSEL driver offering an unprecedented level of integration and high speed performance. The part incorporates a full range of features to ensure consistently outstanding eye diagrams. The data inputs are AC coupled, eliminating the need for external capacitors. The LTC5100 has a precisely controlled 50Ω output that is DC coupled to the laser, allowing arbitrary placement of the IC. No coupling capacitors, ferrite beads or external transistors are needed, simplifying layout, reducing board area and the risk of signal corruption. The unique output stage of the LTC5100 confines the modulation current to the ground system, isolating the high speed signal from the power supply to minimize RFI.

The LTC5100 supports fully automated production with its extensive monitoring and control features. Integrated 10-bit DACs eliminate the need for external potentiometers. An on-board 10-bit ADC provides the laser current and voltage, as well as monitor diode current and temperature. Status information is available from the I<sup>2</sup>C serial interface for feedback and statistical process control.

An internal digital controller compensates laser temperature drift and provides extensive laser safety features.

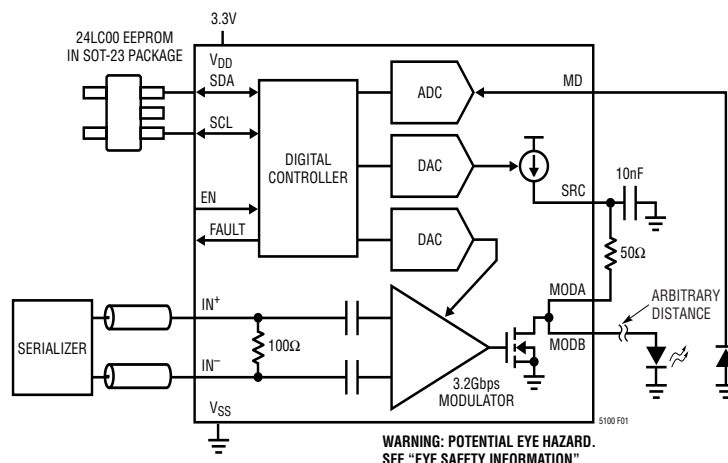
**LT**, LTC and LT are registered trademarks of Linear Technology Corporation.

I<sup>2</sup>C is a trademark of Philips Electronics N.V.

\*Vertical Cavity Surface Emitting Laser

\*\*Downloadable from [www.linear.com](http://www.linear.com)

## TYPICAL APPLICATION



**3.2Gbps Electrical Eye Diagram**

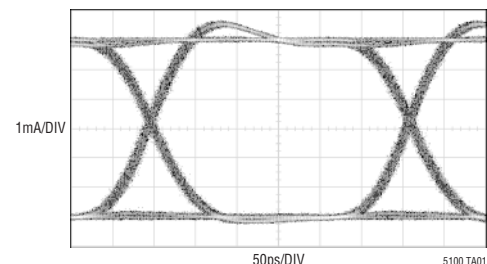


Figure 1. VCSEL Transmitter with Automatic Power Control

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## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{DD}$ ,  $V_{DD(HS)}$  ..... 4V

$IN^+$ ,  $IN^-$  ( $C_{ml\_en} = 1$ ) (Note 6)

Peak Voltage .....  $V_{DD(HS)} - 1.2V$  to  $V_{DD(HS)} + 0.3V$

Average Voltage .....  $V_{DD(HS)} - 0.6V$  to  $V_{DD(HS)} + 0.3V$

$IN^+$ ,  $IN^-$  ( $C_{ml\_en} = 0$ ) (Note 4) ..  $-0.3V$  to  $V_{DD(HS)} + 0.3V$

$C_{ml\_en} = 0$  (Note 4)

Peak Difference Between  $IN^+$  and  $IN^-$  .....  $\pm 2.5V$

Average Difference Between  $IN^+$  and  $IN^-$  .....  $\pm 1.25V$

MODA, MODB (Transmitter Disabled) ....  $-0.3V$  to  $2.75V$

MODA, MODB

(Transmitter Enabled) .....  $V_{DD(HS)} - 2.75V$  to  $2.75V$

EN, SDA, SCL, FAULT .....  $-0.3V$  to  $V_{DD} + 0.3V$

MD, SRC .....  $-0.3V$  to  $V_{DD}$

Ambient Operating Temperature Range ..  $-40^{\circ}C$  to  $85^{\circ}C$

Storage Temperature Range .....  $-65^{\circ}C$  to  $125^{\circ}C$

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>16-LEAD (4mm × 4mm) PLASTIC QFN</p> <p><math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 37^{\circ}C/W</math></p> <p>EXPOSED PAD IS <math>V_{SS}</math> (PIN 17)</p> <p>MUST BE SOLDERED TO PCB GROUND PLANE</p>	ORDER PART NUMBER
	LTC5100EUF
	UF PART MARKING
	5100

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ ;  $V_{DD} = V_{DD(HS)} = 3.3V$ ,  $I_S = 24mA$ ;  $I_M = 12mA$  ( $I_{MPP} = 24mA$ );  $49.9\Omega$ , 1% resistor from SRC (Pin 14) to MODA (Pin 11);  $50\Omega$ , 1% load AC coupled to MODB (Pin 10);  $10nF$ , 10% capacitor from SRC (Pin 14) to  $V_{SS}$ ;  $C_{ml\_en} = 0$ ,  $L_{pc\_en} = 1$ , transmitter enabled, unless otherwise noted. Test circuit in Figure 5.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Power Supply</b>					
$V_{DD}$ , $V_{DD(HS)}$ Operating Voltage	●	3.135	3.3	3.465	V
$V_{DD} + V_{DD(HS)}$ Quiescent Current, Excluding the SRC Pin Current (Note 2)	$V_{DD} = 3.465V$				
	Transmitter Disabled, Power_down_en = 1		4.5		mA
	Transmitter Enabled, $I_{S\_rng} = I_{M\_rng} = 3$ $I_{MPP} = 24mA$		54		mA
<b>High Speed Data Inputs (<math>IN^+</math> and <math>IN^-</math> Pins) (Test Circuit, Figure 5)</b>					
Input Signal Amplitude	Peak-to-Peak Differential Voltage (The Single-Ended Peak-to-Peak Voltage is One Half the Differential Voltage)		500 to 2400		mV <sub>p-p</sub>
Common Mode Input Signal Range (Note 3)	$C_{ml\_en} = 0$ (Note 4)	0	$V_{DD(HS)}$		V
Differential Input Resistance			80 to 120		$\Omega$
Common Mode Input Resistance	$C_{ml\_en} = 0$ (Note 5)		50		k $\Omega$
Open-Circuit Voltage	$C_{ml\_en} = 0$ (Note 5)		1.65		V
<b>SRC Pin Current, <math>I_S</math></b>					
Full-Scale $I_S$ Current	$I_{S\_rng} = 0$	6	9		mA
	$I_{S\_rng} = 1$	12	18		mA
	$I_{S\_rng} = 2$	18	27		mA
	$I_{S\_rng} = 3$	24	36		mA
Minimum Operating Current (Note 7)		1/16 of Full-Scale $I_S$ Current			
Resolution			10		Bits
SRC Pin Voltage Range		1.2	$V_{DD} - 200mV$		V

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**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD} = V_{DD(HS)} = 3.3\text{V}$ ,  $I_S = 24\text{mA}$ ;  $I_M = 12\text{mA}$  ( $I_{MPP} = 24\text{mA}$ );  $49.9\Omega$ , 1% resistor from SRC (Pin 14) to MODA (Pin 11);  $50\Omega$ , 1% load AC coupled to MODB (Pin 10);  $10\text{nF}$ , 10% capacitor from SRC (Pin 14) to  $V_{SS}$ ;  $\text{Cml\_en} = 0$ ,  $\text{Lpc\_en} = 1$ , transmitter enabled, unless otherwise noted. Test circuit in Figure 5.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Laser Bias Current, <math>I_B</math></b>					
Full-Scale Current (Note 8)	$I_{S\_rng} = 0$ $I_{S\_rng} = 1$ $I_{S\_rng} = 2$ $I_{S\_rng} = 3$	$6 - I_M$ $12 - I_M$ $18 - I_M$ $24 - I_M$	$9 - I_M$ $18 - I_M$ $27 - I_M$ $36 - I_M$		mA mA mA mA
Absolute Accuracy	SRC Pin and MODA, MODB Pin Currents Within Specified Voltage Ranges		$\pm 25$		%
Resolution			10		Bits
Linear Tempco Resolution			122		ppm/ $^\circ\text{C}$
Linear Tempco Range			$\pm 15625$		ppm/ $^\circ\text{C}$
Second Order Tempco Resolution			3.81		ppm/ $^\circ\text{C}^2$
Second Order Tempco Range			$\pm 488$		ppm/ $^\circ\text{C}^2$
Temperature Stability	$I_{b\_tc1} = 0$ , $I_{b\_tc2} = 0$		$\pm 500$		ppm/ $^\circ\text{C}$
Off-State Leakage	Transmitter Disabled, $V_{SRC} = 1.2\text{V}$			50	$\mu\text{A}$
<b>MODA, MODB Pin Current, <math>I_M</math></b>					
Full Scale, Peak-to-Peak Modulation Current (Note 9)	$I_{m\_rng} = 0$ $I_{m\_rng} = 1$ $I_{m\_rng} = 2$ $I_{m\_rng} = 3$	6 12 18 24	9 18 27 36		mA mA mA mA
Minimum Operating Current (Note 10)		1/8 of Full-Scale Peak-to-Peak Modulation Current			
Resolution (Note 11)			9		Bits
Current Stability	$I_{m\_tc1} = 0$ , $I_{m\_tc2} = 0$		$\pm 500$		ppm/ $^\circ\text{C}$
Voltage Range	Peak Transient Voltage on MODA and MODB	1.2		2.7	V
Absolute Accuracy of the Modulation Current			$\pm 25$		%
Linear Tempco Resolution			122		ppm/ $^\circ\text{C}$
Linear Tempco Range			$\pm 15625$		ppm/ $^\circ\text{C}$
Second Order Tempco Resolution			3.81		ppm/ $^\circ\text{C}^2$
Second Order Tempco Range			$\pm 484$		ppm/ $^\circ\text{C}^2$
Maximum Bit Rate			3.2		Gbps
Modulation Current Rise and Fall Times	20% to 80% Measured with K28.5 Pattern at 2.5Gbps		60		ps
Deterministic Jitter, Peak-to-Peak (Note 12)	Measured with K28.5 Pattern at 3.2Gbps		10		ps
Random Jitter, RMS (Note 13)			1		ps <sub>RMS</sub>
Pulse Width Distortion			10		ps
<b>Automatic Power Control (Note 14)</b>					
Minimum Operating Current for the Monitor Diode (Note 15)			20% of Full Scale Monitor Diode Current		
Temperature Stability	$I_{md\_tc1} = 0$ , $I_{md\_tc2} = 0$		$\pm 500$		ppm/ $^\circ\text{C}$
Monitor Diode Bias Voltage (Note 16)	$I_{MD} \leq 1600\mu\text{A}$		1.45		V

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD} = V_{DD(HS)} = 3.3\text{V}$ ,  $I_S = 24\text{mA}$ ;  $I_M = 12\text{mA}$  ( $I_{MPP} = 24\text{mA}$ );  $49.9\Omega$ , 1% resistor from SRC (Pin 14) to MODA (Pin 11);  $50\Omega$ , 1% load AC coupled to MODB (Pin 10);  $10\text{nF}$ , 10% capacitor from SRC (Pin 14) to  $V_{SS}$ ;  $Cml\_en = 0$ ,  $Lpc\_en = 1$ , transmitter enabled, unless otherwise noted. Test circuit in Figure 5.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Automatic Power Control (Note 14)</b>					
Temperature Compensation (Note 17)					
Linear Tempco Resolution			$254 \cdot I_{md\_nom}/1024$		ppm/ $^\circ\text{C}$
Linear Tempco Range			$\pm 32300 \cdot I_{md\_nom}/1024$		ppm/ $^\circ\text{C}$
<b>ADC</b>					
Resolution			10		Bits
<b>Source Current Measurement, <math>I_S</math> (SRC Pin Current)</b>					
Full Scale	$I_{s\_rng} = 0$		9		mA
	$I_{s\_rng} = 1$		18		mA
	$I_{s\_rng} = 2$		27		mA
	$I_{s\_rng} = 3$		36		mA
Accuracy			$\pm 3\%$ of Full Scale $\pm 25\%$ of Reading		
<b>Average Modulation Current Measurement, <math>I_M</math> (Note 18)</b>					
Full Scale	$I_{m\_rng} = 0$		9		mA
	$I_{m\_rng} = 1$		18		mA
	$I_{m\_rng} = 2$		27		mA
	$I_{m\_rng} = 3$		36		mA
Accuracy			$\pm 3\%$ of Full Scale $\pm 25\%$ of Reading		
<b>Laser Diode Voltage Measurement</b>					
Full Scale			3.5		V
Accuracy			$\pm 150\text{mV} \pm 10\%$ of Reading		
<b>Monitor Diode Current Measurement (Note 19)</b>					
Full Scale	$I_{md\_rng} = 0$		34		$\mu\text{A}$
	$I_{md\_rng} = 1$		136		$\mu\text{A}$
	$I_{md\_rng} = 2$		544		$\mu\text{A}$
	$I_{md\_rng} = 3$		2176		$\mu\text{A}$
Zero Scale	ADC Code = 0		1/8 of Full Scale		
Resolution Relative to Reading			0.2		%
Accuracy			$\pm 25\%$ of Reading		
<b>Temperature Measurement</b>					
Full Scale	Celsius		239		$^\circ\text{C}$
Sensitivity			0.500		$^\circ\text{C}/\text{LSB}$
<b>Termination Resistor Voltage Measurement</b>					
Full Scale	$I_{s\_rng} = 0$		400		mV
	$I_{s\_rng} = 1$		800		mV
	$I_{s\_rng} = 2$		1200		mV
	$I_{s\_rng} = 3$		1600		mV
Accuracy			$\pm 30\text{mV} \pm 10\%$ of Reading		
<b>Safety Shutdown, Undervoltage Lockout (UVLO)</b>					
Undervoltage Detection	$V_{DD}$ Decreasing		2.8		V
Undervoltage Detection Hysteresis			150		mV

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ;  $V_{DD} = V_{DD(HS)} = 3.3\text{V}$ ,  $I_S = 24\text{mA}$ ;  $I_M = 12\text{mA}$  ( $I_{MPP} = 24\text{mA}$ );  $49.9\Omega$ , 1% resistor from SRC (Pin 14) to MODA (Pin 11);  $50\Omega$ , 1% load AC coupled to MODB (Pin 10);  $10\text{nF}$ , 10% capacitor from SRC (Pin 14) to  $V_{SS}$ ;  $Cml\_en = 0$ ,  $Lpc\_en = 1$ , transmitter enabled, unless otherwise noted. Test circuit in Figure 5.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Bias Current Limit, <math>I_{B(LIMIT)}</math></b>					
Set Point Resolution			7		Bits
Set Point Range	$Is\_rng = 0$		9		mA
	$Is\_rng = 1$		18		mA
	$Is\_rng = 2$		27		mA
	$Is\_rng = 3$		36		mA
<b>Optical Power Limit</b> Automatic Power Control Mode Only, $Apc\_en = 1$					
Overpower Limit	Expressed in % Over the $I_{md}$ Set Point		50		%
Underpower Limit	Expressed in % Under the $I_{md}$ Set Point		-50		%
Safety Shutdown Response Time	Time from the Fault Occurance to Reduction of the Laser Bias Current to 10% of Nominal		100		$\mu\text{s}$
<b>FAULT Output, Open-Drain Mode, <math>Flt\_drv\_mode = 0</math></b>					
Output Low Voltage	$I_{OL} = 3.3\text{mA}$			0.4	V
Output High Leakage Current	$V_{FAULT} = 2.4\text{V}$			10	$\mu\text{A}$
<b>FAULT Output, Open-Drain Mode with 330<math>\mu\text{A}</math> Internal Pull Up, <math>Flt\_drv\_mode = 1</math></b>					
Output Low Voltage	$I_{OL} = 3.3\text{mA}$			0.4	V
Output High Current	$V_{FAULT} = 2.4\text{V}$		-280		$\mu\text{A}$
<b>FAULT Output, Open-Drain Mode with 500<math>\mu\text{A}</math> Internal Pull Up, <math>Flt\_drv\_mode = 2</math></b>					
Output Low Voltage	$I_{OL} = 3.3\text{mA}$			0.4	V
Output High Current	$V_{FAULT} = 2.4\text{V}$		-425		$\mu\text{A}$
<b>FAULT Output, Complementary Drive Mode, <math>Flt\_drv\_mode = 3</math></b>					
Output High Voltage	$I_{OH} = -3.3\text{mA}$	2.4			V
Output Low Voltage	$I_{OL} = 3.3\text{mA}$			0.4	V
<b>EN Input, <math>I_{b\_gain}</math> or (<math>Apc\_gain</math> in APC Mode) = 16, <math>I_{m\_gain} = 4</math>, <math>Is\_rng = 0</math>, <math>I_{m\_rng} = 0</math></b>					
Input Low Voltage				0.8	V
Input High Voltage		2			V
Input Low Current	$En\_polarity = 0$ (EN Active Low), $V_{EN} = 0\text{V}$		-10		$\mu\text{A}$
Input High Current	$En\_polarity = 0$ (EN Active Low), $V_{EN} = V_{DD}$		-10 to 10		$\mu\text{A}$
Input Low Current	$En\_polarity = 1$ (EN Active High), $V_{EN} = 0\text{V}$		-10 to 10		$\mu\text{A}$
Input High Current	$En\_polarity = 1$ (EN Active High), $V_{EN} = V_{DD}$		10		$\mu\text{A}$
Transmit Enable Time	Time from Active Transition on EN to 95% of Nominal Laser Power and 95% of Full Modulation. First Time Transmission is Enabled After Power On or with $Rapid\_restart\_en = 0$		100		ms
Transmit Re-Enable Time	Time from Active Transition on EN to 95% of Nominal Laser Power and 95% of Full Modulation. When Transmission is Re-Enabled After the First Time and with $Rapid\_restart\_en = 1$		1		ms
Transmit Disable Time	Time from Inactive Transition on EN to 5% of Nominal Laser Power		10		$\mu\text{s}$
Minimum Pulse Width Required to Clear a Latched Fault		10			$\mu\text{s}$

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = V_{DD(HS)} = 3.3\text{V}$ ,  $I_S = 24\text{mA}$ ;  $I_M = 12\text{mA}$  ( $I_{MPP} = 24\text{mA}$ );  $49.9\Omega$ , 1% resistor from SRC (Pin 14) to MODA (Pin 11);  $50\Omega$ , 1% load AC coupled to MODB (Pin 10);  $10\text{nF}$ , 10% capacitor from SRC (Pin 14) to  $V_{SS}$ ;  $\text{Cml\_en} = 0$ ,  $\text{Lpc\_en} = 1$ , transmitter enabled, unless otherwise noted. Test circuit in Figure 5.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SCL, SDA</b>					
SCL, SDA Input Low Voltage, $V_{IL}$		-0.5		$0.3 \cdot V_{DD}$	V
SCL, SDA Input High Voltage, $V_{IH}$		$0.7 \cdot V_{DD}$		$V_{DD} + 0.5$	V
SCL, SDA Input Low Current (Note 21)	$V_{SDA}, V_{SCL} = 0.1 \cdot V_{DD}$		-100		$\mu\text{A}$
SCL, SDA Input High Current (Note 21)	$V_{SDA}, V_{SCL} = 0.9 \cdot V_{DD}$		-100		$\mu\text{A}$
SCL, SDA Output Low Voltage	$I_{OL} = 3\text{mA}$	0		0.4	V
Hysteresis			280		mV
<b>Serial Interface Timing (Note 20)</b>					
SCL Clock Frequency				100	kHz
Hold Time (Repeated) START Condition. After This Period the First Clock Pulse is Generated		4			$\mu\text{s}$
Low Period of the SCL Clock		4.7			$\mu\text{s}$
High Period of the SCL Clock		4			$\mu\text{s}$
Set-Up Time for a Repeated START Condition		4.7			$\mu\text{s}$
Data Hold Time		0		3.45	$\mu\text{s}$
Data Set-Up Time		250			ns
Input Rise Time of Both SDA and SCL Signals				1000	ns
Output Fall Time of SCL and SDA from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from $10\text{pF}$ to $400\text{pF}$				300	ns
Set-Up Time for STOP Condition		4			$\mu\text{s}$
Bus Free Time Between a STOP and START Condition		4.7			$\mu\text{s}$
Capacitive Load for Each Bus Line				400	pF
Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)		$0.1 \cdot V_{DD}$			V
Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)		$0.2 \cdot V_{DD}$			V

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** The quiescent  $V_{DD}$  and  $V_{DD(HS)}$  currents refer to the current with zero SRC pin current (i.e., the laser is operating with zero bias current and zero modulation current). The total power supply current is the quiescent current plus the SRC pin current,  $I_S$ , plus any current sunk from  $IN^+$  and  $IN^-$ .

**Note 3:** The peak transient voltage at the  $IN^+$  and  $IN^-$  pins must not exceed the range of  $-300\text{mV}$  to  $V_{DD(HS)} + 300\text{mV}$ .

**Note 4:** When  $\text{Cml\_en} = 0$  (not in CML mode), the termination is  $100\Omega$  differential with  $50\text{k}$  common mode to  $V_{DD(HS)}/2$ .

**Note 5:** The common mode input resistance is measured relative to  $V_{DD(HS)}/2$  with the inputs tied together.

**Note 6:** When  $\text{Cml\_en} = 1$  (CML mode), the termination is nominally  $50\Omega$  to  $V_{DD(HS)}$  on each of the  $IN^+$  and  $IN^-$  pins.

**Note 7:** The SRC pin current can be programmed to near zero in each range, but the recommended minimum operating level is 1/16 of full scale.

**Note 8:** The laser bias current is the average current delivered to the laser. It is equal to the SRC pin current minus the average modulation current at the MODA and MODB pins, or  $I_B = I_S - I_M$ . Full scale for the bias current therefore depends on  $I_{S\_rng}$  and the actual modulation current.

**Note 9:** The MODA and MODB pins are connected on-chip. The modulation current refers to the sum of the currents on these pins.  $I_M$  refers to the total average current at the MODA and MODB pins.  $I_{MPP}$  refers to the total peak-to-peak modulation current at the MODA and MODB pins.  $I_{MPP}$  differs from the laser modulation current,  $I_{MOD}$ .  $I_{MPP}$  splits between the laser and the termination resistor according to  $I_{MOD} = I_{MPP} \cdot R_T / (R_T + R_{LD})$ , where  $R_T$  is the value of the termination resistor and  $R_{LD}$  is the dynamic resistance of the laser diode.

## ELECTRICAL CHARACTERISTICS

**Note 10:** The modulation current can be programmed to near zero in each range, but the high speed performance is not guaranteed for currents less than the specified minimum.

**Note 11:** The effective resolution of the modulation current is 9 bits because the modulation servo system uses only one-half of the 10-bit ADC range.

**Note 12:** As defined in ANSI x3.230, Annex A, deterministic jitter is the peak-to-peak deviation of the 50% crossings of the modulation signal when compared to the ideal time crossings. The specification for the LTC5100 pertains to the electrical modulation signal. The K28.5 pattern is the repeating sequence 00111110101100000101.

**Note 13:** Random jitter is the standard deviation of the 50% crossings of the electrical modulation signal as measured by an oscilloscope. It is measured with a 1GHz square wave after quadrature subtraction of the random jitter of the pulse generator and oscilloscope. Peak-to-peak random jitter is defined as 14 times the RMS random jitter.

**Note 14:** The LTC5100 digitizes and servo controls the logarithm of the monitor diode current. Many of the characteristics of the APC system, such as range and resolution, are determined by the ADC.

**Note 15:** The minimum practical operating current for the monitor diode is determined by servo settling time considerations.

**Note 16:**  $I_{MD}$  must be less than 25 $\mu$ A, 100 $\mu$ A, 400 $\mu$ A and 1600 $\mu$ A corresponding to  $lmd\_rng = 0, 1, 2, 3$ .

**Note 17:** The temperature coefficients of the monitor diode current depend on the  $I_{MD}$  setting because of the logarithmic relationship between the set point and the monitor diode current.  $lmd\_nom$  is the digital code setting for the nominal monitor diode current.  $lmd\_nom$  lies between 0 and 1023.

**Note 18:** The ADC digitizes the average modulation current, which is 50% of the peak-to-peak current for a 50% duty cycle signal.

**Note 19:** The LTC5100 ADC digitizes the logarithm of the monitor diode current. This implies that the ADC resolution is a constant percentage of reading and that the monitor diode current is non-zero when the ADC reads zero. See the Design Notes for further information.

**Note 20:** Serial interface timing is guaranteed by design from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

**Note 21:** The LTC5100 has 100 $\mu$ A nominal pull-up current sources on the SCL and SDA pins to eliminate the need for external pull-up resistors when connected to a single EEPROM device. The LTC5100 meets the maximum rise time specification of 1000ns with external I<sup>2</sup>C bus capacitances up to 25pF. Example: 10pF EEPROM + 150mm trace ~ 25pF.

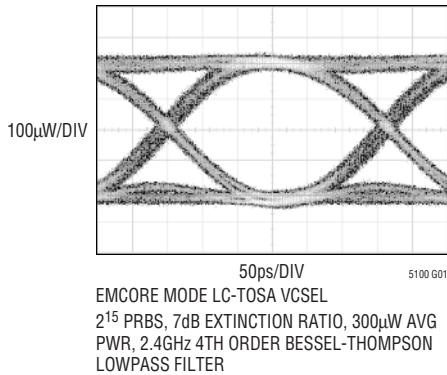
**Note 22:**  $V_{DD}$  and  $V_{DD(HS)}$  must be tied together on the PC board.



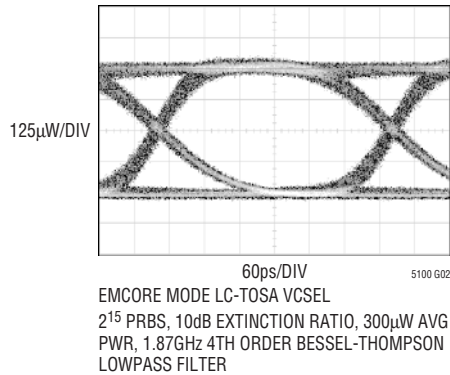
## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = V_{DD(HS)} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $Cml\_en = 0$ ,  $Lpc\_en = 1$ , transmitter enabled, unless otherwise noted. Test circuit shown in Figure 5.

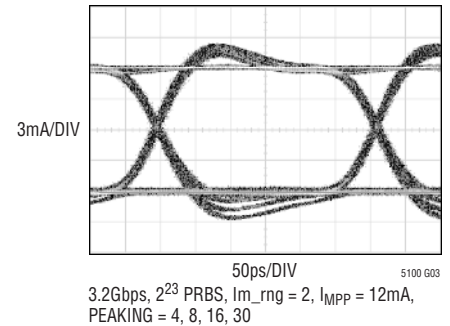
**Optical Eye Diagram at 3.2Gbps  
with 850nm VCSEL**



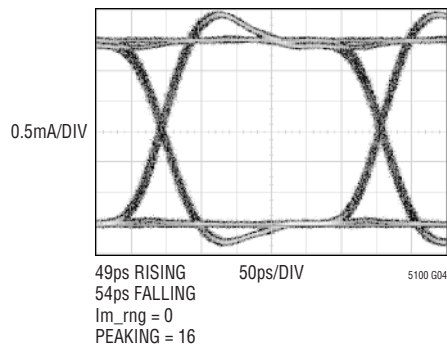
**Optical Eye Diagram at 2.5Gbps  
with 850nm VCSEL**



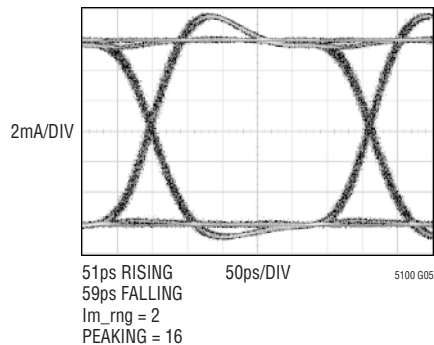
**Effect of Peaking Control on the  
Electrical Eye Diagram**



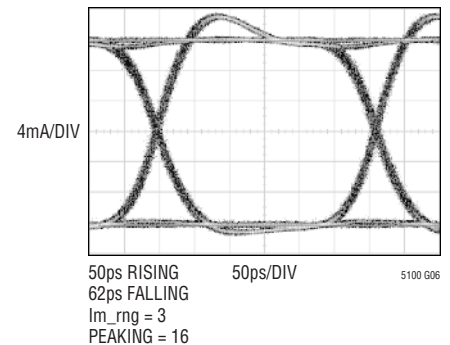
**Electrical Eye Diagram at 25°C  
3.2Gbps, 2<sup>23</sup> PRBS,  $I_{MPP} = 3mA$**



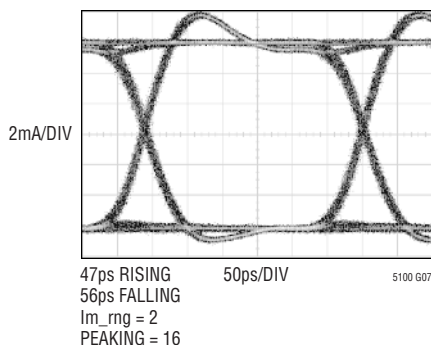
**Electrical Eye Diagram at 25°C  
3.2Gbps, 2<sup>23</sup> PRBS,  $I_{MPP} = 12mA$**



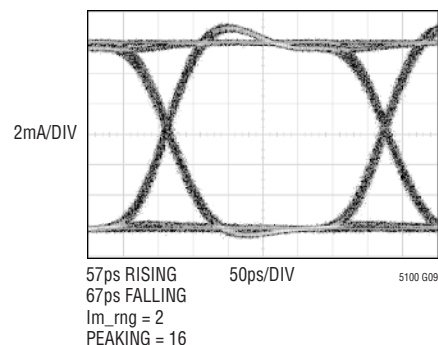
**Electrical Eye Diagram at 25°C  
3.2Gbps, 2<sup>23</sup> PRBS,  $I_{MPP} = 24mA$**



**Electrical Eye Diagram at -40°C,  
3.2Gbps, 2<sup>23</sup> PRBS,  $I_{MPP} = 12mA$**



**Electrical Eye Diagram at 85°C,  
3.2Gbps, 2<sup>23</sup> PRBS,  $I_{MPP} = 12mA$**

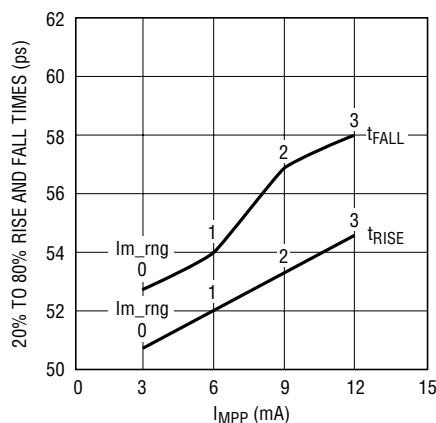




## TYPICAL PERFORMANCE CHARACTERISTICS

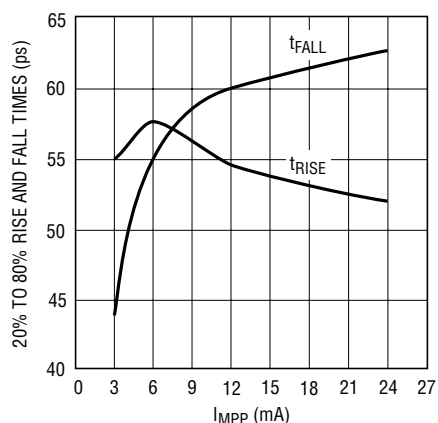
$V_{DD} = V_{DD(HS)} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $C_{ml\_en} = 0$ ,  $L_{pc\_en} = 1$ , transmitter enabled, unless otherwise noted. Test circuit shown in Figure 5.

**Rise and Fall Times vs  $I_M$  at the Midpoint of Each  $I_{m\_rng}$**



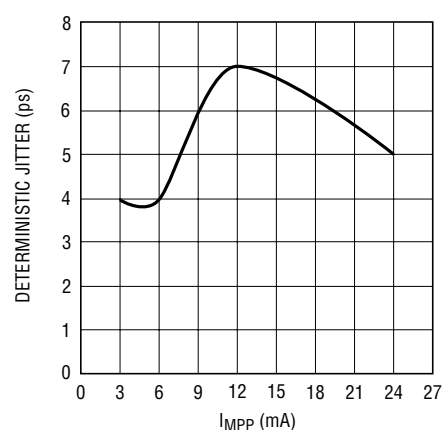
5100 G13

**Rise and Fall Times vs  $I_{MPP}$  for  $I_{m\_rng} = 3$**



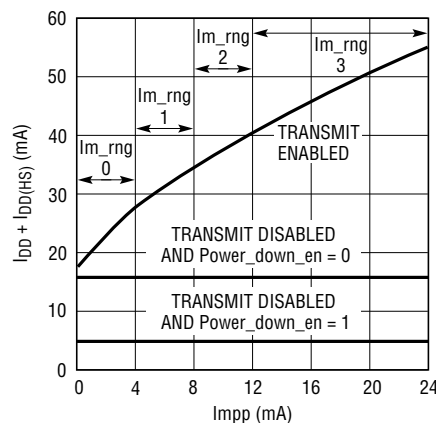
5100 G14

**Deterministic Jitter vs  $I_{MPP}$  for  $I_{m\_rng} = 3$**



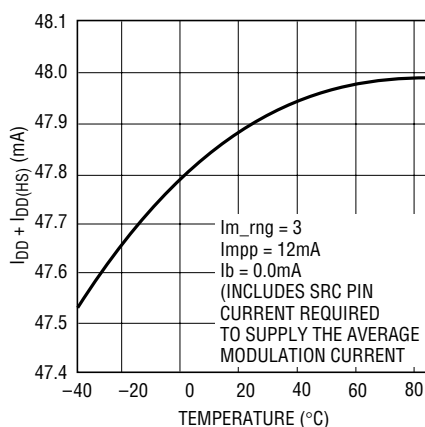
5100 G15

**Supply Current vs Modulation Level (Excluding Laser Current)**



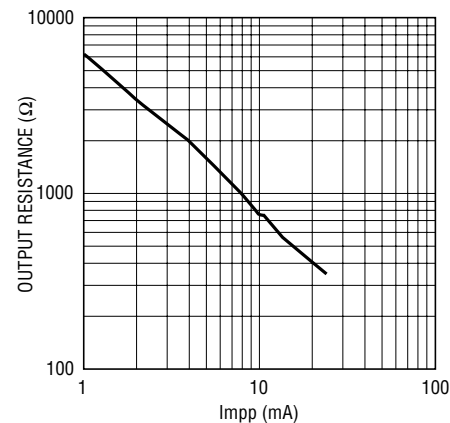
5100 G16

**Supply Current vs Temperature**



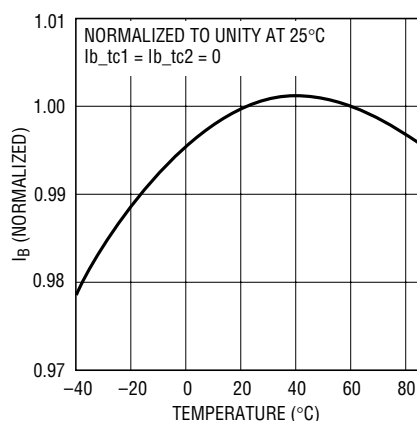
5100 G17

**Modulator Output Resistance vs Modulation Level**



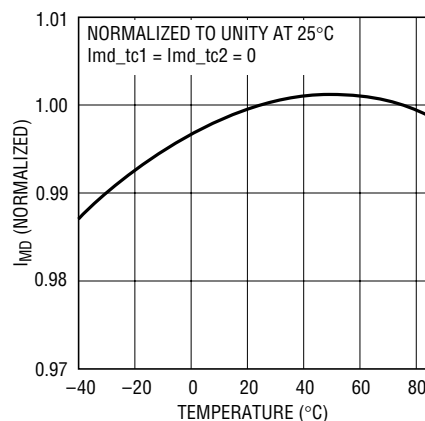
5100 G18

**Laser Bias Current vs Temperature in CCC Mode**



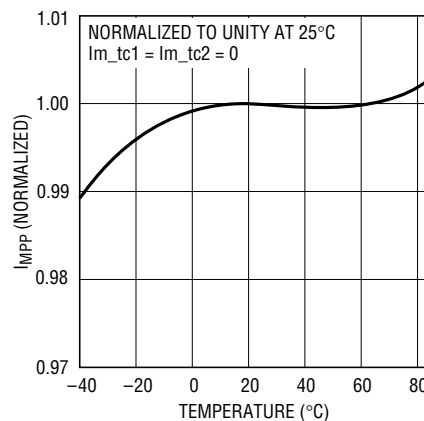
5100 G20

**Monitor Diode Current vs Temperature in APC Mode**



5100 G21

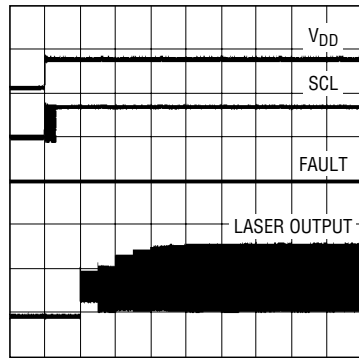
**Laser Modulation Current vs Temperature,  $I_{m\_rng} = 1$**

5100 G22  
sn5100 5100fs

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{DD} = V_{DD(HS)} = 3.3V$ ,  $T_A = 25^\circ C$ ,  $C_{ml\_en} = 0$ ,  $L_{pc\_en} = 1$ , transmitter enabled, unless otherwise noted.

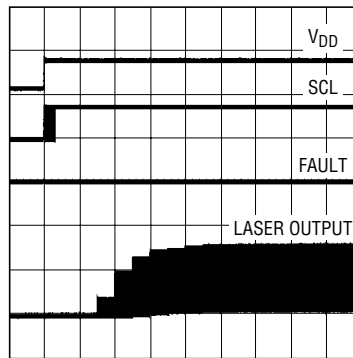
Hot Plug with EN Active in CCC Mode



10ms/DIV

5100 G23

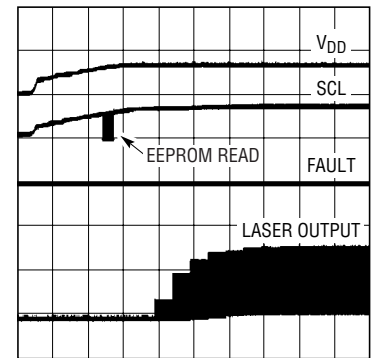
Hot Plug with EN Active in APC Mode



10ms/DIV

5100 G24

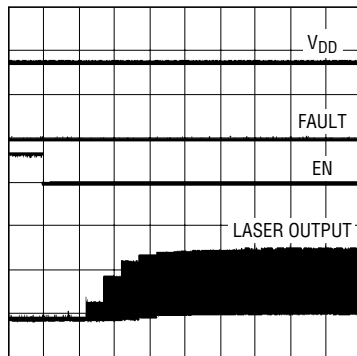
Start-Up with Slow Ramping Supply in APC Mode



10ms/DIV

5100 G25

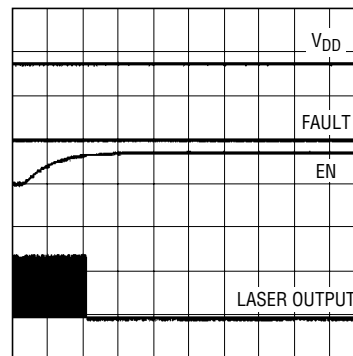
Transmitter Enable



5μs/DIV

5100 G26

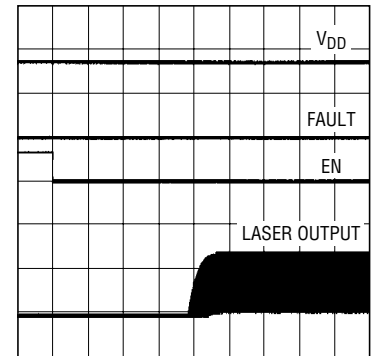
Transmitter Disable



5μs/DIV

5100 G27

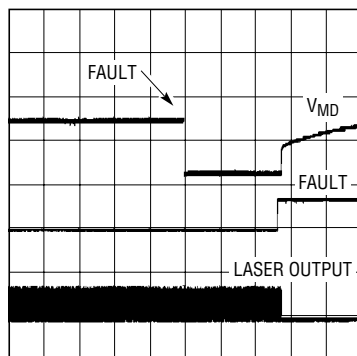
Transmitter Enable, Rapid Restart



10μs/DIV

5100 G28

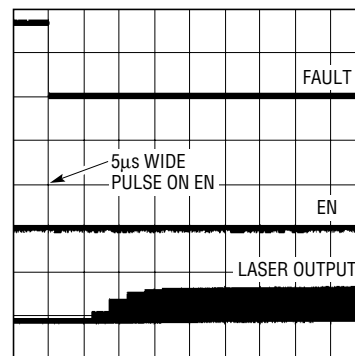
Response to Fault



10μs/DIV

5100 G29

Fault Recovery Time



10ms/DIV

5100 G30

## PIN FUNCTIONS

**V<sub>SS</sub> (Pins 1, 4, 9, 12, 17):** Ground for Digital, Analog and High Speed Circuitry. These pins are internally connected. Connect Pins 1, 4, 9 and 12 to the ground plane with minimal trace lengths. Place a minimum of four vias (preferably nine vias) to the ground plane in the Exposed Pad area. Most of the high speed modulation current is returned through the Exposed Pad (Pin 17).

**IN<sup>+</sup>, IN<sup>-</sup> (Pins 2, 3):** High Speed Laser Modulation Inputs. The inputs are differential with internal termination resistors. The input amplifier is internally AC coupled. With current mode logic (CML) enabled, the inputs are independently terminated to V<sub>DD(HS)</sub> with 50Ω resistors. With CML disabled, the inputs provide 100Ω differential termination and permit rail-to-rail common mode range. The input pins can be AC coupled with external capacitors. When externally AC coupled, the input pins self-bias to V<sub>DD(HS)</sub>/2. The Cml\_en bit selects the termination mode.

**FAULT (Pin 5):** Signals One of Five Safety Fault Conditions: laser overcurrent, overpower, underpower, power supply undervoltage and memory load error. The pin can be programmed active high or active low with the Flt\_pin\_polarity bit. The FAULT pin can be programmed to four different drive modes with the Flt\_drv\_mode bits.

**SDA, SCL (Pins 6, 7):** Serial Interface Data and Clock Signals. The pins are open drain with a 100μA internal pull-up current. An external pull-up resistor can be added to drive larger capacitive loads.

**V<sub>DD(HS)</sub> (Pin 8):** Power Input for the High Speed Laser Modulation Circuitry. Filter this pin with a ferrite bead and bypass the pin directly to the ground plane with a 10nF ceramic capacitor.

**MODA, MODB (Pins 11, 10):** High Speed Laser Modulation Outputs. MODA and MODB are connected on-chip and driven by an open-drain output transistor. One of these pins should be connected to the laser. The other should be connected to a termination resistor. See the Applications Information section for details.

**MD (Pin 13):** Monitor Diode Input for Automatic Power Control of the Laser Bias Current. The MD pin allows connection to the cathode or anode of the monitor diode. The Md\_polarity bit selects the polarity of the monitor diode.

**SRC (Pin 14):** Current Source for Biasing the Laser. See the Applications Information section for details.

**EN (Pin 15):** Transmitter Enable and Disable Input. This input is TTL compatible and can be programmed for active high or active low operation with the En\_polarity bit. An internal 10μA current source disables the transmitter if the EN pin becomes disconnected. This safety feature operates whether the EN pin is active high or active low.

**V<sub>DD</sub> (Pin 16):** Power Input for Digital and Low Speed Analog Circuitry. Connect this pin to V<sub>DD(HS)</sub> (Pin 8) with a short trace. No bypassing is needed at the V<sub>DD</sub> pin if the trace length to the V<sub>DD(HS)</sub> bypass capacitor is less than 10mm long.

## BLOCK DIAGRAM

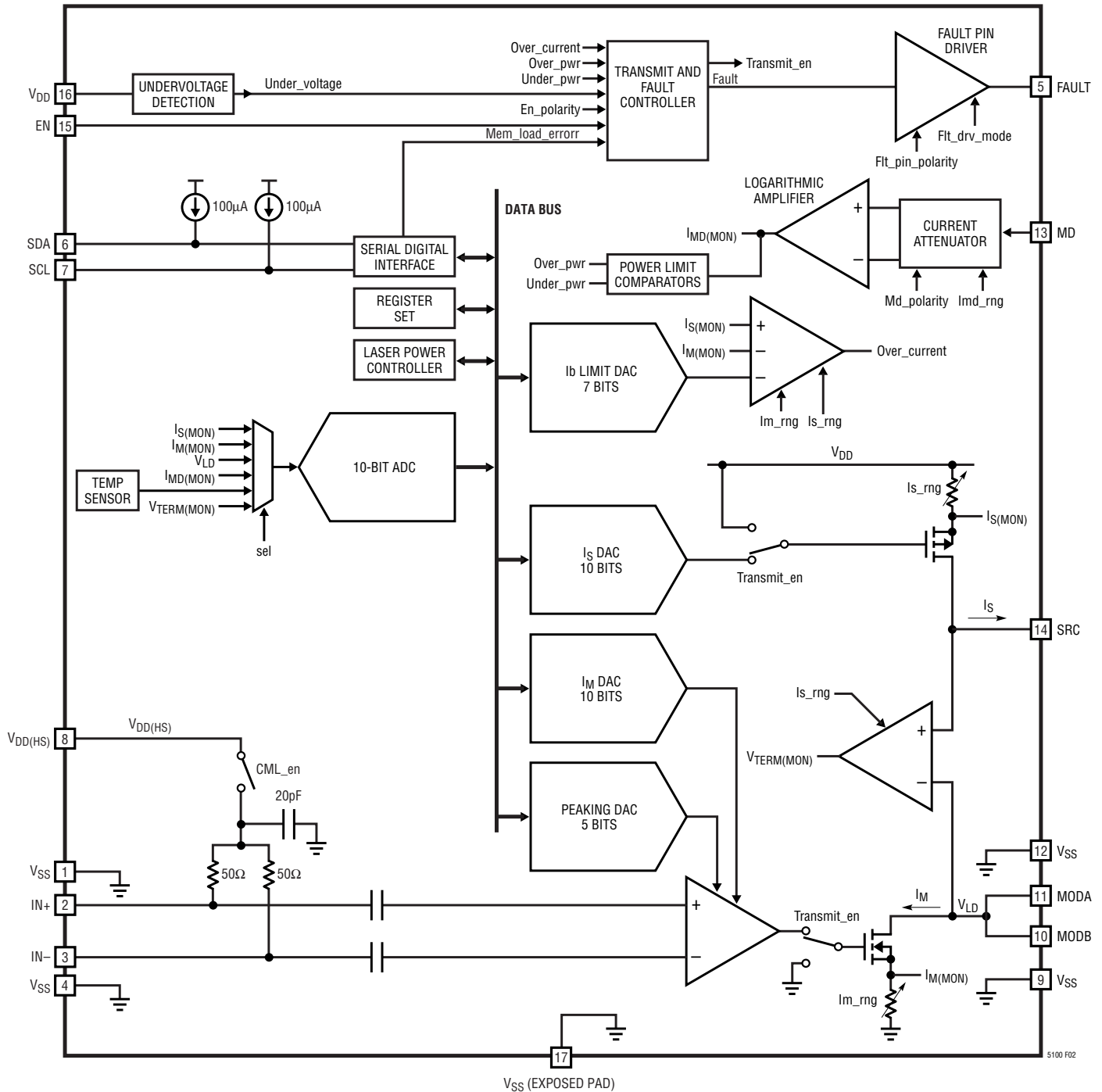


Figure 2. Block Diagram

## FUNCTIONAL DIAGRAMS

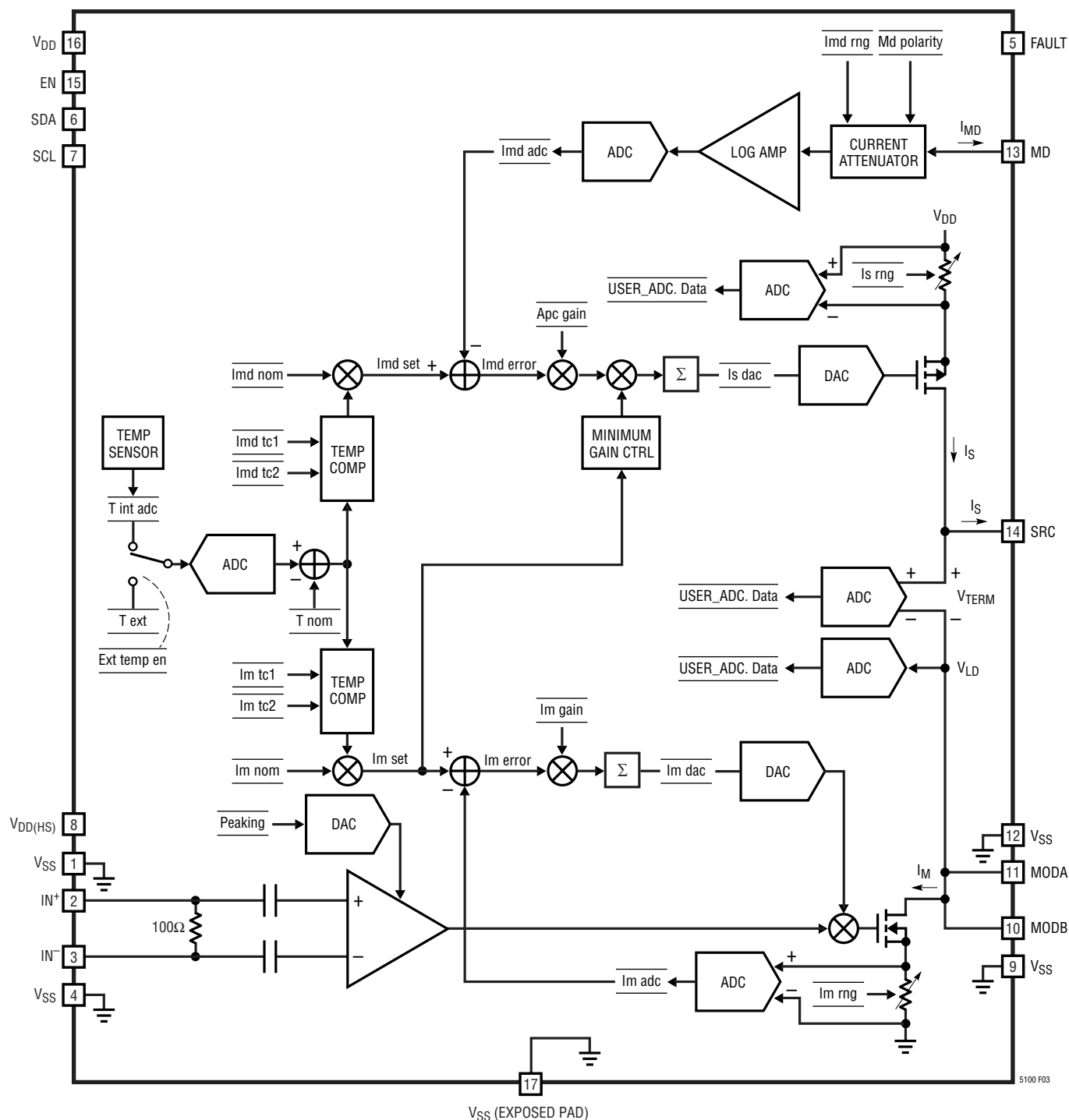


Figure 3. Functional Diagram—Automatic Power Control Mode

## FUNCTIONAL DIAGRAMS

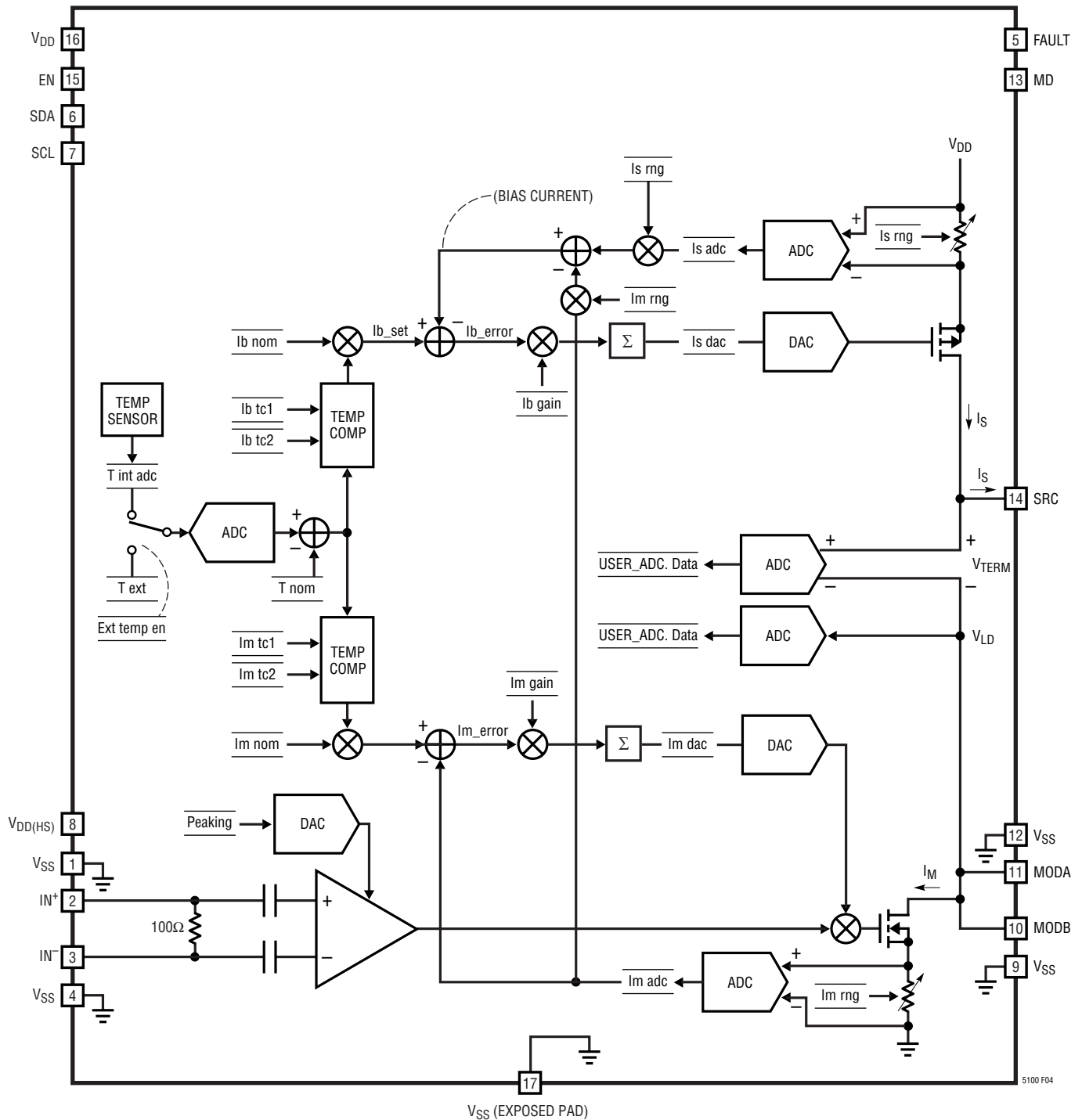


Figure 4. Functional Diagram—Constant Current Control Mode

## TEST CIRCUIT

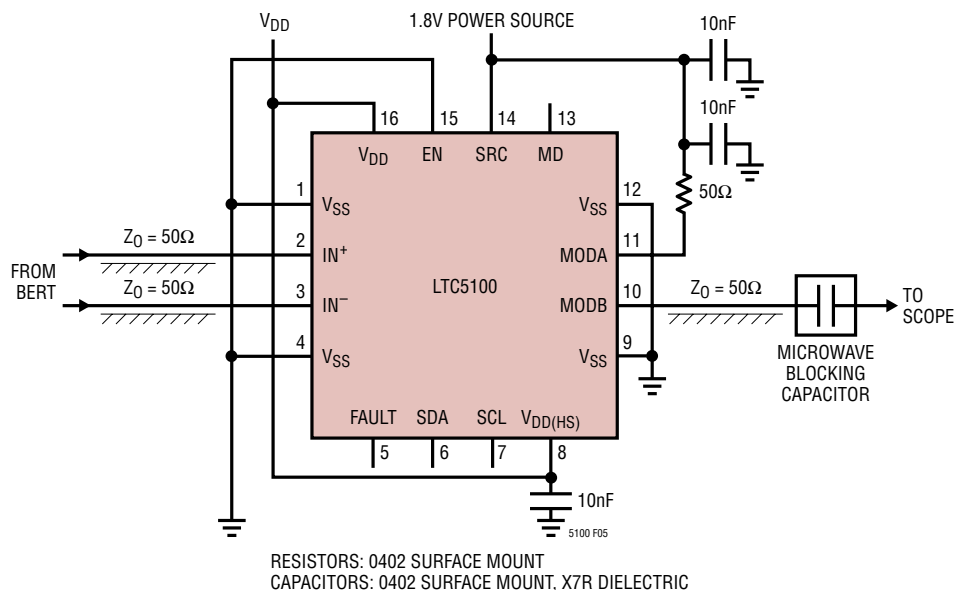


Figure 5. Test Circuit

## EQUIVALENT INPUT AND OUTPUT CIRCUITS

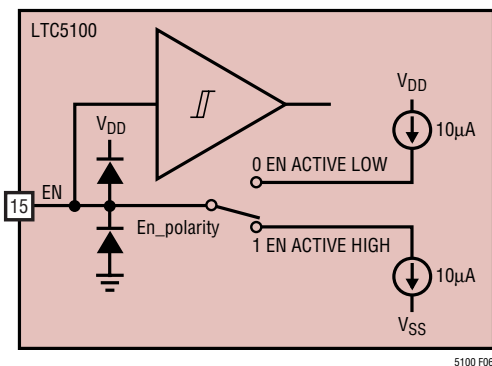


Figure 6. Equivalent Circuit for the EN Pin

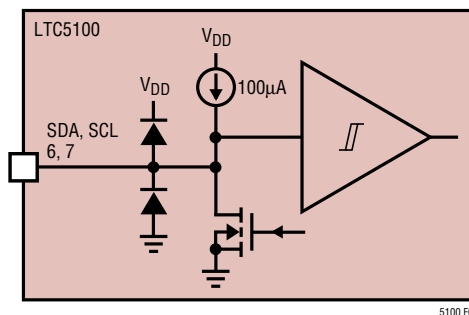


Figure 7. Equivalent Circuit for the SDA and SCL Pins

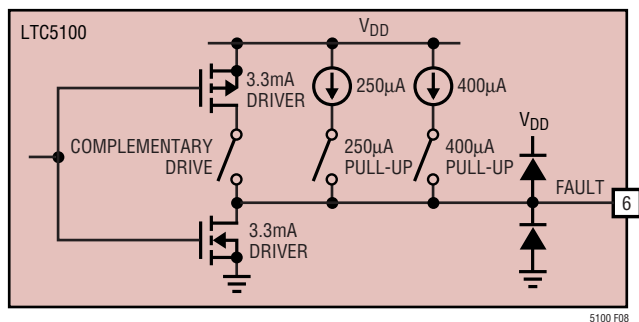


Figure 8. Equivalent Circuit for the FAULT Pin.  
All Switches are Open in Open-Drain Mode

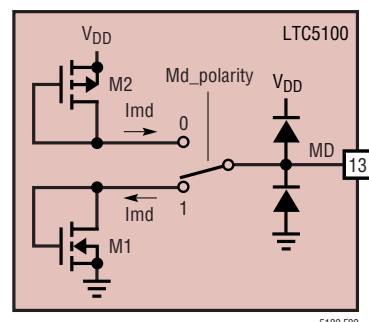


Figure 9. Equivalent Circuit for the MD Pin

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## EQUIVALENT INPUT AND OUTPUT CIRCUITS

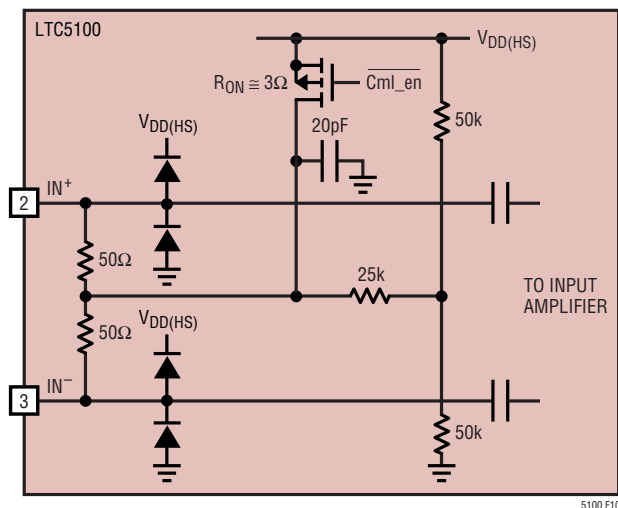


Figure 10. Equivalent Circuit for the IN<sup>+</sup> and IN<sup>-</sup> Pins

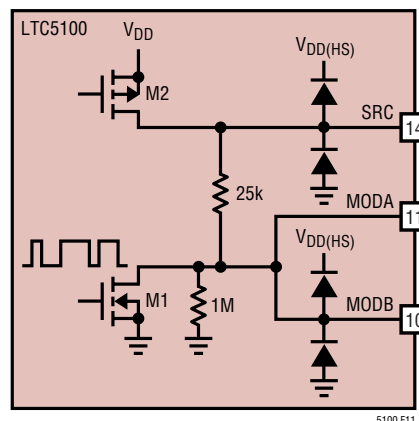


Figure 11. Equivalent Circuit for the SRC, MODA and MODB Pins

## OPERATION

### OVERVIEW

(Refer to Figure 1 and the Block Diagram in Figure 2)

The LTC5100 is optimized to drive common cathode VCSELs in high speed fiber optic transceivers. The chip incorporates several features that make it very compact and easy-to-use while delivering exceptional high speed performance. Only a capacitor, a resistor and a small EEPROM (excluding laser diode and power supply filtering) are needed to build a complete fiber optic transmitter. Digital control over the I<sup>2</sup>C serial interface allows fully automated laser setup to improve manufacturing efficiency. The LTC5100's extensive set of eye safety features meet GBIC and SFF requirements but go beyond the standards with open-pin protection, redundant transmitter enable controls and other interlocks.

10-bit integrated DACs set laser bias and modulation levels, eliminating the cost and space of digital potentiometers. A multiplexed ADC allows monitoring of temperature and laser operating conditions in production or field operation. Laser bias and modulation currents are digitally temperature compensated to second order for tight control of average power and extinction ratio. The LTC5100

provides both constant current and automatic power control of the laser bias current. In automatic power control mode, special circuitry maintains constant settling time in spite of variations in the laser slope efficiency and monitor diode response characteristics.

The high speed inputs of the LTC5100 are internally terminated in 50Ω and internally AC coupled, eliminating all external components at the inputs. The modulation output is DC coupled to the laser and presents a high quality resistive drive impedance to deliver very fast and clean eye diagrams in spite of laser impedance variations. The modulation output is capable of driving significant lengths of transmission line, allowing the LTC5100 to be placed at an arbitrary distance from the laser. This feature allows for packaging flexibility within the module.

The LTC5100 minimizes electromagnetic interference (EMI) with several architectural features. The unique design of the driver output forces the high speed modulation current to circulate only in the laser and ground system. The high speed amplifier chain and the digital circuitry are internally filtered and decoupled to further reduce power supply noise generation.

## OPERATION

### LASER BIAS AND MODULATION

#### Modulator Architecture

The LTC5100 drives common cathode lasers using a method called “shunt switching”. As shown in Figure 12, shunt switching involves sourcing DC current into the laser diode and shunting part of that current with a high speed current switch to produce the required modulation. The SRC pin provides the DC current and the MODA, MODB pins (which are connected on chip) provide the high speed modulation current. This technique results in a very fast, single-ended driver that confines the high speed modulation current to the laser and ground system. The LTC5100 actually uses a modified shunt switching scheme in which the source current is delivered through a “termination” resistor,  $R_T$ , that is bypassed to ground with a large capacitor. The resistor brings three advantages to the modulation stage. First, it gives the modulator a precise resistive output impedance to damp ringing and absorb reflections from the laser. Second, the resistor isolates the capacitance of the SRC pin from the high speed signal path, further improving modulation speed. Third, the resistor and capacitor heavily filter the high speed output signal so that it does not modulate the power supply and cause radiation or interference. On-chip decoupling of the high speed amplifiers further reduces power supply noise generation.

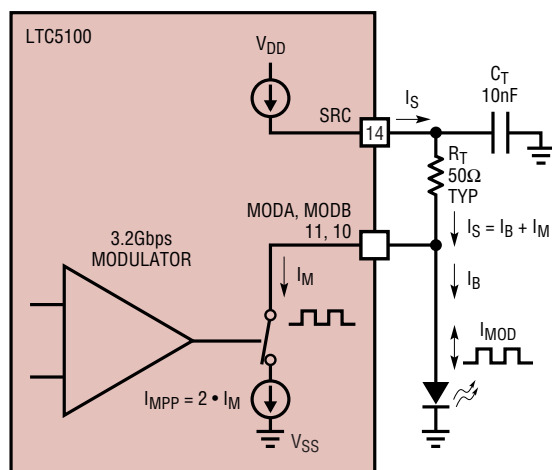


Figure 12. Simplified Laser Bias and Modulation Circuit

#### Terminology and Basic Calculations

Figure 12 through Figure 16 define terminology that is used throughout this data sheet. The current delivered by the SRC pin is called  $I_S$ . The *average* modulation current delivered by the chip at the MODA, MODB pins is called  $I_M$ . The laser bias current,  $I_B$ , is defined as the average current in the laser.  $I_B$  is the difference between the source current and average modulation current.

The *peak-to-peak* modulation current delivered by the chip is called  $I_{MPP}$ .  $I_{MPP}$  is twice the value of  $I_M$  because the high speed data is assumed to have a 50% duty cycle. The peak-to-peak modulation current is divided between the termination resistor and the laser. The peak-to-peak modulation amplitude *in the laser* is called  $I_{MOD}$ . The relationship between  $I_{MPP}$  and  $I_{MOD}$  depends on the relative values of the termination resistor and the laser dynamic resistance.

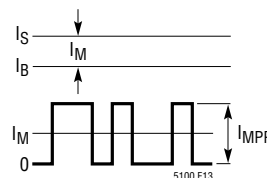


Figure 13. Components of the LTC5100 Source and Modulation Currents (The Laser Bias Current is Also Shown)

The relationships between the source, bias, and modulation currents are as follows.

$$I_B = I_S - I_M \quad (1)$$

$$I_{MPP} = 2 \cdot I_M \quad (2)$$

$$I_{MOD} = \frac{R_T}{(R_T + R_{LD})} \cdot I_{MPP} \quad (3)$$

where

$R_T$  is the termination resistor value.

$R_{LD}$  is the dynamic resistance of the laser, defined in Figure 15.

The expression for  $I_B$  in Equation 1 shows that the maximum achievable laser bias current is a function of the maximum source current,  $I_S$ , and the average modulation

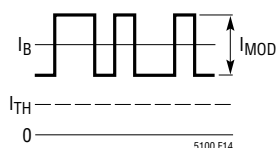
## OPERATION

current,  $I_M$ . The maximum value of  $I_S$  is given in the Electrical Characteristics and the value of  $I_M$  depends on the laser characteristics and the termination resistor value.

The logic “1” and “0” current levels in the laser are given by:

$$I_1 = I_B + \frac{I_{MOD}}{2} \quad (4)$$

$$I_0 = I_B - \frac{I_{MOD}}{2} \quad (5)$$



**Figure 14. Components of the Laser Bias and Modulation Currents**

The power levels corresponding to  $I_1$  and  $I_0$  are  $P_1$  and  $P_0$ , as shown in Figure 16.

$$P_1 = \eta(I_1 - I_{TH}) \quad (6)$$

$$P_0 = \eta(I_0 - I_{TH}) \quad (7)$$

where  $\eta$  is the slope efficiency and  $I_{th}$  is the laser threshold current, defined in Figure 16.

The average optical power and extinction ratio are given by:

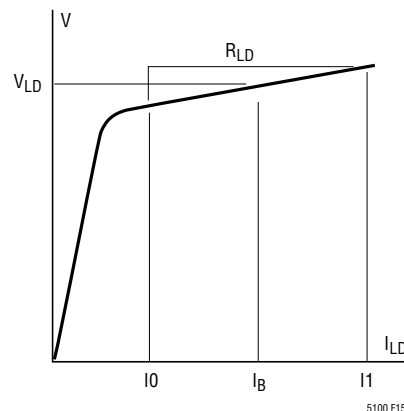
$$P_{AVG} = \frac{P_1 + P_0}{2} \quad (8)$$

$$ER = \frac{P_1}{P_0} \quad (9)$$

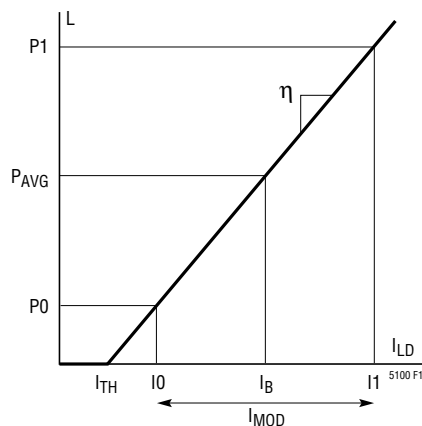
The average voltage on the laser diode relative to ground is  $V_{LD}$  (see Figure 12 and Figure 15). The voltage on the SRC pin is:

$$\begin{aligned} V_S &= V_{LD} + I_S \cdot R_T \\ &= V_{LD} + (I_B + I_M) \cdot R_T \end{aligned} \quad (10)$$

The value  $V_S$  is important because  $V_S$  must not exceed the limits given in the Electrical Characteristics.



**Figure 15. Approximate VI Curve for a Laser Diode**



**Figure 16. Approximate LI Curve for a Laser Diode**

The voltage across the termination resistor is:

$$\begin{aligned} V_{TERM} &= V_{SRC} - V_{MODA} \\ &= I_S \cdot R_T \end{aligned} \quad (11)$$

The LTC5100 can digitize the voltage across the termination resistor using the on-chip ADC, which can give a more accurate measurement of  $I_S$  than that given by digitizing the current internally. See the Electrical Characteristics for details.

### Temperature Compensation

The LTC5100 digitally compensates the temperature drift of the laser bias current, laser modulation current and

## OPERATION

monitor photodiode current. In each case the fundamental calculation is the same. The LTC5100's digital controller multiplies the nominal value of the quantity ( $I_B$ ,  $I_M$  or  $I_{MD}$ ) by a quadratic function of temperature. Temperature measurements are supplied either by an on-chip temperature sensor or by an external microprocessor, according to the setting of `Ext_temp_en`. The general temperature compensation formula is:

$$I = I_{nom} \cdot (TC2 \cdot 2^{-18} \cdot \Delta T^2 + TC1 \cdot 2^{-13} \cdot \Delta T + 1) \quad (12)$$

where  $I$  is the digital representation of the laser bias current, modulation current or monitor diode current ( $I_B$ ,  $I_M$  or  $I_{MD}$ ).

When using the internal temperature sensor (`Ext_temp_en` = 0), the temperature measurements are taken by the on-chip ADC, and  $\Delta T$  is the change in the LTC5100 die temperature relative to a user defined nominal temperature:

$$\Delta T = T_{int\_adc} - T_{nom} \quad (13)$$

When using an external temperature source (`Ext_temp_en` = 1), the temperature measurements are provided in digital form by a microprocessor or host computer and  $\Delta T$  is the change in temperature relative to a user defined nominal temperature:

$$\Delta T = T_{ext} - T_{nom} \quad (14)$$

$T_{int\_adc}$ ,  $T_{ext}$ , and  $T_{nom}$  are 10-bit, unsigned numbers scaled at 0.5K/LSB. The maximum temperature that can be represented is therefore  $2^{10} \cdot 0.5^\circ\text{K} = 512^\circ\text{K}$  or  $239^\circ\text{C}$ .

$TC1$  and  $TC2$  are the first and second order temperature coefficients. They correspond to the registers `Im_tc1` and `Im_tc2` for modulation current, `Ib_tc1` and `Ib_tc2` for bias current and `Imd_tc1` and `Imd_tc2` for monitor diode current. In each case  $TC1$  and  $TC2$  are 8-bit signed numbers in two's complement format. The range of the temperature coefficients is therefore  $-128$  to  $+127$ . When  $TC1$  is multiplied by its weighting coefficient of  $2^{-13}$  in Equation 12, the effective value of the first order temperature coefficient is 122ppm/ $^\circ\text{C}$  per LSB. The full-scale range is approximately  $\pm 15500$  ppm/ $^\circ\text{C}$ . When  $TC2$  is multiplied by its weighting coefficient of  $2^{-18}$  in Equation 12, the effective value of the second order temperature coefficient is 3.81 ppm/ $^\circ\text{C}^2$  per LSB. The full-scale range is approximately  $\pm 484$  ppm/ $^\circ\text{C}^2$ .

Note that Equation 12 is applied to the digital representation of the currents, not the physical current themselves. This is a particularly important point where monitor diode current is concerned, because the digital representation of the monitor diode current is the logarithm of the current. Thus the temperature compensation is of the logarithm of the monitor diode current and not the current itself.

### Notation Used for Registers and Bit Fields

The LTC5100 has a large set of registers, many of which are subdivided into fields of bits. Register names are given in all capitals (`SYS_CONFIG`) and bit fields are given in mixed case (`Apc_en`). For example, the bit that enables Automatic Power Control mode is contained in the System Configuration register. This bit is denoted by:

`SYS_CONFIG.Apc_en`

In many cases this bit field will simply be referred to as "Apc\_en."

The functional diagrams of Figure 3 and Figure 4 show registers and bit fields within registers between horizontal bars. For example, the "Data" field in the ADC register is shown as:

USER\_ADC.Data

A write operation to this register is shown as:

→ USER\_ADC.Data

A register read operation is shown as:

Peaking →

### Range Selection for the Source and Modulation Currents

The source and modulation currents each have four ranges of operation to optimize ADC and DAC resolution as well as high frequency performance. The source current range is controlled by two bits called `Is_rng`. Similarly, the modulation current range is controlled by two bits called `Im_rng`. The maximum current that can be delivered is proportional to the range, so the current output is 1, 2, 3 or 4 times the typical base value of 9mA for the source current and 4.5mA for the average modulation current or 9mA peak-to-peak.

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Figure 17 depicts the current ranges for the source current. The guaranteed full scale is 6mA per range. The minimum operating level should be limited to 1/16 of full scale to avoid the coarse relative quantization seen in any ADC or DAC when operated at low levels. The source range,  $I_{S\_rng}$ , should be selected as low as possible such that the source current,  $I_S$ , stays within the guaranteed current limits over temperature, considering the laser temperature characteristics. From Equation 1 we can see that the source current is the sum of the laser bias and the average modulation currents:

$$I_S = I_B + I_M \quad (15)$$

$I_{S\_rng}$  should be chosen to support the total current required for laser bias and modulation, taking temperature changes in  $I_B$  and  $I_M$  into account.

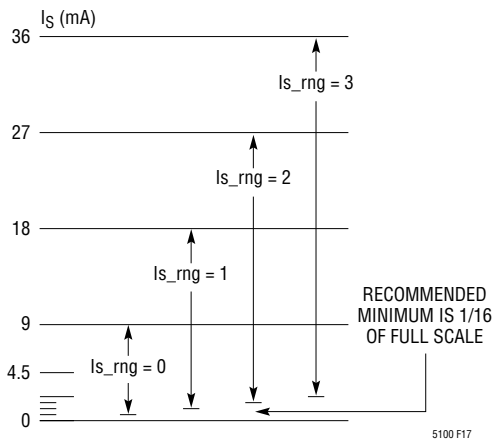


Figure 17. Ranges for the Source Current

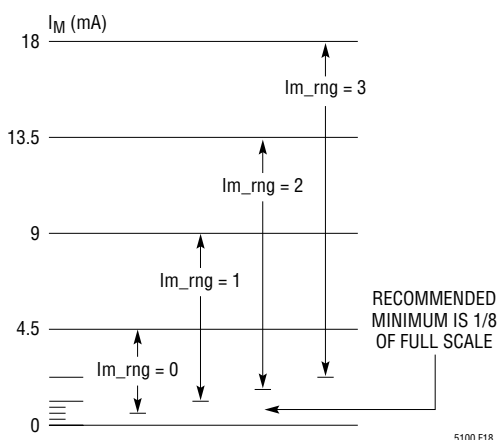


Figure 18. Ranges for the Modulation Current

Figure 18 depicts the current ranges for the average modulation current. This is the average modulation current at the MODA and MODB pins of the chip (recall that the MODA and MODB pins are connected on-chip). The peak-to-peak modulation at the pins of the chip is twice the average. Guaranteed full scale is 3mA average or 6mA pp per range. The minimum operating level should be limited to 1/8 of full scale to preserve the quality of the eye diagram. Operating below 1/8 full scale causes increased overshoot and undershoot. The modulation range,  $I_{M\_rng}$ , should be selected as low as possible such that the modulation current,  $I_M$ , stays within the guaranteed current limits over temperature. The modulation current varies over temperature to compensate the loss in slope efficiency typical of most VCSELs. Therefore, the choice of  $I_{M\_rng}$  should take temperature changes into account.

### High Speed Aspects of the Modulation Output

The LTC5100 modulation output presents a resistive drive impedance with very low reflection coefficient. This output design suppresses ringing and reflections to maintain the quality of the eye diagrams in spite of laser impedance variations. The reflection coefficient is sufficiently low that the LTC5100 can drive the laser over an arbitrary length of transmission line, as shown in Figure 19. A well designed transceiver module goes virtually unnoticed in this system. The only practical limitation on interconnect length to the laser is high frequency line loss.

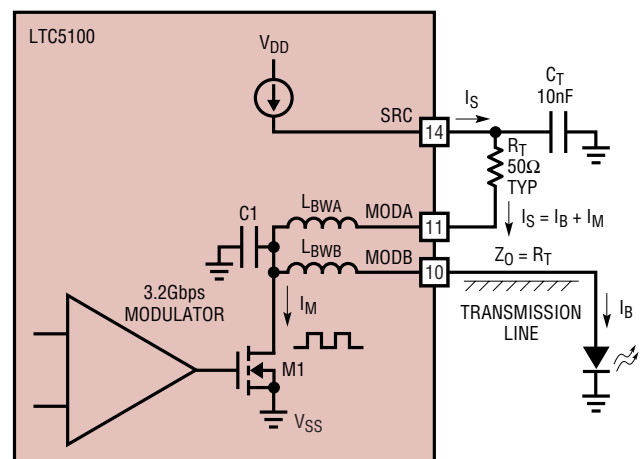


Figure 19. High Speed Details of the Modulation Output

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Figure 19 shows how the LTC5100 achieves a low reflection coefficient. The unavoidable capacitance of the high speed driver transistor, bond pads and ESD protection circuitry (C1) is compensated by the inductance of the bond wires ( $L_{BWA}$  and  $L_{BWB}$ ).

The high speed behavior of the circuit in Figure 19 can be understood in greater detail by examining the simplified circuit in Figure 20. In Figure 20 the switched current source (M1 in Figure 19) launches a current step (1) toward the termination resistor (2A) and toward the transmission line (2B) connected to the laser. The laser is typically mismatched to the line impedance and reflects a portion of the incident wave (3) back toward the MODB pin. There it encounters an L-C-L structure composed of the bond wires and driver capacitance. This structure is carefully designed as a lumped element approximation to the transmission line impedance. It therefore transmits wave (3) through the IC package without reflecting energy back toward the laser. The traveling wave passes through the chip largely unimpeded (4) and is absorbed by the matched termination resistor,  $R_T$ .

The matched termination is provided by the termination resistor,  $R_T$ , decoupled by capacitor  $C_T$ .  $C_T$  forms an AC short across the entire frequency range contained in the modulation data.

The termination resistor,  $R_T$ , need not be  $50\Omega$ .  $50\Omega$  is best for electrical testing because it matches the impedance of most high frequency instruments.  $R_T$  can be made smaller,  $35\Omega$ , for example, to more closely match a laser with low dynamic impedance or to allow more voltage headroom at the SRC pin. This may be necessary for lasers that run at high voltages or high bias currents.  $R_T$  can be made larger,  $70\Omega$  for example, to more closely match a laser with high

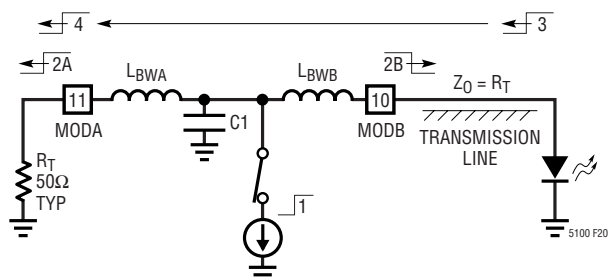


Figure 20. Wave Propagation in the Laser Interconnect

dynamic impedance or if a narrow, high impedance PC board trace is needed to connect to the laser.

Figure 21 shows that the high speed modulation current is confined to the ground system, laser and back termination network. No high speed current circulates in the power supply where it could cause radiation and interference problems.

## HIGH SPEED DATA INPUTS

The high speed data inputs,  $IN^+$  and  $IN^-$ , are internally terminated in  $50\Omega$  and internally AC coupled, eliminating the need for external termination resistors and AC coupling capacitors. Figure 10 shows the equivalent circuit for the high speed data pins. By default, the high speed data inputs are terminated differentially with  $100\Omega$  for compatibility with LVDS, PECL and similar differential signaling standards ( $Cml\_en = 0$ ). Alternately, the inputs can be programmed for  $50\Omega$  single-ended termination to the power supply for biasing a current mode logic (CML) driver. To select CML compatibility, program  $Cml\_en$  to 1. Although internally AC coupled, the inputs are biased with high valued resistors ( $50k$  equivalent) to  $V_{DD(HS)}/2$ , so the LTC5100 remains compatible with external AC coupling capacitors. When externally AC coupled, the inputs self-bias to approximately  $V_{DD(HS)}/2$ .

Internal AC coupling gives the LTC5100 rail-to-rail input common mode capability. The inputs can be driven as much as  $300mV$  beyond the rail during peak excursions. The AC coupling circuit is a distributed highpass filter with

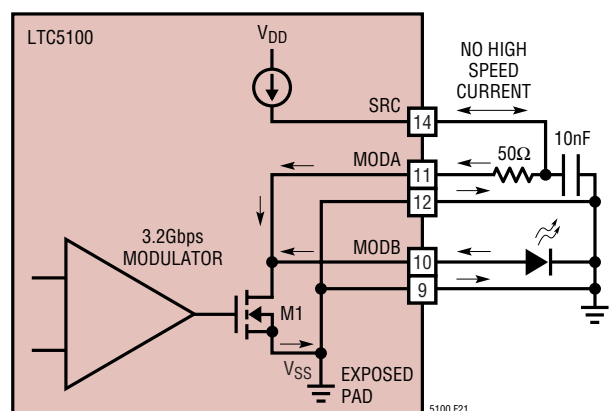


Figure 21. High Speed Current Flow in the Modulation Output

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approximately second order characteristics. The design maximizes the flatness of the step response over extended periods, giving optimal performance during long strings of ones or zeros in the data.

### MODULATION CURRENT CONTROL IN APC AND CCC MODES

The LTC5100 controls the modulation current with a digital servo control loop using feedback from the on-chip ADC. Figure 3 and Figure 4 are Functional Diagrams of the LTC5100 operating in Automatic Power Control (APC) mode and Constant Current Control (CCC) modes, respectively. These diagrams show the organization and operation of the servo control loops for laser bias and laser modulation. Either diagram can be used to understand the modulation current control loop.

#### Servo Control

The average modulation current is controlled by a digital servo loop (shown in the lower half of Figure 3). The nominal modulation current,  $I_{m\_nom}$ , is multiplied by a temperature compensation factor, producing a 10-bit digital set point value,  $I_{m\_set}$ .  $I_{m\_set}$  is the target value for average modulation current. The ADC digitizes the average modulation current, producing a 10-bit value  $I_{m\_adc}$ . The difference between the target value and the actual value produces the servo loop error signal,  $I_{m\_error}$ .  $I_{m\_error}$  is multiplied by a constant,  $I_{m\_gain}$ , to set the loop gain. The result is integrated in a digital accumulator and applied to a 10-bit DAC, increasing or decreasing the modulation amplitude as required to drive the loop error to zero. The servo loop adjusts the modulation amplitude every four milliseconds, producing 250 servo iterations per second.

The modulation servo loop operates on the average modulation current, which is one-half of the peak-to-peak value for a 50% duty cycle signal. The analog electronics in the high speed modulator ensure that controlling the average modulation current is equivalent to controlling the peak-to-peak current.

The ADC input for average modulation current is scaled such that code 512 is the nominal full-scale value, corresponding to 4.5mA per range. Thus, if  $I_{m\_rng} = 0$  and  $I_m = 4.5mA$ , the ADC digitizes code 512. The control system for the modulation current effectively has 9-bit resolution, because at most one-half of the 10-bit ADC range is utilized. This provision maximizes the compliance voltage range of the modulation output.

The difference equation for the modulation servo loop is:

$$\begin{aligned} I_{m\_adc_n} &= I_{m\_adc_{n-1}} + \frac{I_{m\_gain}}{8} \cdot I_{m\_error} \\ &= I_{m\_adc_{n-1}} + \frac{I_{m\_gain}}{8} \cdot (I_{m\_set} - I_{m\_adc_{n-1}}) \end{aligned} \quad (16)$$

$I_{m\_gain}$  is a 3-bit digital value, so the scaling factor,  $I_{m\_gain}/8$ , takes on the discrete values 0, 1/8, 2/8, ..., 7/8. If  $I_{m\_gain} = 4$ , then  $I_{m\_gain}/8 = 0.5$  and the error in the control loop is cut in half with each servo iteration. In this case the step response of the loop is given by:

$$I_{m\_adc_n} = I_{m\_set} \cdot \left[ 1 - \left( 1 - \frac{I_{m\_gain}}{8} \right)^n \right] \quad (17)$$

The step response has the familiar exponential settling characteristic of a first order system. The step response is shown in Figure 22 for  $I_{m\_gain} = 4$ . The remaining error is reduced by one-half with each servo iteration. In seven iterations, or about 28ms, the modulation current settles to under 1% in this example. The measured step response, including the modulation envelope, is shown in the Typical Performance Characteristics.

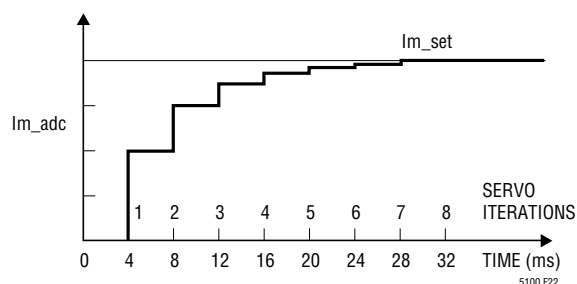


Figure 22. Step Response of the Average Modulation Current for  $I_{m\_gain} = 4$



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Reducing  $Im\_gain$  slows the settling time and increasing  $Im\_gain$  speeds the settling time. For example, with  $Im\_gain = 1$ , the residual loop error is cut by 1/8 with each servo iteration. In this case it would take 35 servo iterations (about 140ms) to settle to 1%. With  $Im\_gain = 7$ , the residual servo loop error is cut by 7/8 with each servo iteration. In this case it would take only three servo iterations (about 12ms) to settle to 1%, but the servo loop will tend to “hunt” or oscillate at a low level with such a high loop gain.

### Temperature Compensation

The set point value for the modulation current,  $Im\_set$  in Figure 3 and Figure 4, changes with temperature to compensate the temperature dependence of the laser diode's slope efficiency. Temperature measurements are supplied either by an on-chip temperature sensor or by an external microprocessor, according to the setting of  $Ext\_temp\_en$ . The temperature compensated expression for  $Im\_set$  is given by:

$$Im\_set = Im\_nom \cdot \left( Im\_tc2 \cdot 2^{-18} \cdot \Delta T^2 + Im\_tc1 \cdot 2^{-13} \cdot \Delta T + 1 \right) \quad (18)$$

$Im\_tc1$  and  $Im\_tc2$  are the first and second order temperature coefficients for the modulation current.

### LASER BIAS CURRENT CONTROL IN APC MODE

Figure 3 is a functional diagram of the LTC5100 operating in automatic power control (APC) mode. In APC mode, the LTC5100 servo controls the average optical power with

feedback from a monitor photodiode. Setting  $Apc\_en = 1$  selects this mode. In APC mode the monitor diode current can be temperature compensated with first and second order temperature coefficients.

Figure 9 shows an equivalent circuit for the MD pin and Figure 23 shows details of the monitor diode circuit. The  $Md\_polarity$  bit selects whether the monitor diode sources or sinks current from the MD pin. A programmable attenuator and logarithmic amplifier permit a very wide range of monitor diode currents spanning 4.25μA to 2176μA (typical) with constant 0.2% set point resolution. The attenuator divides the monitor diode current by 1, 4, 16 or 64 depending on the value of  $Imd\_rng$ . Two bits called  $Imd\_rng$  control the attenuator setting, selecting a full scale current range of 34, 136, 544 or 2176μA typical. A 5kHz lowpass filter provides antialiasing and limits noise. The logarithmic amplifier compresses the dynamic range of the monitor diode current and plays a role in maintaining constant and predictable settling times regardless of the photodiode characteristics.

### Range Selection

Figure 24 depicts the current ranges for the monitor diode current. The full-scale range of the monitor diode current is  $34\mu A \cdot 4^{Imd\_rng}$  typical where  $Imd\_rng = 0, 1, 2$  or 3. The minimum operating level should be limited to 20% of full scale to ensure adequate settling time of the optical power output of the laser. The range should be selected so that the monitor diode current stays within the guaranteed current limits over temperature.

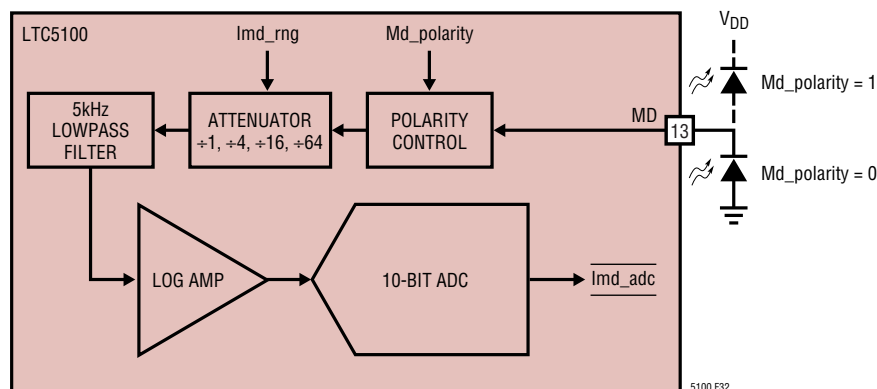


Figure 23. Detail of the Monitor Photodiode Circuit

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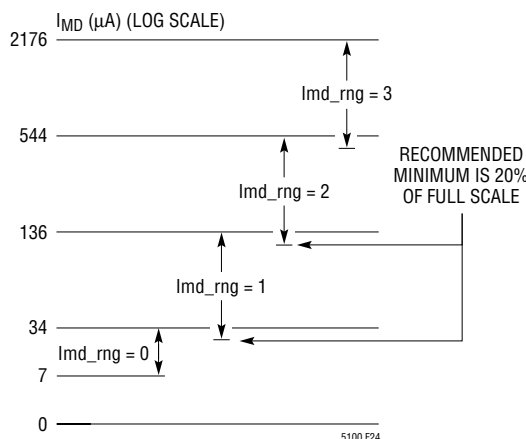


Figure 24. Operating Ranges for the Monitor Diode Current

The SRC pin current range,  $I_{s\_rng}$ , should be chosen so that the SRC pin can supply the required bias current over temperature. See the section titled Range Selection for the Source and Modulation Currents.

### Servo Control

The average optical power is controlled by a digital servo loop shown in the upper half of Figure 3. The loop sets and controls the *logarithm* of the monitor diode current. The logarithm of the nominal monitor diode current,  $I_{md\_nom}$ , is multiplied by a temperature compensation factor, producing a 10-bit digital set point value,  $I_{md\_set}$ .  $I_{md\_set}$  is therefore the temperature compensated *logarithm* of the target value for monitor diode current. The ADC digitizes the logarithm of the monitor diode current, producing a 10-bit value called  $I_{md\_adc}$ . The difference between the target value and the actual value produces the servo loop error signal,  $I_{md\_error}$ .  $I_{md\_error}$  is multiplied by a constant,  $A_{pc\_gain}$ , to set the loop gain.  $I_{md\_error}$  is also multiplied by the set point value of the modulation current to further stabilize the servo dynamics, as explained below. The result is integrated in a digital accumulator and applied to a 10-bit DAC, increasing or decreasing the SRC pin current (and consequently the laser bias current) as required to drive the loop error to zero. The servo loop adjusts the laser bias current every four milliseconds, producing 250 servo iterations per second.

The open-loop gain of the APC loop is proportional to the laser slope efficiency,  $\eta$  (Watts/Amp), and monitor diode

response,  $\gamma$  (Amps/Watt). These parameters vary widely from laser to laser. If nothing is done to compensate the variations in  $\eta$  and  $\gamma$ , the settling time of the optical power output will vary over an unacceptably wide range. For example, a 4:1 variation in slope efficiency and a 5:1 variation in monitor diode response could create a 20:1 variation in settling time.

The LTC5100 uses two techniques to fully compensate for variations in the laser and monitor diode characteristics, achieving constant settling times under all conditions. First, taking the logarithm of the monitor diode current precisely compensates variations in the monitor diode response. Second, multiplying the error signal by the modulation current precisely compensates for variations in laser slope efficiency.

The difference equation for the APC loop is:

$$\begin{aligned} I_{m\_adc_n} &= I_{m\_adc_{n-1}} + A \cdot I_{md\_error} \\ &= I_{m\_adc_{n-1}} + A \cdot (I_{md\_set} - I_{md\_adc_{n-1}}) \end{aligned} \quad (19)$$

where  $A$  is the small-signal loop gain, given by:

$$\begin{aligned} A &= \frac{A_{pc\_gain}}{32} \cdot \frac{1 + I_{s\_rng}}{1 + I_{m\_rng}} \cdot \frac{1}{\ln(8)} \\ &\quad \cdot \frac{ER - 1}{ER + 1} \cdot \frac{R_T + R_{LD}}{R_T} \end{aligned} \quad (20)$$

where:

$\ln(8) = 2.079$  is the natural logarithm of 8

$ER$  is the extinction ratio

$R_T$  is the termination resistance

$R_{LD}$  is the dynamic resistance of the laser diode

$A_{pc\_gain}$  is a 5-bit digital value, so the scaling factor,  $A_{pc\_gain}/32$ , takes on the discrete values 0, 1/32, 2/32, ..., 31/32.

In practice, the extinction ratio is usually high ( $ER \gg 1$ ), and  $R_T \sim R_{LD}$ , so Equation 20 simplifies to:

$$A \approx \frac{A_{pc\_gain}}{32} \cdot \frac{1 + I_{s\_rng}}{1 + I_{m\_rng}} \quad (21)$$

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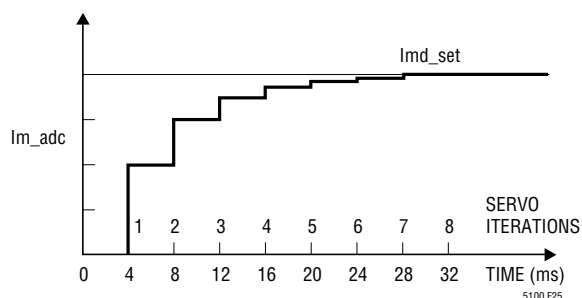
Equation 20 shows that the loop gain is completely independent of the slope efficiency and monitor diode response. Consequently the servo dynamics and settling time are independent of these highly varying quantities. The  $Apc\_gain$  quantity can be set to compensate for the selected values of  $Is\_rng$  and  $Im\_rng$  as well as the extinction ratio, termination resistance and laser dynamic resistance.

The step response of the APC loop is:

$$Im\_adc_n = Im\_set \cdot [1 - (1 - A)^n] \quad (22)$$

The step response given in Equation 22 has the familiar exponential settling characteristic of a first order system. The step response is shown in Figure 25 for  $A = 0.5$ . The remaining error is reduced by one-half with each servo iteration. In seven iterations, or about 28ms, the modulation current settles to under 1% in this example. The measured step response, including the modulation envelope, is shown in the Typical Performance Characteristics.

Choosing  $A = 0.5$  is nearly optimal because it results in smooth, exponential settling.  $A = 1$  will settle in about two servo iterations or 8ms, but “hunting” or low level oscillation will be seen in the laser bias current.  $A > 1$  results in overshoot and  $A > 2$  results in sustained high level oscillation.



**Figure 25. Step Response of the Monitor Diode Current for a Total Loop Gain of 0.5**

### Temperature Compensation

The set point value for the monitor diode current,  $Im\_set$  in Figure 3, can be changed with temperature to compensate the temperature dependence of the monitor diode response. Temperature measurements are supplied either by an on-chip temperature sensor or by an external

microprocessor, according to the setting of  $Ext\_temp\_en$ . The temperature compensated expression for  $Im\_set$  is given by:

$$Im\_set = Im\_nom \cdot \left( Im\_tc2 \cdot 2^{-18} \cdot \Delta T^2 + Im\_tc1 \cdot 2^{-13} \cdot \Delta T + 1 \right) \quad (23)$$

$Im\_tc1$  and  $Im\_tc2$  are the first and second order temperature coefficients for the monitor diode current. Equation 23 applies to the digital representation of the monitor diode current. Recall that  $Im\_set$  is the digital set point for the *logarithm* of the monitor diode current. This fact has two important implications. First, the first order temperature coefficient in Equation 23 ( $Im\_tc1$ ) results in an exponential change in the physical monitor diode current with temperature. However, the monitor diode temperature drift is usually very small, and the exponential is well approximated as linear. Second, if  $Im\_tc2 = 0$ , the relative temperature sensitivity of the physical current is given by:

$$\frac{dI_{MD}}{dT} \cdot \frac{1}{I_{MD}} = \ln(8) \cdot 2^{-13} \cdot Im\_tc1 \cdot \frac{Im\_nom}{1024} \quad (24)$$

where  $I_{MD}$  is the physical monitor diode current in Amps.

Equation 24 shows that the temperature coefficient of the physical current depends on the nominal monitor diode current. For example, if  $Im\_nom = 512$  and  $Im\_tc1 = 4$ , the physical temperature compensation would be:

$$\frac{dI_{MD}}{dT} \cdot \frac{1}{I_{MD}} = \ln(8) \cdot 2^{-13} \cdot 4 \cdot \frac{512}{1024} = 508 \text{ ppm/}^\circ\text{C} \quad (25)$$

The effect of  $Im\_tc2$  on the physical monitor diode current has no simple physical interpretation. In most cases it will be sufficient to set  $Im\_tc2$  to zero and use the first order temperature coefficient,  $Im\_tc1$  to correct monitor diode drift.

### LASER BIAS CURRENT CONTROL IN CCC MODE

Figure 4 is a functional diagram of the LTC5100 operating in constant current control (CCC) mode. In CCC mode, the LTC5100 sets the laser bias current directly. Setting  $Apc\_en = 0$  selects this mode. In CCC mode the laser bias

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current can be temperature compensated with first and second order temperature coefficients.

### Servo Control

The laser bias current is controlled by a digital servo loop (shown in the upper half of Figure 4) and can be understood as follows. The nominal bias current,  $I_{b\_nom}$ , is multiplied by a temperature compensation factor, producing a 10-bit digital set point value,  $I_{b\_set}$ .  $I_{b\_set}$  is the target value for the laser bias current. The ADC digitizes the SRC pin current and the average modulation current, producing 10-bit values  $I_{s\_adc}$  and  $I_{m\_adc}$ . The laser bias current is the difference between the SRC pin current and the average modulation current (Equation 1). The system generates a digital representation of the laser bias current by calculating:

$$I_{b\_adc} = I_{s\_rng} \cdot I_{s\_adc} - I_{m\_rng} \cdot I_{m\_adc} \quad (26)$$

where  $I_{b\_adc}$  is the result of a calculation. (The ADC never digitizes the laser bias current directly.)

The difference between the target value and the actual value is the servo loop error signal,  $I_{b\_error}$ .  $I_{b\_error}$  is multiplied by a constant,  $I_{b\_gain}$ , to set the loop gain. The result is integrated in a digital accumulator and applied to a 10-bit DAC, increasing or decreasing the SRC pin current as required to drive the loop error to zero. The servo loop adjusts the SRC pin current every four milliseconds, producing 250 servo iterations per second.

The simplified difference equation for the bias current servo loop is, assuming  $I_{m\_nom} = 0$ :

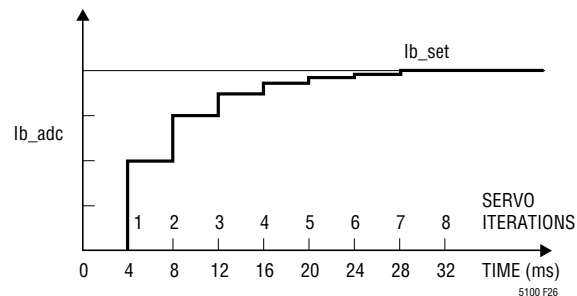
$$\begin{aligned} I_{b\_adc_n} &= \\ I_{b\_adc_{n-1}} &+ \frac{I_{b\_gain}}{32} \cdot (I_{s\_rng} + 1) \cdot I_{b\_error} \\ &= I_{b\_adc_{n-1}} + \frac{I_{b\_gain}}{32} \cdot (I_{s\_rng} + 1) \\ &\quad \cdot (I_{b\_set} - I_{b\_adc_{n-1}}) \end{aligned} \quad (27)$$

$I_{b\_gain}$  is a 5-bit digital value, so the scaling factor,  $I_{b\_gain}/32$ , takes on the discrete values 0, 1/32, 2/32, ..., 31/32. If  $I_{b\_gain} \cdot (I_{s\_rng} + 1) = 16$ , then  $I_{b\_gain} \cdot (I_{s\_rng} + 1)/32 = 0.5$  and the error in the control loop is cut in half

with each servo iteration. In this case the step response of the loop is given by, assuming  $I_{m\_nom} = 0$ :

$$I_{b\_adc_n} = I_{b\_set} \cdot \left[ 1 - \left( 1 - \frac{I_{b\_gain} \cdot (I_{s\_rng} + 1)}{32} \right)^n \right] \quad (28)$$

The step response has the familiar exponential settling characteristic of a first order system. The step response is shown in Figure 26 for  $I_{b\_gain} \cdot (I_{s\_rng} + 1) = 16$ . The remaining error is reduced by one-half with each servo iteration. In seven iterations, or about 28ms, the laser bias current settles to under 1% in this example. The measured step response is shown in the Typical Performance Characteristics.



**Figure 26. Step Response of the Laser Bias Current for  $(I_{b\_gain}) \cdot (I_{s\_rng} + 1) = 16$**

Reducing  $I_{b\_gain}$  slows the settling time and increasing  $I_{b\_gain}$  speeds the settling time. For example, with  $I_{b\_gain} \cdot (I_{s\_rng} + 1) = 1$ , the residual loop error is cut by 1/32 with each servo iteration. In this case it would take 145 servo iterations (about 580ms) to settle to 1%. With  $I_{b\_gain} \cdot (I_{s\_rng} + 1) = 31$ , the residual servo loop error is cut by 31/32 with each servo iteration. In this case it would take only two servo iterations (about 8ms) to settle to 1%.

Setting  $I_{m\_nom} \neq 0$  slows the settling time of the laser bias current somewhat. This effect can easily be compensated by increasing  $I_{b\_gain}$ .

### Temperature Compensation

The set point value for the laser bias current,  $I_{b\_set}$  in Figure 4, can change with temperature to compensate the temperature dependence of the laser diode's threshold current. Temperature measurements are supplied either

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by an on-chip temperature sensor or by an external microprocessor, according to the setting of Ext\_temp\_en. The temperature compensated expression for Ib\_set is given by:

$$Ib\_set = Ib\_nom \cdot \left( Ib\_tc2 \cdot 2^{-18} \cdot \Delta T^2 + Ib\_tc1 \cdot 2^{-13} \cdot \Delta T + 1 \right) \quad (29)$$

Ib\_tc1 and Ib\_tc2 are the first and second order temperature coefficients for the laser bias current.

## TRANSMIT ENABLE, FAULT DETECTION AND EYE SAFETY

The LTC5100 is compatible with the Gigabit Interface Converter (GBIC) specification, but includes additional features and safety interlocks. Figure 27 shows the state diagram for enabling the transmitter and detecting faults.

The EN pin and Soft\_en control bit enable and disable the transmitter. The EN pin may be programmed for active high or active low operation with the En\_polarity bit.

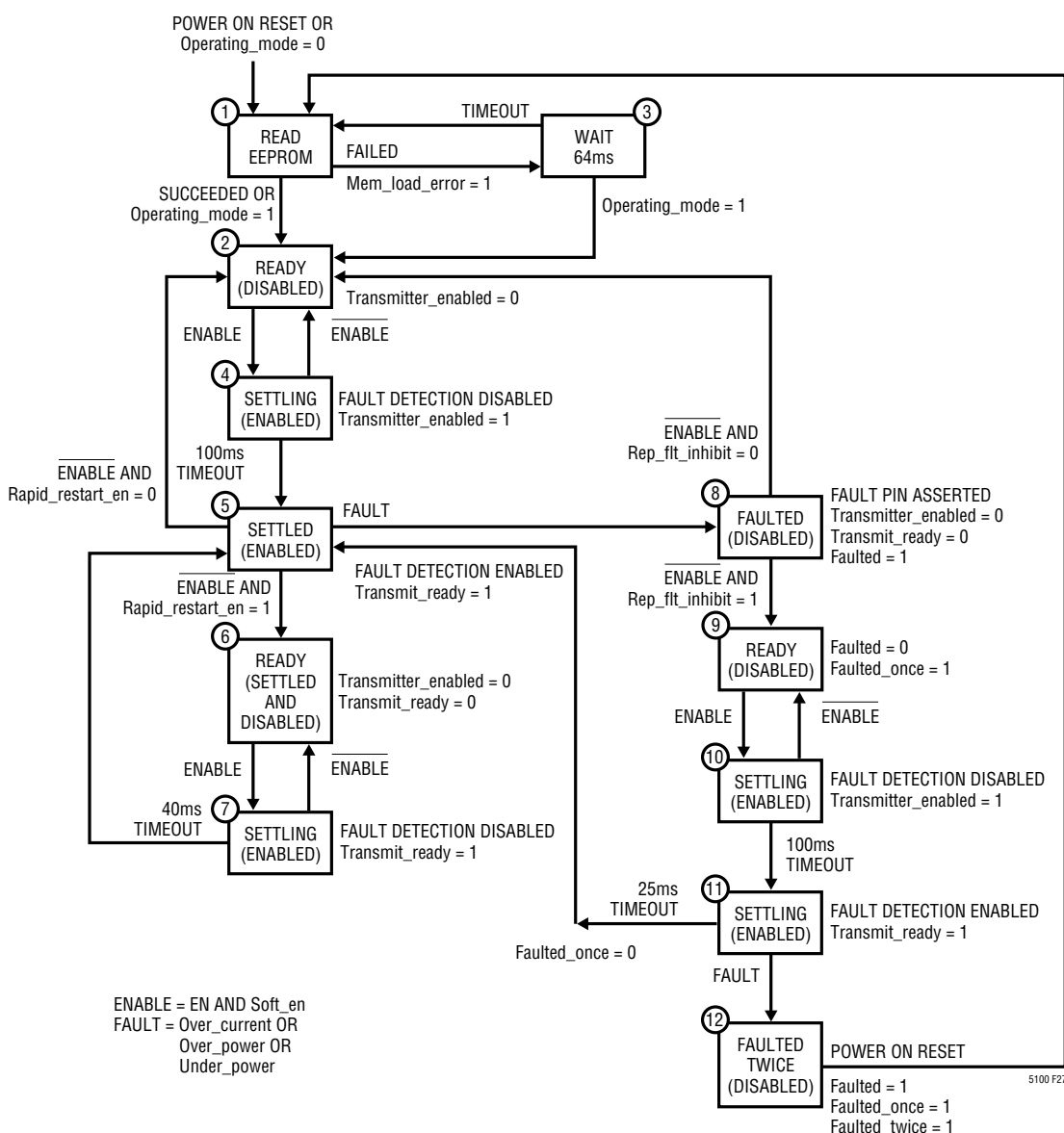


Figure 27. State Diagram for Transmitter Enable and Fault Detection

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The EN pin and the Soft\_en bit must both be active to enable the transmitter, providing an extra degree of safety and allowing full software control of the transmitter enable function. As shown in Figure 6, the EN pin has a weak 10 $\mu$ A current source that pulls it to the inactive state in case of an accidental open on the pin. The EN and Soft\_en bits are inhibited until the LTC5100 has successfully loaded its registers from an EEPROM or the Operating\_mode bit has been set, signaling that a microprocessor has assumed control of the chip.

The first time the transmitter is enabled after initial power up, the servo loops find the correct DAC settings for bias and modulation current through a feedback process. Initial settling is typically within 300ms. If the transmitter is disabled and subsequently re-enabled, the previously determined DAC settlings are restored. In this case settling occurs typically within 1ms. This feature is called “Rapid Restart” and can be overridden by setting the Rapid\_restart\_en bit to zero.

The LTC5100 has sophisticated eye safety and fault handling features. Five types of faults are detected: low supply voltage, excessive laser bias current, overpower, underpower and EEPROM memory load failure. Table 1 summarizes these five faults and how they are handled in the LTC5100.

Faults are latched in compliance with GBIC requirements. Faults can be independently enabled (except for low supply voltage and memory load failure) and are recorded in an internal register for readout over the serial bus. If two faults occur simultaneously, the fault with the highest priority (see Table 1) is recorded in the FLT\_STATUS register. This register indicates the cause of the fault and is cleared only when read (not when the fault itself is cleared.) Low supply voltage and memory load failure are considered hard faults and cannot be masked or overridden. They prevent the transmitter from begin enabled until they are cleared.

Normally, a fault automatically disables the transmitter and shuts down the laser. In some systems it may be desirable to allow data transmission to continue after a

**Table 1. Fault Detection and Handling**

	FAULT TYPE					
	LASER OVERCURRENT	LASER OVERPOWER	LASER UNDERPOWER	EEPROM MEMORY LOAD FAULT	POWER SUPPLY UNDERVOLTAGE	SOFTWARE FORCED FAULT
Fault Occurs When	Laser Bias Current Exceeds the Value in the IB_LIMIT Register	Monitor Diode Current is 50% Greater Than the Set Point	Monitor Diode Current is 50% Less than the Set Point	EEPROM Load Starts But Fails to Complete	V <sub>DD</sub> Drops Below 2.8V	The Flt_pin_override and Force_flt Bits are Set
Priority	5	4	3	2	1	NA
Cleared by Power-On Reset	Yes	Yes	Yes	Yes	No	Yes
Latched in the FLT_STATUS Register	Yes	Yes	Yes	Yes	Yes	No (Not Part of the FLT_STATUS Register)
Cleared from the FLT_STATUS Register on Read	Yes	Yes	Yes	Yes	Yes	No (Not Part of the FLT_STATUS Register)
Latched at the FAULT Pin	Yes	Yes	Yes	Yes	No (The FAULT Pin Signals a Fault as Long as the Supply Voltage Remains Too Low)	Yes (Actually Latched in the FLT_CONFIG Register)
Enabled by	Over_current_en	Over_pwr_en and Apc_en	Under_pwr_en and Apc_en	Always Enabled	Always Enabled	Flt_pin_override
Glitch Rejection	4 $\mu$ s	4 $\mu$ s	4 $\mu$ s	NA	200mV Typical Hysteresis	NA

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fault has occurred. For example, the software in the host system may need to evaluate the cause of the fault before shutting down the laser. If `Auto_shutdn_en` = 1, the LTC5100 automatically disables the transmitter after a fault. If `Auto_shutdn_en` = 0, data transmission continues after a fault. The transmitter is not disabled until the host system drives the EN pin inactive or clears the `Soft_en` bit. Low power supply voltage and memory load errors are considered hard faults and always disable the transmitter, regardless of the setting of `Auto_shutdn_en`.

The LTC5100 implements the GBIC protocol for preventing software from repeatedly re-enabling a faulted transmitter. When a first fault is detected, it can be cleared by disabling the transmitter. If the transmitter is re-enabled and a second fault occurs within 25ms after fault detection is enabled, the transmitter is permanently disabled. Only cycling power to the LTC5100 can clear this condition. This feature is called “Repeated Fault Inhibit” and can be overridden by setting the `Repeatedflt_inhibit` bit to zero.

The FAULT pin can be configured active high or active low with the `Flt_pin_polarity` bit. The FAULT pin can be programmed for open drain, 330 $\mu$ A internal pull-up, 500 $\mu$ A internal pull-up or complementary (push-pull) drive with the two `Flt_drv_mode` bits. Refer to Figure 8 for an equivalent circuit of the FAULT pin.

The FAULT pin can be overridden in software for testing purposes or to allow a microprocessor in the transceiver module to fully control the module’s fault output. If the `Flt_pin_override` bit is set, then the `Forceflt` bit fully controls the state of the FAULT pin.

The state of the LTC5100 can be monitored by reading the `FLT_STATUS` register. See Table 21 for a description of the status bits.

## EYE SAFETY INFORMATION

Communications lasers can emit levels of optical power that pose an eye safety risk. While the LTC5100 provides certain fault detection features, these features alone do not ensure that a laser transmitter using the LTC5100 is compliant with IEC 825 or the regulations of any particular agency. The user must analyze the safety requirements of their transceiver module or system, activate the

appropriate laser safety features of the LTC5100, and take any *additional* precautions needed to ensure compliance of the end product with the requirements of the relevant regulatory agencies. In particular, the LTC5100 produces laser currents in response to digitally programmed commands. The user must ensure software written to control the LTC5100 does not cause excessive levels of radiation to be emitted by the laser.

## POWER CONSUMPTION AND POWER MANAGEMENT

The power consumption of the LTC5100 is dependent on several variables, including the modulation current range (set by `Im_rng`), the laser bias and modulation levels, and the state of the transmitter (whether enabled or disabled.) If `Power_down_en` = 1, the LTC5100 turns off its high speed amplifiers when the transmitter is disabled, reducing supply current to less than 5mA (typical). See the Typical Performance Characteristics for further information.

## HIGH SPEED PEAKING CONTROL

The LTC5100 has the ability to selectively peak the falling edge of the modulation waveform to accelerate the turn-off of the laser diode. The 5-bit PEAKING register controls this function. See the Typical Performance Characteristics for further information. Lower values in the PEAKING register increase the falling edge peaking.

## ANALOG-TO-DIGITAL CONVERSION

### Overview

The ADC in the LTC5100 is a 10-bit, dual slope integrating converter with excellent linearity and noise rejection. A multiplexer allows digitizing six quantities:

- SRC pin current,  $I_S$
- Average modulation current,  $I_M$
- Laser diode voltage,  $V_{LD}$
- Monitor diode current,  $I_{MD}$
- Termination resistor voltage,  $V_{TERM}$
- Die temperature,  $T$

All of these measurements are available to the user via the I<sup>2</sup>C serial bus.

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### Conversion Sequence

The ADC has a 1ms conversion time and operates in a four-cycle sequence. Three of these cycles are dedicated to the needs of the servo controllers for laser bias and modulation current. One cycle is available to the user to convert any desired quantity. Table 2 shows how the four conversion time slots are allocated. The temperature compensation and servo loop calculations are done during the User cycle. The source and modulation DACs are also updated during this cycle.

**Table 2. ADC Conversion Sequence**

CYCLE	APC MODE	CCC MODE	RESULT STORED IN REGISTER
1	T	T	T_INT_ADC
2	I <sub>M</sub>	I <sub>M</sub>	IM_ADC
3	I <sub>MD</sub>	I <sub>S</sub>	IMD_ADC/IS_ADC
4	User	User	USER_ADC

### User Access to the ADC

The results of each conversion cycle in Table 2 are stored in user accessible registers. The last die temperature measurement can be read over the I<sup>2</sup>C bus at any time by reading the T\_INT\_ADC register. Note that the quantity converted during the third cycle depends on whether the chip is in APC or CCC mode. The result of the third conversion cycle is stored in a register that is called IMD\_ADC in APC mode and IS\_ADC in CCC mode. There is only one register, but it is given two names to indicate the quantity it actually holds.

The fourth cycle, called the user cycle, is available to digitize any of the six multiplexed signals. The result can be read out over the I<sup>2</sup>C serial bus. The signal to be digitized during the user cycle is selected by setting the three-bit field USER\_ADC.Adc\_src\_sel (see Table 23). For example, setting Adc\_src\_sel = 2 programs the multiplexer to select the laser diode voltage, V<sub>LD</sub>. During the next user conversion cycle, V<sub>LD</sub> is converted and stored to the USER\_ADC.Data field. When the conversion is complete, USER\_ADC.Valid is set and USER\_ADC.Adc\_src indicates the signal source whose converted value is stored in USER\_ADC.Data. Reading or

writing the USER\_ADC register clears the Valid bit. The Valid bit remains cleared until the next user conversion is complete. USER\_ADC.Adc\_src always corresponds to the signal source whose data is stored in USER\_ADC.Data, not the source that was most recently selected by writing USER\_ADC.Adc\_src\_sel. The Valid bit and Adc\_src field are useful for monitoring when the ADC has updated the USER\_ADC.Data field. Table 3 gives an extended example of accessing the USER\_ADC register.

Note that the content of the USER\_ADC register is different for writing and for reading, even though the I<sup>2</sup>C command used to access this register is the same in both cases. See Table 23 and Table 24 for a detailed definition of the bit fields in the USER\_ADC register. Table 23 also shows how to convert ADC digital codes to real-world quantities.

### DIRECT MICROPROCESSOR CONTROL OF THE LASER BIAS AND MODULATION CURRENT

Setting Lpc\_en to zero turns off the LTC5100's digital Laser Power Controller (see Figure 2). The source and modulation DACs (Is\_dac and Im\_dac) can then be written from the I<sup>2</sup>C serial bus, allowing an external microprocessor or test computer to directly control the source and modulation currents.

### DIGITAL CONTROL AND THE I<sup>2</sup>C SERIAL INTERFACE

The LTC5100 has extensive digital control and monitoring features. These features can be used during final assembly of a transceiver module to set up the laser and verify performance. In normal operation, the LTC5100 can operate standalone or under microprocessor supervision. Operating standalone, the LTC5100 automatically loads its configuration and laser operating parameters (bias current, modulation current, monitor diode current) from a small external EEPROM at power up. Operating under microprocessor supervision, the microprocessor is in total control of setting up the LTC5100.

### I<sup>2</sup>C Serial Interface Protocol

The digital interface for the LTC5100 is I<sup>2</sup>C, a 2-wire serial bus standard that is fully documented in "I<sup>2</sup>C-Bus and How

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Table 3. Example of User ADC Cycle Access

ADC CYCLE	SIGNAL SOURCE	WRITE TO Adc_src_sel	READ FROM ADC_USER REGISTER	Adc_src	Valid	Data	COMMENT
1	T			V <sub>TERM</sub>	0	V <sub>TERM</sub> (1)	Selected Signal Source is V <sub>TERM</sub>
2	I <sub>M</sub>			V <sub>TERM</sub>	0	V <sub>TERM</sub> (1)	
3	I <sub>S</sub>			V <sub>TERM</sub>	0	V <sub>TERM</sub> (1)	
4	User (V <sub>TERM</sub> )			V <sub>TERM</sub>	0	V <sub>TERM</sub> (1)	
1	T			V <sub>TERM</sub>	1	V <sub>TERM</sub> (2)	ADC Updates Data with New Data, Setting Valid
2	I <sub>M</sub>	V <sub>LD</sub>		V <sub>TERM</sub>	0	V <sub>TERM</sub> (2)	User Selects New Signal Source, V <sub>LD</sub> , Clearing Valid
3	I <sub>S</sub>			V <sub>TERM</sub>	0	V <sub>TERM</sub> (2)	
4	User (V <sub>LD</sub> )			V <sub>TERM</sub>	0	V <sub>TERM</sub> (2)	
1	T			V <sub>LD</sub>	1	V <sub>LD</sub> (1)	ADC Updates Data with New Data, Setting Valid and Changing Adc_src to Reflect the Source of the New Data
2	I <sub>M</sub>			V <sub>LD</sub>	1	V <sub>LD</sub> (1)	
3	I <sub>S</sub>		V <sub>LD</sub>	V <sub>LD</sub>	0	V <sub>LD</sub> (1)	User Reads the ADC_USER Register, Clearing Valid
4	User (V <sub>LD</sub> )			V <sub>LD</sub>	0	V <sub>LD</sub> (1)	
1	T			V <sub>LD</sub>	1	V <sub>LD</sub> (2)	ADC Updates Data with New Data, Setting Valid
2	I <sub>M</sub>			V <sub>LD</sub>	1	V <sub>LD</sub> (2)	
3	I <sub>S</sub>			V <sub>LD</sub>	1	V <sub>LD</sub> (2)	
4	User (V <sub>LD</sub> )			V <sub>LD</sub>	1	V <sub>LD</sub> (2)	

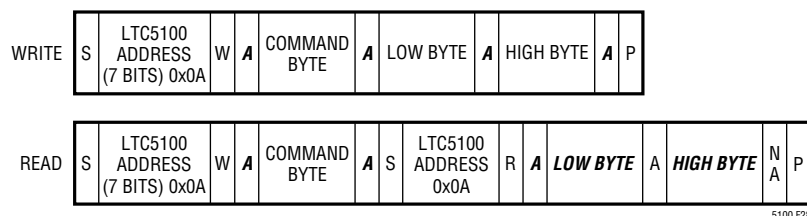


Figure 28. I<sup>2</sup>C Serial Read/Write Sequences (LTC5100 Responses are Shown in Bold Italics)

to Use It, V1.0” by Philips Semiconductor. The 7-bit I<sup>2</sup>C bus address for the LTC5100 is 0x0A (hex). When the Read/Write bit that follows is a “1”, the resulting 8-bit word becomes 0x15. When the Read/Write bit is a “0”, the 8-bit word becomes 0x14. To communicate with the LTC5100, the bus master transmits the LTC5100 address followed by a command byte and data as defined by the I<sup>2</sup>C bus specification and shown in Figure 28 and Table 4. Note that 16 bits of data are always transmitted, low byte first, high byte last. Within each transmitted byte, the bit order is

MSB .. LSB. The register set and I<sup>2</sup>C command set for the LTC5100 are documented in Table 7 through Table 30.

Table 4. Legend for the I<sup>2</sup>C Protocol

SYMBOL	MEANING
S	Start
W	Write
R	Read
A	Acknowledge
NA	No Acknowledge
P	Stop

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### Standalone Operation

On power-up the LTC5100 becomes an I<sup>2</sup>C bus master and attempts to load its configuration data from an external EEPROM. If an EEPROM responds, the LTC5100 reads 16-bytes of data and transfers this data to the internal register set. When a 16-byte transfer is completed without error, the LTC5100 becomes ready to enable the transmitter and begin driving the laser. If a bus error occurs during this transfer, the load sequence is aborted and a Mem\_load\_error is generated, preventing the transmitter from being enabled until a successful memory load attempt is completed or until an external agent sets the Operating\_mode bit. Every 64ms another attempt is made to load the EEPROM until the memory is read or until

Operating\_mode = 1. Table 5 shows the memory map for the EEPROM.

The LTC5100 generates I<sup>2</sup>C address 0xAE (1010\_1110 binary) when accessing the EEPROM, making it compatible with a wide range of EEPROM sizes. Table 6 details how the LTC5100 interacts with EEPROMs from 128 bits to 16k bits and from where it gets its data.

The LTC5100 supports hot plugging in standalone mode. If the Soft\_en bit is set in the EEPROM and the EN pin is active, the LTC5100 loads its configuration data from the EEPROM and immediately enables the transmitter. The transmitter is typically enabled and settled within the 300ms t<sub>init</sub> period required by the GBIC specification.

**Table 5. EEPROM Memory Map**

	BIT							
BYTE	7	6	5	4	3	2	1	0
15	Reserved			Peaking (4:0)				
14	Ib_gain(4:0)/Apc_gain(4:0)					Im_gain(2:0)		
13	Reserved				Imd_rng(1:0)		T_nom(9:8)	
12	T_nom(7:0)							
11	Im_tc2(7:0)							
10	Im_tc1(7:0)							
9	Reserved				Im_rng(1:0)		Im_nom(9:8)	
8	Im_nom(7:0)							
7	Ib_tc2(7:0)/Imd_tc2(7:0)							
6	Ib_tc1(7:0)/Imd_tc2(7:0)							
5	Reserved				Is_rng(1:0)		Ib_nom(9:8)/Imd_nom (9:8)	
4	Ib_nom(7:0)/Imd_nom(7:0)							
3	Reserved				Rep_flt_inhibit	Rapid_restart_en	Flt_drv_mode	
2	Lpc_en	Auto_shutdn_en	Flt_pin_polarity	Flt_pin_override	Force_flt	Over_pwr_en	Under_pwr_en	Over_current_en
1	Reserved	Ib_limit						
0	Cml_en	Md_polarity	Ext_temp_en	Power_down_en	Apc_en	En_polarity	Soft_en	Operating_mode

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**Table 6. Effective Base Addresses for Various Sized EEPROMs**

GENERIC PART NUMBER	24LC00	24LC01B	24LC02B	24LC04B	24LC16B
Bits	128	1k	2k	4k	16k
Bytes	16	128	256	512	2048
Device Address (Binary)	1010xxx.	1010xxx.	1010xxx.	1010.xxa	1010cba.
Word Address Space (Binary)	xxxx_nnnn	xnnn_nnnn	nnnn_nnnn	nnnn_nnnn	nnnn_nnnn
LTC5100 Generates Device Address	1010_111. = 0xAE	1010_111. = 0xAE	1010_111. = 0xAE	1010_111. = 0xAE	1010_111. = 0xAE
LTC5100 Generates Word Address	0110_0000 = 0x60	0110_0000 = 0x60	0110_0000 = 0x60	0110_0000 = 0x60	0110_0000 = 0x60
Effective Base Address	0000_0000 = 0x00	0110_0000 = 0x60	0110_0000 = 0x60	0001_0110_0000 = 0x160	0111_0110_0000 = 0x760
Comments	Minimum Size EEPROM. Loads Every Byte in the EEPROM.	EEPROM Not Big Enough for GBIC ID. LTC5100 Loads from 0x60 to 0x6F	Standard GBIC EEPROM. Smallest EEPROM That is Big Enough to Hold the LTC5100 Data and the GBIC ID. LTC5100 Loads from 0x60 to 0x6F, the First 16 Bytes of the Vendor Area	LTC5100 Loads from an Area Outside the GBIC ID Data Area	LTC5100 Loads from an Area Outside the GBIC ID Data Area

### Microprocessor Controlled Operation

An external microprocessor or a test computer can take full control of the LTC5100 by setting the Operating\_mode bit. When this bit is set, the LTC5100 stops searching for an external EEPROM and takes commands from the microprocessor. It is even possible to combine standalone and microprocessor controlled modes. If an EEPROM is present, the LTC5100 will load its configuration registers from the EEPROM at power-up. A microprocessor or test computer can then read and write the LTC5100 registers at will.

The primary purpose of the Operating\_mode bit is to stop the LTC5100's EEPROM load attempts. Once the LTC5100 has loaded itself from an EEPROM (if present), it is not

technically necessary to set the Operating\_mode bit to communicate with the LTC5100.

The LTC5100 attempts to read the EEPROM every 64ms until it successfully loads its registers or until the Operating\_mode bit is set. There is a finite chance that the microprocessor and the LTC5100 will generate an I<sup>2</sup>C bus collision if an EEPROM load attempt coincides with the microprocessor's attempt to access the LTC5100. In this case, the microprocessor will receive a NACK (not-acknowledged) response to its transmissions. The microprocessor needs only to cease transmission in accordance with the I<sup>2</sup>C protocol and try again. If the microprocessor makes this second attempt within 64ms (typical), it is guaranteed not to collide with the LTC5100.

## REGISTER DEFINITIONS

Table 7. Register Set Overview

REGISTER GROUP	REGISTER NAME		I <sup>2</sup> C COMMAND CODE (HEX)	READ/WRITE ACCESS	REFERENCE INFORMATION
	CONSTANT CURRENT CONTROL MODE	AUTOMATIC POWER CONTROL MODE			
System Operating Configuration	SYS_CONFIG	“	0x10	R/W	Table 8
	LOOP_GAIN	“	0x1E	R/W	Table 9
	PEAKING	“	0x1F	R/W	Table 10
	Reserved	“	0x08	R/W	Table 11
Laser Setup Coefficients	IB	IMD	0x15	R/W	Table 12
	IB_TC1	IMD_TC1	0x16	R/W	Table 13
	IB_TC2	IMD_TC2	0x17	R/W	Table 14
	IM	“	0x19	R/W	Table 15
	IM_TC1	“	0x1A	R/W	Table 16
	IM_TC2	“	0x1B	R/W	Table 17
Temperature	T_EXT	“	0x0D	R/W	Table 18
	T_NOM	“	0x1D	R/W	Table 19
Fault Monitoring and Eye Safety	FLT_CONFIG	“	0x13	R/W	Table 20
	FLT_STATUS	“	0x12	R	Table 21
	IB_LIMIT	“	0x11	R/W	Table 22
ADC	USER_ADC	“	0x18	R/W	Tables 23, 24
	T_INT_ADC	“	0x05	R/W	Table 25
	IM_ADC	“	0x06	R/W	Table 26
	IS_ADC	IMD_ADC	0x07	R/W	Table 27
DAC	IS_DAC	“	0x01	R/W	Table 28
	IM_DAC	“	0x02	R/W	Table 29
	PWR_LIMIT_DAC	“	0x03	R	Table 30

## REGISTER DEFINITIONS

**Table 8. Register: SYS\_CONFIG—System Configuration (I<sup>2</sup>C Command Code 0x10)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:8		
.Cml_en	7	0	Current Mode Logic Enable 0: Floating Differential Input Termination: 100Ω Across IN <sup>+</sup> and IN <sup>-</sup> 1: CML Compatible Input Termination: 50Ω from IN <sup>+</sup> to V <sub>DD(HS)</sub> and from IN <sup>-</sup> to V <sub>DD(HS)</sub>
.Md_polarity	6	0	Monitor Diode Polarity 0: Cathode Connected to the MD Pin, Sinking Current from the Pin 1: Anode Connected to the MD Pin, Sourcing Current Into the Pin
.Ext_temp_en	5	0	External Temperature Enable Selects the Source of Temperature Measurements for Temperature Compensation. 0: Internal Temperature Sensor 1: Externally Supplied Through the Serial Interface
.Power_down_en	4	1	Power Down Enable Allow Power Reduction When the Transmitter is Disabled. 0: No Power Reduction When the Transmitter is Disabled. 1: Reduce Power Consumption When Transmitter is Disabled by Turning Off the High Speed Amplifiers.
.Apc_en	3	0	Automatic Power Control Enable Select the Means of Controlling the Laser Bias Current. 0: Constant Current Control 1: Automatic Power Control Using Feedback from the Monitor Diode
.En_polarity	2	0	EN Pin Polarity Set the Input Polarity of the EN Pin. 0: Active Low: A Logic Low Input Level Enables the Transmitter. 1: Active High: A Logic High Input Level Enables the Transmitter. Note: In order to Enable the Transmitter, Both the EN Pin and Soft_en Bit Must be Asserted.
.Soft_en	1	0	Soft Transmitter Enable Enables Transmitter Through the Serial Interface. 0: Disable the Transmitter 1: Enable the Transmitter (if the EN Pin is Active) Note: In order to Enable the Transmitter, Both the EN Pin and Soft_en Bit Must be Asserted.
.Operating_mode	0	0	Digital Operating Control Mode Select Whether the LTC5100 Operates Autonomously or Under External Control. 0: Standalone Operation: Configuration Parameters are Loaded from an External EEPROM at Power Up. 1: Externally Controlled Operation: Configuration Parameters are Set by an External Microprocessor or Test Computer.

## REGISTER DEFINITIONS

**Table 9. Register: LOOP\_GAIN—Control Loop Gain (I<sup>2</sup>C Command Code 0x1E)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:8		
.Ib_gain (.Apc_gain in APC Mode)	7	0	Bias Current or APC Loop Gain
	6	0	This Bit Field Modifies the Open-Loop Gain of the Bias Current Servo Control Loop. The Effect of This Bit Field Differs in Constant Current Control (CCC) Mode and in Automatic Power Control (APC) Mode. In CCC Mode, This Bit Field is Called Ib_gain. In APC Mode, This Bit Field is Called Apc_gain.
	5	1	
	4	0	
	3	0	
			<p><b>Constant Current Control (CCC) Mode</b> (Apc_en = 0): The Loop Gain and Settling Time are Independent of Is_rng. The Default Value of Ib_gain Yields Stable but Slow Settling of the Laser Bias Current for Any Value of Is_rng.</p> <p><b>Automatic Power Control (APC) Mode</b> (Apc_en = 1): The Open-Loop Gain of the Bias Current Servo Loop Depends on the Value of Is_rng. The Default Value of Apc_gain Yields Stable but Potentially Slow Settling of the Laser Bias Current for any Value of Is_rng.</p>
Im_gain	2	0	Modulation Current Loop Gain
	1	0	This Bit Field Modifies the Open-Loop Gain of the Modulation Current Servo Loop. The Open-Loop Gain is Approximately Im_gain/32. The Loop Gain and Settling Time are Independent of Im_rng. The Default Value of Im_gain Yields Stable but Slow Settling of the Laser Modulation Current.
	0	1	

**Table 10. Register: PEAKING—High Speed Modulation Peaking (I<sup>2</sup>C Command Code 0x1F)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:5		
.Peaking	4	1	Peaking Control for the Modulation Output
	3	0	This Bit Field Controls the High Speed Peaking of the Modulation Output. Decreasing the Value of Peaking Increases the Undershoot on the Falling Edge of the Modulation Signal. The Peaking Control can be Used to Compensate for Slow Laser Turn-Off Characteristics.
	2	0	
	1	0	
	0	0	

**Table 11. Register: Reserved—Reserved for Internal Use. This Register is for Test Puposes Only. Do Not Write to this Register (I<sup>2</sup>C Command Code 0x08)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:7		
.Reserved	6	1	Reserved for Internal Use, Do Not Write.
	5	0	
	4	0	
	3	0	
.Reserved	2	1	Reserved for Internal Use, Do Not Write.
	1	0	
	0	0	



## REGISTER DEFINITIONS

**Table 12. Register: IB (IMD)—Laser Bias Current Register (Monitor Diode Current in APC Mode) (I<sup>2</sup>C Command Code 0x15)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES															
.Reserved	15:12																	
.Is_rng	11	0	Source Current Range															
	10	0	Is_rng Sets the Full-Scale Range of the SRC Pin Current. The Table Below Shows the Available Ranges. <b>Values for Is_rng</b>															
			<table><tr><th>Binary Value</th><th>Decimal Value</th><th>Nominal Full-Scale SRC Pin Current (mA)</th></tr><tr><td>00</td><td>0</td><td>9</td></tr><tr><td>01</td><td>1</td><td>18</td></tr><tr><td>10</td><td>2</td><td>27</td></tr><tr><td>11</td><td>3</td><td>36</td></tr></table>	Binary Value	Decimal Value	Nominal Full-Scale SRC Pin Current (mA)	00	0	9	01	1	18	10	2	27	11	3	36
	Binary Value	Decimal Value	Nominal Full-Scale SRC Pin Current (mA)															
	00	0	9															
	01	1	18															
10	2	27																
11	3	36																
		See the Electrical Specifications for Guaranteed Limits in Each Range.																
.Ib_nom (.Imd_nom in APC Mode)	9	0	Bias Current or Monitor Diode Current Setting at the Nominal Temperature															
	8	0	This Bit Field has Different Functions Depending on Apc_en.															
	7	0	This Bit Field is an Unsigned 10-Bit Integer.															
	6	0	<b>Constant Current Control (CCC) Mode</b> (Apc_en = 0): Ib_nom Sets the Laser Bias Current at Temperature T = T_nom. The physical Bias Current at T_nom is Given by: $I_B = \frac{I_{b\_nom}}{1024} \cdot (Is\_rng + 1) \cdot 9mA \text{ (typical)}$															
	5	0																
	4	0																
	3	0																
	2	0	<b>Automatic Power Control (APC) Mode</b> (Apc_en = 1): Imd_nom Sets the Monitor Diode Current at the Temperature T = T_nom. The Physical Monitor Diode Current at T_nom is Given by: $I_{MD} = 4.25\mu A \cdot 4^{Imd\_rng} \cdot \exp\left[\ln(8) \cdot \frac{Imd\_nom}{1024}\right]$															
	1	0																
	0	0																

**Table 13. Register: IB\_TC1 (IMD\_TC1)—Laser Bias/Monitor Diode Current First Order Temperature Coefficient (I<sup>2</sup>C Command Code 0x16)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:8		
.Ib_tc1 (.Imd_tc1 in APC Mode)	7	0	First Order Temperature Coefficient for Bias Current or Monitor Diode Current
	6	0	This Bit Field is a Signed 8-Bit, Two's Complement Integer. Thus its Value Ranges from –128 to 127.
	5	0	This Bit Field has Different Functions Depending on Apc_en.
	4	0	<b>Constant Current Control (CCC) Mode</b> (Apc_en = 0): Ib_tc1 Sets the First Order Temperature Coefficient for the Laser Bias Current. The Nominal Scaling is 2 <sup>–13</sup> /°C or 122ppm/°C per LSB.
	3	0	
	2	0	<b>Automatic Power Control (APC) Mode</b> (Apc_en = 1): Imd_tc1 Sets the First Order Temperature Coefficient for the Monitor Diode Current. See Laser Bias Current Control in APC Mode in the Operation Section for Details.
	1	0	
	0	0	

## REGISTER DEFINITIONS

**Table 14. Register: IB\_TC2 (IMD\_TC2)—Laser Bias/Monitor Diode Current Second Order Temperature Coefficient (I<sup>2</sup>C Command Code 0x17)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:8		
.Ib_tc2 (.Imd_tc2 in APC Mode)	7	0	Second Order Temperature Coefficient for Bias Current or Monitor Diode Current
	6	0	This Bit Field is a Signed 8-Bit, Two's Complement Integer. Thus its Value Ranges from –128 to 127.
	5	0	This Bit Field has Different Functions Depending on Apc_en.
	4	0	<b>Constant Current Control (CCC) Mode</b> (Apc_en = 0): Ib_tc2 Sets the Second Order Temperature Coefficient for the Laser Bias Current. The Nominal Scaling is $2^{-18}/^{\circ}\text{C}^2$ or 3.81ppm/ $^{\circ}\text{C}^2$ per LSB.
	3	0	
	2	0	<b>Automatic Power Control (APC) Mode</b> (Apc_en = 1): Imd_tc2 Sets the Second Order Temperature Coefficient for the Monitor Diode Current. See Laser Bias Current Control in APC Mode in the Operation Section for Details.
	1	0	
	0	0	

**Table 15. Register: IM—Laser Modulation Current (I<sup>2</sup>C Command Code 0x19)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES																						
.Reserved	15:12																								
.Im_rng	11	0	Modulation Current Range																						
	10	0	Im_rng Sets the Full-Scale Range of the Modulation Current																						
<table border="1"> <thead> <tr> <th rowspan="2">Binary Value</th><th rowspan="2">Decimal Value</th><th colspan="2">Nominal Full-Scale MODA and MODB Pin Current</th></tr> <tr> <th>Peak-to-Peak (mA)</th><th>Average (mA)</th></tr> </thead> <tbody> <tr> <td>00</td><td>0</td><td>9</td><td>4.5</td></tr> <tr> <td>01</td><td>1</td><td>18</td><td>9</td></tr> <tr> <td>10</td><td>2</td><td>27</td><td>13.5</td></tr> <tr> <td>11</td><td>3</td><td>36</td><td>18</td></tr> </tbody> </table>				Binary Value	Decimal Value	Nominal Full-Scale MODA and MODB Pin Current		Peak-to-Peak (mA)	Average (mA)	00	0	9	4.5	01	1	18	9	10	2	27	13.5	11	3	36	18
Binary Value	Decimal Value	Nominal Full-Scale MODA and MODB Pin Current																							
		Peak-to-Peak (mA)	Average (mA)																						
00	0	9	4.5																						
01	1	18	9																						
10	2	27	13.5																						
11	3	36	18																						
See the Electrical Specifications for Guaranteed Limits in Each Range.																									
These Currents Represent the Peak-to-Peak Current at the MODA and MODB Pins. (The MODA and MODB Pins are Tied Together On Chip).																									
.Im_nom	9	0	Modulation Current Setting at the Nominal Temperature																						
	8	0	This Bit Field is an Unsigned 10-Bit Integer. Im_nom Sets the Average Modulation Current Delivered at the MODA and MODB Pins. (The MODA and MODB Pins are Tied Together On Chip). The Peak-to-Peak Current is Twice the Average Current for a Data Stream with 50% Duty Cycle. The Modulation Current Reaching the Laser Depends on its Dynamic Resistance Relative to the Termination Resistor.																						
	7	0																							
	6	0																							
	5	0																							
	4	0																							
	3	0																							
	2	0																							
	1	0																							
	0	0																							

## REGISTER DEFINITIONS

**Table 16. Register: IM\_TC1—Laser Modulation Current First Order Temperature Coefficient (I<sup>2</sup>C Command Code 0x1A)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:8		
.Im_tc1	7	0	First Order Temperature Coefficient for Modulation Current  This Bit Field is a Signed 8-Bit, Two's Complement Integer. Thus its Value Ranges from –128 to 127. Im_tc1 Sets the First Order Temperature Coefficient for the Modulation Current. The Nominal Scaling is 2 <sup>-13</sup> /°C or 122ppm/°C per LSB.
	6	0	
	5	0	
	4	0	
	3	0	
	2	0	
	1	0	
	0	0	

**Table 17. Register: IM\_TC2—Laser Modulation Current Second Order Temperature Coefficient (I<sup>2</sup>C Command Code 0x1B)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:8		
.Im_tc2	7	0	Second Order Temperature Coefficient for Modulation Current  This Bit Field is a Signed 8-Bit, Two's Complement Integer. Thus its Value Ranges from –128 to 127. Im_tc2 Sets the Second Order Temperature Coefficient for the Laser Bias Current. The Nominal Scaling is 2 <sup>-18</sup> /°C <sup>2</sup> or 3.81ppm/°C <sup>2</sup> per LSB.
	6	0	
	5	0	
	4	0	
	3	0	
	2	0	
	1	0	
	0	0	

**Table 18. Register: T\_EXT—External Temperature (I<sup>2</sup>C Command Code 0x0D)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:10		
.T_ext	9	0	Externally Supplied Temperature for Temperature Compensation Calculations (Unsigned 10-Bit Integer)
	8	0	
	7	0	
	6	0	By Convention the Scaling of T_ext is 512K or 239°C Full Scale, Corresponding to 0.5°C/LSB. However, Any Scaling is Permissible as Long as the Temperature Compensation Coefficients are Also Appropriately Scaled.
	5	0	
	4	0	
	3	0	T_ext = (T + 273°C)/0.5°C, Where T is the External Temperature in Degrees Celsius.
	2	0	
	1	0	
	0	0	

REGISTER DEFINITIONS

Table 19. Register: T\_NOM—Nominal Temperature (Includes lmd\_rng) (I<sup>2</sup>C Command Code 0x1D)

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:12		
.lmd_rng	11	0	Monitor Diode Current Range
	10	0	lmd_rng Sets the Full-Scale Range of the Monitor Diode Current.
.T_nom	9	0	Nominal Temperature
	8	0	T_nom is the Temperature with Respect to Which All Temperature Compensation Calculations are Made. T_nom is Usually the Temperature at Which the LTC5100 and Laser Diode were Set Up In Production.
	7	0	
	6	0	
	5	0	The Scaling is 512K or 239°C Full Scale, Corresponding to 0.5°C/LSB
	4	0	T_nom = (T + 273°C)/0.5°C, Where T is the Nominal Temperature in Degrees Celsius.
	3	0	
	2	0	
	1	0	
	0	0	

## REGISTER DEFINITIONS

**Table 20. Register: FLT\_CONFIG—Fault Configuration (Refer also to Table 1) (I<sup>2</sup>C Command Code 0x13)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:12		
Rep_flt_inhibit	11	0	Repeated Fault Inhibit 0: Allow Repeated Attempts to Clear a Fault and Re-enable the Transmitter. 1: Inhibit Repeated Attempts to Clear a Fault. Only One Attempt to Clear a Fault is Allowed. If the Fault Recurs Within 25ms of Re-enabling the Transmitter, the Transmitter is Disabled Until Power is Cycled.
Rapid_restart_en	10	1	Rapid_restart_en 0: Rapid Restart Disabled: The Servo Controller Settings for the Laser Bias and Modulation Currents are Reset to Zero when the Transmitter is Disabled. When Re-enabled, the Laser Currents Start from Zero and Settle Typically Within the 300ms Standard Initialization Time, t <sub>int</sub> , from the GBIC Specification. 1: Rapid Restart Enabled: The Servo Controller Settings for the Laser Bias and Modulation Currents are Retained when the Transmitter is Disabled. When Re-enabled, the Retained Servo Values are Loaded into the SRC_DAC and MOD_DAC, Allowing Settling Typically Within the 1ms Standard Turn-On Time, t <sub>on</sub> , from the GBIC Specification.
Flt_drv_mode	9	0	FAULT Pin Drive Mode 00: Open Drain (3.3mA Sink Capability) 01: Open Drain, 280μA Internal Pull Up 10: Open Drain, 425μA Internal Pull Up 11: Push-Pull (3.3mA Source and Sink Capability)
	8	0	
Lpc_en	7	1	Laser Power Controller (LPC) Enable 0: LPC Disabled: Allows External Control of the SRC_DAC and MOD_DAC Registers from the Serial Interface. This Setting Gives an External Microprocessor or Test Computer Full Control of the SRC_DAC and MOD_DAC Registers. 1: LPC Enabled: The LPC Continuously Updates the SRC_DAC and MOD_DAC Registers to Servo Control the Laser. (Any Values Written to These Registers Over the Serial Interface Will be Overwritten by the LPC.)
Auto_shutdn_en	6	1	Automatic Transmitter Shutdown Enable 0: Disabled: When a Fault Occurs the LTC5100 Continues to Drive the Laser. This Mode Allows a Microprocessor or Test Computer to Mediate the Decision to Shut Down the Transmitter. The Microprocessor can Turn Off the Transmitter by Driving the EN Pin Inactive or by Clearing the Soft_en Bit in the SYS_CONFIG Register. 1: Enabled: When a Fault Occurs, the Transmitter is Automatically Disabled.
Flt_pin_polarity	5	1	FAULT Pin Polarity 0: Active Low: The FAULT Pin is Driven Low to Signal a Fault. 1: Active High: The FAULT Pin is Driven High to Signal a Fault.
Flt_pin_override	4	0	FAULT Pin Override 0: The FAULT Pin is Driven Active when a Fault Occurs. 1: Internal Control of the FAULT Pin is Overridden. When a Fault Occurs, the Fault is Detected and Latched Internally, but the FAULT Pin Remains Inactive. This Mode Allows a Microprocessor or Test Computer to Mediate Fault Handling. The Microprocessor can Drive the FAULT Pin Active by Setting the Force_flt Bit.
Force_flt	3	0	Force the FAULT Pin Output. Force_flt Gives a Microprocessor or Test Computer Full Control of the FAULT Pin, Allowing External Mediation of Fault Handling. 0: Force the FAULT Pin Inactive. 1: Force the FAULT Pin Active. This Bit Has No Effect Unless Flt_pin_override = 1.
Over_pwr_en	2	1	Enables Detection of a Laser Overpower Fault. 0: Disabled, 1: Enabled
Under_pwr_en	1	1	Enables Detection of a Laser Underpower Fault. 0: Disabled, 1: Enabled
Over_current_en	0	1	Enables Detection of a Laser Overcurrent Fault. 0: Disabled, 1 Enabled

## REGISTER DEFINITIONS

**Table 21. Register: FLT\_STATUS—Fault Status (I<sup>2</sup>C Command Code 0x12)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:11		
.Transmit_ready	10	0	Transmit Ready Indicates that the Laser Bias and Modulation Currents Have Settled to Within Specification and the LTC5100 is Ready to Transmit Data. A Fault Clears This Bit. 0: Not Ready, 1: Ready
.Transmitter_enabled	9	0	Transmitter Enabled Indicates That the Transmitter is Enabled and the Laser Bias and Modulation Currents Are on (Though Not Necessarily Settled.) The Transmitter is Enabled When the EN pin and Soft_en Bits are Active and No Faults Have Occurred. A Fault Clears This Bit. 0: Transmitter is Disabled, 1: Transmitter is Enabled.
.En_pin_state	8	Varies	EN Pin State Indicates the Logic Level on the EN Pin. The En_polarity Bit Has No Effect on En_pin_state. The Power-On Reset Value Reflects the State of the EN Pin. 0: EN Pin is Low. 1: EN Pin is High.
.Faulted_twice	7	0	Faulted Twice (Only Active When Rep_flt_inhibit is Set) 0: Either No Faults or Only One Fault Has Been Detected. 1: A Second Fault Has Been Detected Within 25ms of Attempting to Clear a First Fault. The Transmitter is Disabled and Can Only be Re-enabled by Cycling the Power.
.Faulted_once	6	1	Faulted Once (Only Active When Rep_flt_inhibit is Set) Indicates That a First Fault Has Been Detected. After a Fault Occurs, Faulted_once Will be Set at the Moment the Transmitter is Disabled (by Setting the EN pin of Soft_en Bit Inactive). If the Transmitter is Subsequently Re-enabled and a Second Fault Occurs Within 25ms, the Faulted_twice Bit is Set. If No Fault Occurs Within 25ms, the Faulted_once Bit is Cleared. 0: A First Fault Has Not Been Detected or Has Been Cleared. 1: A First Fault Has Been Detected.
.Faulted	5	1	Faulted 0: The LTC5100 is Not in the Faulted State. 1: A Fault Has Occurred and the LTC5100 Has Entered the Faulted State (the Transmitter is Not Disabled Unless Auto_shutdown_en is Set).
.Under_votlage Cleared-on-read	4	1	Undervoltage Fault Indicator (Always Enabled) Indicates That a Power Supply Undervoltage Event Occurred. 0: No Fault, 1: Undervoltage Fault Detected. The Undervoltage Bit is Always Set at Power Up. Read the FLT_STATUS Register Immediately After Power-Up to Clear This Bit.
.Mem_load_error Cleared-on-read	3	0	Memory (EEPROM) Load Error Indicator (Always Enabled) Indicates That an Attempt to Load the Registers from EEPROM Was Started But Did Not Complete Successfully. 0: No Fault, 1: EEPROM Load Failed.
.Over_power Cleared-on-read	2	0	Laser Overpower Fault Indicator (Enabled by Over_pwr_en) Indicates That a Laser Overpower Fault Occurred. Overpower Occurs When the Monitor Diode Current Exceeds its Set Point. An Overpower Fault Can Occur Only in APC Mode. 0: No Fault, 1: Overpower Fault Detected.
.Under_power Cleared-on-read	1	0	Laser Underpower Fault Indicator (Enabled by Under_pwr_en) Indicates That a Laser Underpower Fault Occurred. Underpower Occurs When the Monitor Diode Current Falls Below its Set Point. An Underpower Fault Can Occur Only in APC Mode. 0: No Fault, 1: Underpower Fault Detected.
.Over_current Cleared-on-read	0	0	Laser Overcurrent Fault Indicator (Enabled by Over_current_en) Indicates That the Laser Bias Current Exceeded the Value Set in the IB_LIMIT Register. 0: No Fault, 1: Overcurrent Fault Detected.

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## REGISTER DEFINITIONS

**Table 22. Register: IB\_LIMIT—Laser Bias Current Limit (I<sup>2</sup>C Command Code 0x11)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:7		
.Ib_limit	6	0	Laser Bias Current Limit
	5	0	This Bit Field is an Unsigned 7-Bit Integer
	4	0	Sets the Detection Level for an Over_current Fault. When the Laser Bias Current Exceeds This Level an Over_current Fault is Generated (Provided Over_current_en is Set).
	3	0	The Physical Bias Current Level is Given By: $I_{B(LIMIT)} = \frac{I_{b\_limit}}{128} \cdot (I_{s\_rng} + 1) \cdot 9mA \text{ (typical)}$
	2	0	
	1	0	
	0	0	

**Table 23. Register: USER\_ADC—Writing (I<sup>2</sup>C Command Code 0x18)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES	
.Reserved	15:3			
.Adc_src_sel	2	0	ADC Source Select	
	1	0	Selects the Signal to be Converted by the ADC During the User ADC Cycle	
	0	0	<b>User ADC Signal Sources</b>	
	<b>Signal Select (Binary)</b>	<b>Signal Name</b>	<b>Description</b>	<b>Scaling</b>
	000	I <sub>S</sub>	Source Current (SRC Pin Current)	I <sub>S</sub> = ADC_code/1024 • (I <sub>S</sub> _rng + 1) • 9mA
	001	I <sub>M</sub>	Average Modulation Current (MODA +MODB Pin Current)	I <sub>M</sub> = ADC_code/1024 • (I <sub>M</sub> _rng + 1) • 9mA
	010	V <sub>LD</sub>	Laser Diode Voltage	V <sub>LD</sub> = ADC_code/1024 • 3.5V
	011	I <sub>MD</sub>	Monitor Diode Current	I <sub>MD</sub> = 4.25µA • 4 <sup>I<sub>md</sub>_rng</sup> • exp[ln(8) • ADC_code/1024]
	100	T	Temperature	T(°C) = ADC_code • 0.5°C – 273°C
	101	V <sub>TERM</sub>	Termination Resistor Voltage	V <sub>TERM</sub> = ADC_code/1024 • (I <sub>S</sub> _rng + 1) • 400mV
	110	Reserved	Reserved	
	111	Reserved	Reserved	



## REGISTER DEFINITIONS

**Table 24. Register: USER\_ADC—Reading (I<sup>2</sup>C Command Code 0x18)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15		
.Adc_src	14	0	ADC Signal Source
	13	0	Specifies the Signal Source of the Last User ADC Conversion. See Table 23 for the Definition of These Signal Sources. Adc_src Reflects the Last Signal Source Converted. It Does Not Necessarily Hold the Last Value Written to the ADC_src_sel Bit Field.
	12	0	
.Reserved	11		
.Valid	10	0	ADC Data Valid Indicates That the Result in the Data Bit Field (Defined Below) Contains Newly Converted Data Since the Last Time Adc_src_sel Was Written or This Register Was Read. Immediately After Power Up Valid is False. Valid Becomes True as Soon as the First User ADC Conversion is Completed.
			0: The ADC Result is Not a Valid Conversion of the Most Recently Selected ADC Source. 1: The ADC Has Finished Conversion and the Result is Valid.
.Data	9	0	ADC Data (10-Bit Unsigned Integer)
	8	0	Contains the Result of the Last User ADC Conversion. See Table 23 for the Definition of the Available Signal Sources.
	7	0	
	6	0	
	5	0	
	4	0	
	3	0	
	2	0	
	1	0	
	0	0	

**Table 25. Register: T\_INT\_ADC—Internal Temperature ADC (I<sup>2</sup>C Command Code 0x05)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:10		
.T_int_adc	9	0	ADC Reading of the Internal (Die) Temperature (10-Bit Unsigned Integer)
	8	0	This Bit Field Contains the Result of the Last Conversion of the LTC5100's Internal Die Temperature.
	7	0	
	6	0	
	5	0	The Scaling is 512°K or 239°C Full Scale, Corresponding to 0.5°C/LSB.
	4	0	
	3	0	$T = T\_int\_adc \cdot 0.5^{\circ}\text{C} - 273^{\circ}\text{C}$ , Where T is the Internal Temperature in Degrees Celsius.
	2	0	
	1	0	
	0	0	

## REGISTER DEFINITIONS

**Table 26. Register: IM\_ADC—Modulation Current ADC (I<sup>2</sup>C Command Code 0x06)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:10		
.Im_adc	9	0	ADC Reading of the Modulation Current (10-Bit Unsigned Integer)
	8	0	Im_adc Contains the Last ADC Conversion of the Average Modulation Current Delivered at the MODA and MODB Pins. (The MODA and MODB Pins are Tied Together On-Chip.) The Peak-to-Peak Current is Twice the Average Current for a Data Stream with 50% Duty Cycle. The Modulation Current Reaching the Laser Depends on its Resistance Relative to the Termination Resistor.
	7	0	
	6	0	
	5	0	
	4	0	The Average Physical Current at the MODA and MODB Pins is Given By: $I_M = \frac{ADC\_code}{1024} \cdot (Im\_rng + 1) \cdot 9mA \text{ (typical)}$
	3	0	
	2	0	
	1	0	
	0	0	

**Table 27. Register: IS\_ADC (IMD\_ADC)—Source Current/Monitor Diode Current ADC (I<sup>2</sup>C Command Code 0x07)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:10		
.Is_adc (.Imd_adc in APC Mode)	9	0	ADC Reading of the SRC Pin Current or Monitor Diode Current
	8	0	This Bit Field Has Different Functions Depending on Apc_en.
	7	0	
	6	0	<b>Constant Current Control (CCC) Mode</b> (Apc_en = 0): Is_adc Contains the Last ADC Conversion of the SRC Pin Current. The Physical SRC Pin Current is Given By: $I_S = \frac{ADC\_code}{1024} \cdot (Is\_rng + 1) \cdot 9mA \text{ (typical)}$
	5	0	
	4	0	
	3	0	<b>Automatic Power Control (APC) Mode</b> (Apc_en = 1): Imd_adc Contains the Last ADC Conversion of the Monitor Diode Current. The Physical Monitor Diode Current is Given By: $I_{MD} = 4.25\mu A \cdot 4^{Imd\_rng} \cdot \exp\left[\ln(8) \cdot \frac{ADC\_code}{1024}\right]$
	2	0	
	1	0	
	0	0	

**Table 28. Register: IS\_DAC—Source Current DAC (I<sup>2</sup>C Command Code 0x01)**

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:10		
.Is_dac	9	0	DAC Setting for the Source Current (the SRC Pin Current)
	8	0	Read Access to This DAC is Always Available. Write Access is Only Valid if LPC_en = 0.
	7	0	
	6	0	$I_S = \frac{Is\_dac}{1024} \cdot (Is\_rng + 1) \cdot 9mA \text{ (typical)}$
	5	0	
	4	0	
	3	0	
	2	0	
	1	0	
	0	0	

## REGISTER DEFINITIONS

Table 29. Register: IM\_DAC—Modulation Current DAC (I<sup>2</sup>C Command Code 0x02)

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:10		
.Im_dac	9	0	DAC Setting for the Peak-to-Peak Modulation Current (the Combined MODA and MODB Pin Currents) Read Access to This DAC is Always Available. Write Access is Only Valid if LPC_en = 0.  $I_M = \frac{Im\_dac}{1024} \cdot (Im\_rng + 1) \cdot 9mA \text{ (typical)}$
	8	0	
	7	0	
	6	0	
	5	0	
	4	0	
	3	0	
	2	0	
	1	0	
	0	0	

Table 30. Register: PWR\_LIMIT\_DAC—Optical Power Limit DAC—Read Only (I<sup>2</sup>C Command Code 0x03)

REGISTER .BITFIELD	BIT	RESET VALUE (BIN)	FUNCTION AND VALUES
.Reserved	15:7		
.pwr_limit_dac Read Only	6	0	DAC Setting for the Over and Underpower Fault Detection Comparator (Read Only)
	5	0	This Bit Field Has Different Functions Depending on Apc_en.
	4	0	
	3	0	
	2	0	<b>Constant Current Control (CCC) Mode</b> (Apc_en = 0): Pwr_limit_dac Has No Function in This Mode. Its Contents are Undefined.  <b>Automatic Power Control (APC) Mode</b> (Apc_en = 1): Pwr_limit_dac Tracks the Value of the Monitor Diode Current. The Laser Power Controller Continuously Updates the PWR_LIMIT_DAC with the Most Recent ADC Reading of Imd. Reading the DAC Will Return the Value of Imd_adc Shifted Right by Three Bits.
	1	0	
	0	0	

## APPLICATIONS INFORMATION

### HIGH SPEED DESIGN AND LAYOUT

Figure 29 and Figure 30 show the schematic and layout of a minimum component count circuit for standalone operation. The exposed pad of the package is soldered to a copper pad on top of the board, and nine vias couple this pad to the ground plane. The four  $V_{SS}$  pins (Pins 1, 4, 9,

and 12) have webs of copper connecting them to the central pad to reduce ground inductance. The laser modulation current returns to the ground plane primarily through the exposed pad. Any measures that reduce the inductance from the pad to the ground plane improve the modulation waveforms and reduce RFI.

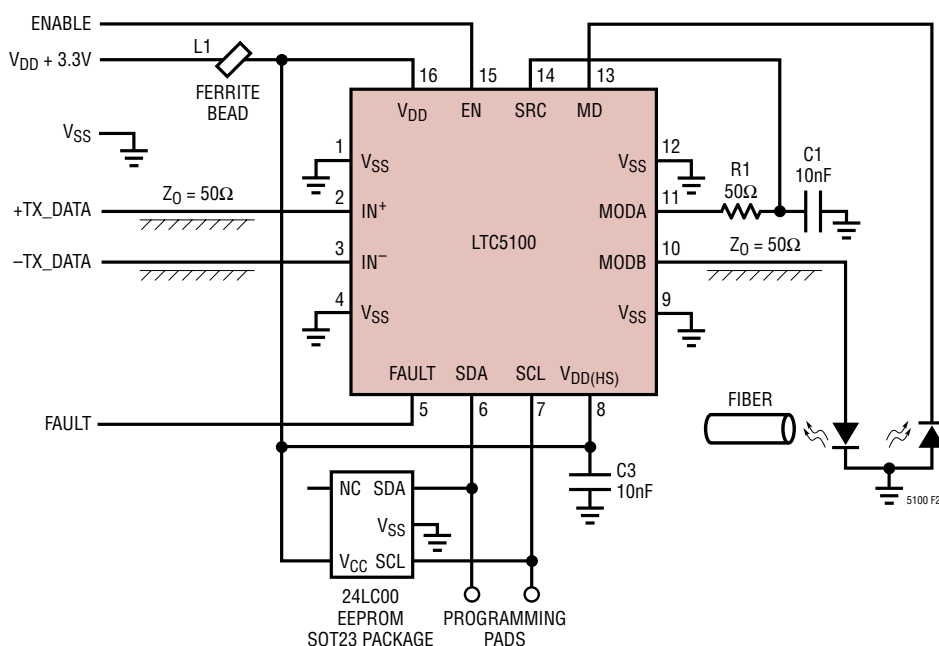


Figure 29. Schematic of a Minimum Component Count Circuit

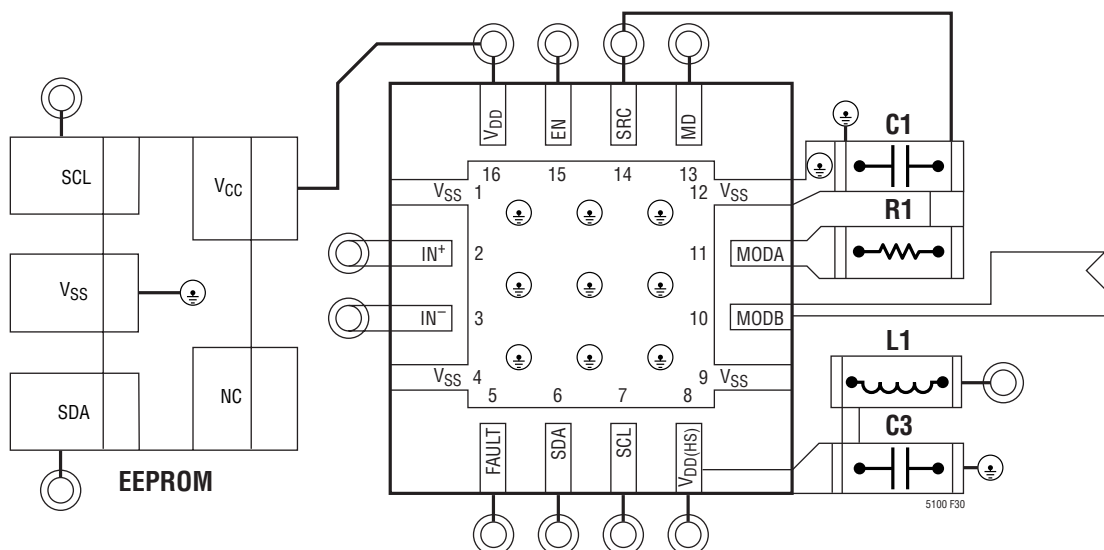


Figure 30. Layout of the Minimum Component Count Circuit Using 0402 Passive Components

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## APPLICATIONS INFORMATION

The termination resistor, R1, and its decoupling capacitor, C1, are placed as close as possible to the LTC5100 to reduce inductance. Inductance in these two components causes high frequency peaking and overshoot in the current delivered to the laser. R1 and C1 are folded against each other so that their mutual inductance and counter-flowing current partially cancel their self-inductance. C1 has two vias to the ground plane and a trace directly to Pin 12. The layout shows the EEPROM placed next to the

LTC5100. However, placement of the EEPROM is not critical. It can be placed several centimeters from the LTC5100 or on the back of the PC board if desired.

The transmission line connecting the MODB pin to the laser has a short length of minimum width trace. The net inductance of this section of trace helps compensate on-chip capacitance to further reduce reflections from the chip.

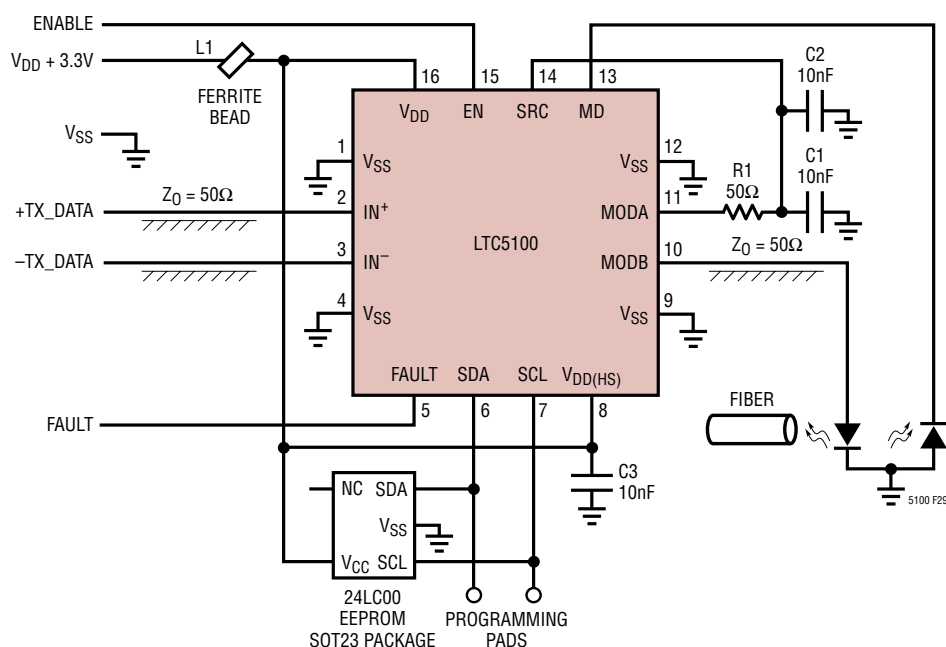


Figure 31. Schematic of a Minimum Output Reflection Coefficient Circuit

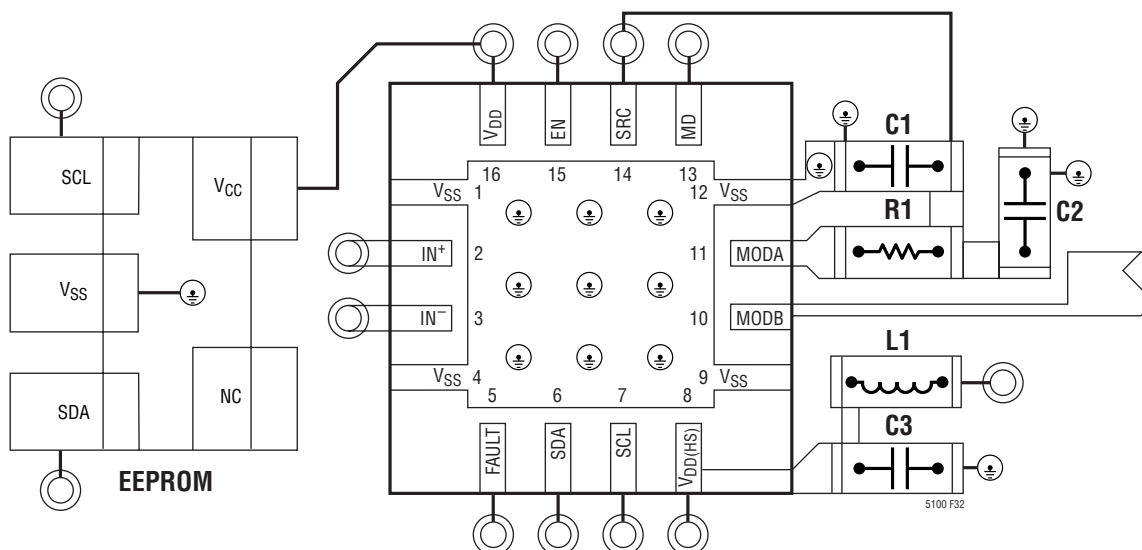


Figure 32. Layout of the Minimum Reflection Coefficient Circuit Using 0402 Passive Components

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## APPLICATIONS INFORMATION

Figure 31 and Figure 32 show the schematic and layout of a minimum reflection coefficient, minimum peaking solution. Two capacitors, C1 and C2 are used to further reduce the inductance in the termination network. C2 has two vias to the ground plane.

### TEMPERATURE COMPENSATION

The LTC5100 has first and second order digital temperature compensation for the laser bias current, laser modulation current, and monitor diode current. Recall that in constant current control mode, the LTC5100 provides direct temperature compensation of the laser bias current and the laser modulation current. In automatic power control mode, the laser bias current is under closed-loop control and the LTC5100 provides temperature compensation for the monitor diode current and the laser modulation current. The simplest procedure for determining the temperature coefficients (TC1 and TC2 in Equation 12, Equation 18, Equation 23, and Equation 29) is as follows:

- Select a nominal or representative laser diode and assemble it into a transceiver module with the LTC5100.
- Set all temperature coefficients to zero.
- Place the transceiver module in a temperature chamber and find the values of  $I_{b\_nom}$ ,  $I_{m\_nom}$ , and  $I_{md\_nom}$  that give constant average optical power and extinction ratio at several temperature points.
- Record the LTC5100's temperature reading,  $T_{int}$ , at each temperature point.
- Select a convenient value for  $T_{nom}$ , the nominal temperature. (It is customary, but not mandatory, to use 25°C for the nominal temperature.)
- Find the best values of TC1 and TC2 by fitting the quadratic temperature compensation formula (Equation 12) to the experimental values of  $I_{b\_nom}$ ,  $I_{m\_nom}$ ,  $I_{md\_nom}$ , and  $T_{int}$ .

To configure the LTC5100 for normal operation, set the nominal current to the value found at the nominal temperature. Set TC1 and TC2 to the values determined by the best fit of the data. For standalone operation, store these values in the EEPROM. For microprocessor operation, store the values in the microprocessor's internal non-volatile memory or in another source of nonvolatile memory and load them into the LTC5100 after power-up.

The above procedure not only corrects for the laser temperature drift, but also corrects the small temperature drift found in the LTC5100's internal references.

### DEMONSTRATION BOARD

Figure 33 shows the schematic of the DC499 demonstration board. Details of the use of this demo board and accompanying software can be found in the DC499 demo board manual. Figure 34 shows the layout of the demo board and Table 31 gives the bill of materials for the demo board.

The core applications circuit for the LTC5100 VCSEL driver appears inside the box in Figure 33. This is the complete circuit for an optical transceiver module, including power supply filtering. It consists of the LTC5100 with EEPROM for storing setup parameters, L1 and C3 for power supply filtering, and R1, C1, and C2 for terminating the 50Ω modulation output. The circuitry outside the box in Figure 33 is for support of the demonstration. 5V power enters through 2-pin connector P2 and is regulated by U3 to 3.3V to power the LTC5100. Connector P1 sends 5V power and serial control signals to another board, allowing a personal computer to control the LTC5100. U4 produces 1.8VDC to bias the modulation output for electrical eye measurements.

High speed data enters the LTC5100 through SMA connectors J1 and J2. The LTC5100 high speed inputs are internally AC coupled with rail-to-rail common mode input voltage range. The input signal swing can go as much as 300mV above  $V_{DD}$  or below  $V_{SS}$  without degrading performance or causing excessive current flow. The high speed inputs may be AC coupled, in which case the common mode voltage floats to mid-supply or 1.65V nominally.

A common cathode VCSEL can be attached to the demo board via SMA connector J3. R1 establishes a precision, low reflection coefficient 50Ω modulation drive. By maintaining a wide band microwave quality 50Ω path, the length of the connection to the laser can be arbitrarily long. The LTC5100 generates 20% to 80% transition times of 60ps (80ps 10% to 90%), corresponding to an instantaneous transition filtered by a 4.4GHz Gaussian lowpass filter. At these speeds the primary limitation on line length is high frequency loss. For high grade, low loss laboratory cabling with silver coated center conductor and foamed PTFE dielectric, a practical limit is about 30cm.

sn5100 5100fs

The demo board includes an EEPROM that provides non-volatile storage for the LTC5100's configuration settings and parameters. For example, the EEPROM stores parameters for the laser bias and modulation levels as well as temperature coefficients and fault detection modes. The LTC5100 transfers the data in the EEPROM to its internal registers at power up. The LTC5100 is designed for hot plugging and can be configured to load the EEPROM and enable the transmitter as soon as power is applied. **Be**

The demo board has three jumpers for enabling the transmitter, observing the electrical eye diagram, and measuring the LTC5100's power supply current. Details of the use of these jumpers are given in the DC499 demo manual.





## APPLICATIONS INFORMATION

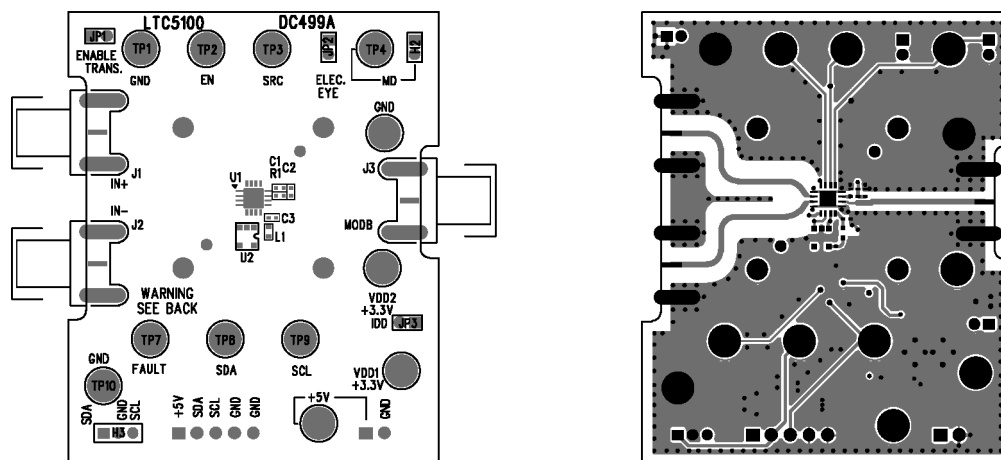


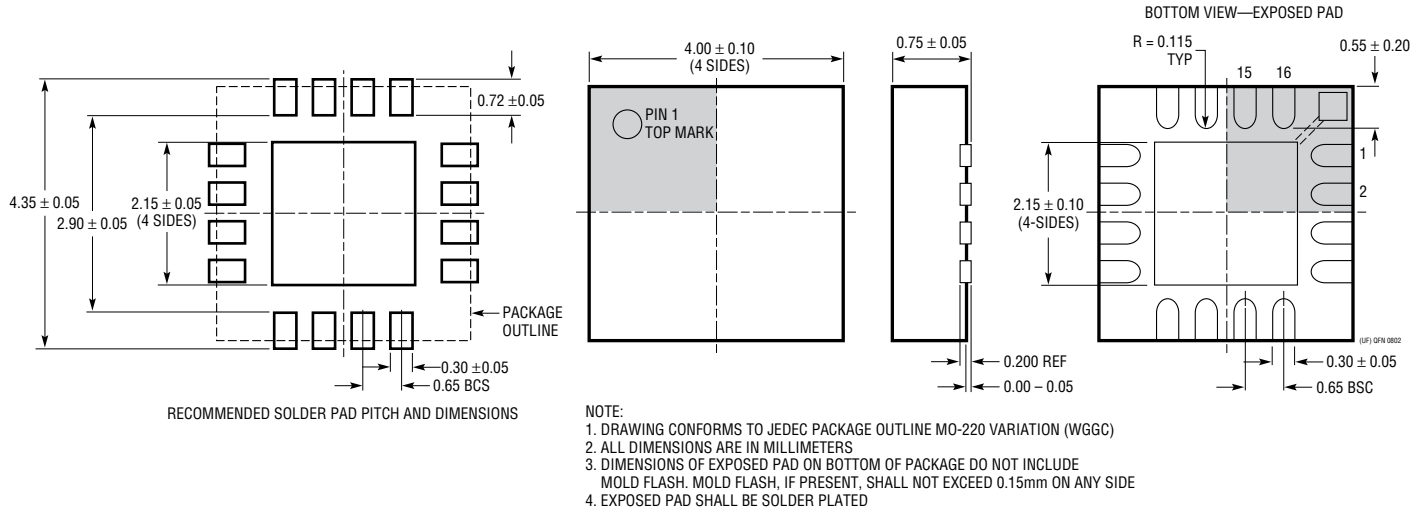
Figure 34 Layout of the DC499 Demo Board (Silkscreen and Top Layer Copper)

Table 31. Bill of Materials for the DC499 Demo Board

REFERENCE	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
5V, V <sub>DD1</sub> , V <sub>DD2</sub> , SDA, SCL, FAULT, EN, SRC, MD, GND(3)	12	2501-2	1-Pin Terminal Turret Test Point	Mill-Max	(516) 922-6000
C1, C2, C3	3	GRP155R71E103JA01	0.01μF 25V 5% X7R 0402 Capacitor	Murata	(770) 436-1300
C4, C5, C6	3	12066D106MAT	10μF 6.3V 20% X5R 1206 Capacitor	AVX	(843) 946-0362
C7	1	0603YC104KAT	0.1μF 16V 10% X7R 0603 Capacitor	AVX	(843) 946-0362
D2,D3	2	B320A	3A Schottky Rectifier Diode	Diodes, Inc.	(805) 446-4800
D4	0	Option (No Load)	N/A (No Load)	N/A	
H2, JP1, JP2, JP3	4	2802S-02G2	2mm 2-Pin Header	Comm Con	(626) 301-4200
H3	1	2802S-03G2	2mm 3-Pin Header	Comm Con	(626) 301-4200
J1, J2, J3	3	142-0701-851	50Ω SMA Edge-Lanch Connector	Johnson Components	(800) 247-8256
L1	1	BLM15AG121PN1D	0402 Ferrite Bead	Murata	(770) 436-1300
P1	1	70553-0004	5-Pin Right Angle Header	Molex	(630) 969-4550
P2	1	70553-0001	2-Pin Right Angle Header	Molex	(630) 969-4550
R1	1	CR05-49R9FM	49.9Ω 1% 1/16W 0402 Resistor	AAC	(800) 508-1521
R2, R5	2	CR16-2212FM	22.1k 1% 1/16W 0603 Resistor	AAC	(800) 508-1521
R3	1	CR16-2672FM	26.7k 1% 1/16W 0603 Resistor	AAC	(800) 508-1521
R4	1	CR16-10R0FM	10Ω 1% 1/16W 0603 Resistor	AAC	(800) 508-1521
U1	1	LTC5100	QFN 4mm × 4mm IC	LTC	(408) 432-1900
U2	1	24LC00	128-Bit IC Bus Serial EEPROM 5-Pin SOT-23	Microchip	
U3	1	LT1762EMS8-3.3	Low Noise LDO Micropower Regulator IC	LTC	(408) 432-1900
U4	1	LT1812CS5	Op Amp with Shutdown IC	LTC	(408) 432-1900
H3	1	CCIJ2mm-138G	2-Pin 2mm Shunt	Comm Con	(626) 301-4200

## PACKAGE DESCRIPTION

**UF Package**  
**16-Lead Plastic QFN (4mm × 4mm)**  
 (Reference LTC DWG # 05-08-1692)



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1773	Current Mode Synchronous Buck Regulator	Design Note 295 "High Efficiency Adaptable Power Supply for XENPAK 10Gbps Ethernet Transceivers"
LTC1923	High Efficiency Thermoelectric Cooler Controller	
LT <sup>®</sup> 1930A	2.2MHz Step-Up DC/DC Converter in 5-Lead SOT-23	Design Note 273 "Fiber Optic Communication Systems Benefit from Tiny, Low Noise Avalanche Photodiode Bias Supply"

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