Ultralow V_{IN}, 15A DC/DC µModule Regulator

FEATURES

- **Complete Switch Mode Power Supply**
- **Input Voltage Range: 1.5V to 5.5V**
- **15A DC Output**
- **Output Voltage Range: 0.8V to 5V**
- **±1.5% Total DC Output Error**
- **Differential Remote Sensing for Precision Regulation**
- **Current Mode Control/ Fast Transient Response**
- **Overcurrent Foldback Protection**
- **Parallel Multiple LTM®4611s for Current Sharing**
- **Frequency Synchronization**
- Selectable Pulse-Skipping or Burst Mode® Operation
- Soft-Start/Voltage Tracking
- Up to 94% Efficiency
- Output Overvoltage Protection
- Small 15mm × 15mm × 4.32mm LGA Package

APPLICATIONS

- Telecom Servers and Networking Equipment
- Storage and ATCA Cards
- General Purpose Point of Load Regulation

DESCRIPTION

The LTM®4611 is a high density 15A output, switch mode DC/DC buck converter power supply capable of operating from very low voltage input supplies. Included in the package are the buck switching controller, power FETs, inductor and loop-compensation components. The LTM4611 delivers up to 15A continuous current at high efficiency from an input voltage of $1.5V_{IN}$ up to $5.5V_{IN}$. The output voltage is set between 0.8V and 5V by a resistor. Only a few input and output capacitors are needed.

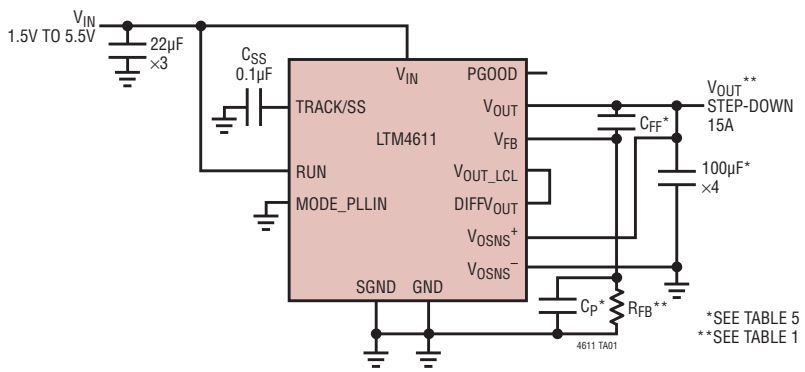
High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, multiphase/current sharing operation, Burst Mode operation and output voltage tracking for supply rail sequencing.

The LTM4611 is available in a thermally enhanced 15mm × 15mm × 4.32mm LGA package. The LTM4611 is PB-free and RoHS compliant.

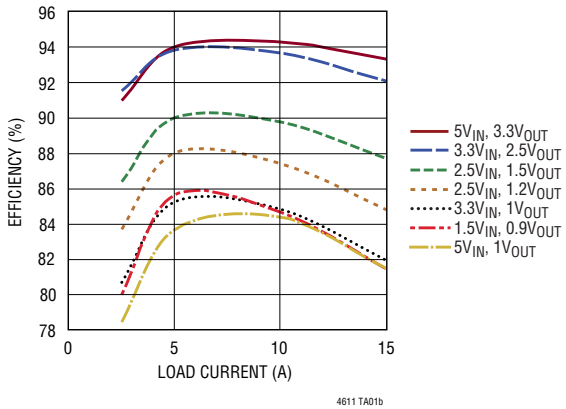
Click to view associated TechClip Videos.

TYPICAL APPLICATION

$1.5V_{IN}$ to $5.5V_{IN}$, 15A Step-Down DC/DC µModule® Regulator



Efficiency vs Load Current



ABSOLUTE MAXIMUM RATINGS

(Note 1)

Terminal Voltages

V_{IN} ..... –0.2V to 6V

V_{OUT} with

DIFF AMP....–0.1V to the Lesser of (V_{IN} + 0.1V) or 4V

V_{OUT} without

DIFF AMP..–0.1V to the Lesser of (V_{IN} + 0.1V) or 5.5V

RUN, $INTV_{CC}$, V_{OUT_LCL} 6V

MODE_PLLIN, PLLFLTR/f_{SET},

TRACK/SS, V_{OSNS}–, V_{OSNS}+,

PGOOD ..... –0.3V to 5.5V

COMP, V_{FB}..... –0.3V to 2.7V

Terminal Currents

$DIFFV_{OUT}$.....–10mA to 1mA

Temperatures

Operating Junction Temperature Range

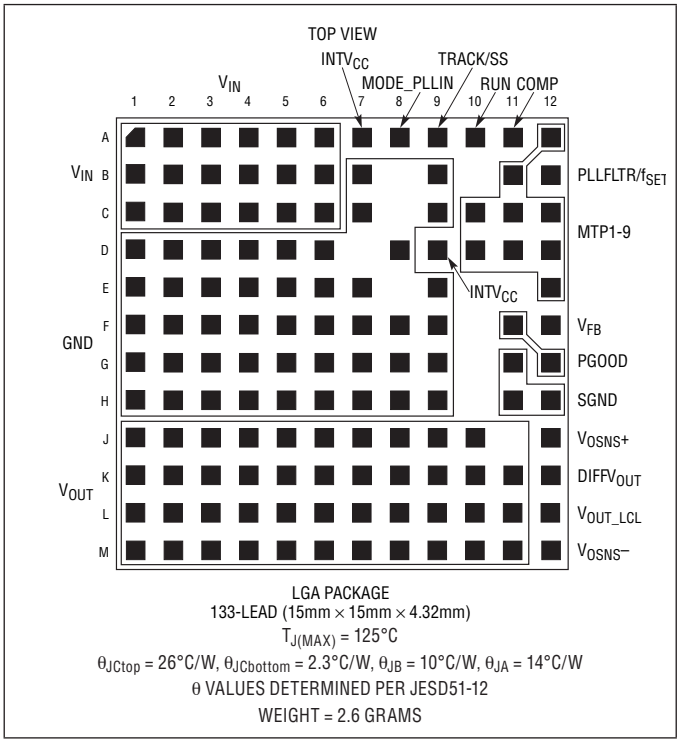
(Note 2) .....–40°C to 125°C

Storage Temperature Range .....–55°C to 125°C

Peak Solder Reflow Body Temperature

(Note 3) ..... 250°C

PIN CONFIGURATION



LGA PACKAGE
133-LEAD (15mm × 15mm × 4.32mm)
$T_{J(MAX)}$ = 125°C
θ_{JCtop} = 26°C/W, $\theta_{JCbottom}$ = 2.3°C/W, θ_{JB} = 10°C/W, θ_{JA} = 14°C/W
θ VALUES DETERMINED PER JESD51-12
WEIGHT = 2.6 GRAMS

ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM4611EV#PBF	LTM4611EV#PBF	LTM4611V	133-Lead (15mm × 15mm × 4.32mm) LGA	–40°C to 125°C
LTM4611IV#PBF	LTM4611IV#PBF	LTM4611V	133-Lead (15mm × 15mm × 4.32mm) LGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.3V, per the typical application in Figure 21.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Specifications							
V_{IN}	Input DC Voltage		●	1.5		5.5	V
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	●	1.1	1.22	1.35	V
V_{RUNHYS}	RUN Pin On Hysteresis				80		mV
$V_{RUN(FLOAT)}$	RUN Pin Voltage when Floating			3.4	3.65	4	V
$I_{RUN(UP,1V)}$	RUN Pin Pull-Up Current (RUN = 1V)				1.1		µA
$I_{RUN(UP,1.5V)}$	RUN Pin Pull-Up Current (RUN = 1.5V)				10		µA
$I_{RUN(DOWN,5V)}$	RUN Pin Pull-Down Current (RUN = 5V)				1		nA
I_Q	Input Supply Bias Current	V_{OUT} = 1.5V, Burst Mode Operation, I_{OUT} = 0.1A V_{OUT} = 1.5V, Pulse-Skipping Mode, I_{OUT} = 0.1A V_{OUT} = 1.5V, Switching Continuous, I_{OUT} = 0.1A Shutdown, RUN = 0V			70 140 145 1.1		mA mA mA mA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 2.5V, V_{OUT} = 1.5V, I_{OUT} = 15A V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 15A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 15A V_{IN} = 1.5V, V_{OUT} = 0.8V, I_{OUT} = 15A			10.4 7.9 5.3 10.2		A A A A
Output Specifications							
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	Utilizing DIFF_AMP, R_{FB} = Not Used, V_{IN} = 1.5V to 5.5V, I_{OUT} = 0A to 15A (Note 4), R_{FB} Electrically Floating, MODE_PLLIN = GND	 ●	0.785 0.781	0.797 0.797	0.809 0.813	V V
$V_{OUT(RANGE)}$	Utilizing DIFF_AMP	(Example See Figure 21)				3.7	V
	Not Utilizing DIFF_AMP	(Example See Figure 20)				5.4	V
$I_{OUT(DC)}$	Output Continuous Current Range	V_{OUT} = V_{FB} (Note 4)		0		15	A
$\frac{\Delta V_{OUT}\ (Line)}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = V_{FB}, V_{IN} from 1.5V to 5.5V, I_{OUT} = 0A	●			0.3	%
$\frac{\Delta V_{OUT}\ (Load)}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 15A, V_{IN} = 3.3V (Note 4)	●		0.2	0.5	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF ×4 X5R Ceramic, V_{IN} = 3.3V, V_{OUT} = 1.5V			8		mV_{P-P}
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF ×4 X5R Ceramic, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} = 3.3V, C_{SS} = 1nF			5		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF ×4 X5R Ceramic, No Load, C_{SS} = 1nF, V_{IN} = 3.3V, V_{OUT} = 1.5V			500		µs
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load V_{IN} = 3.3V, V_{OUT} = 1.5V, C_{OUT} = 100µF ×4 X5R Ceramic, C_{FF} = 100pF			60		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load V_{IN} = 3.3V, V_{OUT} = 1.5V, C_{OUT} = 100µF ×4 X5R Ceramic, C_{FF} = 100pF			40		µs
$I_{OUT(PK)}$	Output Current Limit	V_{IN} = 5V, V_{OUT} = 1.5V V_{IN} = 3.3V, V_{OUT} = 1.5V			30 30		A A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full internal operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 3.3V, per the typical application in Figure 21.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = V_{FB}	●	0.783	0.797	0.811	V
I_{FB}					–10		nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.84	0.87	0.89	V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V		0.9	1.4	1.9	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			90		ns
R_{FBHI}	Resistor Between V_{OUT_LCL} and V_{FB} Pins			60.05	60.40	60.75	kΩ
V_{OSNS}^+, V_{OSNS}^- CM RANGE	Common Mode Input Range	V_{IN} = 3.3V, Run > 1.5V		0		$INTV_{CC}$ – 1	V
$DIFFV_{OUT}$ Range	DIFF_AMP Output Voltage Range	V_{IN} = 3.3V, $DIFFV_{OUT}$ Load = 100k		0		$INTV_{CC}$	V
V_{OS}	DIFF_AMP Input Offset Voltage Magnitude		 ●			1.25 2	mV mV
A_V	DIFF_AMP Differential Gain				1		V/V
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output V_{FB} Ramping Positive, PGOOD Transitioning ↓ V_{FB} Ramping Positive, PGOOD Transitioning ↑ V_{FB} Ramping Negative, PGOOD Transitioning ↓ V_{FB} Ramping Negative, PGOOD Transitioning ↑		 –10 5 5 –10	 –7.5 7.5 7.5 –7.5	 –5 10 10 –5	 % % % %
SR	DIFF_AMP Slew Rate				2		V/µs
GBP	DIFF_AMP Gain-Bandwidth Product				3		MHz
CMRR	DIFF_AMP Common Mode Rejection				100		dB
R_{IN}	DIFF_AMP Input Resistance	V_{OSNS}+ to GND		19.9	20.0	20.1	kΩ
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	1.5V < V_{IN} < 5.5V		4.8	5	5.2	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 50mA			0.5		%
Oscillator and Phase-Locked Loop							
f_S	Output Ripple Voltage Frequency	V_{IN} = 3.3V, V_{OUT} = 1.5V, 0.85V ≤ PLLFLTR/f_{SET} ≤ 2.0V		280		835	kHz
f_{SYNC}	SYNC Capture Range			360		710	kHz
PLLFLTR/$f_{SET(FLOAT)}$	PLLFLTR/f_{SET} Open-Circuit Voltage	PLLFLTR/f_{SET} Pin Voltage When Floating			1.23		V
Frequency Nominal	Nominal Frequency	PLLFLTR/f_{SET} Floating			500		kHz
Frequency Low	Lowest Frequency	PLLFLTR/f_{SET} = 0.85V			330		kHz
Frequency High	Highest Frequency	PLLFLTR/f_{SET} = 2.0V			780		kHz
$I_{PLLFLTR}$	PLLFLTR Sourcing Capability Sinking Capability	 Mode_PLLIN Frequency > f_{OSC} Mode_PLLIN Frequency < f_{OSC}			 –13 13		 µA µA
$R_{MODE(PLLIN)}$	Mode_PLLIN Input Resistance				250		kΩ
V_{IH}	Clock Input Level High			2.0			V
V_{IL}	Clock Input Level Low					0.6	V
Mode_PLLIN Clock	Clock Input Duty Cycle Range			40	50	60	%

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4611 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4611E is guaranteed to meet performance specifications over the 0°C to 125°C operating junction temperature (T_J) range. Specifications over the full –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4611I is guaranteed to meet specifications over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

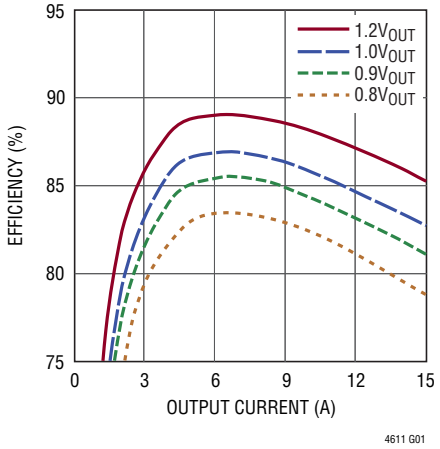
Note 3: Consistent with Pb-free 260°C peak IR reflow soldering profiles. See Application Note 100.

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

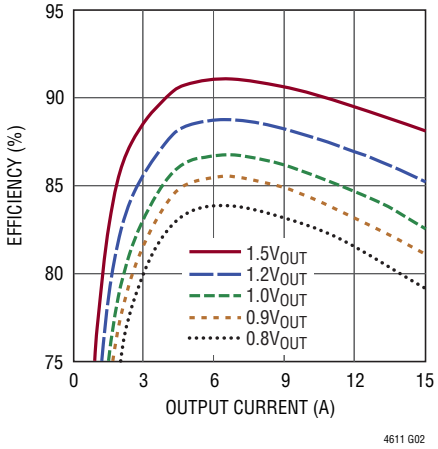
Note 5: The minimum on-time condition is specified for a peak-to-peak inductor ripple current of ~40% of I_{MAX} Load. (See the Typical Applications section)

TYPICAL PERFORMANCE CHARACTERISTICS

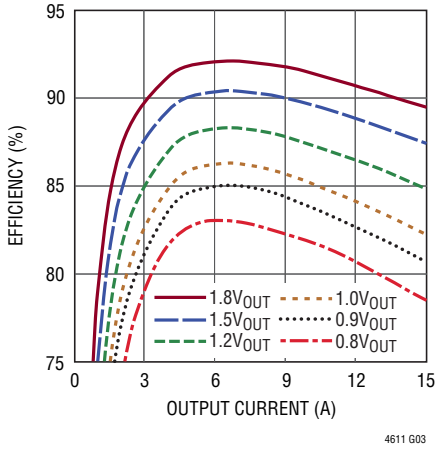
Efficiency vs Load Current at 1.5V_{IN}, Forced Continuous Mode



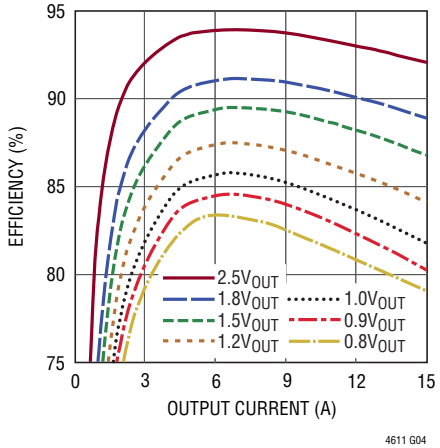
Efficiency vs Load Current at 1.8V_{IN}, Forced Continuous Mode



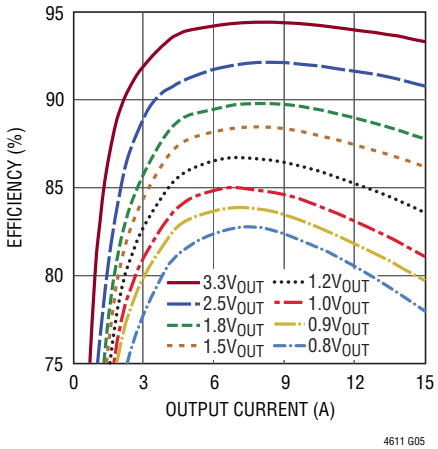
Efficiency vs Load Current at 2.5V_{IN}, Forced Continuous Mode



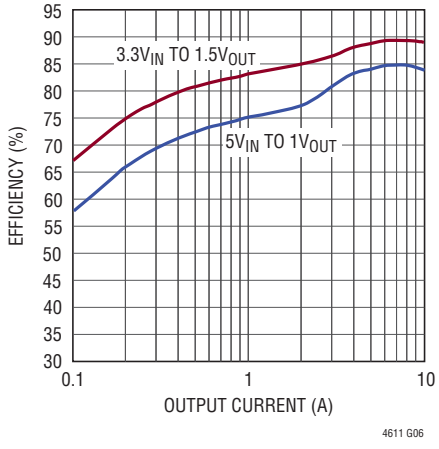
Efficiency vs Load Current at 3.3V_{IN}, Forced Continuous Mode



Efficiency vs Load Current at 5V_{IN}, Forced Continuous Mode

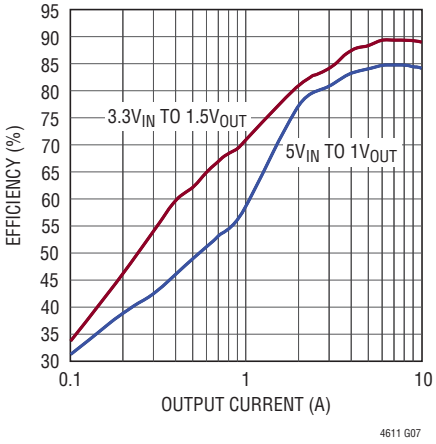


Burst Mode Efficiency

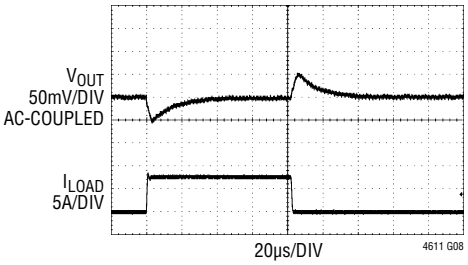


TYPICAL PERFORMANCE CHARACTERISTICS

Pulse-Skipping Mode Efficiency

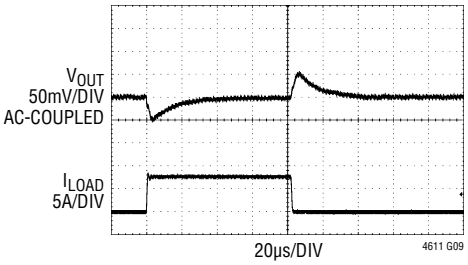


1V Transient Response, $3.3V_{IN}$



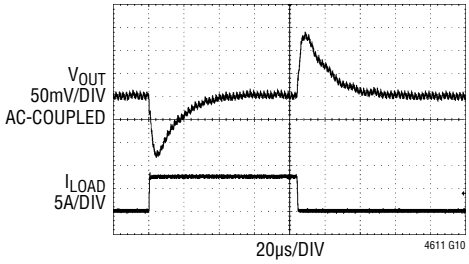
V_{IN} = 3.3V, V_{OUT} = 1V, USING DIFF AMP
4 × 100µF CERAMIC OUTPUT CAPACITORS
C_{FF} = 47pF, C_P = NONE
7.5A LOAD STEP AT 7.5A/µs

1V Transient Response, $5V_{IN}$



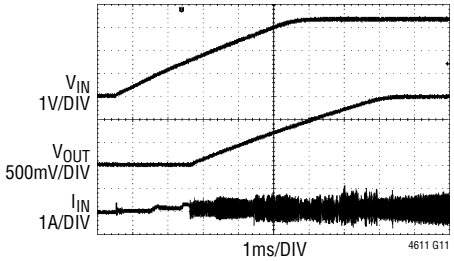
V_{IN} = 5V, V_{OUT} = 1V, USING DIFF AMP
4 × 100µF CERAMIC OUTPUT CAPACITORS
C_{FF} = 47pF, C_P = NONE
7.5A LOAD STEP AT 7.5A/µs

3.3V Transient Response, $5V_{IN}$



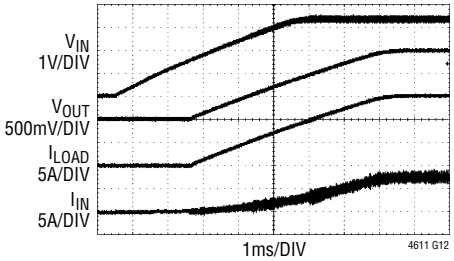
V_{IN} = 5V, V_{OUT} = 3.3V, USING DIFF AMP
2 × 100µF CERAMIC OUTPUT CAPACITORS
C_{FF} = 10pF, C_P = NONE
7.5A LOAD STEP AT 7.5A/µs

Start-Up, No Load



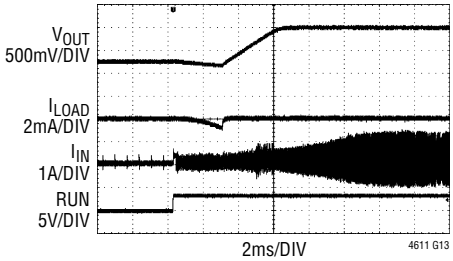
V_{IN} = 3.3V, V_{OUT} = 1.5V, NO LOAD
3 × 22µF CERAMIC INPUT CAPACITORS
C_{SS} = 10nF
4 × 100µF CERAMIC OUTPUT CAPACITORS
C_{FF} = 33pF, C_P = 10pF

Start-Up, 15A Load



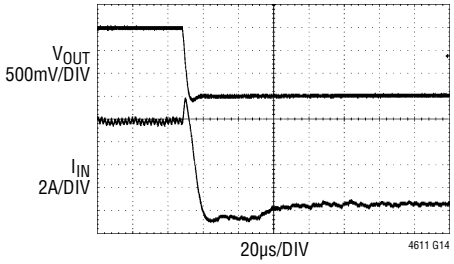
V_{IN} = 3.3V, V_{OUT} = 1.5V, 100mΩ LOAD
3 × 22µF CERAMIC INPUT CAPACITORS
C_{SS} = 10nF
4 × 100µF CERAMIC OUTPUT CAPACITORS
C_{FF} = 33pF, C_P = 10pF

Start-Up, Pre-Bias



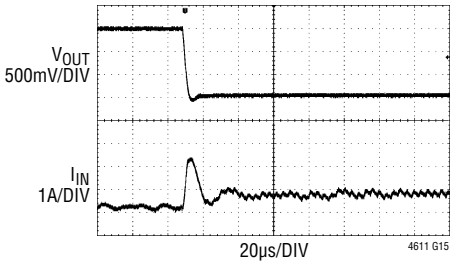
V_{IN} = 3.3V, V_{OUT} = 1.5V, 0.75V PRE-BIAS LOAD
3 × 22µF CERAMIC INPUT CAPACITORS
C_{SS} = 10nF
4 × 100µF CERAMIC OUTPUT CAPACITORS
C_{FF} = 33pF, C_P = 10pF

Short-Circuit, 15A



V_{IN} = 3.3V, V_{OUT} = 1.5V
15A LOAD PRIOR TO SHORT

Short-Circuit, No Load



V_{IN} = 3.3V, V_{OUT} = 1.5V
NO LOAD PRIOR TO SHORT

PIN FUNCTIONS

V_{IN} (A1-A6, B1-B6, C1-C6): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT} (J1-J10, K1-K11, L1-L11, M1-M11): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 5.

GND (B7, B9, C7, C9, D1-D6, D8, E1-E7, E9, F1-F9, G1-G9, H1-H9): Power Ground Pins for Both Input and Output Returns.

PGOOD (F11, G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage exceeds a ±5% regulation window. Both pins are tied together internally.

SGND (G11, H11, H12): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See the layout guidelines in Figure 17.

MODE_PLLIN (A8): Forced Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to GND to force continuous mode operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode operation. Leaving the pin floating will enable Burst Mode operation. A clock on this pin will enable synchronization with forced continuous operation. See the Applications Information section.

PLLFLTR/f_{SET} (B12): Phase-Locked Loop Lowpass Filter for the Internal Phase Detector. LTM4611's default switching frequency is 500kHz. Its switching frequency can be increased by connecting a resistor from this pin to $INTV_{CC}$, or decreased by connecting a resistor from this pin to SGND. See the Applications Information section.

V_{FB} (F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT_LCL} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between the V_{FB} and GND pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details.

TRACK/SS (A9): Output Voltage Tracking Pin and Soft-Start Inputs. The pin has a 1.4µA pull-up current source. A capacitor from this pin to ground will set a soft-start ramp rate. In tracking, the regulator output can be tracked to a different voltage. The different voltage is applied to a voltage divider then the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. Tie all TRACK/SS pins together for parallel operation. See the Applications Information section.

COMP (A11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Tie all COMP pins together for parallel operation. The device is internally compensated.

RUN (A10): Run Control Pin. A voltage above 1.35V will turn on in the module. The V_{IN} undervoltage lockout (UVLO) of the LTM4611 must be set with resistor networks from V_{IN} to RUN and optionally from RUN to GND. Tie all RUN pins together for parallel operation.

$INTV_{CC}$ (A7, D9): Internal 5V LDO for Driving the Control Circuitry and the Power MOSFET Drivers. Both pins are internally connected.

V_{OUT_LCL} (L12): This pin connects to V_{OUT} through a 1M resistor and to V_{FB} with a 60.4k resistor. The remote sense amplifier output $DIFFV_{OUT}$ is connected to V_{OUT_LCL}, and drives the 60.4k top feedback resistor in remote sensing applications. When the remote sense amplifier is used, the $DIFF\_V_{OUT}$ effectively eliminates the 1MΩ from V_{OUT} to V_{OUT_LCL}. When the remote sense amplifier is not used, then connect V_{OUT_LCL} to V_{OUT} directly.

PIN FUNCTIONS

V_{OSNS}^+ (J12) (+): Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.7V$. For $V_{OUT} > 3.7V$, tie V_{OSNS}^+ to GND to rail the output of the remote sense amplifier.

V_{OSNS}^- (M12) (–): Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.7$ V. For $V_{OUT} > 3.7V$, tie V_{OSNS}^- to $INTV_{CC}$ to rail the output of the remote sense amplifier.

$DIFFV_{OUT}$ (K12): Output of the Remote Sense Amplifier. This pin connects to the V_{OUT_LCL} pin for remote sense applications. Otherwise float when not used.

MTP1:A12, MTP2:B11, MTP3:C10, MTP4:C11, MTP5:C12, MTP6:D10, MTP7:D11, MTP8:D12, MTP9:E12: Extra mounting pads used for increased solder integrity strength. Leave electrically open circuit.

BLOCK DIAGRAM

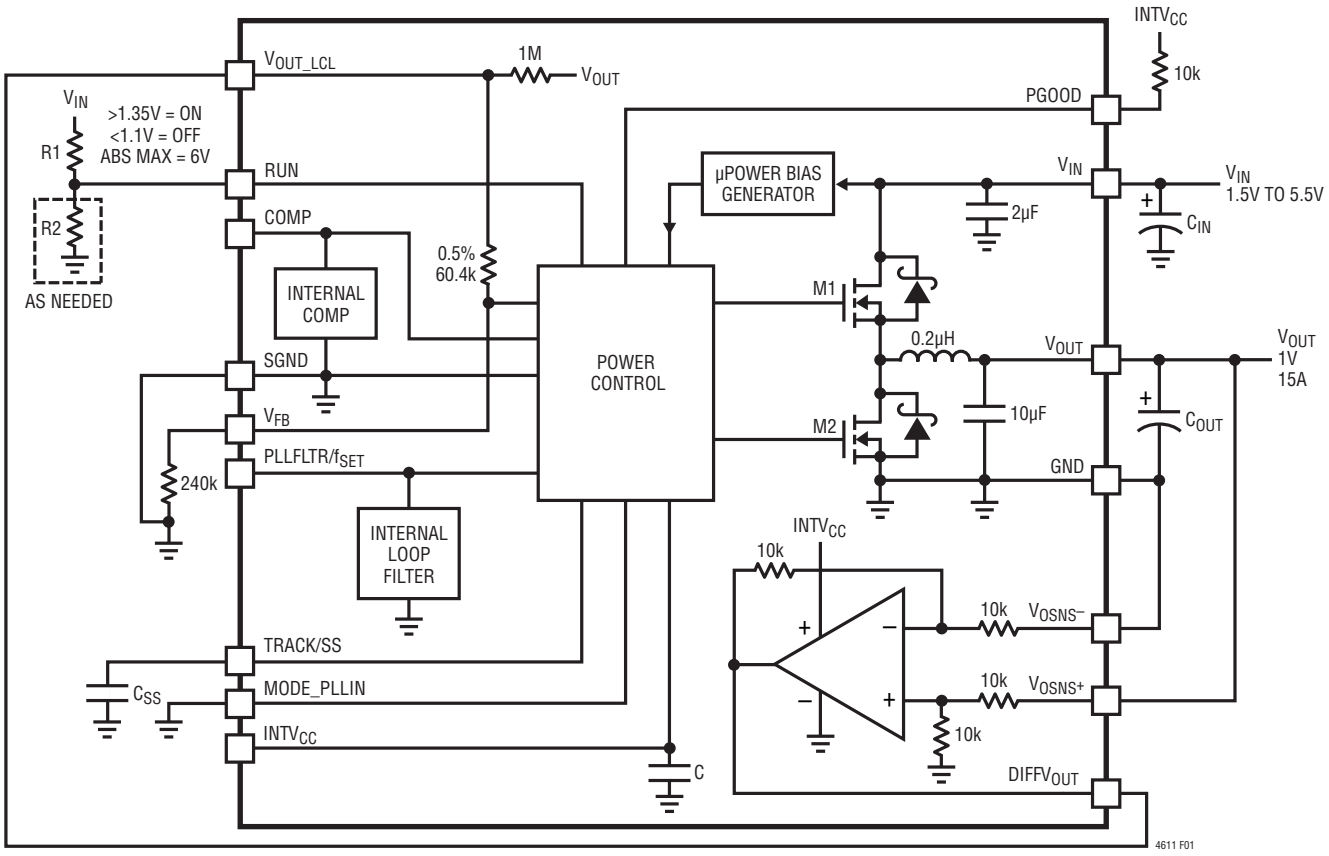


Figure 1. Simplified LTM4611 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 1.5V to 5.5V, V_{OUT} = 1V)	I_{OUT} = 15A			66		μF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 1.5V to 5.5V, V_{OUT} = 1V)	I_{OUT} = 15A			400		μF

OPERATION

Power Module Description

The LTM4611 is a high performance single output standalone nonisolated switching mode DC/DC power supply. It can provide a 15A output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from $0.8V_{DC}$ to $5V_{DC}$ over a 1.5V to 5.5V input range. The typical application schematic is shown in Figure 21.

The LTM4611 has an integrated constant-frequency current mode regulator, power MOSFETs, 0.2µH inductor and other supporting discrete components. The nominal switching frequency range is from 330kHz to 780kHz, and the default operating frequency is 500kHz. For switching noise-sensitive applications, it can be externally synchronized from 360kHz to 710kHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4611 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltage in the event of an overvoltage >7.5%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output is cleared.

Pulling the RUN pin below 1.1V forces the regulator into a shutdown state. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Application Information section.

The LTM4611 is internally compensated to be stable over all operating conditions. Table 5 provides a guideline for input and output capacitances for several operating conditions. The Linear Technology µModule Power Design Tool will be provided for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground.

A remote sense amplifier is provided for accurately sensing output voltages ≤3.7V at the load point.

Multiphase operation can be easily employed with the synchronization inputs using an external clock source. See the Typical Applications.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE_PLLIN pin. These light-load features will accommodate battery operation. Efficiency graphs are provided for light-load operation in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The typical LTM4611 application circuit is shown in Figure 21. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 5 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. The V_{IN} to V_{OUT} minimum dropout is still a function of its load current at very low input voltages. A dropout voltage of 300mV from input to output of LTM4611 is achievable at 15A load, but reflected input voltage ripple and noise should be taken into consideration in such applications. Additionally, the transient-handling capability of the source supply feeding LTM4611 can become an important factor in truly achieving ultralow dropout at high output current. For example, V_{IN} can sag or overshoot dramatically when LTM4611 responds to heavy transient step loads on its output, if insufficient input bypass capacitance is used in combination with a sluggish source supply.

When V_{OUT} is expected to be within 600mV of V_{IN}, or when the caliber of the source supply is in question, it is recommended to evaluate the amount and quality of input bypass capacitance needed to maintain one's target dropout voltage with the source supply that will be used in the end application. Demo Board DC1588A can be used for such evaluation.

At very low duty cycles the minimum specified on-time must be maintained. See the Frequency Adjustment section and temperature derating curves.

To prevent overstress to the µpower bias generator, do not ramp up V_{IN} at a rate exceeding 5V/µs (in practice, it is difficult to violate this guideline.) There is no restriction on how rapidly V_{IN} may be discharged.

Output Voltage Programming

The PWM controller has an internal 0.8V ±1.75% reference voltage over temperature. As shown in the Block Diagram, a 60.4k internal feedback resistor connects the V_{OUT_LCL} and V_{FB} pins together. When the remote sense amplifier is used, then $DIFFV_{OUT}$ is connected to the V_{OUT_LCL} pin. If the remote sense amplifier is not used, then V_{OUT_LCL} connects to V_{OUT}. The output voltage will default to 0.8V with no feedback resistor. Adding a resistor R_{FB} from V_{FB} to GND programs the output voltage:

$$V_{OUT} = 0.8V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}	0.8V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5.0V
R_{FB} (kΩ)	Open	243	121	68.1	47.5	28.0	19.1	11.5

For parallel operation of N LTM4611s, the following equation can be used to solve for R_{FB}:

$$R_{FB} = \frac{60.4k / N}{\frac{V_{OUT}}{0.8V} - 1}$$

Tie the V_{FB} pins together for each parallel output. The COMP, TRACK/SS, V_{OUT_LCL}, and RUN pins must also be tied together as shown in Figures 18 and 19.

For parallel applications, best noise immunity can be achieved by placing capacitors of value C_P from V_{FB} to GND, and value C_{FF} from V_{OUT} to V_{FB}, local to each µModule. If space limitations impede realizing this, then placement of capacitors of value N • C_P from V_{FB} to GND, and value N • C_{FF} from V_{OUT} to the bussed V_{FB} signal, can suffice.

Input Capacitors

The LTM4611 module should be connected to a low AC impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement. Typically 22µF X7R ceramics are a good choice with RMS ripple current ratings of ~2A each. A 100µF to 150µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

APPLICATIONS INFORMATION

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a Polymer capacitor.

Output Capacitors

The LTM4611 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be the low ESR tantalum capacitor, the low ESR Polymer capacitor or ceramic capacitors. The typical output capacitance range is from 200µF to 800µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 7A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 5 matrix, and the Linear Technology µModule Power Design Tool will be provided for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Linear Technology µModule Power Design Tool can calculate the output ripple reduction as the number of implemented phase's increases by N times.

Burst Mode Operation

The LTM4611 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply leave the MODE_PLLIN pin floating. During Burst Mode operation, the peak current of the inductor is set to approximately 33% of the maximum peak current value in normal operation even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In this sleep mode, the internal circuitry is partially turned off, reducing the LTM4611's quiescent current while the load current is supplied by the output capacitors. When the output voltage drops–causing I_{TH} to rise–the internal sleep line goes low and the LTM4611 resumes normal operation. The next oscillator cycle turns on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4611 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be

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enabled by tying the MODE_PLLIN pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the I_{TH} voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4611's output voltage is in regulation.

Multiphase Operation

For outputs that demand more than 15A of load current, multiple LTM4611 devices can be paralleled to provide more output current without increasing input and output voltage ripples. The MODE_PLLIN pin allows the LTM4611 to be synchronized to an external clock (between 360kHz to 710kHz) and the internal phase-locked loop allows the LTM4611 to lock onto input clock phase as well. The PLLFLTR/f_{SET} pin has the onboard loop filter for the PLL. See Figures 18 and 19 for a synchronizing example circuit.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used. See Application Note 77.

The LTM4611 device is an inherently current mode controlled device, so parallel modules will have good current sharing. This will balance the thermals on the design. Tie the COMP, V_{OUT_LCL} and V_{FB} pins of each LTM4611 together to share the current evenly. In addition, tie the respective TRACK/SS and RUN pins of paralleled LTM4611 devices together, to ensure proper start-up and shutdown behavior. Figures 18 and 19 show schematics of LTM4611 devices operating in parallel.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 2).

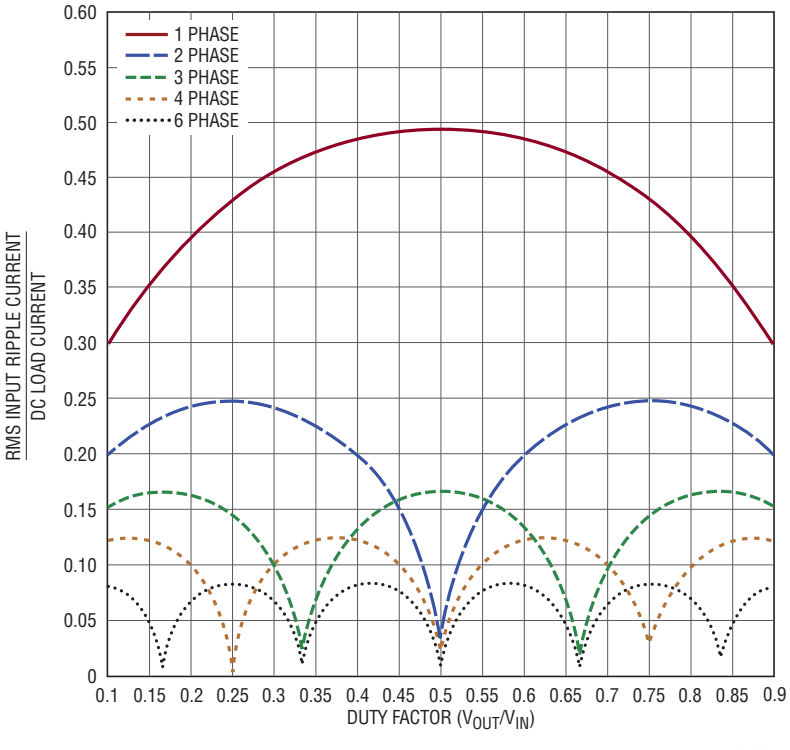

Figure 2. Normalized Input RMS Ripple Current vs Duty Factor for One to Six µModules (Phases)

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PLL, Frequency Adjustment and Synchronization

The default switching frequency of the LTM4611–with PLLFLTR/f_{SET} left floating–is 500kHz, nominally. The PLLFLTR/f_{SET} pin is driven to 1.23V through a high impedance (>350kΩ) network. If desired, a resistor (R_{fSET}) can be connected from the PLLFLTR/f_{SET} pin to $INTV_{CC}$ to increase the switching frequency to as high as 780kHz, nominally. Alternatively, R_{fSET} can instead be connected from PLLFLTR/f_{SET} to signal ground (SGND) to decrease the switching frequency to as low as the minimum specified value of 330kHz, nominally. In practical terms, however, be advised that switching frequencies below 400kHz may be of limited benefit due to the high inductor ripple currents associated with that operating condition. See Figure 3.

There exists a fundamental trade-off between switch mode DC/DC power conversion efficiency and switching frequency: higher operating module switching frequency enables the smallest overall solution size (minimized output capacitance) for a given application; whereas, lower switching frequency enables the highest efficiency for a given application (to the extent that peak and RMS inductor currents can be supported), but requires more output capacitance to maintain comparable output voltage ripple and noise characteristics.

The LTM4611 can be synchronized from 360kHz to 710kHz with an input clock that has a high level above 2V and a low level below 0.6V. Again in practical terms, be advised that switching frequencies below 400kHz may be of limited benefit due to the high inductor ripple currents associated with that operating condition. See the Typical Applications section for synchronization examples. The LTM4611 minimum on-time is limited to 90ns. Guardband the on-time to 130ns. The on-time can be calculated as:

$$t_{ON(MIN)} = \frac{1}{FREQ} \bullet \left(\frac{V_{OUT}}{V_{IN}} \right)$$

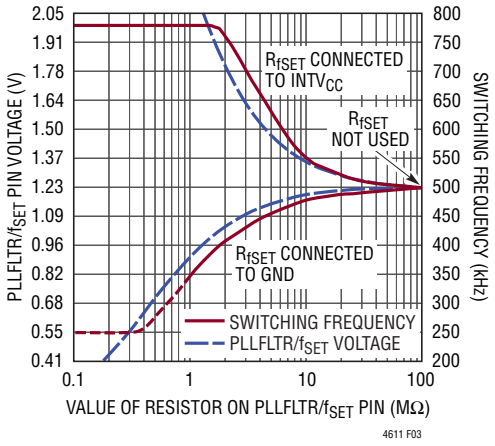

Figure 3. Relationship Between Oscillator Frequency, PLLFLTR/f_{SET} Voltage, and External R_{ISET} Value and Connection

Output Voltage Tracking and Soft-Start Functions

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4611 uses an accurate 60.4k resistor internally for the top feedback resistor. Figure 4 shows an example of coincident tracking.

$$V_{OUT\_SLAVE} = \left(1 + \frac{60.4k}{R_{FB2}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.8V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.8V. R_{TA} in Figure 4 will be equal to the R_{FB2} for coincident tracking.

The TRACK/SS pin of the master can be controlled by an external ramp or the soft-start function of that regulator can be used to develop that master ramp. The LTM4611 can be used as a master by setting the ramp rate on its track pin using a soft-start capacitor. A 1.4µA current source is used to charge the soft-start capacitor. The following equation can be used:

$$t_{SOFTSTART} = 0.8V \bullet \left(\frac{C_{SS}}{1.4\mu A} \right)$$

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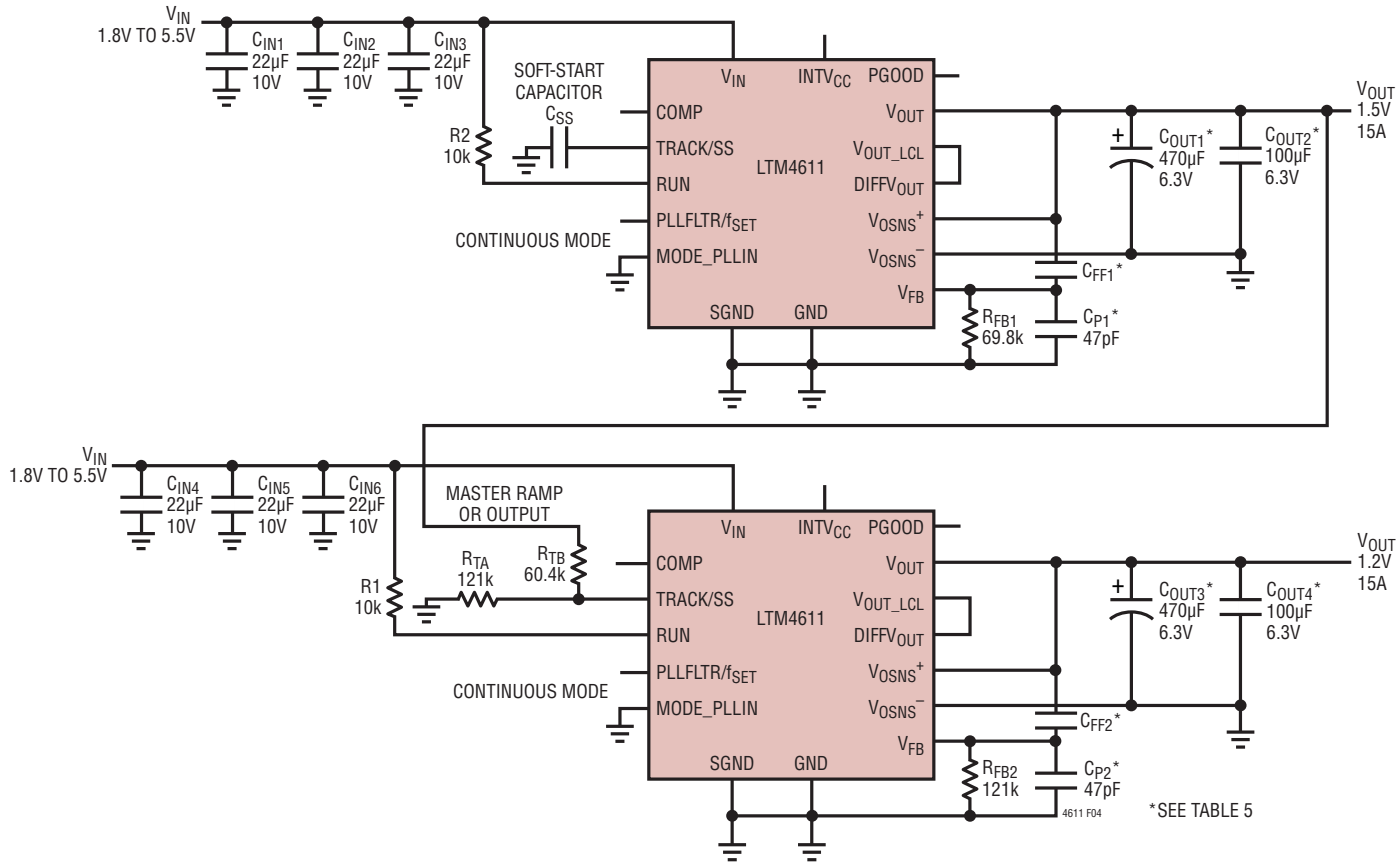

Figure 4. Dual Outputs (1.5V and 1.2V) With Tracking

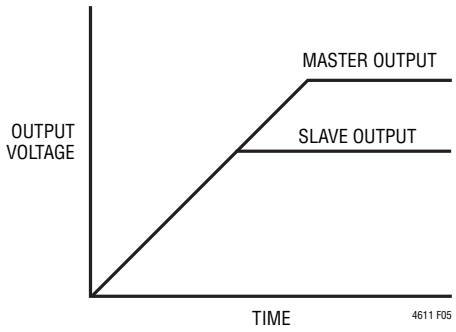

Figure 5. Output Voltage Coincident Tracking

Even for applications that do not require tracking or sequencing, a minimum recommended value for C_{SS} is 10nF (X7R MLCC, 10% tolerance, nominal; X5R material may be substituted if the capacitor temperature will not exceed 85°C), yielding extreme turn-on rise times of 3.8ms minimum to 9.8ms maximum. Tracking a rail in a manner such that TRACK/SS ramps up at a rate faster than 210V/s may also warrant special attention, as explained in the following.

Faster turn-on and tracking rates are achievable, if needed: one need only decrease the default PLLFLTR/f_{SET} RC time constant. Recall that the PLLFLTR/f_{SET} pin is biased to 1.23V via a high impedance source (>350kΩ); also be aware that the internal PLL filter contains an initially discharged 10nF capacitor prior to $INTV_{CC}$ being established.

Requiring the output voltage to power up rapidly without attention to the PLLFLTR/f_{SET} time-constant results in an initial switching frequency of operation that is initially lower than expected (~250kHz)—only during the early stages of start-up—until the PLLFLTR/f_{SET} voltage reaches steady-state value (1.23V by default).

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Decreasing the PLLFLTR/f_{SET} RC time constant can be accomplished, for example, by driving the PLLFLTR/f_{SET} pin with an external, lower impedance resistor divider network from $INTV_{CC}$ and GND to PLLFLTR/f_{SET}—in the simplest of implementations, by shorting PLLFLTR/f_{SET} to $INTV_{CC}$ (thereby programming the switching frequency to 780kHz, nominal), or by driving the PLLFLTR/f_{SET} pin from a low impedance voltage source.

When, in addition to needing faster turn-on time, one is also synchronizing to an external clock signal, one need bear in mind: the PLL's sink and source current is recommended for not more than ±8µA loading, and the PLL will need to successfully drive any external PLLFLTR/f_{SET} network impedance to achieve phase lock; and lastly, some phase shift in clock synchronization will occur as external loading on PLLFLTR/f_{SET} becomes heavier.

To be clear, using a C_{SS} value of 10nF (or higher) eliminates the need for any of the above special considerations or provisions.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK/SS pin. As mentioned above, the TRACK/SS pin has a control range from 0V to 0.8V. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in volts/time. The equation:

$$\frac{MR}{SR} \bullet 60.4k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in volts/time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 60.4k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.8V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB}}{R_{FB2}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.8V. Since R_{TB} is equal to the 60.4k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB2} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 60.4k, and R_{TA} = 121k in Figure 4.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach its final value before the master output.

For example, MR = 1.5V/ms, and SR = 1.2V/ms. Then R_{TB} = 75k. Solve for R_{TA} to equal to 87k.

Beware that without any kind of soft-start ramp up, it is important to provide thorough input filter capacitance to handle input surge currents at start-up, so as to avoid excessive input line sag and power supply *motor boating*. Leaving provision for at least a soft-start capacitor in one's application is strongly recommended.

Overcurrent and Overvoltage Protection

The LTM4611 has overcurrent protection (OCP) in a short circuit. The internal current comparator threshold folds back during a short to reduce the output current. An overvoltage condition (OVP) above 7.5% of the regulated output voltage will force the top MOSFET off and the bottom MOSFET on until the condition is cleared. An input electronic circuit breaker or fuse can be sized to be tripped or cleared when the bottom MOSFET is turned on to protect against the overvoltage. Foldback current limiting is disabled during soft-start or tracking start-up.

Run Enable

The RUN pin is used to enable the power module or sequence the power module. The threshold is 1.22V. The RUN pin must be used as an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin:

$$R2 = \frac{R1}{\frac{V_{UVLO}}{1.22V} - 1}$$

To achieve the lowest possible UVLO, 1.22V, leave R2 unpopulated. R1 can be 10k, or if R2 is unpopulated, R1 may be replaced with a hardwired connection from V_{IN} to RUN.

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See the Block Diagram for the example of use. When RUN is below its threshold, TRACK/SS is pulled low by internal circuity.

$INTV_{CC}$ Regulator

The LTM4611 has an internally regulated bias supply called $INTV_{CC}$. This regulator output has a 4.7µF ceramic capacitor internal. This regulator powers the internal controller and MOSFET drivers. The gate driver current is ~13mA for 500kHz operation and ~20mA for 780kHz operation; the regulator loss is ~40mW and ~60mW, respectively.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 5 is provided for most application requirements. The Linear Technology µModule Power Design Tool will be provided for other control loop optimization.

Thermal Considerations and Output Current Derating

The LTM4611 output current may need to be derated if it is required to operate in a high ambient temperature or deliver a large amount of continuous power. Some factors that influence derating are input voltage, output power, ambient temperature, airflow, and elevation (air density). The power loss curves in Figures 7 to 9 and current derating curves in Figures 10 to 16 can be used as a guide. These curves were generated by an LTM4611 mounted to a 95mm × 76mm 4-layer FR4 printed circuit board (PCB) 1.6mm thick with two ounce copper for the outer layers and one ounce copper for the two inner layers. Boards of other sizes and layer count can exhibit different thermal behavior, so it is ultimately incumbent upon the user to verify proper operation over the intended system's line, load and environmental operating conditions.

The thermal resistance numbers listed in the Pin Configuration section of the data sheet are based on modeling the µModule package mounted on a test board specified per JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The thermal coefficients provided are based on JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

For increased accuracy and fidelity to the actual application, many designers use finite element analysis (FEA) to predict thermal performance. To that end, the Pin Configuration section of the data sheet typically gives four thermal coefficients:

1. θ_{JA}: thermal resistance from junction to ambient.
2. $\theta_{JCbottom}$: thermal resistance from junction to the bottom of the product case.
3. θ_{JCtop}: thermal resistance from junction to top of the product case.
4. θ_{JB}: thermal resistance from junction to the printed circuit board.

While the meaning of each of these coefficients may seem to be intuitive, JEDEC has defined each to avoid confusion and inconsistency. These definitions are given in JESD 51-12, and are quoted or paraphrased in the following:

1. θ_{JA} is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not necessarily reflect an actual application or viable operating condition.
2. $\theta_{JCbottom}$ is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop} is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

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4. θ_{JB} is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

Given these definitions, it should now be apparent that none of these thermal coefficients reflects an actual physical operating condition of a µModule. Thus, none of them can be individually used to accurately predict the thermal performance of the product. Likewise, it would be inappropriate to attempt to use any one coefficient to correlate to the junction temperature versus load graphs given in the product's data sheet. The only appropriate way to use the coefficients is to run a detailed thermal analysis, such as FEA, which considers all of the thermal resistances simultaneously.

A graphical representation of these thermal resistances is given in Figure 6.

The blue resistances are contained within the µModule, and the green are outside.

The die temperature of the LTM4611 must be lower than the maximum rating of 125°C, so care should be taken in the layout of the circuit to ensure good heat sinking of the LTM4611. The bulk of the heat flow out of the LTM4611 is through the bottom of the module and the LGA pads into the printed circuit board. Consequently, a poor printed circuit board design can cause excessive heating, resulting in impaired performance or reliability. Please refer to the PCB Layout section for printed circuit board design suggestions

The 1.2V, 2.5V and 3.3V power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 16 for calculating an approximate θ_{JA} thermal resistance for the LTM4611 with various heat sinking and air flow conditions, as evaluated on the aforementioned 4-layer FR4 PCB. The power loss curves are taken at room temperature, and are increased with multiplicative factors with ambient temperature. These approximate factors are: 1 up to 50°C; 1.1 for 60°C; 1.15 for 70°C; 1.2 for 80°C; 1.25 for 90°C; 1.3 for 100°C; 1.35 for 110°C and 1.4 for 120°C. The derating curves are plotted with the output current starting at 15A and the ambient temperature at 55°C. The output voltages are 1.2V, 2.5V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without air flow, and with and without a heat sink attached with thermally conductive adhesive tape. The BGA heat sinks evaluated in Table 5 yield very comparable performance in laminar airflow despite being visibly different in construction and form factor. The power loss increase with ambient temperature change is factored into the derating

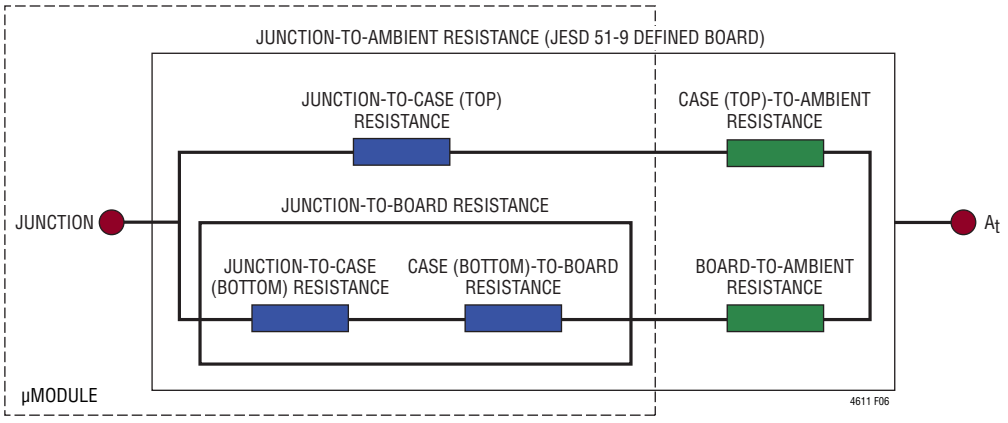

Figure 6

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curves. The junctions are maintained at 115°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 115°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 11, the load current is derated to ~12A at ~75°C with no air or heat sink and the power loss for the 3.3V to 1.2V at 12A output is a 2.82W loss. The 2.82W loss is calculated with the ~2.4W room temperature loss from the 3.3V to 1.2V power loss curve at 12A (Figure 7), and the 1.175 multiplying factor at 75°C ambient. If the 75°C ambient temperature is subtracted from the 115°C junction temperature, then the difference of 40°C divided by 2.82W yields a thermal resistance, θ_{JA}, of 14.2°C/W—in good agreement with Table 2. Tables 2, 3 and 4 provide equivalent thermal resistances for 1.2V, 2.5V and 3.3V outputs with and without air flow and heat sinking. The derived thermal resistances in Tables 2, 3 and 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors.

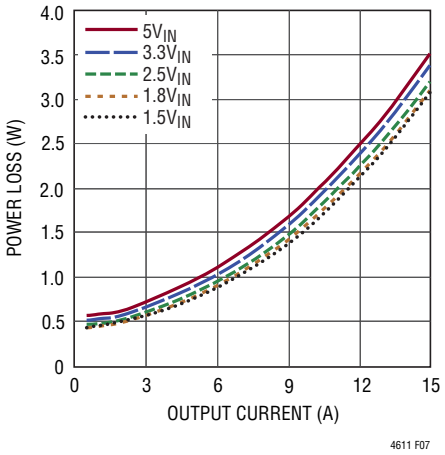

Figure 7. 1.2V_{OUT} Power Loss

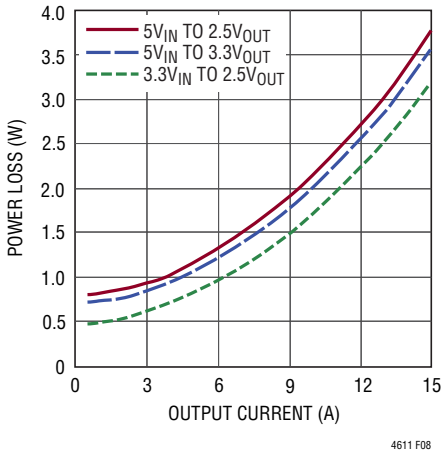

Figure 8. 2.5V_{OUT} and 3.3V_{OUT} Power Loss

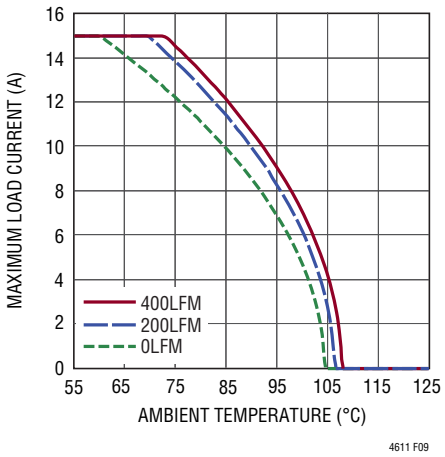

Figure 9. 5V_{IN} to 1.2V_{OUT} No Heat Sink

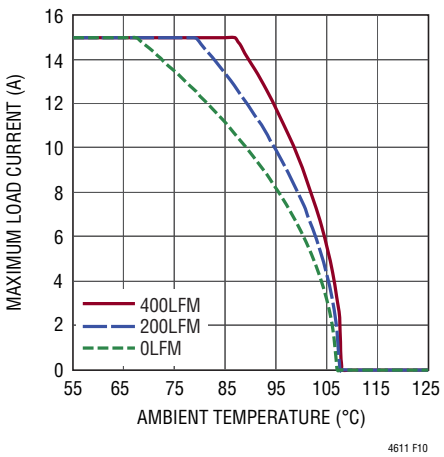

Figure 10. 5V_{IN} to 1.2V_{OUT} with Heat Sink

APPLICATIONS INFORMATION

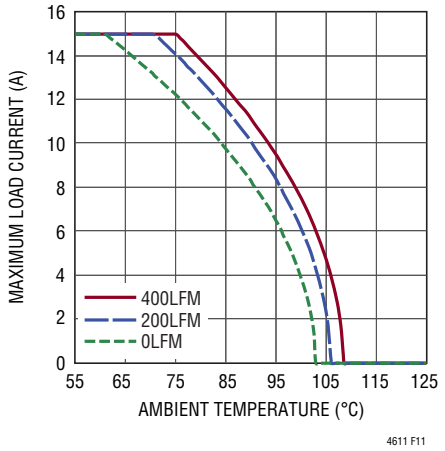

Figure 11. $3.3V_{IN}$ to $1.2V_{OUT}$ No Heat Sink

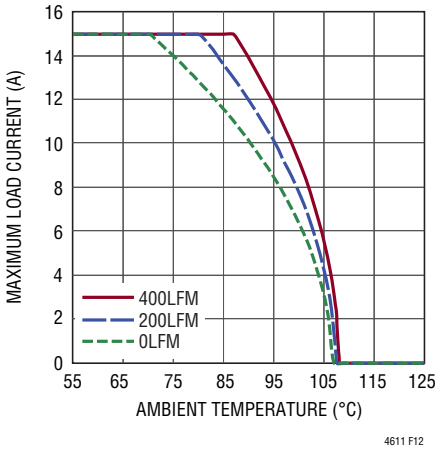

Figure 12. $3.3V_{IN}$ to $1.2V_{OUT}$ with Heat Sink

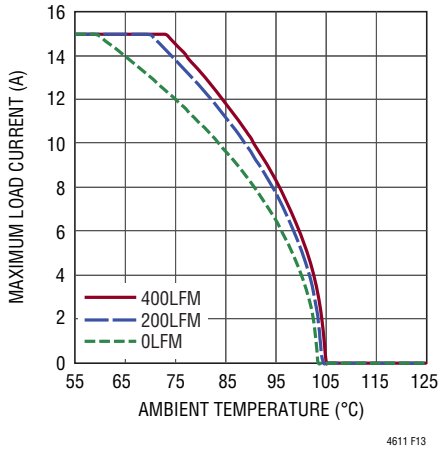

Figure 13. $3.3V_{IN}$ to $2.5V_{OUT}$ No Heat Sink

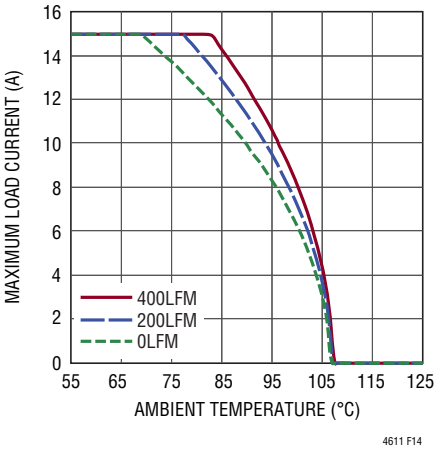

Figure 14. $3.3V_{IN}$ to $2.5V_{OUT}$ with Heat Sink

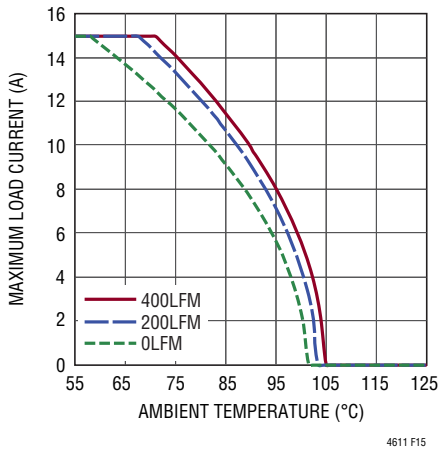

Figure 15. $5V_{IN}$ to $3.3V_{OUT}$ No Heat Sink

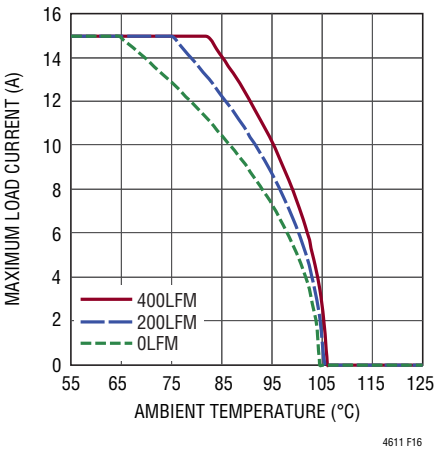

Figure 16. $5V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

APPLICATIONS INFORMATION

Table 2. 1.2V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 9, 11	5V, 3.3V	Figure 7	0	None	14
Figures 9, 11	5V, 3.3V	Figure 7	200	None	11.5
Figures 9, 11	5V, 3.3V	Figure 7	400	None	10.6
Figures 10, 12	5V, 3.3V	Figure 7	0	BGA Heat Sink	11.5
Figures 10, 12	5V, 3.3V	Figure 7	200	BGA Heat Sink	8.4
Figures 10, 12	5V, 3.3V	Figure 7	400	BGA Heat Sink	7.5

Table 3. 2.5V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 13	3.3V	Figure 8	0	None	15.5
Figures 13	3.3V	Figure 8	200	None	12.7
Figures 13	3.3V	Figure 8	400	None	12.1
Figures 14	3.3V	Figure 8	0	BGA Heat Sink	12.6
Figures 14	3.3V	Figure 8	200	BGA Heat Sink	10.6
Figures 14	3.3V	Figure 8	400	BGA Heat Sink	8.9

Table 4. 3.3V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 15	5V	Figure 8	0	None	14
Figures 15	5V	Figure 8	200	None	11.5
Figures 15	5V	Figure 8	400	None	10.2
Figures 16	5V	Figure 8	0	BGA Heat Sink	12
Figures 16	5V	Figure 8	200	BGA Heat Sink	10.1
Figures 16	5V	Figure 8	400	BGA Heat Sink	9.3

APPLICATIONS INFORMATION

Table 5. Output Voltage Response Versus Component Matrix, 0A to 7.5A Load Step

TYPICAL MEASURED VALUES

C_{OUT1} VENDORS	PART NUMBER	C_{OUT2} VENDORS	PART NUMBER
AVX	12106D107MAT2A (100µF, 6.3V, 1210 Case Size)	Sanyo POSCAP	6TPF330M9L (330µF, 6.3V, 9mΩ ESR, D3L Case Size)
Taiyo Yuden	JMK325BJ107MM-T (100µF, 6.3V, 1210 Case Size)	Sanyo POSCAP	2R5TPE470M9 (470µF, 2.5V, 9mΩ ESR, D2E Case Size)
TDK	C3225X5R0J107MT (100µF, 6.3V, 1210 Case Size)		
AVX	1206D226MAT (22µF, 6.3V, 1206 Case Size)		
Taiyo Yuden	JMK316BJ226ML-T (22µF, 6.3V, 1206 Case Size)		
TDK	C3216X5R0J226MT (22µF, 6.3V, 1206 Case Size)		

V_{OUT} (V)	V_{IN} (V)	C_{IN}* (CERAMIC)	C_{IN}* (BULK)	C_{OUT2} (CERAMIC)	C_{OUT1} (BULK)	C_{FF}	C_P	USING DIFF AMP	FIGURE	TRANSIENT DROOP, 0A TO 7.5A LOAD STEP (mV)	TRANSIENT PEAK-TO-PEAK, 0A TO 7.5A TO 0A (mV_{P-P})	RECOVERY TIME (µs)	LOAD STEP SLEW RATE (A/µs)	R_{SET} (kΩ)
0.9	1.5	2 × 47µF	470µF	5 × 100µF	None	220pF	None	Y	21	65	118	15	7.5	481
0.9	1.5	2 × 47µF	470µF	3 × 22µF	470µF	22pF	None	Y	21	63	122	25	7.5	481
0.9	1.8	2 × 47µF	220µF	4 × 100µF	None	220pF	None	Y	21	65	119	20	7.5	481
0.9	1.8	2 × 47µF	220µF	3 × 22µF	470µF	47pF	None	Y	21	60	113	25	7.5	481
0.9	1.8	2 × 47µF	220µF	4 × 22µF	330µF	22pF	None	Y	21	64	119	30	7.5	481
0.9	2.5	2 × 47µF	150µF	5 × 100µF	None	33pF	10pF	Y	21	54	108	20	7.5	481
0.9	2.5	2 × 47µF	150µF	7 × 22µF	330µF	None	22pF	Y	21	65	123	20	7.5	481
0.9	3.3	2 × 47µF	150µF	4 × 100µF	None	47pF	None	Y	21	50	104	25	7.5	481
0.9	3.3	2 × 47µF	150µF	7 × 22µF	330µF	10pF	10pF	Y	21	55	109	20	7.5	481
0.9	5	2 × 47µF	150µF	4 × 100µF	None	47pF	None	Y	21	47	102	20	7.5	481
0.9	5	2 × 47µF	150µF	6 × 22µF	330µF	10pF	10pF	Y	21	61	116	20	7.5	481
1	1.5	2 × 47µF	680µF	5 × 100µF	None	220pF	None	Y	21	70	128	20	7.5	243
1	1.5	2 × 47µF	680µF	3 × 22µF	470µF	33pF	None	Y	21	62	121	25	7.5	243
1	1.8	2 × 47µF	330µF	4 × 100µF	None	220pF	None	Y	21	68	123	20	7.5	243
1	1.8	2 × 47µF	330µF	3 × 22µF	470µF	33pF	None	Y	21	60	115	30	7.5	243
1	1.8	2 × 47µF	330µF	4 × 22µF	330µF	22pF	None	Y	21	66	123	30	7.5	243
1	2.5	2 × 47µF	150µF	4 × 100µF	None	47pF	None	Y	21	61	115	25	7.5	243
1	2.5	2 × 47µF	150µF	7 × 22µF	330µF	10pF	10pF	Y	21	63	115	25	7.5	243
1	3.3	2 × 47µF	150µF	4 × 100µF	None	47pF	None	Y	21	52	106	30	7.5	243
1	3.3	2 × 47µF	150µF	7 × 22µF	330µF	10pF	10pF	Y	21	57	111	20	7.5	243
1	5	2 × 47µF	150µF	4 × 100µF	None	47pF	None	Y	21	53	108	25	7.5	243
1	5	2 × 47µF	150µF	6 × 22µF	330µF	10pF	10pF	Y	21	62	119	25	7.5	243
1.2	1.5	2 × 47µF	1000µF	6 × 100µF	None	220pF	None	Y	21	82	145	20	7.5	121
1.2	1.5	2 × 47µF	1000µF	2 × 22µF	470µF	47pF	None	Y	21	70	133	30	7.5	121
1.2	1.8	2 × 47µF	470µF	4 × 100µF	None	220pF	None	Y	21	75	136	25	7.5	121
1.2	1.8	2 × 47µF	470µF	3 × 22µF	470µF	22pF	None	Y	21	64	126	30	7.5	121
1.2	1.8	2 × 47µF	470µF	4 × 22µF	330µF	22pF	None	Y	21	72	137	30	7.5	121
1.2	2.5	2 × 47µF	220µF	4 × 100µF	None	100pF	None	Y	21	58	114	30	7.5	121
1.2	2.5	2 × 47µF	220µF	5 × 22µF	330µF	10pF	10pF	Y	21	65	122	25	7.5	121
1.2	3.3	2 × 47µF	150µF	4 x 100µF	None	33pF	10pF	Y	21	60	116	30	7.5	121
1.2	3.3	2 × 47µF	150µF	7 × 22µF	330µF	10pF	10pF	Y	21	63	117	20	7.5	121
1.2	5	2 × 47µF	150µF	4 × 100µF	None	47pF	None	Y	21	47	105	30	7.5	121

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V_{OUT} (V)	V_{IN} (V)	C_{IN}* (CERAMIC)	C_{IN}* (BULK)	C_{OUT2} (CERAMIC)	C_{OUT1} (BULK)	C_{FF}	C_P	USING DIFF AMP	FIGURE	TRANSIENT DROOP, 0A TO 7.5A LOAD STEP (mV)	TRANSIENT PEAK-TO-PEAK, 0A TO 7.5A TO 0A (mV_{P-P})	RECOVERY TIME (µs)	LOAD STEP SLEW RATE (A/µs)	R_{SET} (kΩ)
1.2	5	2 × 47µF	150µF	6 × 22µF	330µF	10pF	10pF	Y	21	64	123	25	7.5	121
1.5	1.8	2 × 47µF	1000µF	6 × 100µF	None	220pF	None	Y	21	83	147	25	7.5	69
1.5	1.8	2 × 47µF	1000µF	2 × 22µF	470µF	47pF	None	Y	21	71	135	40	7.5	69
1.5	2.5	2 × 47µF	220µF	4 × 100µF	None	220pF	None	Y	21	64	122	40	7.5	69
1.5	2.5	2 × 47µF	220µF	5 × 22µF	330µF	22pF	10pF	Y	21	68	133	30	7.5	69
1.5	3.3	2 × 47µF	150µF	4 × 100µF	None	33pF	10pF	Y	21	66	123	30	7.5	69
1.5	3.3	2 × 47µF	150µF	4 × 22µF	330µF	22pF	None	Y	21	67	124	30	7.5	69
1.5	5	2 × 47µF	150µF	4 × 100µF	None	33pF	10pF	Y	21	59	122	30	7.5	69
1.5	5	2 × 47µF	150µF	6 × 22µF	330µF	None	10pF	Y	21	67	131	30	7.5	69
1.8	2.5	2 × 47µF	330µF	4 × 100µF	None	220pF	None	Y	21	73	137	45	7.5	48.1
1.8	2.5	2 × 47µF	330µF	5 × 22µF	330µF	22pF	None	Y	21	76	145	35	7.5	48.1
1.8	3.3	2 × 47µF	150µF	4 × 100µF	None	47pF	10pF	Y	21	57	118	40	7.5	48.1
1.8	3.3	2 × 47µF	150µF	4 × 22µF	330µF	22pF	None	Y	21	69	137	30	7.5	48.1
1.8	5	2 × 47µF	150µF	4 × 100µF	None	33pF	10pF	Y	21	64	127	40	7.5	48.1
1.8	5	2 × 47µF	150µF	6 × 22µF	330µF	None	10pF	Y	21	69	133	30	7.5	48.1
2.5	3.3	2 × 47µF	330µF	3 × 100µF	None	100pF	None	Y	21	71	143	45	7.5	28.4
2.5	3.3	2 × 47µF	330µF	4 × 100µF	None	100pF	None	Y	21	66	123	40	7.5	28.4
2.5	3.3	2 × 47µF	330µF	3 × 22µF	330µF	47pF	None	Y	21	67	128	50	7.5	28.4
2.5	5	2 × 47µF	150µF	3 × 100µF	None	100pF	None	Y	21	60	134	45	7.5	28.4
2.5	5	2 × 47µF	150µF	4 × 100µF	None	100pF	None	Y	21	54	115	50	7.5	28.4
2.5	5	2 × 47µF	150µF	5 × 22µF	330µF	22pF	None	Y	21	81	160	40	7.5	28.4
3.3	5	2 × 47µF	150µF	2 × 100µF	None	22pF	None	Y	21	137	274	40	7.5	19.3
3.3	5	2 × 47µF	150µF	3 × 100µF	None	47pF	None	Y	21	67	143	50	7.5	19.3
3.3	5	2 × 47µF	150µF	4 × 100µF	None	100pF	None	Y	21	56	119	60	7.5	19.3
3.3	5	2 × 47µF	150µF	5 × 22µF	330µF	22pF	None	Y	21	95	193	45	7.5	19.3
5	5.5	2 × 47µF	680µF	1 × 100µF	None	10pF	None	N	20	264	511	30	7.5	11.5
5	5.5	2 × 47µF	680µF	7 × 22µF	None	None	None	N	20	218	431	40	7.5	11.5

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
Wakefield Engineering	LTN20069	www.wakefield.com
AAVID Thermalloy	375424B00034G	www.aavidthermalloy.com

THERMALLY CONDUCTIVE ADHESIVE TAPE MANUFACTURER	PART NUMBER	WEBSITE
Chromerics	T411	www.chromerics.com

*The quantity and quality of bulk input bypass capacitance needed, particularly for low dropout scenarios ($V_{IN} - V_{OUT}$ < 600mV) is mainly dependent on the output impedance and dynamic response of the power source feeding the LTM4611(s). Consider, in the extreme: for a heavy load step, the full transient on LTM4611's output is directly referred to its input, and the LTM4611 can only deliver to its output whatever the source supply and local input caps can provide. Sluggish source supplies will call for more bulk capacitance placed locally to the LTM4611's input, to assist the source supply in riding through severe transient load steps.

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Safety Considerations

The LTM4611 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support overvoltage protection and overcurrent protection.

Layout Checklist/Example

The high integration of LTM4611 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the respective COMP, V_{FB}, V_{OUT_LCL}, TRACK/SS and RUN pins together. Use an internal layer to closely connect these pins together. Figure 17 gives a good example of the recommended layout. Figures 18 and 19 show schematics of the LTM4611 devices operating in parallel.
- To facilitate stuffing verification, test and debug activities, consider routing control signals of the LTM4611 with short traces to localized test points, test pads or test vias–as PCB layout space permits. Both in-house and contract manufacturers enjoy gaining electrical access to all non low impedance (>10Ω) pins of an IC or µModule device to improve in-circuit test (ICT) coverage.

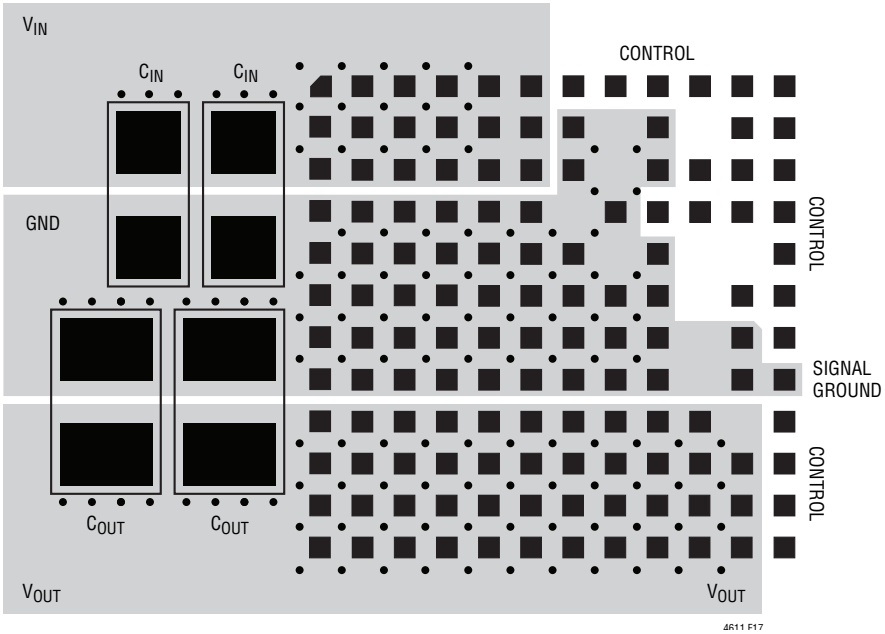


Figure 17. Recommended PCB Layouts

TYPICAL APPLICATIONS

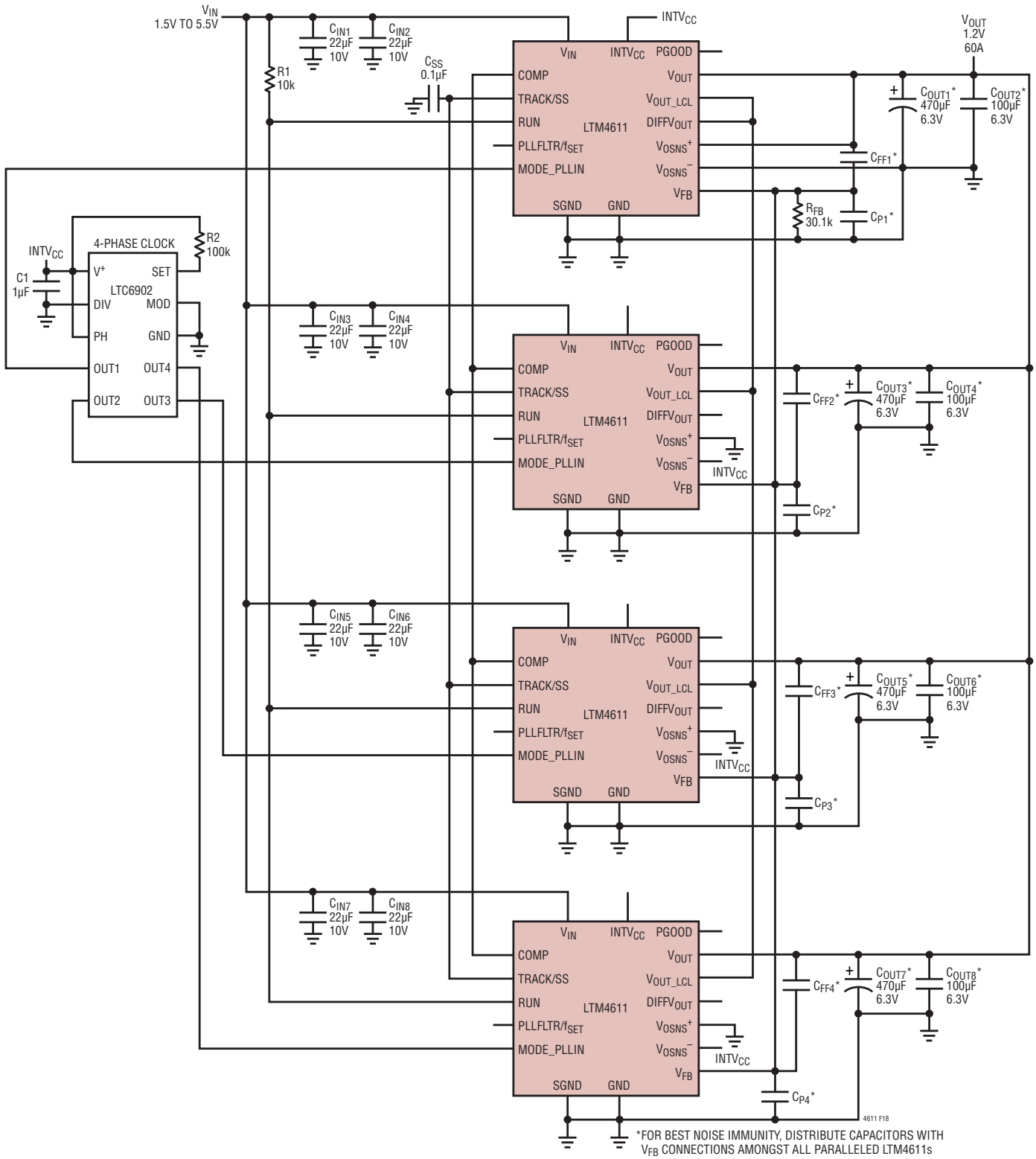


Figure 18. 1.2V, 60A, Current Sharing with 4-Phase Operation

TYPICAL APPLICATIONS

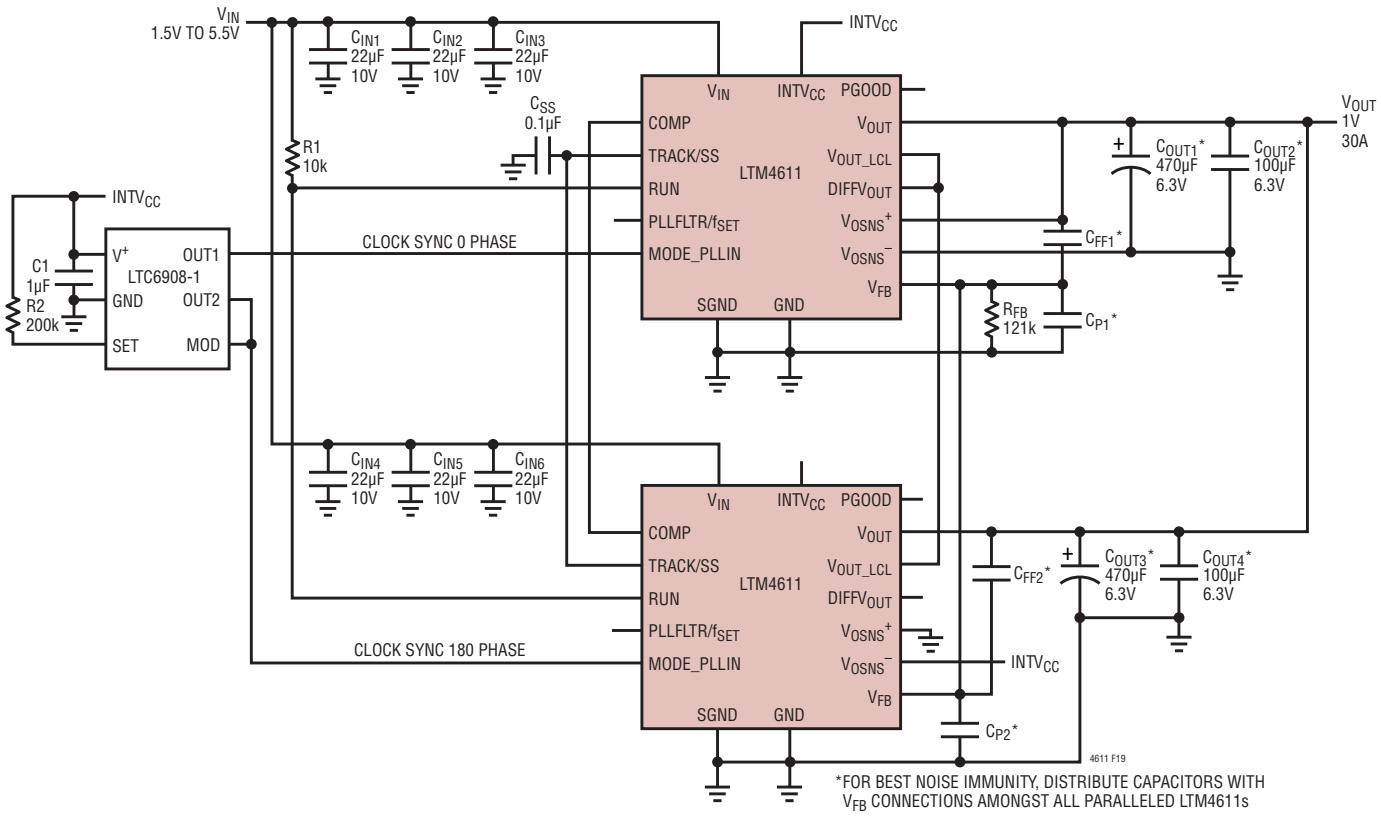


Figure 19. 1V at 30A LTM4611 Two Parallel Outputs with 2-Phase Operation

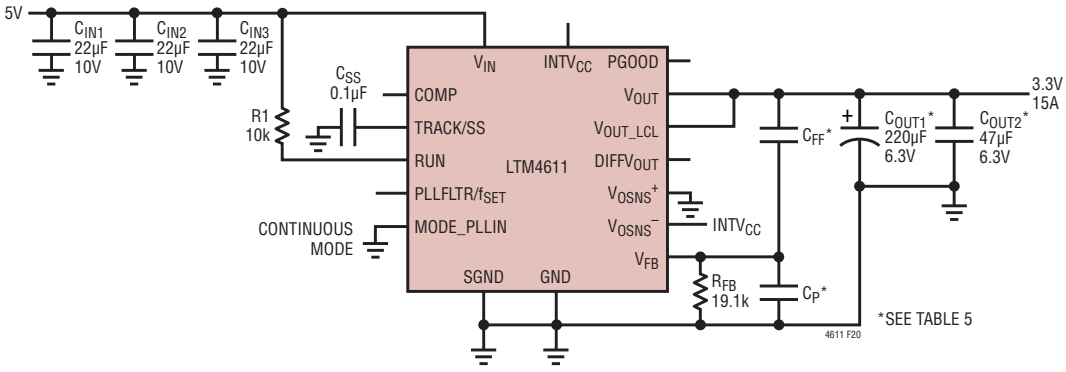
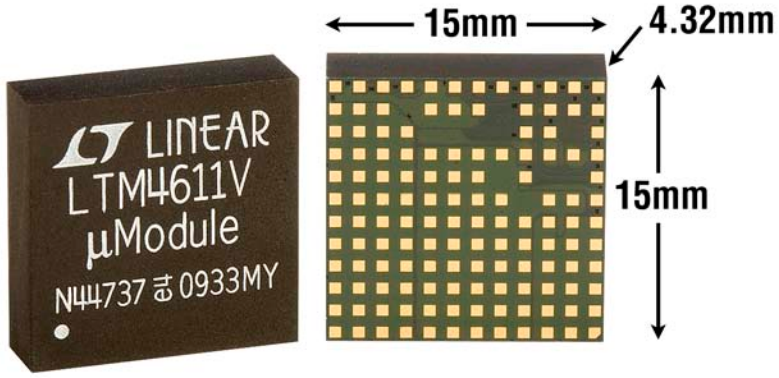


Figure 20. 3.3V at 15A Design, Example of Not Using Differential Remote Sense

PACKAGE PHOTOGRAPH



PACKAGE DESCRIPTION

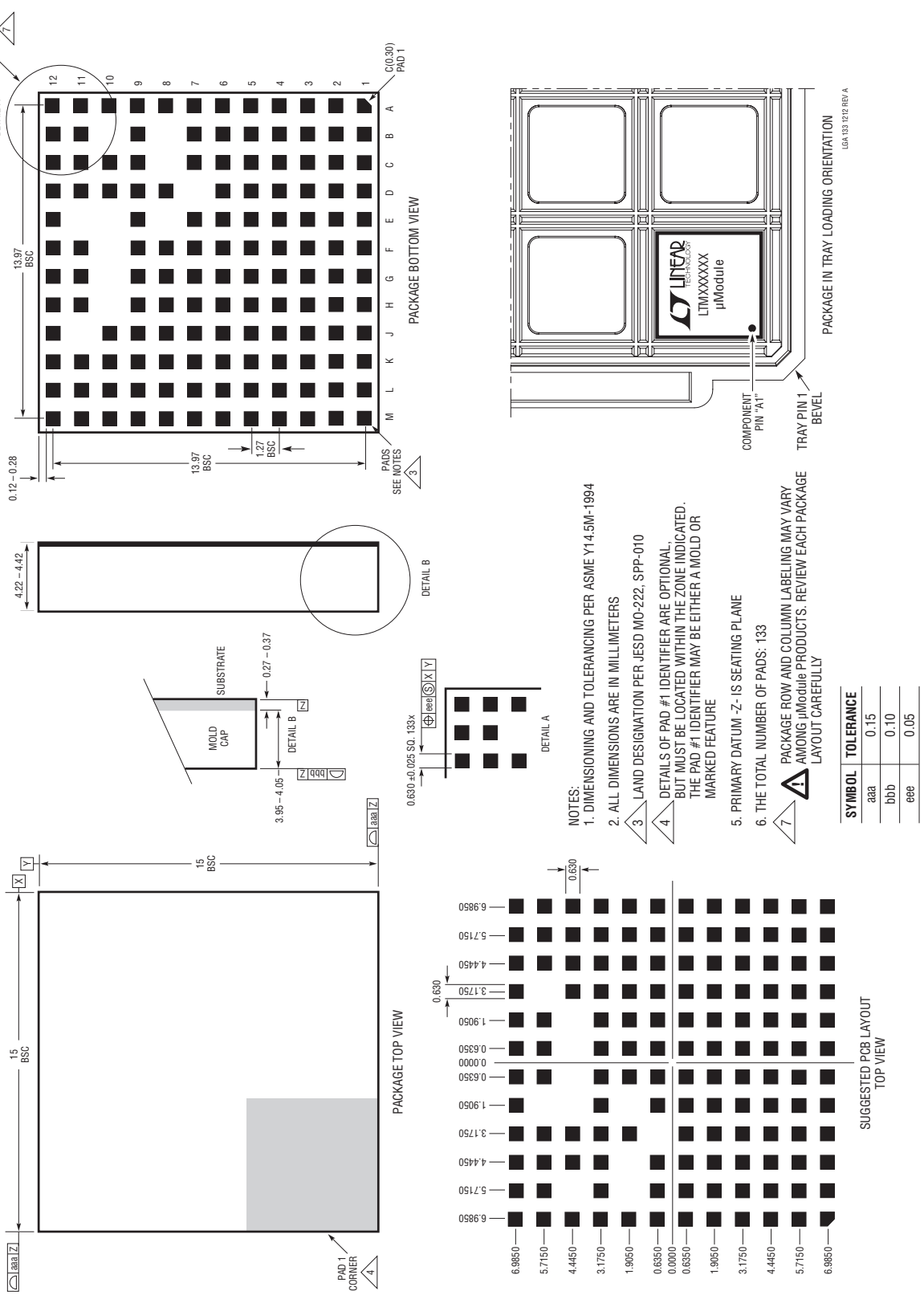
Pin Assignment Table
(Arranged by Pin Number)

PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME	
A1	V_{IN}	B1	V_{IN}	C1	V_{IN}	D1	GND	E1	GND	F1	GND
A2	V_{IN}	B2	V_{IN}	C2	V_{IN}	D2	GND	E2	GND	F2	GND
A3	V_{IN}	B3	V_{IN}	C3	V_{IN}	D3	GND	E3	GND	F3	GND
A4	V_{IN}	B4	V_{IN}	C4	V_{IN}	D4	GND	E4	GND	F4	GND
A5	V_{IN}	B5	V_{IN}	C5	V_{IN}	D5	GND	E5	GND	F5	GND
A6	V_{IN}	B6	V_{IN}	C6	V_{IN}	D6	GND	E6	GND	F6	GND
A7	$INTV_{CC}$	B7	GND	C7	GND	D7	-	E7	GND	F7	GND
A8	MODE_PLLIN	B8	-	C8	-	D8	GND	E8	-	F8	GND
A9	TRACK/SS	B9	GND	C9	GND	D9	$INTV_{CC}$	E9	GND	F9	GND
A10	RUN	B10	-	C10	MTP3	D10	MTP6	E10	-	F10	-
A11	COMP	B11	MTP2	C11	MTP4	D11	MTP7	E11	-	F11	PGOOD
A12	MTP1	B12	$PLLFLTR/f_{SET}$	C12	MTP5	D12	MTP8	E12	MTP9	F12	V_{FB}

PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME	
G1	GND	H1	GND	J1	V_{OUT}	K1	V_{OUT}	L1	V_{OUT}	M1	V_{OUT}
G2	GND	H2	GND	J2	V_{OUT}	K2	V_{OUT}	L2	V_{OUT}	M2	V_{OUT}
G3	GND	H3	GND	J3	V_{OUT}	K3	V_{OUT}	L3	V_{OUT}	M3	V_{OUT}
G4	GND	H4	GND	J4	V_{OUT}	K4	V_{OUT}	L4	V_{OUT}	M4	V_{OUT}
G5	GND	H5	GND	J5	V_{OUT}	K5	V_{OUT}	L5	V_{OUT}	M5	V_{OUT}
G6	GND	H6	GND	J6	V_{OUT}	K6	V_{OUT}	L6	V_{OUT}	M6	V_{OUT}
G7	GND	H7	GND	J7	V_{OUT}	K7	V_{OUT}	L7	V_{OUT}	M7	V_{OUT}
G8	GND	H8	GND	J8	V_{OUT}	K8	V_{OUT}	L8	V_{OUT}	M8	V_{OUT}
G9	GND	H9	GND	J9	V_{OUT}	K9	V_{OUT}	L9	V_{OUT}	M9	V_{OUT}
G10	-	H10	-	J10	V_{OUT}	K10	V_{OUT}	L10	V_{OUT}	M10	V_{OUT}
G11	SGND	H11	SGND	J11	-	K11	V_{OUT}	L11	V_{OUT}	M11	V_{OUT}
G12	PGOOD	H12	SGND	J12	V_{OSNS^+}	K12	$DIFFV_{OUT}$	L12	V_{OUT_LCL}	M12	V_{OSNS^-}

PACKAGE DESCRIPTION

LGA Package
133-Lead (15mm × 15mm × 4.32mm)
(Reference LTC DWG # 05-08-1777 Rev A)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 133
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/11	Added Video TechClip Link	1
B	5/13	Added new video icon.	1

TYPICAL APPLICATION

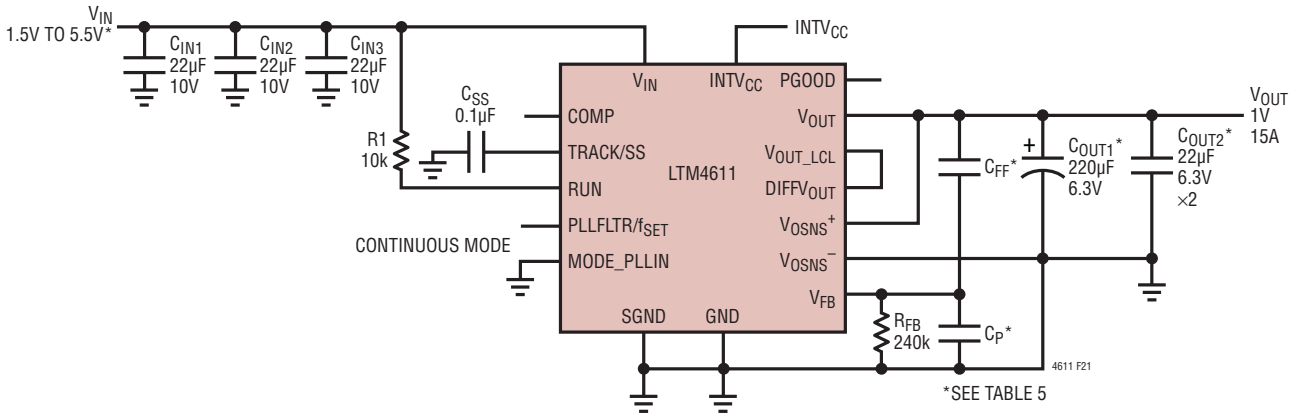


Figure 21. 1.5V to 5.5V_{IN}, 1V at 15A Design

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4600	10A DC/DC µModule	Basic 10A DC/DC µModule
LTM4601A	12A DC/DC µModule with PLL, Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation to 48A, Pin Compatible with the LTM4611 and LTM4617
LTM4602	6A DC/DC µModule	Pin Compatible with the LTM4600
LTM4603	6A DC/DC µModule with PLL and Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version has no Remote Sensing, Pin Compatible with the LTM4601
LTM4604A	4A Low Voltage DC/DC µModule	2.375V ≤ V_{IN} ≤ 5.5V; 0.8V ≤ V_{OUT} ≤ 5V, 9mm × 15mm × 2.3mm (Ultrathin) LGA Package
LTM4605	Buck-Boost DC/DC µModule Family	All Pin Compatible; Up to 5A; Up to 36V_{IN}, 34V_{OUT} 15mm × 15mm × 2.8mm
LTM4606	Ultralow Noise 6A DC/DC µModule	4.5V ≤ V_{IN} ≤ 28V, 0.6V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 2.8mm Package
LTM4607	Buck-Boost DC/DC µModule Family	All Pin Compatible; Up to 5A; Up to 36V_{IN}, 34V_{OUT} 15mm × 15mm × 2.8mm
LTM4608A	8A Low Voltage DC/DC µModule	2.7V ≤ V_{IN} ≤ 5.5V; 0.6V ≤ V_{OUT} ≤ 5V; 9mm × 15mm × 2.8mm LGA Package
LTM4609	Buck-Boost DC/DC µModule Family	All Pin Compatible; Up to 5A; Up to 36V_{IN}, 34V_{OUT} 15mm × 15mm × 2.8mm
LTM4612	Ultralow Noise High V_{OUT} DC/DC µModule	5A, 5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, 15mm × 15mm × 2.8mm Package
LTM8023	36V, 2A DC/DC µModule	3.6V ≤ V_{IN} ≤ 36V, 0.8V ≤ V_{OUT} ≤ 10V, 9mm × 11.25mm × 2.8mm Package
LTM8032	Ultralow Noise 36V, 2A DC/DC µModule	EN55022 Class B Compliant; 0.8V ≤ V_{OUT} ≤ 10V; 3.6V ≤ V_{IN} ≤ 36V; 9mm × 15mm × 2.8mm

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