# High Efficiency Buck + VLDO Regulator

## FEATURES

- **High Efficiency, 500mA Buck Plus 300mA VLDO™ Regulator**
  - **Auto Start-Up Powers VLDO/Linear Regulator Output Prior to Buck Regulator Output**
- **Independent High Efficiency, 500mA Buck ($V_{IN}$: 2.7V to 5.5V)**
- **300mA VLDO Regulator with 30mA Standalone Mode**
- **No External Schottky Diodes Required**
- **Buck Output Voltage Range: 0.8V to 5V**
- **VLDO Input Voltage Range ($LV_{IN}$): 0.9V to 5.5V**
- **VLDO Output Voltage Range VLDO: 0.4V to 4.1V**
- Selectable Fixed Frequency, Pulse-Skip Operation or
- Burst Mode® Operation
- Short-Circuit Protected
- Current Mode Operation for Excellent Line and Load Transient Response
- Constant Frequency Operation: 2.25MHz
- Low Dropout Buck Operation: 100% Duty Cycle
- Small, Thermally Enhanced, 10-Lead (3mm × 3mm) DFN Package

## APPLICATIONS

- PDAs/Palmtop PCs
- Digital Cameras
- Cellular Phones
- PC Cards
- Wireless and DSL Modems
- Other Portable Power Systems

## DESCRIPTION

The LTC®3541-1 combines a synchronous buck DC/DC converter with a very low dropout linear regulator (VLDO) to provide up to two output voltages from a single input voltage with minimal external components. When configured for dual output operation, the LTC3541-1's auto start-up feature will bring the VLDO/linear regulator output into regulation in a controlled manner prior to enabling the Buck regulator output without the need for external pin control. Buck output prior to VLDO/linear regulator output sequencing may also be obtained via external pin control. The input voltage range is ideally suited for Li-Ion battery-powered applications, as well as powering sub-3.3V logic from 5V or 3.3V rails.

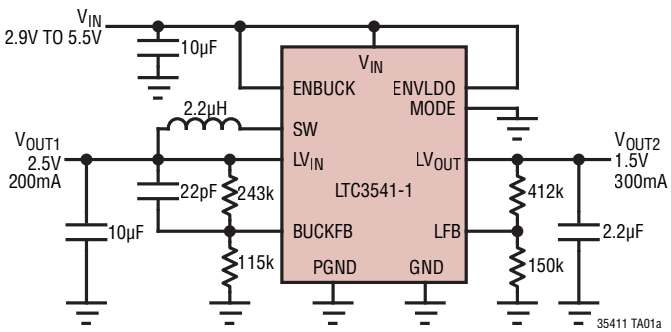
The synchronous buck converter provides a high efficiency output, typically 90%, capable of providing up to 500mA of continuous output current while switching at 2.25MHz, allowing the use of small surface mount inductors and capacitors. A mode-select pin allows Burst Mode operation to be enabled for higher efficiency at light load currents, or disabled for lower noise, constant frequency operation.

The VLDO regulator provides a low noise, low voltage output capable of providing up to 300mA of continuous output current using only a 2.2µF ceramic capacitor. The input supply voltage of the VLDO regulator ($LV_{IN}$) may come from the buck regulator or a separate supply.

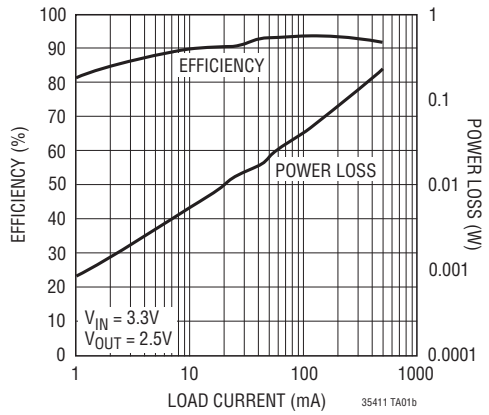


## TYPICAL APPLICATION

**LTC3541-1 Typical Application**




**Buck (Burst) Efficiency and Power Loss vs Load Current**



## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

Supply Voltages:
- $V_{IN}$, $LV_{IN}$ ..... –0.3V to 6V
- $LV_{IN} – V_{IN}$ ..... <0.3V

Pin Voltages:
- ENVLDO, ENBUCK, MODE, SW, LFB, BUCKFB ..... –0.3V to ($V_{IN}$ + 0.3V)

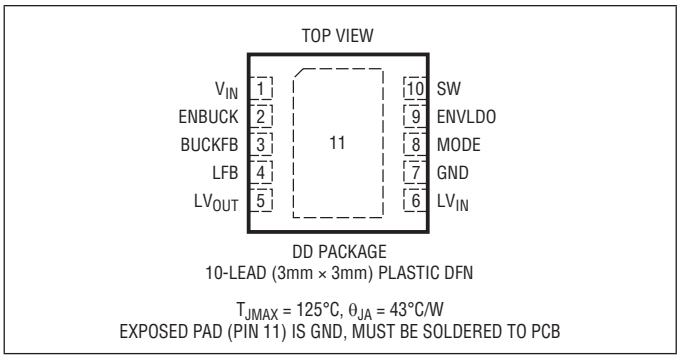
Linear Regulator $I_{OUT(MAX)}$ (100ms) (Note 9) .....100mA

Operating Ambient Temperature Range (Note 2).....–40°C to 85°C

Junction Temperature (Note 5) ..... 125°C

Storage Temperature Range ..... –65°C to 125°C

## PIN CONFIGURATION




DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

http://www.linear.com/product/LTC3541-1#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3541EDD-1#PBF | LTC3541EDD-1#TRPBF | LCWQ | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise specified (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{PK}$ | Peak Inductor Current | $V_{IN}$ = 4.2V (Note 8) | | 0.8 | 0.95 | 1.25 | A |
| $I_{BUCKFB}$ | BUCKFB Pin Input Current | $V_{BUCKFB}$ = 0.9V | ● | | | ±50 | nA |
| $I_{LFB}$ | LFB Pin Input Current | $V_{LFB}$ = 0.45V | ● | –200 | –40 | | nA |
| $V_{IN}$ | Input Voltage Range | (Note 4) | ● | 2.7 | | 5.5 | V |
| $V_{IN(LINEREG)}$ | Buck $V_{IN}$ Line Regulation | $V_{IN}$ = 2.7V to 5.5V, ENBUCK = $V_{IN}$, ENVLDO = 0V, MODE = $V_{IN}$ (Note 6) | ● | | 0.04 | 0.4 | %/V |
| | VLDO $V_{IN}$ Line Regulation (Referred to LFB) | $V_{IN}$ = 2.7V to 5.5V, $LV_{OUT}$ = 1.2V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, $I_{OUT(VLDO)}$ = 100mA, $LV_{IN}$ = 1.5V | | | 0.6 | | mV/V |
| | Linear Regulator $V_{IN}$ Line Regulation (Referred to LFB) | $V_{IN}$ = 2.7V to 5.5V, $LV_{OUT}$ = 1.2V, ENBUCK = 0V, ENVLDO = $V_{IN}$, $I_{OUT(LREG)}$ = 10mA | | | 0.6 | | mV/V |
| $LV_{IN(LINEREG)}$ | $LV_{IN}$ Line Regulation (Referred to LFB) | $LV_{IN}$ = 0.9V to 5.5V, $V_{IN}$ = 5.5V, $LV_{OUT}$ = 0.4V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, MODE = $V_{IN}$, $I_{OUT(VLDO)}$ = 100mA | | | 0.3 | | mV/V |
| $VLDO_{DO}$ | $LV_{IN}$ – $LV_{OUT}$ Dropout Voltage (Note 9) | $LV_{IN}$ = 1.5V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, MODE = $V_{IN}$, $I_{OUT(VLDO)}$ = 50mA, $V_{LFB}$ = 0.3V | | | 28 | 60 | mV |
| $V_{LOADREG}$ | Buck Output Load Regulation | ENBUCK = $V_{IN}$, ENVLDO = 0V, MODE = $V_{IN}$ (Note 6) | | | 0.5 | | % |
| | VLDO Output Load Regulation | $I_{OUT(VLDO)}$ = 1mA – 300mA, $LV_{IN}$ = 1.5V, $LV_{OUT}$ = 1.2V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, MODE = $V_{IN}$ | ● | | 0.25 | 0.5 | % |
| | Linear Regulator Output Load | $I_{OUT(LREG)}$ = 1mA – 30mA, $LV_{OUT}$ = 1.2V, ENBUCK = 0V, ENVLDO = $V_{IN}$ | ● | | 0.25 | 0.5 | % |
| $V_{BUCKFB}$ | Reference Regulation Voltage (Note 6) | ENBUCK = $V_{IN}$, ENVLDO = 0V, $T_A$ = 25°C | | 0.784 | 0.8 | 0.816 | V |
| | | ENBUCK = $V_{IN}$, ENVLDO = 0V, 0°C ≤ $T_A$ ≤ 85°C | | 0.782 | 0.8 | 0.818 | V |
| | | ENBUCK = $V_{IN}$, ENVLDO = 0V, –40°C ≤ $T_A$ ≤ 85°C | ● | 0.78 | 0.8 | 0.82 | V |
| $V_{LFB}$ | Reference Regulation Voltage (Note 7) | ENBUCK = 0V, ENVLDO = $V_{IN}$, $T_A$ = 25°C | | 0.392 | 0.4 | 0.408 | V |
| | | ENBUCK = 0V, ENVLDO = $V_{IN}$, 0°C ≤ $T_A$ ≤ 85°C | | 0.391 | 0.4 | 0.409 | V |
| | | ENBUCK = 0V, ENVLDO = $V_{IN}$, –40°C ≤ $T_A$ ≤ 85°C | ● | 0.390 | 0.4 | 0.410 | V |
| $I_S$ | Buck + VLDO Burst Mode Sleep $V_{IN}$ Quiescent Current | $LV_{IN}$ = 1.5V, $LV_{OUT}$ = 1.2V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, MODE = 0V, $I_{OUT(VLDO)}$ = 10µA, $V_{BUCKFB}$ = 0.9V | | | 85 | | µA |
| | Buck + VLDO Burst Mode Active $V_{IN}$ Quiescent Current | $LV_{IN}$ = 1.5V, $LV_{OUT}$ = 1.2V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, MODE = 0V, $I_{OUT(VLDO)}$ = 10µA, $V_{BUCKFB}$ = 0.7V | | | 315 | | µA |
| | Buck + VLDO Pulse-Skip Mode Active $V_{IN}$ Quiescent Current | $LV_{IN}$ = 1.5V, $LV_{OUT}$ = 1.2V, ENBUCK = $V_{IN}$, ENVLDO = $V_{IN}$, MODE = $V_{IN}$, $I_{OUT(VLDO)}$ = 10µA, $V_{BUCKFB}$ = 0.7V | | | 300 | | µA |
| | Buck Burst Mode Sleep $V_{IN}$ Quiescent Current | $V_{BUCKFB}$ = 0.9V, $I_{OUT(BUCK)}$ = 0A, ENBUCK = $V_{IN}$, ENVLDO = 0V, MODE = 0V | | | 55 | | µA |
| | Buck Burst Mode Active $V_{IN}$ Quiescent Current | $V_{BUCKFB}$ = 0.7V, $I_{OUT(BUCK)}$ = 0A, ENBUCK = $V_{IN}$, ENVLDO = 0V, MODE = 0V | | | 300 | | µA |
| | Buck Pulse-Skip Mode Active $V_{IN}$ Quiescent Current | $V_{BUCKFB}$ = 0.7V, $I_{OUT(BUCK)}$ = 0A, ENBUCK = $V_{IN}$, ENVLDO = 0V, MODE = $V_{IN}$ | | | 285 | | µA |
| | Linear Regulator $V_{IN}$ Quiescent Current | $LV_{OUT}$ = 1.2V, ENBUCK = 0V, ENVLDO = $V_{IN}$, $I_{OUT(LREG)}$ = 10µA | | | 50 | | µA |
| | $V_{IN}$ Shutdown Quiescent Current | ENBUCK = 0V, ENVLDO = 0V | | | 2.5 | | µA |
| | $LV_{IN}$ Shutdown Quiescent Current | $LV_{IN}$ = 3.6V, ENBUCK = 0V, ENVLDO = 0V | | | 0.1 | | µA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.6V unless otherwise specified (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $f_{OSC}$ | Oscillator Frequency | | ● | 1.8 | 2.25 | 2.7 | MHz |
| $R_{PFET}$ | $R_{DS(ON)}$ of P-Channel MOSFET | $I_{SW}$ = 100mA | | | 0.25 | | Ω |
| $R_{NFET}$ | $R_{DS(ON)}$ of N-Channel MOSFET | $I_{SW}$ = 100mA | | | 0.35 | | Ω |
| $I_{LSW}$ | SW Leakage | Enable = 0V, $V_{SW}$ = 0V or 6V, $V_{IN}$ = 6V | | | ±0.01 | ±1 | µA |
| $V_{IH}$ | Input Pin High Threshold | MODE, ENBUCK, ENVLDO | ● | 0.9 | | | V |
| $V_{IL}$ | Input Pin Low Threshold | MODE, ENBUCK, ENVLDO | ● | | | 0.3 | V |
| $I_{MODE}$, $I_{ENBUCK}$, $I_{ENVLDO}$ | Input Pin Current | | ● | | ±0.01 | ±1 | µA |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3541-1 is guaranteed to meet performance specifications from 0°C to 85°C. VLDO/linear regulator output is tested and specified under pulse load conditions such that $T_J \approx T_A$, and are 100% production tested at 25°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Minimum operating $LV_{IN}$ voltage required for VLDO regulator regulation is:

$$LV_{IN} \geq LV_{OUT} + V_{DROPOUT} \text{ and } LV_{IN} \geq 0.9V$$

**Note 4:** Minimum operating VIN voltage required for VLDO regulator and linear regulator regulation is:

$$V_{IN} \geq LV_{OUT} + 1.4V \text{ and } V_{IN} \geq 2.7V$$

**Note 5:** TJ is calculated from the ambient temperature, $T_A$, and power dissipation, $P_D$, according to the following formula:

$$T_J = T_A + (P_D \bullet 43°C/W)$$

**Note 6:** The LTC3541-1 is tested in a proprietary test mode that connects VBUCKFB to the output of the error amplifier. For the reference regulation and line regulation tests, the output of the error amplifier is set to the midpoint. For the load regulation test, the output of the error amplifier is driven to minimum and maximum of the signal range.

**Note 7:** Measurement made in closed loop linear regulator configuration with $LV_{OUT}$ = 1.2V, $I_{LOAD}$ = 10µA.

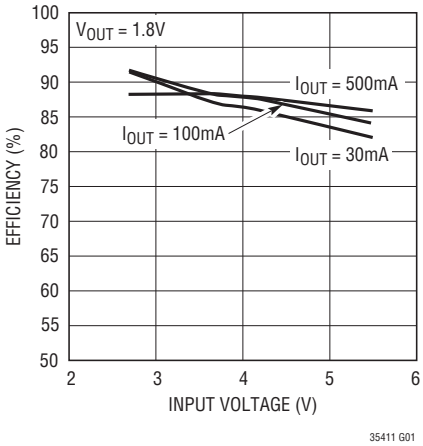
**Note 8:** Measurement made in a proprietary test mode with slope compensation disabled.

**Note 9:** Measurement is assured by design, characterization and statistical process control.

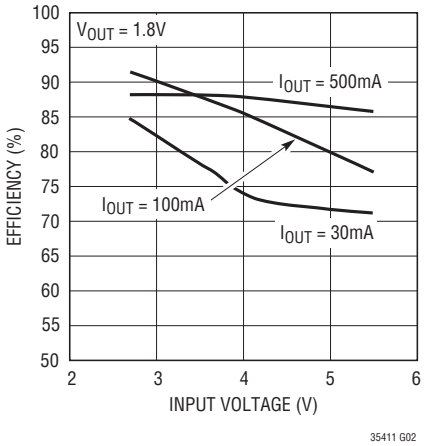
**Note 10:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

# TYPICAL PERFORMANCE CHARACTERISTICS

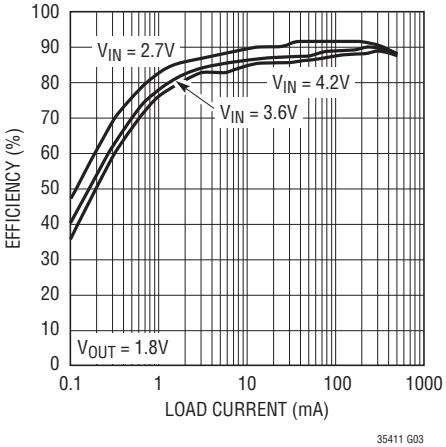
### Efficiency vs Input Voltage for Buck (Burst)



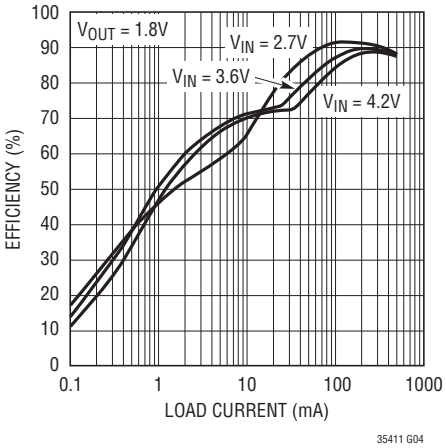

### Efficiency vs Input Voltage for Buck (Pulse Skip)



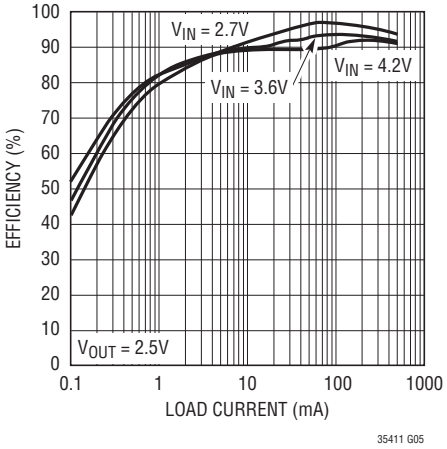

### Efficiency vs Load Current for Buck (Burst)



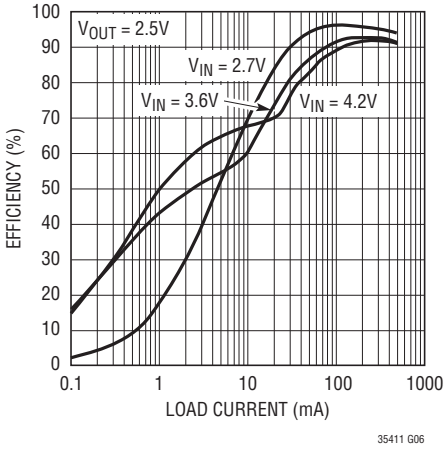

### Efficiency vs Load Current for Buck (Pulse Skip)



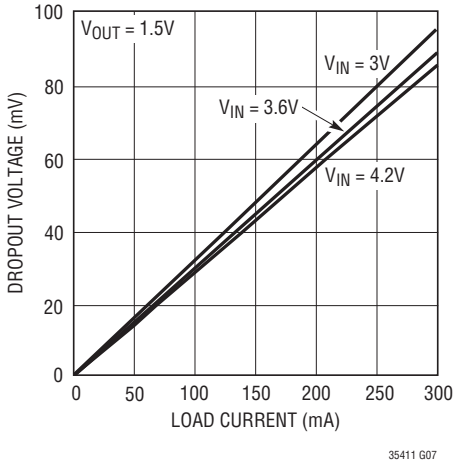

### Efficiency vs Load Current for Buck (Burst)



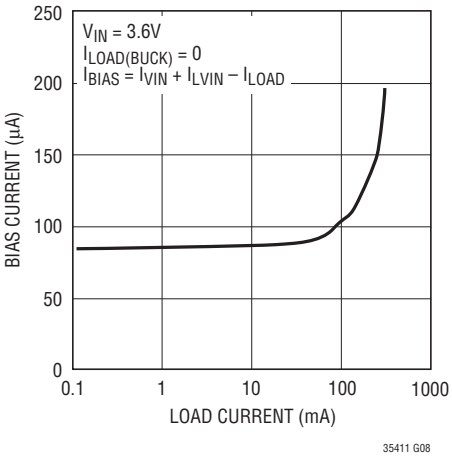

### Efficiency vs Load Current for Buck (Pulse Skip)



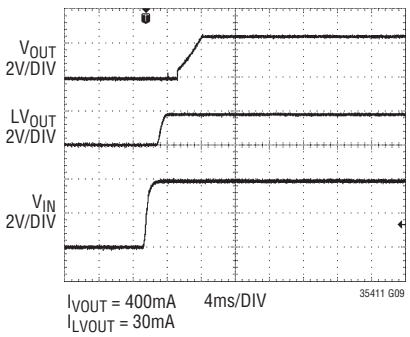

### VLDO Dropout Voltage vs Load Current




### Buck (Burst) Plus VLDO Bias Current vs VLDO Load Current

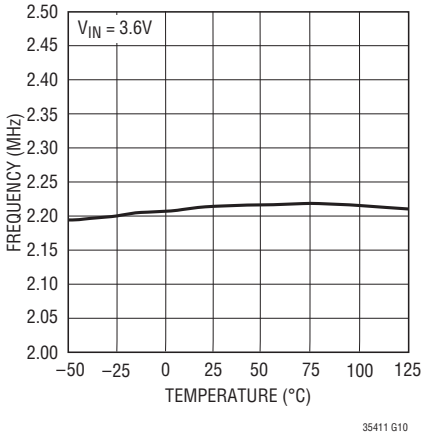



### Output (Auto Start-Up Sequence, Buck in Pulse Skip) vs Time

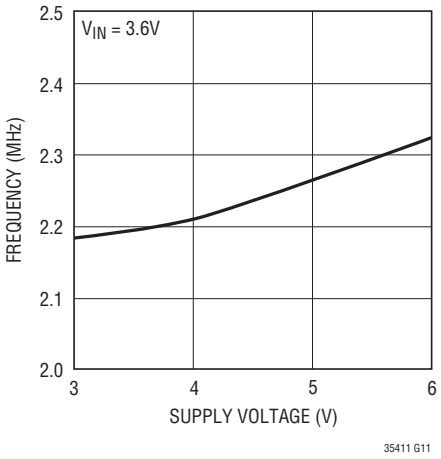


# TYPICAL PERFORMANCE CHARACTERISTICS

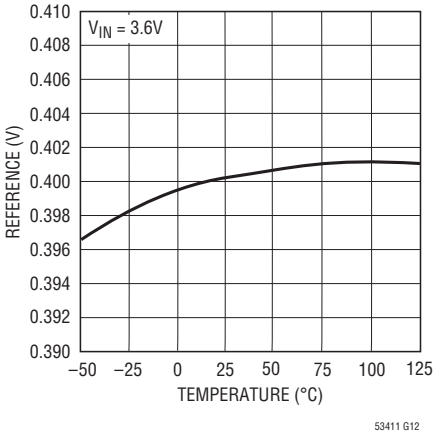
### Oscillator Frequency vs Temperature



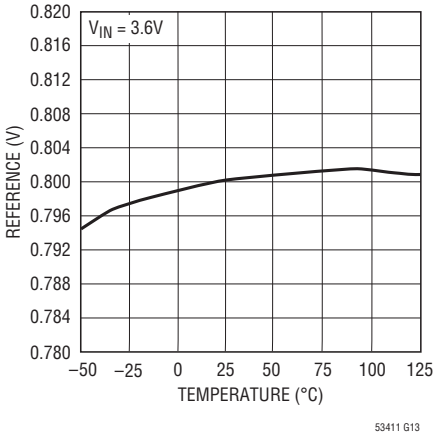

### Oscillator Frequency vs Supply Voltage



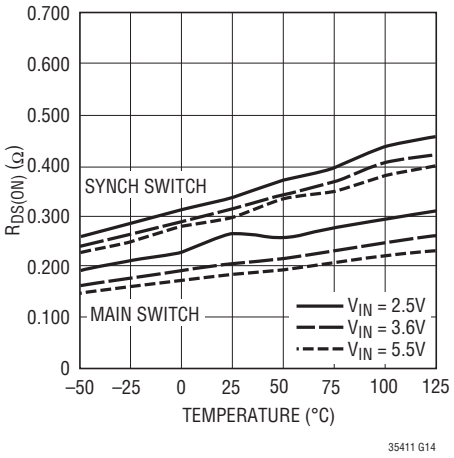

### VLDO/Linear Regulator Reference vs Temperature



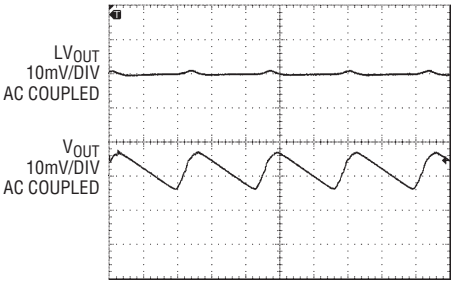

### Buck Reference vs Temperature




### $R_{DS(ON)}$ vs Temperature

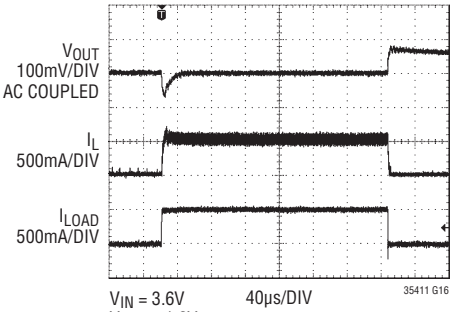



### Buck (Burst) and VLDO Output



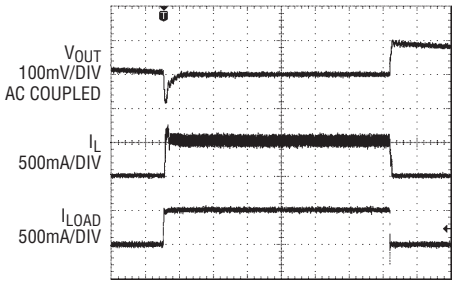

VIN = 3.6V 2µs/DIV
LVOUT = 1.5V
VOUT = 1.8V
ILOAD = 50mA
Burst Mode OPERATION

### Buck (Pulse Skip) Load Step from 1mA to 500mA



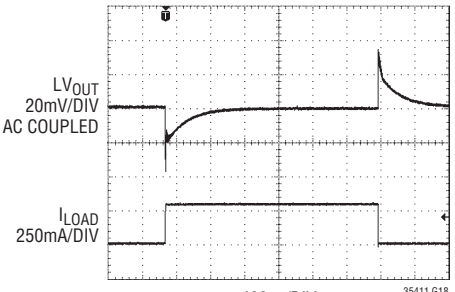

VIN = 3.6V 40µs/DIV
VOUT = 1.8V
ILOAD = 1mA TO 500mA

### Buck (Burst) Load Step from 1mA to 500mA




VIN = 3.6V 40µs/DIV
VOUT = 1.8V
ILOAD = 1mA TO 500mA

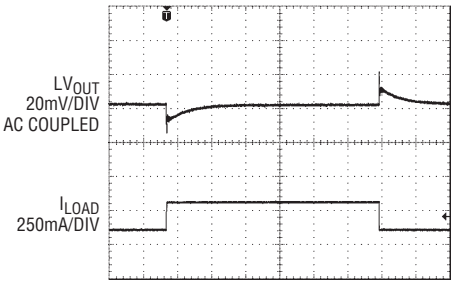
### VLDO Load Step from 1mA to 300mA




VIN = 3.6V 400µs/DIV
LVOUT = 1.5V
ILOAD = 1mA TO 300mA

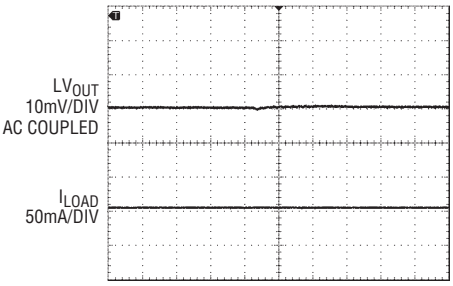
# TYPICAL PERFORMANCE CHARACTERISTICS

**VLDO Load Step from 100mA to 300mA**



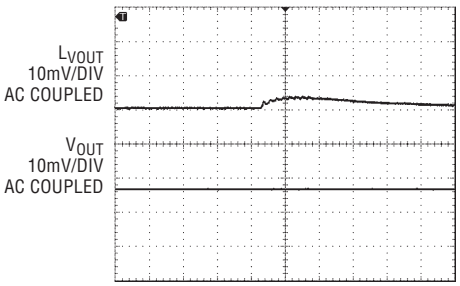

$V_{IN}$ = 3.6V 400µs/DIV
$LV_{OUT}$ = 1.5V
$I_{LOAD}$ = 100mA TO 300mA

**Linear Regulator to VLDO Transition, Load = 1mA**



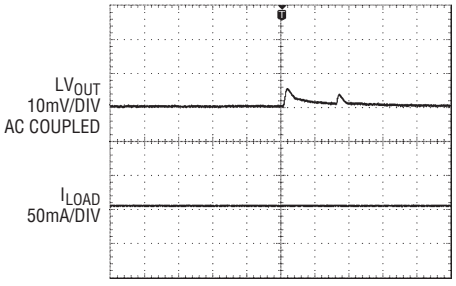

$V_{IN}$ = 3.6V 40µs/DIV
$LV_{OUT}$ = 1.5V
$I_{LOAD}$ = 1mA

**Linear Regulator to VLDO Transition, Load = 30mA**



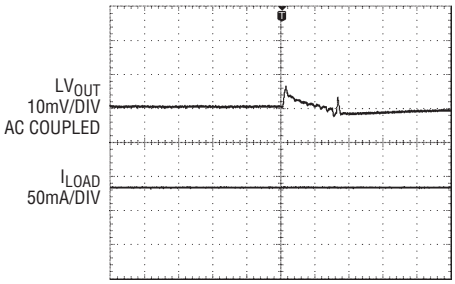

$V_{IN}$ = 3.6V 2µs/DIV
$LV_{OUT}$ = 1.5V
$V_{OUT}$ = 1.875V
$I_{LOAD}$ = 50mA
Burst Mode OPERATION

**VLDO to Linear Regulator Transition, Load = 1mA**




$V_{IN}$ = 3.6V 40µs/DIV
$LV_{OUT}$ = 1.5V
$I_{LOAD}$ = 1mA

**VLDO to Linear Regulator Transition, Load = 30mA**




$V_{IN}$ = 3.6V 40µs/DIV
$LV_{OUT}$ = 1.5V
$I_{LOAD}$ = 30mA

## PIN FUNCTIONS

**$V_{IN}$ (Pin 1):** Main Supply Pin. This pin must be closely decoupled to GND with a 10µF or greater capacitor.

**ENBUCK (Pin 2):** Buck Enable Pin. This pin enables the buck regulator when driven to a logic high.

**BUCKFB (Pin 3):** Buck Regulator Feedback Pin. This pin receives the buck regulator's feedback voltage from an external resistive divider.

**LFB (Pin 4):** VLDO/Linear Regulator Feedback Pin. This pin receives either the VLDO or linear regulator's feedback voltage from an external resistive divider.

**$LV_{OUT}$ (Pin 5):** VLDO/Linear Regulator Output Pin. This pin provides the regulated output voltage from the VLDO or linear regulator.

**$LV_{IN}$ (Pin 6):** VLDO/Linear Regulator Input Supply Pin. This pin provides the input supply voltage for the VLDO power FET.

**GND (Pin 7):** Analog Ground Pin.

**MODE (Pin 8):** Buck Mode Selection Pin. This pin enables buck Pulse-Skip operation when driven to a logic high and enables buck Burst Mode operation when driven to a logic low.

**ENVLDO (Pin 9):** VLDO/Linear Regulator Enable Pin. When driven to a logic high, this pin enables the linear regulator when the ENBUCK pin is driven to a logic low, and enables the VLDO when the ENBUCK pin is driven to a logic high.

**SW (Pin 10):** Switch Node Pin. This pin connects the internal main and synchronous power MOSFET switches to the external inductor for the buck regulator.

**Exposed Pad (Pin 11):** Ground Pin. This pin must be soldered to the PCB to provide both electrical contact to ground and good thermal contact to the PCB.

**Note:** Table 1 details the truth table for the control pins of the LTC3541-1.

**Table 1. LTC3541-1 Control Pin Truth Table**

| PIN NAME | | | |
|---|---|---|---|
| ENBUCK | ENVLDO | MODE | OPERATIONAL DESCRIPTION |
| 0 | 0 | X | LTC3541-1 Powered Down |
| 0 | 1 | X | Buck Powered Down, VLDO Regulator Powered Down, Linear Regulator Enabled |
| 1 | 0 | 0 | Buck Enabled, VLDO Regulator Powered Down, Linear Regulator Powered Down, Burst Mode Operation |
| 1 | 0 | 1 | Buck Enabled, VLDO Regulator Powered Down, Linear Regulator Powered Down, Pulse-Skip Mode Operation |
| 1 | 1 | 0 | Buck Enabled, VLDO Regulator Enabled, Linear Regulator Powered Down, Burst Mode Operation |
| 1 | 1 | 1 | Buck Enabled, VLDO Regulator Enabled, Linear Regulator Powered Down, Pulse-Skip Mode Operation |

## BLOCK DIAGRAM

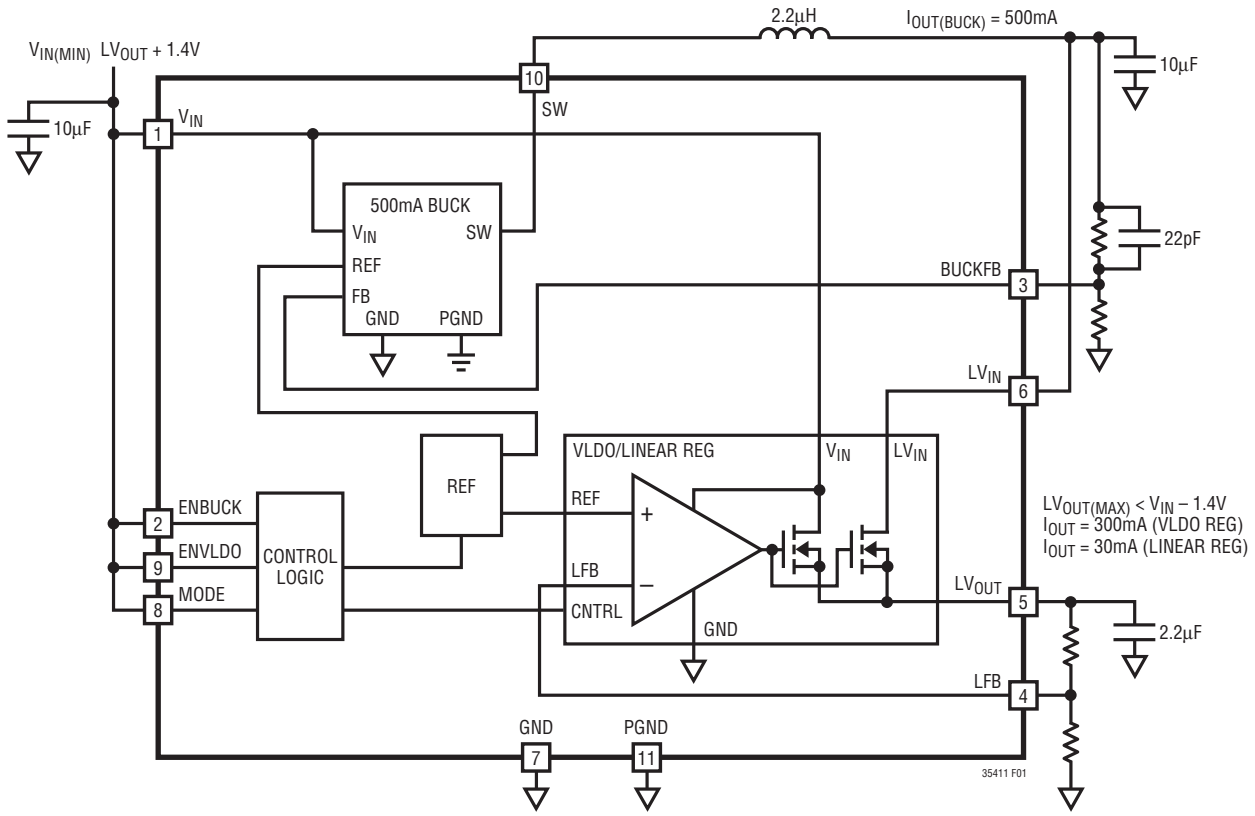



**Figure 1. LTC3541-1 Functional Block Diagram**

## OPERATION

The LTC3541-1 contains a high efficiency synchronous buck converter, a very low dropout regulator (VLDO) and a linear regulator. It can be used to provide up to two output voltages from a single input voltage making the LTC3541-1 ideal for applications with limited board space. The combination and configuration of these major blocks within the LTC3541-1 is determined by way of the control pins ENBUCK and ENVLDO as defined in Table 1.

With the ENBUCK pin driven to a logic high and ENVLDO driven to a logic low, the LTC3541-1 enables the buck converter to efficiently reduce the voltage provided at the $V_{IN}$ input pin to an output voltage which is set by an external feedback resistor network. The buck regulator can be configured for Pulse-Skip or Burst Mode operation by driving the MODE pin to a logic high or logic low respectively. The buck regulator is capable of providing a maximum output current of 500mA, which must be taken into consideration when using the buck regulator to provide the power for both the VLDO and for external loads.

With the ENBUCK pin driven to a logic low and ENVLDO driven to a logic high, the LTC3541-1 enables the linear regulator, providing a low noise regulated output voltage at the $LV_{OUT}$ pin while drawing minimal quiescent current from the $V_{IN}$ input pin. This feature allows output voltage $LV_{OUT}$ to be brought into regulation without the presence of the $LV_{IN}$ voltage.

With the ENBUCK and ENVLDO pins both driven to a logic high, the LTC3541-1 enables the high efficiency buck converter and VLDO regulator, providing dual output operation from a single input voltage. When configured in this manner, the LTC3541-1's auto start-up sequencing feature will bring the VLDO/linear regulator output into regulation in a controlled manner prior to enabling the

## OPERATION

buck regulator without the need for external pin control. A detailed discussion of the transitions between the VLDO and linear regulator can be found in the VLDO/Linear Regulator Loop section.

### Buck Regulator Control Loop

The LTC3541-1 internal buck regulator uses a constant frequency, current mode, step-down architecture. Both the main (top, P-channel MOSFET) and synchronous (bottom, N-channel MOSFET) switches are internal. During normal operation, the internal main switch is turned on at the beginning of each clock cycle provided the internal feedback voltage to the buck is less than the reference voltage. The current into the inductor provided to the load increases until the current limit is reached. Once the current limit is reached the main switch turns off and the energy stored in the inductor flows through the bottom synchronous switch into the load until the next clock cycle.

The peak inductor current is determined by comparing the buck feedback signal to an internal 0.8V reference. When the load current increases, the output of the buck and hence the buck feedback signal decrease. This decrease causes the peak inductor current to increase until the average inductor current matches the load current. While the main switch is off, the synchronous switch is turned on until either the inductor current starts to reverse direction or the beginning of a new clock cycle.

When the MODE pin is driven to a logic low, the LTC3541-1 buck regulator operates in Burst Mode operation for high efficiency. In this mode, the main switch operates based upon load demand. In Burst Mode operation the peak inductor current is set to a fixed value, where each burst event can last from a few clock cycles at light loads to nearly continuous cycling at moderate loads. Between burst events the main switch and any unneeded circuitry are turned off, reducing the quiescent current. In this sleep state, the load is being supplied solely from the output capacitor. As the output voltage droops, an internal error amplifier's output rises until a wake threshold is reached causing the main switch to again turn on. This process repeats at a rate that is dependent upon the load current demand.

When the MODE pin is driven to a logic high the LTC3541-1 operates in Pulse-Skip mode for low output voltage ripple. In this mode, the LTC3541-1 continues to switch at a constant frequency down to very low currents, where it will begin skipping pulses used to control the main (top) switch to maintain the proper average inductor current.

If the input supply voltage is decreased to a value approaching the output voltage, the duty cycle of the buck is increased toward maximum on-time and 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the main switch and the inductor.

### VLDO/Linear Regulator Loop

In the LTC3541-1, the VLDO and linear regulator loops consist of an amplifier and N-channel MOSFET output stages that, when connected with the proper external components, will servo the output to maintain a regulator output voltage, $LV_{OUT}$. The internal reference voltage provided to the amplifier is 0.4V allowing for a wide range of output voltages. Loop configurations enabling the VLDO or the linear regulator are stable with an output capacitance as low as 2.2µF and as high as 100µF. Both the VLDO and the linear regulators are capable of operating with an input voltage, $V_{IN}$, as low as 2.7V, but are subject to the constraint that $V_{IN}$ must be greater than $LV_{OUT}$ + 1.4V.

The VLDO is designed to provide up to 300mA of output current at a very low $LV_{IN}$ to $LV_{OUT}$ voltage. This allows a clean, secondary, analog supply voltage to be provided with a minimum drop in efficiency. The VLDO is provided with thermal protection that is designed to disable the VLDO function when the output, pass transistor's junction temperature reaches approximately 160°C. In addition to thermal protection, short-circuit detection is provided to disable the VLDO function when a short-circuit condition is sensed. This circuit is designed such that an output current of approximately 1A can be provided before this circuit will trigger. As detailed in the Electrical Characteristics, the VLDO regulator will be out of regulation when this event occurs. Both the thermal and short-circuit faults when detected are treated as catastrophic fault condi-

## OPERATION

tions. The LTC3541-1 will be reset upon the detection of either event. The N-channel MOSFET incorporated in the VLDO has its drain connected to the $LV_{IN}$ pin as shown in Figure 1. To ensure reliable operation, the $LV_{IN}$ voltage must be stable before the VLDO is enabled. For the case where the voltage on the $LV_{IN}$ pin is supplied by the buck regulator, the internal power supply sequencing logic assures voltages are applied in the appropriate manner. For the case where an external supply is used to power the $LV_{IN}$ pin, the voltage on the $LV_{IN}$ pin must be stable before the ENVLDO pin is brought from a low to a high. Further, the external $LV_{IN}$ voltage must be reduced in conjunction with $V_{IN}$ whenever $V_{IN}$ is pulled low or removed.

The linear regulator is designed to provide a lower output current (30mA) than that available from the VLDO. The linear regulator's output pass transistor has its drain tied to the $V_{IN}$ rail. This allows the linear regulator to be turned on prior to, and independent of, the buck regulator which would ordinarily drive the VLDO in a typical application. The linear regulator is provided with thermal protection that is designed to disable the linear regulator function when the output pass transistor's junction temperature reaches approximately 160°C. In addition to thermal protection, short-circuit detection is provided to disable the linear regulator function when a short-circuit condition is sensed. This circuit is designed such that an output current of approximately 120mA can be provided before this circuit will trigger. As detailed in the Electrical Characteristics, the linear regulator will be out of regulation when this event occurs. Both the thermal and short-circuit faults are treated as catastrophic fault conditions. The LTC3541-1 will be reset upon the detection of either event.

The N-channel MOSFET incorporated in the linear regulator has its drain connected to the $V_{IN}$ pin as shown in Figure 1. The size of this MOSFET and its associated power bussing is designed to accommodate 30mA of DC current. Currents above this can be supported for short periods as stipulated in the Absolute Maximum Ratings section.

Transitioning from linear regulator mode to VLDO mode, accomplished by bringing ENBUCK from a logic low to a logic high while ENVLDO is a logic high, is designed to be as seamless and transient free as possible. The precise transient response of $LV_{OUT}$ due to this transition is a function of $C_{OUT}$ and the load current. Waveforms given in the Typical Performance Characteristics show typical transient responses using the minimum $C_{OUT}$ of 2.2µF and load currents of 1mA and 30mA respectively. Generally, the amplitude of any transients present will decrease as $C_{OUT}$ is increased. To ensure reliable operation and adherence to the load regulation limits presented in the Electrical Characteristics table, the load current must not exceed the linear regulator $I_{OUT}$ limit of 30mA within 20ms after ENBUCK has transitioned to a logic high. The 300mA $I_{OUT}$ limit of VLDO applies thereafter. Further, for configurations that do not use the LTC3541-1's buck regulator to provide the VLDO input voltage ($LV_{IN}$), the user must ensure a stable $LV_{IN}$ voltage is present no less than 1ms prior to ENBUCK transitioning to a logic high.

In a similar manner, transitioning from VLDO mode to linear regulator mode, accomplished by bringing ENBUCK from a logic high to a logic low while ENVLDO is a logic high, is designed to be as seamless and transient free as possible. Again, the precise transient response of $LV_{OUT}$ due to this transition is a function of $C_{OUT}$ and the load current. Waveforms given in the Typical Performance Characteristics show typical transient responses using the minimum $C_{OUT}$ of 2.2µF and load currents of 1mA and 30mA respectively. Generally, the amplitude of any transients present will decrease as $C_{OUT}$ is increased. To ensure reliable operation and adherence to the load regulation limits presented in the Electrical Characteristics table, the load current must not exceed the linear regulator $I_{OUT}$ limit of 30mA 1ms prior to ENBUCK transitioning to a logic low and thereafter. Further, for configurations that do not use the LTC3541-1's buck regulator to provide the VLDO input voltage ($LV_{IN}$), the user must continue to ensure a stable $LV_{IN}$ voltage no less than 1ms after ENBUCK has transitioned to a logic low.

## APPLICATIONS INFORMATION

The basic LTC3541-1 application circuit is shown on the first page of this data sheet. External component selection is driven by the load requirement and requires the selection of L, followed by $C_{IN}$, $C_{OUT}$, and feedback resistor values for the buck and the selection of the output capacitor and feedback values for the VLDO and linear regulator.

### BUCK REGULATOR

#### Inductor Selection

For most applications, the appropriate inductor value will be in the range of 1.5µH to 3.3µH with 2.2µH the most commonly used. The exact inductor value is chosen largely based on the desired ripple current and burst ripple performance. Generally, large value inductors reduce ripple current, and conversely, small value inductors produce higher ripple current. Higher $V_{IN}$ or $V_{OUT}$ may also increase the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current is $\Delta I_L$ = 200mA (40% of 500mA).

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 600mA rated inductor should be enough for most applications (500mA + 100mA). For better efficiency, choose a low DC resistance inductor.

#### Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirement and any radiated field/EMI requirements rather than what the LTC3541-1 requires to operate. Table 2 shows some typical surface mount inductors that work well in LTC3541-1 applications.

**Table 2. Representative Surface Mount Inductors**

| PART NUMBER | VALUE (µH) | DCR (Ω MAX) | MAX DC CURRENT (A) | SIZE W × L × H (mm³) |
|---|---|---|---|---|
| Sumida CDRH3D23 | 1.0<br>1.5<br>2.2<br>3.3 | 0.025<br>0.029<br>0.038<br>0.048 | 2.0<br>1.5<br>1.3<br>1.1 | 3.9 × 3.9 × 2.4 |
| Sumida CMD4D06 | 2.2<br>3.3 | 0.116<br>0.174 | 0.950<br>0.770 | 3.5 × 4.3 × 0.8 |
| Coilcraft ME3220 | 1.0<br>1.5<br>2.2<br>3.3 | 0.058<br>0.068<br>0.104<br>0.138 | 2.7<br>2.2<br>1.0<br>1.3 | 2.5 × 3.2 × 2.0 |
| Murata LQH3C | 1.0<br>2.2 | 0.060<br>0.097 | 1.00<br>0.79 | 2.5 × 3.2 × 2.0 |
| Sumida CDRH2D11/HP | 1.5<br>2.2 | 0.06<br>0.10 | 1.00<br>0.72 | 3.2 × 3.2 × 1.2 |

#### $C_{IN}$ and $C_{OUT}$ Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $V_{OUT}/V_{IN}$. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{required}\ I_{RMS} \cong I_{OMAX} \frac{\left[V_{OUT}\left(V_{IN}-V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer with any question regarding proper capacitor choice.

The selection of $C_{OUT}$ for the buck regulator is driven by the desired buck loop transient response, required effective series resistance (ESR) and burst ripple performance.

The LTC3541-1 minimizes the required number of external components by providing internal loop compensation for the buck regulator loop. Loop stability, transient response and burst performance can be tailored by choice of output capacitance. For many applications, desirable stability, transient response and ripple performance can

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be obtained by choosing an output capacitor value of 10µF to 22µF. Typically, once the ESR requirement for $C_{OUT}$ has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple $\Delta V_{OUT}$ is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left( ESR + \frac{1}{8fC_{OUT}} \right)$$

where f = operating frequency, $C_{OUT}$ = output capacitance and $\Delta I_L$ = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage.

Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

### Using Ceramic Input and Output Capacitors

High value, low cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating, and low ESR make them ideal for switching regulator applications. Since the LTC3541-1's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input and the output. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$, large enough to damage the part.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

### Output Voltage Programming

The output voltage is set by tying BUCKFB to a resistive divider according to the following formula:

$$V_{OUT} = 0.8V \left( 1 + \frac{R2}{R1} \right)$$

Since the impedance at the BUCKFB pin is dependent upon the resistor divider network used, and phase shift due to this impedance directly impacts the transient response of the buck, R1 should be chosen <125k. In addition, stray capacitance at this pin should be minimized (<5pF) to prevent excessive phase shift. Finally, special attention should be given to any stray capacitances that can couple external signals onto the BUCKFB pin producing undesirable output ripple. For optimum performance connect the BUCKFB pin to R1 and R2 with a short PCB trace and minimize all other stray capacitance to the BUCKFB pin.

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure 6.

### Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, $V_{OUT}$ immediately shifts by an amount equal to ($\Delta I_{LOAD}$ • ESR), where ESR is the effective series

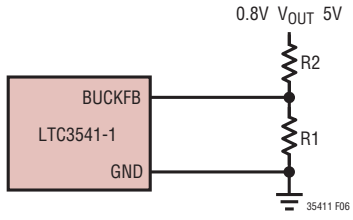


**Figure 6. Setting the LTC3541-1 Output Voltage**

## APPLICATIONS INFORMATION

resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$, which generates a feedback error signal. The regulator loop then acts to return $V_{OUT}$ to its steady-state value. During this recovery time $V_{OUT}$ can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • $C_{LOAD}$). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

### VLDO/LINEAR REGULATOR

#### Adjustable Output Voltage

The LTC3541-1 $LV_{OUT}$ output voltage is set by the ratio of two external resistors as shown in Figure 7. The device servos $LV_{OUT}$ to maintain the LFB pin voltage at 0.4V (referenced to ground). Thus, the current in R1 is equal to 0.4V/R1. For good transient response, stability, and accuracy, the current in R1 should be at least 2µA, thus the value of R1 should be no greater than 200k. The current in R2 is the current in R1 plus the LFB pin bias current. Since the LFB pin bias current is typically <10nA, it can be ignored in the output voltage calculation. The output voltage can be calculated using the formula in Figure 8. Note that in shutdown the output is turned off and the divider current will be zero once $C_{OUT}$ is discharged.

The LTC3541-1 VLDO and linear regulator loops operate at a relatively high gain of –3.5µV/mA and –3.4µV/mA respectively, referred to the LFB input. Thus, a load current change of 1mA to 300mA produces a 1.05mV drop at the LFB input for the VLDO and a load current change of 1mA to 30mA produces a 0.1mV drop at the LFB input

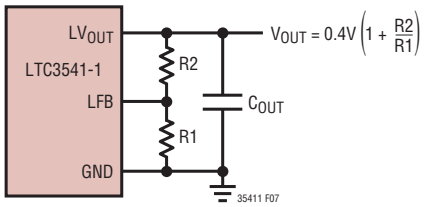


**Figure 7. Programming the LTC3541-1**

for the linear regulator. To calculate the change referred to the output simply multiply by the gain of the feedback network (i.e., 1 + R2/R1). For example, to program the output for 1.2V choose R2/R1 = 2. In this example, an output current change of 1mA to 300mA produces 1.05mV • (1 + 2) = 3.15mV drop at the output.

Since the LFB pin is relatively high impedance (depending on the resistor divider used), stray capacitance at this pin should be minimized (<10pF) to prevent phase shift in the error amplifier loop. Additionally, special attention should be given to any stray capacitances that can couple external signals onto the LFB pin producing undesirable output ripple. For optimum performance connect the LFB pin to R1 and R2 with a short PCB trace and minimize all other stray capacitance to the LFB pin.

#### Output Capacitance and Transient Response

The LTC3541-1 is designed to be stable with a wide range of ceramic output capacitors. The ESR of the output capacitor affects stability, most notably with small capacitors. A minimum output capacitor of 2.2µF with an ESR of 0.05Ω or less is recommended to ensure stability. The LTC3541-1 VLDO is a micropower device and output transient response will be a function of output capacitance. Larger values of output capacitance decrease the peak deviations and provide improved transient response for larger load current changes. Note that bypass capacitors used to decouple individual components powered by the LTC3541-1 will increase the effective output capacitor value. High ESR tantalum and electrolytic capacitors may be used, but a low ESR ceramic capacitor must be in parallel at the output. There is no minimum ESR or maximum capacitor size requirement.

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Extra consideration must be given to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit large voltage and temperature coefficients as shown in Figures 8 and 9. When used with a 2V regulator, a 1µF Y5V capacitor can lose as much as 75% of its initial capacitance over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are usually more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. In all cases, the output capacitance should never drop below 1µF or instability or degraded performance may occur.

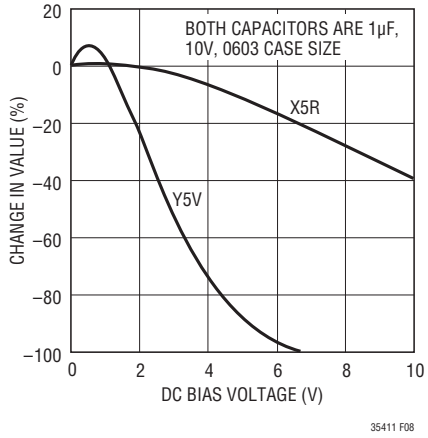


**Figure 8. Change in Capacitor vs Bias Voltage**

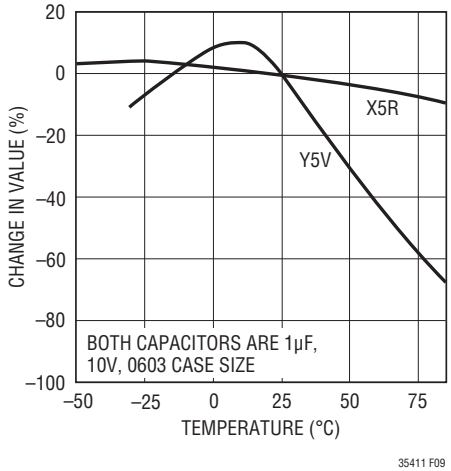


**Figure 9. Change in Capacitor vs Temperature**

### EFFICIENCY CONSIDERATIONS

Generally, the efficiency of a regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual loss terms to determine which terms are limiting efficiency and what if any change would yield the greatest improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual loss terms as a percentage of input power.

Although all dissipative elements in the circuit produce losses, three main sources typically account for the majority of the losses in the LTC3541-1 circuits: $V_{IN}$ quiescent current, $I^2R$ losses and loss across VLDO output device. When operating with both the buck and VLDO active (ENBUCK and ENVLDO equal to logic high), $V_{IN}$ quiescent current loss and loss across the VLDO output device dominate the efficiency loss at low load currents, whereas the $I^2R$ loss and loss across the VLDO output device dominate the efficiency loss at medium to high load currents. At low load currents with the part operating with the linear regulator (ENBUCK equal to logic low, ENVLDO equal to logic high), efficiency is typically dominated by the loss across the linear regulator output device and $V_{IN}$ quiescent current. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of little consequence.

1. The $V_{IN}$ quiescent current loss in the buck is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power switches. Each time the gate is switched from high to low to high again, a packet of charge, $d_q$, moves from $V_{IN}$ to ground. The resulting $d_q/d_t$ is the current out of $V_{IN}$ that is typically larger than the DC bias current

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and proportional to frequency. Both the DC bias and gate charge losses are proportional to $V_{IN}$ and thus their effects will be more pronounced at higher supply voltages.

2. $I^2R$ losses are calculated from the resistances of the internal switches, $R_{SW}$, and external inductor $R_L$. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain $I^2R$ losses, simply add $R_{SW}$ to $R_L$ and multiply the result by the square of the average output current.

3. Losses in the VLDO/linear regulator are due to the DC bias currents as given in the Electrical Characteristics and to the ($V_{IN} - V_{OUT}$) voltage drop across the internal output device transistor.

Other losses when the buck and VLDO are in operation (ENBUCK and ENVLDO equal logic high), including $C_{IN}$ and $C_{OUT}$ ESR dissipative losses and inductor core losses, generally account for less than 2% total additional loss.

### THERMAL CONSIDERATIONS

The LTC3541-1 requires the package backplane metal (GND pin) to be well soldered to the PC board. This gives the DFN package exceptional thermal properties. The power handling capability of the device will be limited by the maximum rated junction temperature of 125°C. The LTC3541-1 has internal thermal limiting designed to protect the device during momentary overload conditions. For continuous normal conditions, the maximum junction temperature rating of 125°C must not be exceeded. It is important to give careful consideration to all sources of thermal resistance from junction to ambient. Additional heat sources mounted nearby must also be considered.

For surface mount devices, heat sinking is accomplished by using the heat-spreading capabilities of the PC board and its copper traces. Copper board stiffeners and plated through holes can also be used to spread the heat generated by power devices.

To avoid the LTC3541-1 exceeding the maximum junction temperature, some thermal analysis is required. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_R = P_D \bullet \theta_{JA}$$

where $P_D$ is the power dissipated by the regulator and $\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, $T_J$, is given by:

$$T_J = T_A + T_R$$

where $T_A$ is the ambient temperature.

As an example, consider the LTC3541-1 with an input voltage $V_{IN}$ of 2.9V, an $LV_{IN}$ voltage of 1.8V, an $LV_{OUT}$ voltage of 1.5V, a load current of 200mA for the buck, a load current of 300mA for the VLDO and an ambient temperature of 85°C. From the typical performance graph of switch resistance, the $R_{DS(ON)}$ of the P-channel switch at 85°C is approximately 0.25Ω. The $R_{DS(ON)}$ of the N-channel switch is approximately 0.4Ω. Therefore, power dissipated by the part is approximately:

$$P_D = (I_{LOADBUCK})^2 \bullet R_{SW} + (I_{LOADVLDO}) \bullet (LV_{IN} - LV_{OUT}) = 167mW$$

For the 3mm × 3mm DFN package, the $\theta_{JA}$ is 43°C/W.

Thus, the junction temperature of the regulator is:

$$T_J = 85°C + (0.167)(43) = 92°C$$

which is well below the maximum junction temperature of 125°C.

Note that at higher supply voltages, the junction temperature is lower due to reduced switch resistance $R_{DS(ON)}$.

# APPLICATIONS INFORMATION

## PC BOARD LAYOUT CHECKLIST

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3541-1. Check the following in your layout:

1. The power traces, consisting of the GND trace, the SW trace and the $V_{IN}$ trace should be kept short, direct and wide.

2. Does the LFB pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of $C_{OUT}$ and ground.

3. Does the (+) plate of $C_{IN}$ connect to $V_{IN}$ as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.

4. Keep the switching node, SW, away from the sensitive LFB node.

5. Keep the (–) plates of $C_{IN}$ and $C_{OUT}$ as close as possible.

## DESIGN EXAMPLE

As a design example, assume the LTC3541-1 is used in a single lithium-ion battery powered cellular phone application. The $V_{IN}$ will be operating from a maximum of 4.2V down to about 3V. The load current requirement is a maximum of 0.5A for the buck output but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. The output voltage for the buck is 1.8V. The requirement for the output voltage of the VLDO is 1.5V while providing up to 0.3A of current. With this information we can calculate L using Equation 2:

$$L = \frac{1}{(f)(\Delta I_L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (2)$$

Substituting $V_{OUT}$ = 1.8V, $V_{IN}$ = 3.6V (typ), $\Delta I_L$ = 0.2A and f = 2.25MHz in Equation 3 gives:

$$L = \frac{1.8V}{2.25MHz(200mA)}\left(1 - \frac{1.8V}{3.6V}\right) = 2\mu H \quad (3)$$

A 2.2µH inductor works well for this application. For best efficiency choose a 600mA or greater inductor with less than 0.2Ω series resistance.

$C_{IN}$ will require an RMS current rating of at least 0.25A = $I_{LOAD(MAX)}/2$ at temperature . $C_{OUT}$ for the buck is chosen as 22µF with an ESR of less than 0.2Ω. In most cases, a ceramic capacitor will satisfy this requirement.

For the feedback resistors of the buck, choose R1 = 80k. R2 can then be calculated from Equation 4 to be:

$$R2 = \left(\frac{V_{OUT}}{0.8} - 1\right) R1 = 100k \quad (4)$$

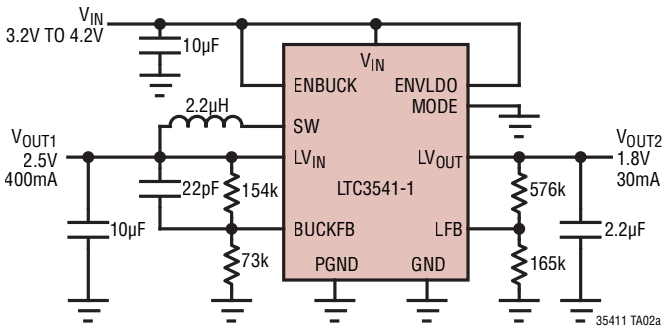
For the feedback resistors of the VLDO, choose R1 = 200k. R2 can then be calculated from Equation 5 to be:

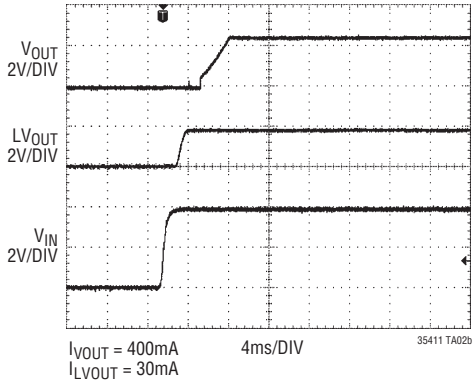
$$R2 = \left(\frac{V_{OUT}}{0.4} - 1\right) R1 = 550k$$

$C_{OUT}$ for the VLDO is chosen as 2.2µF.

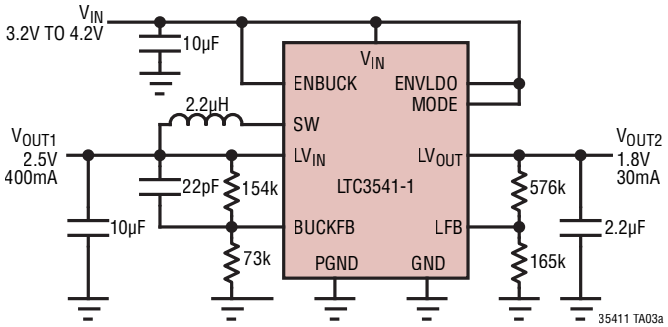
# TYPICAL APPLICATIONS

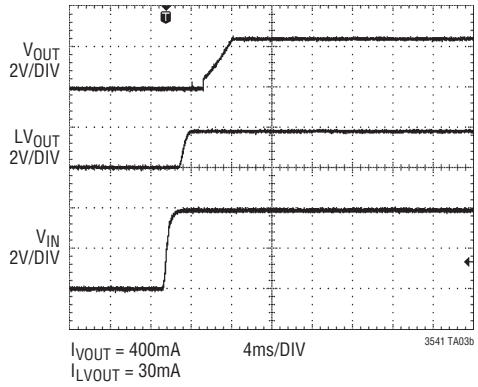
**Dual Output with Minimal External Components Using Auto Start-Up Sequence, Buck in Burst Mode Operation for High Efficiency Down to Low Load Currents**



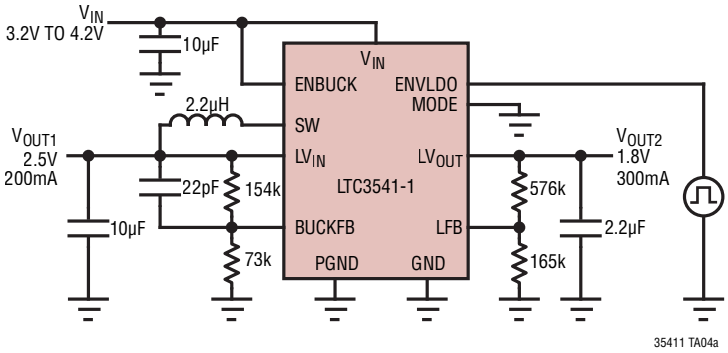

**Dual Output with Minimal External Components Using Auto Start-Up Sequence, Buck in Pulse Skip Mode for Low Noise Operation**

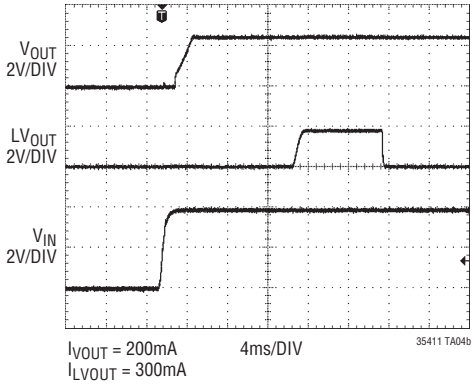


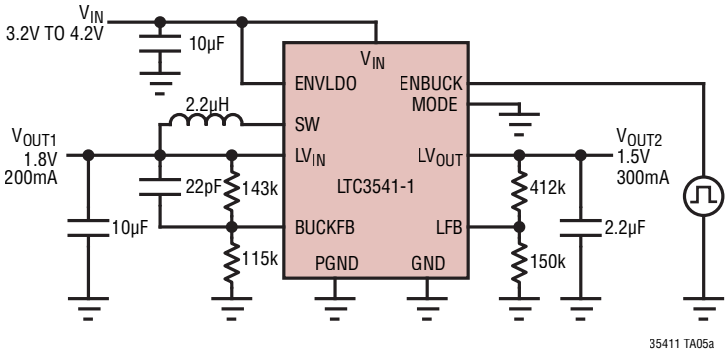
# TYPICAL APPLICATIONS

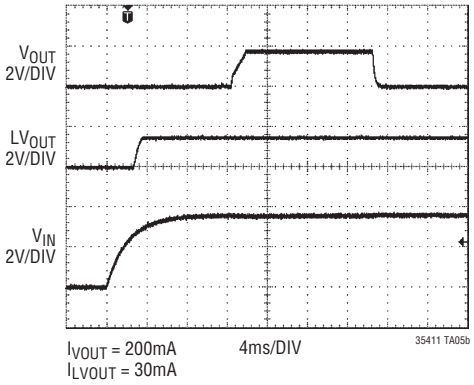
**Dual Output Using Minimal External Components with $V_{OUT2}$ Controlled by External Logic Signal, Buck in Burst Mode Operation for High Efficiency Down to Low Load Currents**




**Dual Output Using Minimal External Components with $V_{OUT1}$ Controlled by External Logic Signal, Buck in Burst Mode Operation for High Efficiency Down to Low Load Currents**

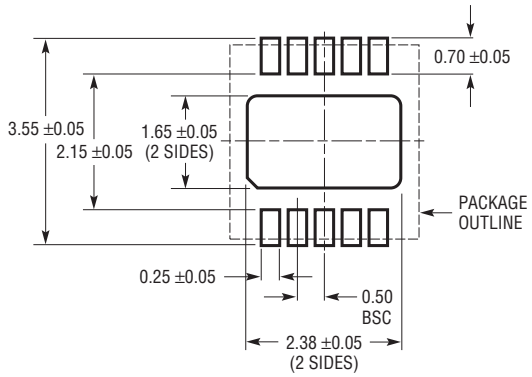


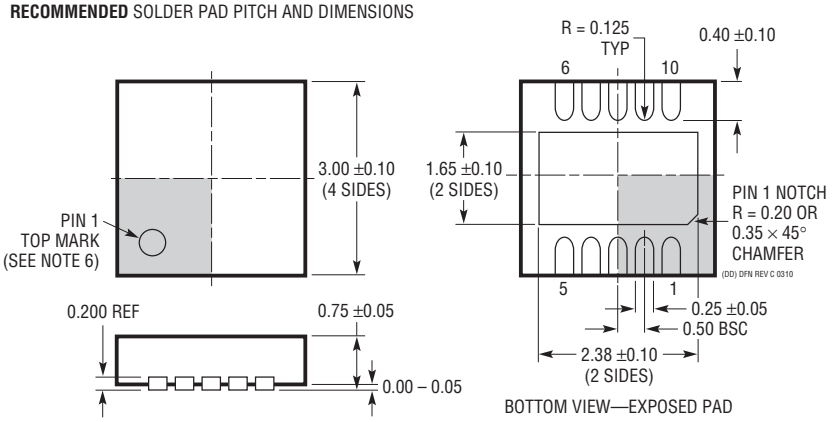
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/product/LTC3541-1#packaging for the most recent package drawings.**

**DD Package**
**10-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1699 Rev C)




**RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS




BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY (Revision history begins at Rev B)

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| B | 04/16 | Revised Typical Application circuit<br>Added 10µF capacitor to $V_{IN}$ line<br>Revised top and bottom schematics | 1<br>9<br>18, 19 |

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LT®3023 | Dual, 2x100mA, Low Noise Micropower LDO | $V_{IN}$: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, $V_{DO}$ = 0.30V, $I_Q$ = 40µA, $I_{SD}$ < 1µA, $V_{OUT}$ = ADJ, DFN, MS Packages, Low Noise < 20µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors |
| LT3024 | Dual, 100mA/500mA, Low Noise Micropower LDO | $V_{IN}$: 1.8V to 20V, $V_{OUT(MIN)}$ = 1.22V, $V_{DO}$ = 0.30V, $I_Q$ = 60µA, $I_{SD}$ < 1µA, $V_{OUT}$ = ADJ, DFN, TSSOP Packages, Low Noise < 20µ$V_{RMS(P-P)}$, Stable with 1µF Ceramic Capacitors |
| LTC3025 | 300mA, Micropower VLDO Linear Regulator | $V_{IN}$: 0.9V to 5.5V, $V_{OUT(MIN)}$ = 0.4V, 2.7V to 5.5V Bias Voltage Required, $V_{DO}$ = 45mV, $I_Q$ = 50µA, $I_{SD}$ < 1µA, $V_{OUT}$ = ADJ, DFN Packages, Stable with 1µF Ceramic Capacitors |
| LTC3407 | Dual Synchronous 600mA Synchronous Step-Down DC/DC Regulator | 1.5MHz Constant Frequency Current Mode Operation, $V_{IN}$ from 2.5V to 5.5V, $V_{OUT}$ Down to 0.6V, DFN, MS Packages |
| LTC3407-2 | Dual Synchronous 800mA Synchronous Step-Down DC/DC Regulator, 2.25MHz | 2.25MHz Constant Frequency Current Mode Operation, $V_{IN}$ from 2.5V to 5.5V, $V_{OUT}$ Down to 0.6V, DFN, MS Packages |
| LTC3445 | $I^2C$ Controllable Buck Regulator with Two LDOs and Backup Battery Input | 600mA, 1.5MHz Current Mode Buck Regulator, $I^2C$ Programmable $V_{OUT}$ from 0.85V to 1.55V, two 50mA LDOs, Backup Battery Input with PowerPath Control, QFN Package |
| LTC3446 | Triple Output Step-Down Converter 1A Output Buck, Two Each 300mA VDLOs | $V_{IN}$: 2.7V to 5.5V, $V_{OUT(MIN)}$ Buck = 0.8V, $V_{OUT(MIN)}$ VLDO = 0.4$V_{OUT(MIN)}$, 14-Pin DFN Package |
| LTC3448 | 600mA ($I_{OUT}$), High Efficiency, 1.5MHz/2.25MHz Synchronous Step-Down Regulator with LDO Mode | $V_{IN}$: 2.7V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, Switches to LDO Mode at ≤3A, DD8, MS8/E Packages |
| LTC3541 | High Efficiency Buck + VLDO Regulator | $V_{IN}$: 2.7V to 5.5V, $V_{OUT(MIN)}$ Buck = 0.8V, $V_{OUT(MIN)}$ VLDO = 0.4V, 3mm × 3mm 10-Pin DFN Package |
| LTC3541-2 | High Efficiency Buck plus VLDO Regulator | $V_{IN}$: 2.9V to 5.5V, $V_{OUT(BUCK)}$ = 1.875V, $V_{OUT(VLDO)}$ = 1.5V, 3mm × 3mm 10-Pin DFN Package |
| LTC3541-3 | High Efficiency Buck plus VLDO Regulator | $V_{IN}$: 3V to 5.5V, $V_{OUT(BUCK)}$ = 1.8V, $V_{OUT(VLDO)}$ = 1.575V, 3mm × 3mm 10-Pin DFN Package |
| LTC3547 | Dual 300mA ($I_{OUT}$), 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ < 1µA, 8-Pin DFN Package |
| LTC3548/LTC3548-1/ LTC3548-2 | Dual 800mA/400mA ($I_{OUT}$), 2.25MHz, Synchronous Step-Down DC/DC Converter | 95% Efficiency, $V_{IN}$: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, $I_Q$ = 40µA, $I_{SD}$ < 1µA, DFN and 10-Pin MS Packages |
| LTC3700 | Step-Down DC/DC Controller with LDO Regulator | $V_{IN}$ from 2.65V to 9.8V, Constant Frequency 550kHz Operation |



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