Micropower Synchronous Buck-Boost DC/DC Converter for WCDMA Applications

FEATURES

- **Optimized Features for WCDMA Handsets**
- **Regulated Output with Input Voltages Above, Below, or Equal to the Output**
- **0.5V to 5V Output Range**
- **Up to 400mA Continuous Output Current From a Single Lithium-Ion Cell**
- **Minimal External Components**
- **1.5MHz Fixed Frequency Operation**
- **Internal Loop Compensation for Fast Response <25µs Full Scale Output Slewing; C_{OUT} 4.7µF**
- Output Disconnect in Shutdown
- 2.75V to 5.5V Input
- <1µA Shutdown Current
- Internal Soft-Start
- Output Overvoltage Protection
- Single Inductor, No Schottky Diodes Required
- Small, Thermally Enhanced 8-Lead (3mm × 3mm) DFN Package

APPLICATIONS

- WCDMA Applications–3G Handsets with High Speed Data Rate Capability
- MP3 Players
- Digital Cameras

DESCRIPTION

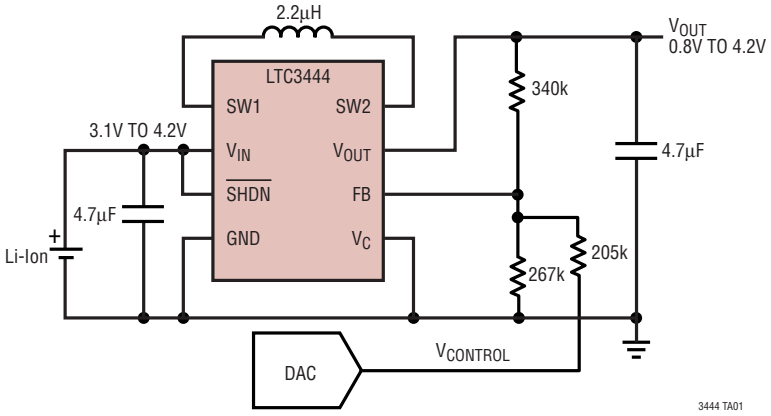
The LTC®3444 is a highly efficient, fixed frequency, buck-boost DC/DC converter, which operates from input voltages above, below, and equal to the output voltage. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for a single Lithium-Ion or multi-cell applications where the output voltage can vary over a wide range.

The LTC3444 has been optimized for use in 3G WCDMA applications. A unique design yields high efficiency at very low output voltages while also eliminating external components. The high speed error amplifier provides the fast transient response required to slew the RF power amplifier from standby to transmit and transmit to stand by power levels. Output overvoltage protection protects the RF power amplifier.

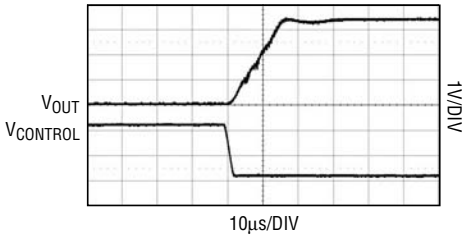
Operating frequency is internally set to 1.5MHz to minimize external component size while maximizing efficiency.

Other features include <1µA shutdown current, internal soft-start, peak current limit and thermal shutdown. The LTC3444 is available in a small, thermally enhanced 8-lead (3mm × 3mm) DFN package.

TYPICAL APPLICATION



LTC3444 Dynamic Response



V_{IN} = 3.6V, V_{OUT} = 0.8V TO 4.2V
$V_{CONTROL}$ = 2.36V TO 0.28V, I_{LOAD} = 100mA

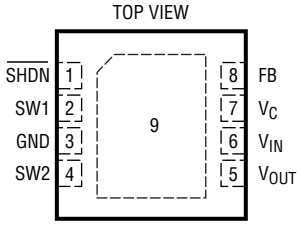
3444 G16a

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN},V_{OUT} Voltages ..... –0.3 to 6V
SW1,SW2 Voltages DC ..... –0.3 to 6V
Pulsed <100ns ..... –0.3 to 7V
$\overline{SHDN}$ Voltage ..... –0.3 to 6V
Operating Temperature (Note 2) ..... –40°C to 85°C
Maximum Junction Temperature (Note 4) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DD PACKAGE
8-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W,
4-LAYER BOARD θ_{JC} = 2.96°C/W
EXPOSED PAD IS GND (PIN 9)
MUST BE SOLDERED TO PCB

ORDER PART NUMBER
LTC3444EDD
DD PART MARKING
LBVZ

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = V_{OUT} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Start-Up Voltage		●	2.55	2.65	2.75	V
Output Voltage Adjust Range		●	0.5		5	V
Feedback Voltage		●	1.19	1.22	1.25	V
Feedback Input Current	V_{FB} = 1.22V			1	50	nA
Quiescent Current - Shutdown	SD = 0V, V_{OUT} = 0V Not Including Switch Leakage			0.1	1	µA
Quiescent Current - Active	(Note 3)			700	1100	µA
NMOS Switch Leakage	Switches B and C			0.1	7	µA
PMOS Switch Leakage	Switches A and D			0.1	10	µA
NMOS Switch On Resistance	Switches B and C			0.19		Ω
PMOS Switch On Resistance	Switches A and D			0.22		Ω
PMOS Switch On Resistance	Switch D V_{IN} = 3.6, V_{OUT} = 1V			0.4		Ω
Input Current Limit		●	2.5	3.5		A
Reverse Current Limit		●	3			A
Max Duty Cycle	Boost (%Switch C On) Buck (% Switch A On)	● ●	70 100	82		% %
Min Duty Cycle		●			0	%
Frequency Accuracy		●	1.2	1.5	1.8	MHz
Error Amp A_{VOL}				65		dB
Error Amp Source Current	V_C = 1.5V, FB = 0V			8		µA
Error Amp Sink Current	V_C = 1.5V, FB = 1.5V			230		µA
Internal Soft-Start Time	$\overline{SHDN}$ Going High			250		µs
Output OV Threshold		●	5.1	5.3	5.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = V_{OUT} = 3.6V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Threshold (On)	IC is Enabled	●	1.4			V
$\overline{SHDN}$ Threshold (Off)	IC is Disabled	●			0.4	V
SHDN Input Current	V_{SHDN} = 3.6V			0.01	1	µA
V_C Output Current	V_C = GND			0.5	2	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

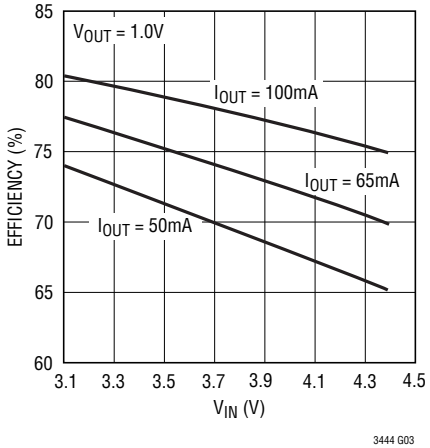
Note 2: The LTC3444E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: Current measurements are performed when the outputs are not switching.

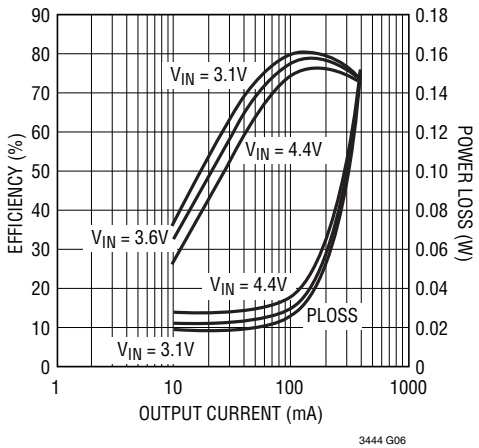
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

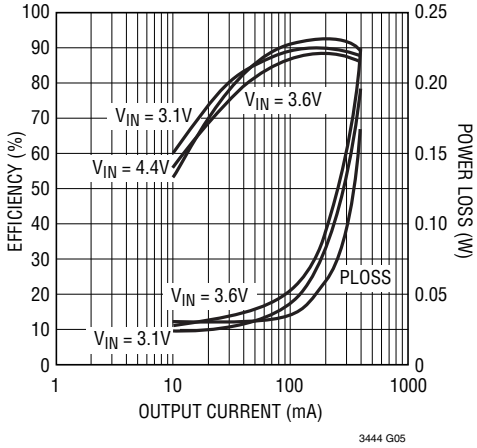
Efficiency vs V_{IN}



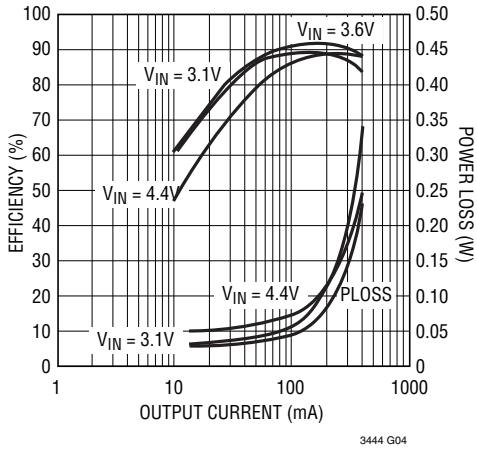
Li-Ion to 1V Efficiency



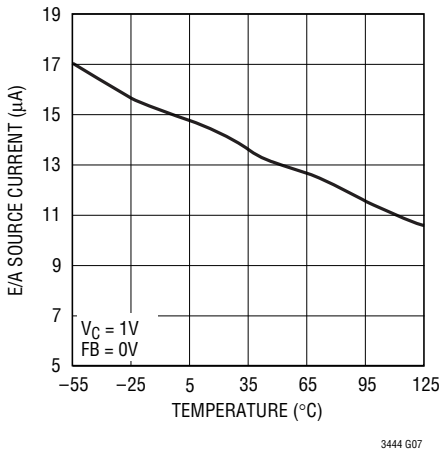
Li-Ion to 3.3V Efficiency



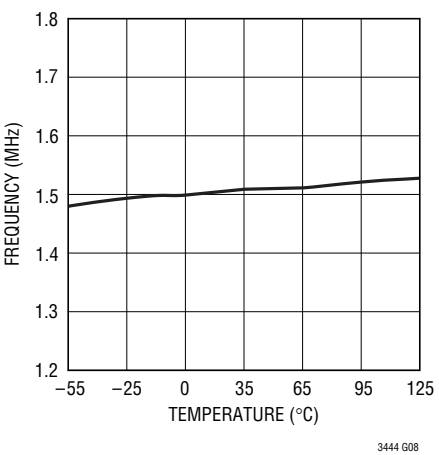
Li-Ion to 4.2V Efficiency



Error Amp Source Current

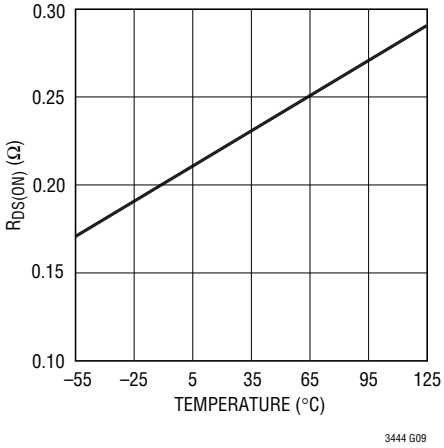


Operating Frequency

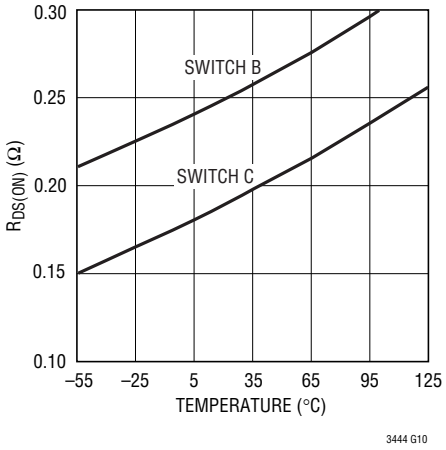


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise specified)

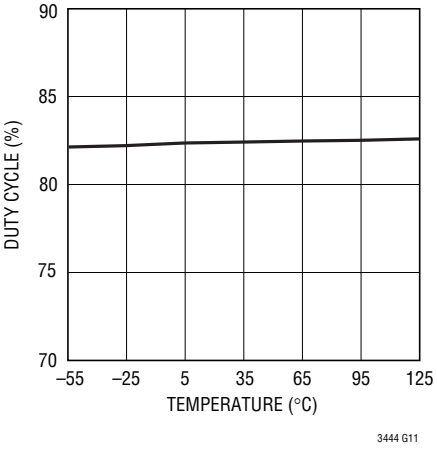
PMOS $R_{DS(ON)}$



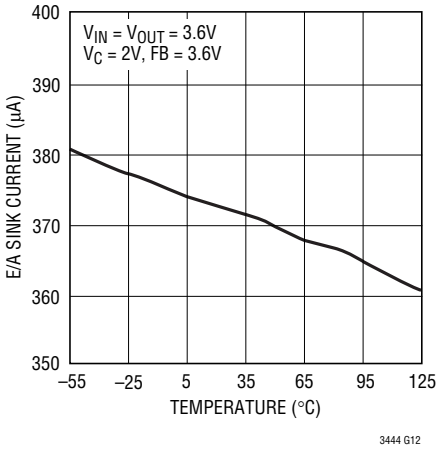
NMOS $R_{DS(ON)}$



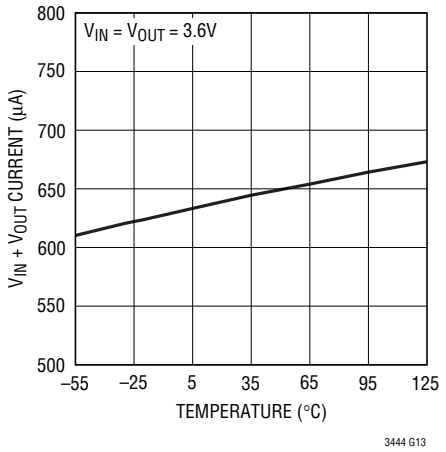
Boost Maximum Duty Cycle



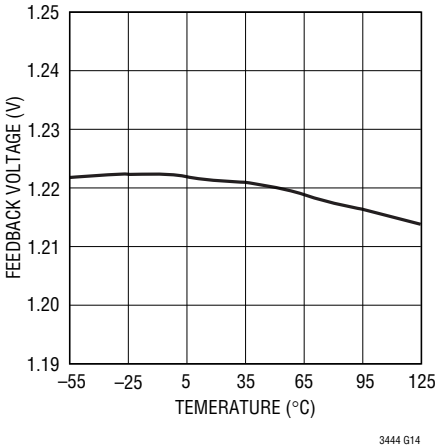
Error Amp Sink Current



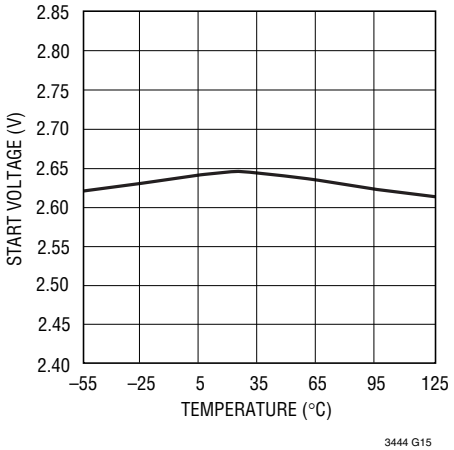
Active Quiescent Current



Feedback Voltage



Minimum Start Voltage



PIN FUNCTIONS

$\overline{SHDN}$ (Pin 1): Shutdown Function. A logic low input shuts down the IC. A logic high input enables the IC and starts the internal soft-start function by limiting the rise time of the internal PWM command.

SW1 (Pin 2): Switch Pin Where the Internal Switches A and B are Connected. Connect inductor from SW1 to SW2. An optional Schottky diode can be connected from ground to SW1 for a moderate efficiency improvement. Minimize trace length to minimize EMI.

GND (Pin 3): Ground Pin for the IC.

SW2 (Pin 4): Switch Pin Where the Internal Switches C and D are Connected. An optional Schottky diode can be connected from SW2 to V_{OUT} for a moderate efficiency improvement. Minimize trace length to keep EMI down.

V_{OUT} (Pin 5): Output of the Synchronous Rectifier. A filter capacitor is placed from V_{OUT} to GND. A ceramic bypass capacitor is recommended as close to the V_{OUT} and GND pins as possible.

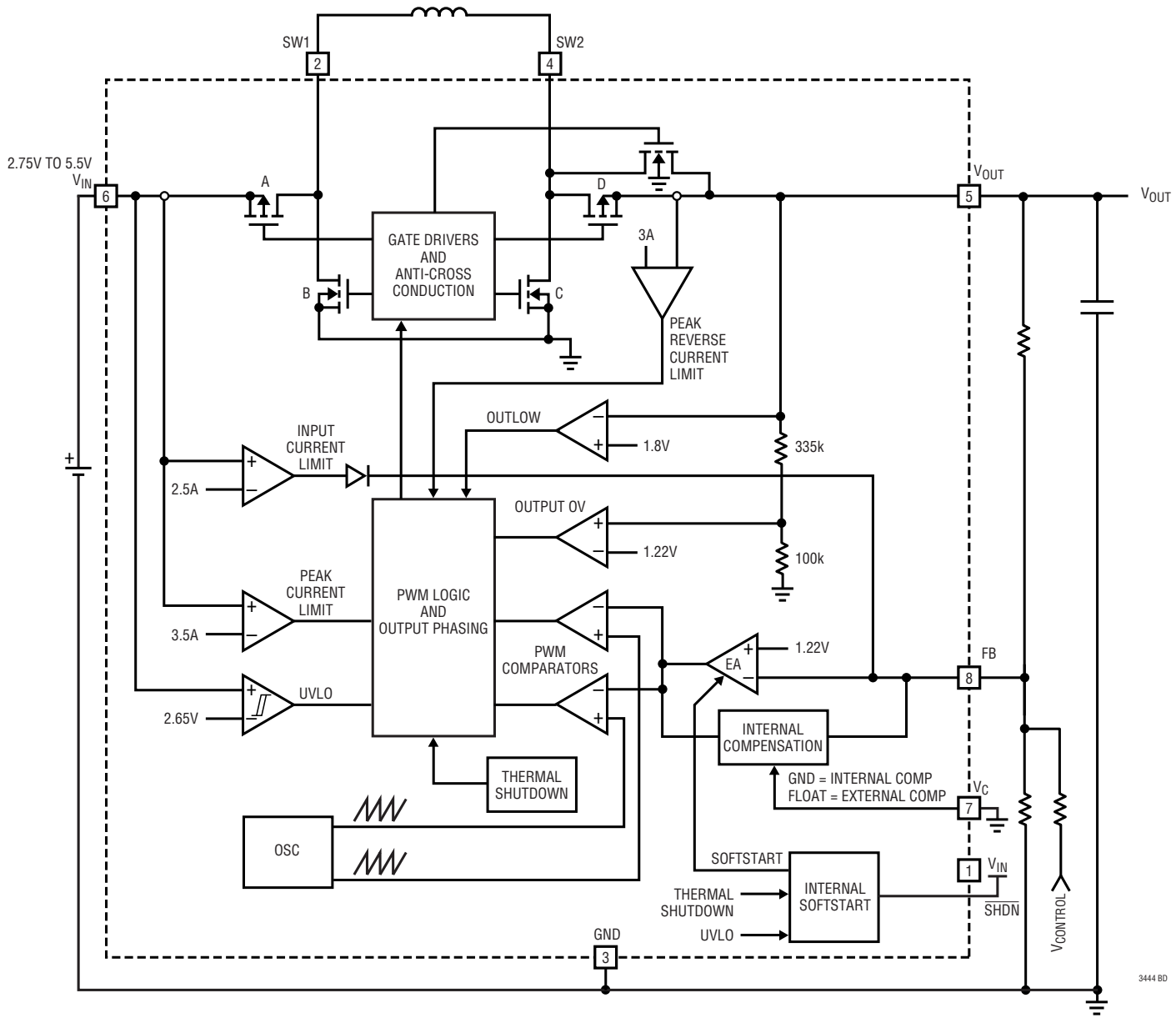
V_{IN} (Pin 6): Input Supply Pin. Internal V_{CC} for the IC. A 4.7µF ceramic capacitor is recommended as close to V_{IN} and GND as possible.

V_C (Pin 7): Error Amp Output. Pull V_C to ground to select internal loop compensation. External compensation may be connected from V_C to FB. Internal compensation will be disabled if V_C is tied to an external compensation network.

FB (Pin 8): Feedback Pin. Connect resistive divider tap here. The output voltage can be adjusted from 0.5V to 5V. The feedback reference voltage is typically 1.22V.

GND (Pin 9, Exposed Pad): Solder to Board GND.

BLOCK DIAGRAM



OPERATION

The LTC3444 is a highly efficient, fixed frequency, buck-boost DC/DC converter, which operates from input voltages above, below, and equal to the output voltage. The topology incorporated in the IC provides a continuous transfer function through all operating modes, making the product ideal for single Lithium-Ion or multi-cell applications where the output voltage can vary over a wide range.

The LTC3444 is designed to provide dynamic voltage control in space constrained 3G WCDMA applications. Due to the high operating frequency and integrated loop compensation a complete WCDMA application requires only six additional components; input and output capacitors (ceramic), an inductor, and three resistors. The high speed error amplifier and integrated loop compensation provide the fast transient response required to slew the RF power amplifier's voltage rail from standby to transmit and transmit to standby levels in < 25µs while minimizing output overshoot or undershoot.

Efficiency under low output voltage conditions (standby mode) is improved by using an N-channel MOSFET in parallel to P-channel MOSFET switch D. This parallel MOSFET eliminates the need for an external Schottky. Output overvoltage protection protects the RF power amplifier from voltages greater than 5.5V.

When used with the proper inductance and output capacitance, the LTC3444 internal compensation is designed to be consistent with the transient requirements of a typical WCDMA application. External compensation can be used with other combinations of inductance and output capacitance, however, the transient response may not be consistent with typical WCDMA requirements.

Output voltage programming is accomplished via a summing resistor input to the feedback resistive divider string. The output voltage varies inversely with the command voltage. When using the internal loop compensation, resistor R1 in the feedback resistive divider string must be 340k. There are no constraints on R1 when using external compensation. However, lower value resistors will decrease the resistance value required for programming the output voltage. Care must be taken not to load down the control voltage source.

OPERATION

Error Amp

The LTC3444 error amplifier is a voltage mode amplifier. The internal loop compensation is designed to optimize transient response to control input change when the proper output L-C and R1 values are used. Refer to Figure 1.

Internal loop compensation is selected by grounding the V_C pin. The loop is designed to exhibit a single pole roll-off (–20dB/dec) with a crossover frequency of ~100KHz. External compensation can be used by connecting the compensation components from FB to V_C. The V_C pin must be allowed to float when using external compensation. If external compensation is used the internal compensation is automatically disabled. A Type III compensation network is typically required to meet the output transient requirements of WCDMA.

During start-up, the ramp rate of the error amp output is controlled to provide a soft-start function. Refer to Figure 2.

Internal Current Limit

There are two different current limit circuits in the LTC3444. The two circuits have internally fixed thresholds.

The first circuit sources current out of the FB pin to drop the output voltage once the peak input current exceeds 2.5A minimum. During conditions where V_{OUT} is near ground, such as during a short circuit or during startup, this threshold is cut in half, providing current foldback protection.

The second circuit is a high-speed peak current limit amplifier that shuts off P-channel MOSFET switch A if the input current exceeds 3.5A typical. The delay to output for this amplifier is typically 50ns.

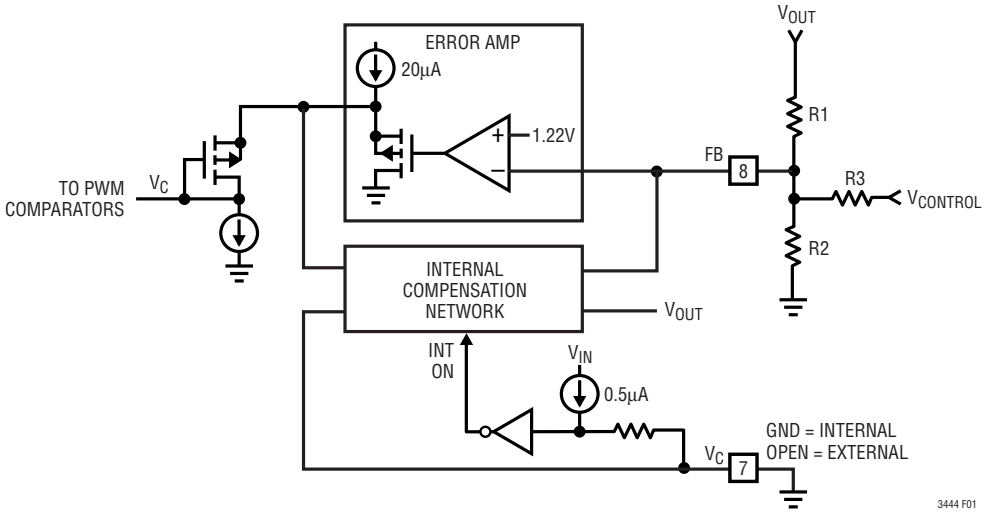


Figure 1. Error Amplifier with Compensation Select Function

OPERATION

Reverse Current Limit

The LTC3444 always operates in forced continuous conduction mode. The reverse current limit amplifier monitors the inductor current from the output through switch D. Once the negative inductor current exceeds 3A minimum, the LTC3444 will shut off switch D. The high reverse current is required to meet the transient slew requirements for WCDMA power amplifiers.

Output Overvoltage Protection

The LTC3444 provides output overvoltage protection. If the output voltage exceeds 5.3V typical, P-channel MOSFET switches A and D are turned off and N-channel MOSFET switches B and C are turned on. Normal switching will resume once the output voltage drops below ~5.1V. If the condition which caused the output overvoltage is still present the output will charge up to 5.3V again and the overvoltage cycle will be repeat. Normal output regulation will resume once the condition responsible for the output overvoltage is removed.

Soft-Start

The soft-start function is initiated when the $\overline{SHDN}$ pin is brought above 1.4V and the LTC3444 is out of UVLO (above minimum input operating specs). The LTC3444 is enabled but the PWM duty cycle is clamped via the error amp output. The soft-start time is internally set to 250µs to minimize output overshoot. A detailed diagram of this function is shown in Figure 2.

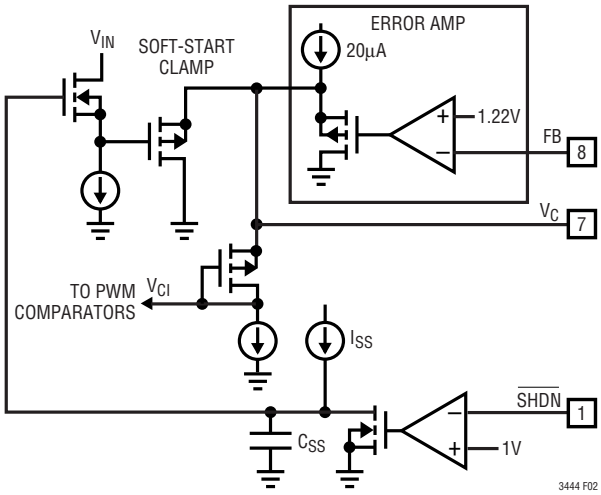


Figure 2. Soft-Start Circuitry

OPERATION

Buck-Boost Four-Switch Control

Figure 3 shows a simplified diagram of how the four internal switches are connected to the inductor, V_{IN}, V_{OUT} and GND. Figure 4 shows the regions of operation for the LTC3444 as a function of the internal control voltage, V_{CI}. Depending on the control voltage, the LTC3444 will operate in either buck, buck-boost or boost mode. The V_{CI} voltage is a level shifted voltage from the output of the error amp (V_C pin) (see Figure 2). The four power switches are properly phased so the transfer between operating modes is continuous, smooth and transparent to the user. The buck-boost region is reached when V_{IN} approaches V_{OUT}. The conduction time of the four switch region is typically 125ns. The three operating modes of the four switch buck-boost converter are described below. Please refer to Figures 3 and 4.

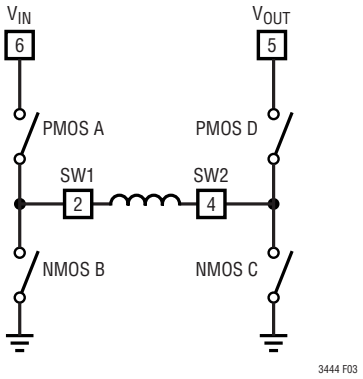


Figure 3. Simplified Diagram of Output Switches

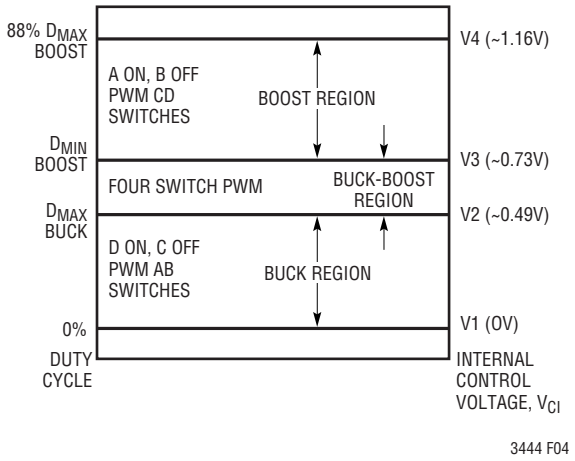


Figure 4. Switch Control vs Internal Control Voltage, V_{CI}

OPERATION

Buck Region ($V_{IN} > V_{OUT}$)

Switch D is always on and switch C is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V1, Switch A is on. During the off time of switch A, synchronous switch B turns on for the remainder of the time. Switches A and B will alternate similar to a typical synchronous buck regulator. As the control voltage increases, the duty cycle of switch A increases until the maximum duty cycle of the converter in buck mode reaches DMAX_BUCK, given by:

$$DMAX\_BUCK = 100\% - D4_{SW}$$

where $D4_{SW}$ = duty cycle % of the four switch range.

$$D4_{SW} = (125ns \bullet f) \bullet 100\ \%$$

where f = operating frequency, Hz.

Beyond this point the "four switch," or Buck-Boost region is reached.

Buck-Boost or Four Switch ($V_{IN} \sim V_{OUT}$)

When the internal control voltage, V_{CI}, is above voltage V2, but below V3, switch pair AD remain on for duty cycle DMAX_BUCK, and the switch pair AC begins to phase in. As switch pair AC phases in, switch pair BD phases out accordingly. When the V_{CI} voltage reaches the edge of the buck-boost range, at voltage V3, the AC switch pair completely phase out the BD pair, and the boost phase begins at duty cycle $D4_{SW}$. The input voltage, V_{IN}, where the four switch region begins is given by:

$$V_{IN} = \frac{V_{OUT}}{1-(125ns \bullet f)} V$$

The point at which the four switch region ends is given by:

$V_{IN} = V_{OUT}(1–D) = V_{OUT}(1–125ns \bullet f)$ V

OPERATION

Boost Region ($V_{IN} < V_{OUT}$)

Switch A is always on and switch B is always off during this mode. When the internal control voltage, V_{CI}, is above voltage V3, switch pair CD will alternately switch to provide a boosted output voltage. This operation is typical to a synchronous boost regulator. The maximum duty cycle of the converter is limited to 82% typical and is reached when V_{CI} is above V4.

CONTROLLING THE OUTPUT VOLTAGE

The output voltage is controlled via a summing resistor input at the feedback (FB) resistive divider string. Refer to Figure 1. The output voltage has an inverse relation to the control voltage as shown in Figure 5. The resistor values are dependent on the desired output voltage range and the control voltage range. When using the internal loop compensation, V_C = GND, **R1 must be 340k.** For external compensation R1 should be chosen first and R2 and R3 calculated from the following equations.

The resistor values are given by:

$$R3 = \frac{(V_{CON(MAX)} - V_{CON(MIN)})}{V_{O(MAX)} - V_{O(MIN)}} \bullet R1\,\Omega$$

$$R2 = \frac{1.22}{\frac{(V_{CON(MAX)} - 1.22)}{R3} - \frac{(1.22 - V_{O(MIN)})}{R1}}\,\Omega$$

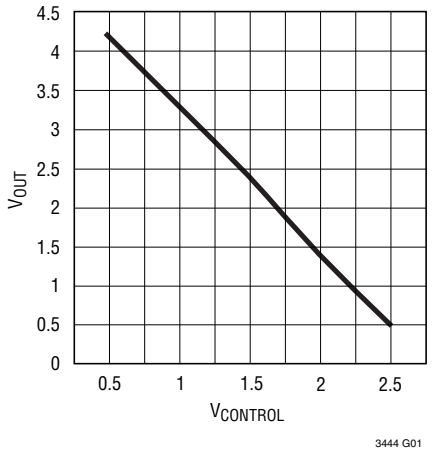


Figure 5. V_{OUT} vs $V_{CONTROL}$ with R1 = 340k, R2 = 249k, and R3 = 182k, $V_{CONTROL}$ = 0.5V to 2.5V

OPERATION

Table 1. Shows some typical resistor value combinations for several $V_{CONTROL}$ vs V_{OUT} voltage ranges. One percent (1%) resistor tolerances were assumed.

Table 1. Typical Resistor Values for V_{OUT} vs $V_{CONTROL}$

$V_{CONTROL}$(V)		V_{OUT} (V)		RESISTANCE (kΩ)		
MIN	MAX	MIN	MAX	R1	R2	R3
0.35	2.4	0.8	4.2	340	271	205
0.35	2.5	0.5	5.0	340	210	162
0.8	2.35	0.8	4.2	340	200	154
0.5	2.5	0.5	4.2	340	249	182

COMPONENT SELECTION

Recommended Component Placement

Figure 6. Shows a recommended component placement. Traces carrying high current should be made short and wide. Trace area at FB and V_C pins should be minimized. Lead lengths to the battery should be kept short. V_{OUT} and V_{IN} ceramic capacitors should be placed close to the IC pins. Multiple vias should be used between layers.

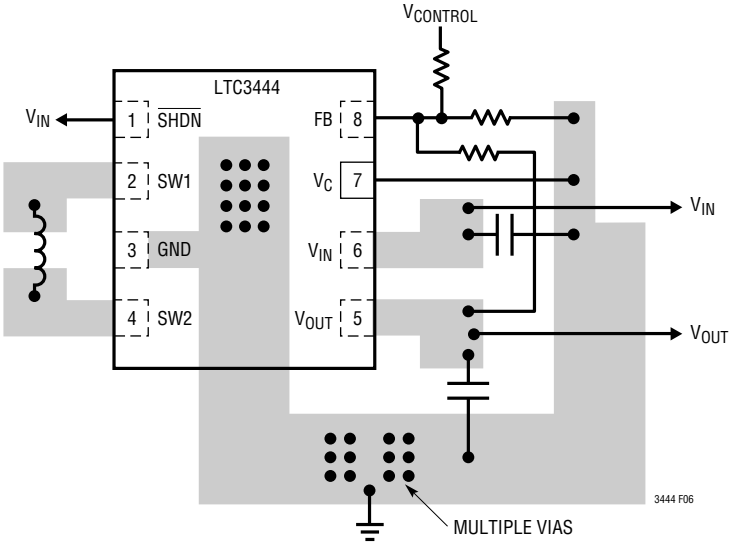


Figure 6. Recommended Component Placement

OPERATION

Inductor Selection

The high frequency operation of the LTC3444 allows the use of small surface mount inductors. The internal loop compensation is designed to work with a 2.2µH inductor (1.5µH for V_{IN} < 3.1V). The 2.2µH inductor was selected to optimize the transient response to the control input. The use of a 2.2µH inductor pushes out the right half plane (RHP) zero frequency and allows the loop crossover to occur at frequencies higher than the output L-C double pole.

For external compensation the inductor selection is based on the desired inductor ripple current. The inductor ripple current is typically set to 20% to 40% of the average inductor current. Increased inductance results in lower ripple current, however, higher inductance pulls in the RHP zero frequency and limits the maximum crossover frequency possible. Refer to Closing the Feedback Loop for more information on the RHP zero. For a given ripple the inductance terms are given as follows:

$$L_{BOOST} > \frac{V_{IN(MIN)} \bullet (V_{OUT} - V_{IN(MIN)})}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L \bullet V_{OUT}} H$$

$$L_{BUCK} > \frac{V_{OUT} \bullet (V_{IN(MAX)} - V_{OUT})}{f \bullet I_{OUT(MAX)} \bullet \Delta I_L \bullet V_{IN(MAX)}} H$$

where f = operating frequency, Hz

ΔI_L = inductor ripple current, A

$V_{IN(MIN)}$ = minimum input voltage, V

$V_{IN(MAX)}$ = maximum input voltage, V

V_{OUT} = output voltage, V

$I_{OUT(MAX)}$ = maximum output load current

In most cases, the boost configuration will be used to determine the minimum inductance allowed for a given ripple current.

For high efficiency, choose a ferrite inductor with a high frequency core material to reduce core loses. The inductor should have low ESR (equivalent series resistance) to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a shielded inductor. See Table 2 for a suggested list of inductor suppliers.

Table 2. Inductor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
Coilcraft	(847) 639-6400	(847) 639-1469	www.coilcraft.com
CoEv Magnetics	(800) 227-7040	(650) 361-2508	www.circuitprotection.com/magnetics.asp
COOPER Bussmann	(636) 394-2877	1-800-544-2570	www.coooperET.com
Murata	(814) 237-1431 (800) 831-9172	(814) 238-0490	www.murata.com
Sumida	USA: (847) 956-0666 Japan: 81(3) 3607-5111	USA: (847) 956-0702 Japan: 81(3) 3607-5144	www.sumida.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com
TOKO	(847) 297-0070	(847) 699-7864	www.tokoam.com

OPERATION

Output Capacitor Selection

A 4.7µF, X5R or X7R type ceramic capacitor should be used when using the internal loop compensation. When using external compensation, larger values of output capacitance can be used, however, larger output capacitance will increase the time needed to slew the output voltage as required in typical WCDMA applications. The bulk value of the output filter capacitor is set to reduce the ripple due to charge into the capacitor each cycle. The steady state ripple due to charge is given by:

$$\%RIPPLE\_BOOST = \frac{I_{OUT} \bullet (V_{OUT} - V_{IN(MIN)}) \bullet 100}{C_{OUT} \bullet V_{OUT}^{2} \bullet f}\%$$

$$\%RIPPLE\_BUCK = \frac{I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) \bullet 100}{C_{OUT} \bullet V_{IN(MAX)} \bullet V_{OUT} \bullet f}\%$$

where C_{OUT} = output filter capacitor in farads
f = switching frequency in Hz.

In a typical application the output capacitance may be many times larger than that calculated above in order to handle the transient load response requirements of the converter. For a rule of thumb, the ratio of the operating frequency to the unity-gain bandwidth of the converter is the amount the output capacitance will have to increase from the above calculations in order to maintain the desired transient response. However, in WCDMA applications the output capacitance should be kept at a minimum to maximize the output slew rate. Refer to the Loop Compensation Networks section of this datasheet.

The other component of ripple is due to the ESR (equivalent series resistance) of the output capacitor. Low ESR capacitors should be used to minimize output voltage ripple. For surface mount applications, Taiyo Yuden or TDK ceramic capacitors, AVX TPS series tantalum capacitors or Sanyo POSCAP are recommended. See Table 3 for contact information.

Ceramic output capacitors should use case size 1206 or larger. Smaller case sizes have a larger voltage coefficient that can greatly reduce the output capacitance value at higher output voltages.

Input Capacitor Selection

Since the V_{IN} pin is the supply voltage for the LTC3444, as well as the input to the power stage of the converter, it is recommended to place at least a 4.7µF, X5R or X7R ceramic bypass capacitor close to the V_{IN} and GND pins. It is also important to minimize any stray resistance from the converter to the battery or other power source.

Table 3. Capacitor Vendor Information

SUPPLIER	PHONE	FAX	WEB SITE
AVX	(803) 448-9411	(803) 448-1943	www.avxcorp.com
Sanyo	(619) 661-6322	(619) 661-1055	www.sanyovideo.com
Taio Yuden	(408) 573-4150	(408) 573-4159	www.t-yuden.com
TDK	(847) 803-6100	(847) 803-6296	www.component.tdk.com

OPERATION

Optional Schottky Diodes

Schottky diodes across the synchronous switches B and D are not required, but provide a lower drop during the break-before-make time (typically 15ns) of the NMOS to PMOS transition, improving efficiency. Use a surface mount Schottky diode such as an MBRM120T3 or equivalent. Do not use ordinary rectifier diodes, since the slow recovery times will compromise efficiency.

Closing the Feedback Loop

The LTC3444 incorporates voltage mode PWM control. The control to output gain varies with operation region (buck, boost, buck-boost), but is usually ~20dB. The output filter exhibits a double pole response, as given by:

$$f_{FILTER\_POLE} = \frac{1}{2 \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

(in buck mode)

$$f_{FILTER\_POLE} = \frac{V_{IN}}{2 \bullet V_{OUT} \bullet \pi \bullet \sqrt{L \bullet C_{OUT}}} Hz$$

(in boost mode)

where L is in Henries and C_{OUT} is in farads.

The output filter zero is given by:

$$f_{FILTER\_ZERO} = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}} Hz$$

where R_{ESR} is the equivalent series resistance of the output cap.

A troublesome problem when operating in boost mode is dealing with the right-half plane zero (RHP), given by:

$$f_{RHPZ} = \frac{V_{IN}^2}{2 \bullet \pi \bullet I_{OUT} \bullet L \bullet V_{OUT}} Hz$$

The RHP zero has a +20dB/dec gain typical of a zero but the –90° phase lag of a pole. This causes the loop gain to flatten out while the phase margin decreases. The only way to combat a RHP zero is to roll off the loop well before the RHP zero frequency.

LOOP COMPENSATION NETWORKS

A simple Type I compensation network, refer to Figure 7, can be incorporated to stabilize the loop, but at a cost of reduced bandwidth and slower transient response. To ensure proper phase margin using Type I compensation, the loop must be crossed over at least a decade before the output LC double pole frequency. The unity-gain frequency of the error amplifier with the Type I compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C2} Hz$$

WCDMA applications demand an improved transient response to the input control voltage. In other applications, the output capacitor can be increased to meet help meet the load transient requirements.

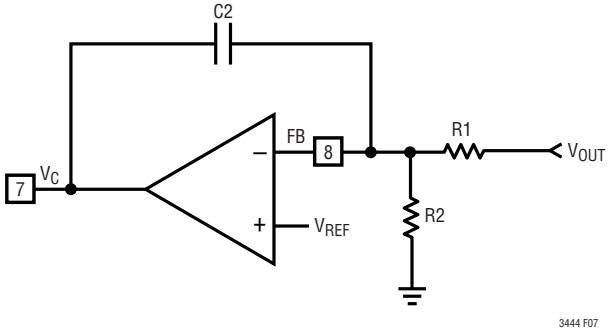


Figure 7. Error Amplifier with Type I Compensation

OPERATION

However, due to the output voltage slewing requirements found in WCDMA applications the output filter capacitor must be minimized. To maximize the transient response, while minimizing the output capacitance, a higher bandwidth, Type III compensation is required. A Type III compensation network, refer to Figure 8, has a double zero to cancel the double pole of the output LC filter and a double pole to compensate for the ESR zero and RHP zero of the boost topology. In addition to the double poles, the Type III network also has a single pole at DC. The Type III compensation provides a maximum 135° phase boost and allows the loop crossover to occur at frequencies higher than the output LC. Refer to Figure 9. Referring to Figure 8, the location of the poles and zeros are given by: Assume $C_2 >> C_3$, $R_1 >> R_4$.

$$f_{POLE1} \cong \frac{1}{2 \bullet \pi \bullet R5 \bullet C3} Hz$$

$$f_{POLE2} = \frac{1}{2 \bullet \pi \bullet R4 \bullet C1} Hz$$

$$f_{ZERO1} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C1} Hz$$

$$f_{ZERO2} = \frac{1}{2 \bullet \pi \bullet R5 \bullet C2} Hz$$

And the unity gain frequency (f_{UG}) of the Type III compensation is given by:

$$f_{UG} = \frac{1}{2 \bullet \pi \bullet R1 \bullet C2} Hz$$

where resistance is in ohms and capacitance is in farads. Note: Bias resistor, R2, does not affect the Pole/Zero placement.

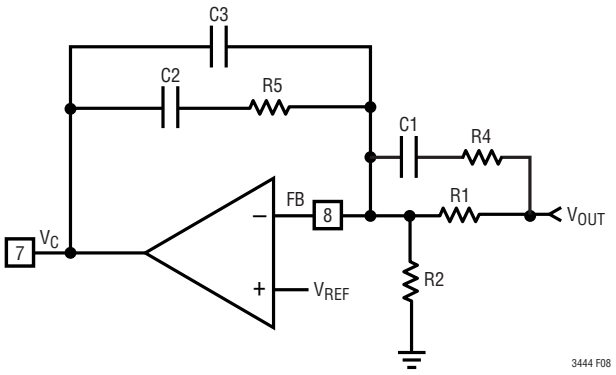


Figure 8, Error Amplifier with Type III Compensation

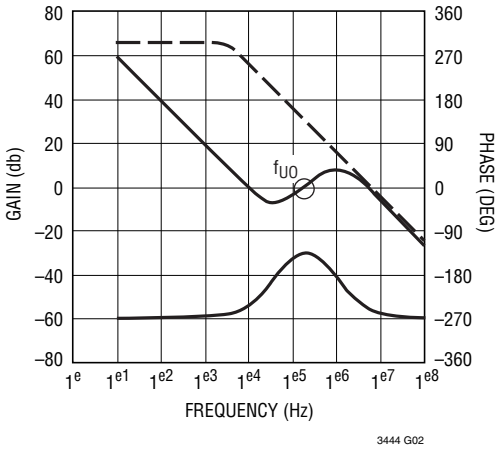
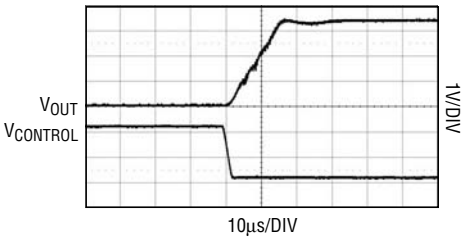


Figure 9. Frequency Response for LTC3444 Error Amplifier with a Typical Type III Compensation Network

TYPICAL APPLICATIONS

Example of Internal Compensation Transient Response for a Command Voltage Change

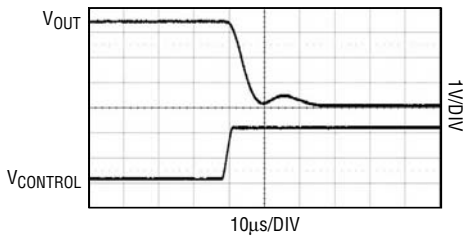
LTC3444 Dynamic Response



V_{IN} = 3.6V, V_{OUT} = 0.8V TO 4.2V
$V_{CONTROL}$ = 2.36V TO 0.28V, I_{LOAD} = 100mA

3444 G16a

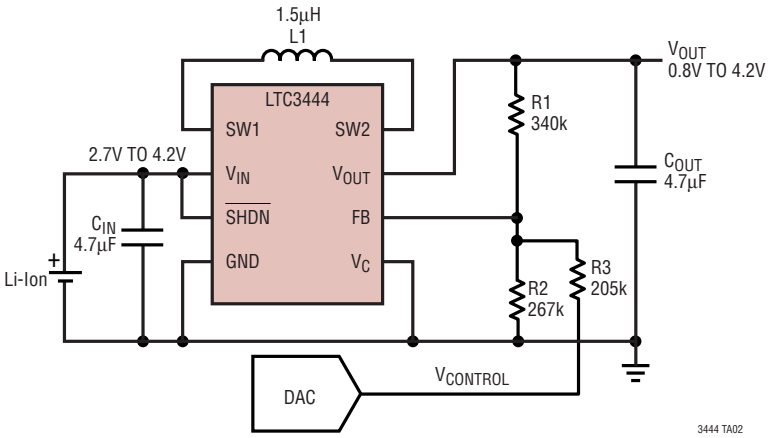
LTC3444 Dynamic Response



V_{IN} = 3.6V, V_{OUT} = 4.2V TO 0.8V
$V_{CONTROL}$ = 0.28V TO 2.36V, I_{LOAD} = 100mA

3444 G17

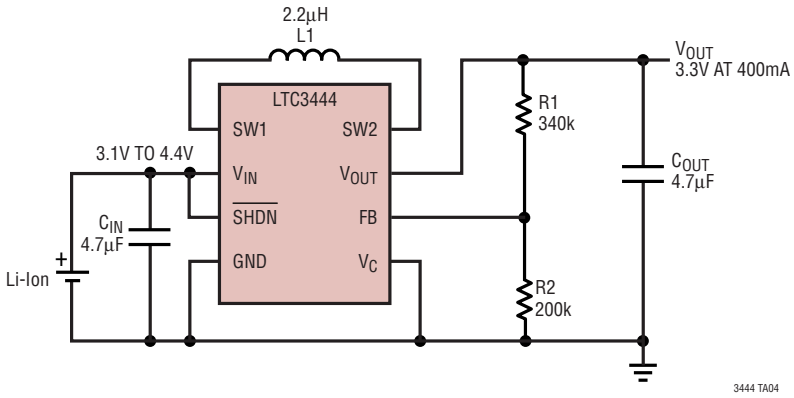
Internally Compensated WCDMA Application. Singe Cell, 2.7V to 4.2V Input, 0.8V to 4.2V at 400mA Output.



C_{IN} = MURATA:GRM31CR61C475K
C_{OUT} = MURATA:GRM31CR61C475K
L1 = COOPER BUSSMAN SD12-2R2

TYPICAL APPLICATIONS

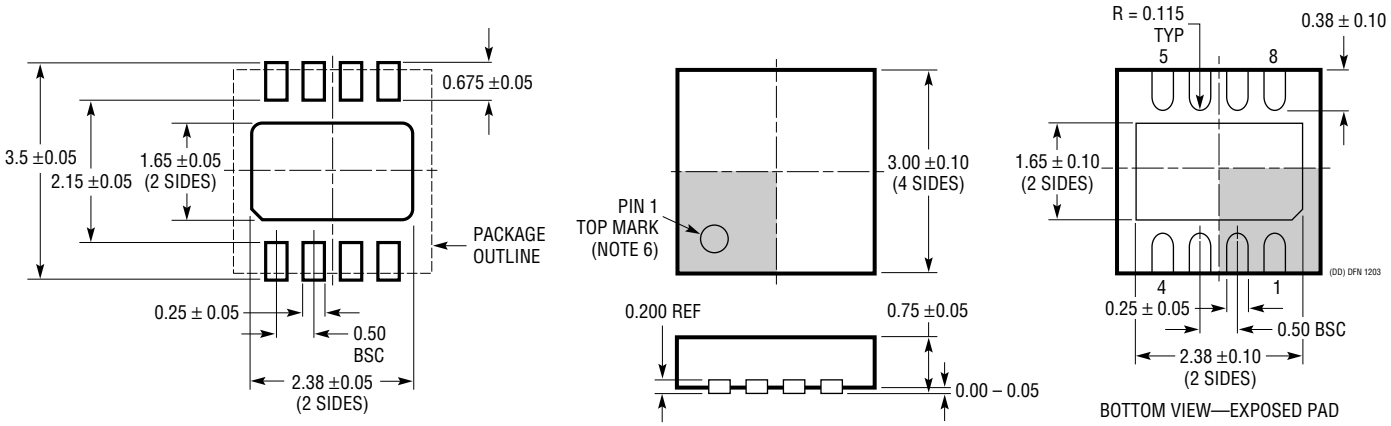
Single Li-Ion, 3.1V to 4.2V Input, 3.3V at 400mA Output with Internal Compensation



C_{IN} = MURATA:GRM31CR61C475K
C_{OUT} = MURATA:GRM31CR61C475K
L1 = COOPER BUSSMAN SD12-2R2

PACKAGE DESCRIPTION

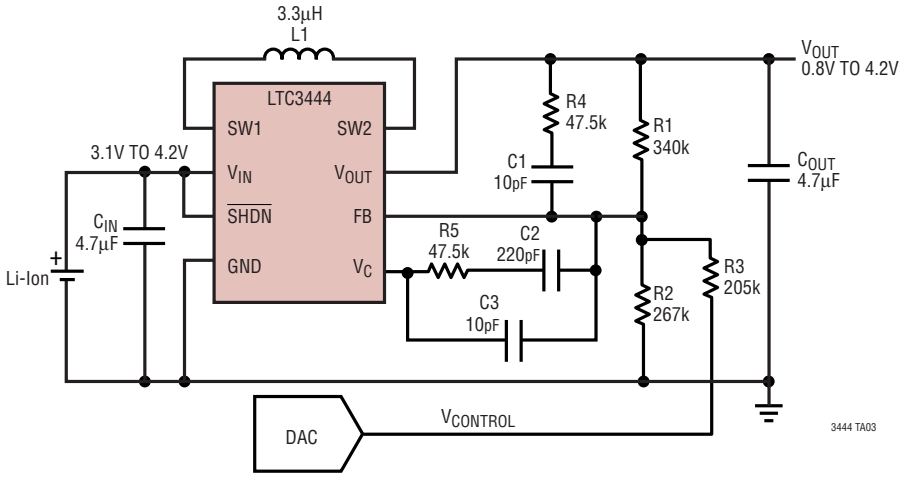
DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)



NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Externally Compensated WCDMA Application. Singe Cell, 3.1V to 4.2V Input, 0.8V to 4.2V at 400mA Output.



C_{IN} = MURATA:GRM31CR61C475K
C_{OUT} = MURATA:GRM31CR61C475K
L1 = COOPER BUSSMAN SD12-3R3

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3403	1.5MHz, 600mA, Synchronous Step-Down Regulator with Bypass Transistor	96% Efficiency, V_{IN}: 2.5V to 5V, V_{OUT}: 0.3V to 3.5V, I_{SD} <1µA, (3mm × 3mm) DFN Package
LTC3408	1.5MHz, 600mA, Synchronous Step-Down Regulator with Bypass Transistor	96% Efficiency, V_{IN}: 2.5V to 5V, V_{OUT}: 0.3V to 3.5V, I_{SD} <1µA, (3mm × 3mm) DFN Package
LTC3440	Up to 2MHz, 600µA, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_{SD} <1µA, I_Q = 25µA, 10-Lead MS Package
LTC3441	1MHz, 1.2A, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V $V_{OUT(MIN)}$ = 2.5V, I_{SD} <1µA, I_Q = 25µA, 12-Lead (4mm × 3mm) DFN Package
LTC3442	Up to 2MHz, 1.2A, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_{SD} <1µA, I_Q = 25µA, 12-Lead (4mm × 3mm) DFN Package
LTC3443	600MHz, 1.2A Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_{SD} <1µA, I_Q = 25µA, 12-Lead (4mm × 3mm) DFN Package

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