LTC3371

4-Channel 8A Configurable Buck DC/DCs with Watchdog and Power-On Reset

FEATURES

- **8 × 1A Buck Power Stages Configurable as 2, 3 or 4 Output Channels**
- **8 Unique Output Configurations (1A to 4A Per Channel)**
- **Independent V_{IN} Supplies for Each DC/DC (2.25V to 5.5V)**
- **Low Total No Load Supply Current:**
  - **15µA In Shutdown (All Channels Off)**
  - **68µA One Channel Active in Burst Mode® Operation**
  - **18µA Per Additional Channel**
- **Precision Enable Pin Thresholds for Autonomous Sequencing**
- 1MHz to 3MHz RT Programmable Frequency (2MHz Default) or PLL Synchronization
- Temp Monitor Indicates Die Temperature
- CT Programmed Watchdog Timer
- Independent $\overline{RST}$ Pins Indicate Buck in Regulation
- Thermally Enhanced 38-Lead 5mm × 7mm QFN and TSSOP Packages

APPLICATIONS

- General Purpose Multichannel Power Supplies: Automotive, Industrial, Distributed Power Systems

DESCRIPTION

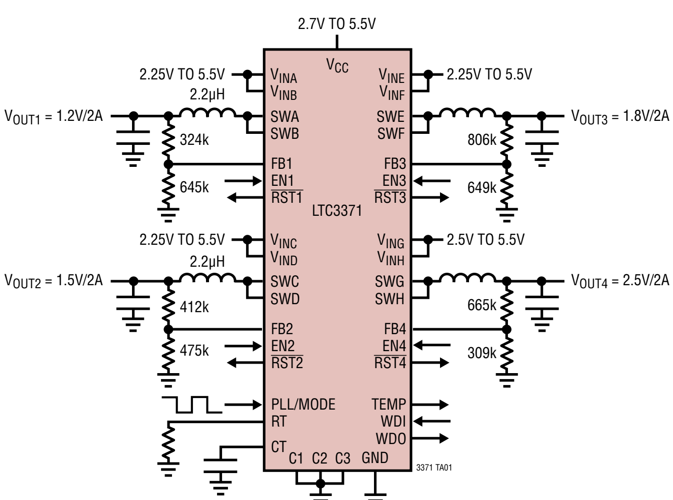
The LTC®3371 is a highly flexible multioutput power supply IC. The device includes four synchronous buck converters, configured to share eight 1A power stages, each of which is powered from independent 2.25V to 5.5V inputs.

The DC/DCs are assigned to one of eight possible power configurations via pin programmable C1-C3 pins. The common buck switching frequency may be programmed with an external resistor, synchronized to an external oscillator, or set to a default internal 2MHz clock. The operating mode for all DC/DCs may be programmed for Burst Mode or forced continuous mode operation.

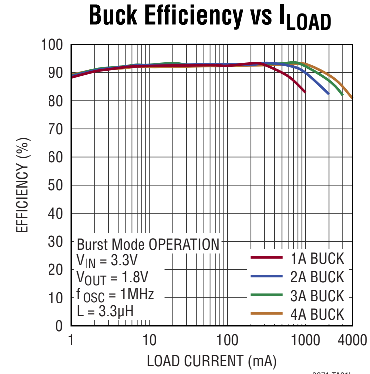
The CT pin programs the timing parameters of four independent $\overline{RST}$ pins as well as the watchdog timer.

To reduce input noise, the buck converters are phased in 90° steps. Precision enable pin thresholds facilitate reliable power sequencing. The LTC3371 is available in low profile 38-lead 5mm × 7mm QFN and TSSOP packages.

TYPICAL APPLICATION



Buck Efficiency vs I_{LOAD}



C3	C2	C1	BUCK1	BUCK2	BUCK3	BUCK4
0	0	0	2A	2A	2A	2A
0	0	1	3A	1A	2A	2A
0	1	0	3A	1A	1A	3A
0	1	1	4A	1A	1A	2A
1	0	0	3A	2A	–	3A
1	0	1	4A	–	2A	2A
1	1	0	4A	–	1A	3A
1	1	1	4A	–	–	4A

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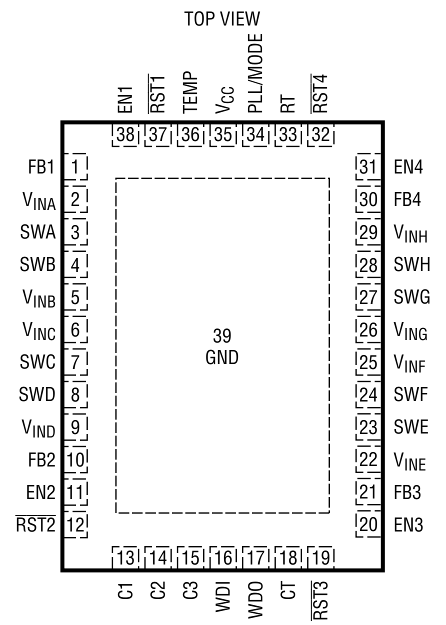
ABSOLUTE MAXIMUM RATINGS (Note 1)

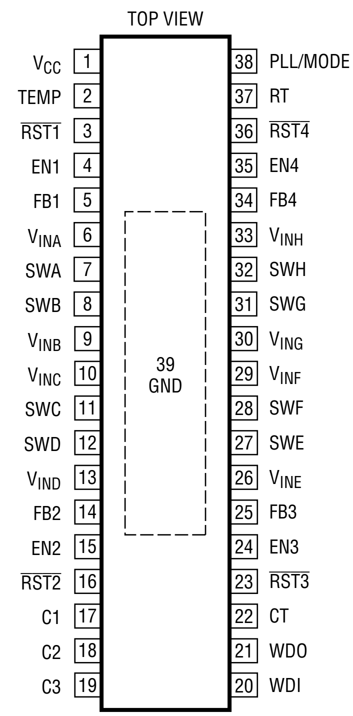
V_{INA-H}, FB1-4, EN1-4, V_{CC}, CT, WDI, WDO, $\overline{RST1-4}$,
RT, PLL/MODE, C1-3 .... –0.3V to 6V
TEMP .... –0.3V to Lesser of (V_{CC} + 0.3V) or 6V
$I_{\overline{RST1-4}}$, I_{WDO} 5mA

Operating Junction Temperature Range
(Notes 2, 3) .... –40°C to 150°C
Storage Temperature Range .... –65°C to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
38-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION http://www.linear.com/product/LTC3371#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3371EUHF#PBF	LTC3371EUHF#TRPBF	3371	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3371IUHF#PBF	LTC3371IUHF#TRPBF	3371	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3371HUHF#PBF	LTC3371HUHF#TRPBF	3371	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 150°C
LTC3371EFE#PBF	LTC3371EFE#TRPBF	LTC3371FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3371IFE#PBF	LTC3371IFE#TRPBF	LTC3371FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3371HFE#PBF	LTC3371HFE#TRPBF	LTC3371FE	38-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{CC} = $V_{INA\text{-}H}$ = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	V_{CC} Voltage Range		●	2.7		5.5	V
$V_{CC(UVLO)}$	Undervoltage Threshold on V_{CC}	V_{CC} Voltage Falling V_{CC} Voltage Rising	● ●	2.325 2.425	2.45 2.55	2.575 2.675	V V
$I_{VCC(ALLOFF)}$	V_{CC} Input Supply Current	All Switching Regulators in Shutdown			15	25	µA
I_{VCC}	V_{CC} Input Supply Current	One Buck Active PLL/MODE = 0V, R_T = 400k, V_{FB_BUCK} = 0.85V PLL/MODE = 2MHz			 50 175	 75 250	 µA µA
f_{OSC}	Internal Oscillator Frequency	V_{RT} = V_{CC}, PLL/MODE = 0V V_{RT} = V_{CC}, PLL/MODE = 0V R_T = 400k, PLL/MODE = 0V	 ● ●	1.8 1.75 1.8	2 2 2	2.2 2.25 2.2	MHz MHz MHz
$f_{PLL/MODE}$	Synchronization Frequency	t_{LOW}, t_{HIGH} > 60ns	●	1		3	MHz
$V_{PLL/MODE}$	PLL/MODE Level High PLL/MODE Level Low	For Synchronization For Synchronization	● ●	1.2 		 0.4	V V
V_{RT}	RT Servo Voltage	R_T = 400k	●	780	800	820	mV
Temp Monitor							
$V_{TEMP(ROOM)}$	TEMP Voltage at 25°C			180	220	260	mV
ΔV_{TEMP}/°C	V_{TEMP} Slope				7		mV/°C
OT	Overtemperature Shutdown				170		°C
OT Hyst	Overtemperature Hysteresis				10		°C
1A Buck Regulators							
V_{IN}	Buck Input Voltage Range		●	2.25		5.5	V
V_{OUT}	Buck Output Voltage Range		●	V_{FB}		V_{IN}	V
$V_{IN(UVLO)}$	Undervoltage Threshold on V_{IN}	V_{IN} Voltage Falling V_{IN} Voltage Rising	● ●	1.95 2.05	2.05 2.15	2.15 2.25	V V
I_{VIN}	Burst Mode Operation Input Current Forced Continuous Mode Operation Input Current Shutdown Input Current	V_{FB} = 0.85V (Note 4) $I_{SW(BUCK)}$ = 0µA, FB = 0V			18 400 0	30 600 2.5	µA µA µA
I_{FWD}	PMOS Current Limit	(Note 5)		1.9	2.3	2.7	A
V_{FB1}	Feedback Regulation Voltage for Buck 1		●	792	800	808	mV
V_{FB}	Feedback Regulation Voltage for Bucks 2-4		●	780	800	820	mV
I_{FB}	Feedback Leakage Current	V_{FB} = 0.85V		–50		50	nA
D_{MAX}	Maximum Duty Cycle	V_{FB} = 0V	●	100			%
R_{PMOS}	PMOS On-Resistance	I_{SW} = 100mA			300		mΩ
R_{NMOS}	NMOS On-Resistance	I_{SW} = –100mA			240		mΩ
I_{LEAKP}	PMOS Leakage Current	EN = 0		–2		2	µA
I_{LEAKN}	NMOS Leakage Current	EN = 0		–2		2	µA
t_{SS}	Soft-Start Time				1		ms
$V_{PGOOD(FALL)}$	Falling PGOOD Threshold for Buck 1	% of Regulated V_{FB}		96.8	98	99.2	%
	Falling PGOOD Threshold for Bucks 2 to 4	% of Regulated V_{FB}		93	95	97	%
$V_{PGOOD(HYS)}$	PGOOD Hysteresis for Bucks 1 to 4	% of Regulated V_{FB}			0.3		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{CC} = V_{INA-H} = 3.3V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Buck Regulators Combined							
I_{FWD2}	PMOS Current Limit	2 Buck Power Stages Combined (Note 5)			4.6		A
I_{FWD3}	PMOS Current Limit	3 Buck Power Stages Combined (Note 5)			6.9		A
I_{FWD4}	PMOS Current Limit	4 Buck Power Stages Combined (Note 5)			9.2		A
Interface Logic Pins ($\overline{RST1-4}$, WDO, WDI, PLL/MODE, C1, C2, C3)							
I_{OH}	Output High Leakage Current	$\overline{RST1-4}$, WDO 5.5V at Pin				1	µA
V_{OL}	Output Low Voltage	$\overline{RST1-4}$, WDO 3mA into Pin			0.1	0.4	V
V_{IH}	WDI Input High Threshold		●	1.2			V
V_{IL}	WDI, C1, C2, C3 Input Low Threshold		●			0.4	V
$t_{WDI(WIDTH)}$	WDI Pulse Width		●	40			ns
V_{IH}	PLL/MODE, C1, C2, C3 Input High Threshold		●	V_{CC} – 0.4			V
V_{IL}	PLL/MODE Input Low Threshold		●			V_{CC} – 1.2	V
Interface Logic Pins (EN1, EN2, EN3, EN4)							
$V_{HI(ALLOFF)}$	Enable Rising Threshold	All Regulators Disabled	●		730	1200	mV
V_{HI}	Enable Rising Threshold	At Least One Regulator Enabled	●		400	420	mV
V_{LO}	Enable Falling Threshold			340	390		mV
I_{EN}	Enable Pin Leakage Current	EN = 3.3V				1	µA
CT Timing Parameters; C_T = 10nF							
t_{WDI0}	Time from WDO Low Until Next WDO Low	C_T = 10nF	 ●	10.3 6.2	12.9 12.9	15.5	Sec Sec
t_{WDI}	Time from Last WDI Until Next WDO Low	C_T = 10nF	 ●	1.30 0.77	1.62 1.62	1.95	Sec Sec
t_{WDL}	Watchdog Lower Boundary	C_T = 10nF	 ●	40	50.6 50.6	60 65	ms ms
t_{WDO}	WDO Low Time Absent a Transition at WDI	C_T = 10nF		160	202	280	ms
t_{RST}	$\overline{RST}$ Assertion Delay	C_T = 10nF		160	202	240	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3371 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3371E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3371I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3371H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

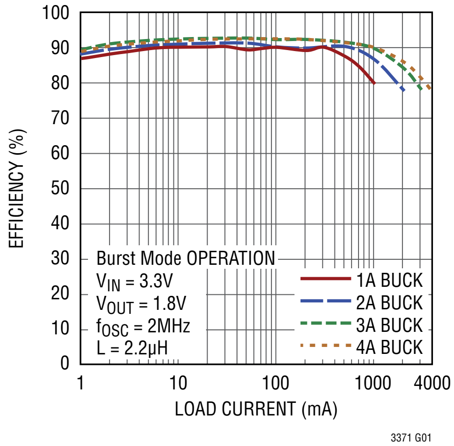
Note 3: The LTC3371 includes overtemperature protection which protects the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Static current, switches not switching. Actual current may be higher due to gate charge losses at the switching frequency.

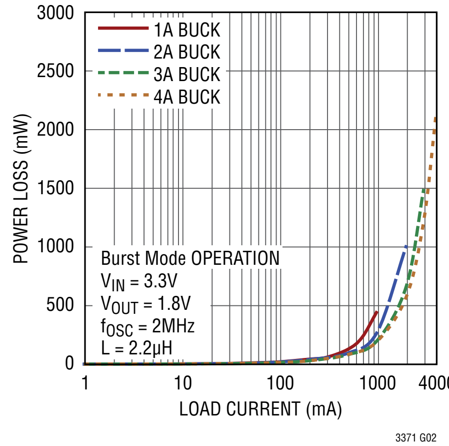
Note 5: The current limit features of this part are intended to protect the IC from short term or intermittent fault conditions. Continuous operation above the maximum specified pin current rating may result in device degradation over time.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

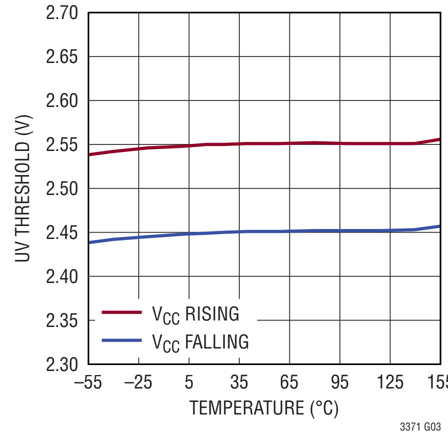
Buck Efficiency vs I_{LOAD}



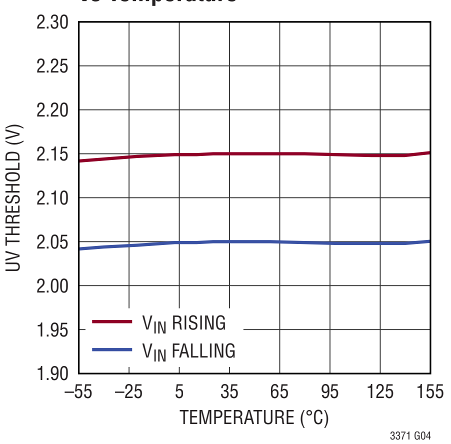
Buck Power Loss vs I_{LOAD}



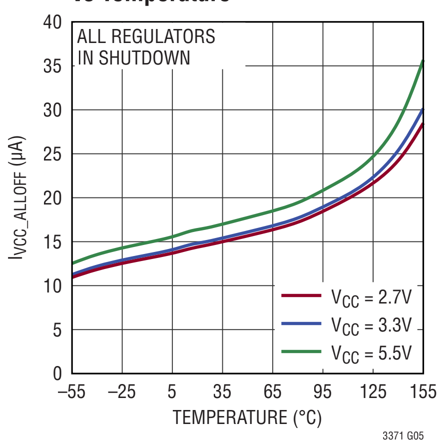
V_{CC} Undervoltage Threshold vs Temperature



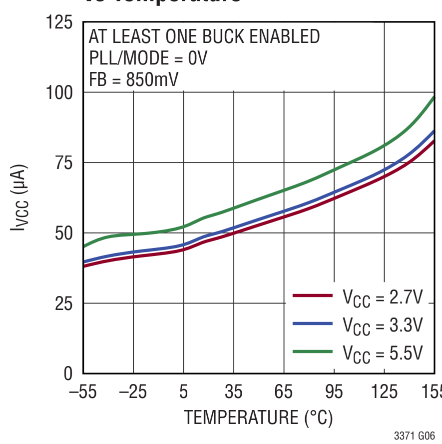
Buck V_{IN} Undervoltage Threshold vs Temperature



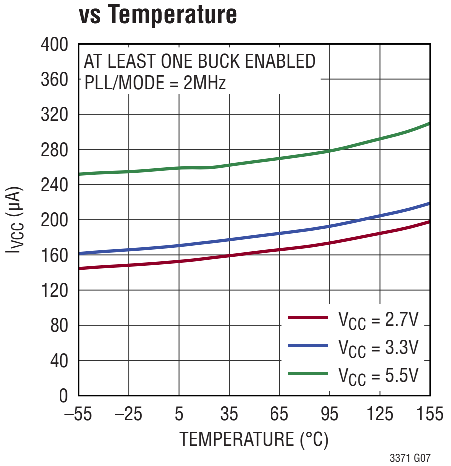
V_{CC} Supply Current vs Temperature



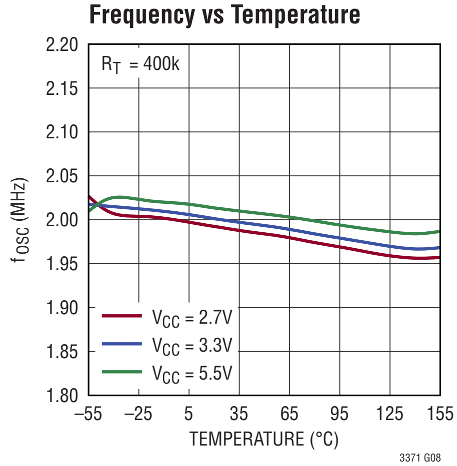
V_{CC} Supply Current vs Temperature



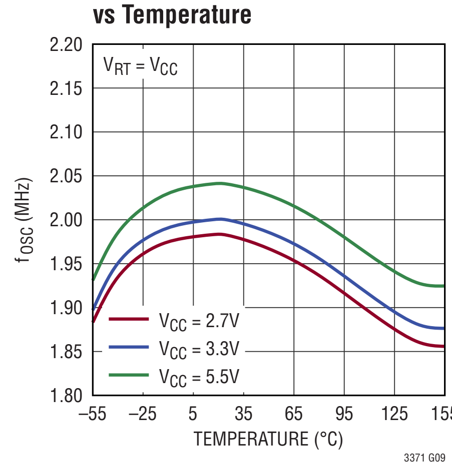
V_{CC} Supply Current vs Temperature



R_T Programmed Oscillator Frequency vs Temperature

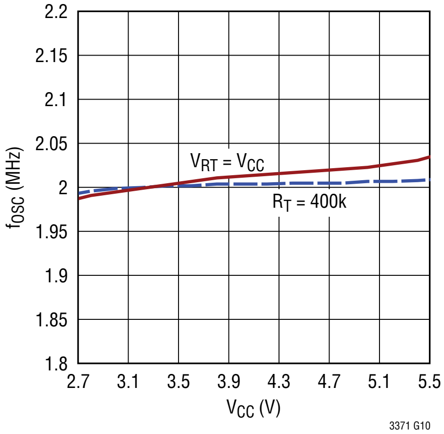


Default Oscillator Frequency vs Temperature

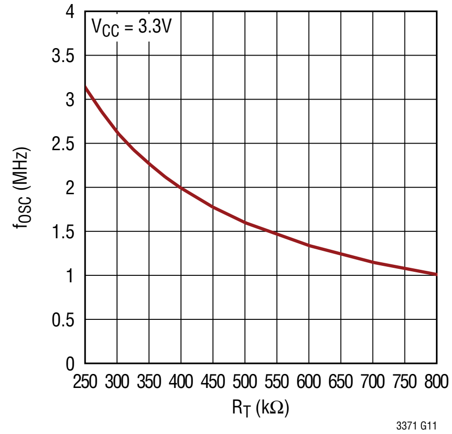


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

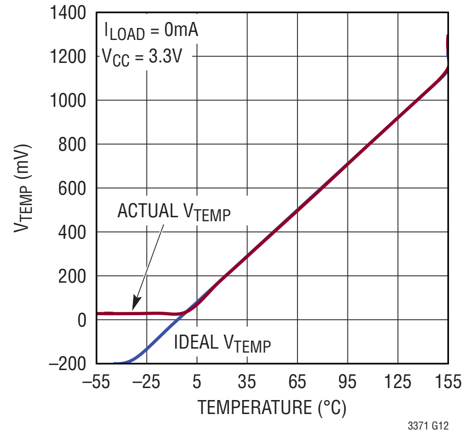
Oscillator Frequency vs V_{CC}



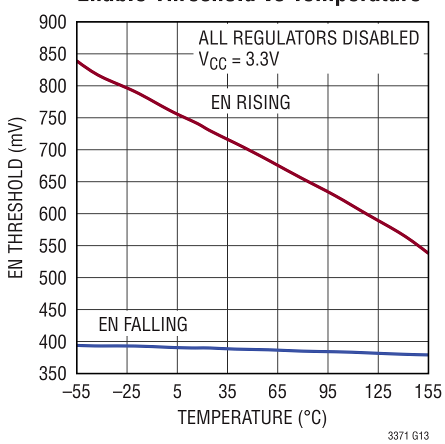
Oscillator Frequency vs R_T



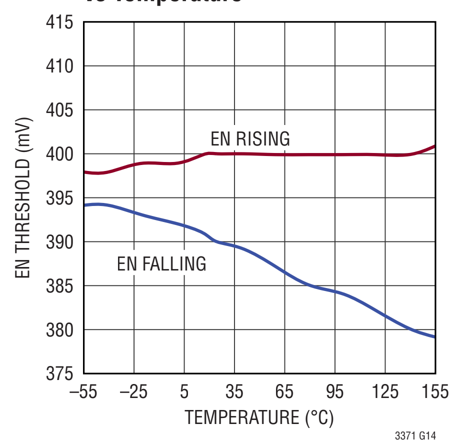
V_{TEMP} vs Temperature



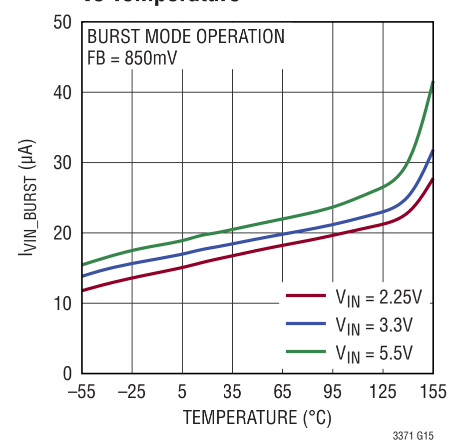
Enable Threshold vs Temperature



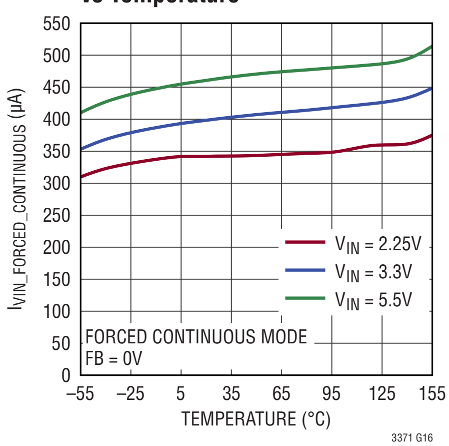
Enable Pin Precision Threshold vs Temperature



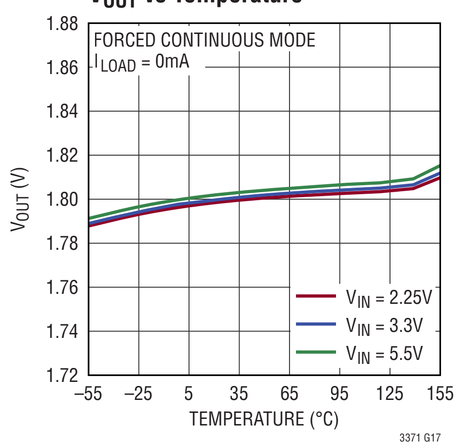
Buck V_{IN} Supply Current vs Temperature



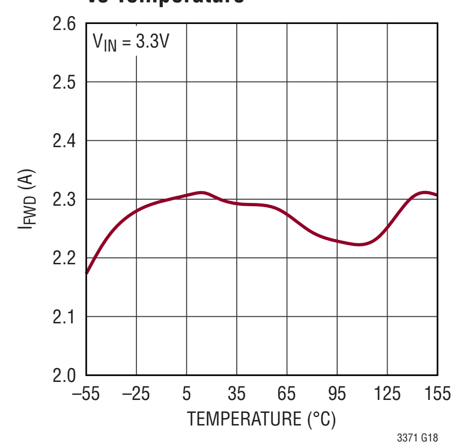
Buck V_{IN} Supply Current vs Temperature



V_{OUT} vs Temperature

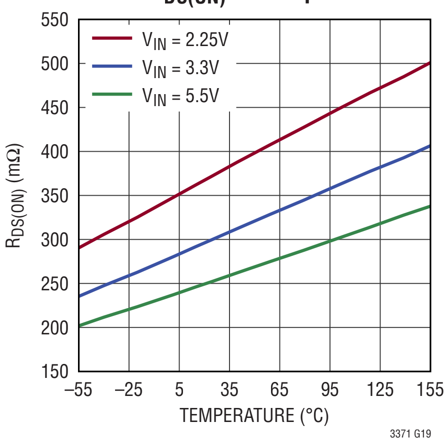


PMOS Current Limit vs Temperature

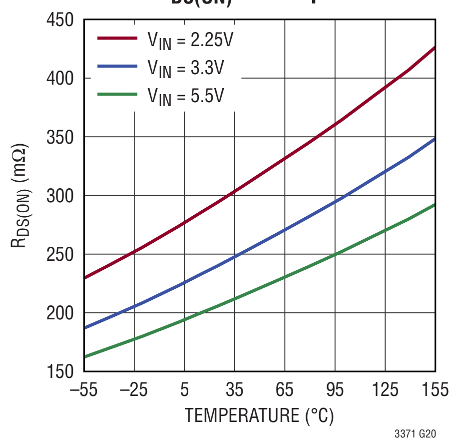


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

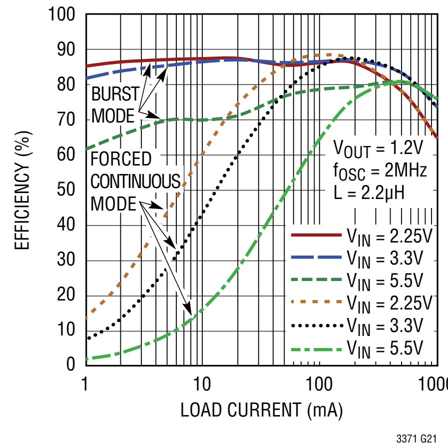
PMOS $R_{DS(ON)}$ vs Temperature



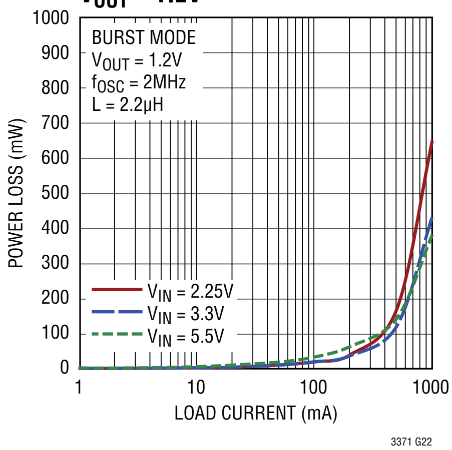
NMOS $R_{DS(ON)}$ vs Temperature



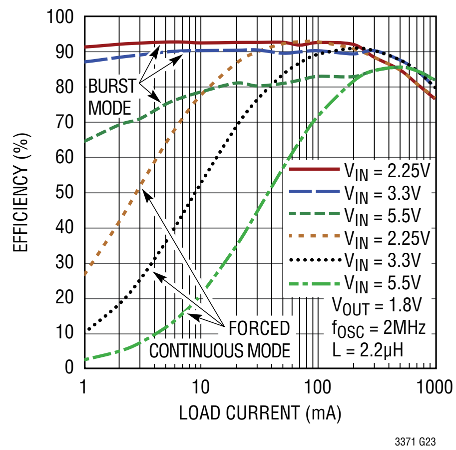
1A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.2V



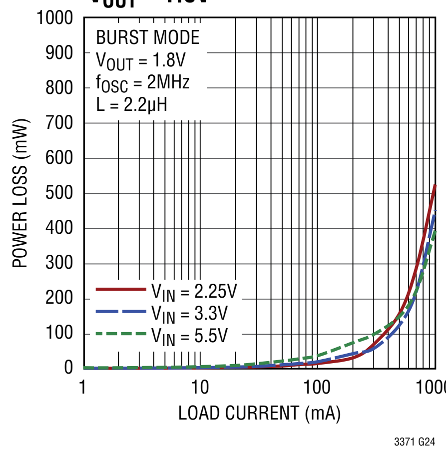
1A Buck Power Loss vs I_{LOAD}, V_{OUT} = 1.2V



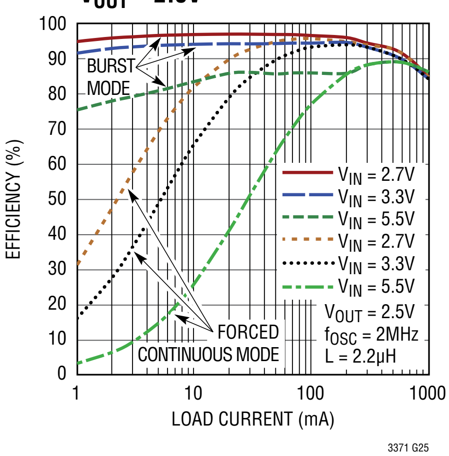
1A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



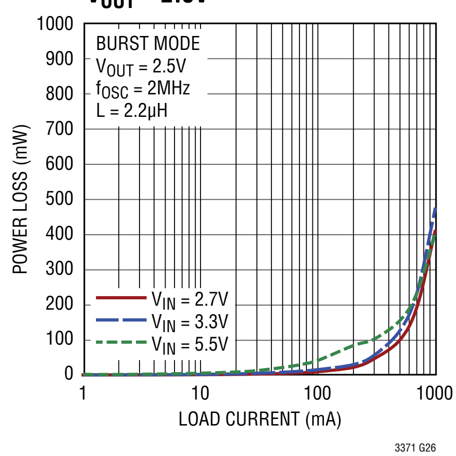
1A Buck Power Loss vs I_{LOAD}, V_{OUT} = 1.8V



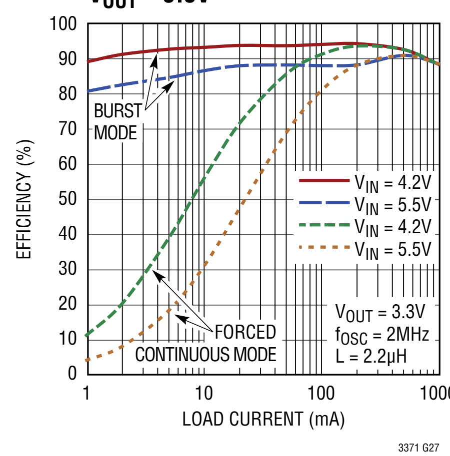
1A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



1A Buck Power Loss vs I_{LOAD}, V_{OUT} = 2.5V

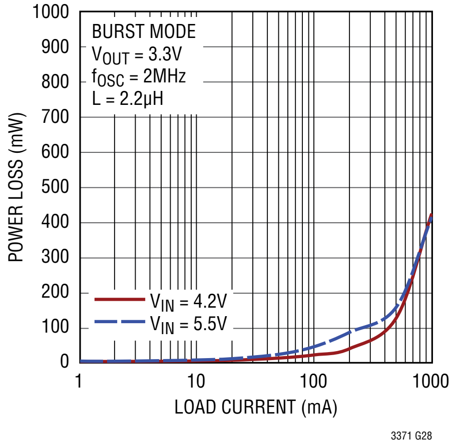


1A Buck Efficiency vs I_{LOAD}, V_{OUT} = 3.3V

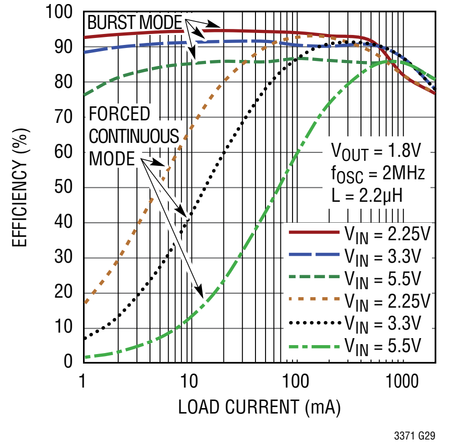


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

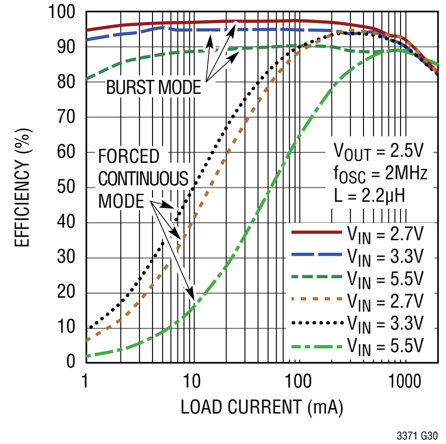
1A Buck Power Loss vs I_{LOAD}, V_{OUT} = 3.3V



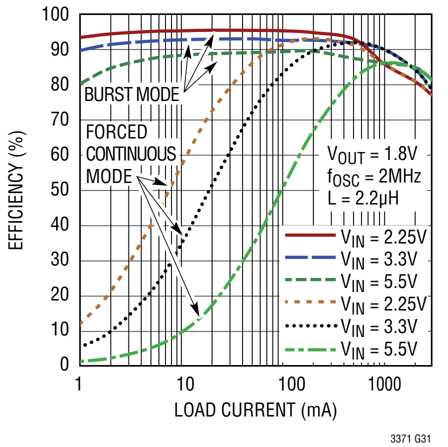
2A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



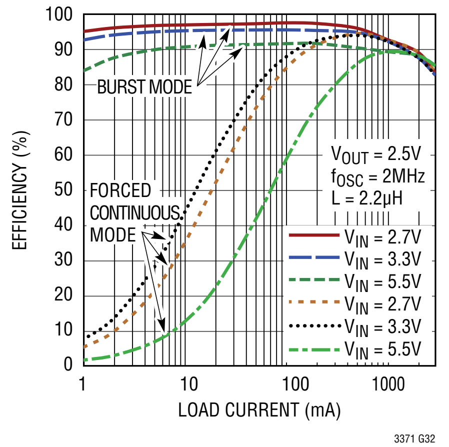
2A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



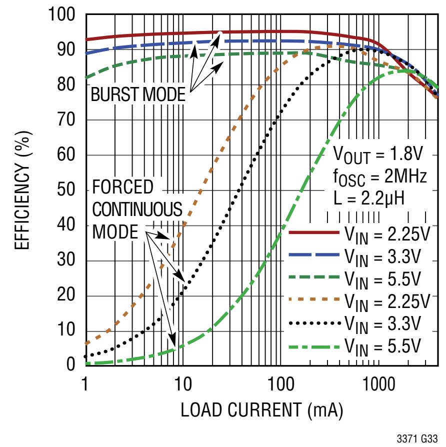
3A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



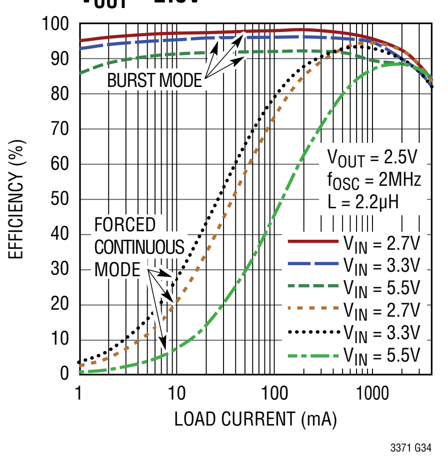
3A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



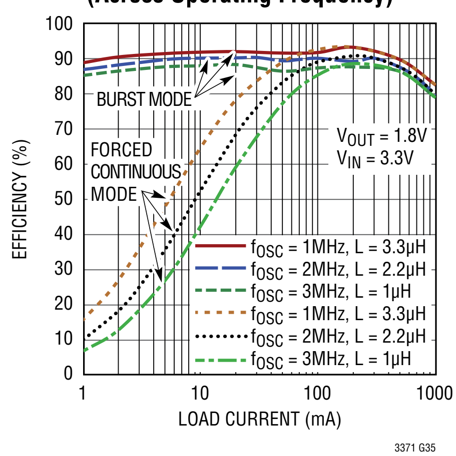
4A Buck Efficiency vs I_{LOAD}, V_{OUT} = 1.8V



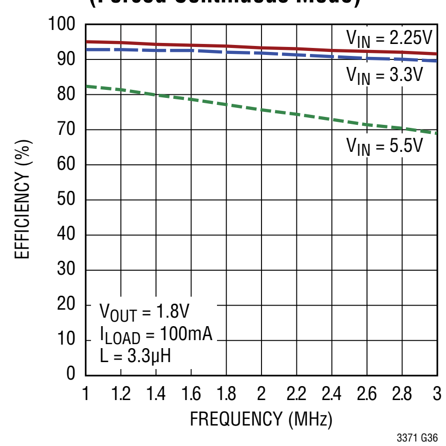
4A Buck Efficiency vs I_{LOAD}, V_{OUT} = 2.5V



1A Buck Efficiency vs I_{LOAD} (Across Operating Frequency)

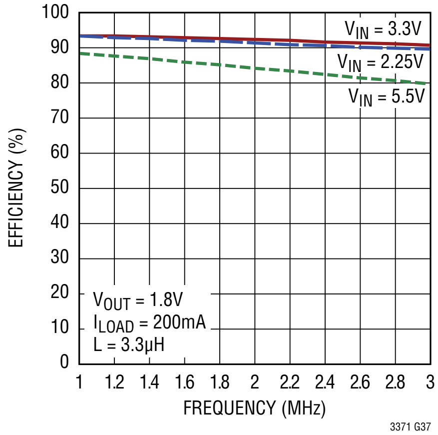


1A Buck Efficiency vs Frequency (Forced Continuous Mode)

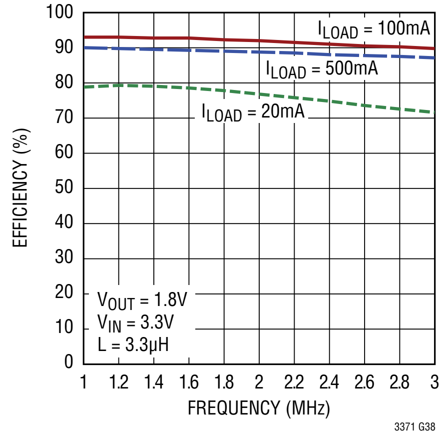


Typical Performance Characteristics $T_A = 25°C$ unless otherwise noted.

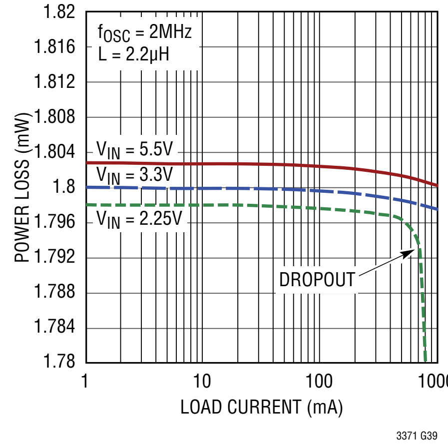
1A Buck Efficiency vs Frequency (Forced Continuous Mode)



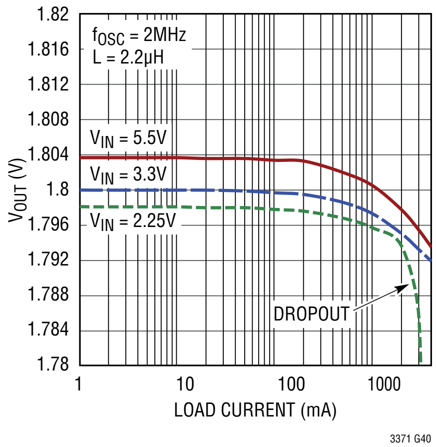
1A Buck Efficiency vs Frequency (Forced Continuous Mode)



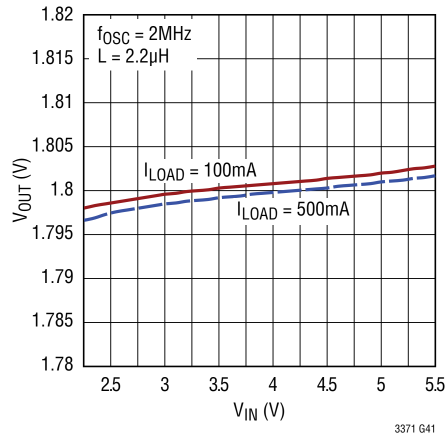
1A Buck Regulator Load Regulation (Forced Continuous Mode)



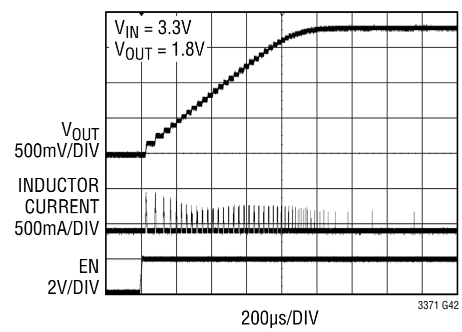
4A Buck Regulator Load Regulation (Forced Continuous Mode)



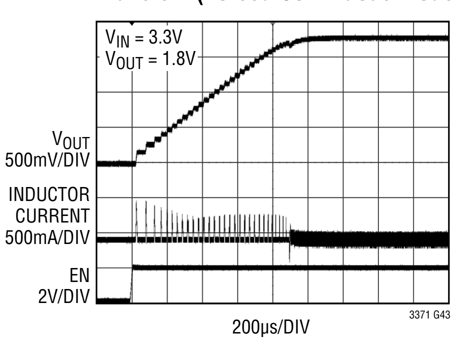
1A Buck Regulator Line Regulation (Forced Continuous Mode)



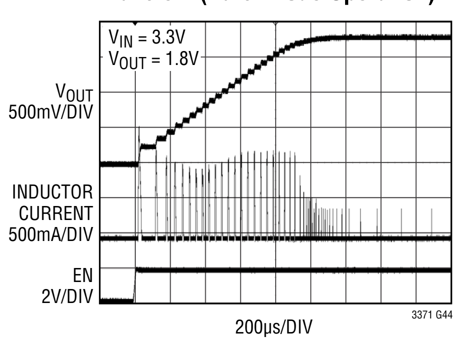
1A Buck Regulator No-Load Startup Transient (Burst Mode Operation)



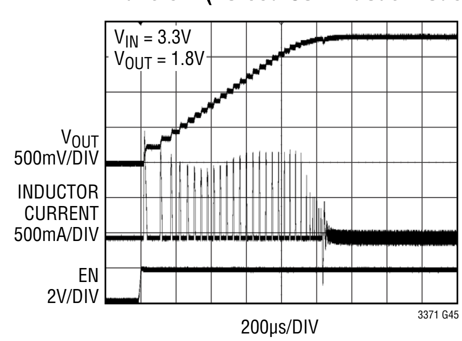
1A Buck Regulator No-Load Startup Transient (Forced Continuous Mode)



4A Buck Regulator No-Load Startup Transient (Burst Mode Operation)

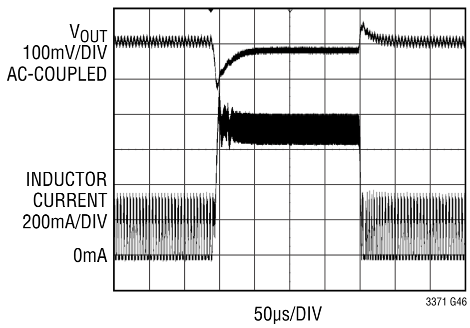


4A Buck Regulator No-Load Startup Transient (Forced Continuous Mode)



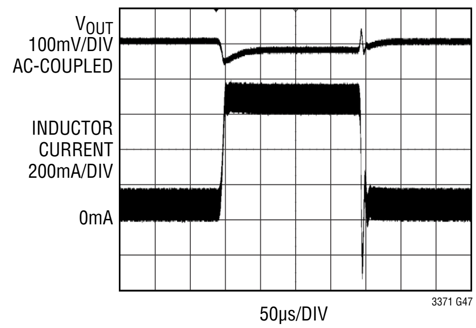
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

1A Buck Regulator, Transient Response (Burst Mode Operation)



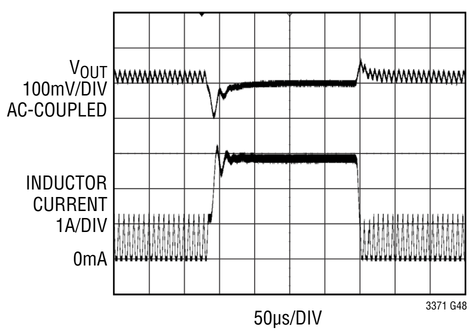
LOAD STEP = 100mA TO 700mA
V_{IN} = 3.3V
V_{OUT} = 1.8V

1A Buck Regulator, Transient Response (Forced Continuous Mode)



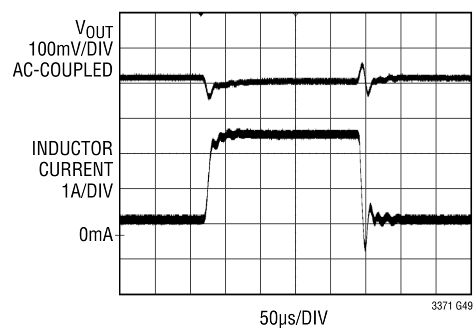
LOAD STEP = 100mA TO 700mA
V_{IN} = 3.3V
V_{OUT} = 1.8V

4A Buck Regulator, Transient Response (Burst Mode Operation)



LOAD STEP = 400mA TO 2.8A
V_{IN} = 3.3V
V_{OUT} = 1.8V

4A Buck Regulator, Transient Response (Forced Continuous Mode)



LOAD STEP = 400mA TO 2.8A
V_{IN} = 3.3V
V_{OUT} = 1.8V

PIN FUNCTIONS (QFN/TSSOP)

FB1 (Pin 1/Pin 5): Buck Regulator 1 Feedback Pin. Receives feedback by a resistor divider connected across the output.

V_{INA} (Pin 2/Pin 6): Power Stage A Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWA (Pin 3/Pin 7): Power Stage A Switch Node. External inductor connects to this pin.

SWB (Pin 4/Pin 8): Power Stage B Switch Node. External inductor connects to this pin.

V_{INB} (Pin 5/Pin 9): Power Stage B Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

V_{INC} (Pin 6/Pin 10): Power Stage C Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWC (Pin 7/Pin 11): Power Stage C Switch Node. External inductor connects to this pin.

SWD (Pin 8/Pin 12): Power Stage D Switch Node. External inductor connects to this pin.

V_{IND} (Pin 9/Pin 13): Power Stage D Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

FB2 (Pin 10/Pin 14): Buck Regulator 2 Feedback Pin. Receives feedback by a resistor divider connected across the output. In configurations where Buck 2 is not used, FB2 should be tied to ground.

EN2 (Pin 11/Pin 15): Buck Regulator 2 Enable Input. Active high. In configurations where Buck 2 is not used, tie EN2 to ground. Do not float.

$\overline{\text{RST2}}$ (Pin 12/Pin 16): Buck Regulator 2 Reset Pin (Active Low). Open-drain output. When Buck 2 is disabled or its regulated output voltage is more than 5% below its programmed level, this pin is driven low. Assertion delay is scaled by the C_T capacitor.

C1 (Pin 13/Pin 17): Configuration Control Input Bit. With C2 and C3, C1 configures the Buck output current power stage combinations. C1 should either be tied to V_{CC} or ground. Do not float.

C2 (Pin 14/Pin 18): Configuration Control Input Bit. With C1 and C3, C2 configures the Buck output current power stage combinations. C2 should either be tied to V_{CC} or ground. Do not float.

C3 (Pin 15/Pin 19): Configuration Control Input Bit. With C1 and C2, C3 configures the Buck output current power stage combinations. C3 should either be tied to V_{CC} or ground. Do not float.

WDI (Pin 16/Pin 20): Watchdog Timer Input. The WDI pin must be toggled either low to high or high to low every 1.62 seconds. Failure to toggle WDI results in the WDO pin being pulled low for 202ms. All times correspond to a 10nF capacitor on the CT pin.

WDO (Pin 17/Pin 21): Watchdog Timer Output. Open-drain output. WDO is pulled low for 202ms during a watchdog timeout period. The WDO pin pulls low if the WDI input does not transition in less than 1.62 seconds since its last transition or 12.9 seconds after a watchdog timeout period. A V_{CC} UVLO event resets the watchdog timer and WDO asserts itself low for the 202ms watchdog timeout period. All times correspond to a 10nF capacitor on the CT pin.

CT (Pin 18/Pin 22): Timing Capacitor Pin. A capacitor connected to GND sets a time constant which is scaled for use by the WDI, WDO, and $\overline{\text{RST1-4}}$ pins.

$\overline{\text{RST3}}$ (Pin 19/Pin 23): Buck Regulator 3 Reset Pin (Active Low). Open-drain output. When Buck 3 is disabled or its regulated output voltage is more than 5% below its programmed level, this pin is driven low. Assertion delay is scaled by the C_T capacitor.

EN3 (Pin 20/Pin 24): Buck Regulator 3 Enable Input. Active high. In configurations where Buck 3 is not used, tie EN3 to ground. Do not float.

FB3 (Pin 21/Pin 25): Buck Regulator 3 Feedback Pin. Receives feedback by a resistor divider connected across the output. In configurations where Buck 3 is not used, FB3 should be tied to ground.

PIN FUNCTIONS (QFN/TSSOP)

V_{INE} (Pin 22/Pin 26): Power Stage E Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWE (Pin 23/Pin 27): Power Stage E Switch Node. External inductor connects to this pin.

SWF (Pin 24/Pin 28): Power Stage F Switch Node. External inductor connects to this pin.

V_{INF} (Pin 25/Pin 29): Power Stage F Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

V_{ING} (Pin 26/Pin 30): Power Stage G Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

SWG (Pin 27/Pin 31): Power Stage G Switch Node. External inductor connects to this pin.

SWH (Pin 28/Pin 32): Power Stage H Switch Node. External inductor connects to this pin.

V_{INH} (Pin 29/Pin 33/): Power Stage H Input Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

FB4 (Pin 30/Pin 34): Buck Regulator 4 Feedback Pin. Receives feedback by a resistor divider connected across the output.

EN4 (Pin 31/Pin 35): Buck Regulator 4 Enable Input. Active high. Do not float.

$\overline{\text{RST4}}$ (Pin 32/Pin 36): Buck Regulator 4 Reset Pin (Active Low). Open-drain output. When Buck 4 is disabled or its regulated output voltage is more than 5% below its programmed level, this pin is driven low. Assertion delay is scaled by the C_T capacitor.

RT (Pin 33/Pin 37): Oscillator Frequency Pin. This pin provides two modes of setting the switching frequency. Connecting a resistor from RT to ground sets the switching frequency based on the resistor value. If RT is tied to V_{CC} the internal 2MHz oscillator is used. Do not float.

PLL/MODE (Pin 34/Pin 38): Oscillator Synchronization and Buck Mode Select Pin. Driving PLL/MODE with an external clock signal synchronizes all switches to the applied frequency, and the buck converters operate in forced continuous mode. The slope compensation is automatically adapted to the external clock frequency. The absence of an external clock signal enables the frequency programmed by the RT pin. When not synchronizing to an external clock this input determines how the LTC3371 operates at light loads. Pulling this pin to ground selects Burst Mode operation. Tying this pin to V_{CC} invokes forced continuous mode operation. Do not float.

V_{CC} (Pin 35/Pin 1): Internal Bias Supply. Bypass to GND with a 10µF or larger ceramic capacitor.

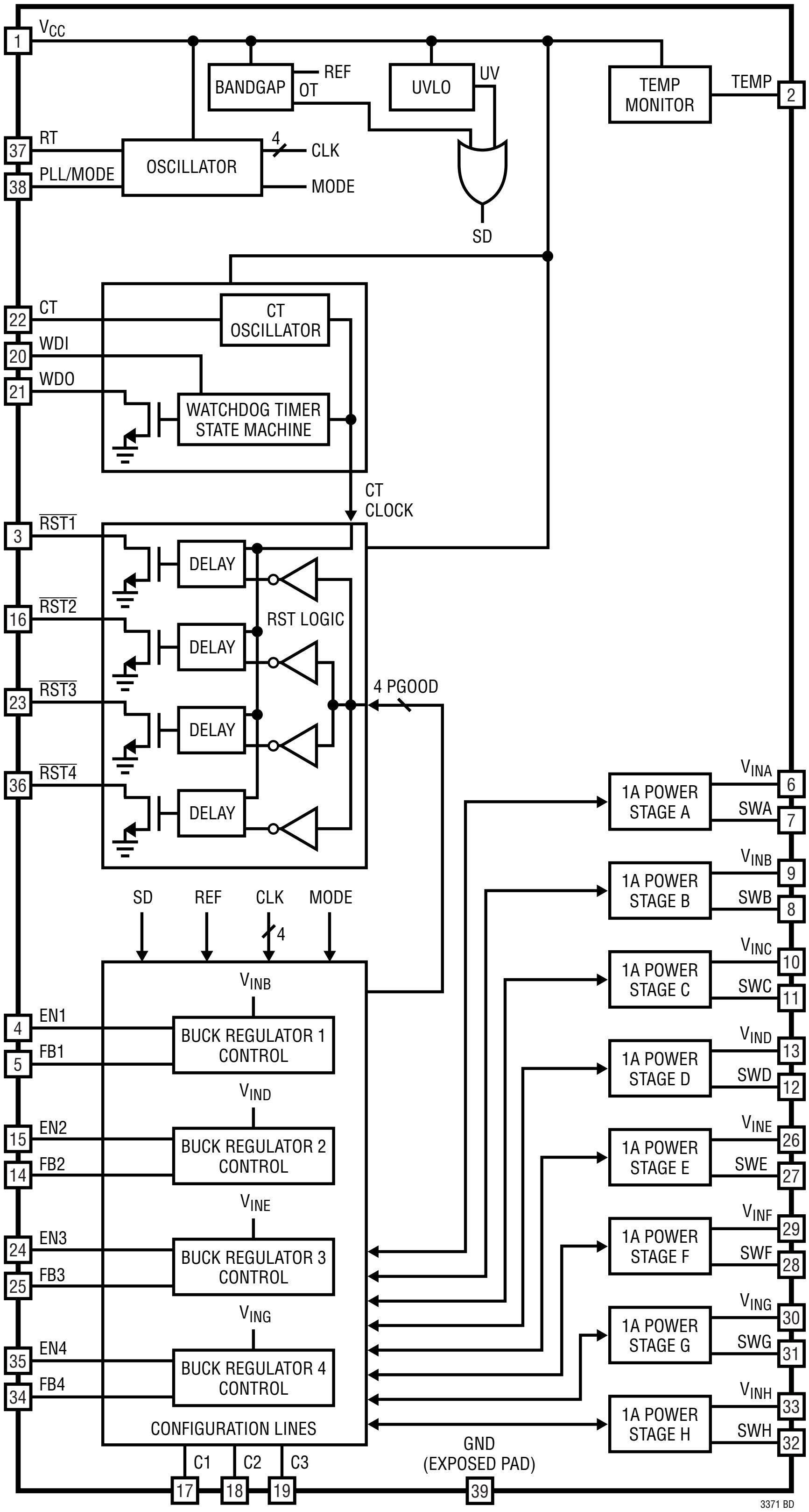
TEMP (Pin 36/Pin 2): Temperature Indication Pin. TEMP outputs a voltage of 220mV (typical) at 25°C. The TEMP voltage increases by 7mV/°C (typical) at higher temperatures giving an external indication of the LTC3371 internal die temperature.

$\overline{\text{RST1}}$ (Pin 37/Pin 3): Buck Regulator 1 Reset Pin (Active Low). Open-drain output. When Buck 1 is disabled or its regulated output voltage is more than 2% below its programmed level, this pin is driven low. Assertion delay is scaled by the C_T capacitor.

EN1 (Pin 38/Pin 4): Buck Regulator 1 Enable Input. Active high. Do not float.

GND (Exposed Pad Pin 39): Ground. The exposed pad must be connected to a continuous printed circuit board ground plane directly under the LTC3371.

BLOCK DIAGRAM (Pin numbers reflect TSSOP package)



3371fb

OPERATION

Buck Switching Regulators

The LTC3371 contains eight monolithic 1A synchronous buck switching channels. These are controlled by up to four current mode regulator controllers. All of the switching regulators are internally compensated and need only external feedback resistors to set the output voltage. The switching regulators offer two operating modes: Burst Mode operation (PLL/MODE = LOW) for higher efficiency at light loads and forced continuous PWM mode (PLL/MODE = HIGH or switching) for lower noise at light loads. In Burst Mode operation at light loads, the output capacitor is charged to a voltage slightly higher than its regulation point. The regulator then goes into a sleep state, during which time the output capacitor provides the load current. In sleep most of the regulator's circuitry is powered down, helping conserve input power. When the output capacitor droops below its programmed value, the circuitry is powered on and another burst cycle begins. The sleep time decreases as load current increases. In Burst Mode operation, the regulator bursts at light loads whereas at higher loads it operates at constant frequency PWM mode operation. In forced continuous mode, the oscillator runs continuously and the buck switch currents are allowed to reverse under very light load conditions to maintain regulation. This mode allows the buck to run at a fixed frequency with minimal output ripple.

Each buck switching regulator can operate at an independent V_{IN} voltage and has its own FB and EN pin to maximize flexibility. The enable pins have two different enable threshold voltages that depend on the operating state of the LTC3371. With all regulators disabled, the enable pin threshold is set to 730mV (typical). Once any regulator is enabled, the enable pin thresholds of the remaining regulators are set to a bandgap-based 400mV and the EN pins are each monitored by a precision comparator. This precision EN threshold may be used to provide event-based sequencing via feedback from other previously enabled regulators. All buck regulators have forward and reverse-current limiting, soft-start to limit inrush current during start-up and short-circuit protection.

The buck switching regulators are phased in 90° steps to reduce noise and input ripple. The phase step determines the fixed edge of the switching sequence, which is when the PMOS turns on. The PMOS off (NMOS on) phase is subject to the duty cycle demanded by the regulator. Buck 1 is set to 0°, Buck 2 is set to 90°, Buck 3 is set to 270°, and Buck 4 is set to180°. In shutdown all SW nodes are high impedance. The buck regulator enable pins may be tied to V_{OUT} voltages through a resistor divider, to program power-up sequencing.

The buck switching regulators feature a controlled shutdown scheme where the inductor current ramps down to zero through the NMOS switch. If any event causes the buck regulator to shut down (EN = LOW, OT, V_{INA-H} or V_{CC} UVLO) the NMOS switch turns on until the inductor current reaches 0mA (typical). Then, the switch pin becomes Hi-Z.

Buck Regulators with Combined Power Stages

Up to four adjacent buck regulators may be combined in a master-slave configuration by setting the configuration via the C1, C2, and C3 pins. These pins should either be tied to ground or pin strapped to V_{CC} in accordance with the desired configuration code (Table 1). Any combined SW pins must be tied together, as must any of the combined V_{IN} pins. EN1 and FB1 are utilized by Buck 1, EN2 and FB2 by Buck 2, EN3 and FB3 by Buck 3, and EN4 and FB4 by Buck 4. If any buck is not used or is not available in the desired configuration, then the associated FB and EN pins must be tied to ground.

Any available combination of 2, 3, or 4 adjacent buck regulators serve to provide up to either 2A, 3A, or 4A of average output load current. For example, code 110 (C3C2C1) configures Buck 1 to operate as a 4A regulator through V_{IN}/SW pairs A, B, C, and D, while Buck 2 is disabled, Buck 3 operates as a 1A regulator through V_{IN}/SW pair E, and Buck 4 operates as a 3A regulator through V_{IN}/SW pairs F, G, and H.

OPERATION

Table 1. Master Slave Program Combinations (Each Letter Corresponds to a V_{IN} and SW Pair)

PROGRAM CODE C3C2C1	BUCK 1	BUCK 2	BUCK 3	BUCK 4
000	AB	CD	EF	GH
001	ABC	D	EF	GH
010	ABC	D	E	FGH
011	ABCH	D	E	FG
100	ABC	DE	Not Used	FGH
101	ABCD	Not Used	EF	GH
110	ABCD	Not Used	E	FGH
111	ABCD	Not Used	Not Used	EFGH

Power Failure Reporting Via $\overline{RST}$ Pins

Power failure conditions are reported back by each buck's associated $\overline{RST}$ pin. Each buck switching regulator has an internal power good (PGOOD) signal. When the regulated output voltage of an enabled switcher falls below 98% for Buck 1 or 95% for Bucks 2-4 of its programmed value, the PGOOD signal is pulled low. If any PGOOD signal stays low for greater than 100μs, then the associated $\overline{RST}$ pin is pulled low, indicating to a microprocessor that a power failure fault has occurred. The 100μs filter time prevents the pin from being pulled low due to a transient. The PGOOD signal has a 0.3% hysteresis such that when the regulated output voltage of an enabled switcher rises above 98.3% or 95.3%, respectively, of its programmed value, the PGOOD signal transitions high.

Once an enabled regulator has its output PGOOD for 202ms (typical, C_T = 10nF) its associated $\overline{RST}$ output goes Hi-Z. Any disabled or inactive switchers will assert a $\overline{RST}$ low.

Temperature Monitoring and Overtemperature Protection

To prevent thermal damage to the LTC3371 and its surrounding components, the LTC3371 incorporates an overtemperature (OT) function. When the LTC3371 die temperature reaches 170°C (typical) all enabled buck switching regulators are shut down and remain in shutdown until the die temperature falls to 160°C (typical).

The temperature may be read back by the user by sampling the TEMP pin analog voltage. The temperature, T, indicated by the TEMP pin voltage is given by:

$$T = \frac{V_{TEMP} - 45mV}{7mV} \cdot 1°C \quad (1)$$

If none of the buck switching regulators are enabled, then the temperature monitor is also shut down to further reduce quiescent current.

Programming the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output voltage ripple.

The operating frequency for all of the LTC3371 regulators is determined by an external resistor that is connected between the RT pin and ground. The operating frequency can be calculated using the following equation:

$$f_{OSC} = \frac{8 \cdot 10^{11} \cdot \Omega Hz}{R_T} \quad (2)$$

While the LTC3371 is designed to function with operating frequencies between 1MHz and 3MHz, it has safety clamps that will prevent the oscillator from running faster than 4MHz (typical) or slower than 250kHz (typical). Tying the RT pin to V_{CC} sets the oscillator to the default internal operating frequency of 2MHz (typical).

The LTC3371's internal oscillator can be synchronized through an internal PLL circuit to an external frequency by applying a square wave clock signal to the PLL/MODE pin. During synchronization, the top MOSFET turn-on of Buck regulator 1 is phase locked to the rising edge of the external frequency source. All other buck switching regulators are locked to the appropriate phase of the external frequency source (see Buck Switching Regulators).

OPERATION

The synchronization frequency range is 1MHz to 3MHz. A synchronization signal on the PLL/MODE pin will force all active buck switching regulators to operate in forced continuous mode PWM.

Windowed Watchdog Timer

A standard watchdog function is used to ensure that the system is in a valid state by continuously monitoring the microprocessor's activity. The microprocessor must toggle the logic state of the WDI pin periodically in order to clear the watchdog timer. The WDI pin reset is read only on a WDI falling edge, such that a single reset signal may be asserted by pulsing the WDI pin for a time greater than the minimum pulse width. If timeout occurs, the LTC3371 asserts a WDO low for the reset timeout period, issuing a system reset. Once the reset timeout completes, WDO is released to go high and the watchdog timer starts again.

During power-up, the watchdog timer initiates in the timeout state with WDO asserted low. As soon as the reset timer times out, WDO goes high and the watchdog timer is started.

The LTC3371 implements a windowed watchdog function by adding a lower boundary condition to the standard watchdog function. If the WDI input receives a falling edge prior to the watchdog lower boundary, the part considers this a watchdog failure, and asserts WDO low (releasing again after the reset timeout period as described above). This will again be followed by another lower boundary time period.

Choosing the C_T Capacitor

The watchdog timeout period is adjustable and can be optimized for software execution. The watchdog timeout period is adjusted by connecting a capacitor between CT and ground. Given a specified watchdog timeout period, the capacitor is determined by:

$$C_T = t_{WDO} \bullet 49.39[nF/s] \quad (3)$$

For example, using a standard capacitor value of 10nF gives a 202ms watchdog timeout period. Further, the other watchdog timing periods scale with t_{WDO}. The watchdog lower boundary time (t_{WDL}) scales as precisely 1/4 of t_{WDO}, the watchdog upper boundary time following the previous WDI pulse scales as eight times that of t_{WDO}, and the watchdog upper boundary time following a watchdog timeout scales as 64 times that of t_{WDO}. Finally the $\overline{RST}$ assertion delay will scale to the same time as t_{WDO}.

These timing periods are illustrated in Figure 1. Each WDO low period is equal to the time period t_2-t_1 (202ms for a 10nF C_T capacitor, typical). If a WDI falling edge occurs before the watchdog lower boundary, indicated by t_3-t_2 (50.6ms for a 10nF C_T capacitor, typical), then another watchdog timeout period occurs. If a WDI falling edge occurs after the watchdog lower boundary (t_4), then the watchdog counter resets, beginning with another watchdog lower boundary period. In the case where a WDI low transition is not detected by the specified time another watchdog timeout period is initiated. This time is indicated by t_5-t_4 (1.62s for a 10nF C_T capacitor, typical). If a WDI low transition is not detected within the specified time following a watchdog timeout period, then another watchdog timeout period is initiated. This time is indicated by t_7-t_6 (12.9s for a 10nF C_T capacitor, typical).

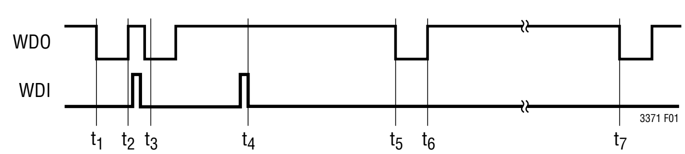


Figure 1. WDO Timing Parameters

APPLICATIONS INFORMATION

Buck Switching Regulator Output Voltage and Feedback Network

The output voltage of the buck switching regulators is programmed by a resistor divider connected from the switching regulator's output to its feedback pin and is given by $V_{OUT} = V_{FB}(1 + R2/R1)$ as shown in Figure 2. Typical values for R1 range from 40k to 1M. The buck regulator transient response may improve with optional capacitor, C_{FF}, that helps cancel the pole created by the feedback resistors and the input capacitance of the FB pin. Experimentation with capacitor values between 2pF and 22pF may improve transient response.

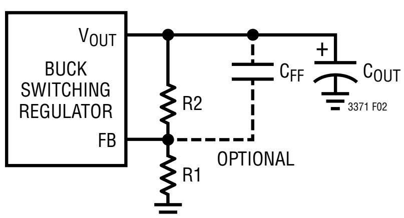


Figure 2. Feedback Components

Buck Regulators

All four buck regulators are designed to be used with inductors ranging from 1µH to 3.3µH depending on the lowest switching frequency at which the buck regulator must operate. When operating at 1MHz a 3.3µH inductor should be used, while at 3MHz a 1µH inductor may be used, or a higher value inductor may be used if reduced current ripple is desired. Table 2 shows some recommended inductors for the buck regulators. The bucks are compensated to operate across the range of possible V_{IN} and V_{OUT} voltages when the appropriate inductance is used for the desired switching frequency.

The input supply should be decoupled with a 10µF capacitor while the output should be decoupled with a 22µF capacitor. Refer to the Capacitor Selection section for details on selecting a proper capacitor.

Combined Buck Power Stages

The LTC3371 has eight power stages that can handle average load currents of 1A each. These power stages may be combined in any one of eight possible combinations, via the C1, C2, and C3 pins (see Table 1). Tables 3, 4, and 5 show recommended inductors for the combined power stage configurations.

The input supply should be decoupled with a 22µF capacitor while the output should be decoupled with a 47µF capacitor for a 2A combined buck regulator. Likewise for 3A and 4A configurations the input and output capacitance must be scaled up to account for the increased load. Refer to the Capacitor Selection section for details on selecting a proper capacitor.

In some cases it may be beneficial to use more power stages than needed to achieve increased efficiency of the active regulators. In general the efficiency will improve by adding stages for any regulator running close to what the rated load current would be without the additional stage. For example, if the application requires a 1A regulator that supplies close to 1A at a high duty cycle, a 3A regulator that only peaks at 3A but averages a lower current, and a 2A regulator that runs at 1.5A at a high duty cycle, better efficiency may be achieved by using the 3A, 3A, 2A configuration.

Input and Output Decoupling Capacitor Selection

The LTC3371 has individual input supply pins for each buck power stage and a separate V_{CC} pin that supplies power to all top level control and logic. Each of these pins must be decoupled with low ESR capacitors to GND. These capacitors must be placed as close to the pins as possible. Ceramic dielectric capacitors are a good compromise between high dielectric constant and stability versus temperature and DC bias. Note that the capacitance of a capacitor deteriorates at higher DC bias. It is important to consult manufacturer data sheets and obtain the true capacitance of a capacitor at the DC bias voltage that it will be operated at. For this reason, avoid the use of Y5V dielectric capacitors. The X5R/X7R dielectric capacitors offer good overall performance.

The input supply voltage Pins 35/1, 2/6, 5/9, 6/10, 9/13, 22/26, 25/29, 26/30, and 29/33 (QFN/TSSOP packages) all need to be decoupled with at least 10µF capacitors. If power stages are combined the supplies should be shorted with as short of a trace as possible, and the decoupling capacitor should be scaled accordingly.

APPLICATIONS INFORMATION

Table 2. Recommended Inductors for 1A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
IHLP1212ABER1R0M-11	1.0	3	38	3 × 3.6 × 1.2	Vishay
1239AS-H-1R0N	1	2.5	65	2.5 × 2.0 × 1.2	Toko
XFL4020-222ME	2.2	3.5	23.5	4 × 4 × 2.1	CoilCraft
1277AS-H-2R2N	2.2	2.6	84	3.2 × 2.5 × 1.2	Toko
IHLP1212BZER2R2M-11	2.2	3	46	3 × 3.6 × 1.2	Vishay
XFL4020-332ME	3.3	2.8	38.3	4 × 4 × 2.1	CoilCraft
IHLP1212BZER3R3M-11	3.3	2.7	61	3 × 3.6 × 1.2	Vishay

Table 3. Recommended Inductors for 2A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XFL4020-102ME	1.0	5.1	11.9	4 × 4 × 2.1	CoilCraft
74437324010	1	5	27	4.45 × 4.06 × 1.8	Wurth Elektronik
XAL4020-222ME	2.2	5.6	38.7	4 × 4 × 2.1	CoilCraft
FDV0530-2R2M	2.2	5.3	15.5	6.2 × 5.8 × 3	Toko
IHLP2020BZER2R2M-11	2.2	5	37.7	5.49 × 5.18 × 2	Vishay
XAL4030-332ME	3.3	5.5	28.6	4 × 4 × 3.1	CoilCraft
FDV0530-3R3M	3.3	4.1	34.1	6.2 × 5.8 × 3	Toko

Table 4. Recommended Inductors for 3A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL4020-102ME	1.0	8.7	14.6	4 × 4 × 2.1	CoilCraft
FDV0530-1R0M	1	8.4	11.2	6.2 × 5.8 × 3	Toko
XAL5030-222ME	2.2	9.2	14.5	5.28 × 5.48 × 3.1	CoilCraft
IHLP2525CZER2R2M-01	2.2	8	20	6.86 × 6.47 × 3	Vishay
74437346022	2.2	6.5	20	7.3 × 6.6 × 2.8	Wurth Elektonik
XAL5030-332ME	3.3	8.7	23.3	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-3R3M	3.3	7.3	27	7.1 × 6.5 × 3	TDK

Table 5. Recommended Inductors for 4A Buck Regulators

PART NUMBER	L (µH)	MAX I_{DC} (A)	MAX DCR (mΩ)	SIZE IN mm (L × W × H)	MANUFACTURER
XAL5030-122ME	1.2	12.5	9.4	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-1R0M120	1	14.1	7.81	7.1 × 6.5 × 3	TDK
XAL5030-222ME	2.2	9.2	14.5	5.28 × 5.48 × 3.1	CoilCraft
SPM6530T-2R2M	2.2	8.4	19	7.1 × 6.5 × 3	TDK
IHLP2525EZER2R2M-01	2.2	13.6	20.9	6.86 × 6.47 × 5	Vishay
XAL6030-332ME	3.3	8	20.81	6.36 × 6.56 × 3.1	CoilCraft
FDVE1040-3R3M	3.3	9.8	10.1	11.2 × 10 × 4	Toko

APPLICATIONS INFORMATION

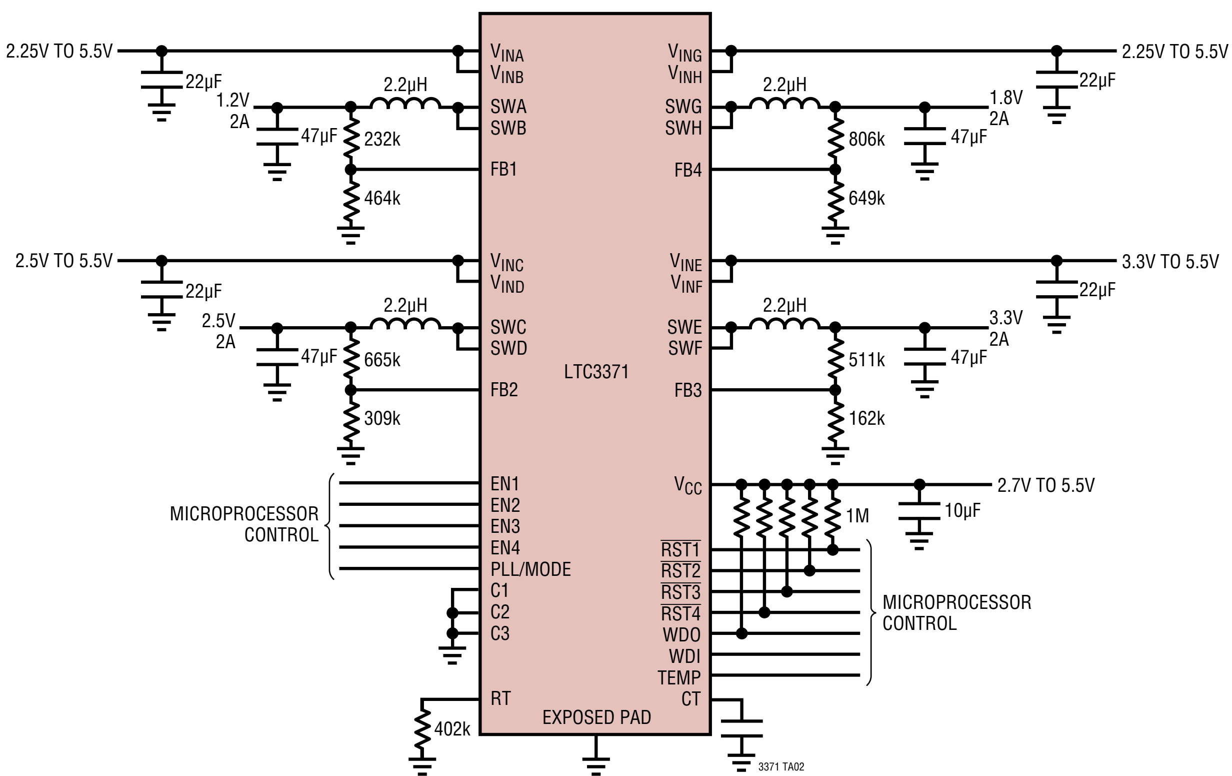
PCB Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3371:

1. The exposed pad of the package (Pin 39) should connect directly to a large ground plane to minimize thermal and electrical impedance.
2. Each of the input supply pins should have a decoupling capacitor.
3. The connections to the switching regulator input supply pins and their respective decoupling capacitors should be kept as short as possible. The GND side of these capacitors should connect directly to the ground plane of the part. These capacitors provide the AC current to the internal power MOSFETs and their drivers. It is important to minimize inductance from these capacitors to the V_{IN} pins of the LTC3371.
4. The switching power traces connecting SWA, SWB, SWC, SWD, SWE, SWF, SWG, and SWH to the inductors should be minimized to reduce radiated EMI and parasitic coupling. Due to the large voltage swing of the switching nodes, high input impedance sensitive nodes, such as the feedback nodes, should be kept far away or shielded from the switching nodes or poor performance could result.
5. The GND side of the switching regulator output capacitors should connect directly to the thermal ground plane of the part. Minimize the trace length from the output capacitor to the inductor(s)/pin(s).
6. In a multiple power stage buck regulator application the trace length of switch nodes to the inductor must be kept equal to ensure proper operation.
7. Care should be taken to minimize capacitance on the TEMP pin. If the TEMP voltage must drive more than ~30pF, then the pin should be isolated with a resistor placed close to the pin of a value between 10k and 100k. Keep in mind that any load on the isolation resistor will create a proportional error.

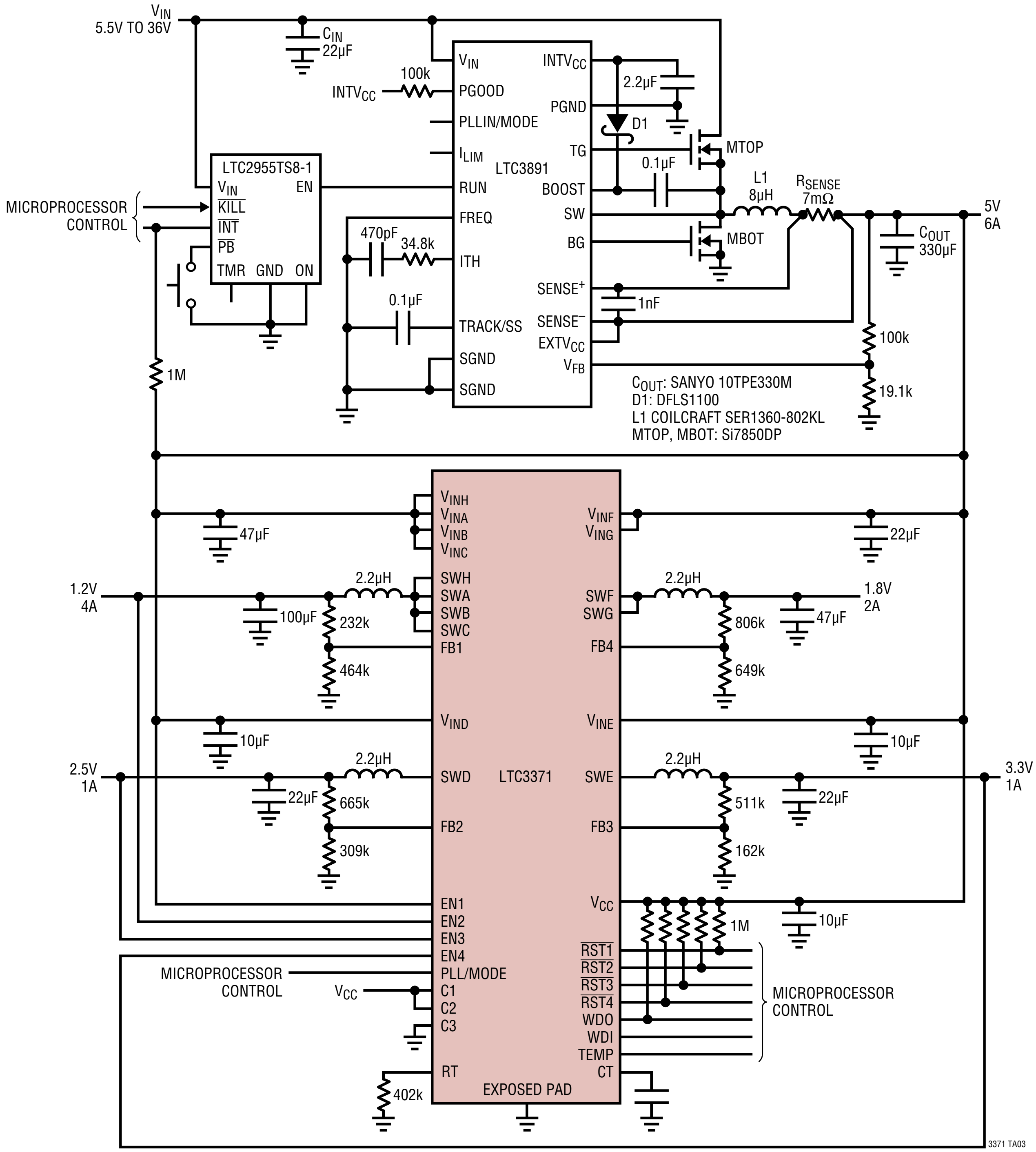
TYPICAL APPLICATIONS

4 × 2A Quad Buck Application



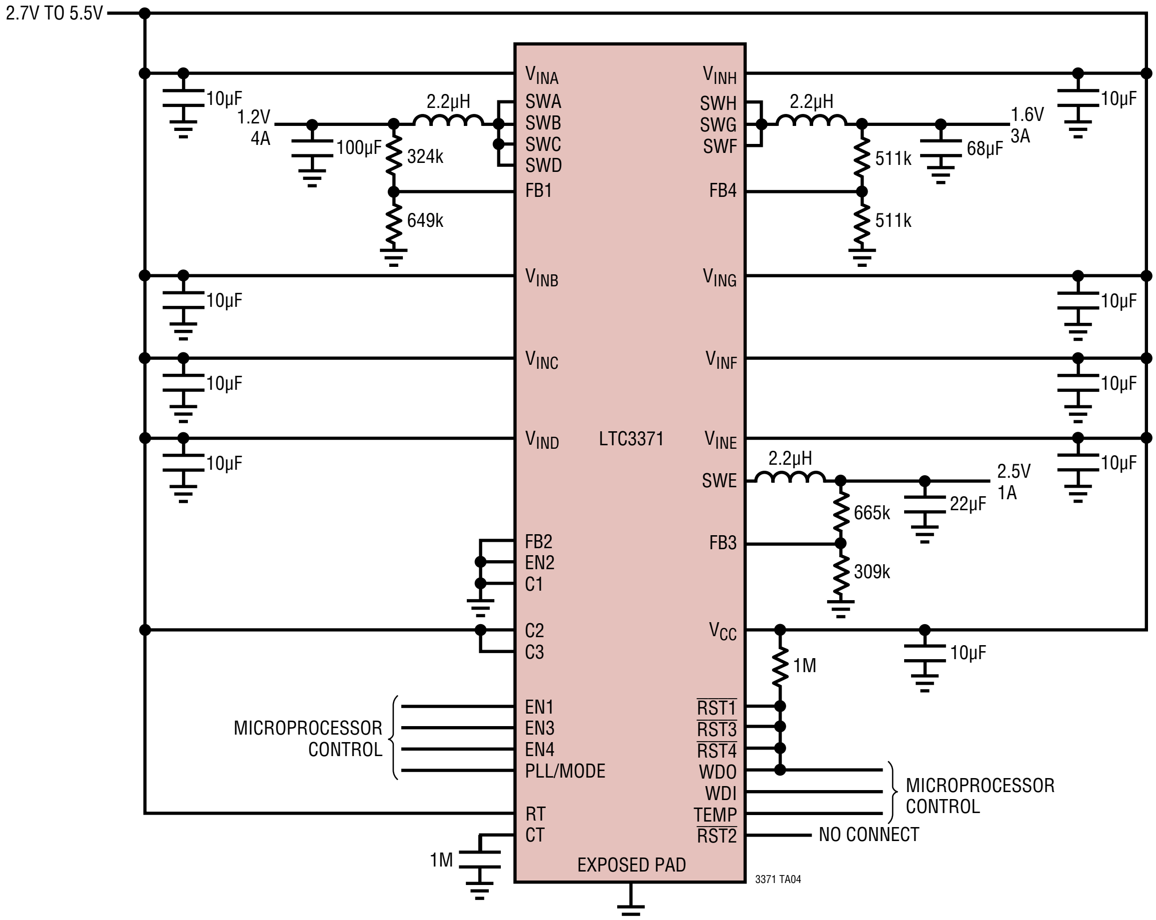
TYPICAL APPLICATIONS

Buck Regulators with Sequenced Start-Up Diven from a High Voltage Upstream Buck Converter



TYPICAL APPLICATIONS

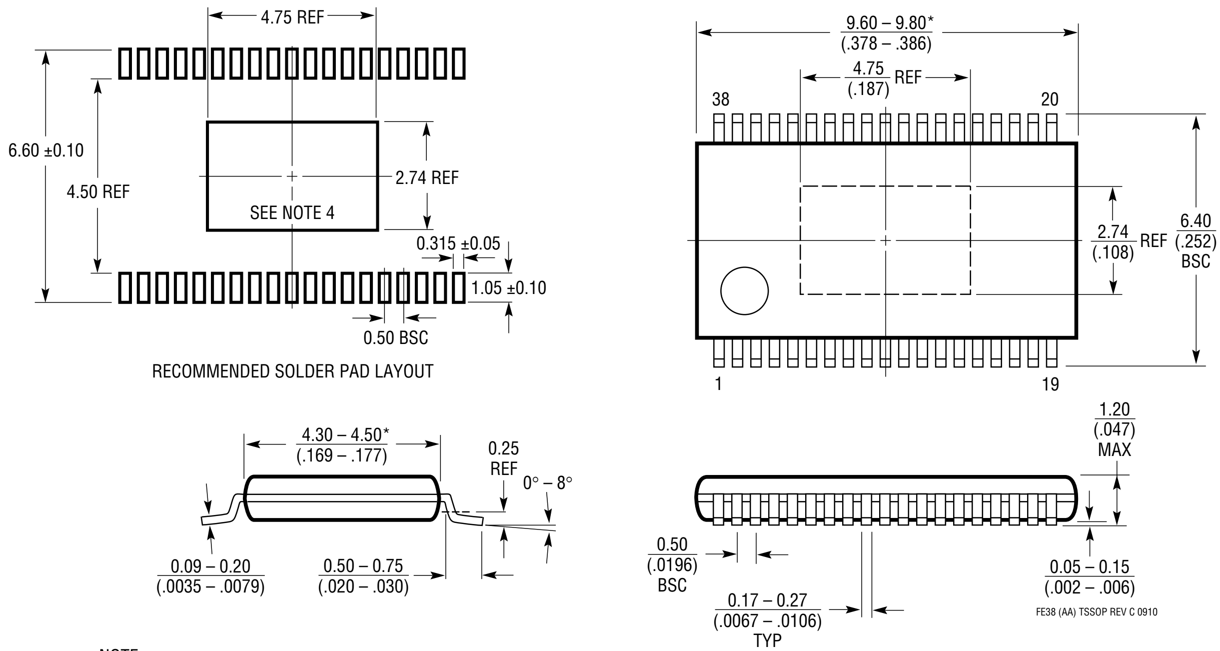
Combined Buck Regulators with Common Input Supply



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3371#packaging for the most recent package drawings.

FE Package
38-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1772 Rev C)
Exposed Pad Variation AA



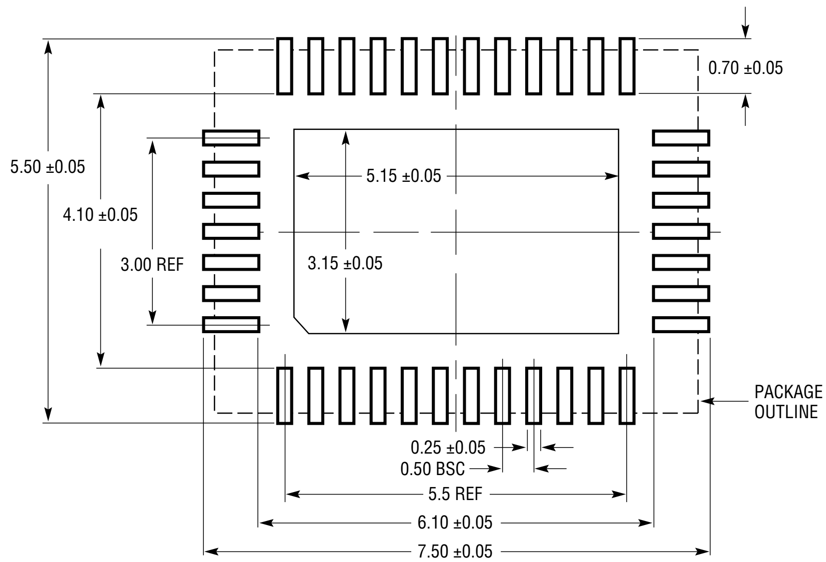
NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

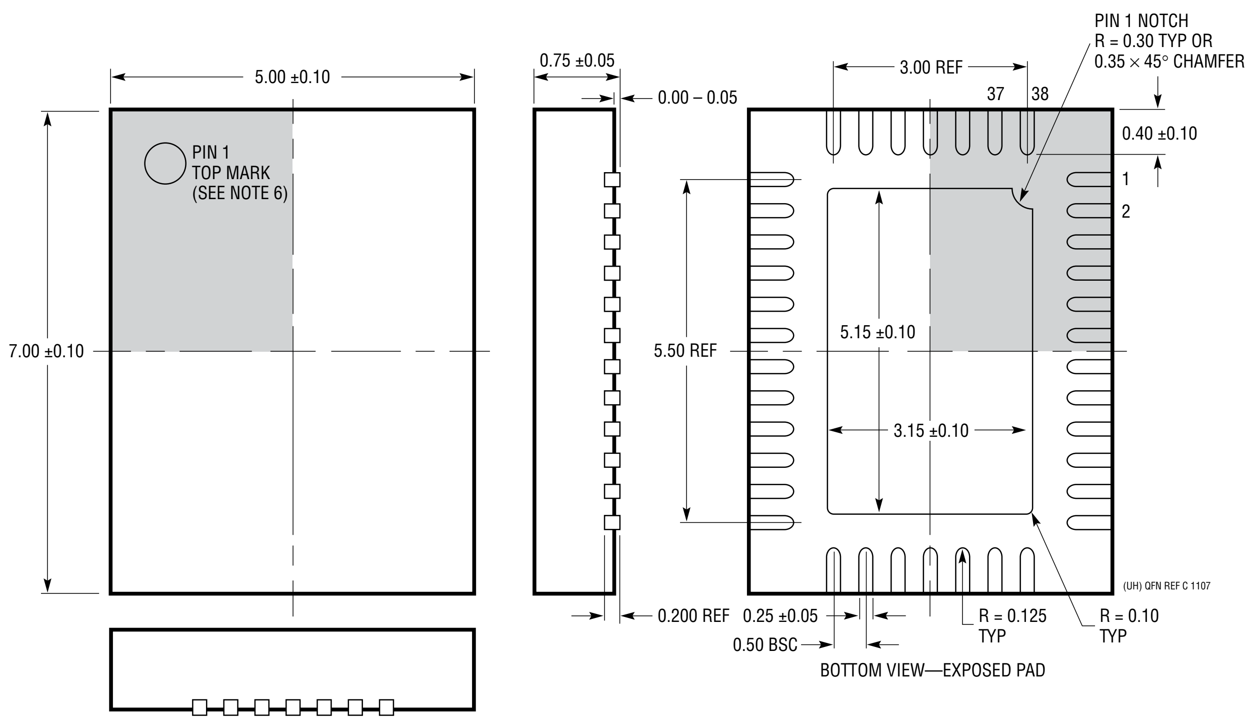
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3371#packaging for the most recent package drawings.

UHF Package
38-Lead Plastic QFN (5mm × 7mm)
(Reference LTC DWG # 05-08-1701 Rev C)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

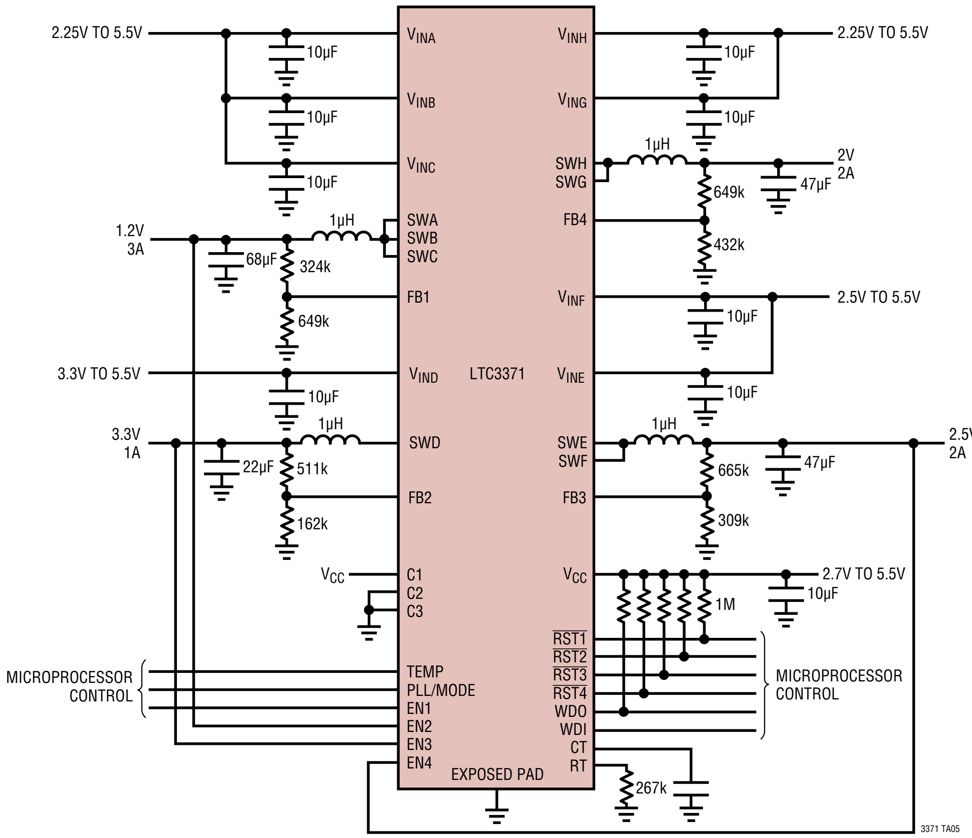
NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE M0-220 VARIATION WHKD
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	05/15	Modified Buck Efficiency graphs legends	1, 6
		Changed Recommended Inductor value, Table 3	19
		Modified Typical Application circuits	21, 22, 23, 26
B	06/16	Add QFN (UHF code) package drawing	24

TYPICAL APPLICATION

Combined Bucks with 3MHz Switching Frequency and Sequenced Power Up



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3589	8-Output Regulator with Sequencing and I^2C	Triple I^2C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A, 1A. High Efficiency 1.2A Buck-Boost DC/DC Converter, Triple 250mA LDO Regulators. Pushbutton On/Off Control with System Reset, Flexible Pin-Strap Sequencing Operation. I^2C and Independent Enable Control Pins, Dynamic Voltage Scaling and Slew Rate Control. Selectable 2.25MHz or 1.12MHz Switching Frequency, 8µA Standby Current, 40-Lead (6mm × 6mm × 0.75mm) QFN Package.
LTC3675	7-Channel Configurable High Power PMIC	Quad Synchronous Buck Regulators (1A, 1A, 500mA, 500mA). Buck DC/DCs Can be Paralleled to Deliver Up to 2× Current with a Single Inductor. 1A Boost, 1A Buck-Boost, 40V LED Driver. 44-Lead (4mm × 7mm × 0.75mm) QFN Package.
LTC3676	8-Channel Power Management Solution for Application Processors	Quad Synchronous Buck Regulators (2.5A, 2.5A, 1.5A, 1.5A). Quad LDO Regulators (300mA, 300mA, 300mA, 25mA). Pushbutton On/Off Control with System Reset. DDR Solution with VTT and VTTR Reference. 40-Lead (6mm × 6mm × 0.75mm) QFN Package.
LTC3375	8-Channel Programmable Configurable 1A DC/DC	8 × 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel to Make a Single Inductor, High Current Output (4A Maximum), 15 Output Configurations Possible, 48-Lead (7mm × 7mm × 0.75mm) QFN Package.
LTC3374	8-Channel Programmable Configurable 1A DC/DC	8 × 1A Synchronous Buck Regulators. Can Connect Up to Four Power Stages in Parallel to Make a Single Inductor, High Current Output (4A Maximum), 15 Output Configurations Possible, 38-Lead (5mm × 7mm × 0.75mm) QFN and TSSOP Packages.
LTC3370	4-Channel Configurable DC/DC with 8 × 1A Power Stages	4 Synchronous Buck Regulators with 8 × 1A Power Stages. Can Connect Up to Four Power Stages in Parallel to Make a Single Inductor, High Current Output (4A Maximum), 8 Output Configurations Possible, Precision PGOODALL Indication, 32-Lead (5mm × 5mm × 0.75mm) QFN Package.

3371fb

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