Wide V_{IN} Range Buck-Boost Charge Pump with Watchdog Timer

FEATURES

- **2.7V – 38V Operating Range (42V Abs Max)**
- **I_Q = 20µA Operating, 1.5µA in Shutdown**
- **Multimode Buck-Boost Charge Pump (2:1, 1:1, 1:2) with Automatic Mode Switching**
- **12V to 5V Efficiency = 81%**
- I_{OUT} Up to 500mA
- V_{OUT}: Fixed 3.3V, 5V or Adjustable (2.5V to 5V)
- Ultralow EMI Emissions
- Engineered for Diagnostic Coverage in ISO 26262 Systems
- Overtemperature, Overvoltage and Short-Circuit Protection
- Operating Junction Temperature: 150°C Max
- POR/Watchdog Controller w/External Timing Control
- Thermally Enhanced 16-Lead MSOP Package

APPLICATIONS

- Automotive ECU/CAN Transceiver Supplies
- Industrial/Telecom Housekeeping Supplies
- Low Power 12V to 5V Conversion

DESCRIPTION

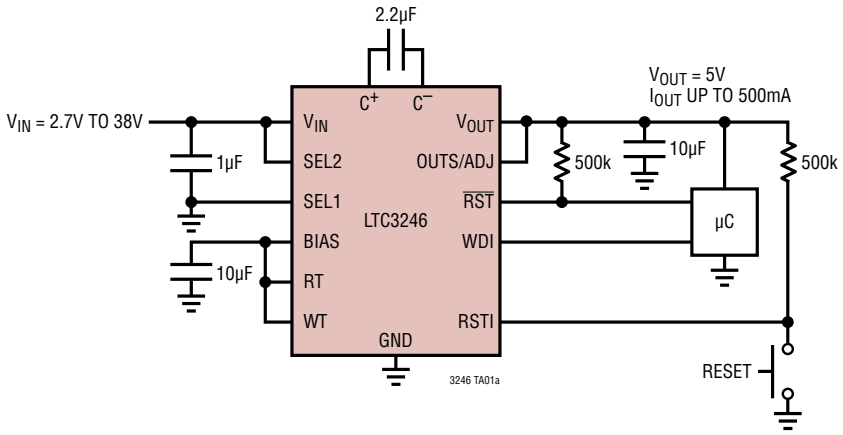
The LTC®3246 is a switched capacitor buck-boost DC/DC converter with integrated watchdog timer. The device produces a regulated output (3.3V, 5V or adjustable) from a 2.7V to 38V input. Switched capacitor fractional conversion is used to maintain regulation over a wide range of input voltage. Internal circuitry automatically selects the conversion ratio to optimize efficiency as input voltage and load conditions vary. No inductors are required.

The LTC3246's reset time and watchdog timeout may be set without external components, or adjusted using external capacitors. A windowed watchdog function is used for high reliability applications. The reset input can be used for additional supply monitoring or be configured as a pushbutton reset.

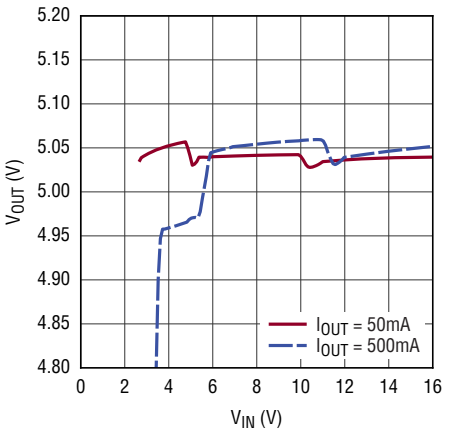
Low operating current (20µA without load, 1.5µA in shutdown) and low external parts count make the LTC3246 ideally suited for low power, space constrained automotive/industrial applications. The device is short-circuit and overtemperature protected and is available in a thermally enhanced 16-lead MSOP package.

TYPICAL APPLICATION

Regulated 5V Output with Pushbutton Reset



Output Voltage vs Input Voltage

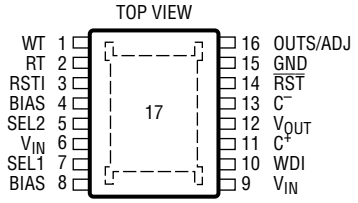


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{IN}, SEL1, SEL2, WDI ..... –0.3V to 42V
V_{OUT}, OUTS/ADJ, RSTI, WT, RT, BIAS, $\overline{RST}$. –0.3V to 6V
$I_{\overline{RST}}$ 10mA
V_{OUT} Short Circuit Duration ..... Indefinite
Lead Temperature (Soldering, 10 sec) ..... 300°C
Operating Junction Temperature Range (Notes 3, 4)
(E-Grade/I-Grade) ..... –40 to 125°C
(H-Grade) ..... –40 to 150°C
(MP-Grade) ..... –55 to 150°C
Storage Temperature Range ..... –65 to 150°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3246#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3246EMSE#PBF	LTC3246EMSE#TRPBF	3246	16-Lead Plastic MSOP	–40°C to 125°C
LTC3246IMSE#PBF	LTC3246IMSE#TRPBF	3246	16-Lead Plastic MSOP	–40°C to 125°C
LTC3246HMSE#PBF	LTC3246HMSE#TRPBF	3246	16-Lead Plastic MSOP	–40°C to 150°C
LTC3246MPMSE#PBF	LTC3246MPMSE#TRPBF	3246	16-Lead Plastic MSOP	–55°C to 150°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult ADI Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, C_{FLY} = 2.2µF, C_{OUT} = 10µF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Input Voltage Range	(Note 5)	●	2.7		38	V
V_{UVLO}	V_{IN} Undervoltage Lockout Threshold		●		2.35	2.7	V
I_{VIN}	V_{IN} Quiescent Current Shutdown CP Enabled, Output in Regulation	 SEL1 = SEL2 = 0V SEL1 = V_{IN} and/or SEL2 = V_{IN}, RSTI = 5V			 1.5 20	 3 30	 µA µA
V_{HIGH}	SEL1, SEL2 Input Voltage		●		1.1	1.6	V
V_{LOW}	SEL1, SEL2 Input Voltage		●	0.4	0.8		V
I_{LOW}	SEL1, SEL2 Input Current	V_{PIN} = 0V	●	–1	0	1	µA
I_{HIGH}	SEL1, SEL2 Input Current	V_{PIN} = 38V	●	0.5	1	2	µA
Charge Pump Operation							
V_{OUTS_5}	VOUTS/ADJ Regulation Voltage SEL1 = 0V, SEL2 = V_{IN}	2.7V < V_{IN} < 38V (Notes 5, 6)	●	4.8		5.2	V
V_{OUTS_3}	VOUTS/ADJ Regulation Voltage SEL1 = V_{IN}, SEL2 = V_{IN}	2.7V < V_{IN} < 38V (Notes 5, 6)	●	3.17		3.43	V
V_{ADJ}	VOUTS/ADJ Regulation Voltage SEL1 = V_{IN}, SEL2 = 0V	2.7V < V_{IN} < 38V (Notes 5, 6)	●	1.08	1.11	1.14	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, CFLY = 2.2µF, C_{OUT} = 10µF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{ADJ}	VOUTS/ADJ Input Current SEL1 = SEL2 = V_{IN}		●	–50	0	+50	nA
I_{OUT_SCKT}	I_{VOUT} Short Circuit Foldback Current	V_{OUT} = 0V			250		mA
R_{OUT}	Charge Pump Output Impedance	2:1 Step-Down Mode 1:1 Step-Down Mode, V_{IN} = 5.5V 1:2 Step-Up Mode, V_{IN} = 3V, V_{OUT} ≥ 3.3V (Note 6)	 ●		1 1.2 4	 8	Ω Ω Ω
$V_{OUT\_OV\_RST}$	V_{OUT} Overvoltage Reset	% of Final Regulation Voltage at Which V_{OUT} Rising Makes $\overline{RST}$ Go Low V_{OUT} Falling Makes $\overline{RST}$ Go Hi-Z	 ● ●	 106	 109 108.5	 111.5 	 % %
$V_{OUT\_UV\_RST}$	V_{OUT} Undervoltage Reset	% of Final Regulation Voltage at Which V_{OUT} Rising Makes $\overline{RST}$ Go Hi-Z V_{OUT} Falling Makes $\overline{RST}$ Go Low	 ● ●	 93	 97.5 95	 99 	 % %
V_{OUT_PD}	V_{OUT} Pull-Down in Shut Down	SEL1 = SEL2 = 0V			100		kΩ
V_{OUT_RIPPLE}	V_{OUT} Ripple Voltage	C_{OUT} = 10µF C_{OUT} = 22µF			50 25		mV mV
Reset Timer Control Pin (RT)							
$I_{RT(UP)}$	RT Pull-Up Current	V_{RT} = 0.3V	●	–2	–3.1	–4.2	µA
$I_{RT(DOWN)}$	RT Pull-Down Current	V_{RT} = 1.3V	●	2	3.1	4.2	µA
$I_{RT(INT)}$	Internal RT Detect Current	V_{RT} = V_{BIAS}	●		0.4	1	µA
$V_{RT(INT)}$	RT Internal Timer Threshold	V_{RT} Rising	●	2.0	2.4	2.65	V
Reset Timer Input (RSTI)							
V_{RSTI_H}	RSTI Input High Voltage		●		1.22	1.27	V
V_{RSTI_L}	RSTI Input Low Voltage		●	1.04	1.2		V
I_{RSTI_H}	RSTI Input High Current	RSTI = 5V	●	–1	0	1	µA
I_{RSTI_L}	RSTI Input Low Current	RSTI = 0V	●	–1	0	1	µA
Reset Timing							
$t_{RST(INT)}$	Internal Reset Timeout Period	V_{RT} = V_{BIAS}		150	200	270	ms
$t_{RST(EXT)}$	Adjustable Reset Timeout Period	C_{RT} = 2.2nF	●	14	21	28	ms
t_{RSTIL}	RSTI Low to $\overline{RST}$ Asserted		●	5	20	40	µs
Reset Output ($\overline{RST}$)							
$V_{OL(\overline{RST})}$	Output Voltage Low $\overline{RST}$	$I_{\overline{RST}}$ = 2mA	●		0.1	0.4	V
$I_{OH(\overline{RST})}$	$\overline{RST}$ Output Voltage High Leakage	$V_{\overline{RST}}$ = 5V	●	–1	0	1	µA
Watchdog Timing							
$t_{WDU(INT)}$	Internal Watchdog Upper Boundary	V_{WT} = V_{BIAS}	●	1.2	1.6	2.2	s
$t_{WDL(INT)}$	Internal Watchdog Lower Boundary	V_{WT} = V_{BIAS}	●	37.5	50	68	ms
$t_{WDR(EXT)}$	External Watchdog Timeout Period	C_{WT} = 2.2nF	●	100	160	220	ms
$t_{WDU(EXT)}$	External Watchdog Upper Boundary		●	$t_{WDR(EXT)}$ • (128/129)			ms
$t_{WDL(EXT)}$	External Watchdog Lower Boundary		●	$t_{WDR(EXT)}$ • (5/129)			ms
Watchdog Timer Input (WDI)							
V_{IH}	WDI Input High Voltage		●		1.1	1.6	V
V_{OL}	WDI Input Low Voltage		●	0.4	0.8		V
I_{IH}	WDI Input High Current	V_{WDI} = 38V	●	–1	0	1	µA
I_{IL}	WDI Input Low Current	V_{WDI} = 0V	●	–1	0	1	µA
$t_{PW(WDI)}$	Input Pulsewidth		●	400			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, CFLY = 2.2µF, C_{OUT} = 10µF, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Watchdog Timer Control Pin (WT)							
$I_{WT(UP)}$	WT Pull-Up Current	V_{WT} = 0.3V	●	–2	–3.1	–4.2	µA
$I_{WT(DOWN)}$	WT Pull-Down Current	V_{WT} = 1.3V	●	2	3.1	4.2	µA
$I_{WT(INT)}$	Internal WT Detect Current	V_{WT} = V_{BIAS}	●		0.4	1	µA
$V_{WT(INT)}$	WT Internal Timer Threshold	V_{WT} Rising	●	2	2.2	2.65	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are referenced to GND unless otherwise specified.

Note 3: The LTC3246E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3246I is guaranteed over the –40°C to 125°C operating junction temperature range. The LTC3246H is guaranteed over the –40°C to 150°C operating junction temperature range. The LTC3246MP is guaranteed and tested over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 4: This IC has overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

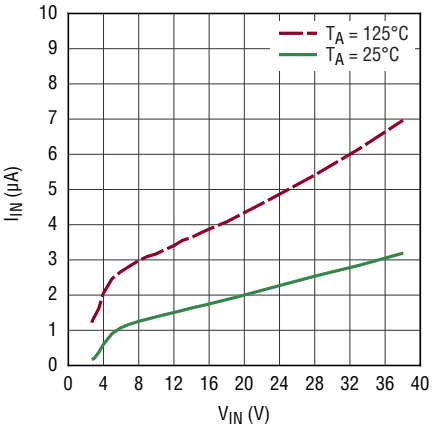
Note 5: The maximum operating junction temperature of 150°C must be followed. Certain combinations of input voltage, output current and ambient temperature will cause the junction temperature to exceed 150°C and must be avoided. See Thermal Management section for information on calculating maximum operating conditions.

Note 6: The LTC3246 will attempt to regulate the output voltage under all load conditions, but like any regulator, the output will drop out if inadequate supply voltage exists for the load. See V_{OUT} Regulation section for calculating available load current at low input operating voltages. Also see "Boost Output Impedance at Dropout vs Temperature" for typical impedance values at output voltages less than 3.3V.

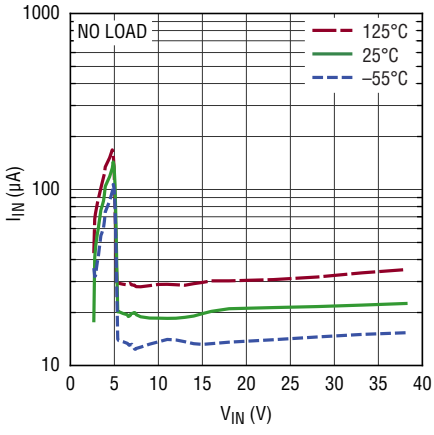
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

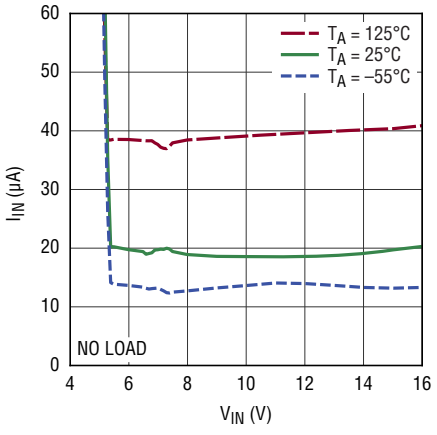
Input Shutdown Current vs Input Voltage



Input Operating Current vs Input Voltage

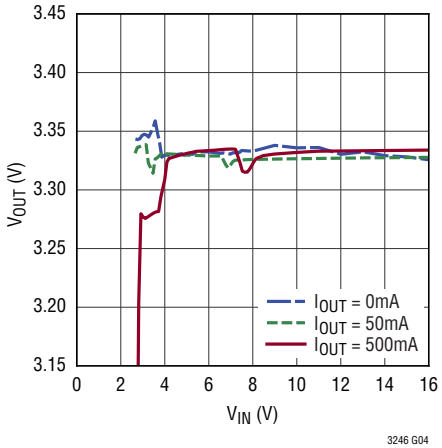


Input Operating Current vs Input Voltage

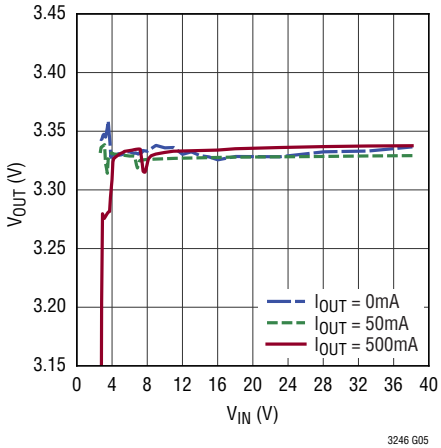


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

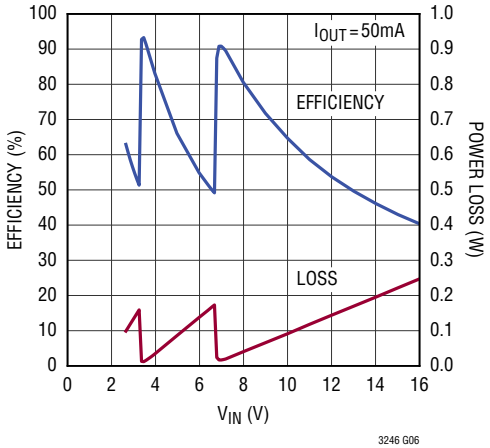
3.3V Fixed Output Voltage vs Input Voltage



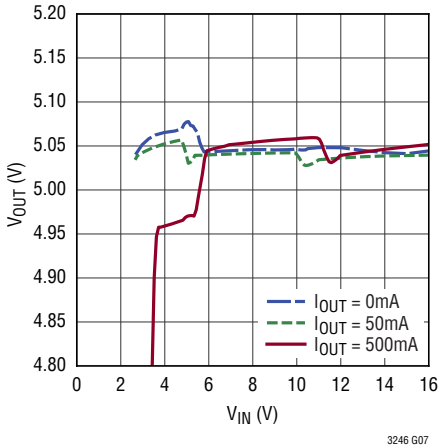
3.3V Fixed Output Voltage vs Input Voltage



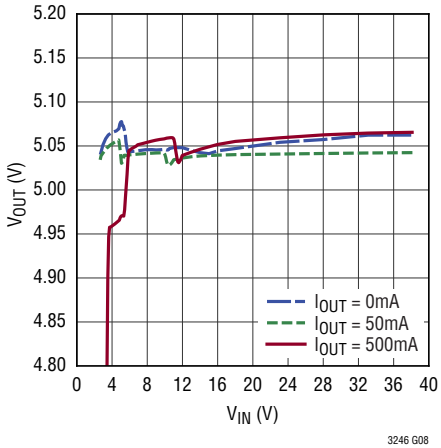
3.3V Efficiency and Power Loss vs Input Voltage



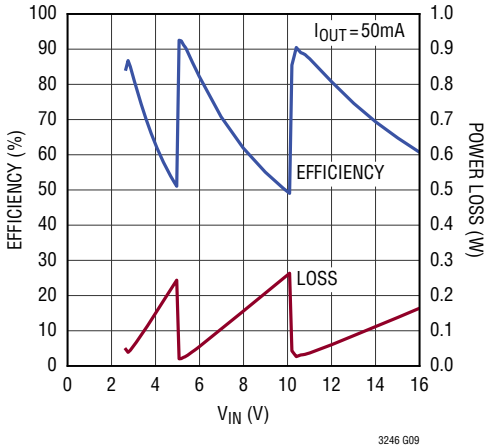
5V Fixed Output Voltage vs Input Voltage



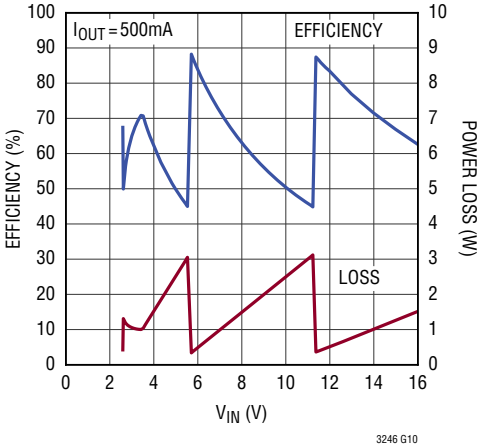
5V Fixed Output Voltage vs Input Voltage



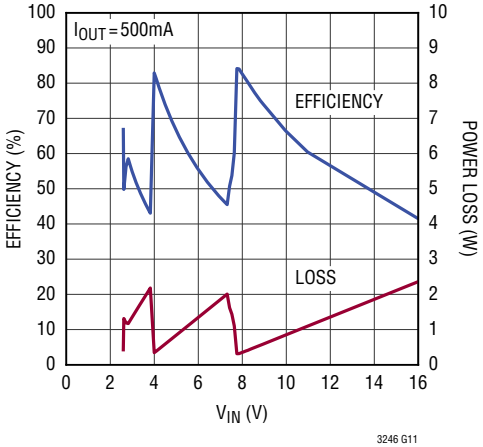
5V Efficiency and Power Loss vs Input Voltage



5V Efficiency and Power Loss vs Input Voltage

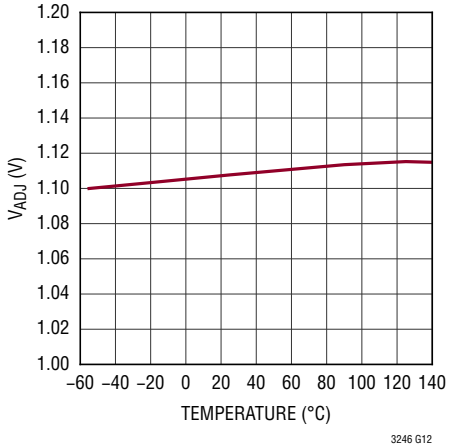


3.3V Efficiency and Power Loss vs Input Voltage

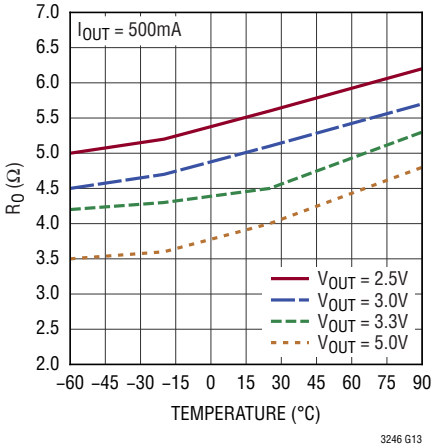


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

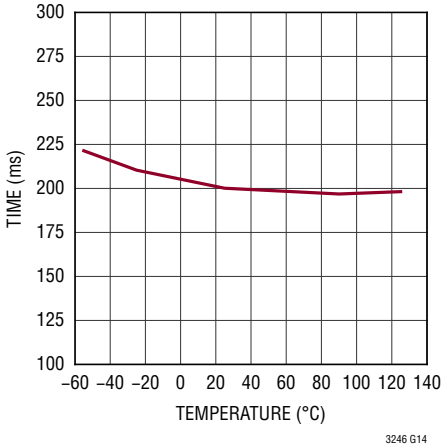
ADJ Regulation Voltage vs Temperature



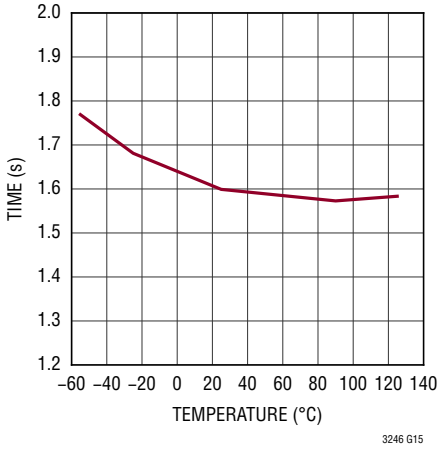
Boost Output Impedance at Dropout vs Temperature



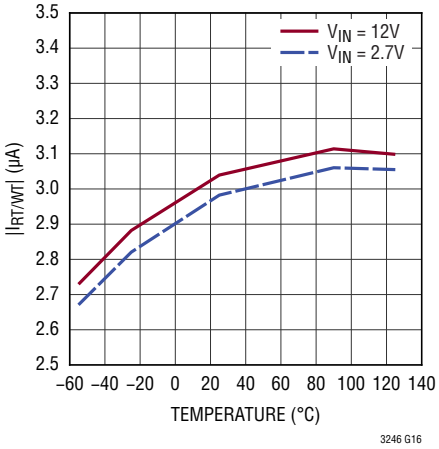
Internal Reset Timeout Period vs Temperature



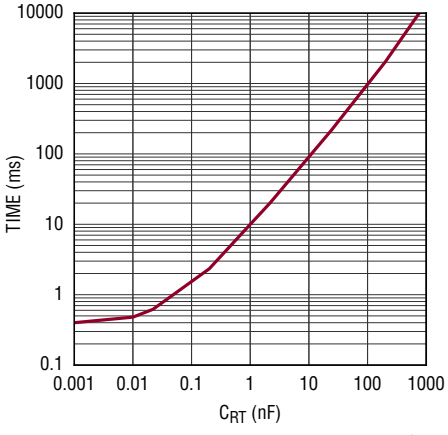
Internal Watchdog Timeout Period vs Temperature



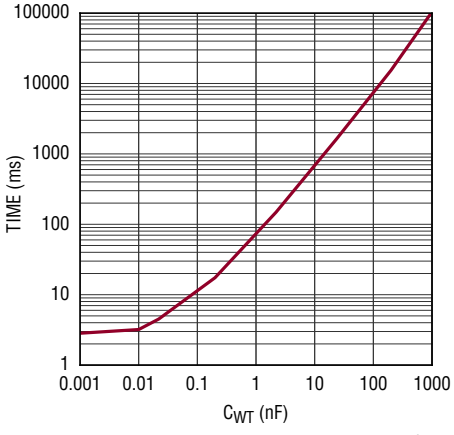
RT/WT Timer Control Current vs Temperature



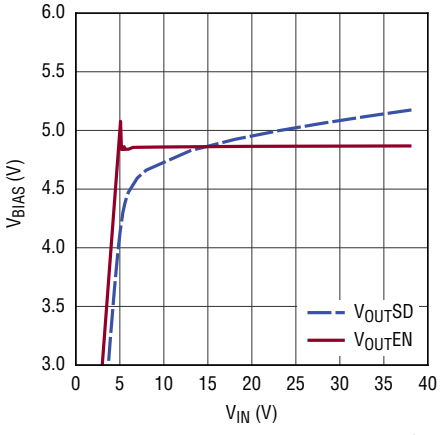
Reset Timeout Period vs C_{RT} Capacitance



Watchdog Timeout Period vs C_{WT} Capacitance

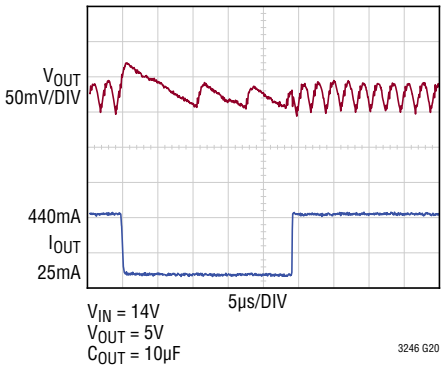


BIAS Output Voltage vs Input Voltage

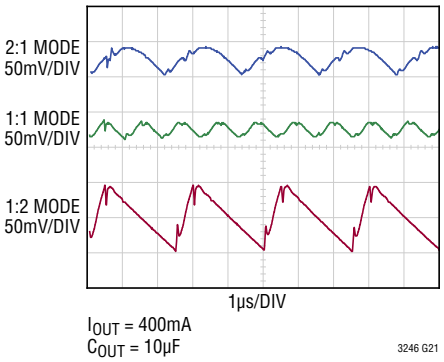


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Output Transient Response

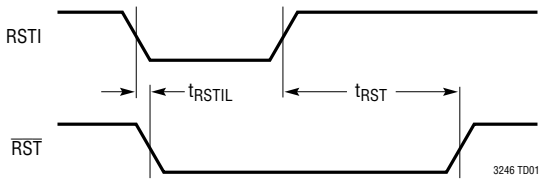


Output Voltage Ripple

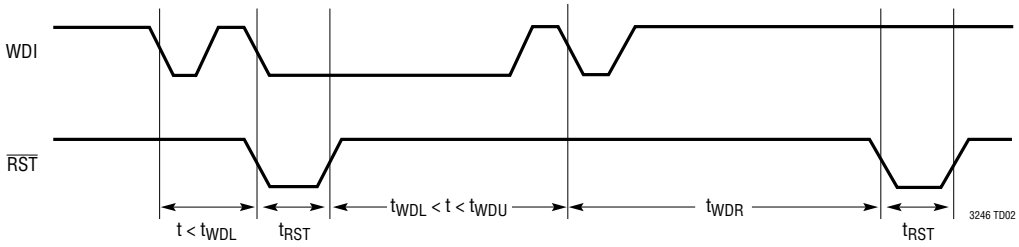


TIMING DIAGRAMS

Charge Pump Output Reset Timing



Watchdog Timing



PIN FUNCTIONS

WT (Pin 1): Watchdog Timer Control Pin. Attach an external capacitor (C_{WT}) to GND to set a watchdog upper boundary timeout time (See "Watchdog Timeout Period vs WT Capacitance" graph on page 6). Tie WT to BIAS to generate a timeout of about 1.6s. Tie WT and WDI to GND to disable the watchdog timer.

RT (Pin 2): Reset Timeout Control Pin. Attach an external capacitor (C_{RT}) to GND to set a reset timeout time (See "Reset Timeout Period vs RT Capacitance" graph on page 6). Tie RT to BIAS to generate a reset timeout of about 200ms.

RSTI (Pin 3): Reset Logic Comparator Pin. The RSTI input is compared to a reference threshold (1.2V typical). If RSTI is below the reference voltage, the part will enter the reset state and the $\overline{RST}$ pin will be low. Once RSTI exceeds the reference voltage and V_{OUT} in regulation, the reset timer is started. $\overline{RST}$ pin will be low until the reset period times out. RSTI is a high impedance pin and must be driven to a valid level. Do not float.

BIAS (Pin 4, 8): Internal BIAS Voltage. The bias pin is for internal operation only and should not be loaded or driven externally. Bypass BIAS with a 10µF or greater ceramic capacitor.

SEL2 (Pin 5): Logic Input Pin. See Table 1 for SEL1/SEL2 operating logic. SEL2 enables and disables the charge pump along with the SEL1 pin. The SEL2 pin has a 1µA (typical) pull down current to ground and can tolerate 38V inputs allowing it to be pin-strapped to V_{IN}.

V_{IN} (Pin 6, 9): Power Input Pin. Input voltage for both charge pump and IC control circuitry. The V_{IN} pin operates from 2.7V to 38V. All V_{IN} pins should be connected together at pins and bypassed with a 1µF or greater ceramic capacitor.

SEL1 (Pin 7): Logic Input Pin. See Table 1 for SEL1/SEL2 operating logic. SEL1 enables and disables the charge pump along with the SEL2 pin. The SEL1 pin has a 1µA (typical) pull down current to ground and can tolerate 38V inputs allowing it to be pin-strapped to V_{IN}.

Table 1. V_{OUT} Operating Modes

SEL2	SEL1	MODE
LOW	LOW	Shutdown
LOW	HIGH	Adjustable V_{OUT}
HIGH	LOW	Fixed 5V
HIGH	HIGH	Fixed 3.3V

WDI (Pin 10): Watchdog Logic Input Pin. If the watchdog timer is not disabled then WDI must be driven such that a falling edge occurs within a time less than the watchdog upper boundary time, or $\overline{RST}$ will be asserted low. The WDI period must also be greater than the watchdog lower boundary time, and only falling edges are considered. Tie WT and WDI to GND to disable the watchdog timer. WDI is a high impedance pin and must be driven to a valid level. Do not float.

C+ (Pin 11): Connect to positive flying capacitor terminal only. Do not load or drive externally.

V_{OUT} (Pin 12): Charge Pump Output Voltage. The charge pump output is enabled if either SEL1 or SEL2 are logic high.

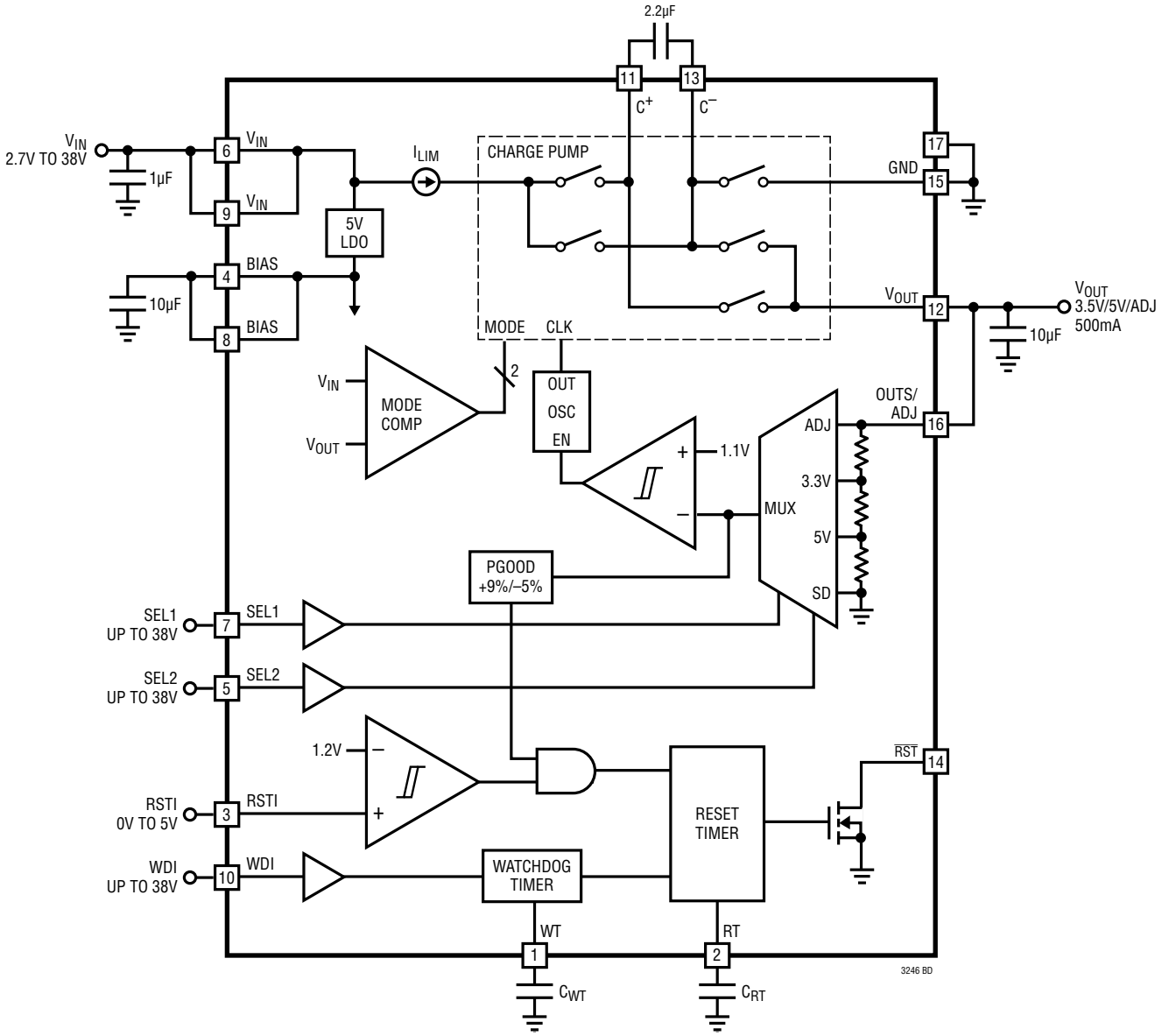
C- (Pin 13): Connect to negative flying capacitor terminal only. Do not load or drive externally.

$\overline{RST}$ (Pin 14): Reset Open Drain Logic Output. The $\overline{RST}$ pin is low impedance during the reset period, and goes high impedance during the watchdog period. $\overline{RST}$ is intended to be pulled up to low voltage supply (such as V_{OUT}) with an external resistor.

GND (Pin 15, Exposed Pad): Ground. The exposed package pad is ground and must be soldered to the PC board ground plane for proper functionality and for rated thermal performance.

OUTS/ADJ (Pin 16): V_{OUT} Sense/Adjust Input Pin. This pin acts as V_{OUT} sense (OUTS) for 5V or 3.3V fixed outputs and adjust (ADJ) for adjustable output through external feedback. The ADJ pin servos to 1.1V when the device is enabled in adjustable mode. (OUTS/ADJ are selected by SEL1 and SEL2 pins; See Table 1). Connect OUTS/ADJ to V_{OUT} or external divider as appropriate.

SIMPLIFIED BLOCK DIAGRAM



APPLICATIONS INFORMATION

General Operation

The LTC3246 uses switched capacitor based DC/DC conversion to provide the efficiency advantages associated with inductor based circuits as well as the cost and simplicity advantages of a linear regulator. The LTC3246 uses an internal switch network and fractional conversion ratios to achieve high efficiency and regulation over widely varying V_{IN} and output load conditions.

Internal control circuitry selects the appropriate conversion ratio based on V_{IN} and load conditions. The device has three possible conversion modes: 2:1 step-down mode, 1:1 step-down mode and 1:2 step-up mode. Only one external flying capacitor is needed to operate in all three modes. 2:1 mode is chosen when V_{IN} is greater than two times the desired V_{OUT}. 1:1 mode is chosen when V_{IN} falls between two times V_{OUT} and V_{OUT}. 1:2 mode is chosen when V_{IN} falls below the desired V_{OUT}. The internal mode control logic maintains output regulation over all load conditions.

Regulation is achieved by sensing the output voltage and enabling charge transfer when the output falls below regulation. When the charge pump is enabled, it controls the current into the flying capacitor to limit the output ripple beyond that of conventional switched capacitor charge pumps. The part has two SEL pins that select the output regulation (fixed 5V, fixed 3.3V or adjustable) as well as shutdown.

The charge pump operates at a nominal frequency of about 450kHz, though actual output ripple frequency will vary with output load, operating mode and output capacitance.

The LTC3246 is designed for applications requiring high system reliability. The part includes output supply monitoring and watchdog timing circuitry as well as overvoltage, short-circuit and overtemperature protection.

V_{OUT} Regulation and Mode Selection

Regulation is achieved by sensing the output voltage and enabling charge transfer when the output falls below the programmed regulation voltage. The amount of charge transferred per cycle is controlled over the full input range to minimize output ripple. The regulation voltage (fixed 5V, fixed 3.3V or adjustable) is selected through the SEL1 and SEL2 pins per Table 1 in the Pin Function section.

The optimal conversion ratio is chosen based on V_{IN}, V_{OUT} and output conditions. Two internal comparators are used to select the default conversion ratio. The conversion ratio switch point is optimized to provide peak efficiency over all supply and load conditions while maintaining regulation. Each comparator also has built-in hysteresis to reduce the tendency of oscillating between modes when a transition point is reached.

The LTC3246 will attempt to regulate its output over the full operating range (2.7V to 38V), but like any regulator the output will drop out of regulation if inadequate supply voltage exists to the operating load. As the input voltage drops, the LTC3246 will eventually end up in the 1:2 step up mode. As the input voltage drops further, the output will eventually drop out of regulation. At this point, the 1:2 step-up charge pump impedance can be calculated as:

$$R_{OUT} = \frac{2 \bullet V_{IN} - V_{OUT}}{I_{OUT}}$$

This equation can be rewritten to determine the output current at which the output will drop out for a given input voltage as:

$$I_{OUT} = \frac{2 \bullet V_{IN} - V_{OUT}}{R_{OUT}} \quad (I_{OUT} \leq 500mA)$$

For a typical 1:2 step-up charge pump impedance of 4Ω with 5V output voltage and 3V input voltage, the output current at dropout will be about:

$$I_{OUT} = \frac{2 \bullet 3 - 4.8}{4} mA = 300mA$$

Thus, typically the part should be able to output 300mA without dropping out. To be conservative, the max 1:2 step-up charge pump impedance of 8Ω should be used which gives a more conservative output current of 150mA.

Any supply impedance in series with the LTC3246 must be doubled and added to the 1:2 step-up charge pump impedance. It is also important to have the specified C_{OUT} and C_{FLY} capacitance to achieve the specified output impedance. Observing dropout will allow the user to calculate the output impedance for their specific application.

APPLICATIONS INFORMATION

Short-Circuit/Thermal Protection

The LTC3246 has built-in short-circuit current limiting on both the V_{OUT} and BIAS outputs to protect the part in the event of a short. During short-circuit conditions, the device will automatically limit the output current from both outputs.

The LTC3246 has thermal protection that will shut down the device if the junction temperature exceeds the overtemperature threshold (typically 175°C). Thermal shutdown is included to protect the IC in cases of excessively high ambient temperatures, or in cases of excessive power dissipation inside the IC. The charge transfer will reactivate once the junction temperature drops back to approximately 165°C.

When the thermal protection is active, the junction temperature is beyond the specified operating range. The thermal and short-circuit protection are intended for momentary overload conditions outside normal operation. Continuous operation above the specified maximum operating conditions may impair device reliability.

Programming the Output Voltage (OUTS/ADJ Pin)

The LTC3246 output voltage programming is very flexible offering a fixed 3.3V output, fixed 5V output as well as adjustable output that is programmed through an external resistor divider. The desired output regulation method is selected through the SEL pins.

For a fixed output simply short OUTS (OUTS/ADJ pin) to V_{OUT} as shown in Figure 1. Fixed 3.3V operation is enabled by driving both SEL1 and SEL2 pins high, while fixed 5V operating is selected by driving SEL2 high with SEL1 low. Driving both SEL1 and SEL2 low shuts down the device causing V_{OUT} to be pulled low by an internal impedance of about 80kΩ.

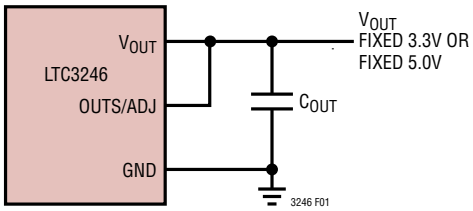


Figure 1. Fixed Output Operation

Adjustable output programming is accomplished by connecting ADJ (OUTS/ADJ pin) to a resistor divider between V_{OUT} and GND as shown in Figure 2. Adjustable operation is enabled by driving SEL1 high and SEL2 low. Driving both SEL1 and SEL2 low shuts down the device, causing V_{OUT} to be pulled low by an internal impedance of about 80kΩ.

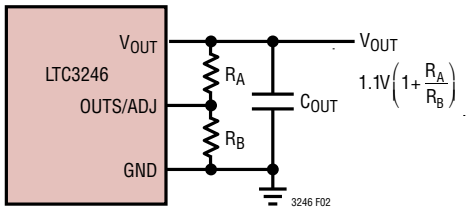


Figure 2. Adjustable Output Operation

Using adjustable operation, the output (V_{OUT}) can be programmed to regulate from 2.5V to 5V. The limited programming range provides the required V_{OUT} operating voltage without overstressing the V_{OUT} pin.

The desired adjustable output voltage is programmed by solving the following equation for R_A and R_B:

$$\frac{R_A}{R_B} = \frac{V_{OUT}}{1.11V} - 1$$

Select a value for R_B in the range of 1k to 1M and solve for R_A. Note that the resistor divider current adds to the total no load operating current. Thus, a larger value for R_B will result in lower operating current.

2:1 Step-Down Charge Pump Operation

When the input supply is greater than about two times the output voltage, the LTC3246 will operate in 2:1 step-down mode. Charge transfer happens in two phases. On the first phase, the flying capacitor (C_{FLY}) is connected between V_{IN} and V_{OUT}. On this phase, C_{FLY} is charged up and current is delivered to V_{OUT}. On the second phase, the flying capacitor (C_{FLY}) is connected between V_{OUT} and GND. The charge stored on C_{FLY} during the first phase is transferred to V_{OUT} on the second phase. When in 2:1 step-down mode, the input current will be approximately

APPLICATIONS INFORMATION

half of the total output current. The efficiency (η) and chip power dissipation (P_D) in 2:1 are approximately:

$$\eta \cong \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \frac{1}{2} I_{OUT}} = \frac{2V_{OUT}}{V_{IN}}$$

$$P_D = \left(\frac{V_{IN}}{2} - V_{OUT} \right) I_{OUT}$$

1:1 Step-Down Charge Pump Operation

When the input supply is less than about two times the output voltage, but more than the programmed output voltage, the LTC3246 will operate in 1:1 step-down mode. This method of regulation is very similar to a linear regulator. Charge is delivered directly from V_{IN} to V_{OUT} through most of the oscillator period. The charge transfer is briefly interrupted at the end of the period. When in 1:1 step-down mode, the input current will be approximately equal to the total output current. Thus, efficiency (η) and chip power dissipation (P_D) in 1:1 are approximately:

$$\eta \cong \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet I_{OUT}} = \frac{V_{OUT}}{V_{IN}}$$

$$P_D = \left(V_{IN} - V_{OUT} \right) I_{OUT}$$

1:2 Step-Up Charge Pump Operation

When the input supply is less than the output voltage, the LTC3246 will operate in 1:2 step-up mode. Charge transfer happens in two phases. On the first phase, the flying capacitor (C_{FLY}) is connected between V_{IN} and GND. On this phase, C_{FLY} is charged up. On the second phase, the flying capacitor (C_{FLY}) is connected between V_{IN} and V_{OUT} and the charge stored on C_{FLY} during the first phase is transferred to V_{OUT}. When in 1:2 step-up mode, the input current will be approximately twice the total output current. Thus, efficiency (η) and chip power dissipation (P_D) in 1:2 are approximately:

$$\eta \cong \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet 2I_{OUT}} = \frac{V_{OUT}}{2V_{IN}}$$

$$P_D = \left(2V_{IN} - V_{OUT} \right) I_{OUT}$$

V_{OUT} Ripple and Capacitor Selection

The type and value of capacitors used with the LTC3246 determine output ripple and charge pump strength. The value of C_{OUT} directly controls the amount of output ripple for a given load current. Output ripple decreases with output capacitance until about 20µF, at which point output peak to peak ripple remains more or less constant. See Figure 3 for graph of output ripple vs output capacitance.

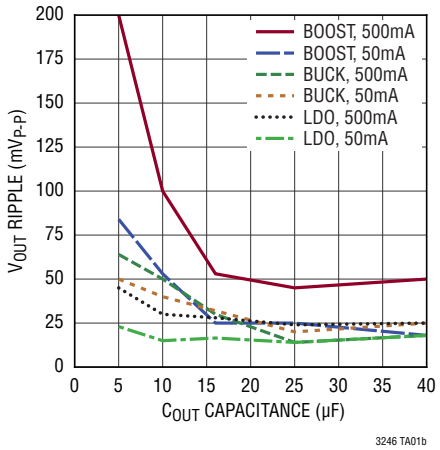


Figure 3. Typical V_{OUT} Ripple Voltage vs C_{OUT} Capacitance

To reduce output noise and ripple, it is suggested that a low ESR (equivalent series resistance < 0.1Ω) ceramic capacitor (10µF or greater) be used for C_{OUT}. For optimal performance, it is best to increase C_{OUT} for low V_{OUT} as the ripple becomes a larger percentage of the regulation voltage degrading performance. Tantalum and aluminum capacitors can be used in parallel with a ceramic capacitor to increase the total capacitance but are not recommended to be used alone because of their high ESR.

V_{OUT} Overvoltage Protection

An internal comparator monitors the voltage at V_{OUT} and will prevent charge transfer in the event that V_{OUT} exceeds the overvoltage threshold (5.9V typ.). Overvoltage protection is added as a safety feature to prevent damage to the part in the event of a fault such as VOUTS/ADJ pin shorted to ground or not connected to V_{OUT}. Charge transfer will start once the output falls to about 5.75V.

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V_{IN} Capacitor Selection

The finite charge transfer architecture used by the LTC3246 makes input noise filtering much less demanding than the sharp current spikes of conventional regulated charge pumps. Depending on the mode of operation, the input current of the LTC3246 can step from about 1A to 0A on a cycle-by-cycle basis. Low ESR will reduce the voltage steps caused by changing input current, while the absolute capacitor value will determine the level of ripple. The total amount and type of capacitance necessary for input bypassing is very dependent on the applied source impedance as well as existing bypassing already on the V_{IN} node. For optimal input noise and ripple reduction, it is recommended that a low ESR ceramic capacitor be used for C_{IN} bypassing. An electrolytic or tantalum capacitor may be used in parallel with the ceramic capacitor on C_{IN} to increase the total capacitance, but, due to the higher ESR, it is not recommended that an electrolytic or tantalum capacitor be used alone for input bypassing. The LTC3246 will operate with capacitors less than 1µF, but, depending on the source impedance, input noise can feed through to the output causing degraded performance. For best performance 1µF or greater total capacitance is suggested for C_{IN}.

Flying Capacitor Selection

Ceramic capacitors should always be used for the flying capacitor. The flying capacitor controls the strength of the charge pump. In order to achieve the rated output current, it is necessary for the flying capacitor to have at least 1µF of capacitance over operating temperature with a bias voltage equal to the programmed V_{OUT} (see Ceramic Capacitor Selection Guidelines). If only 100mA or less of output current is required for the application, the flying capacitor minimum can be reduced to 0.2µF. The voltage rating of the ceramic capacitor should be V_{OUT} + 1V or greater.

Ceramic Capacitor Selection Guidelines

Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X5R or X7R material will retain most of its capacitance from –40°C to 85°C, whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range (60% to 80% loss typical). Z5U and Y5V capacitors may also have a very strong voltage coefficient, causing them to lose an additional 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than discussing the specified capacitance value. For example, over rated voltage and temperature conditions, a 4.7µF, 10V, Y5V ceramic capacitor in an 0805 case may not provide any more capacitance than a 1µF, 10V, X5R or X7R available in the same 0805 case. In fact, over bias and temperature range, the 1µF, 10V, X5R or X7R will provide more capacitance than the 4.7µF, 10V, Y5V. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitance values are met over operating temperature and bias voltage. Below is a list of ceramic capacitor manufacturers and how to contact them:

MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
Kemet	www.kemet.com
Murata	www.murata
Taiyo Yuden	www.t-yuden.com
TDK	www.tdk.com
Wurth Elektronik	www.we-online.com

BIAS Pin and Capacitor Selection

The BIAS pin of the LTC3246 is a 5V output that is generated by an internal Low Drop-Out (LDO) regulator supplied by V_{IN}. The BIAS voltage is used as a supply for the internal low voltage circuitry. A capacitor on the BIAS pin is necessary to stabilize the LDO output and minimize ripple during transient conditions. A low ESR ceramic capacitor with a minimum capacitance of 2µF over temperature with 5V bias should be used. Since the BIAS voltage comes from an LDO, the BIAS voltage will drop with V_{IN} as V_{IN} goes below 5V. This is normal and expected operation. The BIAS pin voltage is for internal circuitry only and should not be loaded externally.

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Reset Generation (RSTI input, $\overline{RST}$ output)

The LTC3246 pulls the $\overline{RST}$ open-drain output low whenever RSTI is below threshold (typically 1.2V) or V_{OUT} is greater than the overvoltage threshold or less than the undervoltage threshold. $\overline{RST}$ remains asserted low for a reset timeout period (t_{RST}) once RSTI goes above the threshold and V_{OUT} is in regulation (within the overvoltage and undervoltage thresholds). $\overline{RST}$ de-asserts by going high impedance at the end of the reset timeout period.

The reset timeout can be configured to use an internal timer without external components or an adjustable timer programmed by connecting an external capacitor from the RT pin to GND. Glitch filtering ensures reliable reset operation without false triggering.

During initial power up, the $\overline{RST}$ output asserts low while V_{IN} is below the V_{IN} undervoltage lockout threshold. The state of V_{OUT} and RSTI have no effect on $\overline{RST}$ while V_{IN} is below the undervoltage lockout threshold. The reset timeout period cannot start until V_{IN} exceeds the undervoltage lockout threshold.

V_{OUT} Undervoltage/Overvoltage Reset

A built-in V_{OUT} supply monitor ensures the V_{OUT} is in regulation before $\overline{RST}$ is allowed to go high impedance. The monitor detects both overvoltage and undervoltage faults.

If V_{OUT} is greater than the overvoltage threshold or less than the undervoltage threshold, the part registers a fault and pulls $\overline{RST}$ low. The fault condition is removed when V_{OUT} is within the overvoltage and undervoltage thresholds.

Load transients within the operating range of the part will not registering as a fault by design.

Selecting the Reset Timing Capacitor

The reset timeout period can be set to a fixed internal timer or programmed with a capacitor in order to accommodate a variety of applications. Connecting a capacitor, C_{RT}, between the RT pin and GND sets the reset timeout period, t_{RST}.

Figure 4 shows the desired reset timeout period as a function of the value of the timer capacitor. Leaving RT open without external capacitor generates a reset timeout of approximately 0.5ms. Shorting RT to BIAS generates a reset timeout of approximately 0.2s.

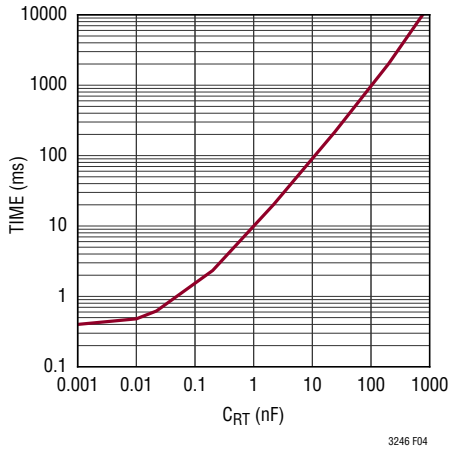


Figure 4. Reset Timeout Period vs C_{RT} Capacitance

$\overline{RST}$ Output Characteristics

$\overline{RST}$ is an open-drain pin and, thus, requires an external pull-up resistor to a logic supply. $\overline{RST}$ may be pulled up to any valid logic level (such as V_{OUT}) providing the voltage limits of the pin are observed (See Absolute Maximum Ratings section).

Watchdog Timer (WDI input, $\overline{RST}$ output)

The LTC3246 includes a windowed watchdog function that can continuously monitor the application's logic or microprocessor and issue automatic resets to aid recovery from unintended lockups or crashes. With the RSTI input held above threshold, the application must periodically toggle the logic state of the watchdog input (WDI pin) in order to clear the watchdog timer. Specifically, successive falling edges on the WDI pin must be spaced by more than the watchdog lower boundary but less than the watchdog upper boundary. As long as this condition holds, $\overline{RST}$ remains high impedance.

If a falling edge arrives before the watchdog lower boundary, or if the watchdog timer reaches the upper boundary without seeing a falling edge on WDI, the watchdog timer immediately enters its reset state and asserts $\overline{RST}$

APPLICATIONS INFORMATION

low for the reset timeout period. Once the reset timeout completes, $\overline{RST}$ is released to go high and the watchdog timer starts again.

During power-up, the watchdog timer remains cleared while $\overline{RST}$ is asserted low. As soon as the reset timer times out, $\overline{RST}$ goes high and the watchdog timer is started.

Setting the Watchdog Timeout Period

The watchdog upper boundary (t_{WDU}) and lower boundary (t_{WDL}) are not observable outside the part; only the watchdog timeout period (t_{WDR}) of the part is observable via the $\overline{RST}$ pin. The watchdog upper boundary (t_{WDU}) occurs one watchdog clock cycle before the watchdog timeout period (t_{WDR}). The *internal* watchdog timeout period consists of 8193 clock cycles, so the *internal* watchdog upper boundary time is essentially the same as the internal watchdog timeout period. Conversely, the *external* watchdog timeout period consists of only 129 clock cycles, so the *external* watchdog upper boundary should be more accurately calculated as:

$$t_{WDU(EXT)} = t_{WDR(EXT)} \bullet \frac{128}{129}$$

The *external* watchdog lower boundary ($t_{WDL(EXT)}$) occurs five clock cycles into the watchdog timeout period ($t_{WDR(EXT)}$). Thus the *external* watchdog lower boundary can be calculated from the *external* watchdog timeout period as:

$$t_{WDL(EXT)} = t_{WDR(EXT)} \bullet \frac{5}{129}$$

The *internal* watchdog lower boundary can be calculated from the *internal* watchdog timeout period by the following:

$$t_{WDL(INT)} = \frac{t_{WDR(INT)}}{32}$$

The watchdog upper boundary is adjustable and can be optimized for software execution. The watchdog upper boundary is adjusted by connecting a capacitor, C_{WT}, between the WT and GND pins.

Figure 5 shows the approximate external watchdog timeout period as a function of the watchdog capacitor. Shorting WT to BIAS sets an upper and lower watchdog timeout period of about 50ms and 1.6s respectively.

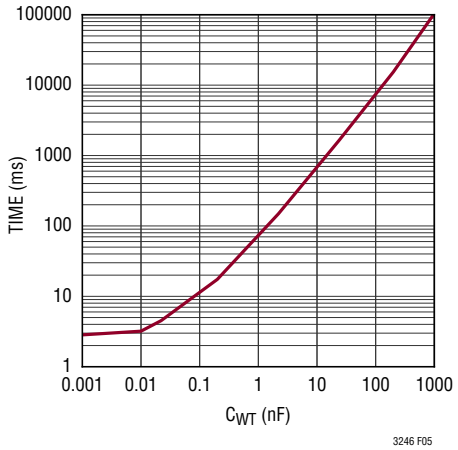


Figure 5. External Watchdog Timeout Period vs C_{WT} Capacitance

Layout Considerations

Due to the high switching frequency and transient currents produced by the LTC3246, careful board layout is necessary for optimal performance. A true ground plane and short connections to all capacitors will optimize performance, reduce noise and ensure proper regulation over all conditions.

When using the LTC3246 with an external resistor divider it is important to minimize any stray capacitance to the ADJ (OUTS/ADJ pin) node. Stray capacitance from ADJ to C^+ or C^- can degrade performance significantly and should be minimized and/or shielded if necessary. Minimize stray capacitance from WT and RT to C^+ and C^- when using external timing capacitors to minimize timing variation.

Thermal Management/Thermal Shutdown

The on-chip power dissipation in the LTC3246 will cause the junction to ambient temperature to rise at rate of typically 40°C/W in still air with a good thermal connection to the PC board. Connecting the die pad (Pin 17) with multiple vias to a large gro und plane under the device can reduce the thermal resistance of the package and PC board con-

APPLICATIONS INFORMATION

siderably. Poor board layout and failure to connect the die pad (Pin 17) to a large ground plane can result in thermal junction to ambient impedance well in excess of 40°C/W. It is also possible to get thermal rates less than 40°C/W with good airflow over the part and PC board.

Because of the wide input operating range, it is possible to exceed the specified operating junction temperature and even reach thermal shutdown (175°C typ). Figure 6 and Figure 7 show the available output current vs ambient temperature to ensure the 150°C operating junction temperature is not exceeded.

The figures assume worst-case operating conditions and a thermal impedance of 40°C/W. It is always safe to operate under the line shown on the graph. Operation above the line is conditional and is the responsibility of the user to calculate worst-case operating conditions (temperature and power) to make sure the part does not exceed the 150°C operating junction temperature for extended periods of time.

The 2:1 Step-Down Charge Pump Operation, 1:1 Step-Down Charge Pump Operation, and 1:2 Step-Up Charge Pump Operation sections provide equations for calculating power dissipation (P_D) in each mode.

For example, if it is determined that the maximum power dissipation (P_D) is 1.2W under normal operation, then the junction to ambient temperature rise will be:

$$T_{JA} = 1.2W \bullet 40°C/W = 48°C$$

Thus, the ambient temperature under this condition cannot exceed 102°C if the junction temperature is to remain below 150°C, and, if the ambient temperature exceeds about 127°C, the device will cycle in and out of the thermal shutdown.

Every application will have a slightly different thermal rise than the specified 40°C/W, especially applications with good airflow. Calculating the actual thermal rate for a specific application circuit is too complex to be presented here, but the thermal rate can be measured in application. This is done by first taking the final application circuit and enabling the LTC3246 under a known power dissipation (P_D) and raising the ambient temperature slowly until the LTC3246 shuts down. Note this temperature as T1. Now, remove the load from the part and raise the ambient temperature slowly until the LTC3246 shuts down again. Note this temperature as T2. The thermal rate can be calculated as:

$$\theta_{JA} = P_D/(T2 - T1)$$

Another method for determining maximum safe operating temperature in application is to configure the LTC3246 to operate under the worst case operating power dissipation. Then slowly raise the ambient temperature until the LTC3246 shuts down. At this point the LTC3246 junction temperature will be about 175°C, so simply subtract 25°C from the shutdown temperature and this is the safe operating temperature for the application.

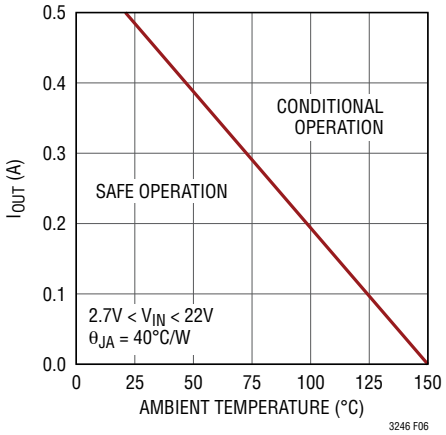


Figure 6. 5V Output Operation vs Ambient Temperature

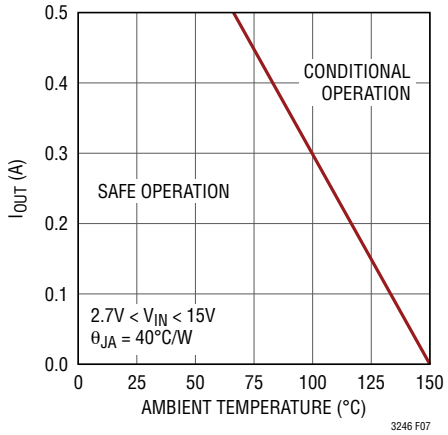
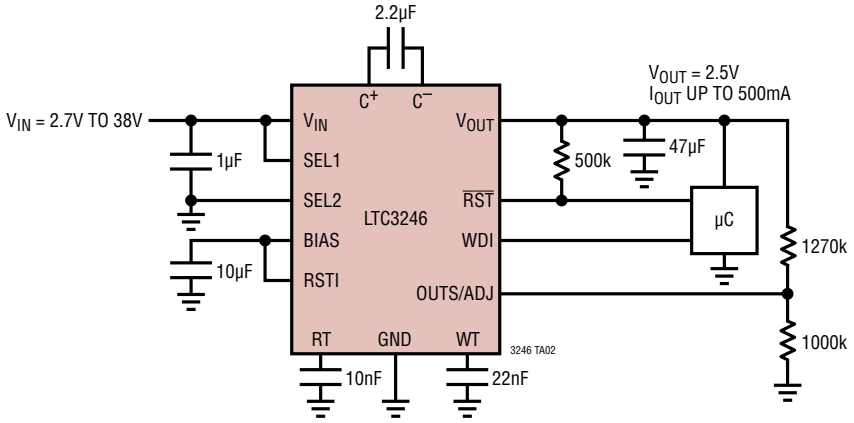


Figure 7. 3.3V Output Operation vs Ambient Temperature

TYPICAL APPLICATIONS

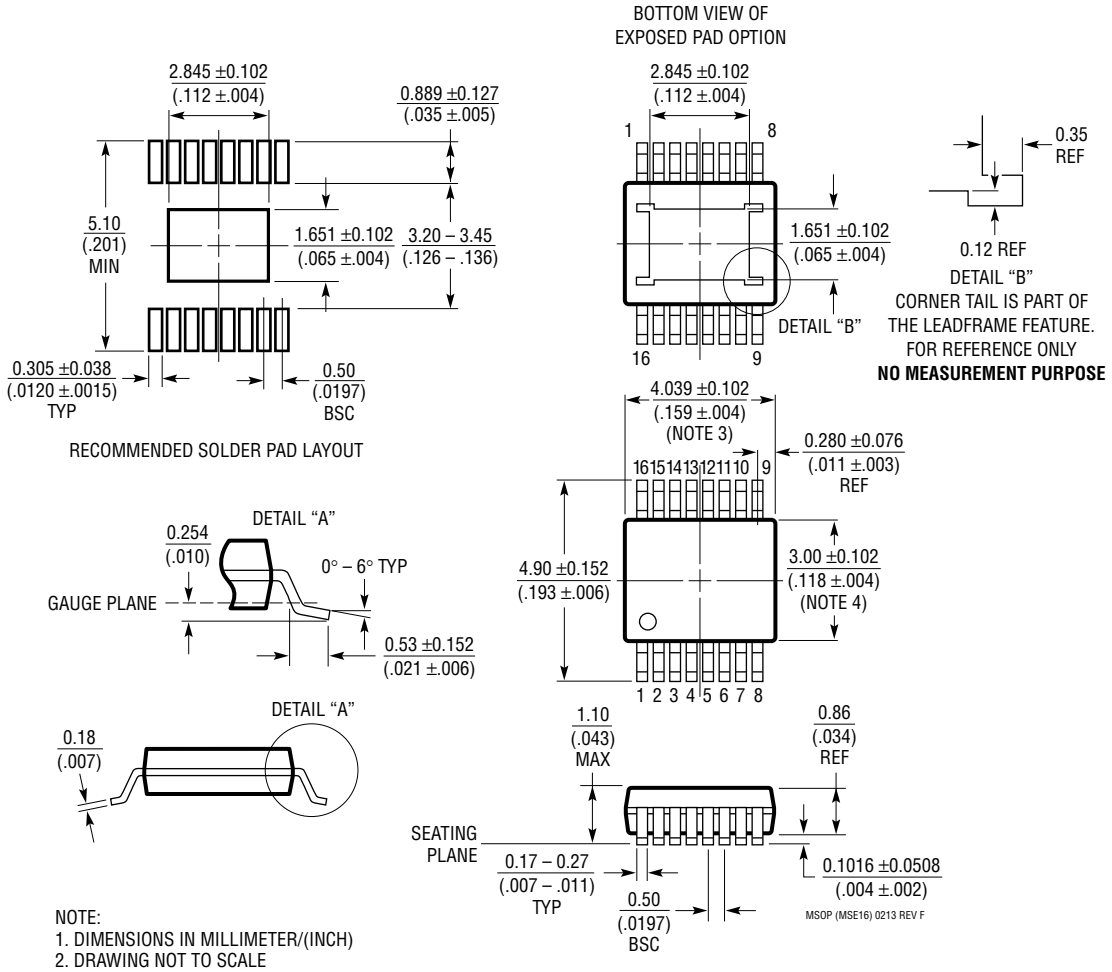
Regulated 2.5V Output with Externally Programmed Watchdog Timing



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC3246#packaging for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



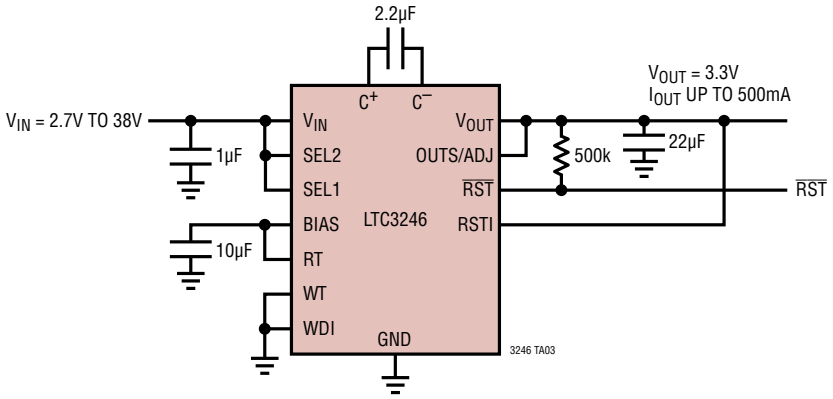
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/17	Changed R_{OUT} V_{IN} condition	3
		Changed V_{RSTI_L} lower limit	3
		Changed I_{OUT} equation resultant to 300mA and text to 150mA	10
		Changed circuit pin names	17

TYPICAL APPLICATION

Reduced Ripple 3.3V Output with Watchdog Timing Disabled



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3204-3.3/ LTC3204B-3.3/ LTC3204-5/ LTC3204B-5	Low Noise, Regulated Charge Pumps in (2mm × 2mm) DFN Package	V_{IN}: 1.8V to 4.5V (LTC3204B-3.3), 2.7V to 5.5V (LTC3204B-5), I_Q = 48µA, B Version without Burst Mode Operation, 6-Lead (2mm × 2mm) DFN Package
LTC3440	600mA (I_{OUT}) 2MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤ 1µA, 10-Lead MS Package
LTC3441	High Current Micropower 1MHz Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 2.5V, I_Q = 25µA, I_{SD} ≤ 1µA, DFN Package
LTC3443	High Current Micropower 600kHz Synchronous Buck-Boost DC/DC Converter	96% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$ = 2.4V, I_Q = 28µA, I_{SD} < 1µA, DFN Package
LTC3240-3.3/ LTC3240-2.5	3.3V/2.5V Step-Up/Step-Down Charge Pump DC/DC Converter	V_{IN}: 1.8V to 5.5V, $V_{OUT(MAX)}$ = 3.3V/2.5V, I_Q = 65µA, I_{SD} < 1µA, 2mm × 2mm DFN Package
LTC3260	Low Noise Dual Supply Inverting Charge Pump	V_{IN} Range: 4.5V to 32V, I_Q = 100µA, 100mA Charge Pump, 50mA Positive LDO, 50mA Negative LDO
LTC3261	High Voltage Low I_Q Inverting Charge Pump	V_{IN} Range: 4.5V to 32V, I_Q = 60µA, 100mA Charge Pump
LTC3245	High Voltage, Low Noise 250mA Buck-Boost Charge Pump	V_{IN} Range: 2.7V to 38V, V_{OUT} Range: 2.5V to 5V, I_Q = 18µA, I_{SD} = 4µA, 3mm × 4mm DFN and 12-Pin MSE Packages
LTC3255	Wide V_{IN} Range Fault Protected 50mA Step-Down Charge Pump	V_{IN} Range: 4V to 48V, V_{OUT} Range: 2.4V to 15V, I_Q = 20µA, 10-Pin 3mm × 3mm DFN and MSE Packages
LTC3256	Wide V_{IN} Range Dual Output 350mA Step-Down Charge Pump with WDT	V_{IN} Range: 5.5V to 38V, V_{OUT} Range: 5V/3.3V, I_Q = 18µA, 16-Pin MSE Package

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