# Precision Dual Supply Monitors with Pin-Selectable Thresholds

## FEATURES

- **Monitors Two Inputs Simultaneously**
- **Nine Threshold Combinations**
- **Three Supply Tolerances (5%, 7.5%, 10%)**
- **Guaranteed Threshold Accuracy: ±1.5% of Monitored Voltage Over Temperature**
- **Internal $V_{CC}$ Auto Select**
- Power Supply Glitch Immunity
- 200ms Reset Time Delay (LTC2904 Only)
- Adjustable Reset Time Delay (LTC2905 Only)
- Open Drain $\overline{RST}$ Output
- Guaranteed $\overline{RST}$ for V1 ≥ 1V or V2 ≥ 1V
- Low Profile (1mm) SOT-23 (ThinSOT™) and Plastic (3mm × 2mm) DFN Packages

## APPLICATIONS

- Desktop and Notebook Computers
- Handheld Devices
- Network Servers
- Core, I/O Monitor

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## DESCRIPTION

The LTC®2904/LTC2905 are dual supply monitors intended for systems with two supply voltages. The dual supply monitors have a common reset output with delay (200ms for the LTC2904 and adjustable using an external capacitor for the LTC2905). This product provides a precise, space-conscious and micropower solution for supply monitoring.

The LTC2904/LTC2905 feature a tight 1.5% threshold accuracy over the whole operating temperature range, and glitch immunity to ensure reliable reset operation without false triggering. The open drain $\overline{RST}$ output is guaranteed to be in the correct state for inputs down to 1V.

The LTC2904/LTC2905 also feature three programming input pins, which program the threshold and tolerance level without requiring any external components. These three programming pins provide a total of 27 different voltage level and tolerance combinations, eliminating the need to have different parts for development and implementation of different systems with different voltage levels requiring monitoring function.

## TYPICAL APPLICATION

**5V, 3.3V Dual Supply Monitor with 5% Tolerance**

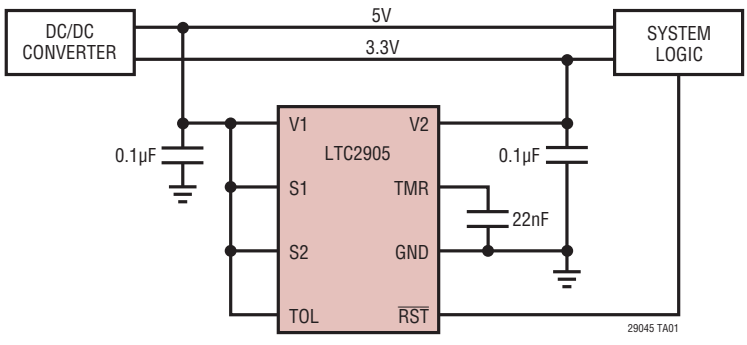



**Table 1. Voltage Threshold Programming**

| V1 | V2 | S1 | S2 |
|---|---|---|---|
| 5.0 | 3.3 | V1 | V1 |
| 3.3 | 2.5 | Open | GND |
| 3.3 | 1.8 | V1 | Open |
| 3.3 | 1.5 | Open | V1 |
| 3.3 | 1.2 | Open | Open |
| 2.5 | 1.8 | GND | GND |
| 2.5 | 1.5 | GND | Open |
| 2.5 | 1.2 | GND | V1 |
| 2.5 | 1.0 | V1 | GND |

## ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

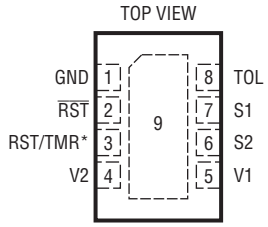
Terminal Voltages
- V1, V2 ..... –0.3V to 7V
- S1, S2, TOL ..... –0.3V to ($V_{CC}$ +0.3V)
- $\overline{RST}$ ..... –0.3V to 7V
- RST (LTC2904) ..... –0.3V to 7V
- TMR (LTC2905) ..... –0.3V to 7V

Operating Temperature Range
- LTC2904C/LTC2905C ..... 0°C to 70°C
- LTC2904I/LTC2905I ..... –40°C to 85°C
- LTC2905H ..... –40°C to 125°C

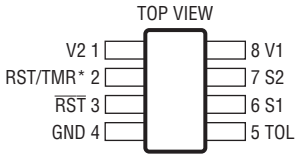
Storage Temperature Range ..... –65°C to 150°C

TSOT Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION




DDB8 PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
EXPOSED PAD IS GND (PIN 9),
MUST BE SOLDERED TO PCB
* RST FOR LTC2904
TMR FOR LTC2905
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 76°C/W




TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
* RST FOR LTC2904
TMR FOR LTC2905
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 195°C/W

## ORDER INFORMATION

**Lead Free Finish**

| TAPE AND REEL (MINI) | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2904CDDB#TRMPBF | LTC2904CDDB#TRPBF | LBCZ | 8-Lead (3mm × 2mm) Plastic DFN | 0°C to 70°C |
| LTC2904IDDB#TRMPBF | LTC2904IDDB#TRPBF | LBDB | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 85°C |
| LTC2905CDDB#TRMPBF | LTC2905CDDB#TRPBF | LAJF | 8-Lead (3mm × 2mm) Plastic DFN | 0°C to 70°C |
| LTC2905HDDB#TRMPBF | LTC2905HDDB#TRPBF | LBCY | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 125°C |
| LTC2905IDDB#TRMPBF | LTC2905IDDB#TRPBF | LBCY | 8-Lead (3mm × 2mm) Plastic DFN | –40°C to 85°C |
| LTC2904CTS8#TRMPBF | LTC2904CTS8#TRPBF | LTBCJ | 8-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC2904ITS8#TRMPBF | LTC2904ITS8#TRPBF | LTBCK | 8-Lead Plastic TSOT-23 | –40°C to 85°C |
| LTC2905CTS8#TRMPBF | LTC2905CTS8#TRPBF | LTAJD | 8-Lead Plastic TSOT-23 | 0°C to 70°C |
| LTC2905HTS8#TRMPBF | LTC2905HTS8#TRPBF | LTAJE | 8-Lead Plastic TSOT-23 | –40°C to 125°C |
| LTC2905ITS8#TRMPBF | LTC2905ITS8#TRPBF | LTAJE | 8-Lead Plastic TSOT-23 | –40°C to 85°C |

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. V1 = 2.5V, V2 = 1V, S1 = TOL = V1, S2 = 0V, unless otherwise noted. (Notes 2, 3)**

| SYMBOL | PARAMETER | | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $V_{RT50}$ | 5V, 5% Reset Threshold | | V1 Input Threshold | ● | 4.600 | 4.675 | 4.750 | V |
| | 5V, 7.5% Reset Threshold | | | ● | 4.475 | 4.550 | 4.625 | V |
| | 5V, 10% Reset Threshold | | | ● | 4.350 | 4.425 | 4.500 | V |
| $V_{RT33}$ | 3.3V, 5% Reset Threshold | | V1, V2 Input Threshold | ● | 3.036 | 3.086 | 3.135 | V |
| | 3.3V, 7.5% Reset Threshold | | | ● | 2.954 | 3.003 | 3.053 | V |
| | 3.3V, 10% Reset Threshold | | | ● | 2.871 | 2.921 | 2.970 | V |
| $V_{RT25}$ | 2.5V, 5% Reset Threshold | | V1, V2 Input Threshold | ● | 2.300 | 2.338 | 2.375 | V |
| | 2.5V, 7.5% Reset Threshold | | | ● | 2.238 | 2.275 | 2.313 | V |
| | 2.5V, 10% Reset Threshold | | | ● | 2.175 | 2.213 | 2.250 | V |
| $V_{RT18}$ | 1.8V, 5% Reset Threshold | | V2 Input Threshold | ● | 1.656 | 1.683 | 1.710 | V |
| | 1.8V, 7.5% Reset Threshold | | | ● | 1.611 | 1.638 | 1.665 | V |
| | 1.8V, 10% Reset Threshold | | | ● | 1.566 | 1.593 | 1.620 | V |
| $V_{RT15}$ | 1.5V, 5% Reset Threshold | | V2 Input Threshold | ● | 1.380 | 1.403 | 1.425 | V |
| | 1.5V, 7.5% Reset Threshold | | | ● | 1.343 | 1.365 | 1.388 | V |
| | 1.5V, 10% Reset Threshold | | | ● | 1.305 | 1.328 | 1.350 | V |
| $V_{RT12}$ | 1.2V, 5% Reset Threshold | | V2 Input Threshold | ● | 1.104 | 1.122 | 1.140 | V |
| | 1.2V, 7.5% Reset Threshold | | | ● | 1.074 | 1.092 | 1.110 | V |
| | 1.2V, 10% Reset Threshold | | | ● | 1.044 | 1.062 | 1.080 | V |
| $V_{RT10}$ | 1V, 5% Reset Threshold | | V2 Input Threshold | ● | 0.920 | 0.935 | 0.950 | V |
| | 1V, 7.5% Reset Threshold | | | ● | 0.895 | 0.910 | 0.925 | V |
| | 1V, 10% Reset Threshold | | | ● | 0.870 | 0.885 | 0.900 | V |
| $V_{CCMIN}$ | Minimum Internal Operating Voltage (Note 2) | | $\overline{RST}$ in Correct Logic State | ● | | | 1 | V |
| $I_{V1}$ | V1 Input Current | | Includes Input Current to Three-State Pins | ● | | 65 | 130 | µA |
| $I_{V2}$ | V2 Input Current | | | ● | | 0.4 | 1.0 | µA |
| $I_{TMR(UP)}$ | TMR Pull-Up Current | LTC2905 | $V_{TMR}$ = 0V | ● | –1.5 | –2.1 | –2.7 | µA |
| $I_{TMR(DOWN)}$ | TMR Pull-Down Current | LTC2905 | $V_{TMR}$ = 1.4V | ● | 1.5 | 2.1 | 2.7 | µA |
| | | LTC2905H | | ● | 1.4 | 2.0 | 2.7 | µA |
| $t_{RST}$ | Reset Timeout Period | LTC2904 | | ● | 140 | 200 | 260 | ms |
| $t_{RST}$ | Reset Timeout Period | LTC2905 | $C_{TMR}$ = 22nF | ● | 140 | 200 | 260 | ms |
| | | LTC2905H | | ● | 140 | | 295 | ms |
| $t_{UV}$ | Vx Undervoltage Detect to RST or $\overline{RST}$ | | Vx Less than Reset Threshold $V_{RTX}$ by More than 1% | | | 150 | | µs |
| $V_{OL}$ | Output Voltage Low RST, $\overline{RST}$ | | I = 2.5mA | ● | | 0.15 | 0.4 | V |
| | | | I = 100µA; V1 = 1V ($\overline{RST}$ Only) | ● | | 0.05 | 0.3 | V |
| $V_{OH}$ | Output Voltage High RST, $\overline{RST}$ (Notes 2, 5) | | I = –1µA | ● | $V_{CC}$–1 | | | V |
| **Three-State Inputs S1, S2, TOL** | | | | | | | | |
| $V_{IL}$ | Low Level Input Voltage | | | ● | | | 0.4 | V |
| $V_{IH}$ | High Level Input Voltage | | | ● | 1.4 | | | V |
| $V_Z$ | Pin Voltage When Left in Open State | | I = –10µA | ● | 0.7 | | | V |
| | | | I = 0µA | | | 0.9 | | V |
| | | | I = 10µA | ● | | | 1.1 | V |
| | 2905H | | I = –10µA | ● | 0.65 | | | V |
| | | | I = 0µA | | | 0.9 | | V |
| | | | I = 10µA | ● | | | 1.15 | V |
| $I_{VPG}$ | Programming Input Current (Note 6) | | | ● | | | ±25 | µA |

## ELECTRICAL CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The greater of V1, V2 is the internal supply voltage ($V_{CC}$).

**Note 3:** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

**Note 4:** For reset thresholds test conditions refer to the voltage threshold programming table in the Applications Information section.

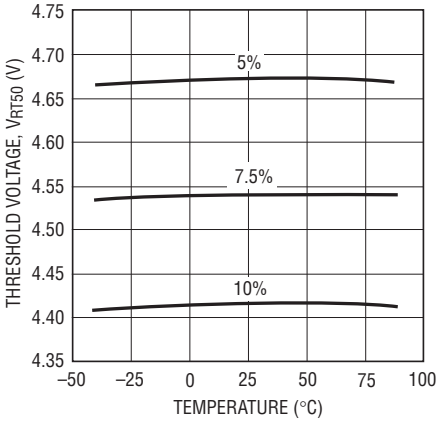
**Note 5:** The output pins $\overline{RST}$ and RST have an internal pull-up to $V_{CC}$ of typically –6µA. However, an external pull-up resistor may be used when faster rise time is required or for $V_{OH}$ voltages greater than $V_{CC}$.

**Note 6:** The input current to the three-state input pins are the pull-up and the pull-down current when the pins are either set to V1 or GND respectively. In the open state, the maximum leakage current to V1 or GND permissible is 10µA.

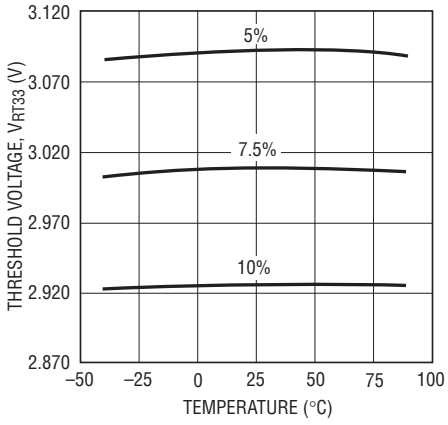
## TYPICAL PERFORMANCE CHARACTERISTICS

**Specifications are at $T_A$ = 25°C unless otherwise noted.**

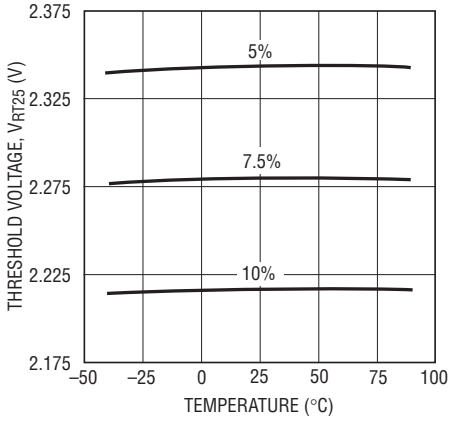
**5V Threshold Voltage vs Temperature**



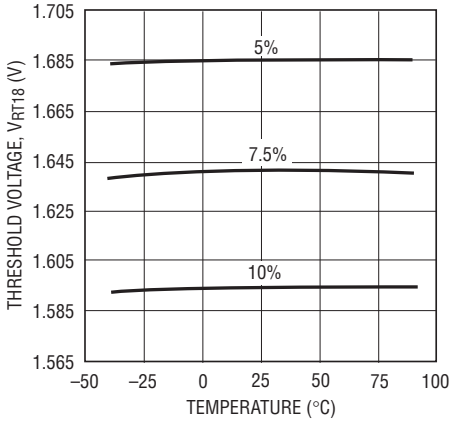

**3.3V Threshold Voltage vs Temperature**



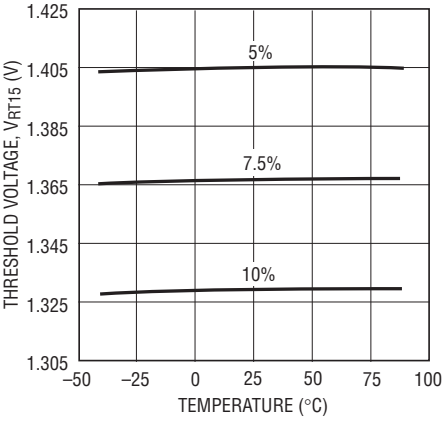

**2.5V Threshold Voltage vs Temperature**



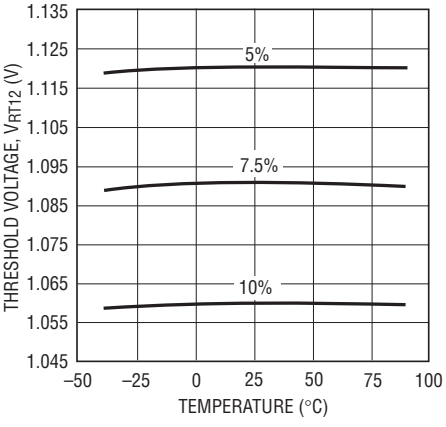

**1.8V Threshold Voltage vs Temperature**




**1.5V Threshold Voltage vs Temperature**



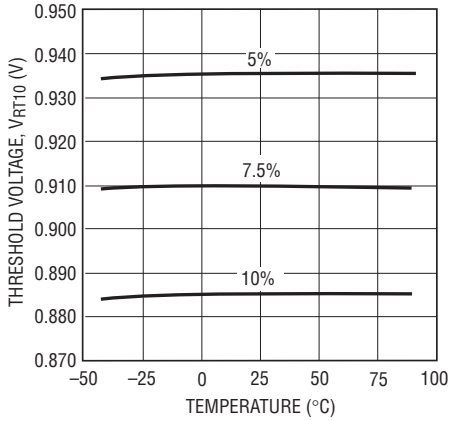

**1.2V Threshold Voltage vs Temperature**



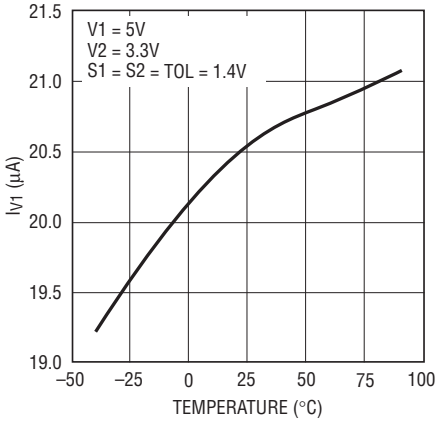
# TYPICAL PERFORMANCE CHARACTERISTICS

**Specifications are at $T_A$ = 25°C unless otherwise noted.**

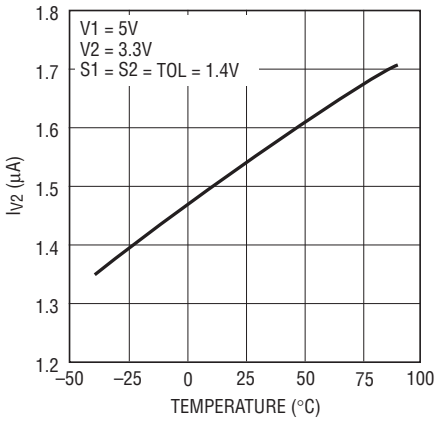
### 1V Threshold Voltage vs Temperature



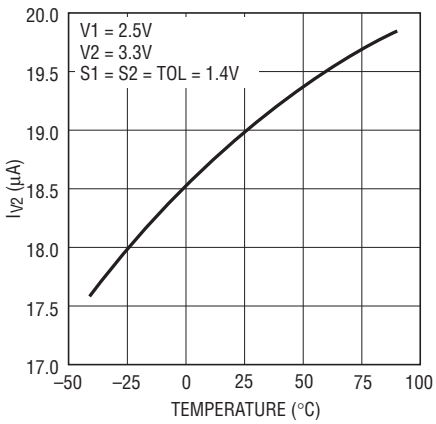

### $I_{V1}$ vs Temperature



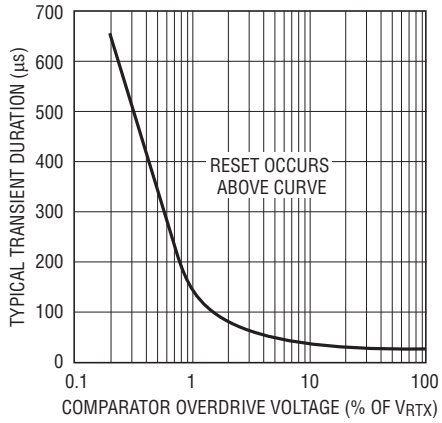

### $I_{V2}$ vs Temperature



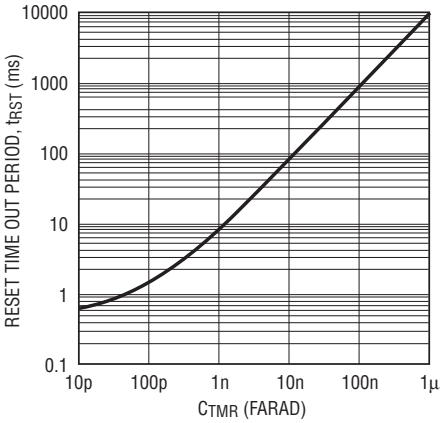

### $I_{V2}$ vs Temperature



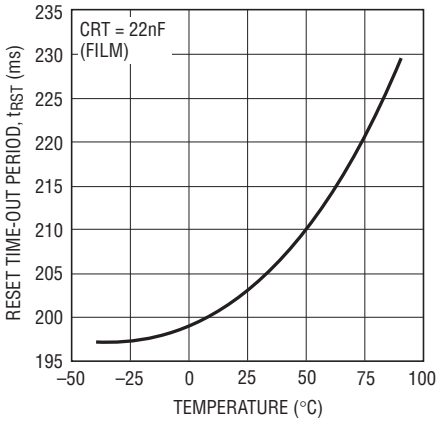

### Typical Transient Duration vs Comparator Overdrive (V1, V2)



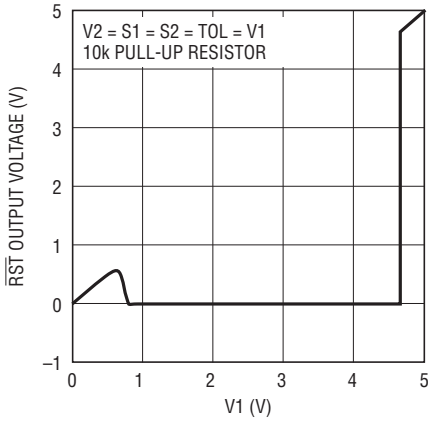

### Reset Time Out Period ($t_{RST}$) vs Capacitance ($C_{TMR}$)



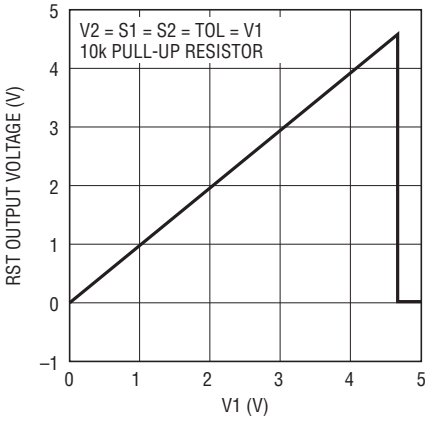

### Reset Timeout Period ($t_{RST}$) vs Temperature




### $\overline{RST}$ Output Voltage vs V1



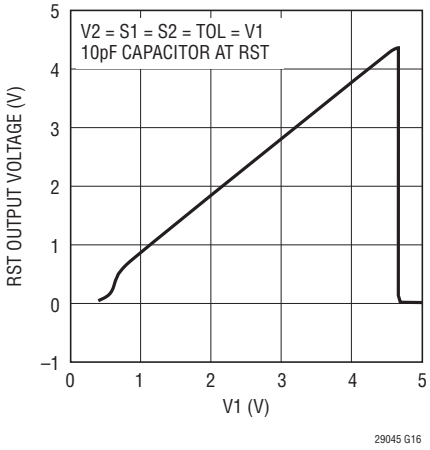

### RST Output Voltage vs V1



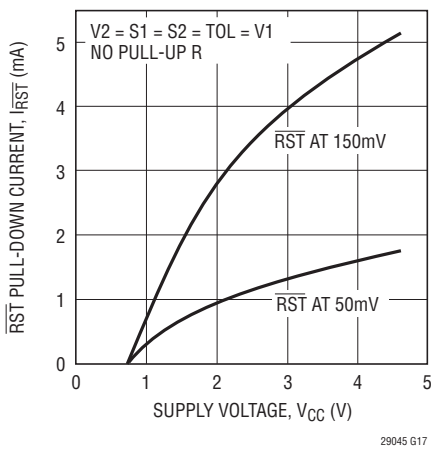
## TYPICAL PERFORMANCE CHARACTERISTICS

**Specifications are at $T_A$ = 25°C unless otherwise noted.**

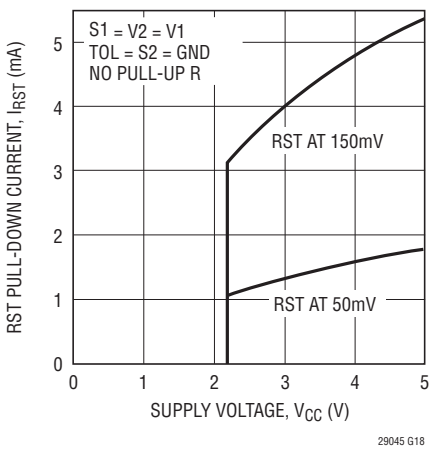
### RST Output Voltage vs V1



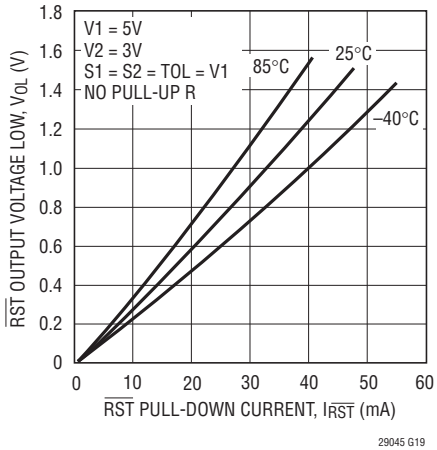

### $\overline{RST}$ Pull-Down Current ($I_{RST}$) vs Supply Voltage ($V_{CC}$)



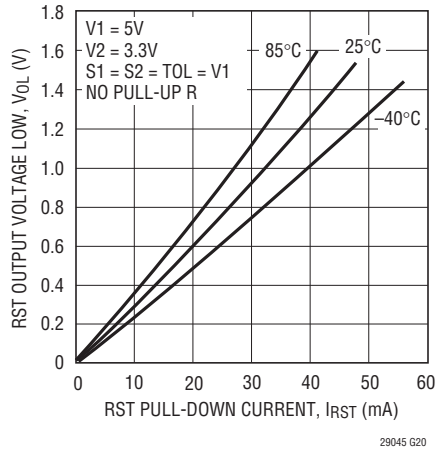

### RST Pull-Down Current ($I_{RST}$) vs Supply Voltage ($V_{CC}$)



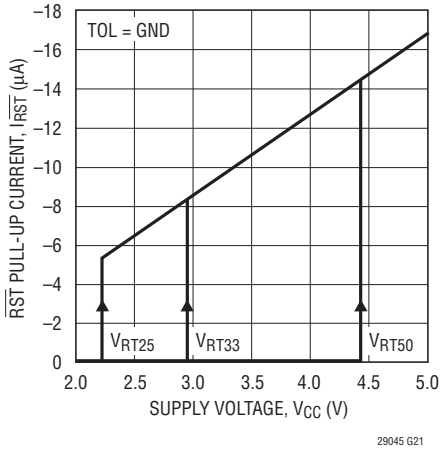

### $\overline{RST}$ Output Voltage Low ($V_{OL}$) vs $\overline{RST}$ Pull-Down Current ($I_{RST}$)



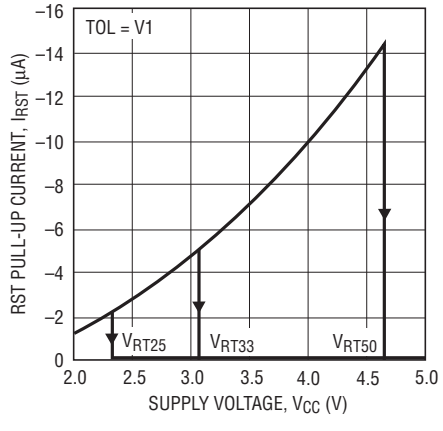

### RST Output Voltage Low ($V_{OL}$) vs RST Pull-Down Current ($I_{RST}$)



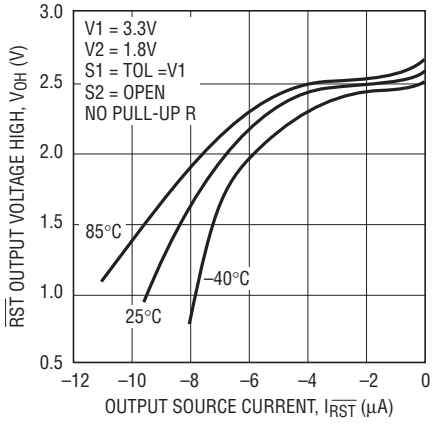

### $\overline{RST}$ Pull-Up Current ($I_{RST}$) vs Supply Voltage ($V_{CC}$)



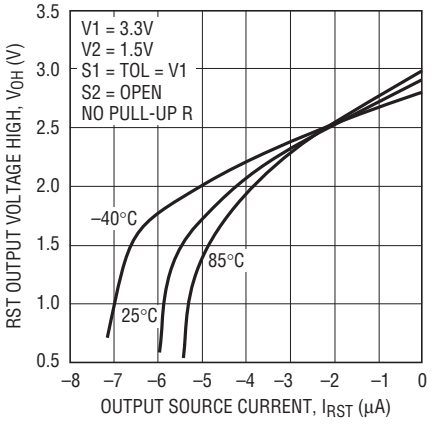

### RST Pull-Up Current ($I_{RST}$) vs Supply Voltage ($V_{CC}$)




### $\overline{RST}$ Output Voltage High ($V_{OH}$) vs $\overline{RST}$ Output Source Current ($I_{RST}$)



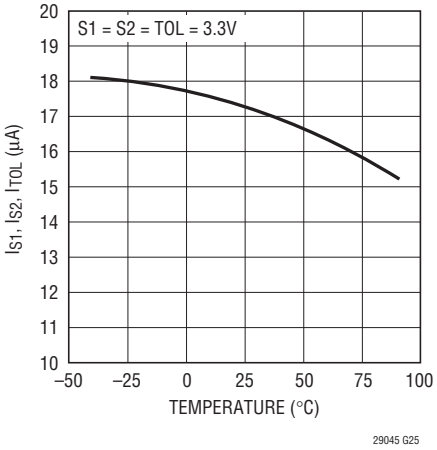

### RST Output Voltage High ($V_{OH}$) vs RST Output Source Current ($I_{RST}$)



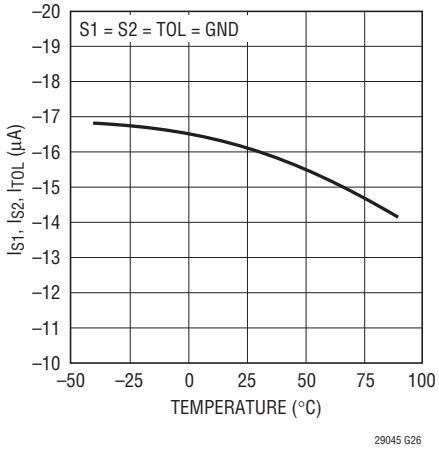
## TYPICAL PERFORMANCE CHARACTERISTICS

**Specifications are at $T_A$ = 25°C unless otherwise noted.**

**$I_{S1}$, $I_{S2}$, $I_{TOL}$ vs Temperature**




**$I_{S1}$, $I_{S2}$, $I_{TOL}$ vs Temperature**




## PIN FUNCTIONS (TS8/DDB8)

**V2 (Pin 1/Pin 4):** Voltage Input 2. Input for V2 monitor. Select from 3.3V, 2.5V, 1.8V, 1.5V, 1.2V or 1.0V. Refer to Table 1 for details. The greater of V1, V2 is also the internal supply voltage, $V_{CC}$. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

**RST (Pin 2/Pin 3):** (LTC2904 Only) Reset Logic Output. When all voltage inputs are above the reset threshold for at least the programmed delay time, this pin pulls low. This pin has a weak pull-up to $V_{CC}$ and may be pulled above $V_{CC}$ using an external pull-up.

**TMR (Pin 2/Pin 3):** (LTC2905 Only) Reset Delay Time Programming Pin. Attach an external capacitor ($C_{TMR}$) to GND to set a reset delay time of 9ms/nF. Leaving the pin open generates a minimum delay of approximately 200µs. A 22nF capacitor will generate a 200ms reset delay time.

**$\overline{RST}$ (Pin 3/Pin 2):** Inverted Reset Logic Output. Pulls low when any voltage input is below the reset threshold and is held low for programmed delay time after all voltage inputs are above threshold. This pin has a weak pull-up to $V_{CC}$ and may be pulled above $V_{CC}$ using an external pull-up.

**GND (Pin 4/Pin 1, Pin 9):** Ground.

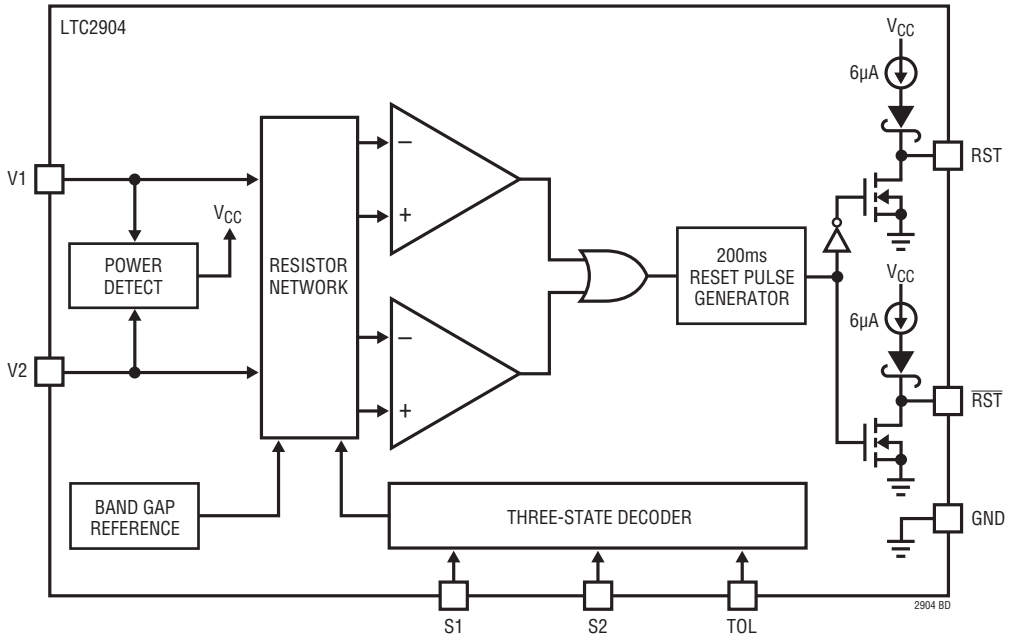
**TOL (Pin 5/Pin 8):** Three-state Input for Supply Tolerance Selection (5%, 7.5% or 10%). See the Applications Information section for tolerance selection chart (Table 2).

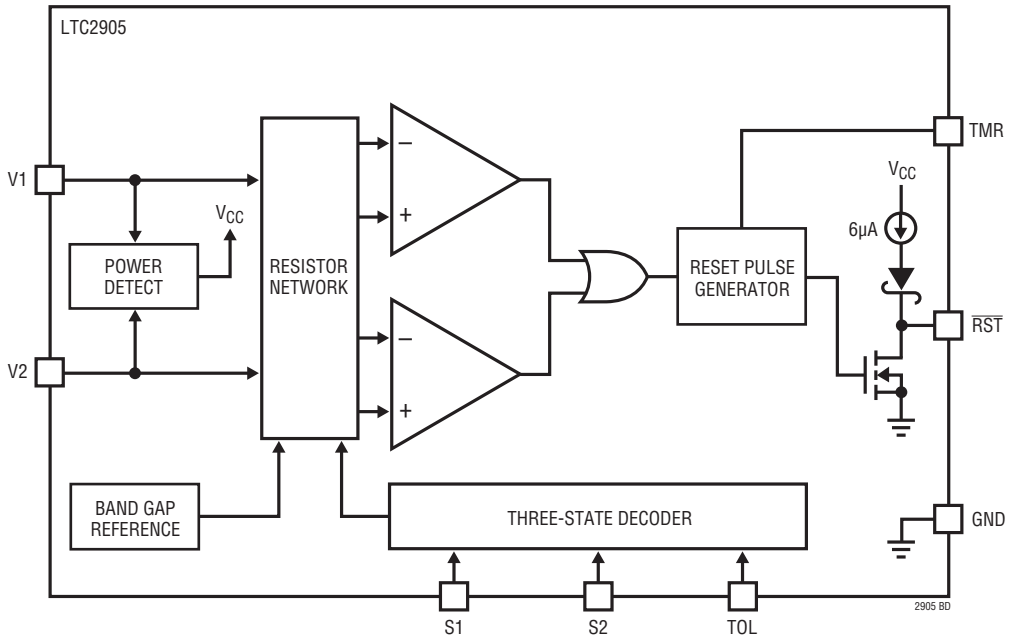
**S1 (Pin 6/Pin 7):** Voltage Threshold Select Three-State Input. Connect to V1, GND or leave unconnected in open state (See Table 1).

**S2 (Pin 7/Pin 6):** The Second Voltage Threshold Select Three-State Input. Connect to V1, GND or leave unconnected in open state (See Table 1).

**V1 (Pin 8/Pin 5):** Voltage Input 1. Input for V1 monitor. Select from 5V, 3.3V, or 2.5V. See Table 1 for details. The greater of V1, V2 is also the internal supply voltage, $V_{CC}$. Bypass this pin to ground with a 0.1µF (or greater) capacitor.

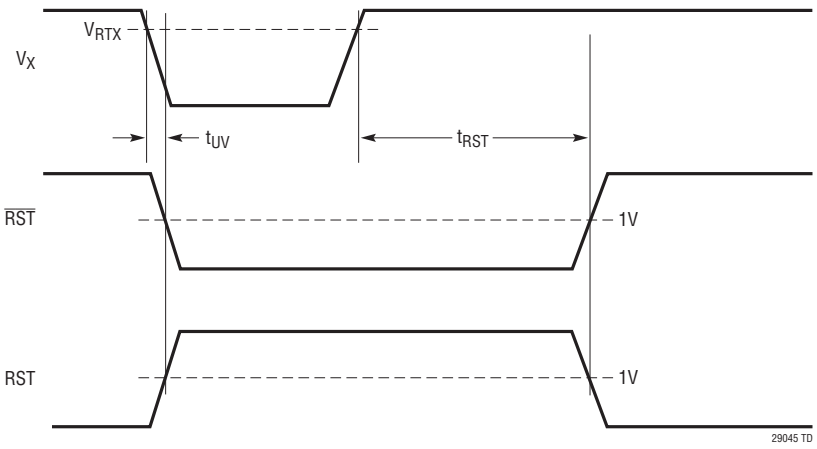
## BLOCK DIAGRAM



## TIMING DIAGRAM

**$V_X$ Monitor Timing**




## APPLICATIONS INFORMATION

### Supply Monitoring

The LTC2904/LTC2905 are low power, high accuracy dual supply monitors with a common reset output and selectable thresholds. Reset delay is set to a nominal of 200ms for the LTC2904 and is adjustable using an external capacitor for the LTC2905.

The two 3-state input pins (S1 and S2) select one of nine possible threshold voltage combinations. Another three-state input pin sets the supply tolerance (5%, 7.5% or 10%). Both input voltages (V1 and V2) must be above predetermined thresholds for the reset not to be invoked. The LTC2904/LTC2905 assert the reset outputs during power-up, power-down and brownout conditions on either of the voltage inputs.

### Power-Up

The greater of V1, V2 is the internal supply voltage ($V_{CC}$). $V_{CC}$ powers the drive circuits for the $\overline{RST}$ pin. Therefore as soon as V1 or V2 reaches 1V during power-up, the $\overline{RST}$ output asserts low.

$V_{CC}$ also powers the drive circuits for the RST pin in the LTC2904. Therefore, RST weakly pulls high when V1 or V2 reaches at least 1V.

Threshold programming is complete when V1 reaches at least 2.17V. After programming, if either V1 or V2 falls below its programmed threshold, $\overline{RST}$ asserts low (RST weakly pulls high) as long as $V_{CC}$ is at least 1V.

Once V1 and V2 rise above their thresholds, an internal timer is started. After the programmed delay time, $\overline{RST}$ weakly pulls high (RST asserts low).

## APPLICATIONS INFORMATION

### Power-Down

On power-down, once either V1 or V2 inputs drops below its threshold, $\overline{RST}$ asserts logic low and RST weakly pulls high. $V_{CC}$ of at least 1V guarantees a logic low of 0.4V at $\overline{RST}$.

### Programming Pins

The three 3-state input pins: S1, S2 and TOL should be connected to GND, V1 or left unconnected during normal operation. Note that when left unconnected, the maximum leakage current allowable from the pin to either GND or V1 is 10µA.

In margining applications, all the 3-state input pins can be driven using a tri-state buffer. Note however the low and high output of the tri-state buffer has to satisfy the $V_{IL}$ and $V_{IH}$ of the 3-state pin listed in the Electrical Characteristics Table. Moreover, when the tri-state buffer is in the high impedance state, the maximum leakage current allowed from the pin to either GND or V1 is 10µA.

### Monitor Programming

Connecting S1 and S2 to GND, V1 or leaving them open selects the LTC2904/LTC2905 input voltage combinations. Table 1 shows the nine possible combinations of nominal input voltages and their corresponding S1, S2 connections.

**Table 1. Voltage Threshold Programming**

| V1 | V2 | S1 | S2 |
|---|---|---|---|
| 5.0 | 3.3 | V1 | V1 |
| 3.3 | 2.5 | Open | GND |
| 3.3 | 1.8 | V1 | Open |
| 3.3 | 1.5 | Open | V1 |
| 3.3 | 1.2 | Open | Open |
| 2.5 | 1.8 | GND | GND |
| 2.5 | 1.5 | GND | Open |
| 2.5 | 1.2 | GND | V1 |
| 2.5 | 1.0 | V1 | GND |

Note: Open = open circuit or driven by a three state buffer in high impedance state with leakage current less than 10µA.

### Tolerance Programming

The three-state input pin, TOL programs the common supply tolerance for both V1 and V2 input voltages (5%, 7.5% or 10%). The larger the tolerance the lower the trip threshold. Table 2 shows the tolerances selection corresponding to a particular connection at the TOL pin.

**Table 2. Tolerance Programming**

| Tolerance | TOL |
|---|---|
| 5% | V1 |
| 7.5% | Open |
| 10% | GND |

### Threshold Accuracy

Reset threshold accuracy is of the utmost importance in a supply sensitive system. Ideally such a system should not reset while supply voltages are within a specified margin below the rated nominal level. Both of the LTC2904/LTC2905 inputs have the same relative threshold accuracy. The specification for LTC2904/LTC2905 is ±1.5% of the programmed nominal input voltage (over the full operating temperature range).

For example, when the LTC2904/LTC2905 are programmed to handle a 5V input with 10% tolerance (S1 = S2 = V1 and TOL = GND, refer to Table 1 and Table 2), it does not issue a reset command when V1 is above 4.5V. The typical 10% trip threshold is at 11.5% below the nominal input voltage level. Therefore, the typical trip threshold for the 5V input is 4.425V. With ±1.5% accuracy, the trip threshold range is 4.425V ±75mV over temperature (i.e. 10% to 13% below 5V). This implies that the monitored system must operate reliably down to 4.35V over temperature.

The same system using a supervisor with only ±2.5% accuracy needs to work reliably down to 4.25V (4.375V ±125mV) or 15% below 5V, requiring the monitored system to work over a much wider operating voltage range.

## APPLICATIONS INFORMATION

In any supervisory application, supply noise riding on the monitored DC voltage can cause spurious resets, particularly when the monitored voltage is near the reset threshold. A less desirable but common solution to this problem is to introduce hysteresis around the nominal threshold. Notice however, this hysteresis introduces an error term in the threshold accuracy. Therefore, a ±2.5% accurate monitor with ±1.0% hysteresis is equivalent to a ±3.5% monitor with no hysteresis.

The LTC2904/LTC2905 takes a different approach to solve this problem of supply noise causing spurious reset. The first line of defense against this spurious reset is a first order low pass filter at the output of the comparator. Thus, the comparator output goes through a form of integration before triggering the output logic. Therefore, any kind of transient at the input of the comparator needs to be of sufficient magnitude and duration before it can trigger a change in the output logic.

The second line of defense is the programmed delay time tRST (200ms for LTC2904 and using an external capacitor for LTC2905). This delay will eliminate the effect of any supply noise whose frequency is above $1/t_{RST}$ on the $\overline{RST}$ and RST output.

When either V1 or V2 drops below its programmed threshold, the $\overline{RST}$ pin asserts low (RST weakly pulls high). Then when the supply recovers above the programmed threshold, the reset-pulse-generator timer starts counting.

If the supply remains above the programmed threshold when the timer finishes counting, the $\overline{RST}$ pin weakly pulls high (RST asserts low). However, if the supply falls below the programmed threshold any time during the period when the timer is still counting, the timer resets and it starts fresh when the supply next rises above the programmed threshold.

Note that this second line of defense is only effective for a rising supply and does not affect the sensitivity of the system to a falling supply. Therefore, the first line of defense that works for both cases of rising and falling is necessary. These two approaches prevent spurious reset caused by supply noise without sacrificing the threshold accuracy.

### Selecting the Reset Timing Capacitor

The reset timeout period for LTC2905 is adjustable in order to accommodate a variety of microprocessor applications. Connecting a capacitor, $C_{TMR}$, between the TMR pin and ground sets the reset timeout period, $t_{RST}$. The following formula determines the value of capacitor needed for a particular reset timeout period:

$$C_{TMR} = t_{RST} \bullet 110 \bullet 10^{-9}\ [F/s]$$

For example, using a standard capacitor value of 22nF would give a 22000/110 = 200ms delay.

Figure 1 shows the desired delay time as a function of the value of the timer capacitor that should be used:

Leaving the TMR pin open with no external capacitor generates a reset timeout of approximately 200µs. For long reset timeout, the only limitation is the availability of large value capacitor with low leakage. The TMR capacitor will never charge if the leakage current exceeds the minimum TMR charging current of 2.1µA (typical).

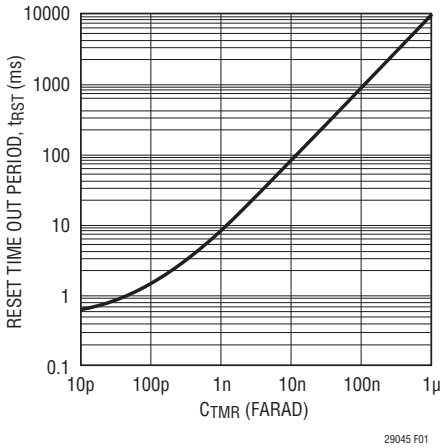



**Figure 1. Reset Timeout Period vs Capacitance**

## APPLICATIONS INFORMATION

### RST and $\overline{RST}$ Output Characteristics

The DC characteristics of the RST and $\overline{RST}$ pull-up and pull-down strength are shown in the Typical Performance Characteristics section. Both RST and $\overline{RST}$ have a weak internal pull-up to $V_{CC}$ = Max (V1, V2) and a strong pull-down to ground.

The weak pull-up and strong pull-down arrangement allow these two pins to have open-drain behavior while possessing several other beneficial characteristics.

The weak pull-ups eliminate the need for external pull-up resistors when the rise time on these pins is not critical. On the other hand, the open-drain $\overline{RST}$ configuration allows for wired-OR connections and can be useful when more than one signal needs to pull down on the $\overline{RST}$ line.

As noted in the Power-Up and Power-Down sections the circuits that drive RST and $\overline{RST}$ are powered by $V_{CC}$. During fault condition, $V_{CC}$ of at least 1V guarantees a maximum $V_{OL}$ = 0.4V at $\overline{RST}$. However, at $V_{CC}$ = 1V the weak pull-up current on RST is barely turned on. Therefore, an external pull-up resistor of no more than 100k is recommended on the RST pin if the state and pull-up strength of the RST pin is crucial at very low $V_{CC}$.

Note however, by adding an external pull-up resistor, the pull-up strength on the RST pin is increased. Therefore, if it is connected in a wired-OR connection, the pull-down strength of any single device needs to accommodate this additional pull-up strength.

### Output Rise and Fall Time Estimation

The RST and $\overline{RST}$ outputs have strong pull-down capability. The following formula estimates the output fall time (90% to 10%) for a particular external load capacitance ($C_{LOAD}$):

$$t_{FALL} \approx 2.2 \bullet R_{PD} \bullet C_{LOAD}$$

where $R_{PD}$ is the on-resistance of the internal pull-down transistor estimated to be typically 40Ω at room temperature (25°C) and $C_{LOAD}$ is the external load capacitance on the pin. Assuming a 150pF load capacitance, the fall time is about 13ns.

The rise time, on the RST and $\overline{RST}$ pins is limited by weak internal pull-up current sources to $V_{CC}$. The following formula estimates the output rise time (10% to 90%) at the RST and $\overline{RST}$ pins:

$$t_{RISE} \approx 2.2\ \ R_{PU} \bullet C_{LOAD}$$

where $R_{PU}$ is the on-resistance of the pull-up transistor. Notice that this pull-up transistor is modeled as a 6µA current source in the Block Diagram as a typical representation.

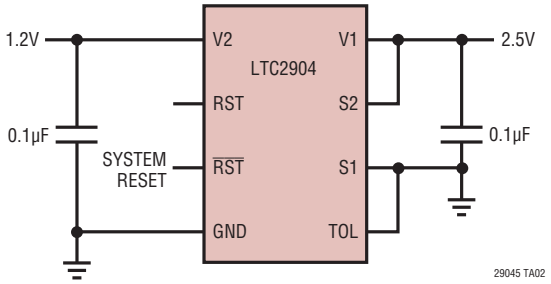
The on-resistance as a function of the $V_{CC}$ = Max (V1, V2) voltage (for $V_{CC}$ > 1V) at room temperature is estimated as follows:

$$R_{PU} = \frac{6 \bullet 10^5}{MAX(V1,V2) - 1V}\ \Omega$$

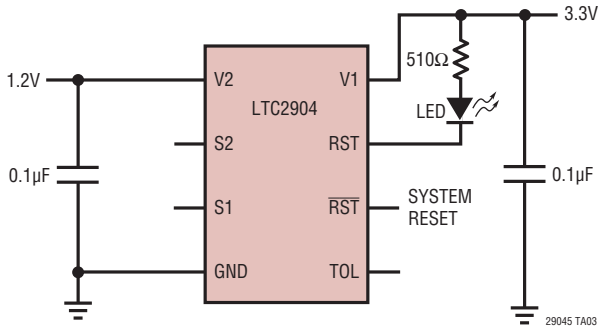
At $V_{CC}$ = 3.3V, $R_{PU}$ is about 260k. Using 150pF for load capacitance, the rise time is 86µs. An external pull-up resistor may be used if the output needs to pull up faster and/or to a higher voltage, for example: the rise time reduces to 3.3µs for a 150pF load capacitance, when using a 10k pull-up resistor.

## TYPICAL APPLICATIONS

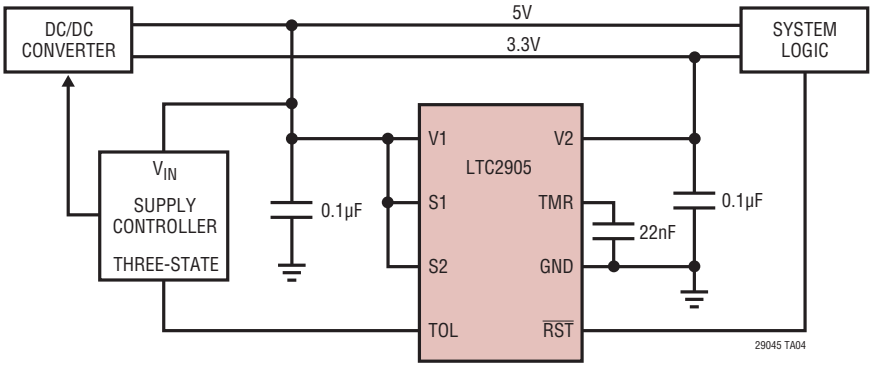
**2.5V, 1.2V Supply Monitor, 10% Tolerance**



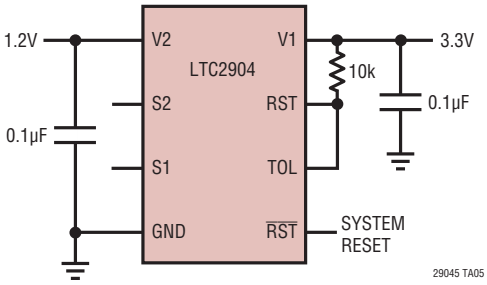

**3.3V, 1.2V Dual Supply Monitor with LED Power Good Indicator, 7.5% Tolerance and Adjustable Timer**




**5V, 3.3V Dual Supply Monitor with Voltage Margining for Automated On-Board Testing**

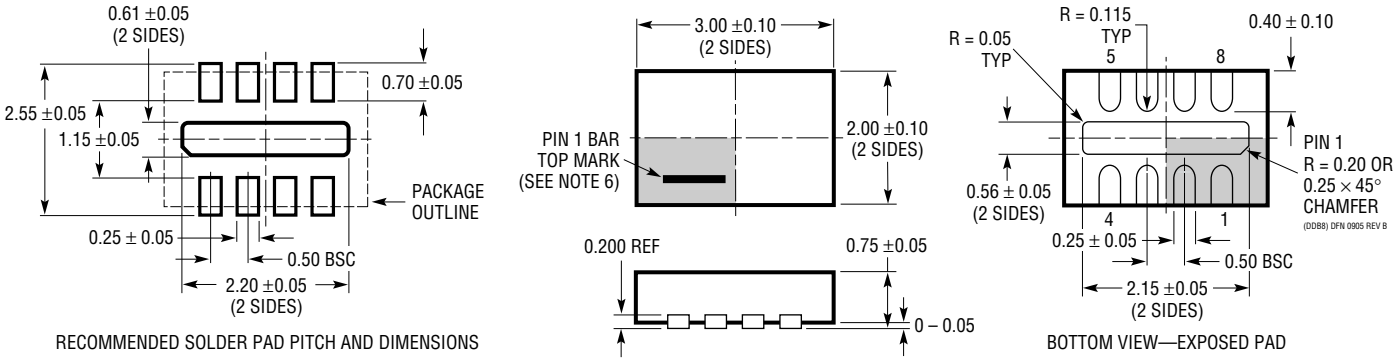



**3.3V, 1.2V Dual Supply Monitor with Asymmetric Hysteresis, 5% Tolerance (Supplies Rising), 10% Tolerance (After RST Goes Low)**



# PACKAGE DESCRIPTION

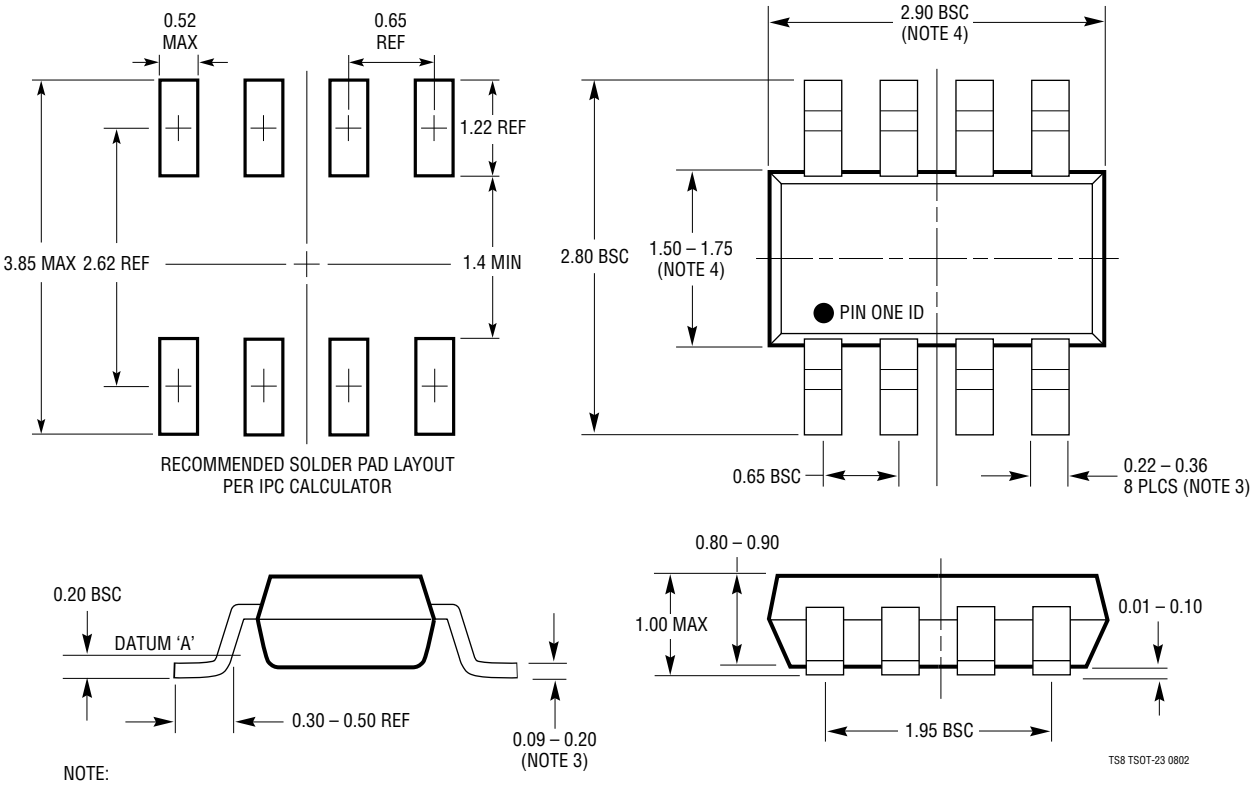
**DDB Package**
**8-Lead Plastic DFN (3mm × 2mm)**
(Reference LTC DWG # 05-08-1702 Rev B)




NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

**TS8 Package**
**8-Lead Plastic TSOT-23**
(Reference LTC DWG # 05-08-1637)




NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193



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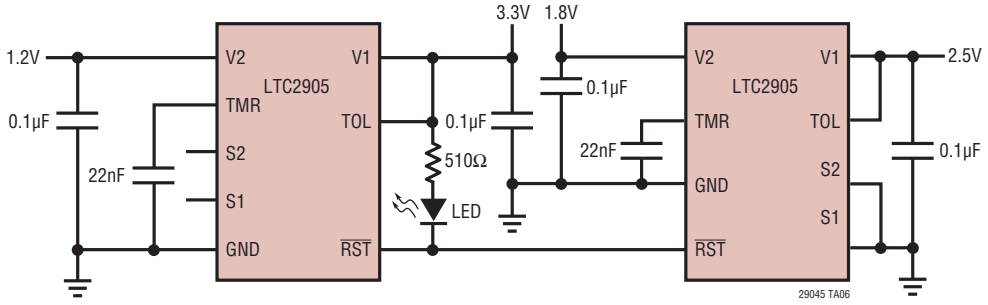
## TYPICAL APPLICATION

**3.3V, 1.2V Dual Supply Monitor with LED Power Good Indicator, 7.5% Tolerance and Adjustable Timer**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC690 | 5V Supply Monitor, Watchdog Timer and Battery Backup | 4.65V Threshold |
| LTC694-3.3 | 3.3V Supply Monitor, Watchdog Timer and Battery Backup | 2.9V Threshold |
| LTC699 | 5V Supply Monitor and Watchdog Timer | 4.65V Threshold |
| LTC1232 | 5V Supply Monitor, Watchdog Timer and Pushbutton Reset | 4.37V/4.62V Threshold |
| LTC1326/LTC1326-2.5 | Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ | 4.725V, 3.118V, 1V Threshold (±0.75%) |
| LTC1536 | Precision Triple Supply Monitor for PCI Applications | Meets PCI $t_{FAIL}$ Timing Specifications |
| LTC1726-2.5/LTC1726-5 | Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ | Adjustable $\overline{\text{RESET}}$ and Watchdog Timeouts |
| LTC1727-2.5/LTC1727-5 | Micropower Triple Supply Monitor with Open-Drain Reset | Individual Monitor Outputs in MSOP |
| LTC1728-1.8/LTC1728-3.3 | Micropower Triple Supply Monitor with Open-Drain Reset | 5-Lead SOT-23 Package |
| LTC1728-2.5/LTC1728-5 | Micropower Triple Supply Monitor with Open-Drain Reset | 5-Lead SOT-23 Package |
| LTC1985-1.8 | Micropower Triple Supply Monitor with Push-Pull Reset Output | 5-Lead SOT-23 Package |
| LTC2900 | Programmable Quad Supply Monitor | Adjustable $\overline{\text{RESET}}$, 10-Lead MSOP, DFN Packages |
| LTC2901 | Programmable Quad Supply Monitor | Adjustable $\overline{\text{RESET}}$ and Watchdog Timer, 16-Lead SSOP Package |
| LTC2902 | Programmable Quad Supply Monitor | Selectable Tolerance, $\overline{\text{RESET}}$ Disable for Margining Functions, 16-Lead SSOP Package |
| LTC2903-1 | Precision Quad Supply Monitor | Ultralow Voltage $\overline{\text{RESET}}$, 6-Lead SOT-23 Package |
| LTC2906 | Dual Supply Monitor with One Pin-Selectable Threshold and One Adjustable Input | 0.5V Adjustable Threshold and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages |
| LTC2907 | Dual Supply Monitor with One Pin-Selectable Threshold and One Adjustable Input | 0.5V Adjustable Threshold, Adjustable $\overline{\text{RESET}}$ Timer and Three Supply Tolerances, 8-Lead SOT-23 and DFN Packages |
| LTC2908 | Precision Six Supply Monitors | Ultralow Voltage $\overline{\text{RESET}}$, 8-Lead SOT-23 and DFN Packages |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