

## Quad, 12-Bit + Sign, 5Msps/Ch Simultaneous Sampling ADC

### FEATURES

- 5Msps/Ch Throughput Rate
- Four Simultaneously Sampling Channels
- Guaranteed 12-Bit, No Missing Codes
- 8V<sub>P-P</sub> Differential Inputs with Wide Input Common Mode Range
- 77dB SNR (Typ) at  $f_{IN} = 2.2\text{MHz}$
- -86dB THD (Typ) at  $f_{IN} = 2.2\text{MHz}$
- Guaranteed Operation to 125°C
- Single 3.3V or 5V Supply
- Low Drift (20ppm/°C Max) 2.048V or 4.096V Internal Reference
- 1.8V to 2.5V I/O Voltages
- CMOS or LVDS SPI-Compatible Serial I/O
- Power Dissipation 45mW/Ch (Typ)
- Small 52-Lead (7mm × 8mm) QFN Package

### APPLICATIONS

- High Speed Data Acquisition Systems
- Communications
- Optical Networking
- Multiphase Motor Control

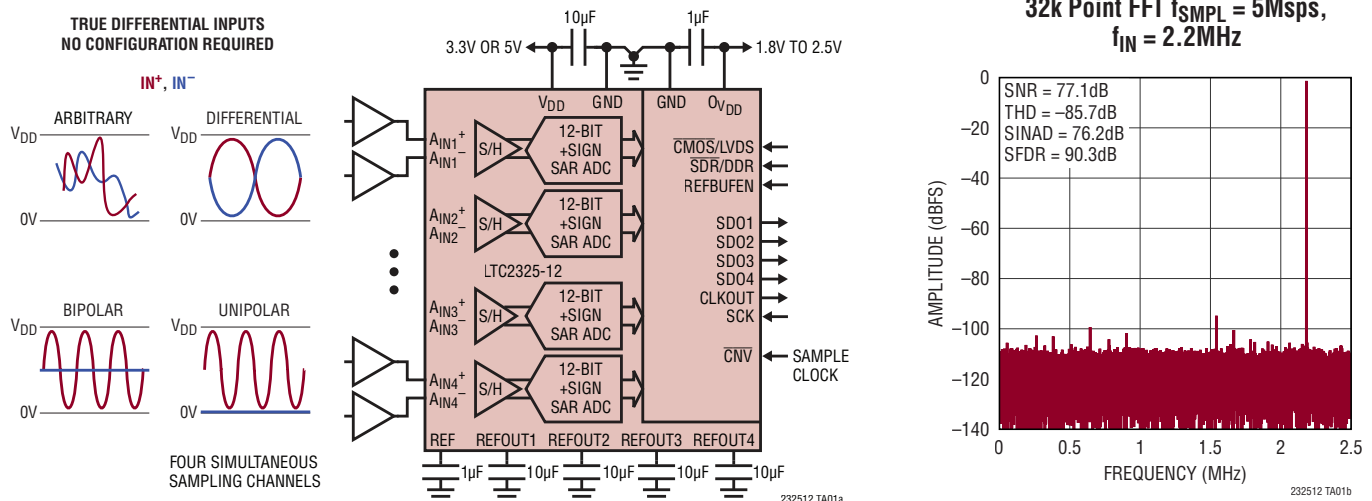
### DESCRIPTION

The **LTC®2325-12** is a low noise, high speed quad 12-bit + sign successive approximation register (SAR) ADC with differential inputs and wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2325-12 has an 8V<sub>P-P</sub> differential input range, making it ideal for applications which require a wide dynamic range with high common mode rejection. The LTC2325-12 achieves ±0.5LSB INL typical, no missing codes at 12 bits and 77dB SNR.

The LTC2325-12 has an onboard low drift (20ppm/°C max) 2.048V or 4.096V temperature-compensated reference. The LTC2325-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 5Msps per channel throughput with one cycle latency makes the LTC2325-12 ideally suited for a wide variety of high speed applications. The LTC2325-12 dissipates only 45mW per channel and offers nap and sleep modes to reduce the power consumption to 26μW for further power savings during inactive periods.

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### TYPICAL APPLICATION



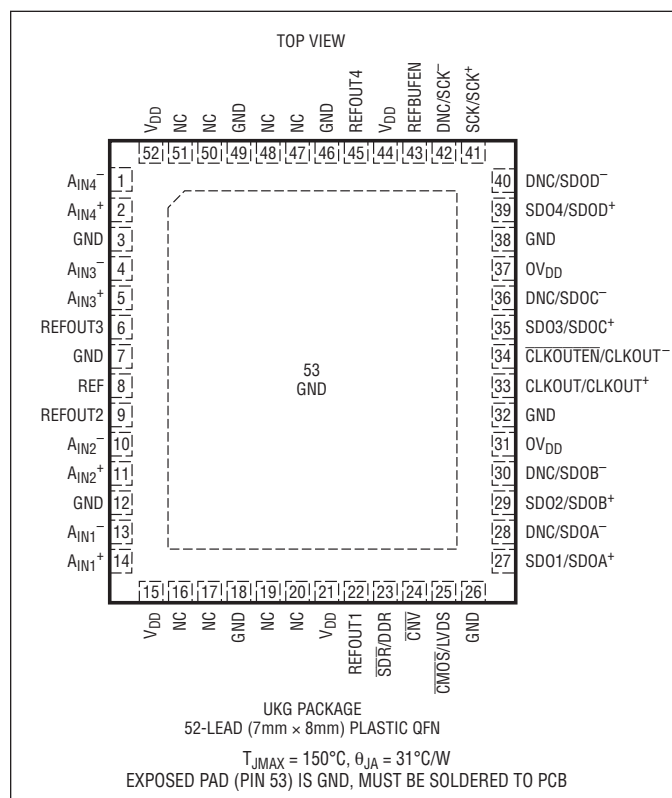
# LTC2325-12

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{DD}$ )	6V
Supply Voltage ( $OV_{DD}$ )	3V
Analog Input Voltage	
$A_{IN+}$ , $A_{IN-}$ (Note 3)	–0.3V to ( $V_{DD} + 0.3V$ )
REFOUT1,2,3,4	–0.3V to ( $V_{DD} + 0.3V$ )
CNV	–0.3V to ( $OV_{DD} + 0.3V$ )
Digital Input Voltage	
(Note 3)	( $GND - 0.3V$ ) to ( $OV_{DD} + 0.3V$ )
Digital Output Voltage	
(Note 3)	( $GND - 0.3V$ ) to ( $OV_{DD} + 0.3V$ )
Operating Temperature Range	
LTC2325C	0°C to 70°C
LTC2325I	–40°C to 85°C
LTC2325H	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

<http://www.linear.com/product/LTC2325-12#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2325CUKG-12#PBF	LTC2325CUKG-12#TRPBF	LTC2325UKG-12	52-Lead (7mm × 8mm) Plastic QFN	0°C to 70°C
LTC2325IUKG-12#PBF	LTC2325IUKG-12#TRPBF	LTC2325UKG-12	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 85°C
LTC2325HUKG-12#PBF	LTC2325HUKG-12#TRPBF	LTC2325UKG-12	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN+}$	Absolute Input Range ( $A_{IN+}$ to $A_{IN-}$ )	(Note 5)	●	0		$V_{DD}$	V
$V_{IN-}$	Absolute Input Range ( $A_{IN+}$ to $A_{IN-}$ )	(Note 5)	●	0		$V_{DD}$	V
$V_{IN+} - V_{IN-}$	Input Differential Voltage Range	$V_{IN} = V_{IN+} - V_{IN-}$	●	–REFOUT1,2,3,4		REFOUT1,2,3,4	V
$V_{CM}$	Common Mode Input Range	$V_{CM} = (V_{IN+} - V_{IN-})/2$	●	0		$V_{DD}$	V
$I_{IN}$	Analog Input DC Leakage Current		●	–1		1	$\mu\text{A}$
$C_{IN}$	Analog Input Capacitance				10		pF
CMRR	Input Common Mode Rejection Ratio	$f_{IN} = 2.2\text{MHz}$			102		dB
$V_{IHCNV}$	$\overline{\text{CNV}}$ High Level Input Voltage		●	1.5			V
$V_{ILCNV}$	$\overline{\text{CNV}}$ Low Level Input Voltage		●			0.5	V
$I_{INCNV}$	$\overline{\text{CNV}}$ Input Current		●	–10		10	$\mu\text{A}$

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	12			Bits
	No Missing Codes		●	12			Bits
	Transition Noise				0.3		$\text{LSB}_{\text{RMS}}$
INL	Integral Linearity Error	(Note 6)	●	–1	$\pm 0.5$	1	LSB
DNL	Differential Linearity Error		●	–0.99	$\pm 0.4$	0.99	LSB
BZE	Bipolar Zero-Scale Error	(Note 7)	●	–1	0	1	LSB
	Bipolar Zero-Scale Error Drift				0.01		$\text{LSB}/^\circ\text{C}$
FSE	Bipolar Full-Scale Error	$V_{\text{REFOUT}1,2,3,4} = 4.096\text{V}$ (REFBUFEN Grounded) (Note 7)	●	–2		2	LSB
	Bipolar Full-Scale Error Drift	$V_{\text{REFOUT}1,2,3,4} = 4.096\text{V}$ (REFBUFEN Grounded)			15		$\text{ppm}/^\circ\text{C}$

**DYNAMIC ACCURACY**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  and  $A_{IN} = -1\text{dBFS}$  (Notes 4, 8).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 4.096\text{V}$ , Internal Reference	●	74	76	dB
		$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 5\text{V}$ , External Reference		76.5		dB
SNR	Signal-to-Noise Ratio	$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 4.096\text{V}$ , Internal Reference	●	75	77	dB
		$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 5\text{V}$ , External Reference		77.6		dB
THD	Total Harmonic Distortion	$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 4.096\text{V}$ , Internal Reference	●	-86	-76	dB
		$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 5\text{V}$ , External Reference		-85		dB
SFDR	Spurious Free Dynamic Range	$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 4.096\text{V}$ , Internal Reference	●	76	93	dB
		$f_{IN} = 2.2\text{MHz}$ , $V_{REFOUT1,2,3,4} = 5\text{V}$ , External Reference		93		dB
	-3dB Input Bandwidth			95		MHz
	Aperture Delay			500		ps
	Aperture Delay Matching			500		ps
	Aperture Jitter			1		ps <sub>RMS</sub>
	Transient Response	Full-Scale Step		30		ns

**INTERNAL REFERENCE CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{REFOUT1,2,3,4}$	Internal Reference Output Voltage	$4.75\text{V} < V_{DD} < 5.25\text{V}$	●	4.078	4.096	V
		$3.13\text{V} < V_{DD} < 3.47\text{V}$	●	2.034	2.048	V
	$V_{REF}$ Temperature Coefficient	(Note 14)	●	3	20	ppm/ $^\circ\text{C}$
	REFOUT1,2,3,4 Output Impedance			0.25		$\Omega$
	$V_{REFOUT1,2,3,4}$ Line Regulation	$4.75\text{V} < V_{DD} < 5.25\text{V}$		0.3		mV/V
$I_{REFOUT1,2,3,4}$	External Reference Current	REFBUFEN = 0V		500		$\mu\text{A}$
		REFOUT1,2,3,4 = 4.096V REFOUT1,2,3,4 = 2.048V (Notes 9, 10)		300		$\mu\text{A}$

## DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS Digital Inputs and Outputs		CMOS/LVDS = GND					
V <sub>IH</sub>	High Level Input Voltage		●	0.8 • OV <sub>DD</sub>			V
V <sub>IL</sub>	Low Level Input Voltage		●	0.2 • OV <sub>DD</sub>			V
I <sub>IN</sub>	Digital Input Current	V <sub>IN</sub> = 0V to OV <sub>DD</sub>	●	-10	10		μA
C <sub>IN</sub>	Digital Input Capacitance		●	5			pF
V <sub>OH</sub>	High Level Output Voltage	I <sub>O</sub> = -500μA	●	OV <sub>DD</sub> - 0.2			V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>O</sub> = 500μA	●	0.2			V
I <sub>OZ</sub>	Hi-Z Output Leakage Current	V <sub>OUT</sub> = 0V to OV <sub>DD</sub>	●	-10	10		μA
I <sub>SOURCE</sub>	Output Source Current	V <sub>OUT</sub> = 0V	●	-10			mA
I <sub>SINK</sub>	Output Sink Current	V <sub>OUT</sub> = OV <sub>DD</sub>	●	10			mA
LVDS Digital Inputs and Outputs		CMOS/LVDS = OV <sub>DD</sub>					
V <sub>ID</sub>	LVDS Differential Input Voltage	100Ω Differential Termination OV <sub>DD</sub> = 2.5V	●	240	600		mV
V <sub>IS</sub>	LVDS Common Mode Input Voltage	100Ω Differential Termination OV <sub>DD</sub> = 2.5V	●	1	1.45		V
V <sub>OD</sub>	LVDS Differential Output Voltage	100Ω Differential Termination OV <sub>DD</sub> = 2.5V	●	220	350	600	mV
V <sub>OS</sub>	LVDS Common Mode Output Voltage	100Ω Differential Termination OV <sub>DD</sub> = 2.5V	●	0.85	1.2	1.4	V
V <sub>OD_LP</sub>	Low Power LVDS Differential Output Voltage	100Ω Differential Termination OV <sub>DD</sub> = 2.5V	●	100	200	350	mV
V <sub>OS_LP</sub>	Low Power LVDS Common Mode Output Voltage	100Ω Differential Termination OV <sub>DD</sub> = 2.5V	●	0.85	1.2	1.4	V

## POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{DD}$	Supply Voltage	5V Operation 3.3V Operation	● ●	4.75 3.13		5.25 3.47	V V
$I_{VDD}$	Supply Current	5Msps Sample Rate ( $I_{IN^+} = I_{IN^-} = 0V$ )	●		31	44.5	mA

### CMOS I/O Mode: CMOS/LVDS = GND

$OV_{DD}$	Supply Voltage		●	1.71		2.63	V
$I_{OVDD}$	Supply Current	5Msps Sample Rate ( $C_L = 5pF$ )	●		4.4	15.5	mA
$I_{NAP}$	Nap Mode Current	Conversion Done ( $I_{VDD}$ )	●		5.3	6.4	mA
$I_{SLEEP}$	Sleep Mode Current	Sleep Mode ( $I_{VDD} + I_{OVDD}$ )	●		20	90	$\mu A$
$P_{D\_3.3V}$	Power Dissipation	$V_{DD} = 3.3V$ , 5Msps Sample Rate Nap Mode Sleep Mode	● ● ●		102 18 20	181 21.1 288	mW mW $\mu W$
$P_{D\_5V}$	Power Dissipation	$V_{DD} = 5V$ , 5Msps Sample Rate Nap Mode Sleep Mode	● ● ●		162 27 30	261 32 424	mW mW $\mu W$

### LVDS I/O Mode: CMOS/LVDS = $OV_{DD}$ , $OV_{DD} = 2.5V$

$OV_{DD}$	Supply Voltage		●	2.37		2.63	V
$I_{OVDD}$	Supply Current	5Msps Sample Rate ( $C_L = 5pF$ , $R_L = 100\Omega$ )	●		26	32	mA
$I_{NAP}$	Nap Mode Current	Conversion Done ( $I_{VDD}$ )	●		5.3	6.4	mA
$I_{SLEEP}$	Sleep Mode Current	Sleep Mode ( $I_{VDD} + I_{OVDD}$ )	●		20	90	$\mu A$
$P_{D\_3.3V}$	Power Dissipation	$V_{DD} = 3.3V$ , 5Msps Sample Rate Nap Mode Sleep Mode	● ● ●		151 52 80	218 58.6 288	mW mW $\mu W$
$P_{D\_5V}$	Power Dissipation	$V_{DD} = 5V$ , 5Msps Sample Rate Nap Mode Sleep Mode	● ● ●		214 50 40	303 69.2 424	mW mW $\mu W$

## ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$f_{SMPL}$	Maximum Sampling Frequency		●			5	Msps
$t_{CYC}$	Time Between Conversions	(Note 11) $t_{CYC} = t_{CNVH} + t_{CONV}$	●	0.2		1000	$\mu s$
$t_{CONV}$	Conversion Time		●			170	ns
$t_{CNVH}$	CNV High Time		●	30			ns
$t_{ACQUISITION}$	Sampling Aperture	(Note 11) $t_{ACQUISITION} = t_{CYC} - t_{CONV}$			28		ns
$t_{WAKE}$	REFOUT1,2,3,4 Wake-Up Time	$C_{REFOUT1,2,3,4} = 10\mu F$			50		ms

### CMOS I/O Mode: SDR, CMOS/LVDS = GND, SDR/DDR = GND

$t_{SCK}$	SCK Period	(Note 13)	●	9.1			ns
$t_{SCKH}$	SCK High Time		●	4.1			ns
$t_{SCKL}$	SCK Low Time		●	4.1			ns
$t_{HSDO\_SDR}$	SDO Data Remains Valid Delay from CLKOUT↓	$C_L = 5pF$ (Note 12)	●	0		1.5	ns
$t_{DSCKCLKOUT}$	SCK to CLKOUT Delay	(Note 12)	●	2.5		4.5	ns

## ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$  (Note 4).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{DCNVSDOZ}}$	Bus Relinquish Time After $\overline{\text{CNV}}\uparrow$	(Note 11)	●		3	ns
$t_{\text{DCNVSDOV}}$	SDO Valid Delay from $\overline{\text{CNV}}\downarrow$	(Note 11)	●		3	ns
$t_{\text{DSCKHCNVH}}$	SCK Delay Time to $\overline{\text{CNV}}\uparrow$	(Note 11)	●	0		ns

### CMOS I/O Mode: DDR, CMOS/LVDS = GND, $\overline{\text{SDR}}/\text{DDR} = \text{OV}_{\text{DD}}$

$t_{\text{SCK}}$	SCK Period		●	18.2		ns
$t_{\text{SCKH}}$	SCK High Time		●	8.2		ns
$t_{\text{SCKL}}$	SCK Low Time		●	8.2		ns
$t_{\text{HSDO\_DDR}}$	SDO Data Remains Valid Delay from $\text{CLKOUT}\downarrow$	$C_L = 5\text{pF}$ (Note 12)	●	0	1.5	ns
$t_{\text{DSCKCLKOUT}}$	SCK to $\text{CLKOUT}$ Delay	(Note 12)	●	2	4.5	ns
$t_{\text{DCNVSDOZ}}$	Bus Relinquish Time After $\overline{\text{CNV}}\uparrow$	(Note 11)	●		3	ns
$t_{\text{DCNVSDOV}}$	SDO Valid Delay from $\overline{\text{CNV}}\downarrow$	(Note 11)	●		3	ns
$t_{\text{DSCKHCNVH}}$	SCK Delay Time to $\overline{\text{CNV}}\uparrow$	(Note 11)	●	0		ns

### LVDS I/O Mode: SDR, CMOS/LVDS = $\text{OV}_{\text{DD}}$ , $\overline{\text{SDR}}/\text{DDR} = \text{GND}$

$t_{\text{SCK}}$	SCK Period		●	9.1		ns
$t_{\text{SCKH}}$	SCK High Time		●	4.1		ns
$t_{\text{SCKL}}$	SCK Low Time		●	4.1		ns
$t_{\text{HSDO\_SDR}}$	SDO Data Remains Valid Delay from $\text{CLKOUT}\downarrow$	$C_L = 5\text{pF}$ (Note 12)	●	0	1.5	ns
$t_{\text{DSCKCLKOUT}}$	SCK to $\text{CLKOUT}$ Delay	(Note 12)	●	2	4	ns
$t_{\text{DSCKHCNVH}}$	SCK Delay Time to $\overline{\text{CNV}}\uparrow$	(Note 11)	●	0		ns

### LVDS I/O Mode: DDR, CMOS/LVDS = $\text{OV}_{\text{DD}}$ , $\overline{\text{SDR}}/\text{DDR} = \text{OV}_{\text{DD}} = 2.5\text{V}$

$t_{\text{SCK}}$	SCK Period		●	18.2		ns
$t_{\text{SCKH}}$	SCK High Time		●	8.2		ns
$t_{\text{SCKL}}$	SCK Low Time		●	8.2		ns
$t_{\text{HSDO\_DDR}}$	SDO Data Remains Valid Delay from $\text{CLKOUT}\downarrow$	$C_L = 5\text{pF}$ (Note 12)	●	0	1.5	ns
$t_{\text{DSCKCLKOUT}}$	SCK to $\text{CLKOUT}$ Delay	(Note 12)	●	2	4	ns
$t_{\text{DSCKHCNVH}}$	SCK Delay Time to $\overline{\text{CNV}}\uparrow$	(Note 11)	●	0		ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to ground.

**Note 3:** When these pin voltages are taken below ground, or above  $V_{\text{DD}}$  or  $\text{OV}_{\text{DD}}$ , they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground, or above  $V_{\text{DD}}$  or  $\text{OV}_{\text{DD}}$ , without latch-up.

**Note 4:**  $V_{\text{DD}} = 5\text{V}$ ,  $\text{OV}_{\text{DD}} = 2.5\text{V}$ ,  $\text{REFOUT}_{1,2,3,4} = 4.096\text{V}$ ,  $f_{\text{SMPL}} = 5\text{MHz}$ .

**Note 5:** Recommended operating conditions.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** Bipolar zero error is the offset voltage measured from  $-0.5\text{LSB}$  when the output code flickers between 0 0000 0000 0000 and 1 1111 1111 1111. Full-scale bipolar error is the worst-case of  $-\text{FS}$  or  $+\text{FS}$

untrimmed deviation from ideal first and last code transitions and includes the effect of offset error.

**Note 8:** All specifications in dB are referred to a full-scale  $\pm 4.096\text{V}$  input with  $\text{REF} = 4.096\text{V}$ .

**Note 9:** When  $\text{REFOUT}_{1,2,3,4}$  is overdriven, the internal reference buffer must be turned off by setting  $\text{REFBUFEN} = 0\text{V}$ .

**Note 10:**  $f_{\text{SMPL}} = 5\text{MHz}$ ,  $I_{\text{REFOUT}_{1,2,3,4}}$  varies proportionally with sample rate.

**Note 11:** Guaranteed by design, not subject to test.

**Note 12:** Parameter tested and guaranteed at  $\text{OV}_{\text{DD}} = 1.71\text{V}$  and  $\text{OV}_{\text{DD}} = 2.5\text{V}$ .

**Note 13:**  $t_{\text{SCK}}$  of 9.1ns allows a shift clock frequency up to 105MHz for rising edge capture.

**Note 14:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

**Note 15:**  $\overline{\text{CNV}}$  is driven from a low jitter digital source, typically at  $\text{OV}_{\text{DD}}$  logic levels.

ADC TIMING CHARACTERISTICS

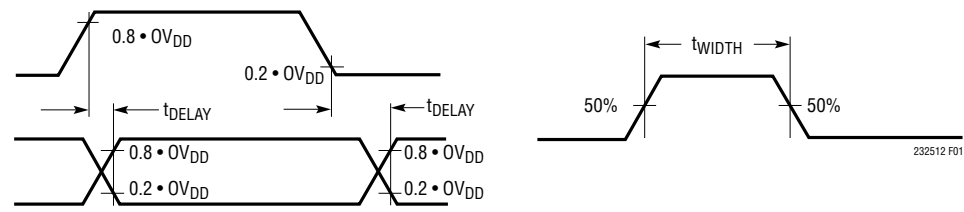
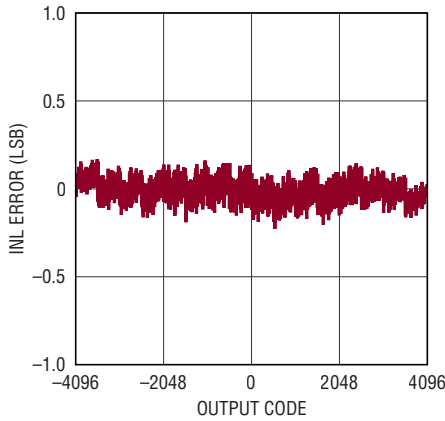


Figure 1. Voltage Levels for Timing Specifications

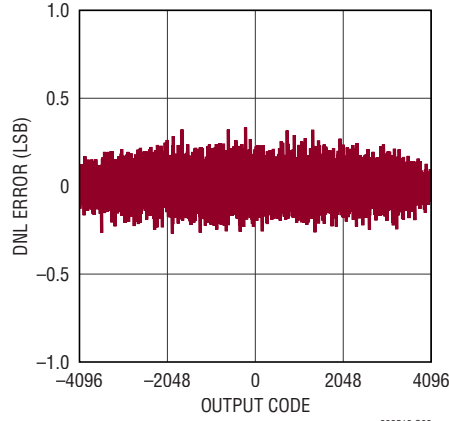
# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $0V_{DD} = 2.5\text{V}$ ,  $\text{REFOUT1,2,3,4} = 4.096\text{V}$ ,  $f_{\text{SAMPL}} = 5\text{Msps}$ , unless otherwise noted.

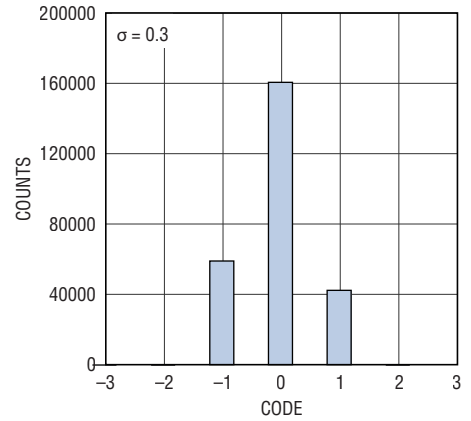
**Integral Nonlinearity vs Output Code**



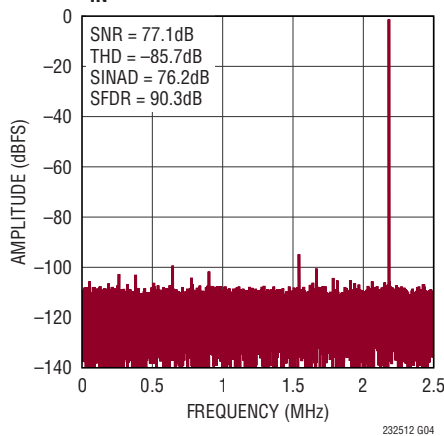
**Differential Nonlinearity vs Output Code**



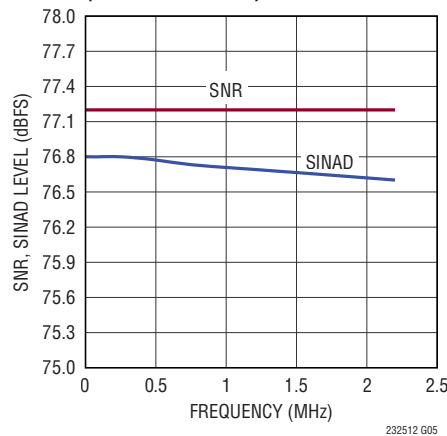
**DC Histogram**



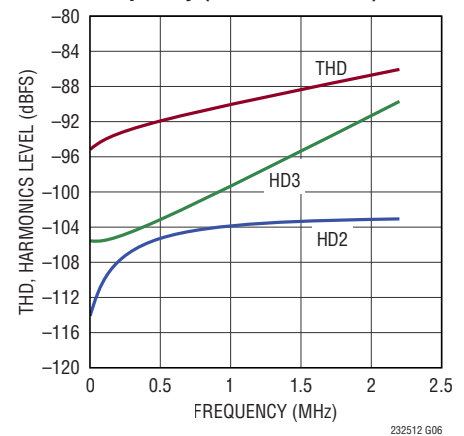
**32k Point FFT,  $f_{\text{SAMPL}} = 5\text{Msps}$ ,  $f_{\text{IN}} = 2.2\text{MHz}$**



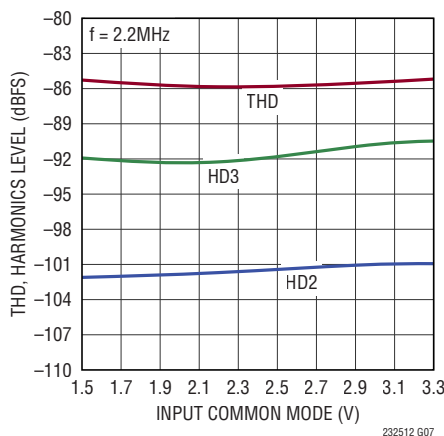
**SNR, SINAD vs Input Frequency (1kHz to 2.2MHz)**



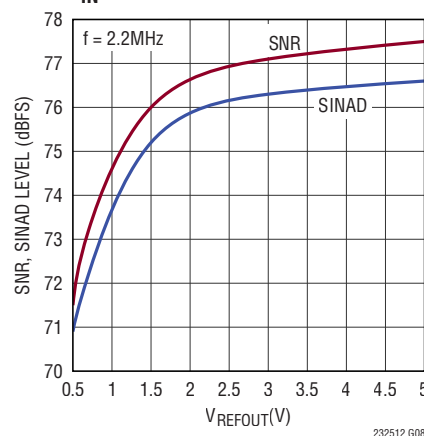
**THD, Harmonics vs Input Frequency (1kHz to 2.2MHz)**



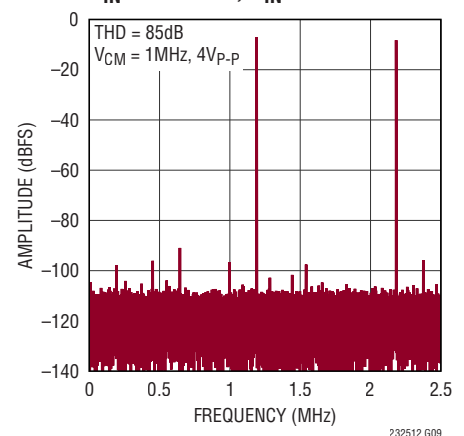
**THD, Harmonics vs Input Common Mode**



**SNR, SINAD vs Reference Voltage,  $f_{\text{IN}} = 2.2\text{MHz}$**



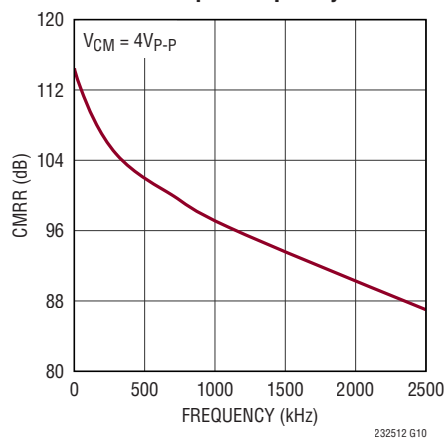
**32k Point FFT, IMD,  $f_{\text{SAMPL}} = 5\text{Msps}$ ,  $A_{\text{IN}}^+ = 1.2\text{MHz}$ ,  $A_{\text{IN}}^- = 2.2\text{MHz}$**



# TYPICAL PERFORMANCE CHARACTERISTICS

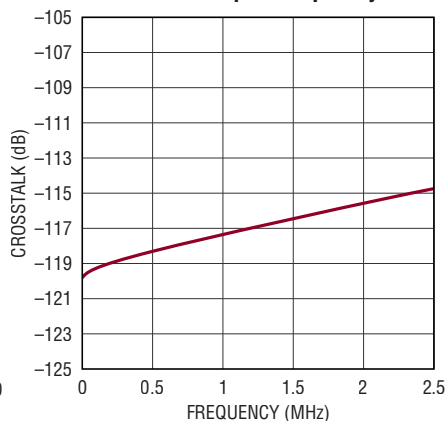
$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 5\text{V}$ ,  $OV_{DD} = 2.5\text{V}$ ,  $REFOUT1,2,3,4 = 4.096\text{V}$ ,  $f_{SAMPL} = 5\text{Msps}$ , unless otherwise noted.

CMRR vs Input Frequency



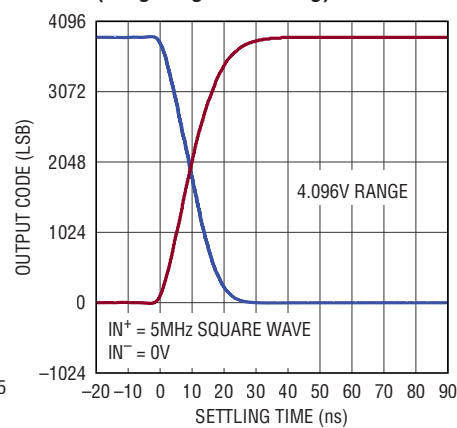
232512 G10

Crosstalk vs Input Frequency



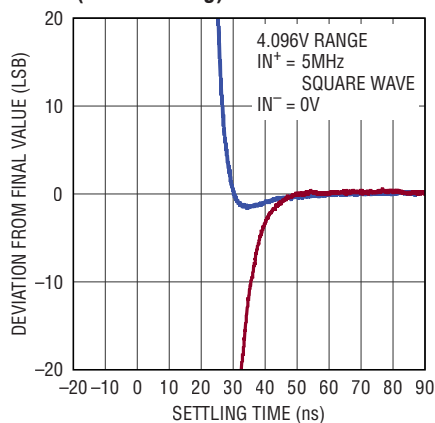
232512 G11

Step Response (Large Signal Settling)



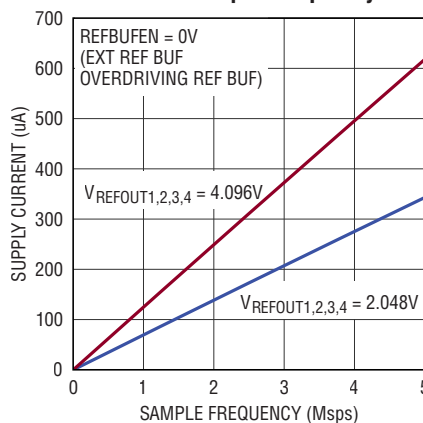
232512 G12

Step Response (Fine Settling)



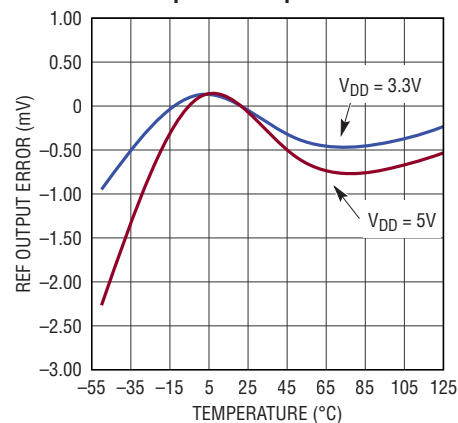
232512 G13

External Reference Supply Current vs Sample Frequency



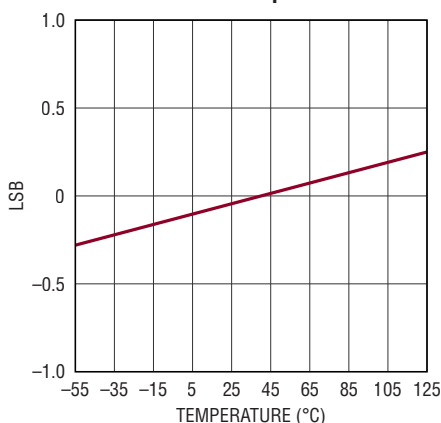
232512 G14

REF Output vs Temperature



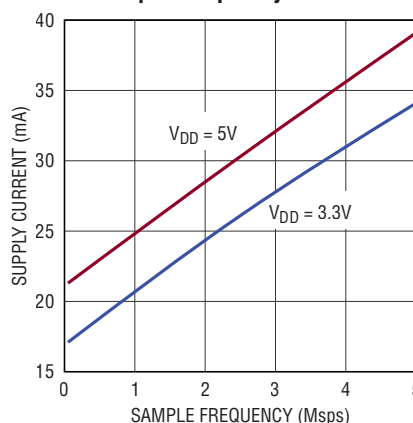
232512 G15

Offset Error vs Temperature

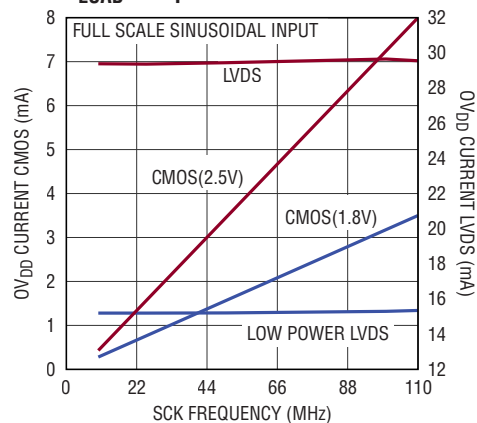


232512 G16

Supply Current vs Sample Frequency



232512 G17

 $OV_{DD}$  Current vs SCK Frequency,  $C_{LOAD} = 10\text{pF}$ 

232512 G18

## PIN FUNCTIONS

### PINS THAT ARE THE SAME FOR ALL DIGITAL I/O MODES

**AIN4<sup>+</sup>, AIN4<sup>-</sup> (Pins 2, 1):** Analog Differential Input Pins. Full-scale range (AIN4<sup>+</sup> – AIN4<sup>-</sup>) is  $\pm$ REFOUT4 voltage. These pins can be driven from V<sub>DD</sub> to GND.

**GND (Pins 3, 7, 12, 18, 26, 32, 38, 46, 49):** Ground. These pins and exposed pad (Pin 53) must be tied directly to a solid ground plane.

**AIN3<sup>+</sup>, AIN3<sup>-</sup> (Pins 5, 4):** Analog Differential Input Pins. Full-scale range (AIN3<sup>+</sup> – AIN3<sup>-</sup>) is  $\pm$ REFOUT3 voltage. These pins can be driven from V<sub>DD</sub> to GND.

**REFOUT3 (Pin 6):** Reference Buffer 3 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 $\mu$ F (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

**REF (Pin 8):** Common 4.096V reference output. Decouple to GND with a 1 $\mu$ F low ESR ceramic capacitor. May be overdriven with a single external reference to establish a common reference for ADC cores 1 through 4.

**REFOUT2 (Pin 9):** Reference Buffer 2 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 $\mu$ F (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

**AIN2<sup>+</sup>, AIN2<sup>-</sup> (Pins 11, 10):** Analog Differential Input Pins. Full-scale range (AIN2<sup>+</sup> – AIN2<sup>-</sup>) is  $\pm$ REFOUT2 voltage. These pins can be driven from V<sub>DD</sub> to GND.

**AIN1<sup>+</sup>, AIN1<sup>-</sup> (Pins 14, 13):** Analog Differential Input Pins. Full-scale range (AIN1<sup>+</sup> – AIN1<sup>-</sup>) is  $\pm$ REFOUT1 voltage. These pins can be driven from V<sub>DD</sub> to GND.

**V<sub>DD</sub> (Pins 15, 21, 44, 52):** Power Supply. Bypass V<sub>DD</sub> to GND with a 10 $\mu$ F ceramic capacitor and a 0.1 $\mu$ F ceramic capacitor close to the part. The V<sub>DD</sub> pins should be shorted together and driven from the same supply.

**REFOUT1 (Pin 22):** Reference Buffer 1 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 $\mu$ F (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

**SDR/DDR (Pin 23):** Double Data Rate Input. Controls the frequency of SCK and CLKOUT. Tie to GND for the falling edge of SCK to shift each serial data output (Single Data Rate, SDR). Tie to OV<sub>DD</sub> to shift serial data output on each edge of SCK (Double Data Rate, DDR). CLKOUT will be a delayed version of SCK for both pin states.

**CONV (Pin 24):** Convert Input. This pin, when high, defines the acquisition phase. When this pin is driven low, the conversion phase is initiated and output data is clocked out. This input must be driven at OV<sub>DD</sub> levels with a low jitter pulse. This pin is unaffected by the CMOS/LVDS pin.

**CMOS/LVDS (Pin 25):** I/O Mode Select. Ground this pin to enable CMOS mode, tie to OV<sub>DD</sub> to enable LVDS mode. Float this pin to enable low power LVDS mode.

**OV<sub>DD</sub> (Pins 31, 37):** I/O Interface Digital Power. The range of OV<sub>DD</sub> is 1.71V to 2.63V. This supply is nominally set to the same supply as the host interface (CMOS: 1.8V or 2.5V, LVDS: 2.5V). Bypass OV<sub>DD</sub> to GND (Pins 32 and 38) with 0.1 $\mu$ F capacitors.

**REFBUFEN (Pin 43):** Reference Buffer Output Enable. Tie to V<sub>DD</sub> when using the internal reference. Tie to ground to disable the internal REFOUT1–4 buffers for use with external voltage references. This pin has a 500k internal pull-up to V<sub>DD</sub>.

**REFOUT4 (Pin 45):** Reference Buffer 4 Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 10 $\mu$ F (X5R, 0805 size) ceramic capacitor. The internal buffer driving this pin may be disabled by grounding the REFBUFEN pin. If the buffer is disabled, an external reference may drive this pin in the range of 1.25V to 5V.

**Exposed Pad (Pin 53):** Ground. Solder this pad to ground.

## PIN FUNCTIONS

### CMOS DATA OUTPUT OPTION ( $\overline{\text{CMOS}}/\text{LVDS} = \text{LOW}$ )

**SDO1 (Pin 27):** CMOS Serial Data Output for ADC Channel 1. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDO1 in SDR mode, 8 SCK edges in DDR mode.

**SDO2 (Pin 29):** CMOS Serial Data Output for ADC Channel 2. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDO2 in SDR mode, 8 SCK edges in DDR mode.

**SDO3 (Pin 35):** CMOS Serial Data Output for ADC Channel 3. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDO3 in SDR mode, 8 SCK edges in DDR mode.

**SDO4 (Pin 39):** CMOS Serial Data Output for ADC Channel 4. The conversion result is shifted MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDO4 in SDR mode, 8 SCK edges in DDR mode.

**CLKOUT (Pin 33):** Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver (FPGA). The logic level is determined by  $\text{OV}_{\text{DD}}$ . This pin echoes the input at SCK with a small delay.

**CLKOUTEN (Pin 34):** CLKOUT can be disabled by tying Pin 34 to  $\text{OV}_{\text{DD}}$  for a small power savings. If CLKOUT is used, ground this pin.

**SCK (Pin 41):** Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins in SDR mode ( $\text{DDR} = \text{LOW}$ ). In DDR mode ( $\overline{\text{SDR}}/\text{DDR} = \text{HIGH}$ ) each edge of this clock shifts the conversion result MSB first onto the SDO pins. The logic level is determined by  $\text{OV}_{\text{DD}}$ .

**DNC (Pins 28, 30, 36, 40, 42):** In CMOS mode, do not connect this pin.

### LVDS DATA OUTPUT OPTION ( $\overline{\text{CMOS}}/\text{LVDS} = \text{HIGH OR FLOAT}$ )

**SDOA<sup>+</sup>, SDOA<sup>-</sup> (Pins 27, 28):** LVDS Serial Data Output for ADC Channel 1. The conversion result is shifted CH1 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDOA in SDR mode, 8 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

**SDOB<sup>+</sup>, SDOB<sup>-</sup> (Pins 29, 30):** LVDS Serial Data Output for ADC Channel 2. The conversion result is shifted CH2 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDOB in SDR mode, 8 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

**CLKOUT<sup>+</sup>, CLKOUT<sup>-</sup> (Pins 33, 34):** Serial Data Clock Output. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. These pins echo the input at SCK with a small delay. These pins must be differentially terminated by an external 100Ω resistor at the receiver (FPGA).

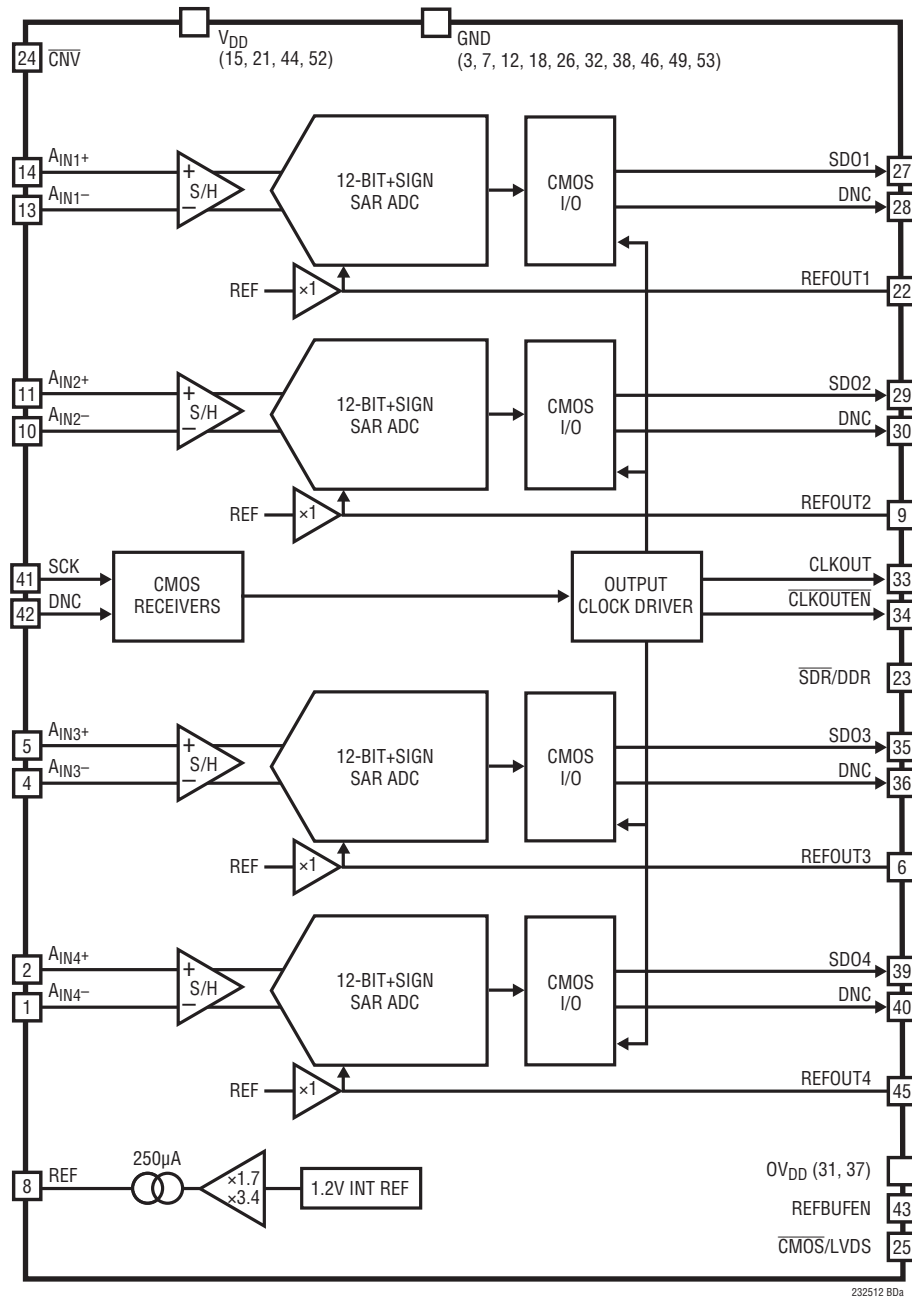
**SDOC<sup>+</sup>, SDOC<sup>-</sup> (Pins 35, 36):** LVDS Serial Data Output for ADC channel 3. The conversion result is shifted CH3 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDOA in SDR mode, 8 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

**SDOD<sup>+</sup>, SDOD<sup>-</sup> (Pins 39, 40):** LVDS Serial Data Output for ADC Channel 4. The conversion result is shifted CH4 MSB first on each falling edge of SCK in SDR mode and each SCK edge in DDR mode. 16 SCK edges are required for 13-bit conversion data to be read from SDOA in SDR mode, 8 SCK edges in DDR mode. Terminate with a 100Ω resistor at the receiver (FPGA).

**SCK<sup>+</sup>, SCK<sup>-</sup> (Pins 41, 42):** Serial Data Clock Input. The falling edge of this clock shifts the conversion result MSB first onto the SDO pins in SDR mode ( $\overline{\text{SDR}}/\text{DDR} = \text{LOW}$ ). In DDR mode ( $\overline{\text{SDR}}/\text{DDR} = \text{HIGH}$ ) each edge of this clock shifts the conversion result MSB first onto the SDO pins. These pins must be differentially terminated by an external 100Ω resistor at the receiver (ADC).

## FUNCTIONAL BLOCK DIAGRAM

CMOS IO Mode



Pin diagram of the AD9288 12-bit SAR ADC with LVDS I/O. The diagram shows 52 pins with various functions including analog inputs (AIN1+, AIN1-, AIN2+, AIN2-, AIN3+, AIN3-, AIN4+, AIN4-), digital inputs (SCK+, SCK-), reference inputs (REF), and LVDS outputs (SDOA+, SDOA-, SDOB+, SDOB-, SDOC+, SDOC-, SDOD+, SDOD-). It also includes pins for REFOUT1, REFOUT2, REFOUT3, REFOUT4, CLKOUT+, CLKOUT-, SDR/DDR, and control pins (OVDD, REFBUFEN, CMOS/LVDS). Power pins VDD (15, 21, 44, 52) and GND (3, 7, 12, 18, 26, 32, 38, 46, 49, 53) are also indicated.

The diagram illustrates the timing of the AD\_CONVERTER. It shows the relationship between the conversion start signal (CNV), the serial clock (SCK), the clock output (CLKOUT), and the data outputs (SD01 and SD04) across two samples, SAMPLE N and SAMPLE N+1.

- CNV:** The conversion start signal. It is active (high) during the ACQUIRE phase and then transitions to a high-impedance (Hi-Z) state during the CONVERSION AND READOUT phase.
- SCK:** The serial clock. It is active during the CONVERSION AND READOUT phase, providing a clock for the data outputs.
- CLKOUT:** The clock output. It is active during the CONVERSION AND READOUT phase, providing a clock for the data outputs.
- SD01 and SD04:** The data outputs. They are active during the CONVERSION AND READOUT phase, providing the digital data for the conversion.
- Serial Data Bits:** The data outputs provide 13 bits of data (D12 to D0) for each sample. The bits D12 to D0 correspond to the previous conversion of the channel (CH1 for SD01 and CH4 for SD04).
- Phases:** The diagram is divided into two main phases: ACQUIRE and CONVERSION AND READOUT. The ACQUIRE phase is the time between the start of the conversion and the start of the readout. The CONVERSION AND READOUT phase is the time during which the data is being read out.

The diagram illustrates the timing of the AD\_CONVERTER signals during an acquisition and conversion cycle. The cycle is divided into two main phases: **ACQUIRE** and **CONVERSION AND READOUT**.

**Signals and Timing:**

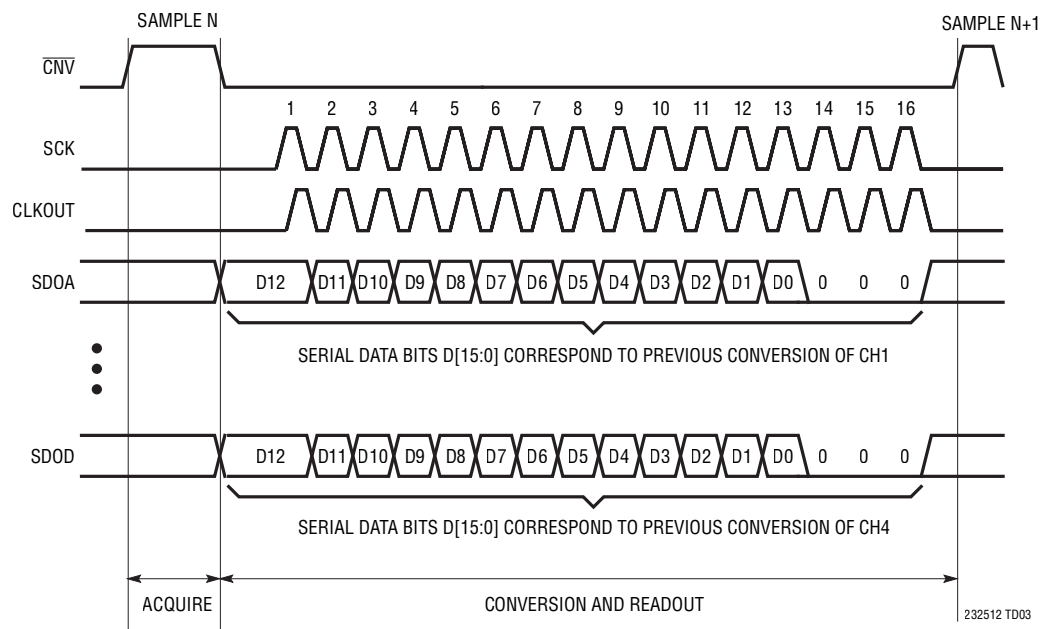
- CNV:** The conversion start signal. It is active (low) during the **ACQUIRE** phase and transitions to high at the start of the **CONVERSION AND READOUT** phase.
- SCK:** The serial clock signal. It is active during the **CONVERSION AND READOUT** phase, with 16 clock cycles labeled 1 through 16.
- CLKOUT:** The clock output signal. It is in a high-impedance (**Hi-Z**) state during the **ACQUIRE** phase and transitions to a square wave during the **CONVERSION AND READOUT** phase.
- SDIO:** The serial data input/output signal. It is in a high-impedance (**Hi-Z**) state during the **ACQUIRE** phase and transitions to a square wave during the **CONVERSION AND READOUT** phase. The data is organized into 16-bit words, with the first 12 bits (D12-D0) corresponding to the previous conversion of the channel (CH1 or CH4) and the last 4 bits (D3-D0) being zeros.

**Annotations:**

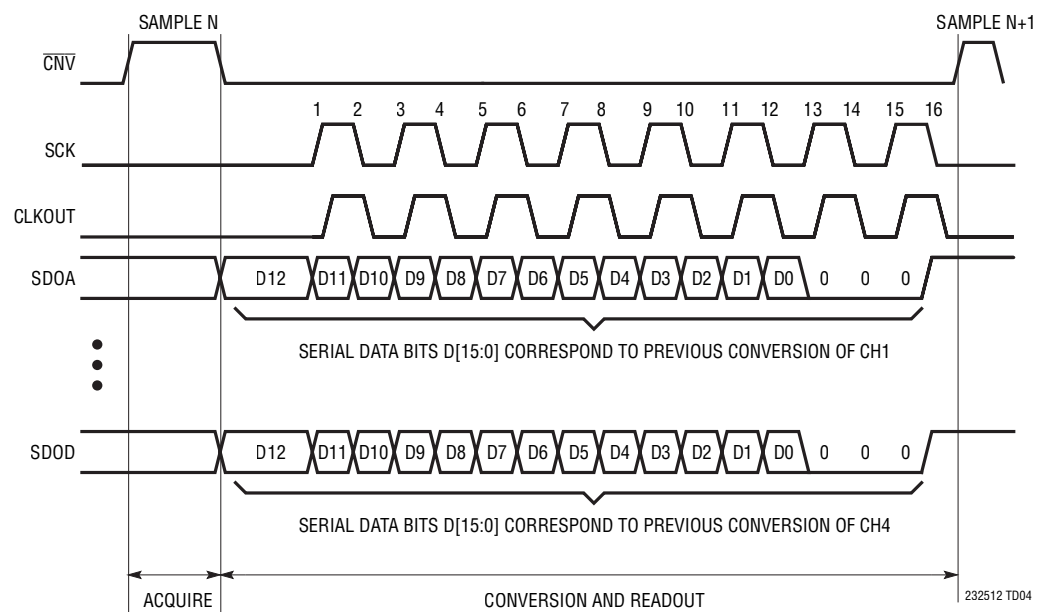
- SAMPLE N:** The start of the acquisition phase.
- SAMPLE N+1:** The start of the next acquisition phase.
- 232512 TD02:** The document reference number.

TIMING DIAGRAM

SDR Mode, LVDS



DDR Mode, LVDS



APPLICATIONS INFORMATION

OVERVIEW

The LTC2325-12 is a low noise, high speed 12-bit successive approximation register (SAR) ADC with differential inputs and a wide input common mode range. Operating from a single 3.3V or 5V supply, the LTC2325-12 has a 4V<sub>P-P</sub> or 8V<sub>P-P</sub> differential input range, making it ideal for applications which require a wide dynamic range. The LTC2325-12 achieves ±0.5LSB INL typical, no missing codes at 12 bits and 77dB SNR.

The LTC2325-12 has an onboard reference buffer and low drift (20ppm/°C max) 4.096V temperature-compensated reference. The LTC2325-12 also has a high speed SPI-compatible serial interface that supports CMOS or LVDS. The fast 5Msps per channel throughput with one-cycle latency makes the LTC2325-12 ideally suited for a wide variety of high speed applications. The LTC2325-12 dissipates only 45mW per channel. Nap and sleep modes are also provided to reduce the power consumption of the LTC2325-12 during inactive periods for further power savings.

CONVERTER OPERATION

The LTC2325-12 operates in two phases. During the acquisition phase, the sample capacitor is connected to the analog input pins A<sub>IN+</sub> and A<sub>IN-</sub> to sample the differential analog input voltage, as shown in Figure 3. A falling edge on the  $\overline{\text{CNV}}$  pin initiates a conversion. During the conversion phase, the 13-bit CDAC is sequenced through a successive approximation algorithm effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g., V<sub>REFOUT</sub>/2, V<sub>REFOUT</sub>/4 ... V<sub>REFOUT</sub>/32768) using a differential comparator. At the end of conversion, a CDAC output approximates the sampled analog input. The ADC control logic then prepares the 13-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2325-12 digitizes the full-scale voltage of 2 • REFOUT1,2,3,4 into 2<sup>13</sup> levels, resulting in an LSB size of 1mV with REF=4.096V. The ideal transfer function is shown in Figure 2. The output data is in 2's complement format. When driven by fully differential inputs, the transfer function spans 2<sup>13</sup> codes. When driven by pseudo-differential inputs, the transfer function spans 2<sup>12</sup> codes.

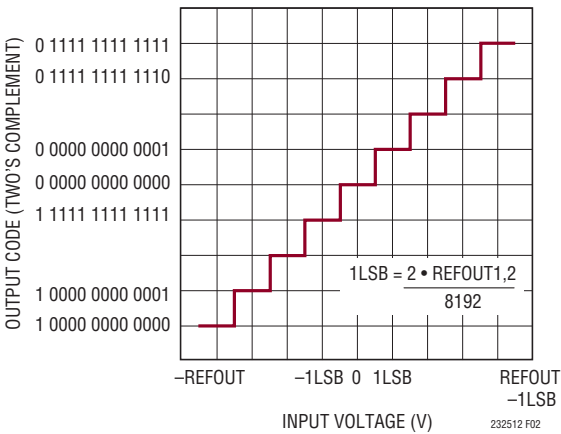


Figure 2. LTC2325-12 Transfer Function

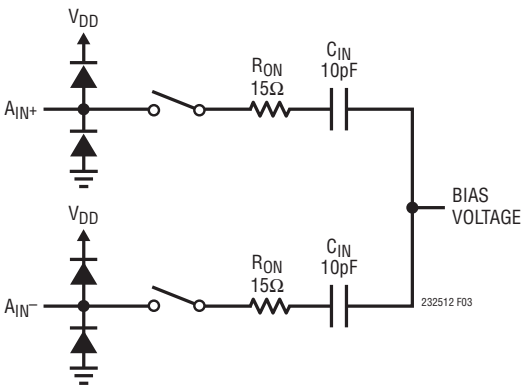


Figure 3. The Equivalent Circuit for the Differential Analog Input of the LTC2325-12

Table 1. Code Ranges for the Analog Input Operational Modes

MODE	SPAN (V <sub>IN+</sub> – V <sub>IN-</sub> )	MIN CODE	MAX CODE
Fully Differential	–REFOUT to +REFOUT	1 0000 0000 0000	0 1111 1111 1111
Pseudo-Differential Bipolar	–REFOUT/2 to +REFOUT/2	1 1000 0000 0000	0 0111 1111 1111
Pseudo-Differential Unipolar	0 to REFOUT	0 0000 0000 0000	0 1111 1111 1111

## APPLICATIONS INFORMATION

### Analog Input

The differential inputs of the LTC2325-12 provide great flexibility to convert a wide variety of analog signals with no configuration required. The LTC2325-12 digitizes the difference voltage between the  $A_{IN+}$  and  $A_{IN-}$  pins while supporting a wide common mode input range. The analog input signals can have an arbitrary relationship to each other, provided that they remain between  $V_{DD}$  and GND. The LTC2325-12 can also digitize more limited classes of analog input signals such as pseudo-differential unipolar/bipolar and fully differential with no configuration required.

The analog inputs of the LTC2325-12 can be modeled by the equivalent circuit shown in Figure 3. The back-to-back diodes at the inputs form clamps that provide ESD protection. In the acquisition phase,  $10\text{pF}$  ( $C_{IN}$ ) from the sampling capacitor in series with approximately  $15\Omega$  ( $R_{ON}$ ) from the on-resistance of the sampling switch

is connected to the input. Any unwanted signal that is common to both inputs will be reduced by the common mode rejection of the ADC sampler. The inputs of the ADC core draw a small current spike while charging the  $C_{IN}$  capacitors during acquisition.

### Single-Ended Signals

Single-ended signals can be directly digitized by the LTC2325-12. These signals should be sensed pseudo-differentially for improved common mode rejection. By connecting the reference signal (e.g., ground sense) of the main analog signal to the other  $A_{IN}$  pin, any noise or disturbance common to the two signals will be rejected by the high CMRR of the ADC. The LTC2325-12 flexibility handles both pseudo-differential unipolar and bipolar signals, with no configuration required. The wide common mode input range relaxes the accuracy requirements of any signal conditioning circuits prior to the analog inputs.

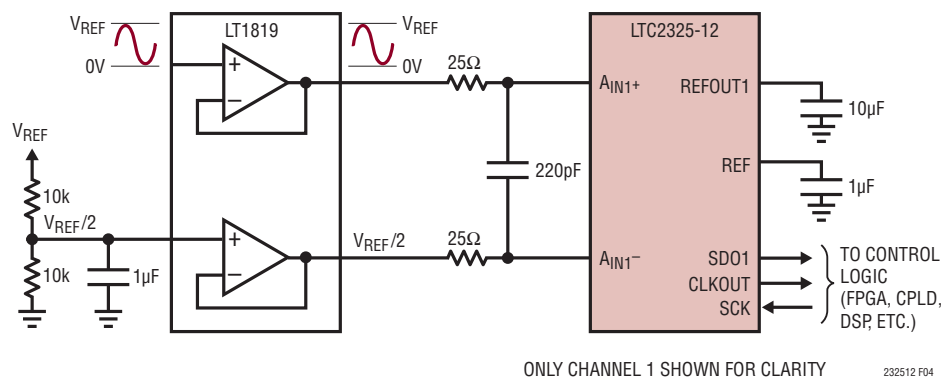


Figure 4. Pseudo-Differential Bipolar Application Circuit

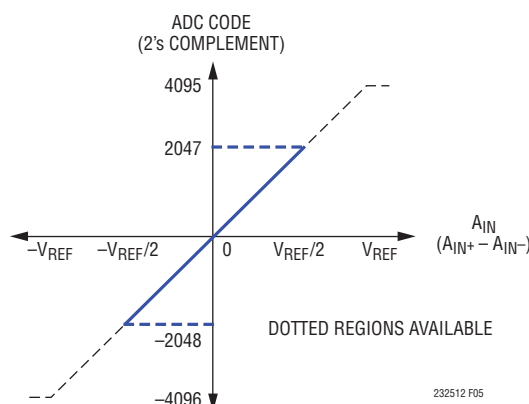


Figure 5. Pseudo-Differential Bipolar Transfer Function

## APPLICATIONS INFORMATION

### Pseudo-Differential Bipolar Input Range

The pseudo-differential bipolar configuration represents driving one of the analog inputs at a fixed voltage, typically  $V_{REF}/2$ , and applying a signal to the other  $A_{IN}$  pin. In this case the analog input swings symmetrically around the fixed input yielding bipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 4, and the corresponding transfer function in Figure 5. The fixed analog input pin need not be set at  $V_{REF}/2$ , but at some point within the  $V_{DD}$  rails allowing the alternate input to swing symmetrically around this voltage. If the input signal ( $A_{IN+} - A_{IN-}$ ) swings beyond  $\pm REFOUT1,2,3,4/2$ , valid codes will be generated by the ADC and must be clamped by the user, if necessary.

### Pseudo-Differential Unipolar Input Range

The pseudo-differential unipolar configuration represents driving one of the analog inputs at ground and applying a signal to the other  $A_{IN}$  pin. In this case, the analog input swings between ground and  $V_{REF}$  yielding unipolar two's complement output codes with an ADC span of half of full-scale. This configuration is illustrated in Figure 6, and the corresponding transfer function in Figure 7. If the input signal ( $A_{IN+} - A_{IN-}$ ) swings negative, valid codes will be generated by the ADC and must be clamped by the user, if necessary.

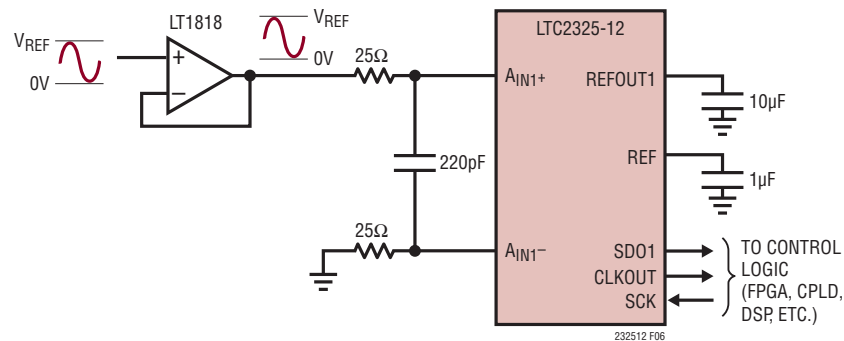


Figure 6. Pseudo-Differential Unipolar Application Circuit

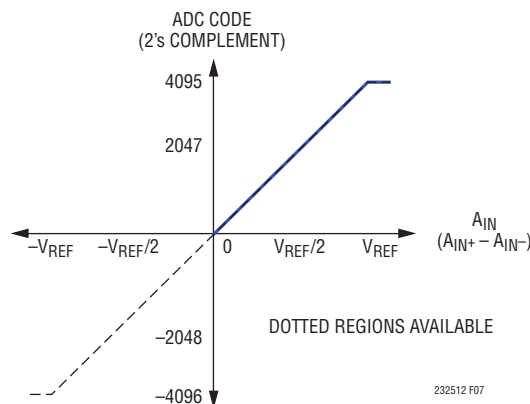


Figure 7. Pseudo-Differential Unipolar Transfer Function

## APPLICATIONS INFORMATION

### Single-Ended-to-Differential Conversion

While single-ended signals can be directly digitized as previously discussed, single-ended to differential conversion circuits may also be used when higher dynamic range is desired. By producing a differential signal at the inputs of the LTC2325-12, the signal swing presented to the ADC is maximized, thus increasing the achievable SNR.

The LT<sup>®</sup>1819 high speed dual operational amplifier is recommended for performing single-ended-to-differential conversions, as shown in Figure 8. In this case, the first amplifier is configured as a unity-gain buffer and the single-ended input signal directly drives the high impedance input of this amplifier.

### Fully-Differential Inputs

To achieve the best distortion performance of the LTC2325-12, we recommend driving a fully-differential signal through LT1819 amplifiers configured as two unity-gain buffers, as shown in Figure 9. This circuit achieves the full data sheet THD specification of  $-88\text{dB}$  at input frequencies up to  $500\text{kHz}$ . A fully-differential input

signal can span the maximum full-scale of the ADC, up to  $\pm\text{REFOUT}_{1,2,3,4}$ . The common mode input voltage can span the entire supply range up to  $V_{\text{DD}}$ , limited by the input signal swing. The fully-differential configuration is illustrated in Figure 10, with the corresponding transfer function illustrated in Figure 11.

### INPUT DRIVE CIRCUITS

A low impedance source can directly drive the high impedance inputs of the LTC2325-12 without gain error. A high impedance source should be buffered to minimize settling time during acquisition and to optimize the distortion performance of the ADC. Minimizing settling time is important even for DC inputs, because the ADC inputs draw a current spike when during acquisition.

For best performance, a buffer amplifier should be used to drive the analog inputs of the LTC2325-12. The amplifier provides low output impedance to minimize gain error and allows for fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the ADC inputs, which draw a small current spike during acquisition.

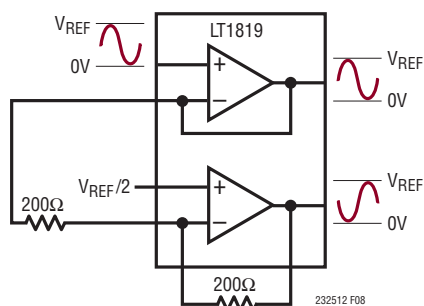


Figure 8. Single-Ended to Differential Driver

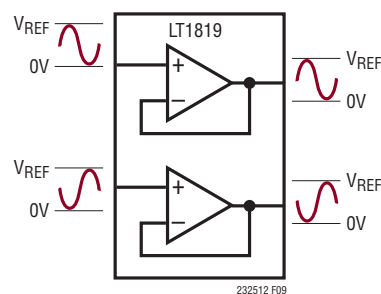


Figure 9. LT1819 Buffering a Fully-Differential Signal Source

## APPLICATIONS INFORMATION

### Input Filtering

The noise and distortion of the buffer amplifier and signal source must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier input with a low bandwidth filter to minimize noise. The simple 1-pole RC lowpass filter shown in Figure 12 is sufficient for many applications.

The sampling switch on-resistance ( $R_{ON}$ ) and the sample capacitor ( $C_{IN}$ ) form a second lowpass filter that limits

the input bandwidth to the ADC core to 110MHz. A buffer amplifier with a low noise density must be selected to minimize the degradation of the SNR over this bandwidth.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

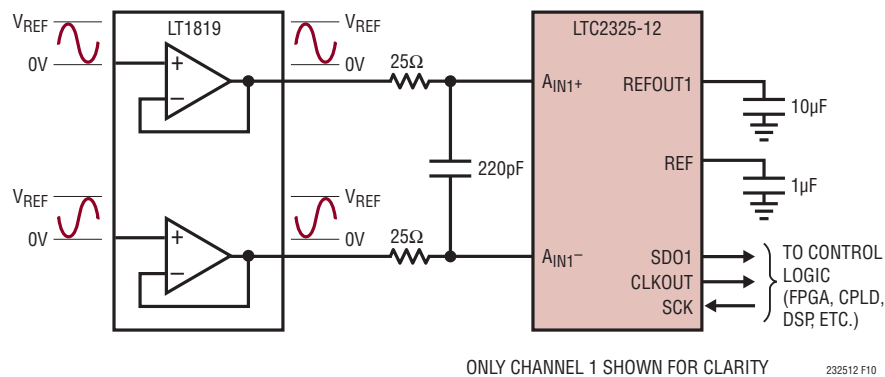


Figure 10. Fully-Differential Application Circuit

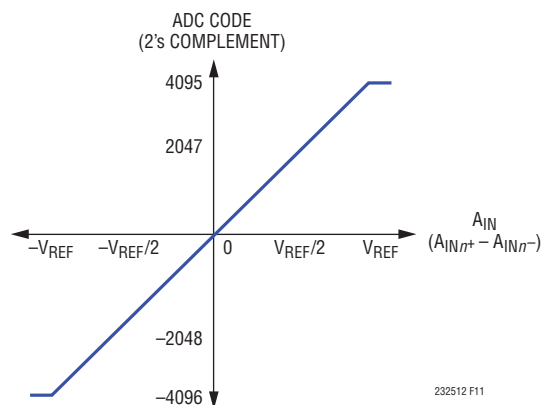


Figure 11. Fully-Differential Transfer Function

## APPLICATIONS INFORMATION

### ADC REFERENCE

#### Internal Reference

The LTC2325-12 has an on-chip, low noise, low drift (20ppm/°C max), temperature compensated band-gap reference. It is internally buffered and is available at REF (Pin 8). The reference buffer gains the internal reference voltage to 4.096V for supply voltages  $V_{DD} = 5V$  and to 2.048V for  $V_{DD} = 3.3V$ . The REF pin also drives

the four internal reference buffers with a current limited output (250 $\mu$ A) so it may be easily overdriven with an external reference in the range of 1.25V to 5V. Bypass REF to GND with a 1 $\mu$ F (X5R, 0805 size) ceramic capacitor to compensate the reference buffer and minimize noise. The 1 $\mu$ F capacitor should be as close as possible to the LTC2325-12 package to minimize wiring inductance. The voltage on the REF pin must be externally buffered if used for external circuitry.

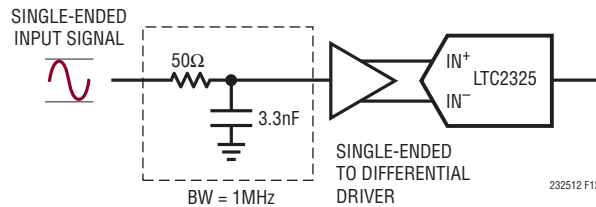


Figure 12. Input Signal Chain

Table 2. Reference Configurations and Ranges

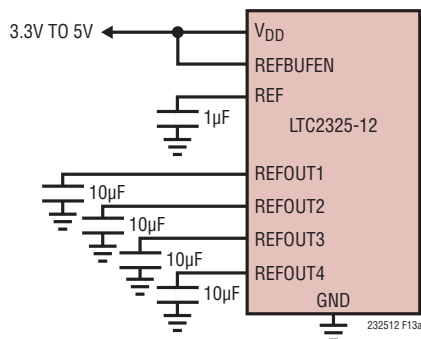
REFERENCE CONFIGURATION	$V_{DD}$	REFBUFEN	REF PIN	REFOUT1,2,3,4 PIN	DIFFERENTIAL INPUT RANGE
Internal Reference with Internal Buffers	5V	5V	4.096V	4.096V	$\pm 4.096V$
	3.3V	3.3V	2.048V	2.048V	$\pm 2.048V$
Common External Reference with Internal Buffer (REF Pin Externally Overdriven)	5V	5V	1.25V to 5V	1.25V to 3.3V	$\pm 1.25V$ to $\pm 5V$
	3.3V	3.3V	1.25V to 5V	1.25V to 3.3V	$\pm 1.25V$ to $\pm 3.3V$
External Reference with REF Buffers Disabled	5V	0V	4.096V	1.25V to 5V	$\pm 1.25V$ to $\pm 5V$
	3.3V	0V	2.048V	1.25V to 3.3V	$\pm 1.25V$ to $\pm 3.3V$

## APPLICATIONS INFORMATION

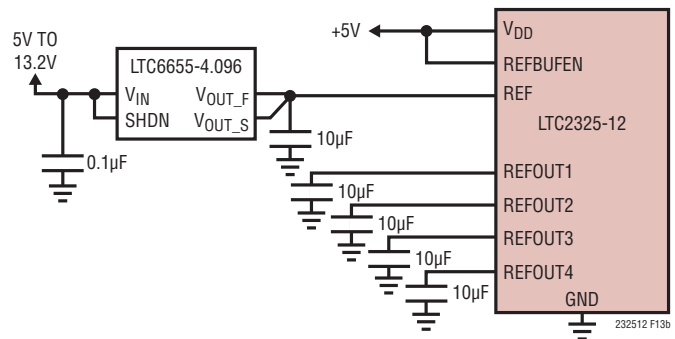
### External Reference

The internal REFOUT1,2,3,4 buffers can also be overdriven from 1.25V to 5V with an external reference at REFOUT1,2,3,4 as shown in Figure 13 (c). To do so, REFBUFEN must be grounded to disable the REF buffers. A 55k internal resistance loads the REFOUT1,2,3,4 pins when the REF buffers are disabled. To maximize the input signal swing and corresponding SNR, the LTC6655-5 is recommended when overdriving REFOUT. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a 10 $\mu$ F ceramic capacitor (X5R, 0805 size) close to each of the REFOUT1,2,3,4 pins. If the REF pin voltage is used as a REFOUT reference when REFBUFEN is connected to GND, it should be buffered externally.

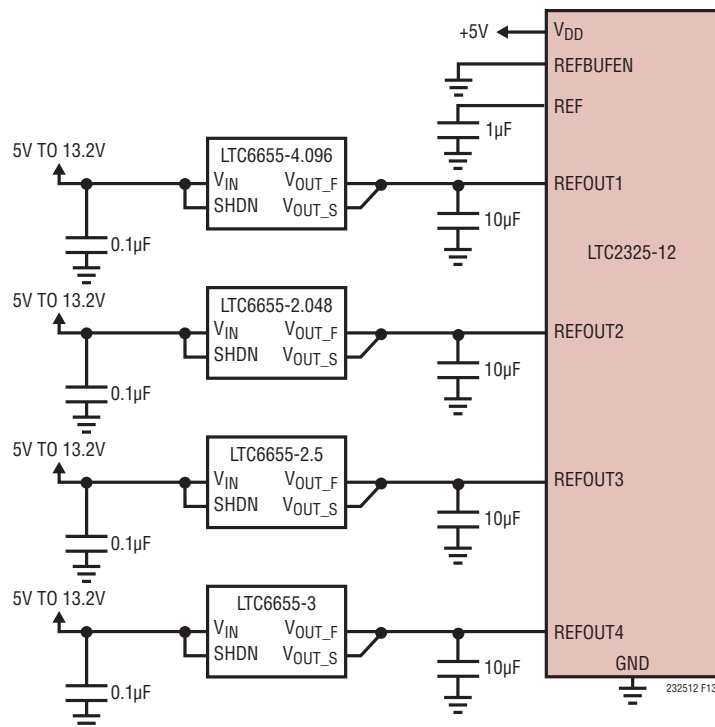
recommended when overdriving REFOUT. The LTC6655-5 offers the same small size, accuracy, drift and extended temperature range as the LTC6655-4.096. By using a 5V reference, a higher SNR can be achieved. We recommend bypassing the LTC6655-5 with a 10 $\mu$ F ceramic capacitor (X5R, 0805 size) close to each of the REFOUT1,2,3,4 pins. If the REF pin voltage is used as a REFOUT reference when REFBUFEN is connected to GND, it should be buffered externally.



(13a) LTC2325-12 Internal Reference Circuit



(13b) LTC2325-12 with a Shared External Reference Circuit



(13c) LTC2325-12 with Different External Reference Voltages

Figure 13. Reference Connections

## APPLICATIONS INFORMATION

### Internal Reference Buffer Transient Response

The REFOUT1,2,3,4 pins of the LTC2325-12 draw charge ( $Q_{\text{CONV}}$ ) from the external bypass capacitors during each conversion cycle. If the internal reference buffer is overdriven, the external reference must provide all of this charge with a DC current equivalent to  $I_{\text{REF}} = Q_{\text{CONV}}/t_{\text{CYC}}$ . Thus, the DC current draw of  $I_{\text{REFOUT1,2,3,4}}$  depends on the sampling rate and output code. In applications where a burst of samples is taken after idling for long periods, as shown in Figure 14,  $I_{\text{REFBUF}}$  quickly goes from approximately  $\sim 75\mu\text{A}$  to a maximum of  $500\mu\text{A}$  for  $\text{REFOUT} = 5\text{V}$  at  $5\text{Msps}$ . This step in DC current draw triggers a transient response in the external reference that must be considered since any deviation in the voltage at REFOUT will affect the accuracy of the output code. Due to the one-cycle conversion latency, the first conversion result at the beginning of a burst sampling period will be invalid. If an external reference is used to overdrive REFOUT1,2,3,4, the fast settling LTC6655 reference is recommended.

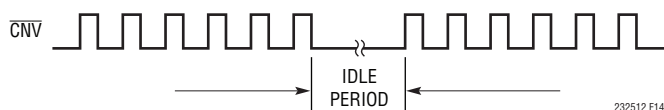


Figure 14.  $\overline{\text{CNV}}$  Waveform Showing Burst Sampling

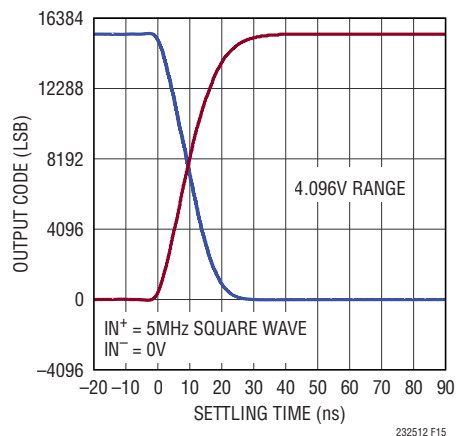


Figure 15. Transient Response of the LTC2325-12

### DYNAMIC PERFORMANCE

Fast Fourier transform (FFT) techniques are used to test the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using an FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. The LTC2325-12 provides guaranteed tested limits for both AC distortion and noise measurements.

### Signal-to-Noise and Distortion Ratio (SINAD)

The signal-to-noise and distortion ratio (SINAD) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the A/D output. The output is bandlimited to frequencies from above DC and below half the sampling frequency. Figure 16 shows that the LTC2325-12 achieves a typical SINAD of 76dB at a 5MHz sampling rate with a 2.2MHz input.

### Signal-to-Noise Ratio (SNR)

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components except the first five harmonics and DC. Figure 16 shows that the LTC2325-12 achieves a typical SNR of 77dB at a 5MHz sampling rate with a 2.2MHz input.

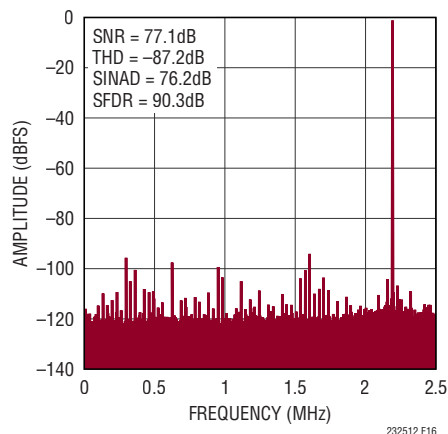


Figure 16. 32k Point FFT of the LTC2325-12

## APPLICATIONS INFORMATION

### Total Harmonic Distortion (THD)

Total harmonic distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half the sampling frequency ( $f_{\text{SAMPL}}/2$ ). THD is expressed as:

$$\text{THD} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_N^2}}{V_1}$$

where  $V_1$  is the RMS amplitude of the fundamental frequency and  $V_2$  through  $V_N$  are the amplitudes of the second through Nth harmonics.

### POWER CONSIDERATIONS

The LTC2325-12 requires two power supplies: the 3.3V to 5V power supply ( $V_{\text{DD}}$ ), and the digital input/output interface power supply ( $\text{OV}_{\text{DD}}$ ). The flexible  $\text{OV}_{\text{DD}}$  supply

allows the LTC2325-12 to communicate with any digital logic operating between 1.8V and 2.5V. When using LVDS I/O, the  $\text{OV}_{\text{DD}}$  supply must be set to 2.5V.

### Power Supply Sequencing

The LTC2325-12 does not have any specific power supply sequencing requirements. Care should be taken to adhere to the maximum voltage relationships described in the Absolute Maximum Ratings section. The LTC2325-12 has a power-on-reset (POR) circuit that will reset the LTC2325-12 at initial power-up or whenever the power supply voltage drops below 2V. Once the supply voltage re-enters the nominal supply voltage range, the POR will reinitialize the ADC. No conversions should be initiated until 10ms after a POR event to ensure the reinitialization period has ended. Any conversions initiated before this time will produce invalid results.

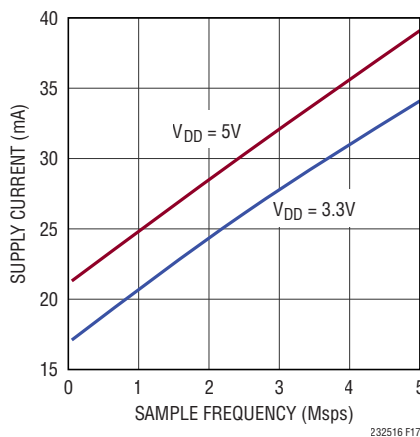


Figure 17. Power Supply Current of the LTC2325-12 Versus Sampling Rate

## APPLICATIONS INFORMATION

### TIMING AND CONTROL

#### $\overline{\text{CNV}}$ Timing

The LTC2325-12 sampling and conversion is controlled by  $\overline{\text{CNV}}$ . A rising edge on  $\overline{\text{CNV}}$  will start sampling and the falling edge starts the conversion and readout process. The conversion process is timed by the SCK input clock. For optimum performance,  $\overline{\text{CNV}}$  should be driven by a clean low jitter signal. The Typical Application at the back of the data sheet illustrates a recommended implementation to reduce the relatively large jitter from an FPGA  $\overline{\text{CNV}}$  pulse source. Note the low jitter input clock times the falling edge of the  $\overline{\text{CNV}}$  signal. The rising edge jitter of  $\overline{\text{CNV}}$  is much less critical to performance. The typical pulse width of the  $\overline{\text{CNV}}$  signal is 30ns with < 1.5ns rise and fall times at a 5Msps conversion rate.

#### SCK Serial Data Clock Input

In SDR mode ( $\overline{\text{SDR}}/\text{DDR}$  Pin 23 = GND), the falling edge of this clock shifts the conversion result MSB first onto the SDO pins. A 100MHz external clock must be applied at the SCK pin to achieve 5Msps throughput using all four SDO outputs. In DDR mode ( $\overline{\text{SDR}}/\text{DDR}$  Pin 23 =  $\text{OV}_{\text{DD}}$ ), each input edge of SCK shifts the conversion result MSB first onto the SDO pins. A 50MHz external clock must be applied at the SCK pin to achieve 5Msps throughput using all five SDO1 through SDO4 outputs.

#### CLKOUT Serial Data Clock Output

The CLKOUT output provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to

capture the SDO output eases timing requirements at the receiver. For low throughput speed applications, CLKOUT can be disabled by tying Pin 34 to  $\text{OV}_{\text{DD}}$ .

#### Nap/Sleep Modes

Nap mode is a method to save power without sacrificing power-up delays for subsequent conversions. Sleep mode has substantial power savings, but a power-up delay is incurred to allow the reference and power systems to become valid. To enter nap mode on the LTC2325-12, the SCK signal must be held high or low and a series of two  $\overline{\text{CNV}}$  pulses must be applied. This is the case for both CMOS and LVDS modes. The second rising edge of  $\overline{\text{CNV}}$  initiates the nap state. The nap state will persist until either a single rising edge of SCK is applied, or further  $\overline{\text{CNV}}$  pulses are applied. The SCK rising edge will put the LTC2325-12 back into the operational (full-power) state. When in nap mode, two additional pulses will put the LTC2325-12 in sleep mode. When configured for CMOS I/O operation, a single rising edge of SCK can return the LTC2325-12 into operational mode. A 10ms delay is necessary after exiting sleep mode to allow the reference buffer to recharge the external filter capacitor. In LVDS mode, exit sleep mode by supplying a fifth  $\overline{\text{CNV}}$  pulse. The fifth pulse will return the LTC2325-12 to operational mode, and further SCK pulses will keep the part from re-entering nap and sleep modes. The fifth SCK pulse also works in CMOS mode as a method to exit sleep. In the absence of SCK pulses, repetitive  $\overline{\text{CNV}}$  pulses will cycle the LTC2325-12 between operational, nap and sleep modes indefinitely.

Refer to the timing diagrams in Figure 18, Figure 19, Figure 20 and Figure 21 for more detailed timing information about sleep and nap modes.

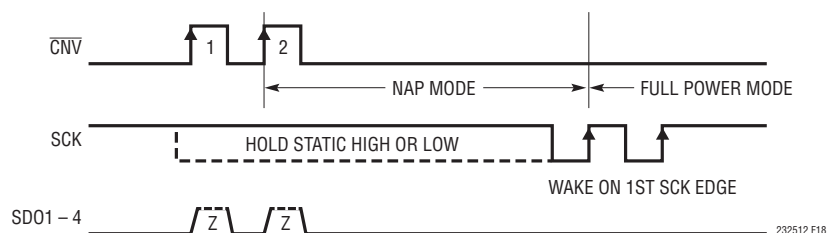


Figure 18. CMOS and LVDS Mode NAP and WAKE Using SCK

## APPLICATIONS INFORMATION

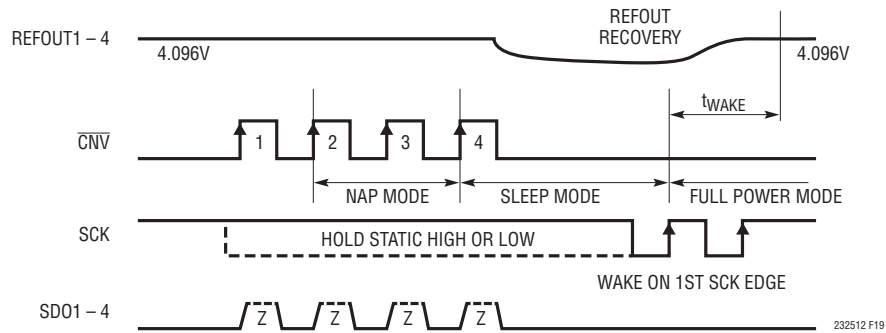


Figure 19. CMOS Mode SLEEP and WAKE Using SCK

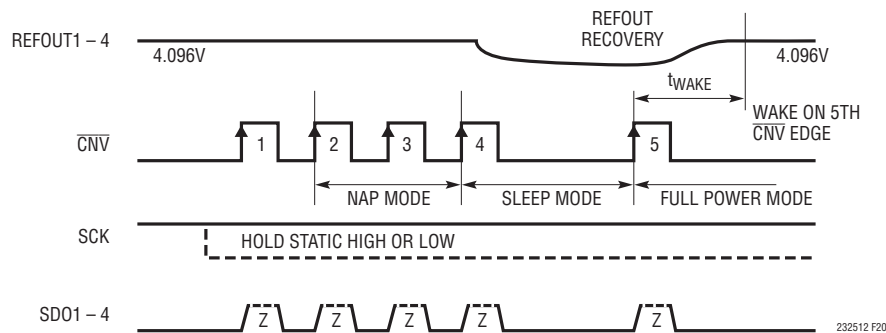
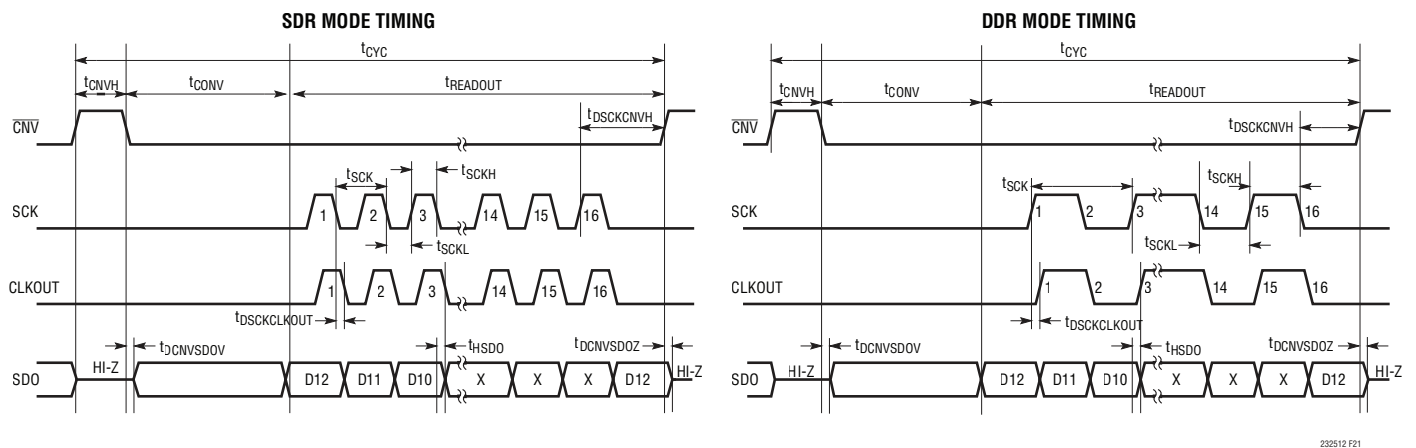
Figure 20. LVDS and CMOS Mode SLEEP and WAKE Using  $\overline{\text{CNV}}$ 

Figure 21. LTC2325-12 Timing Diagram

## APPLICATIONS INFORMATION

### DIGITAL INTERFACE

The LTC2325-12 features a serial digital interface that is simple and straightforward to use. The flexible  $OV_{DD}$  supply allows the LTC2325-12 to communicate with any digital logic operating between 1.8V and 2.5V. In addition to a standard CMOS SPI interface, the LTC2325-12 provides an optional LVDS SPI interface to support low noise digital design. The  $\overline{CMOS}/LVDS$  pin is used to select the digital interface mode. The SCK input clock shifts the conversion result MSB first on the SDO pins. CLKOUT provides a skew-matched clock to latch the SDO output at the receiver. The timing skew of the CLKOUT and SDO outputs are matched. For high throughput applications, using CLKOUT instead of SCK to capture the SDO output eases timing requirements at the receiver. In CMOS mode, use the SDO1 – SDO4, and CLKOUT pins as outputs. Use the SCK pin as an input. In LVDS mode, use the SDOA+ / SDOA- through SDOD+ / SDOD- and CLKOUT+ / CLKOUT- pins as differential outputs. Each LVDS lane yields one channel worth of data: SDOA yields CH1 data, SDOB yields CH2 data, SDOC yields CH3 data and SDOD yields CH4 data. These pins must be differentially terminated by an external 100 $\Omega$  resistor at the receiver (FPGA). The SCK+ / SCK- pins are differential inputs and must be terminated differentially by an external 100 $\Omega$  resistor at the receiver (ADC).

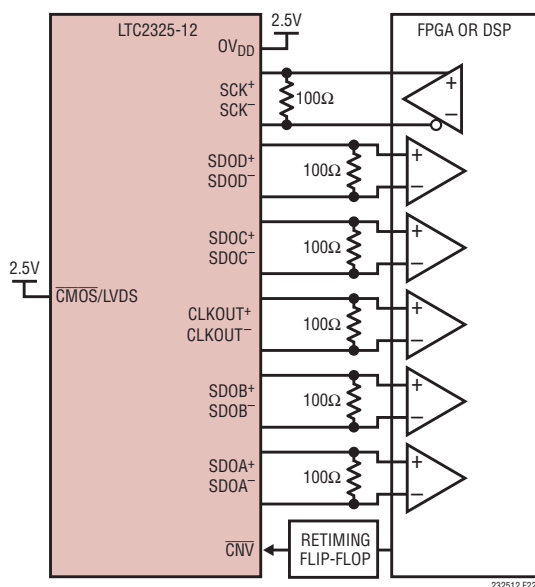


Figure 22. LTC2325-12 Using the LVDS Interface

### SDR/DDR Modes

The LTC2325-12 has an SDR (single data rate) and DDR (double data rate) mode for reading conversion data from the SDO pins. In both modes, CLKOUT is a delayed version of SCK. In SDR mode, each negative edge of SCK shifts the conversion data out the SDO pins. In DDR mode, each edge of the SCK input shifts the conversion data out. In DDR mode, the required SCK frequency is half of what is required in SDR mode. Tie  $\overline{SDR}/DDR$  to ground to configure for SDR mode and to  $OV_{DD}$  for DDR mode. The CLKOUT signal is a delayed version of the SCK input and is phase aligned with the SDO data. In SDR mode, the SDO transitions on the falling edge of CLKOUT as illustrated in Figure 21. We recommend using the rising edge of CLKOUT to latch the SDO data into the FPGA register in SDR mode. In DDR mode, the SDO transitions on each input edge of SCK. We recommend using the CLKOUT rising and falling edges to latch the SDO data into the FPGA registers in DDR mode. Since the CLKOUT and SDO data are phase aligned, we recommend digitally delaying the SDO data in the FPGA to provide adequate setup and hold timing margins in DDR mode.

### BOARD LAYOUT

To obtain the best performance from the LTC2325-12, a printed circuit board is recommended. Layout for the printed circuit board (PCB) should ensure the digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital clocks or signals adjacent to analog signals or underneath the ADC.

Supply bypass capacitors should be placed as close as possible to the supply pins. Low impedance common returns for these bypass capacitors are essential to the low noise operation of the ADC. A single solid ground plane is recommended for this purpose. When possible, screen the analog input traces using ground.

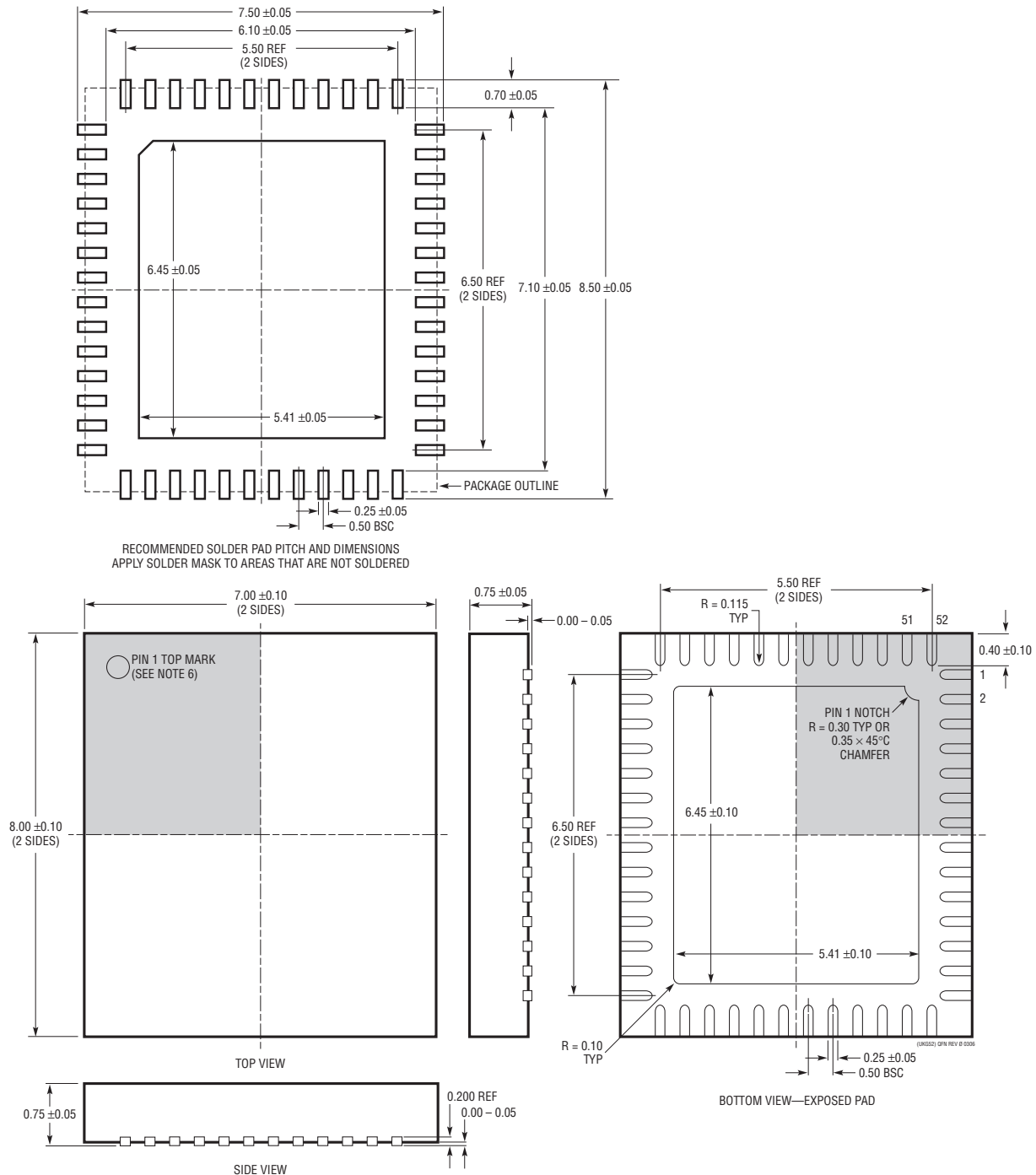
### Recommended Layout

For a detailed look at the reference design for this converter, including schematics and PCB layout, please refer to [DC2395A](#), the evaluation kit for the LTC2325-12.

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC2325-12#packaging> for the most recent package drawings.

**UKG Package**  
**52-Lead Plastic QFN (7mm × 8mm)**  
 (Reference LTC DWG # 05-08-1729 Rev 0)



**NOTE:**

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



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