Dual 14-Bit 170Msps ADC with JESD204B Serial Outputs

FEATURES

- **6.0Gbps JESD204B Interface**
- Only One Output Lane Required for Both ADCs ($F_S \leq 150$Msps)
- 70dBFS SNR
- 90dBFS SFDR
- Low Power: 751mW Total
- Single 1.8V Supply
- Easy to Drive $1.5V_{P-P}$ Input Range
- 1.25GHz Full Power Bandwidth S/H
- Optional Clock Divide by Two
- Optional Clock Duty Cycle Stabilizer
- Low Power Sleep and Nap Modes
- Serial SPI Port for Configuration
- 48-Lead (7mm × 7mm) QFN Package

APPLICATIONS

- Communications
- Cellular Base Stations
- Software Defined Radios
- Medical Imaging
- High Definition Video
- Test and Measurement Instrumentation

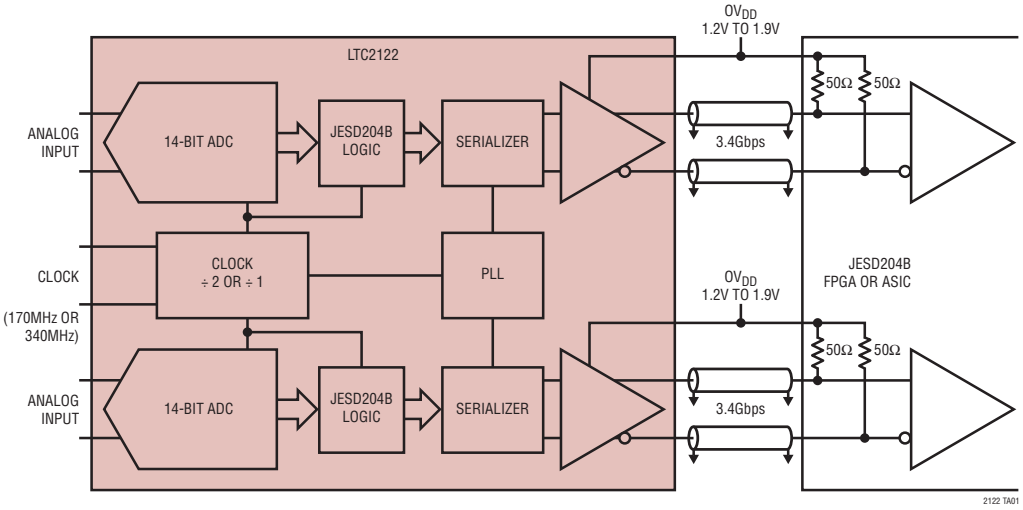
DESCRIPTION

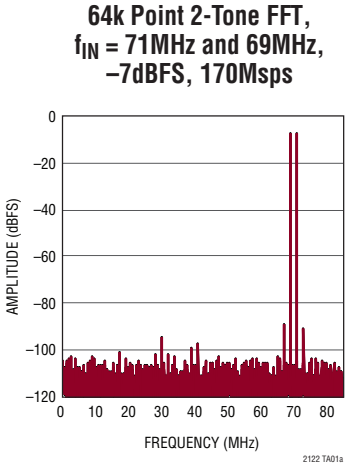
The LTC®2122 is a 2-channel simultaneous sampling 170Msps 14-bit A/D converter with serial JESD204B outputs. It is designed for digitizing high frequency, wide dynamic range signals. It is perfect for demanding communications applications with AC performance that includes 70dBFS SNR and 90dBFS spurious free dynamic range (SFDR). The 1.25GHz input bandwidth allows the ADC to under-sample high frequencies.

The JESD204B serial interface simplifies the PCB design by minimizing the number of data lines required. At 170Msps, only two 3.4Gbps output lanes are required. For sample rates up to 150Msps, both ADCs may share the same output lane at up to 6.0Gbps.

The DEVCLK$^+$ and DEVCLK$^-$ inputs can be driven differentially with sine wave, PECL, or LVDS signals. An optional clock divide-by-two circuit or clock duty cycle stabilizer maintains high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages

V_{DD}, OV_{DD} ..... 0.3V to 2V

Analog Input Voltage

$A_{INA/B}^+$, $A_{INA/B}^-$ ..... –0.3V to (V_{DD} + 0.2V)

SENSE (Note 3) ..... –0.3V to (V_{DD} + 0.2V)

Digital Input Voltage

DEVCLK+, DEVCLK–, SYSREF+, SYSREF–,

SYNC~+, SYNC~– (Note 3) ..... –0.3V to (V_{DD} + 0.3V)

$\overline{CS}$, SDI, SCK (Note 4) ..... –0.3V to 3.9V

SDO (Note 4) ..... –0.3V to 3.9V

Digital Output Voltage ..... –0.3V to (V_{DD} + 0.3V)

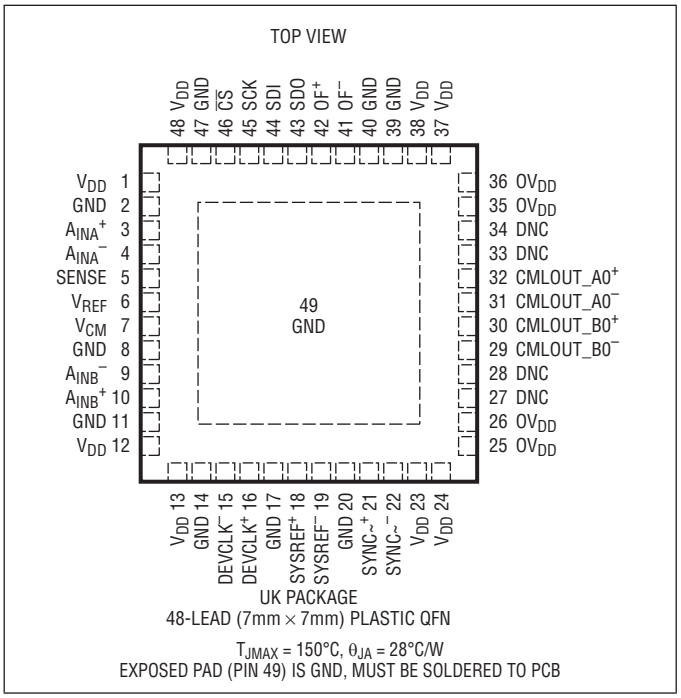
Operating Ambient Temperature Range

LTC2122C ..... 0°C to 70°C

LTC2122I ..... –40°C to 85°C

Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UK PACKAGE

48-LEAD (7mm × 7mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 28°C/W

EXPOSED PAD (PIN 49) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2122CUK#PBF	LTC2122CUK#TRPBF	LTC2122UK	48-Lead (7mm × 7mm) Plastic QFN	0°C to 70°C
LTC2122IUK#PBF	LTC2122IUK#TRPBF	LTC2122UK	48-Lead (7mm × 7mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)		●	14			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–5.1	±1.2	5.1	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.35	0.9	LSB
Offset Error	(Note 7)	●	–13	±5	13	mV
Gain Error	Internal Reference External Reference	 ●	 –4.0	±1.5 ±1	 2.2	%FS %FS
Offset Drift				±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±30 ±10		ppm/°C ppm/°C
Transition Noise				1.82		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	1.7V < V_{DD} < 1.9V	●		1.5		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input (Note 8)	●	V_{CM} – 20mV	V_{CM}	V_{CM} + 20mV	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	1.2	1.250	1.3	V
I_{IN1}	Analog Input Leakage Current	0 < A_{IN}^+, A_{IN}^- < V_{DD}, No Clock	●	–1		1	µA
I_{IN2}	SENSE Input Leakage Current	1.2V < SENSE < 1.3V	●	–1		1	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				1		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.15		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				75		dB
BW–3dB	Full-Power Bandwidth				1250		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SNR	Signal-to-Noise Ratio	15MHz Input 70MHz Input 140MHz Input	 ●	 67.7	70 69.8 69.1	 	dBFS dBFS dBFS
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	15MHz Input 70MHz Input 140MHz Input	 ●	 76	90 85 80	 	dBFS dBFS dBFS
	Spurious Free Dynamic Range 4th Harmonic or Higher	15MHz Input 70MHz Input 140MHz Input	 ●	 83	95 95 85	 	dBFS dBFS dBFS
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	15MHz Input 70MHz Input 140MHz Input	 ●	 67.3	69.9 69.4 68.5	 	dBFS dBFS dBFS
Crosstalk	Crosstalk Between Channels	Up to 250MHz Input			–90		dB

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0		0.435 • V_{DD} – 18mV	0.435 • V_{DD}	0.435 • V_{DD} + 18mV	V
V_{CM} Output Temperature Drift				±37		ppm/°C
V_{CM} Output Resistance	–1mA < I_{OUT} < 1mA			4		Ω
V_{REF} Output Voltage	I_{OUT} = 0		1.225	1.250	1.275	V
V_{REF} Output Temperature Drift				±30		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA			7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V			0.6		mV/V

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Analog Supply Voltage	Single-Lane Operation Two-Lane Operation	● ●	1.8 1.7	1.85 1.8	1.9 1.9	V V
OV_{DD}	Output Supply Voltage	CML Current = 16mA, Directly Terminated (Note 8) CML Current = 16mA, AC Terminated	● ●	1.2 1.4		1.9 1.9	V V
I_{VDD}	Analog Supply Current		●		417	459	mA
I_{OVDD}	Output Supply Current Per Lane	CML Current = 12mA	●	11	12	13.8	mA
P_{DISS}	Power Dissipation	V_{DD} = 1.8V, Excluding OV_{DD} Power	●		751	826	mW
P_{SLEEP}	Sleep Mode Power				2		mW
P_{NAP}	Nap Mode Power				433		mW

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLOCK INPUTS (DEVCLK⁺, DEVCLK⁻)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2	 1.5	V V
R_{IN}	Input Resistance	(See Figure 2)			10		kΩ
C_{IN}	Input Capacitance				2		pF
Differential Digital Inputs (SYNC~⁺, SYNC~⁻, SYSREF⁺, SYSREF⁻)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2	 1.5	V V
R_{IN}	Input Resistance				6.7		kΩ
C_{IN}	Input Capacitance				2		pF

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 8)			3		pF
SDO OUTPUT (Open-Drain Output. Requires 2k Pull-Up Resistor if SDO Is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance	(Note 8)			4		pF
LVDS OUTPUTS (OF^+, OF^-)							
V_{OD}	Differential Output Voltage	100Ω Differential Load	●	247	350	454	mV
V_{OS}	Common Mode Output Voltage		●	1.125	1.25	1.375	V
CML Outputs							
V_{DIFF}	CML Differential Output Voltage	Output Current Set to 10mA Output Current Set to 12mA Output Current Set to 14mA Output Current Set to 16mA			500 600 700 800		mVppd mVppd mVppd mVppd
V_{OH}	Output High Level	Directly-Coupled 50Ω to OV_{DD} Directly-Coupled 100Ω Differential AC-Coupled			OV_{DD} OV_{DD}-1/4 V_{DIFF} OV_{DD}-1/4 V_{DIFF}		V V V
V_{OL}	Output Low Level	Directly-Coupled 50Ω to OV_{DD} Directly-Coupled 100Ω Differential AC-Coupled			OV_{DD}-1/2 V_{DIFF} OV_{DD}-3/4 V_{DIFF} OV_{DD}-3/4 V_{DIFF}		V V V
V_{OCM}	Output Common Mode Level	Directly-Coupled 50Ω to OV_{DD} Directly-Coupled 100Ω Differential AC-Coupled			OV_{DD}-1/4 V_{DIFF} OV_{DD}-1/2 V_{DIFF} OV_{DD}-1/2 V_{DIFF}		V V V
R_{OUT}	Output Resistance	Single-Ended Differential	 ●	 80	50 100	 120	Ω Ω

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_S, $1/t_S$	Sampling Frequency	(Note 9)	●	50		170	MHz
t_L	1× CLK Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	2.79 1.5	2.94 2.94	10 10	ns ns
t_H	1× CLK High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	2.79 1.5	2.94 2.94	10 10	ns ns
t_{DCK}	DEVCLK Period	2X_CLK SPI Register = 0 2X_CLK SPI Register = 1	● ●	5.88 2.94		20 10	ns ns
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Readback Mode C_{SDO} = 20pF, R_{PULLUP} = 2kΩ	● ●	40 250			ns ns
t_{CSS}	$\overline{CS}$ Falling to SCK Rising Set Up Time		●	5			ns
t_{SCH}	SCK Rising to $\overline{CS}$ Rising Hold Time		●	5			ns
t_{SCS}	SCK Falling to $\overline{CS}$ Falling Set Up Time		●	5			ns

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{DS}	SDI to SCK Rising Set Up Time		●	5			ns
t_{DH}	SCK Rising to SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode C_{SDO} = 20pF, R_{PULLUP} = 2kΩ	●			125	ns
JESD204B Timing (Note 8)							
$t_{BIT, UI}$	High Speed Serial Bit Period	1 Lane Mode (2 ADC to One Lane) 2 Lane Mode (1 Lane Per ADC)	● ●	167 294		1000 1000	ps ps
t_{JIT}	Total Jitter of CML Outputs (P-P)	> 3.125Gbps Per Lane (BER = 1E-15, Note 8) ≤ 3.125Gbps Per Lane (BER = 1E-12, Note 8)	● ●			0.3 0.35	UI UI
t_{SU_SYN}	SYNC~ to CLK Set-Up Time	(Note 8)	●	0.6			ns
t_{H_SYN}	DEVCLK to SYNC~ Hold Time	(Note 8)	●	0.6			ns
t_{SU_SYS}	SYSREF to DEVCLK Set-Up Time	(Note 8)	●	0.2		(t_{DCK} – 0.32)	ns
t_{H_SYS}	DEVCLK to SYSREF Hold Time	(Note 8)	●	0.32			ns
LAT_{P1}	Pipeline Latency, Single-Lane Mode	(Note 10)	●	10.5		10.5	t_S
LAT_{P2}	Pipeline Latency, 2-Lane Mode	(Note 10)	●	13.5		13.5	t_S
t_{DS}	Delay from DEVCLK to Serial Data Out	(Note 8)	●			0.6	t_S
LAT_{SC1}	Latency from SYNC~ Assertion to COMMA Out, Single Lane Mode	(Note 10)	●	7		7	t_S
LAT_{SC2}	Latency from SYNC~ Assertion to COMMA Out, 2-Lane Mode	(Note 10)	●	10		10	t_S
LAT_{SL1}	Latency from SYNC~ De-assertion to LAS Out, Single-Lane Mode	(Note 10, 11)	●	3		3	t_S
LAT_{SL2}	Latency from SYNC~ De-assertion to LAS Out, 2-Lane Mode	(Note 10, 11)	●	6		6	t_S
LAT_{OF}	Overflow Latency	(Note 10)	●	6		6	t_S
t_{D_OF1X}	Analog Delay of OF with 1X_CLK	(Note 8)	●	1.4	1.7	2.0	ns
t_{D_OF2X}	Analog Delay of OF with 2X_CLK	(Note 8)	●	1.6	1.9	2.2	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = 1.8V, f_{SAMPLE} = 170MHz, differential DEVCLK+/DEVCLK– = $2V_{P-P}$ sine wave, input range = $1.5V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5LSB when the output code flickers between 01 1111 1111 1111 and 10 0000 0000 0000.

Note 8: Guaranteed by design, not subject to test.

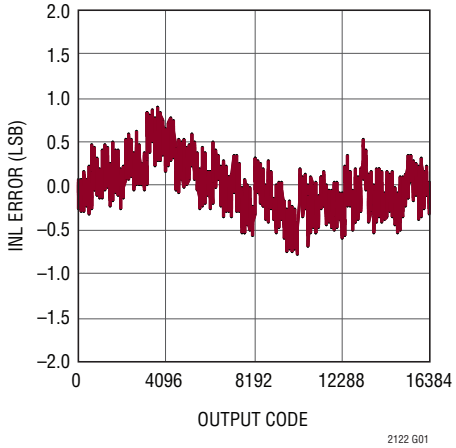
Note 9: Recommended operating conditions.

Note 10: When the "2×_CLK" SPI register bit is set, the DEVCLK frequency is 2× the sampling frequency. When the "2×_CLK" bit is not set, the DEVCLK frequency is equal to the sampling frequency. Latency is measured in units of sampling periods (t_S), where t_S is the inverse of the sampling frequency.

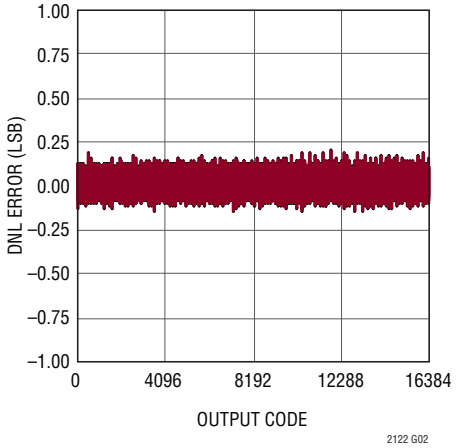
Note 11: When in subclass 0, the Lane Alignment Sequence (LAS) latency measurement begins at the start of the frame following the detection of SYNC~ de-assertion. When in subclasses 1 or 2 this LAS latency measurement begins at the start of the first multiframe following the detection of SYNC~ de-assertion.

TYPICAL PERFORMANCE CHARACTERISTICS

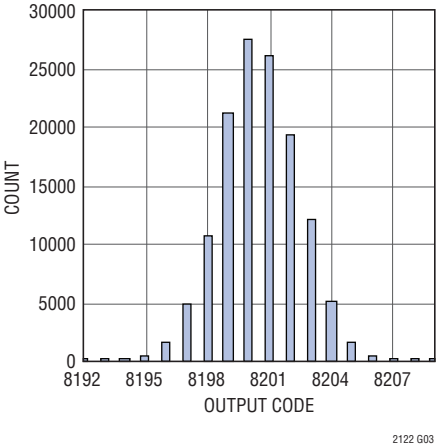
Integral Nonlinearity (INL)



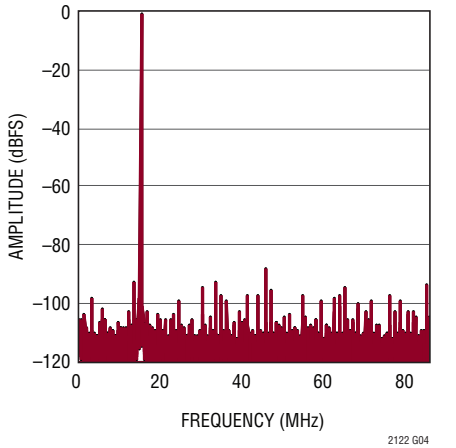
Differential Nonlinearity (DNL)



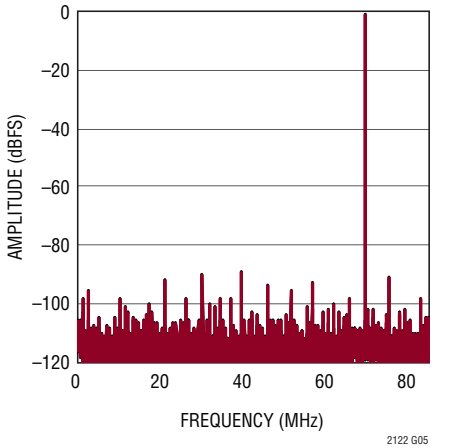
AC Grounded Input Histogram



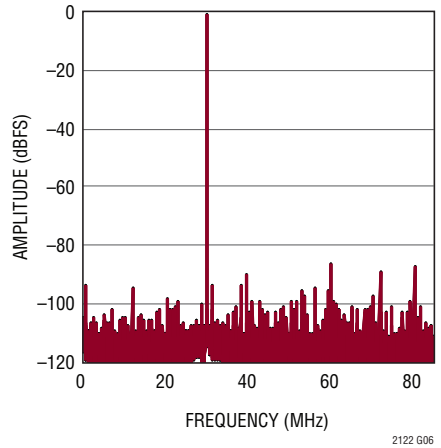
64k Point FFT, f_{IN} = 15.0MHz, –1dBFS, 170Msps



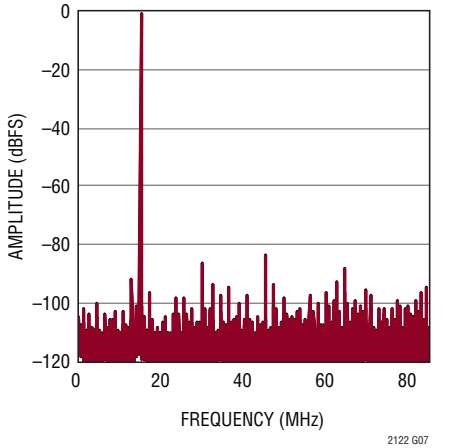
64k Point FFT, f_{IN} = 69.8MHz, –1dBFS, 170Msps



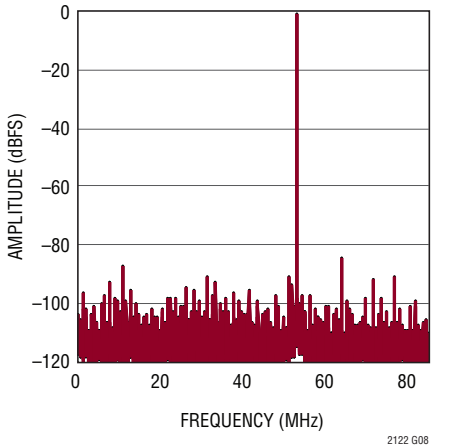
64k Point FFT, f_{IN} = 140.0MHz, –1dBFS, 170Msps



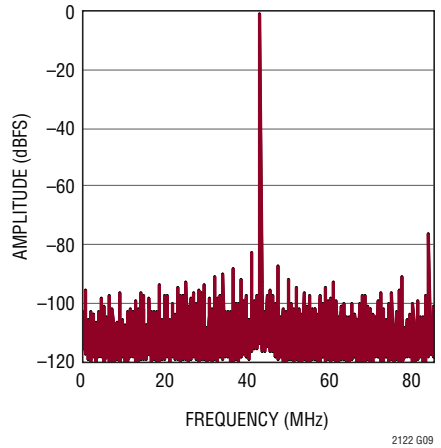
64k Point FFT, f_{IN} = 185.1MHz, –1dBFS, 170Msps



64k Point FFT, f_{IN} = 223.1MHz, –1dBFS, 170Msps

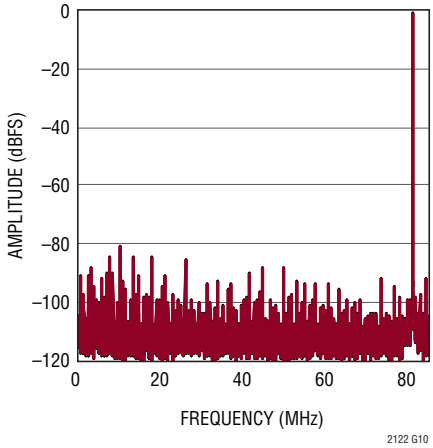


64k Point FFT, f_{IN} = 383.1MHz, –1dBFS, 170Msps

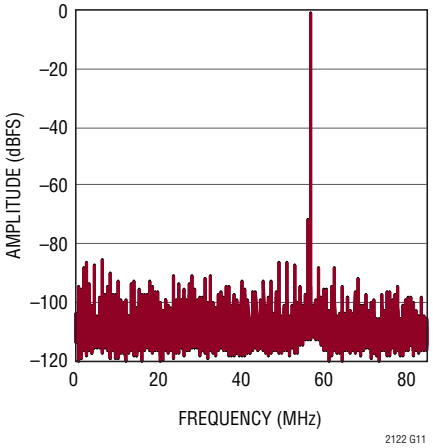


TYPICAL PERFORMANCE CHARACTERISTICS

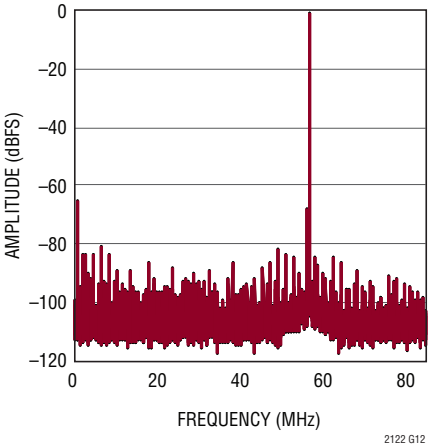
64k Point FFT, f_{IN} = 421.1MHz, –1dBFS, 170Msps



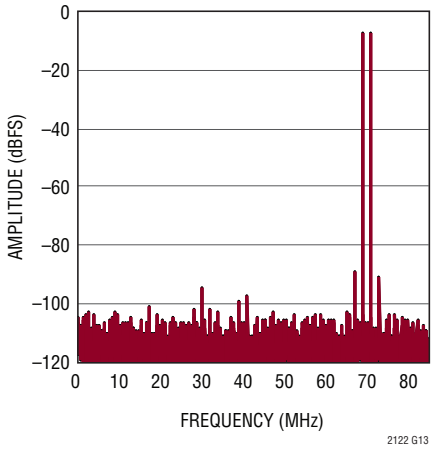
64k Point FFT, f_{IN} = 567.0MHz, –1dBFS, 170Msps



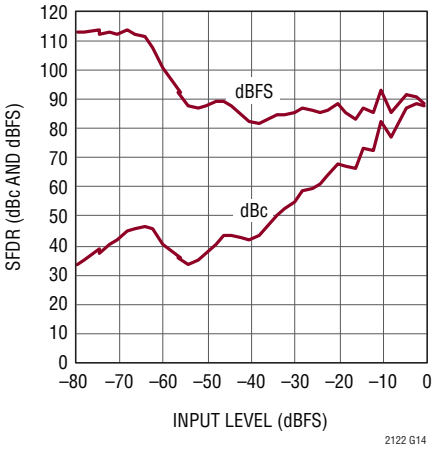
64k Point FFT, f_{IN} = 907.0MHz –1dBFS, 170Msps



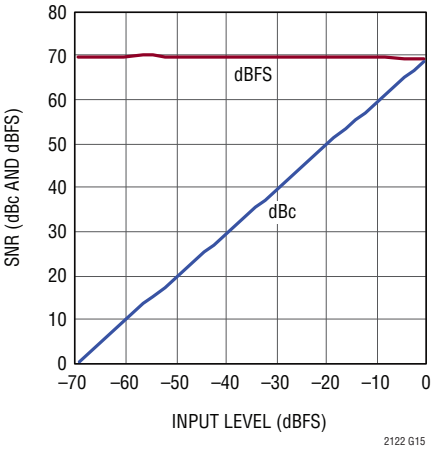
64k Point 2-Tone FFT, f_{IN} = 71MHz and 69MHz, –7dBFS, 170Msps



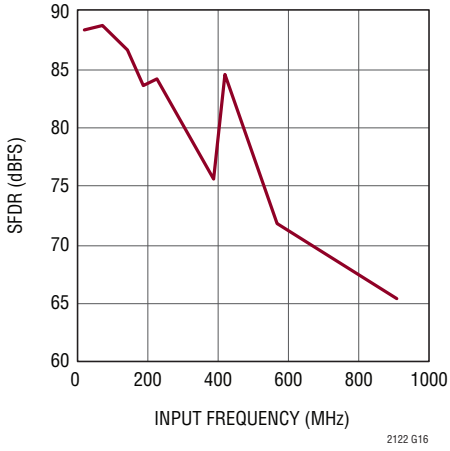
SFDR vs Input Level, f_{IN} = 70MHz, 1.5V Range, 170Msps



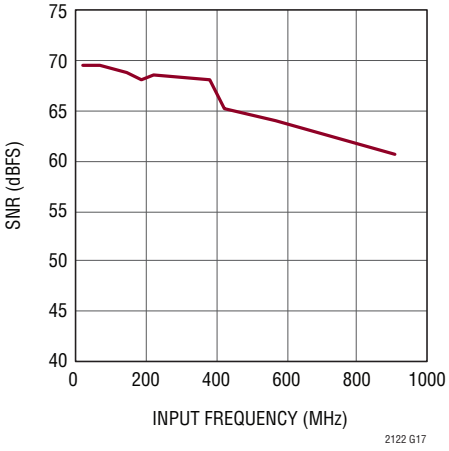
SNR vs Input Level, f_{IN} = 70MHz, 1.5V Range, 170Msps



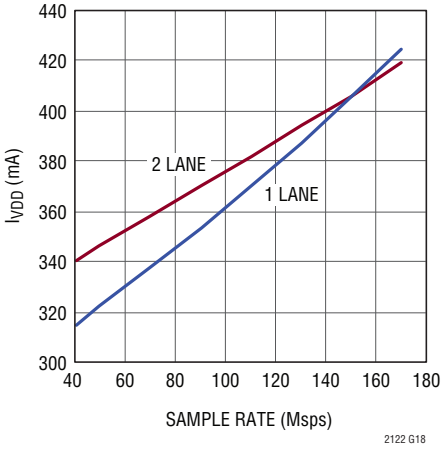
SFDR vs Input Frequency, –1dBFS, 1.5V Range, 170Msps



SNR vs Input Frequency, –1dBFS, 1.5V Range, 170Msps

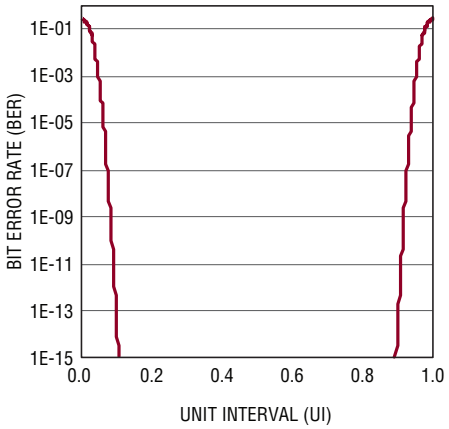


I_{VDD} vs Sample Rate, f_{IN} = 15MHz, –1dBFS



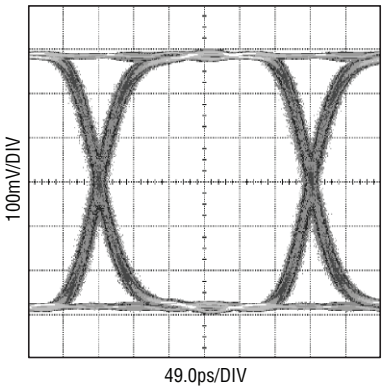
TYPICAL PERFORMANCE CHARACTERISTICS

CMLOUT Bathtub Curve, 3.4Gbps



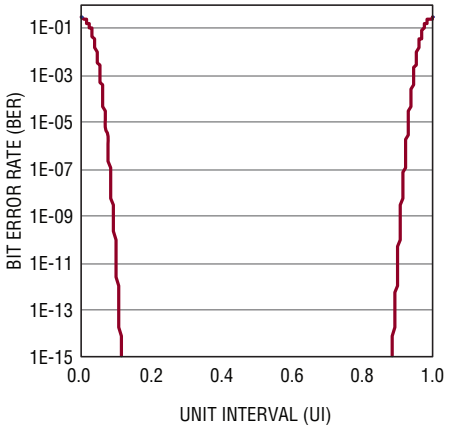
2122 G19

CMLOUT Eye Diagram, 3.4Gbps



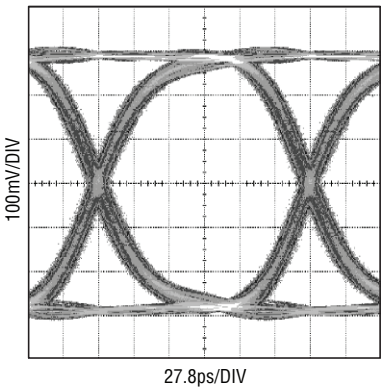
2122 G20

CMLOUT Bathtub Curve, 6.0Gbps



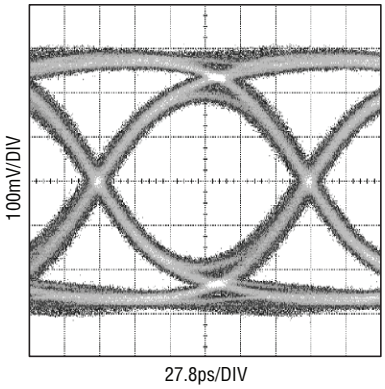
2122 G21

CMLOUT Eye Diagram, 6.0Gbps Single Lane



2122 G22

CMLOUT Eye Diagram, 6.0Gbps, Single Lane, 8in (20cm) FR4



2122 G23

PIN FUNCTIONS

V_{DD} (Pins 1, 12, 13, 23, 24, 37, 38, 48): 1.8V Power Supply. Bypass to ground with 0.1µF ceramic capacitors. Adjacent pins can share bypass capacitor.

GND (Pins 2, 8, 11, 14, 17, 20, 39, 40, 47, Exposed Pad Pin 49): Device Power Ground. The exposed pad must be soldered to the PCB ground.

A_{INA}^+/A_{INA}^- (Pins 3, 4): Analog Input Pair for Channel A.

SENSE (Pin 5): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±0.75V input range. An external reference between 1.2V and 1.3V applied to SENSE selects an input range of $\pm 0.6 \times V_{SENSE}$.

V_{REF} (Pin 6): Reference Voltage Output. Bypass to ground with a 2.2µF ceramic capacitor. Nominally 1.25V.

V_{CM} (Pin 7): Common Mode Bias Output. Nominally equal to $0.435 \bullet V_{DD}$. V_{CM} should be used to bias the common mode of the analog inputs. Bypass to ground with a 0.1µF ceramic capacitor.

A_{INB}^-/A_{INB}^+ (Pins 9, 10): Analog Input Pair for Channel B.

$DEVCLK^-/DEVCLK^+$ (Pins 15, 16): Device Clock Input Pair. The sample clock is derived from this differential signal. An internal DEVCLK divider may be programmed through the SPI to either divide by one or two ($DEVCLK = DEVCLK^+ – DEVCLK^-$).

In divide-by-one mode, the analog signal is sampled on the falling edge of DEVCLK.

In divide-by-two mode, the analog signal is sampled once every two DEVCLK cycles on the rising edge of DEVCLK. The actual sampling cycle is established at the time of the clock divider initialization. In subclass 1, a low-to-high transition of the SYSREF signal will initialize the divide-by-two circuit on the first rising edge of DEVCLK. In subclass 2, a low to high transition of the SYNC~ signal will initialize the divide-by-two circuit on the first rising edge of DEVCLK.

$SYSREF^+/SYSREF^-$ (Pins 18, 19): A JESD204B Subclass 1 Input Signal Pair. A low to high transition of SYSREF is sampled on the rising edge of DEVCLK to reset the internal dividers and set up deterministic latency ($SYSREF = SYSREF^+ – SYSREF^-$).

$SYNC\sim^+/SYNC\sim^-$ (Pins 21, 22): A JESD204B Synchronization Input Signal Pair. Used to establish initial Code-Group synchronization for all three subclasses. A low level of the SYNC~ signal causes the LTC2122 to output K28.5 commas ($SYNC\sim = SYNC\sim^+ – SYNC\sim^-$).

In subclass 2 a low to high transition of SYNC~ is sampled on the rising edge of DEVCLK to reset the internal dividers and set up deterministic latency.

OV_{DD} (Pins 25, 26, 35, 36): 1.2V to 1.9V Output Driver Supply. Bypass each pair to ground with 0.1µF ceramic capacitors.

$CMLOUT\_B0^-/CMLOUT\_B0^+$ (Pins 29, 30): Current Mode Logic Output Pair for Channel B in two lane mode. Must be terminated with a 50Ω resistor to OV_{DD}, a differential 100Ω resistor to the complementary output, or AC coupled to another termination voltage.

$CMLOUT\_A0^-/CMLOUT\_A0^+$ (Pins 31, 32): Current Mode Logic Output Pair for Channel A in two lane mode or for both Channel A and Channel B in one lane mode. Must be terminated with a 50Ω resistor to OV_{DD}, a differential 100Ω resistor to the complementary output, or AC coupled to another termination voltage.

OF^-/OF^+ (Pins 41, 42): Over/Underflow LVDS Digital Output. OF is high when an overflow or underflow has occurred. The overflows for channel A and channel B are multiplexed together and transmitted at twice the sample frequency ($OF = OF^+ – OF^-$).

SDO (Pin 43): Serial Interface Data Output. SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain N-channel MOSFET output that requires an external 2k pull-up resistor from 1.8V to 3.3V. If readback from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected.

SDI (Pin 44): Serial Interface Data Input. SDI is the serial interface data input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. SDI can be driven with 1.8V to 3.3V logic.

SCK (Pin 45): Serial Interface Clock Input. SCK is the serial interface clock input. SCK can be driven with 1.8V to 3.3V logic.

$\overline{CS}$ (Pin 46): Serial Interface Chip Select Input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. SCK must be low at the time of the falling edge of $\overline{CS}$, for proper operation. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

BLOCK DIAGRAM

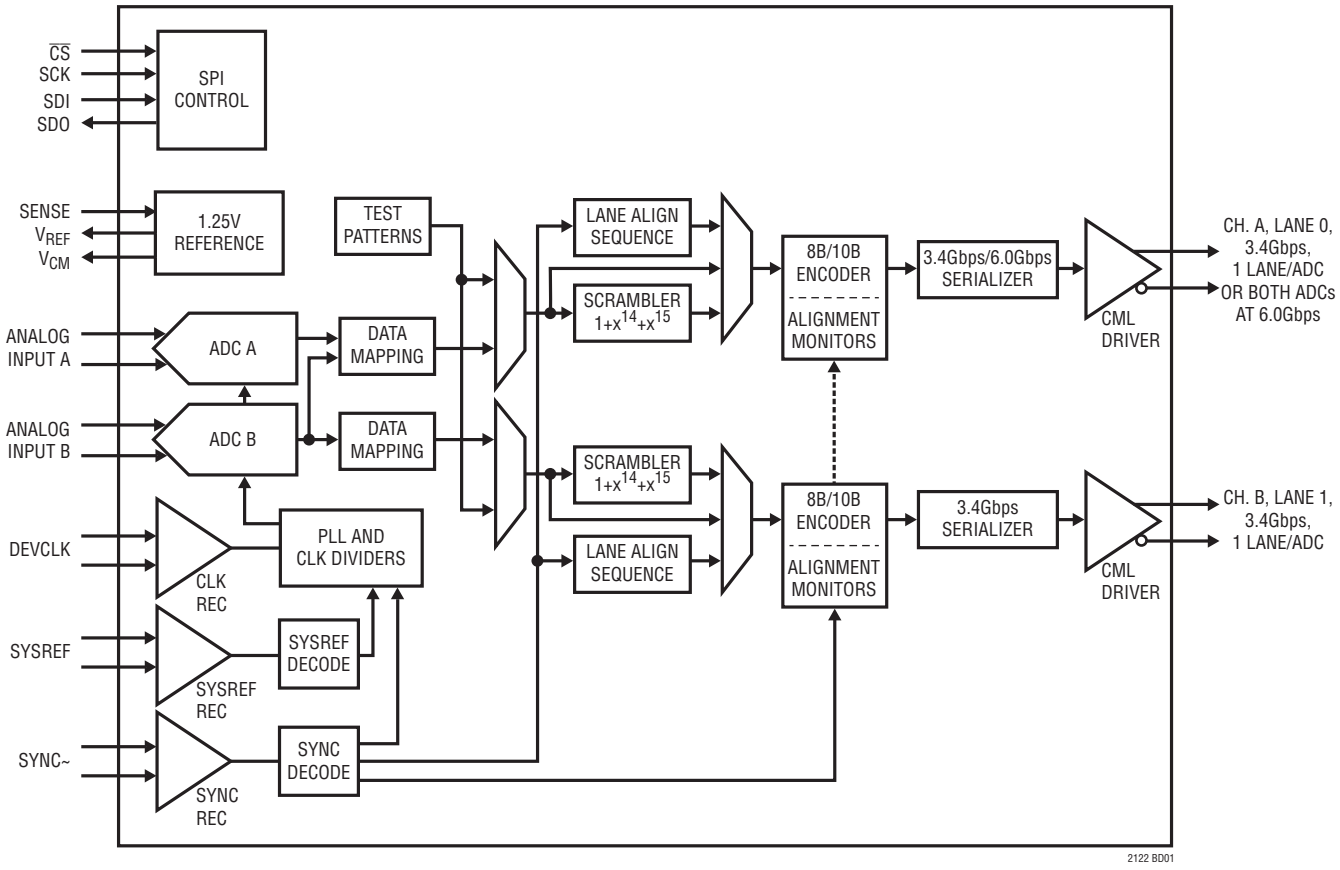
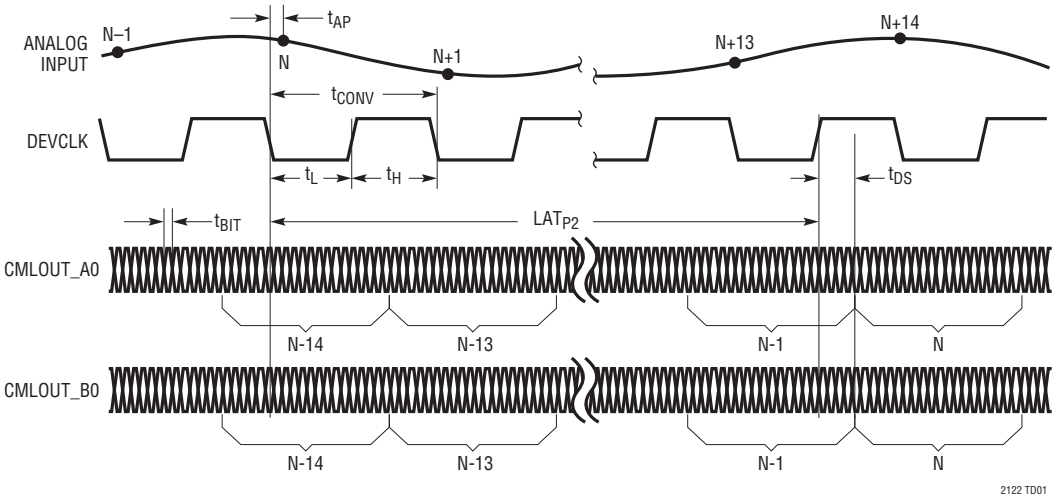
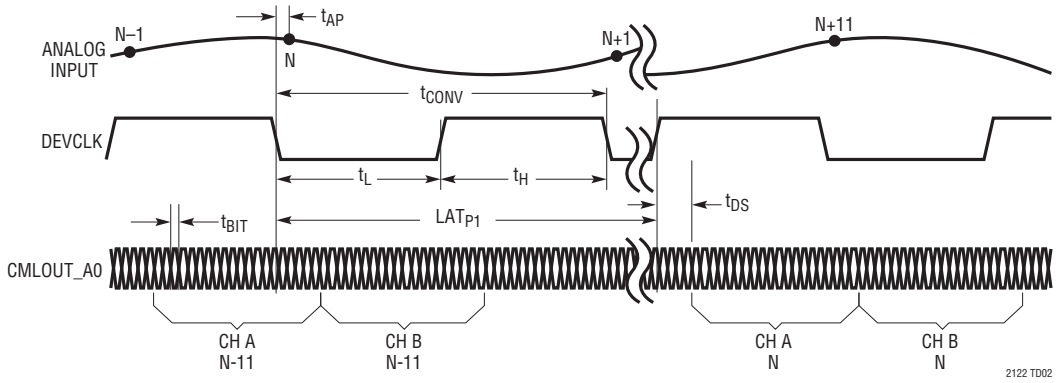


Figure 1. Functional Block Diagram

TIMING DIAGRAM

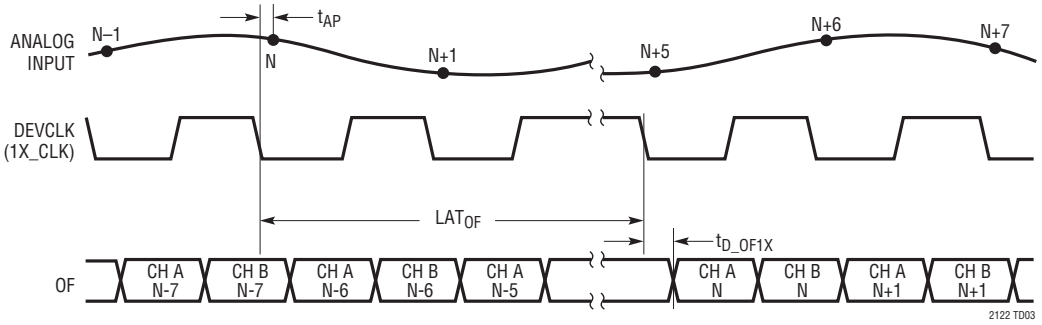


Two-Lane Timing (One Lane Per ADC), $f_{DEVCLK} = f_S$

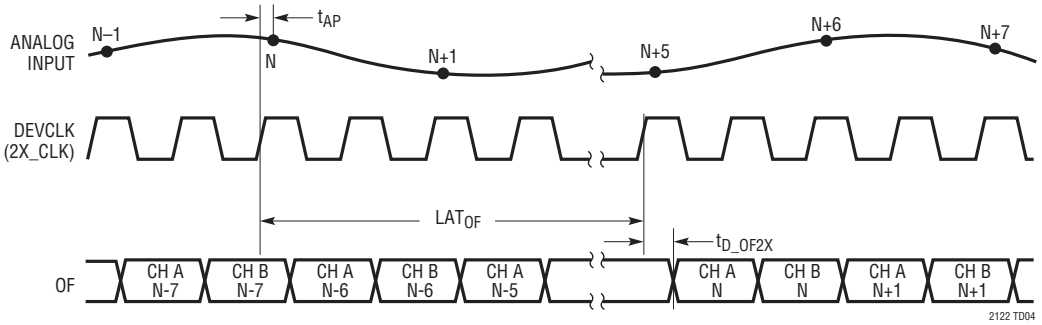


One-Lane Timing (Two ADCs On One Lane), $f_{DEVCLK} = f_S$

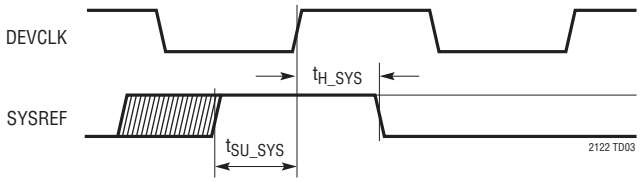
TIMING DIAGRAM



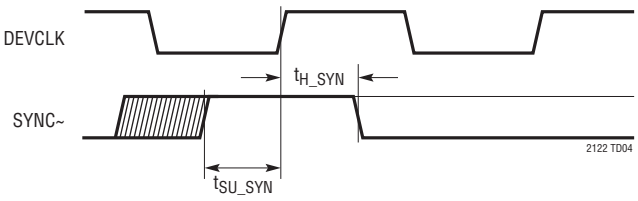
Over Flow (OF) Timing, 1X_CLK Mode



Over-Flow (OF) Timing 2X_CLK Mode



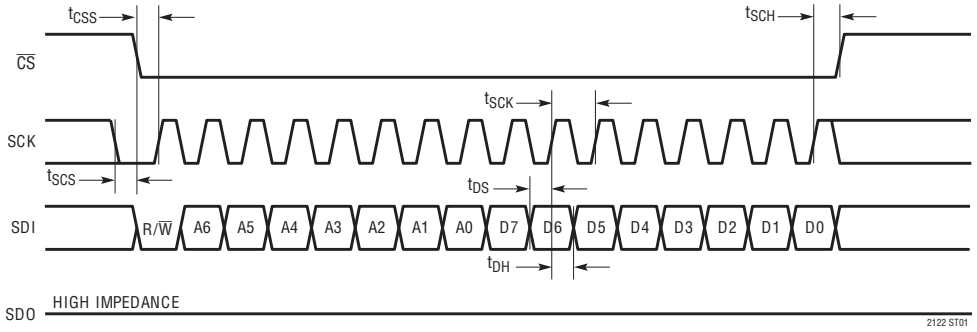
SYSREF Timing (Subclass 1)



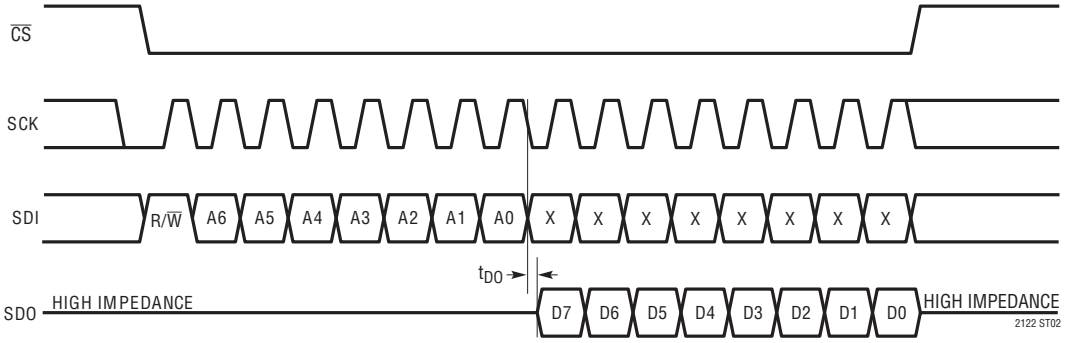
SYNC~ Rising Edge Clock Reset Timing (Subclass 2)

NOTE: DEVCLK = DEVCLK$^+$ – DEVCLK$^-$,
SYSREF = SYSREF$^+$ – SYSREF$^-$,
SYNC~ = SYNC~$^+$ – SYNC~$^-$,

SPI TIMING



SPI Timing, Write Mode



SPI Timing, Read Mode

DEFINITIONS

ADC PERFORMANCE TERMS

Aperture Delay Time

The time it takes for the input signal to be held by the sample-and-hold circuit after the sampling edge of DEVCLK (DEVCLK = DEVCLK$^+$ - DEVCLK$^-$). The delay measurement starts at the instant the differential DEVCLK signals cross each other.

In divide-by-one mode, the analog signal is sampled on the falling edge of DEVCLK.

In divide-by-two mode, the analog signal is sampled once every two DEVCLK cycles on the rising edge of DEVCLK. The actual sampling cycle is established at the time of the clock divider initialization. In subclass 1, a low to high transition of the SYSREF signal will initialize the divide-by-two circuit on the first rising edge of DEVCLK. In subclass 2, a low to high transition of the SYNC~ signal will initialize the divide-by-two circuit on the first rising edge of DEVCLK.

Aperture Delay Jitter

The variation in the aperture delay time from conversion to conversion. This random variation will result in noise when sampling an AC input. The signal to noise ratio due to the jitter alone will be:

$$SNR_{JITTER} = -20\log (2\pi \bullet f_{IN} \bullet t_{JITTER})$$

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies fa and fb are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at the sum and difference frequencies of mfa ± nfb, where m and n = 0, 1, 2, 3, etc. For example, the 3rd order IMD terms include (2fa + fb), (fa + 2fb), (2fa – fb) and (fa – 2fb). The 3rd order IMD is defined as the ratio of the RMS value of either input tone to the RMS value of the largest 3rd order IMD product.

Signal-to-Noise Plus Distortion Ratio

The signal-to-noise plus distortion ratio [S/(N+D)] is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components at the ADC output. The output is band limited to frequencies above DC to below half the sampling frequency.

Crosstalk

Crosstalk is the coupling from one channel (being driven by a full-scale signal) onto the other channel (being driven by a –1dBFS signal).

Signal-to-Noise Ratio

The signal-to-noise (SNR) is the ratio between the RMS amplitude of the fundamental input frequency and the RMS amplitude of all other frequency components, except the first five harmonics.

Spurious Free Dynamic Range (SFDR)

The ratio of the RMS input signal amplitude to the RMS value of the peak spurious spectral component expressed in dBc. SFDR may also be calculated relative to full scale and expressed in dBFS.

DEFINITIONS

SERIAL INTERFACE TERMS

8B/10B Encoding

A data encoding standard that encodes an 8-bit octet into a 10-bit code-group (IEEE Std 802.3-2002 part 3, clause 36.2). The resulting code-group is ideal for serial transmission for two fundamental reasons: 1) The receiver does not require a high speed clock to capture the data because the code-groups are run-length limited to ensure a sufficient number of transitions for PLL-based clock recovery 2) AC coupling is permitted because the code-groups are DC balanced (see Running Disparity).

A table of the 256 possible input octets with the resulting 10-bit code-groups is documented in IEEE Std 802.3-2002 part 3 Table 36-1. A name associated with each of the 256 data code-groups is formatted "Dx.y", with x ranging from 0 to 31 and y ranging from 0 to 7. Additionally, Table 36-2 of the standard defines a set of 12 special code-groups used as non-data characters (such as commas) with the naming format of "Kx.y".

Current Mode Logic (CML)

A circuit technique used to implement differential high speed logic. CML employs differential pairs (usually n-type) to steer current into resistive loads. It is possible to implement any logic function using CML. The output swing and offset is dependent on the bias current, the load resistance, and termination resistance.

This product family uses CML drivers to transmit high speed serial data to the outside world. The output driver bias current is typically programmable from 10mA to 16mA, generating a signal swing of approximately $250mV_{P-P}$ (500mVppd) to $400mV_{P-P}$ (800mVppd) across the combined internal and external termination resistance of 25Ω (50Ω source//50Ω termination) on each output (mVppd stands for mV_{P-P} differential).

Code-Group

The 10-bit output from an 8B/10B encoder or the 10-bit input to the 8B/10B decoder.

Comma

A special 8B/10B code-group containing the binary sequence "0011111" or "1100000". Commas are used for frame alignment and synchronization because a comma sequence cannot be generated by any combination of normal code-groups (unless a bit error occurs). There are three special code-groups that contain a comma, K28.1, K28.5, and K28.7.

For brevity, each of these three special code-groups are often called a comma, but in the strictest sense it is the first 7 bits of these code-groups that are designated a comma.

DC Balanced Signal

A specially conditioned signal that may be AC coupled with minimal degradation to the signal. DC balance is achieved when the average number of 1's and 0's are equal, eliminating the undesirable effects of DC wander on the receive side of the coupling capacitor. When 8B/10B coding is used, DC balance is achieved by following disparity rules (see Running Disparity).

De-Scrambler

A logic block that restores scrambled data to its pre-scrambled state. A self aligning de-scrambler is based on the same pseudo random bit sequence as the scrambler, so it requires no alignment signals. In this product family the scrambler is based on the $1+x^{14}+x^{15}$ polynomial, and the self aligning process results in an initial loss of 15 bits, or one ADC sample.

Deterministic Latency

A predictable and repeatable delay from the input to the output of the system. JESD204B subclasses1 and 2 employ technologies that support a predictable and repeatable pipeline delay through the system.

Frame

The LTC2122 frame consists of two complete code-groups per lane, and constitutes one complete ADC sample per lane.

DEFINITIONS

Frame Alignment Monitoring (FAM)

After initial frame synchronization has been established, frame alignment monitoring enables the receiver to verify that code-group alignment is maintained without the loss of data. This is done by substituting a K28.7 comma for the last code-group of the frame when certain conditions are met. The receiver uses this comma as a position marker within the frame for alignment verification. After decoding the data, the receiver replaces the K28.7 comma with the original data.

Initial Frame Synchronization

The process of communicating frame boundary information to the receiver for alignment purposes. The receiver asserts the SYNC~ signal causing the ADC to transmit K28.5 commas to the receiver. The receiver deasserts the SYNC~ signal, and the ADC ceases transmission of commas according to the rules of the particular sub-class and mode of operation. The point of termination of commas in the data stream marks the frame boundary.

Lane Alignment Monitoring (LAM)

In JESD204B, lane alignment is attained and monitored through the use of the 8B/10B K28.3 special characters. These characters are conditionally embedded in the data stream at the end of the multiframe. The receiver uses this character as a position marker within the multiframe for lane alignment verification. After decoding the data, the receiver replaces the K28.3 character with the original data.

Local Multiframe Clock (LMFC)

An internal clock within each device of a JESD204B system that marks the multiframe boundary.

Multiframe

A group of frames intended to be of long duration compared to lane mismatches in multiple lane systems. In JESD204B the maximum Multiframe length is 32 frames.

There is no external multiframe clock in a JESD204B system, so the signal marking the multiframe boundaries is referred to as the local multiframe clock (LMFC).

Octet

The 8-bit input to an 8B/10B encoder, or the 8-bit output from an 8B/10B decoder.

Run-Length Limited (RLL)

Data that has been encoded for the purpose of limiting the number of consecutive 1's or 0's in a data stream.

This process guarantees that there will be an adequate number of transitions in the serial data for the receiver to lock onto with a phase-locked loop and recover the high speed clock.

Running Disparity

In order to maintain DC balance most 8B/10B code-groups have two output possibilities for each input octet. The running disparity is calculated to determine which of the two code-groups should be transmitted to maintain DC balance.

The disparity of a code-group is analyzed in two segments called sub-blocks. Sub-block1 consists of the first six bits of a code-group and sub-block2 consists of the last four bits of a code-group. When a sub-block is more heavily weighted with 1's the running disparity is positive, and when it is more heavily weighted with 0's the running disparity is negative. When the number of 1's and 0's are equal in a sub-block, the running disparity remains unchanged.

The polarity of the current running disparity determines which code-group should be transmitted to maintain DC balance. For a complete description of disparity rules, refer to IEEE Std 802.3-2002 part 3, Clause 36.2.4.4.

Pseudo Random Bit Sequence (PRBS)

A data sequence having a random nature over a finite interval. The most commonly used PRBS test patterns may be described by a polynomial in the form of $1+x^m+x^n$ and have a random nature for the length of up to 2n-1 bits, where n indicates the order of the PRBS polynomial and m plays a role in maximizing the length of the random sequence.

Scrambler

A logic block that applies a pseudo random bit sequence to the input octets to minimize the tonal content of the high speed serial bit stream.

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2122 is a two-channel, 14-bit 170Msps A/D converter with JESD204B high speed serial outputs. The analog inputs must be driven differentially. The DEVCLK inputs should be driven differentially for optimal performance. The high speed serial interface is capable of data rates of up to 6.0Gbps per lane. The overflow/underflow indicators are available as part of the high speed serial data, and optionally as low-latency double data rate LVDS outputs. A SPI port provides programmability of multiple user options.

ANALOG INPUT

The analog inputs are differential CMOS sample-and hold circuits (Figure 2). The inputs must be driven differentially around a common mode voltage set by the V_{CM} output pin, which is nominally 0.8V. For the 1.5V input range, the inputs should swing from V_{CM} – 0.375V to V_{CM} + 0.375V. There should be 180° phase difference between the inputs. The two channels are simultaneously sampled by a shared clock circuit.

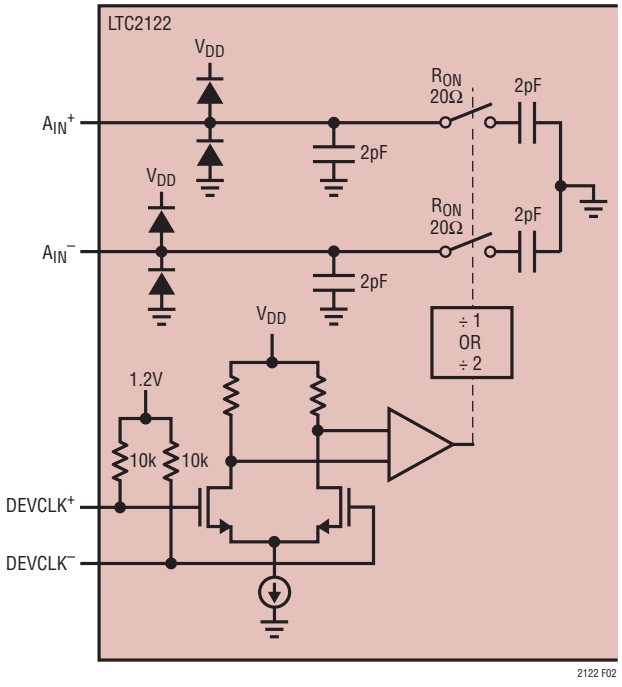


Figure 2. Equivalent Input Circuit for a Single Channel

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wide band noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's specific input frequency.

Transformer-Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with the common mode supplied through a pair of resistors via the V_{CM} pin. At higher input frequencies a transmission line balun transformer (Figures 4 and 5) has better balance, resulting in lower A/D distortion.

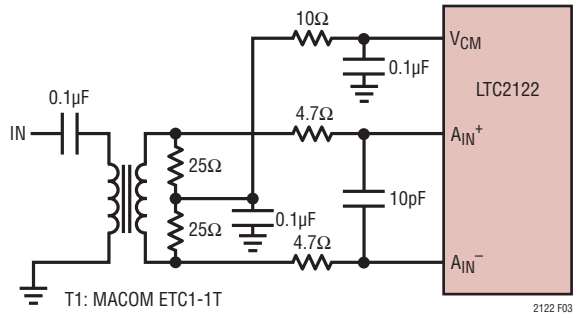


Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

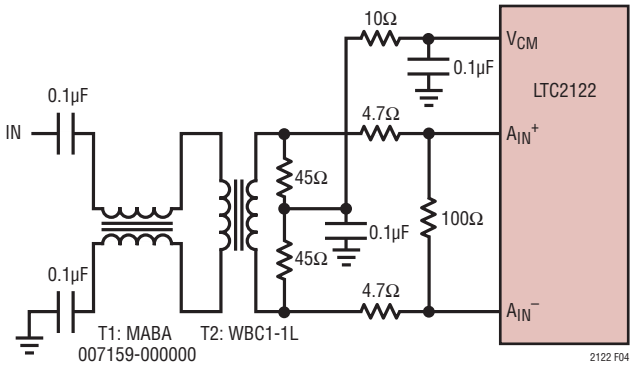


Figure 4. Recommended Front-End Circuit for Input Frequencies from 15MHz to 150MHz

APPLICATIONS INFORMATION

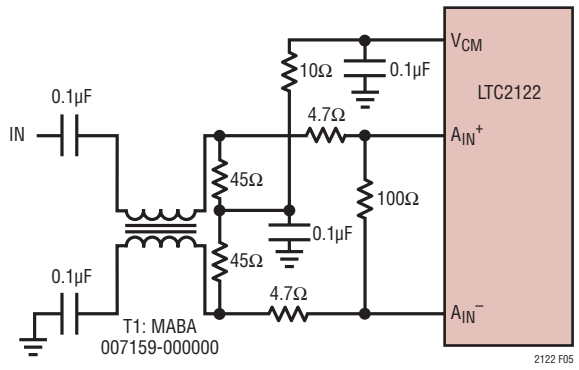


Figure 5. Recommended Front-End Circuit for Input Frequencies from 150MHz to 900MHz

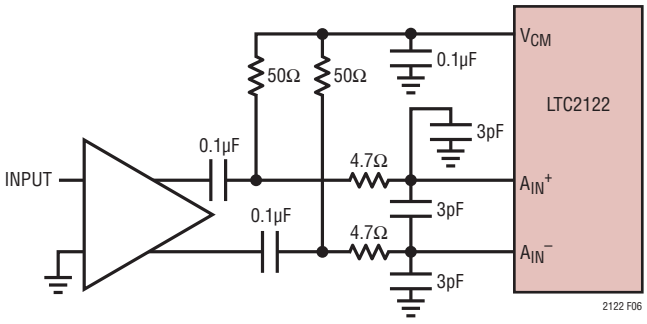


Figure 6. Front-End Circuit Using a High Speed Differential Amplifier

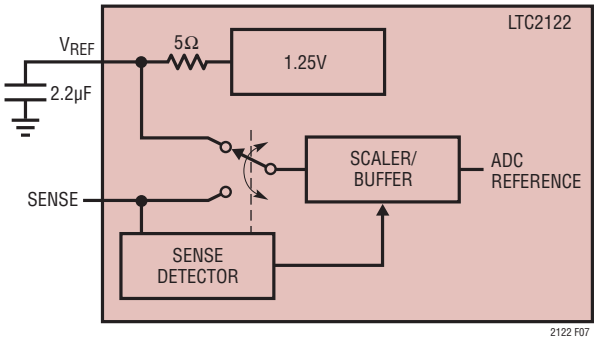


Figure 7. Reference Circuit

Amplifier Circuits

Figure 6 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion. At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 3 through 5) should convert the signal to differential before driving the A/D. The A/D cannot be driven single-ended.

Reference

The LTC2122 has an internal 1.25V voltage reference. For a 1.5V input range with internal reference, connect SENSE to V_{DD}. For a 1.5V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 7).

Device Clock (DEVCLK) Input

The DEVCLK is used to derive the ADC sample clock, so the signal quality of the DEVCLK inputs strongly affects the A/D noise performance. The DEVCLK inputs should be treated as analog signals. Do not route them next to digital traces on the circuit board. The DEVCLK inputs are internally biased to 1.2V through 10k equivalent resistance (Figure 8).

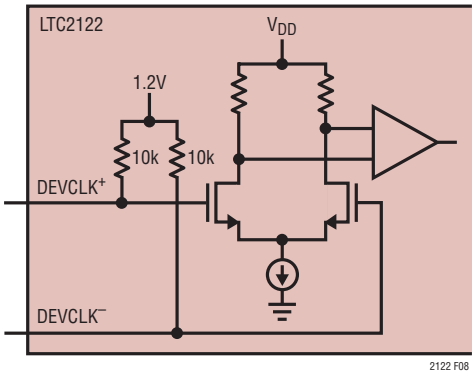


Figure 8. Equivalent DEVCLK Input Circuit

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If the common mode of the driver is within 1.1V to 1.5V, it is possible to drive the DEVCLK inputs directly. Otherwise a transformer or coupling capacitors are needed (Figures 9 and 10). The maximum (peak) voltage of the input signal should never exceed V_{DD} +0.1V or go below –0.1V.

The ADC sample clock is derived from DEVCLK. For good performance the sample clock should have a 50% (±5%) duty cycle. There are two programmable options provided in the LTC2122 that will ensure a 50% duty cycle sample clock:

1) An optional DEVCLK divide-by-two circuit is provided in the clock path to convert a 2X harmonic DEVCLK to a 50% duty cycle sample clock. The 2X_CLK option is enabled via SPI register 2, bit 2.

2) If a 2X clock is not available, the clock Duty Cycle Stabilizer (DCS) circuit may be enabled. When enabled, the DEVCLK duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. The duty cycle stabilizer is enabled via SPI register 2, bit 0. If the 2X_CLK option is selected in the SPI register the Duty Cycle Stabilizer is disabled regardless of the state of the DCS_en bit.

For applications where the sample rate needs to be changed quickly and a 2X clock is not available, both the 2X_CLK and the clock duty cycle stabilizer may be disabled. In this case, care should be taken to make the DEVCLK a 50% (±5%) duty cycle.

Overflow Detection

An overflow (OF) is detected when the analog inputs are either over-ranged or under-ranged. There are two mechanisms for reporting an OF event:

1) The OF bit is transmitted as part of the serial bit stream following the LSB of the ADC data.

2) There is a separate LVDS output pair dedicated to early indication of an OF event. The LVDS OF indicator has a latency of 6 sample clock cycles. Both ADC OF signals are multiplexed to one output pair at double data rate. The Channel A OF signal is active on the first half of the internal sample clock and the Channel B OF signal is active on the second half of the cycle.

The LVDS OF indicator is output at standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required to function properly. The termination resistor should be located as close as possible to the LVDS receiver. If used, this LVDS output pair is enabled via SPI register 2, bit 1.

DATA FORMAT

Table 1 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. The output data format is offset binary.

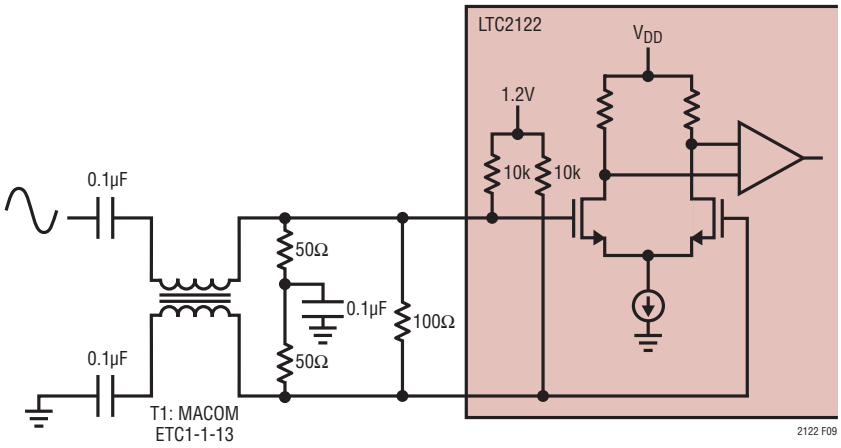

Figure 9. Sinusoidal DEVCLK Drive

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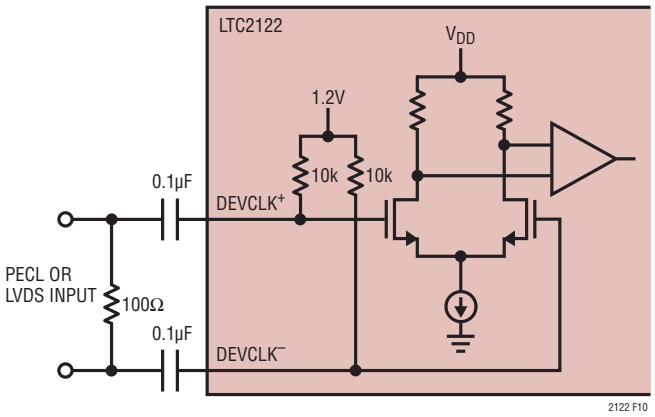

Figure 10. AC Coupled DEVCLK Drive

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (1.5V RANGE)	OF	D13-D0 (OFFSET BINARY)
>0.75V	1	11 1111 1111 1111
+0.75V	0	11 1111 1111 1111
+0.749908V	0	11 1111 1111 1110
+0.0000915V	0	10 0000 0000 0001
+0.000000V	0	10 0000 0000 0000
–0.0000915V	0	01 1111 1111 1111
–0.0001831V	0	01 1111 1111 1110
–0.7499084V	0	00 0000 0000 0001
–0.75V	0	00 0000 0000 0000
< –0.75V	1	00 0000 0000 0000

Power Down Modes

The power down modes are controlled through register 1 of the SPI interface. The two ADC channels may be powered down separately, simultaneously, or the entire device may be placed in sleep mode to conserve power. The “PDA” and “PDB” SPI register bits are used to power down each ADC channel individually while keeping the internal clock and reference circuits active. “SLEEP” powers down the entire device, resulting in < 5mW power consumption. The amount of time required to recover from sleep mode depends on the size of the bypass capacitor on V_{REF}. For the suggested value of 2.2µF, the A/D will stabilize after 0.1ms + 2500 • tp where tp is the period of the sampling clock.

Nap Mode

In "NAP” mode both ADC cores are powered down while the internal clock circuits, reference circuits, and serial interface stay active, allowing faster wake-up. While in nap mode the data at the output of the each ADC is forced to zero. The SPI and the serial test patterns are fully functional in nap mode, so any test pattern may be selected through the SPI. Recovering from nap mode requires at least 100 clock cycles.

JESD204B Overview

JESD204B is a JEDEC standard that defines a high speed serial interface for data converters. The advantages of serialization include the simplification of printed circuit board (PCB) layout through the reduction of traces on the PCB. JESD204B solves several problems associated with serial data transmission, such as the identification of the start of a sample and the proper alignment of data arriving on multiple lanes.

JESD204B devices encode the parallel data using industry standard 8B/10B code-groups (IEEE 802.3-2002, section 3). There is an overhead requirement of 2 bits for every 8 encoded bits (8 bits are encoded to 10 bits), but encoding the ADC data prior to serialization provides certain benefits which make the transmitted data more suitable for serial transmission: These benefits include DC balance (for AC coupling), and Run-Length Limiting (providing a sufficient number of transitions for the receiver to extract the clock from the data with a Phase-Locked Loop).

Figures 11 and 12 illustrate the transformation of ADC sampled data into 10-bit code-groups prior to transmission. The code-groups are formed into frames and multiframes. For the LTC2122, there are two possible lane configurations:

1) One lane mode (both ADCs multiplexed to one lane) at up to 6.0Gbps per lane (up to 150Msps).

2) Two lane mode (one lane per ADC) operating at up to 3.4Gbps per lane.

SYNC~ Signal

In addition to the high speed serial lanes, JESD204B requires the use of a SYNC~ (active low) signal. The SYNC~ signal originates from the receiver and serves as a request to the LTC2122 that synchronization is required (JESD204B 4.9).

APPLICATIONS INFORMATION

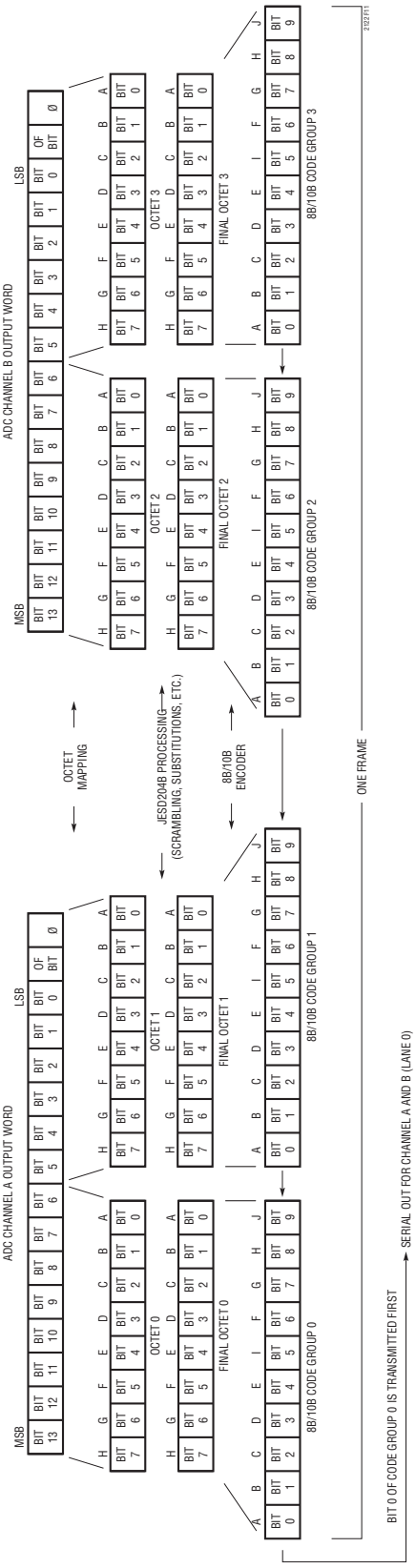

Figure 11. Word Formation of the Single Lane in One-Lane Mode

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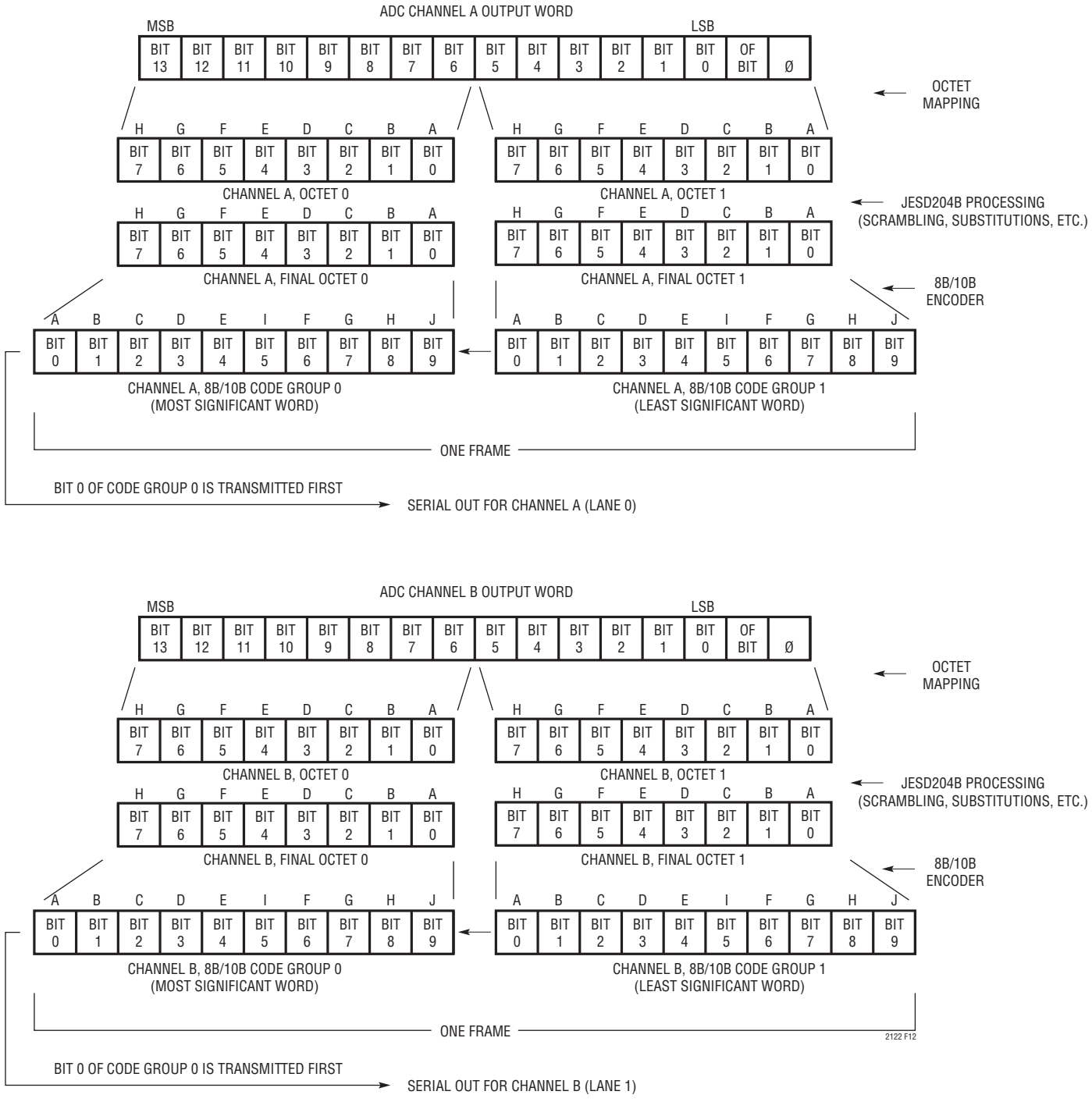

Figure 12. Word Formation of Each Lane in Two-Lane Mode

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Table 2. JESD204B Link Configuration Parameters

JESD204B LINK CONFIGURATION PARAMETER	LTC2122 DEVICE VALUE FOR SINGLE LANE MODE	LTC2122 DEVICE VALUE FOR ONE LANE PER ADC MODE	ENCODING
DID<7:0>	SPI Programmable	SPI Programmable	Binary Value
ADJCNT<3:0>	NA, 0000	NA, 0000	Binary Value
BID<3:0>	SPI Programmable	SPI Programmable	Binary Value
ADJDIR	NA, 0	NA, 0	Binary Value
PHADJ	NA, 0	NA, 0	Binary Value
LID_{-1}<4:0> CMLOUT_A0 CMLOUT_B0	 0_0000 NA	 0_0000 0_0001	 Binary Value Minus 1
SCR<0>	SPI Programmable	SPI Programmable	Binary Value
L_{-1}<4:0>	0_0000	0_0001	Binary Value Minus 1
F_{-1}<7:0>	0000_0011	0000_0001	Binary Value Minus 1
K_{-1}<4:0>	SPI Programmable	SPI Programmable	Binary Value Minus 1
M_{-1}<7:0>	0000_0001	0000_0001	Binary Value Minus 1
CS<1:0>	01	01	Binary Value
N_{-1}<4:0>	0_1101	0_1101	Binary Value Minus 1
SUBCLASSV<2:0>	SPI Programmable	SPI Programmable	Binary Value
N'_{-1}<4:0>	0_1111	0_1111	Binary Value Minus 1
JESDV<2:0>	001	001	Binary Value
S_{-1}<4:0>	0_0000	0_0000	Binary Value Minus 1
HD	0	0	Binary Value
CF<4:0>	0_0000	0_0000	Binary Value
FCHK<7:0>	Sum of all fields mod 256	Sum of all fields mod 256	Binary Value

JESD204B Link Configuration Parameters

There are 20 link configuration parameters used by JESD204B to describe the operation of the link (JESD204B 8.3, Table 20). The receiver must match the parameters of the LTC2122 in order for error free communication to take place. Table 2 summarizes the link parameters of the LTC2122.

JESD204B Subclasses

There are 3 subclasses of operation for JESD204B. These subclasses provide different levels of deterministic latency through the communication link. Below is a simple overview of the three subclasses:

Subclass 0: No deterministic latency support is provided. There is no support for resetting and aligning critical clocks between the LTC2122 and the receiver. The LTC2122 is compliant with this subclass.

Subclass 1: Deterministic latency is obtained through the addition of a SYSREF signal. The SYSREF signal provides precise timing information for aligning critical clocks in the LTC2122 and in the receiver. The low to high transition of SYSREF is sampled by the rising edge of DEVCLK, so the DEVCLK and SYSREF signals should originate from close proximity to each other and delays between these signals should closely match (Figure 13). The LTC2122 is compliant with this subclass.

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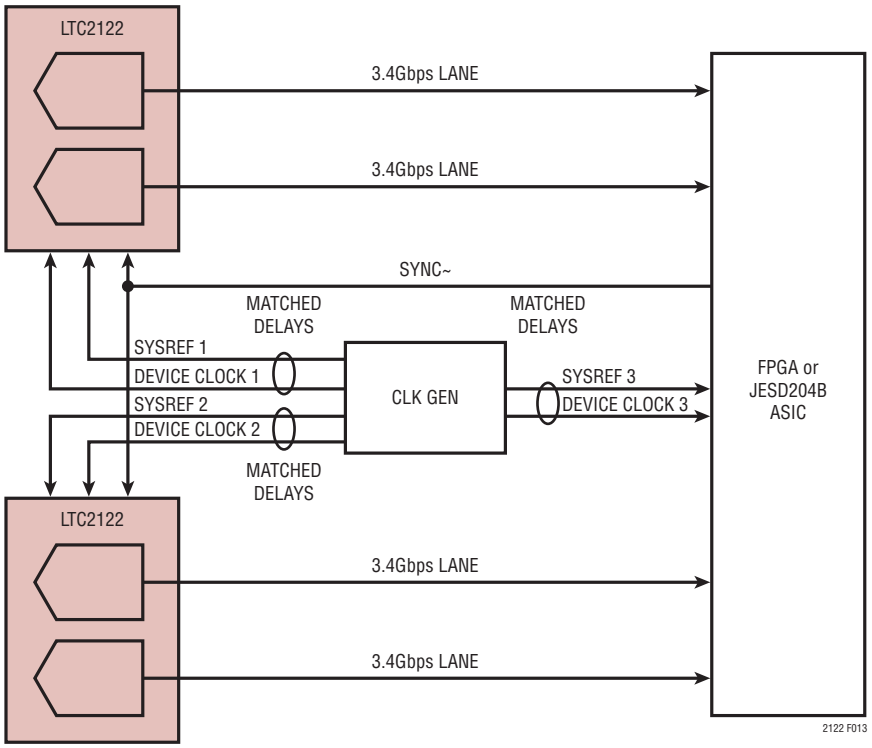
As an added subclass 1 protection, the LTC2122 provides an optional Alert mode. Depending on the SYSREF generation circuit, there could be an erroneous or short pulse generated as the first SYSREF pulse. To avoid the possibility of alignment errors due to a compromised first pulse, an optional Alert mode may be enabled in the SPI. While in Alert mode, the LTC2122 will ignore the first SYSREF pulse, and reset critical clocks with the second pulse. The first pulse, therefore, serves to arm the system, and the second pulse resets the clocks. After a programmable number of multiframes without a second SYSREF pulse, the system is disarmed until the next SYSREF pulse is received. Figure 14 illustrates the state machine of the Subclass 1 Alert mode.

Subclass 2: Deterministic latency support is obtained by sampling the low to high transition of the SYNC~ signal with the rising edge of DEVCLK. Upon detection of the SYNC~ low to high transition, the critical clocks are realigned. The LTC2122 is compatible with this subclass, but the detection resolution is always determined by the ADC DEVCLK frequency.



NOTE: INTERNAL CLOCKS ARE RESET BY SYSREF ON THE RISING EDGE OF THE DEVICE CLOCK. FOR DETERMINISTIC LATENCY, EACH SYSREF/DEVICE CLOCK PAIR SHOULD HAVE MATCHED DELAYS, AND SHOULD SATISFY SETUP AND HOLD REQUIREMENTS, t_{SU_SYN} AND t_{H_SYS}.

Figure 13. JESD204B Subclass 1 Configuration

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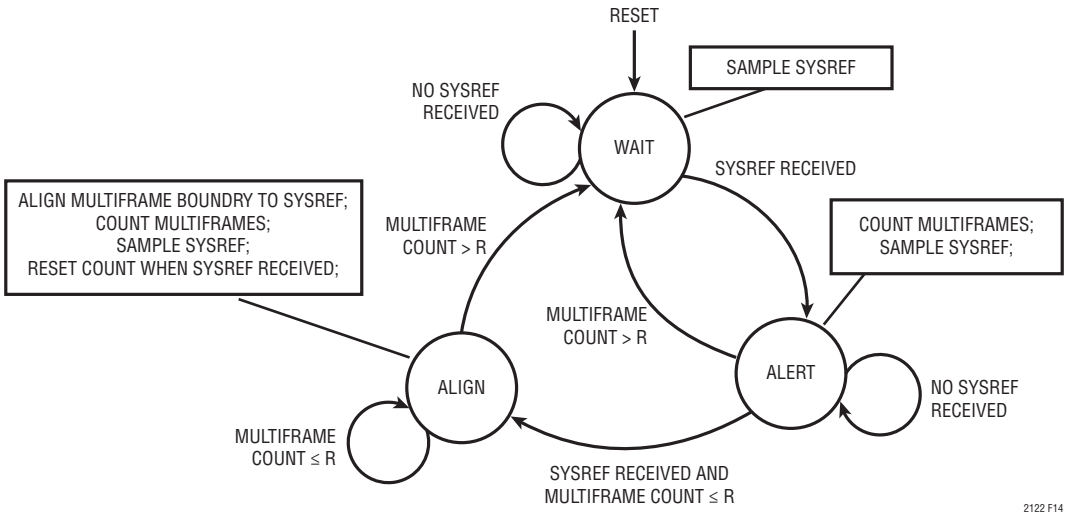

Figure 14. Alert Mode of Subclass 1

Code-Group Synchronization
(JESD204B 5.3.3.1)

In order for each receiver to properly align to the received serial data, each ADC transmitter must communicate the location of the start of a code-group and the start of a frame to its receiver. When multiple ADC devices are transmitting on multiple lanes, this alignment must take place on all lanes simultaneously in order for the receivers to determine the relationship between lanes. A receiver initiates synchronization by asserting its SYNC~ signal. When multiple receivers are present, the SYNC~ signals of all receivers may be logically ORed to provide synchronization requests to all ADC devices simultaneously. The following synchronization process may be initiated by the receivers at any time:

- The receiver issues a request for synchronization by asserting the SYNC~ signal (active low).
- The ADC device will detect the SYNC~ assertion on the fifth rising edge of its Local Frame Clock (LFC). At the beginning of the frame following detection, each ADC transmitter will broadcast a continuous stream of K28.5 symbols in place of data.
- After the receiver has successfully received at least four consecutive K28.5 symbols, it will deassert the SYNC~ signal.

Subclass 0:

- The ADC device will detect the deassertion of the SYNC~ signal on the rising edge of its device clock, and continue to transmit K28.5 symbols on each lane until the beginning of the frame following detection.
- If the Initial Lane Alignment Sequence (ILAS) is not disabled, the ADC device will reset its multiframe start marker and transmit an ILAS followed by encoded ADC data. The ILAS will be four multiframes in length.
- If the ILAS is disabled, the ADC device will begin transmitting encoded ADC data on each lane.

Subclass 1:

- The ADC device will detect the deassertion of the SYNC~ signal on the rising edge of its device clock, and continue to transmit K28.5 symbols on each lane until the beginning of the next multiframe.
- If the ILAS is not disabled, the ADC device will transmit an ILAS at the beginning of the multiframe. The ILAS is immediately followed by encoded ADC data.
- If the ILAS is disabled the ADC device will begin transmitting encoded ADC data on each lane at the beginning of the multiframe boundary.

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Subclass 2:

- Unique to this subclass, the SYNC~ signal must be deasserted by the receiver on its multiframe boundary. The ADC device will detect the deassertion of the SYNC~ signal on the rising edge of its device clock (for minimum latency error the ADC device clock frequency must be greater than or equal to the receiver device clock frequency).
- The ADC's Local Frame Clock (LFC) and Local Multiframe Clock (LMFC) are reset on the detected edge.
- After resetting the internal clocks, the ADC device will continue to transmit K28.5 symbols on each lane for one multiframe (at least 5 frames + 9 octets) to enable the receiver to re-sync to the new clock positions. The ADC device will then cease K28.5 transmission at the next multiframe start.
- If the ILAS is enabled, the ADC device will transmit an ILAS followed by encoded ADC data.
- If the ILAS is not enabled the ADC device will transmit encoded ADC data on each lane.

The start of a code-group will coincide with the start of each K28.5 symbol.

The start of a frame will coincide with the first non-K28.5 symbol after the SYNC~ signal has been deasserted.

Initial Lane Alignment Sequence Transmission
(JESD204B 5.3.3.5)

When the lane alignment sequence is not disabled via the SPI, the sequence illustrated in the Lane Alignment Sequence Tables will be transmitted immediately after code-group synchronization is complete. The lane alignment sequence consists of four complete multiframes. The minimum number of octets in a multiframe is ultimately controlled by the configuration contents of the 2nd multiframe in the lane alignment sequence.

The lane alignment sequence is constructed as follows:

- Each multiframe in the sequence will begin with a K28.0 control character, and will end with a K28.3 symbol.
- An 8-bit lane alignment counter is used to generate the octet data for the lane alignment sequence. The counter is reset by the code-group synchronization process. The counter is clocked by an octet clock (character clock).
- The octet of the lane alignment counter is always transmitted during the lane alignment sequence unless a control character or configuration octet is being transmitted.
- The second multiframe contains the configuration data. The configuration data begins on the 3rd octet of the multiframe, and is preceded by a K28.4 symbol.
- The lane alignment sequence may not be scrambled (the Scramble option in the SPI register is ignored).

Note that the K28.3 symbol is the lane alignment symbol, and may be used by the receivers to align the multiframe boundary pointers in all the lanes in the link.

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Lane Alignment Sequence Tables for Two Lane Mode (One Lane per ADC), 1st Multiframe

Table 3a. Minimum Multiframe Length (*K* = 9), 1st Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Octet Counter	01	D1.0
1	Octet Counter	02	D2.0
	Octet Counter	03	D3.0
2	Octet Counter	04	D4.0
	Octet Counter	05	D5.0
3	Octet Counter	06	D6.0
	Octet Counter	07	D7.0
4	Octet Counter	08	D8.0
	Octet Counter	09	D9.0
5	Octet Counter	0A	D10.0
	Octet Counter	0B	D11.0
6	Octet Counter	0C	D12.0
	Octet Counter	0D	D13.0
7	Octet Counter	0E	D14.0
	Octet Counter	0F	D15.0
8	Octet Counter	10	D16.0
	Lane Alignment Symbol		K28.3

Table 3b. Maximum Multiframe Length (*K* = 32), 1st Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Octet Counter	01	D1.0
1	Octet Counter	02	D2.0
	Octet Counter	03	D3.0
2	Octet Counter	04	D4.0
	Octet Counter	05	D5.0
3	Octet Counter	06	D6.0
	Octet Counter	07	D7.0
4	Octet Counter	08	D8.0
	Octet Counter	09	D9.0
5	Octet Counter	0A	D10.0
	Octet Counter	0B	D11.0
6	Octet Counter	0C	D12.0
	Octet Counter	0D	D13.0
7	Octet Counter	0E	D14.0
	Octet Counter	0F	D15.0
8	Octet Counter	10	D16.0
	Octet Counter	11	D17.0
⋮	⋮	⋮	⋮
25	Octet Counter	32	D18.1
	Octet Counter	33	D19.1
26	Octet Counter	34	D20.1
	Octet Counter	35	D21.1
27	Octet Counter	36	D22.1
	Octet Counter	37	D23.1
28	Octet Counter	38	D24.1
	Octet Counter	39	D25.1
29	Octet Counter	3A	D26.1
	Octet Counter	3B	D27.1
30	Octet Counter	3C	D28.1
	Octet Counter	3D	D29.1
31	Octet Counter	3E	D30.1
	Lane Alignment Symbol		K28.3

APPLICATIONS INFORMATION

Lane Alignment Sequence Tables for Two Lane Mode (One Lane per ADC), 2nd Multiframe

Table 3c. Minimum Multiframe Length (*K* = 9), 2nd Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Start of Link Configuration		K28.4
1	*DID*[7:0]	*00	D0.0
	{*ADJCNT*[3:0], *BID*[3:0]}	*00	D0.0
2	{*0, ADJDIR, PHADJ, LID*[4:0]}	00	D0.0
	{*SCR, 00, L–1*[4:0]}	*01	D1.0
3	*F–1* [7:0]	01	D1.0
	{*000, K–1*[4:0]}	*08	D8.0
4	*M–1* [7:0]	01	D1.0
	{*CS*[1:0]], *0,* [*N–1* [4:0]}	4D	D13.2
5	{*SUBCLASSV*[2:0], *N'–1*[4:0]}	0F	D15.0
	{*JESDV*[2:0], *S–1* [4:0]}	20	D0.1
6	{*HD*[0], *00, CF*[4:0]}	00	D0.0
	Reserved	00	D0.0
7	Reserved	00	D0.0
	FCHK[7:0]	29	D9.1
8	Octet Counter	22	D2.1
	Lane Alignment Symbol		K28.3

X_{-1} Indicates that field X is affected by -1 encoding

{} Indicates concatenation

* Indicates a field directly programmable through the SPI

Configuration Field Defaults: *DID* = 0, *BID* = 0, *LID* = 0, *SCR* = 0, *L* = 2, *F* = 2, *K* = 9 or 32, *M* = 2, *CS* = 1, *N* = 14, SUBCLASSV = 0, *N'* = 16, *S* = 1, *HD* = 0, *CF* = 0

Field Descriptions: *DID* = Device ID, *BID* = Bank ID, *LID* = Lane ID, *SCR* = Scrambling enabled, *L* = Lanes per device, *F* = Octets per frame, *K* = Frames per multiframe, *M* = Converters per device, *CS* = Control bits per sample, *N* = Converter Resolution, *N'* = Total bits per sample, *S* = Samples per converter per frame, *HD* = High density format, *CF* = Control words per frame per link, *FCHK* = Checksum of all fields (mod 256)

Table 3d. Maximum Multiframe Length (*K* = 32), 2nd Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Start of Link Configuration		K28.4
1	*DID*[7:0]	*00	D0.0
	{*ADJCNT*[3:0], *BID*[3:0]}	*00	D0.0
2	{0, *ADJDIR*, *PHADJ*, *LID*[4:0]}	*00	D0.0
	{*SCR*[0], 00, *L–1*[4:0]}	*01	D1.0
3	*F–1* [7:0]	01	D1.0
	{000, *K–1*[4:0]}	*1F	D8.0
4	*M–1* [7:0]	01	D1.0
	{*CS*[1:0]], 0, [*N–1* [4:0]}	4D	D13.2
5	{*SUBCLASSV*[2:0], *N'–1*[4:0]}	0F	D15.0
	{*JESDV*[2:0], *S–1* [4:0]}	20	D0.1
6	{*HD*[0], 00, *CF*[4:0]}	00	D0.0
	Reserved	00	D0.0
7	Reserved	00	D0.0
	FCHK[7:0]	40	D0.2
8	Octet Counter	50	D16.2
	Octet Counter	51	D17.2
⋮	⋮	⋮	⋮
25	Octet Counter	72	D18.3
	Octet Counter	73	D19.3
26	Octet Counter	74	D20.3
	Octet Counter	75	D21.3
27	Octet Counter	76	D22.3
	Octet Counter	77	D23.3
28	Octet Counter	78	D24.3
	Octet Counter	79	D25.3
29	Octet Counter	7A	D26.3
	Octet Counter	7B	D27.3
30	Octet Counter	7C	D28.3
	Octet Counter	7D	D29.3
31	Octet Counter	7E	D30.3
	Lane Alignment Symbol		K28.3

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Lane Alignment Sequence Tables for Two Lane Mode (One Lane per ADC), 3rd Multiframe

Table 3e. Minimum Multiframe Length (*K* = 9), 3rd Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Octet Counter	25	D5.1
1	Octet Counter	26	D6.1
	Octet Counter	27	D7.1
2	Octet Counter	28	D8.1
	Octet Counter	29	D9.1
3	Octet Counter	2A	D10.1
	Octet Counter	2B	D11.1
4	Octet Counter	2C	D12.1
	Octet Counter	2D	D13.1
5	Octet Counter	2E	D14.1
	Octet Counter	2F	D15.1
6	Octet Counter	30	D16.1
	Octet Counter	31	D17.1
7	Octet Counter	32	D18.1
	Octet Counter	33	D19.1
8	Octet Counter	34	D20.1
	Lane Alignment Symbol		K28.3

Table 3f. Maximum Multiframe Length (*K* = 32), 3rd Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Octet Counter	81	D1.4
1	Octet Counter	82	D2.4
	Octet Counter	83	D3.4
2	Octet Counter	84	D4.4
	Octet Counter	85	D5.4
3	Octet Counter	86	D6.4
	Octet Counter	87	D7.4
4	Octet Counter	88	D8.4
	Octet Counter	89	D9.4
5	Octet Counter	8A	D10.4
	Octet Counter	8B	D11.4
6	Octet Counter	8C	D12.4
	Octet Counter	8D	D13.4
7	Octet Counter	8E	D14.4
	Octet Counter	8F	D15.4
8	Octet Counter	90	D16.4
	Octet Counter	91	D17.4
⋮	⋮	⋮	⋮
25	Octet Counter	B2	D18.5
	Octet Counter	B3	D19.5
26	Octet Counter	B4	D20.5
	Octet Counter	B5	D21.5
27	Octet Counter	B6	D22.5
	Octet Counter	B7	D23.5
28	Octet Counter	B8	D24.5
	Octet Counter	B9	D25.5
29	Octet Counter	BA	D26.5
	Octet Counter	BB	D27.5
30	Octet Counter	BC	D28.5
	Octet Counter	BD	D29.5
31	Octet Counter	BE	D30.5
	Lane Alignment Symbol		K28.3

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Lane Alignment Sequence Tables for Two Lane Mode (One Lane per ADC), 4th Multiframe

Table 3g. Minimum Multiframe Length (*K* = 9), 4th Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Octet Counter	37	D23.1
1	Octet Counter	38	D24.1
	Octet Counter	39	D25.1
2	Octet Counter	3A	D26.1
	Octet Counter	3B	D27.1
3	Octet Counter	3C	D28.1
	Octet Counter	3D	D29.1
4	Octet Counter	3E	D30.1
	Octet Counter	3F	D31.1
5	Octet Counter	40	D0.2
	Octet Counter	41	D1.2
6	Octet Counter	42	D2.2
	Octet Counter	43	D3.2
7	Octet Counter	44	D4.2
	Octet Counter	45	D5.2
8	Octet Counter	46	D6.2
	Lane Alignment Symbol		K28.3

Table 3h. Maximum Multiframe Length (*K* = 32), 4th Multiframe

FRAME	DESCRIPTION	DATA OCTET (HEX)	8B/10B SYMBOL
0	Start of Subsequence		K28.0
	Octet Counter	C1	D1.6
1	Octet Counter	C2	D2.6
	Octet Counter	C3	D3.6
2	Octet Counter	C4	D4.6
	Octet Counter	C5	D5.6
3	Octet Counter	C6	D6.6
	Octet Counter	C7	D7.6
4	Octet Counter	C8	D8.6
	Octet Counter	C9	D9.6
5	Octet Counter	CA	D10.6
	Octet Counter	CB	D11.6
6	Octet Counter	CC	D12.6
	Octet Counter	CD	D13.6
7	Octet Counter	CE	D14.6
	Octet Counter	CF	D15.6
8	Octet Counter	D0	D16.6
	Octet Counter	D1	D17.6
⋮	⋮	⋮	⋮
25	Octet Counter	F2	D18.7
	Octet Counter	F3	D19.7
26	Octet Counter	F4	D20.7
	Octet Counter	F5	D21.7
27	Octet Counter	F6	D22.7
	Octet Counter	F7	D23.7
28	Octet Counter	F8	D24.7
	Octet Counter	F9	D25.7
29	Octet Counter	FA	D26.7
	Octet Counter	FB	D27.7
30	Octet Counter	FC	D28.7
	Octet Counter	FD	D29.7
31	Octet Counter	FE	D30.7
	Lane Alignment Symbol		K28.3

APPLICATIONS INFORMATION

JESD204B Modes of Operation

Scramble Mode

(JESD204B 5.2, Annex D)

To avoid spectral interference from the serial data output, a SPI enabled data scrambler is added between the ADC data and the 8B/10B encoder to randomize the spectrum of the serial link. The polynomial used for the scrambler is $1+x^{14}+x^{15}$, which is a pseudorandom pattern repeating itself every $2^{15}–1$.

The scrambled data is converted into two valid 8B/10B code-groups. The 8B/10B code-groups are then serialized and transmitted.

The receiver is required to deserialize the data, decode the code-groups into octets, and descramble them back to the original octets using the self-aligning descrambler described in JESD204B 5.2.

Frame Alignment Monitoring (FAM)

(JESD204B 5.3.3.4, 7.3)

A frame contains more than one octet or code-group, so it is necessary to periodically verify that the frame alignment of the receiver is correct.

When frame alignment monitoring is not disabled via the SPI, the receiver may verify frame alignment without the loss of data. To accomplish this, predetermined data in the last code-group of the frame is substituted with the control character, K28.7. The receiver is required to detect the K28.7 character and replace it with the original data. In this way, the last octet or code-group may be verified. There are two possible frame alignment monitoring modes.

FAM mode 1 is implemented when scrambling is not enabled as follows:

- If the data in the last code-group of the current frame equals the data in the last code-group of the previous frame, the converter will replace the last code-group with the control character K28.7 before serialization. However, if a K28.7 symbol was already transmitted in the previous frame, the actual code-group will be transmitted. If lane alignment monitoring is enabled and it is the last code-group of a multiframe, a K28.3 will be transmitted in place of the K28.7, even if a control character was transmitted in the previous frame.
- Upon receiving a K28.7 symbol, the receiver is required to replace it with the data decoded at the same position of the previous frame.

FAM mode 2 is implemented when scrambling is enabled as follows:

- If the data in the last code-group of the current frame equals D28.7, the converter will replace this data with the K28.7 control character. If lane alignment monitoring is enabled and it is the last code-group of a multiframe, a K28.3 will be transmitted in place of the K28.7.
- Upon receiving a K28.7 symbol, the receiver is required to replace it with D28.7.

With FAM enabled the receiver is required to search for the presence of K28.7 symbols in the data stream. If two successive K28.7 symbols are detected at the same position other than the assumed end of frame, the receiver will realign its frame boundary to the new position.

Lane Alignment Monitoring (LAM)

(JESD204B 5.3.3.6, 7.5)

When multiple lanes are present in a link, it is useful to periodically monitor the continued alignment of each lane.

APPLICATIONS INFORMATION

Lane alignment symbols are inserted into the transmitted data on a substitution basis to enable the receiver to verify lane alignment without the loss of data. In this mode, predetermined data in the last code-group of a multiframe is substituted with the control character K28.3. The receiver is required to detect the K28.3 character and replace it with the original data. In this way, the last code-group of a multiframe may be marked and used for lane alignment. There are two possible lane alignment monitoring modes.

LAM mode 1 is implemented when scrambling is not enabled as follows:

- If it is the last code-group of a multiframe and the data equals the data in the last code-group of the previous frame, the converter will replace the current code-group with the control character K28.3.
- Upon receiving a K28.3 symbol, the receiver is required to replace it with the data decoded at the same position of the previous frame.

LAM mode 2 is implemented when scrambling is enabled as follows:

- If it is the last code-group of a multiframe and the data of code-group equals D28.3, the converter will replace this data with the K28.3 control character.
- Upon receiving a K28.3 symbol, the receiver is required to replace it with D28.3.

Simple and Complex Periodic Test Patterns

Seven test patterns are a provided to the user for evaluation and system debug.

Pattern 1: Periodic K28.5

Pattern 1 contains both disparities of the K28.5 Comma, and is 20 bits long. The K28.5 pattern contains a unique combination of maximum and minimum run-lengths, making this pattern useful in quickly observing the effects of Inter Symbol Interference (ISI).

Pattern 2: Periodic K28.7

Pattern 2 produces a square wave of the minimum possible frequency for the high speed serial interface (a “1111100000” pattern).

Pattern 3: Periodic D21.5

Pattern 3 produces the maximum possible frequency for the high speed interface (a “1010” pattern).

Pattern 4: PRBS15

Pattern 4 is a Pseudo Random Bit Sequence based on the polynomial $1+x^{14}+x^{15}$ (the same polynomial used by the scrambler described in JESD204B 5.2). When this pattern is selected, the scrambler is internally forced on and the ADC data is forced to zero. The length of the sequence is $2^{15}–1$ prior to 8B/10B encoding.

When Frame and Lane Alignment Monitoring are not disabled, substitution of data will take place as described in the Frame Alignment Monitoring and Lane Alignment sections of this data sheet.

Pattern 5: Repeated Lane Alignment Sequence

Pattern 5 is the continuous transmission of the lane alignment sequence as described in JESD204B 5.3.3.8.2. In this mode, the following occurs:

Case 1 - SYNC~ is active before entering this state

- Code-group synchronization is performed (K28.5 commas are transmitted in whole frames until SYNC~ is deasserted).
- The lane alignment sequence is transmitted repeatedly according to tables 3a to 3h.

Case 2 - SYNC~ is not active before entering this state

- At least one multiframe of K28.5 commas are transmitted.
- The lane alignment sequence is transmitted repeatedly according to tables 3a to 3h.

If scrambling is enabled, the test samples will not be scrambled.

This test sequence is sensitive to a synchronization request from the receiver. If the SYNC~ signal is asserted at any time during test sample transmission, the lane alignment sequence pointer will be reset, and Case 1 will be repeated.

APPLICATIONS INFORMATION

Pattern 6: Long Transport Layer Test Pattern

Pattern 6 is a test pattern defined in JESD204B 5.1.6.3. The transmission of this test pattern over the link provides a way to verify that the data mapping of the ADC matches the receiver. To place the ADC in this test pattern transmission mode, the corresponding bit must be set in the periodic test pattern SPI register. Once this bit is set, the following occurs:

Case 1 - SYNC~ is active before entering this state

- Code-group synchronization is performed (K28.5 commas are transmitted in whole frames until SYNC~ is deasserted).
- The lane alignment sequence is transmitted (if not disabled) according to Tables 3a to 3h.
- The test pattern of Tables 4a and 4b are repeatedly transmitted on multiframe boundaries.

Case 2 - SYNC~ is not active before entering this state

- The test pattern of Tables 4a and 4b will be transmitted at the start of the next frame.
- Retransmission of the test pattern will occur at the start of each multiframe.

If scrambling is enabled, the test samples will be scrambled, but the lane alignment sequence will not be scrambled.

This test pattern is sensitive to a synchronization request from the receiver. If the SYNC~ signal is asserted at any time during test pattern transmission, the test pattern pointer will be reset, and Case 1 will be repeated.

Table 4a. Long Transport Layer Test Pattern Description for Single Lane (*L* = 1), 4 Octets per Frame (*F* = 4),1 Sample/Converter/Frame Period (*S* = 1)

Test Sample Sequence	ADC 0 (Channel A)		ADC 1 (Channel B)	
	Lane 0 Octets			
Frame 0 (*CID*+1)	0000_0000	0000_0110	0000_0000	0000_1000
Frame 1 (*SID*+1)	0000_0000	0000_0100	0000_0000	0000_0110
Frame *i*, 2≤*i*≤*K* (*MSB* Set to 1)	1000_0000	0000_0000	1000_0000	0000_0000

Table 4b. Long Transport Layer Test Pattern Description for 1 Lane/ADC (*L* = 2), 2 Octets per Frame (*F* = 2), 1 Sample/Converter/Frame Period (*S* = 1)

Test Sample Sequence	ADC 0 (Channel A)		ADC 1 (Channel B)	
	Lane 0 Octets		Lane 2 Octets	
Frame 0 (*CID* + 1)	0000_0000	0000_0110	0000_0000	0000_1000
Frame 1 (*SID* + 1)	0000_0000	0000_0100	0000_0000	0000_0100
Frame 2	1000_0000	0000_0000	1000_0000	0000_0010
Frame 3	1000_0000	0000_0000	1000_0000	0000_0000
Frame *i*, 2 ≤ *i* ≤ *K* (*MSB* Set to 1)	1000_0000	0000_0000	1000_0000	0000_0000

Note: *CID* = Converter ID, *SID* = Sample ID, *K* = Frames in Multiframe, 1 indicates the Control-Bit Position (overflow bit)

APPLICATIONS INFORMATION

Pattern 7: Modified RPAT

JESD204B clauses 4.4.1, 4.5.1, and 4.6.1 require that one of two possible patterns be supported by the transmitter for jitter compliance testing. The modified RPAT pattern is one of these two patterns, and consists of 12 specific code-groups repeated continuously (a description of the modified RPAT sequence may be found in IEEE Std. 802.3-2008 Annex 48A).

This RPAT pattern must begin with positive disparity. To gracefully force positive disparity, a ten character preamble is transmitted. The first nine characters will be the D5.6 code-group. The D5.6 preserves the previous disparity. If the disparity of these nine symbols is positive, the tenth preamble character will also be a D5.6 symbol. If the disparity is negative a reversal is forced by transmitting a D16.2 code-group as the tenth preamble character.

Table 5. Modified RPAT Test Pattern

CODE-GROUP NAME	OCTET VALUE (HEX)	DISPARITY
D30.5	BE	+
D23.6	D7	–
D3.1	23	+
D7.2	47	+
D11.3	6B	+
D15.4	8F	+
D19.5	B3	+
D20.0	14	+
D30.2	5E	–
D27.7	FB	+
D21.1	35	+
D25.2	59	+

Serial Programming

The $\overline{CS}$, SCK, SDI and SDO pins make up the Serial Peripheral Interface (SPI) pins that program the A/D control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. SCK must be low at the time of the falling edge of $\overline{CS}$ for proper operation (see the SPI Timing Diagrams). The data on the SDI pin is latched on the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next 7 bits are the address of the register (A6:A0). The final 8 bits are the register data (D7:D0). If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0).

If the R/$\overline{W}$ bit is high, data in the register selected by the address bits (A6:A0) will be read back on the SDO pin (see the SPI Timing Diagrams). During a read-back command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground through a 200Ω resistor. If register data is read back through SDO, an external 2kΩ pull-up resistor is required. If serial data is only written and read-back is not needed, SDO may be left floating and no pull-up resistor is needed.

Table 6 shows a map of the mode control registers.

Soft Reset

The mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. A global reset of all SPI registers to the default values may be performed by writing a 1 to Bit D7 of Address 0. After the reset is complete, Bit D7 is automatically set back to zero. This register is write-only.

APPLICATIONS INFORMATION

Table 6. SPI Register Memory Map

SPI REGISTER DESCRIPTION	ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
Soft Reset	0	Reset							
Power Down	1					SLEEP	NAP	PDB	PDA
ADC CNTL	2						2X_CLK	OF_en	DCS_en
Device ID	3	DID[7:0]							
Bank ID	4					BID[3:0]			
Lanes (–1)	5						L_{-1}[2:0]		
Frames/Multiframe (–1)	6				K_{-1} [4:0]				
JESD204B Modes	7			LAS_dis	LAM_dis	FAM_dis	Reserved	RST_dis	SCR_en
JESD204B Subclass Modes	8	R_{-1}[2:0] (Alert Length)			Alert	TX_SYNC	SUBCLASS[2:0]		
Periodic Test Patterns	9						PAT[2:0]		
Normal Data							0	0	0
K28.5 (SYNC Comma)							0	0	1
K28.7 (…1111100000…)							0	1	0
D21.5 (…10101010…)							0	1	1
PRBS15 ($1+x^{14}+x^{15}$)							1	0	0
Lane Alignment Sequence							1	0	1
Long Transport Layer Test Pattern							1	1	0
Modified RPAT pattern							1	1	1
CML Output Magnitude	10							CML BIAS[1:0]	
10mA (250mV)								0	0
12mA (300mV)								0	1
14mA (350mV)								1	0
16mA (400mV)								1	1

Note: X_{-1} indicates that field X is affected by –1 encoding

APPLICATIONS INFORMATION

Register A0: Reset Register (Address 00h)

D7	D6	D5	D4	D3	D2	D1	D0
Reset	X	X	X	X	X	X	X

This register is "Write Only". Readback from this register will be all ones

Bit 7 **RESET** Software Reset Bit

0 = Reset Disabled

1 = Software Reset. All SPI registers are set to default values. This bit is automatically set back to zero after the reset is complete.

Bits 6-0 Unused Bits

Register A1: Power Down Modes (Address 01h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	Sleep	Nap	PDB	PDA

Bits 7-4 Unused Bit

Bit 3 **SLEEP**

0 = Normal Operation

1 = Power Down Entire ADC

Bit 2 **NAP**

0 = Normal Operation (Default Setting)

1 = Low Power Keep-Alive Mode for Both Channels

Bit 1 **PDB**

0 = Normal Operation (Default Setting)

1 = Power Down Channel B

Bit 0 **PDA**

0 = Normal Operation (Default Setting)

1 = Power Down Channel A

Register A2: ADC Control (Address 02h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	2X_CLK	OF_en	DCS_en

Bits 7-3 Unused Bits

Bit 2 **2X_CLK**

0 = DEVCLK Frequency is Equal to Sample Frequency (Default Setting)

1 = DEVCLK Frequency is Twice the Sample Frequency

Bit 1 **OF_en**

0 = LVDS Overflow Output is Disabled (Default Setting)

1 = LVDS Overflow Output is Enabled

Bit 0 **DCS_en**

0 = Duty Cycle Stabilizer is Disabled (Default Setting)

1 = Duty Cycle Stabilizer is Enabled

Register A3: Device ID (Address 03h)

D7-D0
DID[7:0]

Bits 7-0 **DID[7:0]** Device ID. Default value is 00000000

DID is defined in JESD204B 8.3. It is only used during the transmission of an initial lane alignment sequence and does not impact the configuration or functionality of the ADC

APPLICATIONS INFORMATION

Register A4: Bank ID (Address 04h)

D7	D6	D5	D4	D3-D0
X	X	X	X	BID[3:0]

Bits 7-4 Unused Bits

Bits 3-0 **BID[3:0]** Bank ID. Default value is 0000

BID is defined in JEDS204B 8.3. Provided as an extension to the DID word. It is only used during the transmission of an initial lane alignment sequence, and does not impact the configuration or functionality of the ADC or serial link

Register A5: Number of Lanes –1 (Address 05h)

D7	D6	D5	D4	D3	D2-D0
X	X	X	X	X	L_{-1}[2:0]

Bits 7-3 Unused Bits

Bits 2-0 **L_{-1}[2:0]** The value of L configures the device. It is also transmitted in the Lane Alignment Sequence

000 = 1 Lane (Both ADCs multiplexed to one lane at up to 6.0Gbps)

001 = 2 Lanes (One Lane per ADC, Default Setting)

Register A6: Number of Frames Per Multiframe –1 (Address 06h)

D7	D6	D5	D4-D0
X	X	X	K_{-1}[4:0]

Bits 7-5 Unused Bits

Bits 4-0 **K_{-1}[4:0]** Frames Per Multiframe minus 1. Default value is 01111 (16 frames per multiframe)

K is defined in JEDS204B 5.3.3.5. For both two and four lane operation, the minimum valid value of K is 9 (K_{-1} = 01000) and the maximum valid value is 32 (K_{-1} = 11111)

Register A7: JESD204B Modes (Address 07h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	LAS_dis	LAM_dis	FAM_dis	0	RST_dis	SCR_en

Bits 7-6 Unused Bits

Bit 5 **LAS_dis**

0 = Lane Alignment Sequence Enabled (Default Setting)

1 = Lane Alignment Sequence Disabled

Bit 4 **LAM_dis**

0 = Lane Alignment Monitor Enabled (Default Setting)

1 = Lane Alignment Monitor Disabled

Bit 3 **FAM_dis**

0 = Frame Alignment Monitor Enabled (Default Setting)

1 = Frame Alignment Monitor Disabled

Bit 2 Reserved bit. Set to 0

Bit 1 **RST_dis**

0 = In Subclass 1, SYSREF Reset of Dividers is Enabled (Default Setting)

In Subclass 2 SYNC~ Reset of Dividers is Enabled (Default Setting)

1 = In Subclass 1, SYSREF Reset of Dividers is Disabled

In Subclass 2 SYNC~ Reset of Dividers is Disabled

Bit 0 **SCR_en**

0 = Scrambling is Disabled (Default Setting)

1 = Scrambling is Enabled

APPLICATIONS INFORMATION

Register A8: JESD204B Subclass Modes (Address 08h)

D7-D5	D4	D3	D2-D0
R_{-1}[2:0]	Alert	TX_SYNC	SUBCLASSV[2:0]

Bits 7-5 **R_{-1} [2:0]** Subclass 1 Alert mode De-arming Length. Default value is 000 (R = 1). Measured in Multiframe Periods

Bit 4 **Alert** Subclass 1 Alert Mode. First Pulse Arms, Second Pulse (and later) are Active

0 = Alert Mode Disabled (Default Setting)

1 = Alert Mode Enabled

Bit 3 **TX_SYNC** A Multiframe of K28.5 Commas are Transmitted If Multiframe Position Changes

0 = Transmitter Induced Synchronization Disabled (Default Setting)

1 = Transmitter Induced Synchronization Enabled

Bits 2-0 **SUBCLASSV[2:0]**

000 = JESD204B Subclass 0 (Default Setting)

001 = JESD204B Subclass 1 (Deterministic Latency Obtained Using SYSYSREF)

010 = JESD204B Subclass 2 (Deterministic Latency Obtained Using SYNC~ Rising Edge)

Register A9: Periodic Test Patterns (Address 09h)

D7	D6	D5	D4	D3	D2-D0
X	X	X	X	X	PAT[2:0]

Bits 7-3 Unused Bits

Bits 2-0 **PAT[2:0]**

000 = Normal ADC Data

001 = K28.5 Pattern (SYNC Comma)

010 = K28.7 Pattern (…1111100000…)

011 = D21.5 Pattern (…1010101010…)

100 = PRBS15 Pattern ($1+x^{14}+x^{15}$)

101 = Lane Alignment Sequence

110 = Long Transport Layer Test Pattern

111 = Modified RPAT Pattern

Register A10: CML Output Magnitude (Address 0Ah)

D7	D6	D5	D4	D3	D2	D1-D0
X	X	X	X	X	X	CMLBIAS[1:0]

Bits 7-2 Unused Bits

Bits 1-0 **CMLBIAS[1:0]** Affects All CML Outputs

00 = 10mA (250mV)

01 = 12mA (300mV)

10 = 14mA (350mV)

11 = 16mA (400mV)

APPLICATIONS INFORMATION

High Speed CML Output Terminations

The CML outputs must be terminated with the transmission line characteristic impedance for proper functionality. In general, the transmission line impedance should be designed to provide either 50Ω single-ended or 100Ω differential.

The OV_{DD} supply voltage and the termination voltage determine the common mode output level of the CML outputs. For proper operation of the CML driver, the output common mode voltage should be greater than 1V.

The directly-coupled termination mode of Figure 15 is recommended when the receiver termination voltage is within the required range. When the CML outputs are directly-coupled to the 50Ω termination resistors, the OV_{DD} supply voltage also serves as the receiver termination voltage, and the output common mode voltage will be in the range of 125mV to 200mV lower than OV_{DD} (depending on the programmed CML current). In this mode, the OV_{DD} voltage should be in the range of 1.125V to 1.2V (minimum), and V_{DD} (maximum).

The directly-coupled differential termination of Figure 16 may be used when no termination voltage at the receiver is available as long as the input common mode voltage is within the required range. In this case, the common mode voltage will be in the range of 250mv to 400mV below OV_{DD}. The minimum OV_{DD} should be in the range of 1.25V to 1.4V (depending on the programmed CML current). The maximum OV_{DD} is equal to V_{DD}.

If the serial receiver's common mode input requirements are not compatible with the directly-coupled termination modes, the DC balanced 8B/10B encoded data will permit DC blocking capacitors as shown in Figure 17. In this AC-coupled mode, the termination voltage is determined by the receiver's requirements. The coupling capacitors should be selected appropriately for the intended operating bit-rate, usually between 1nF to 10nF. In the AC-coupled mode, the output common mode voltage will be 250mV to 400mV below OV_{DD}, so the OV_{DD} supply voltage should be in the same range as the directly coupled differential case. The LTC2122 is fully AC compliant with the JESD204B specification.

Table 7. Minimum OV_{DD} Voltage

CML CURRENT	DIRECTLY COUPLED MIN OV_{DD}	DIRECTLY COUPLED DIFFERENTIAL MIN OV_{DD}	AC COUPLED MIN OV_{DD}
10mA	1.125V	1.25V	1.25V
12mA	1.15V	1.3V	1.3V
14mA	1.175V	1.35V	1.35V
16mA	1.2V	1.4V	1.4V

APPLICATIONS INFORMATION

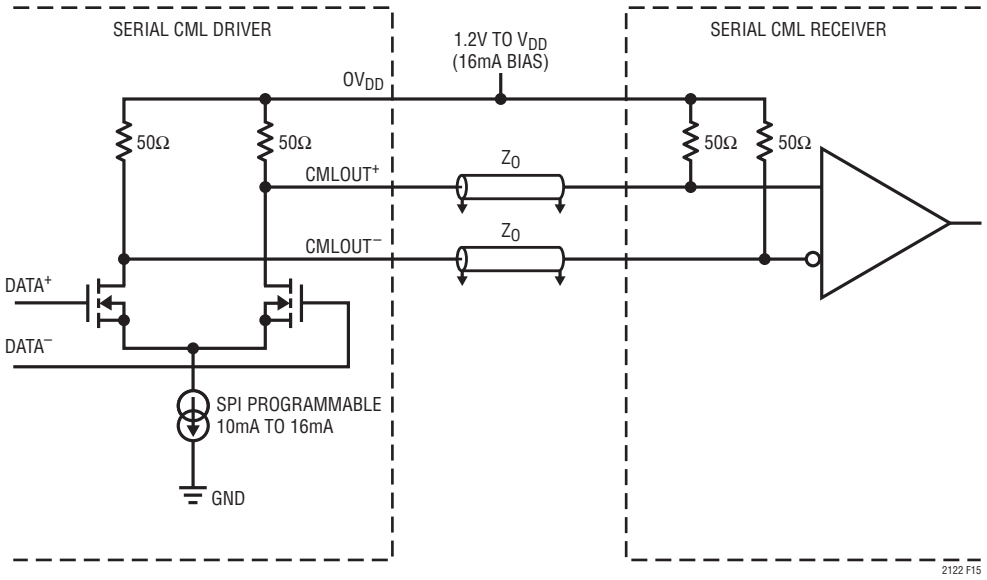


Figure 15. CML Termination, Directly Coupled Mode

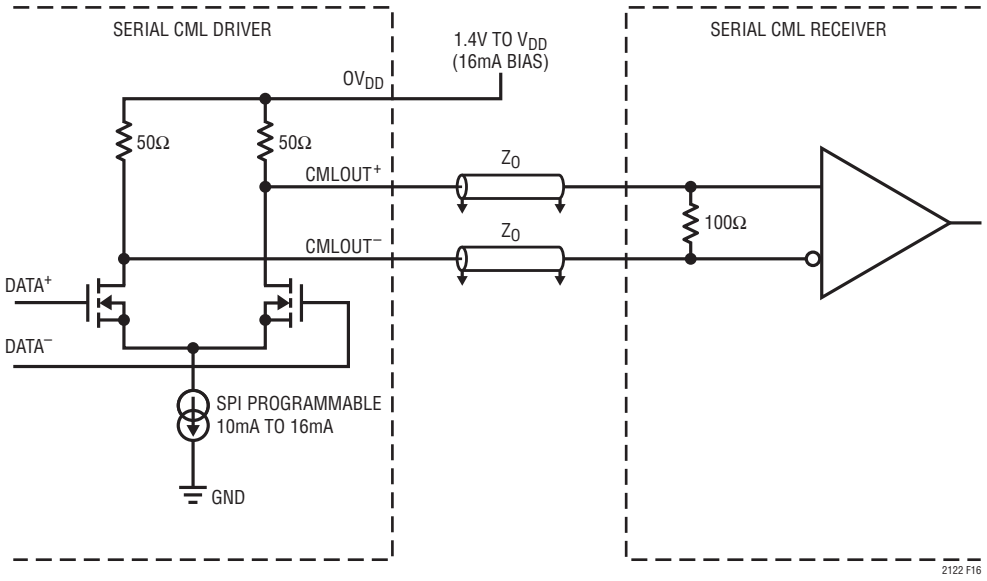


Figure 16. CML Termination, Directly Coupled Differential Mode

APPLICATIONS INFORMATION

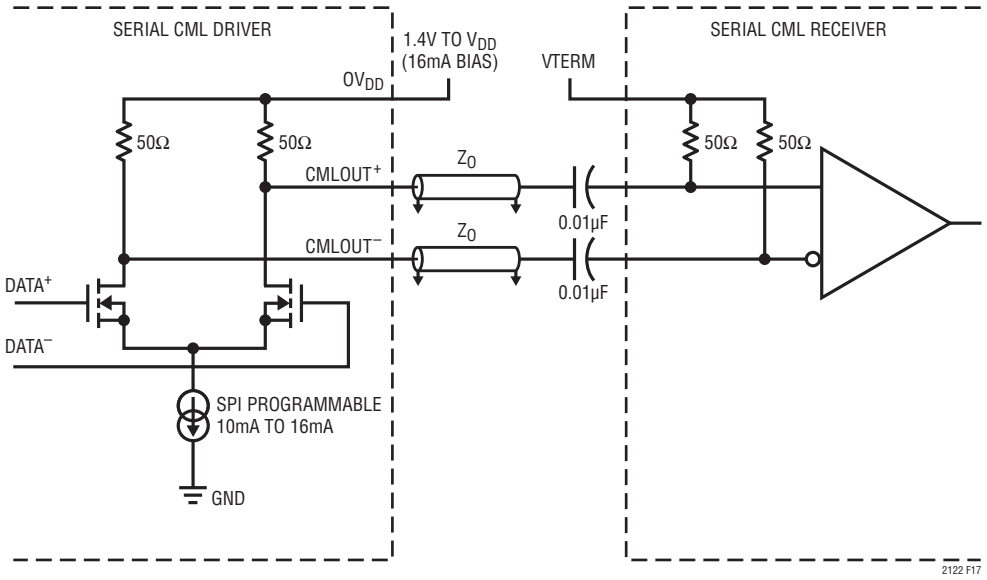


Figure 17. CML Termination, AC-Coupled Mode

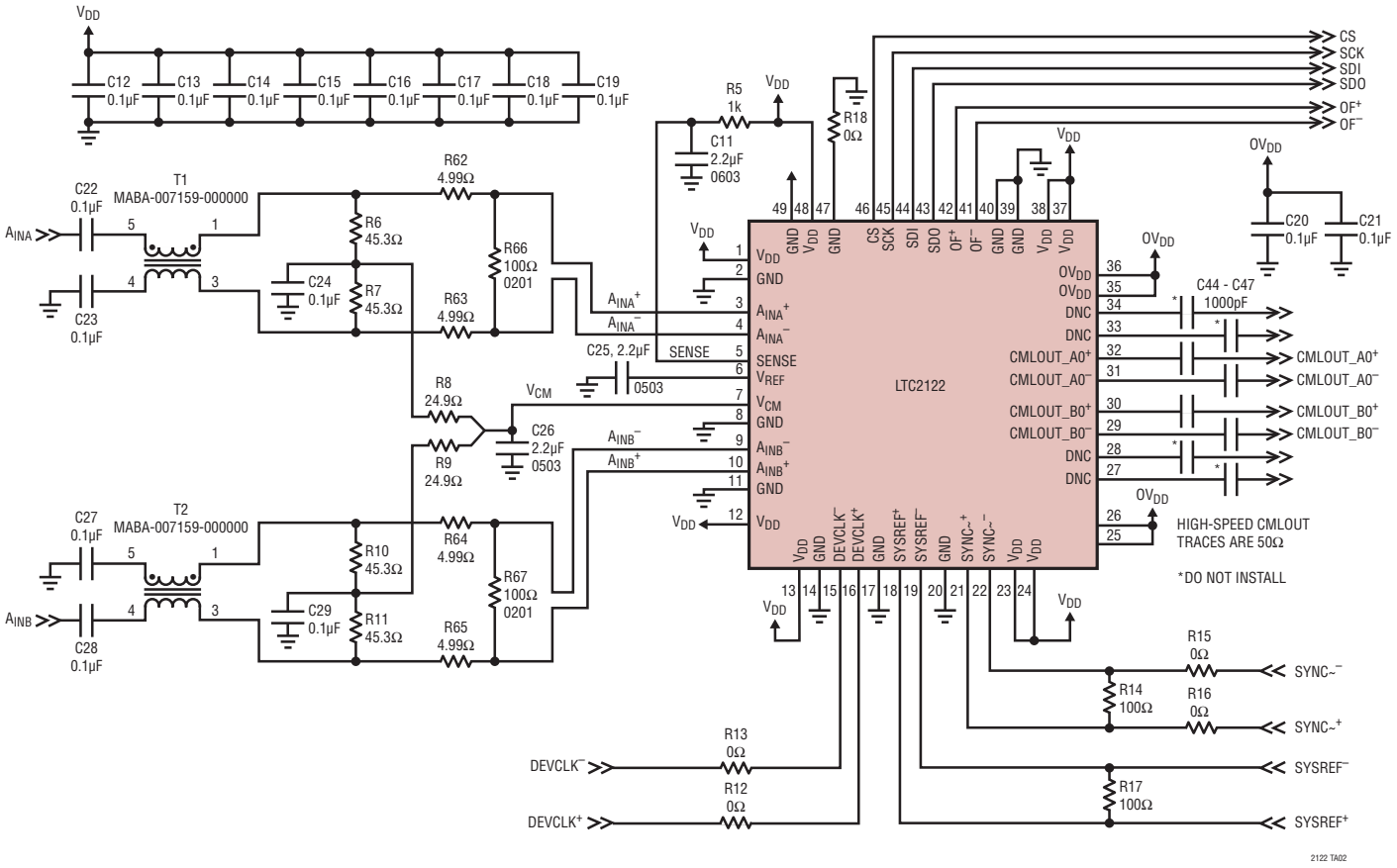
GROUNDING AND BYPASSING

The LTC2122 requires a printed circuit board with a clean and unbroken ground plane in the first layer beneath the ADC. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC. High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF} pins. Bypass capacitors must be located as close to the pins as possible. Size 0402 ceramic capacitors are recommended. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible. The analog inputs, clock signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

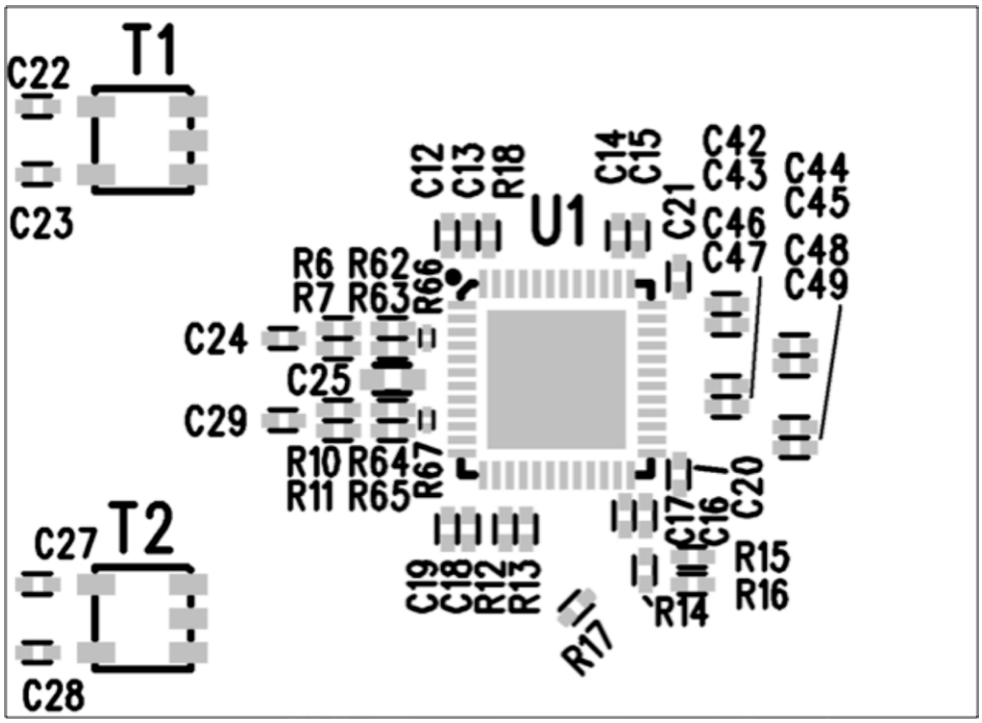
Most of the heat generated by the LTC2122 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board. This pad should be connected to the internal ground planes by an array of vias.

TYPICAL APPLICATIONS



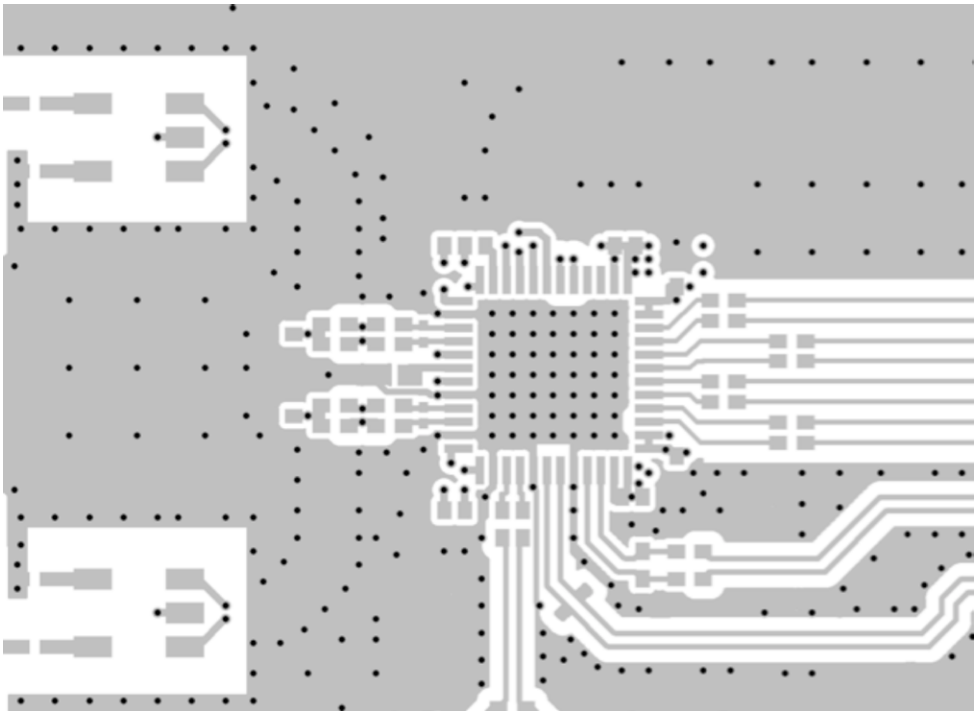
TYPICAL APPLICATIONS

Silkscreen Top

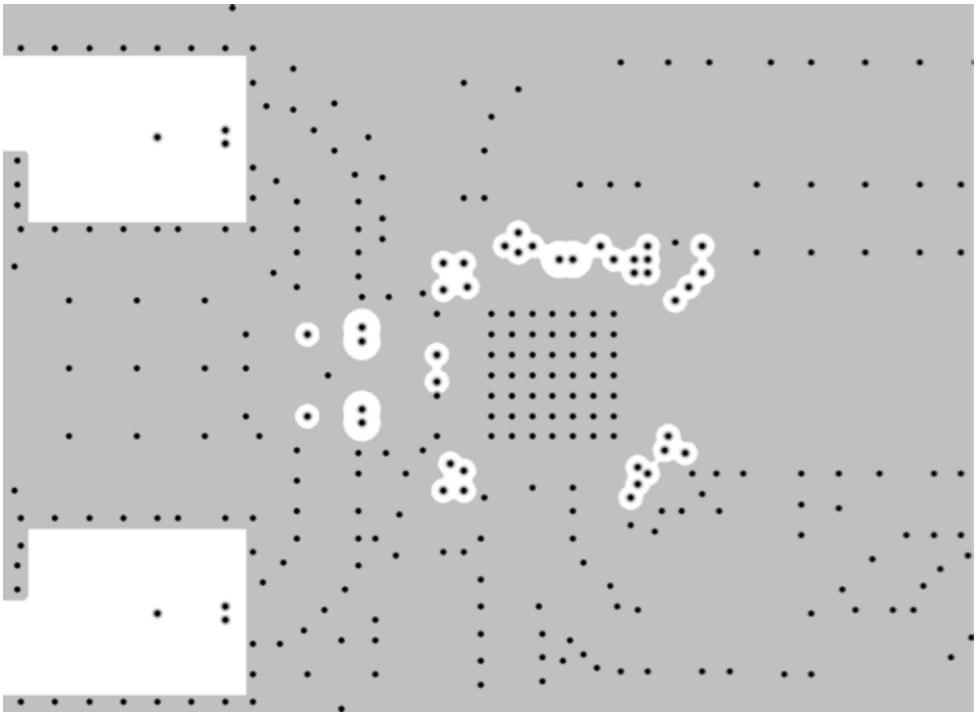


TYPICAL APPLICATIONS

Top Side

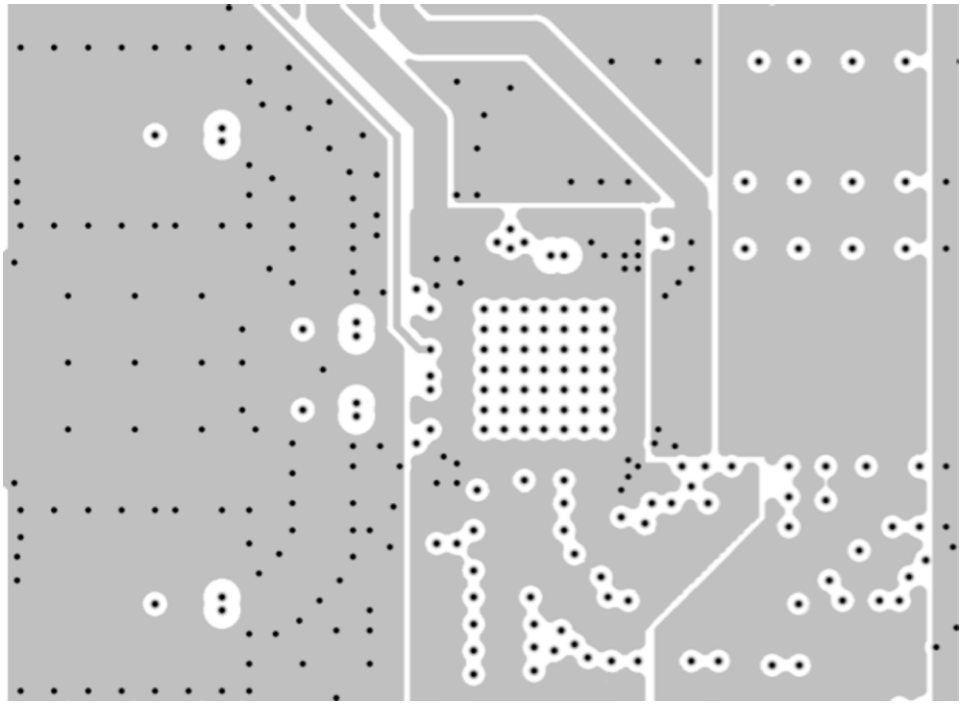


Inner Layer 2, GND

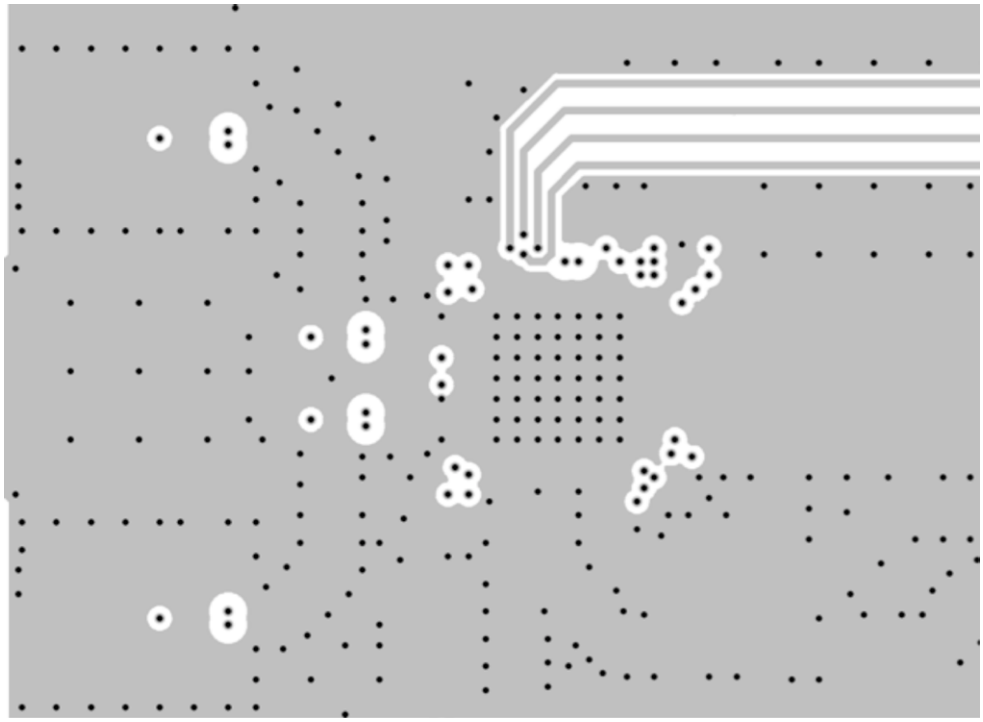


TYPICAL APPLICATIONS

Inner Layer 3

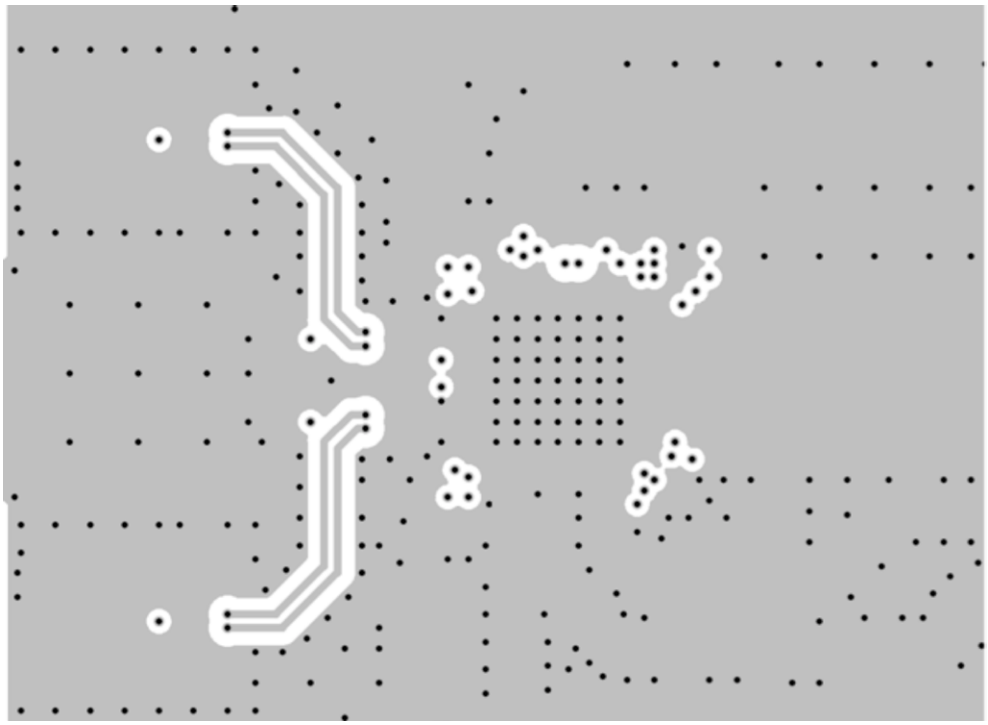


Inner Layer 4

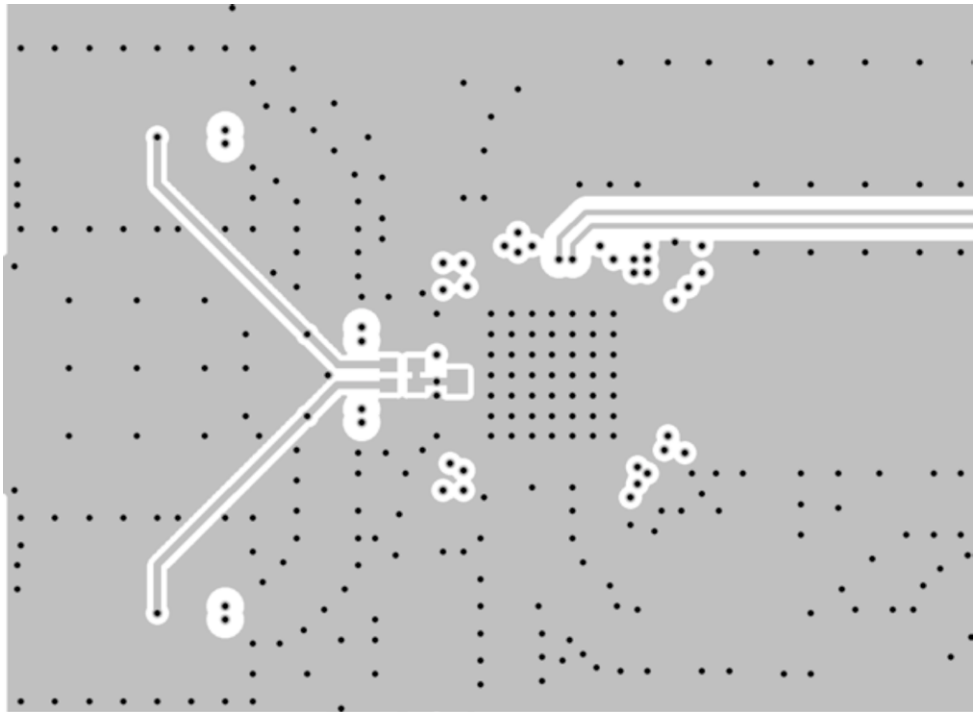


TYPICAL APPLICATIONS

Top Side



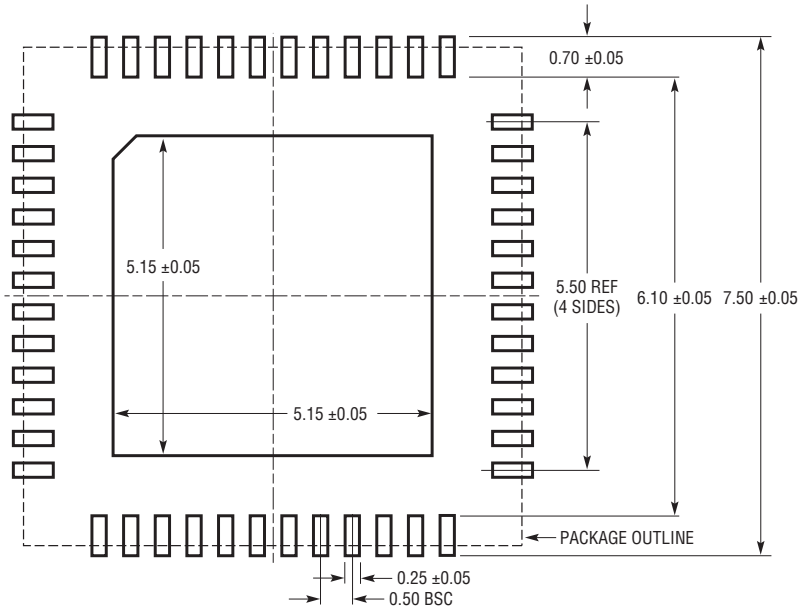
Inner Layer 2, GND



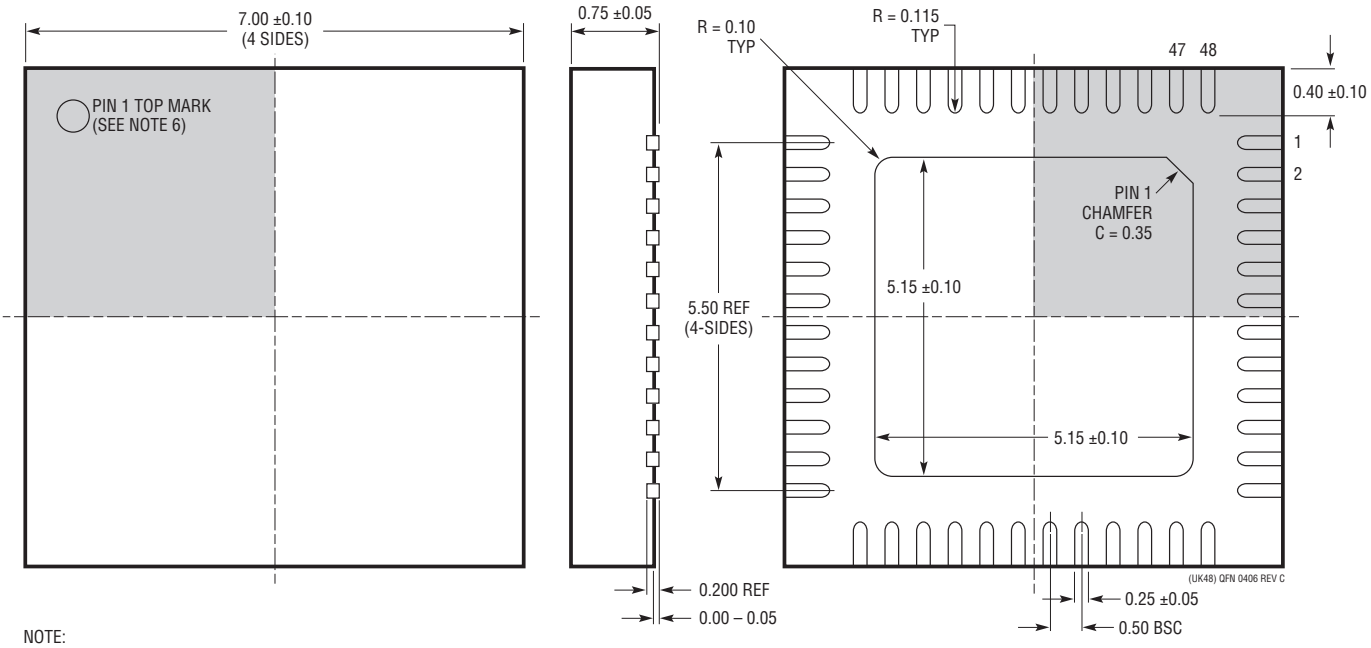
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UK Package
48-Lead Plastic QFN (7mm × 7mm)
(Reference LTC DWG # 05-08-1704 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



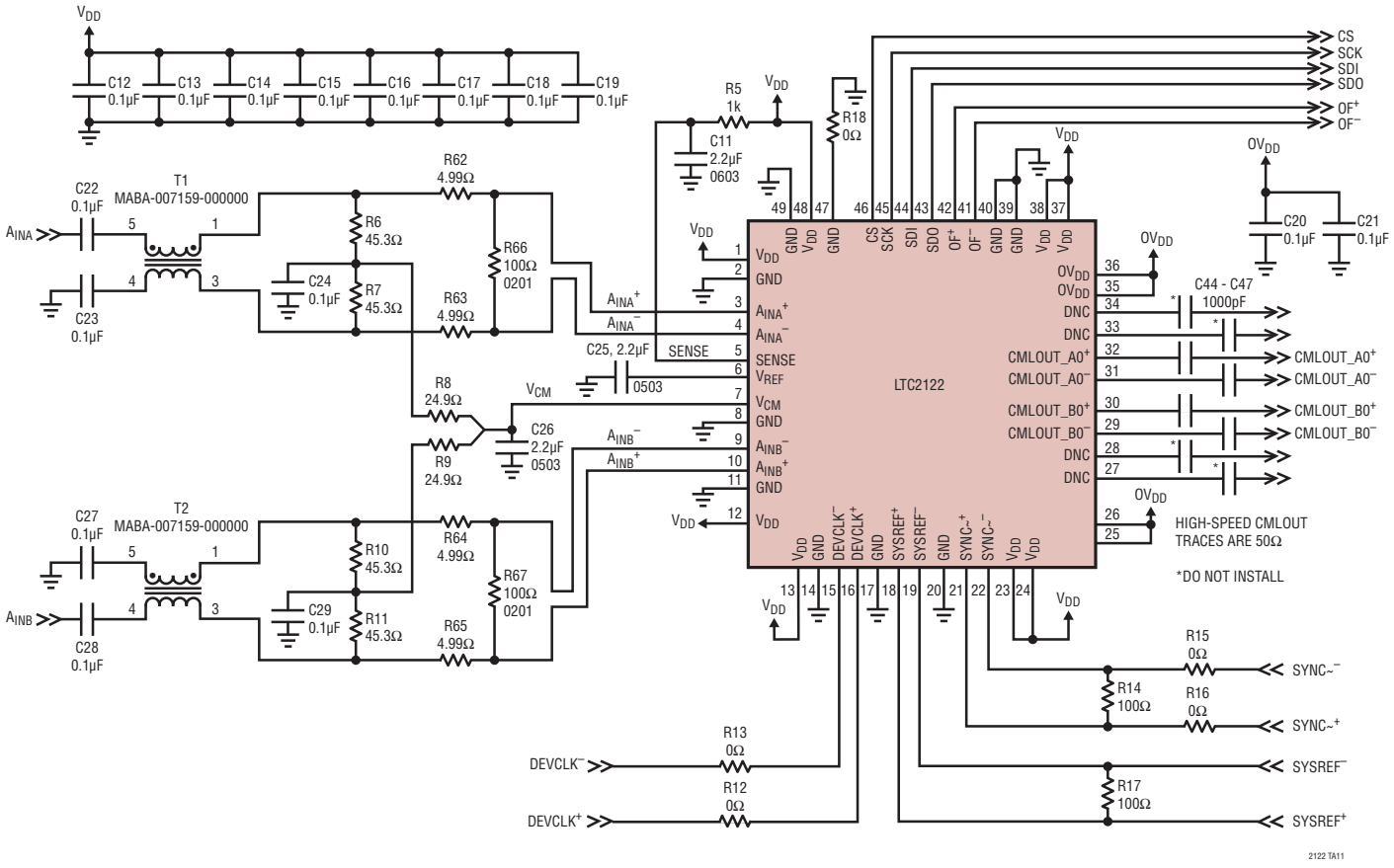
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WKKD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/14	Updated the crosstalk specification Added t_{DCK} specification Updated the t_{SU_SYS} and t_{H_SYS} specifications	3 5 6
B	09/15	Updated SPI Port Timing section Updated DEVCLK and $\overline{CS}$ pins description Updated Aperture Delay Time description Revised Long Transport Layer Text Pattern description	5, 15, 36 10, 11 16 35, 37 and 40

TYPICAL APPLICATION



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2123	14-bit, 250Msps 1.8V Dual ADC, JESD204B Serial Outputs	864mW, 70dB SNR, 90dB SFDR, 7mm × 7mm QFN Package, 5Gbps JESD204B Serial Interface
LTC2158-14	14-Bit 310Msps 1.8V Dual ADC, DDR LVDS Outputs	724mW, 68.8dB SNR, 88dB SFDR, 9mm × 9mm QFN Package
LTC2157-14/ LTC2156-14/ LTC2155-14	14-Bit, 250Msps/210Msps/170Msps, 1.8V Dual ADC, DDR LVDS Outputs	650mW/616mW/567mW, 70dB SNR, 90dB SFDR, 9mm × 9mm QFN Package
LTC2274	16-bit 105Msps 3.3V Single ADC with JESD204 Serial Outputs	1300mW, 77.6dB SNR, 100dB SFDR, 6mm × 6mm QFN Package
Receiver Subsystems		
LTM®9013	300MHz Wideband Receiver	Integrated I/Q Demodulator, IF Amplifier, and Dual 14-Bit, 310Msps High Speed ADC, 15mm × 15mm BGA Package

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