

LTC1864/LTC1865

µPower, 16-Bit, 250ksps 1- and 2-Channel ADCs in MSOP

FEATURES

- 16-Bit 250ksps ADCs in MSOP Package
- Single 5V Supply
- Low Supply Current: 850µA (Typ)
- Auto Shutdown Reduces Supply Current to 2µA at 1ksps
- True Differential Inputs
- 1-Channel (LTC1864) or 2-Channel (LTC1865) Versions
- SPI/MICROWIRE[™] Compatible Serial I/O
- 16-Bit Upgrade to 12-Bit LTC1286/LTC1298
- Pin Compatible with 12-Bit LTC1860/LTC1861
- Guaranteed Operation to +125°C (MSOP Package)

APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power Battery-Operated Instrumentation
- Isolated and/or Remote Data Acquisition

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DESCRIPTION

The LTC®1864/LTC1865 are 16-bit A/D converters that are offered in MSOP and SO-8 packages and operate on a single 5V supply. At 250ksps, the supply current is only 850µA. The supply current drops at lower speeds because the LTC1864/LTC1865 automatically power down between conversions. These 16-bit switched capacitor successive approximation ADCs include sample-andholds. The LTC1864 has a differential analog input with an adjustable reference pin. The LTC1865 offers a softwareselectable 2-channel MUX and an adjustable reference pin on the MSOP version.

The 3-wire, serial I/O, small MSOP or SO-8 package and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans down to 1V full scale, allow direct connection to signal sources in many applications, eliminating the need for external gain stages.

TYPICAL APPLICATION

Single 5V Supply, 250ksps, 16-Bit Sampling ADC









ABSOLUTE MAXIMUM RATINGS

Ground Voltage Difference	
AGND, DGND LTC1865 MSOP Package ±0.3	/
Analog Input (GND – 0.3V) to (V _{CC} + 0.3V)
Digital Input (GND – 0.3V) to 7V	/
Digital Output (GND – 0.3V) to (V_{CC} + 0.3V)
Power Dissipation 400mW	/

(Notes 1, 2)

Operating Temperature Range	
LTC1864C/LTC1865C/	
LTC1864AC/LTC1865AC0°C to 7	′0°C
LTC1864I/LTC1865I/	
LTC1864AI/LTC1865AI40°C to 8	35°C
LTC1864H/LTC1865H	
LTC1864AH/LTC1865AH40°C to 12	25°C
Storage Temperature Range65°C to 15	50°C
Lead Temperature (Soldering, 10 sec)30)0°C

PIN CONFIGURATION



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1864CMS8#PBF	LTC1864CMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864IMS8#PBF	LTC1864IMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	-40°C to 85°C
LTC1864HMS8#PBF	LTC1864HMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	-40°C to 125°C
LTC1864ACMS8#PBF	LTC1864ACMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864AIMS8#PBF	LTC1864AIMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	-40°C to 85°C
LTC1864AHMS8#PBF	LTC1864AHMS8#TRPBF	LTHQ	8-Lead Plastic MSOP	-40°C to 125°C
LTC1864CS8#PBF	LTC1864CS8#TRPBF	1864	8-Lead Plastic SO	0°C to 70°C
LTC1864IS8#PBF	LTC1864IS8#TRPBF	18641	8-Lead Plastic SO	-40°C to 85°C
LTC1864ACS8#PBF	LTC1864ACS8#TRPBF	1864A	8-Lead Plastic SO	0°C to 70°C
LTC1684AIS8#PBF	LTC1684AIS8#TRPBF	1864AI	8-Lead Plastic SO	-40°C to 85°C
LTC1865CMS#PBF	LTC1865CMS#TRPBF	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865IMS#PBF	LTC1865IMS#TRPBF	LTHS	10-Lead Plastic MSOP	-40°C to 85°C



ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1865HMS#PBF	LTC1865HMS#TRPBF	LTHS	10-Lead Plastic MSOP	-40°C to 125°C
LTC1865ACMS#PBF	LTC1865ACMS#TRPBF	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865AIMS#PBF	LTC1865AIMS#TRPBF	LTHS	10-Lead Plastic MSOP	-40°C to 85°C
LTC1865AHMS#PBF	LTC1865AHMS#TRPBF	LTHS	10-Lead Plastic MSOP	-40°C to 125°C
LTC1865CS8#PBF	LTC1865CS8#TRPBF	1865	8-Lead Plastic SO	0°C to 70°C
LTC1865IS8#PBF	LTC1865IS8#TRPBF	18651	8-Lead Plastic SO	-40°C to 85°C
LTC1865ACS8#PBF	LTC1865ACS8#TRPBF	1865A	8-Lead Plastic SO	0°C to 70°C
LTC1865AIS8#PBF	LTC1865AIS8#TRPBF	1865AI	8-Lead Plastic SO	-40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1864CMS8	LTC1864CMS8#TR	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864IMS8	LTC1864IMS8#TR	LTHQ	8-Lead Plastic MSOP	-40°C to 85°C
LTC1864HMS8	LTC1864HMS8#TR	LTHQ	8-Lead Plastic MSOP	-40°C to 125°C
LTC1864ACMS8	LTC1864ACMS8#TR	LTHQ	8-Lead Plastic MSOP	0°C to 70°C
LTC1864AIMS8	LTC1864AIMS8#TR	LTHQ	8-Lead Plastic MSOP	-40°C to 85°C
LTC1864AHMS8	LTC1864AHMS8#TR	LTHQ	8-Lead Plastic MSOP	-40°C to 125°C
LTC1864CS8	LTC1864CS8#TR	1864	8-Lead Plastic SO	0°C to 70°C
LTC1864IS8	LTC1864IS8#TR	18641	8-Lead Plastic SO	-40°C to 85°C
LTC1864ACS8	LTC1864ACS8#TR	1864A	8-Lead Plastic SO	0°C to 70°C
LTC1684AIS8	LTC1684AIS8#TR	1864AI	8-Lead Plastic SO	-40°C to 85°C
LTC1865CMS	LTC1865CMS#TR	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865IMS	LTC1865IMS#TR	LTHS	10-Lead Plastic MSOP	-40°C to 85°C
LTC1865HMS	LTC1865HMS#TR	LTHS	10-Lead Plastic MSOP	-40°C to 125°C
LTC1865ACMS	LTC1865ACMS#TR	LTHS	10-Lead Plastic MSOP	0°C to 70°C
LTC1865AIMS	LTC1865AIMS#TR	LTHS	10-Lead Plastic MSOP	-40°C to 85°C
LTC1865AHMS	LTC1865AHMS#TR	LTHS	10-Lead Plastic MSOP	-40°C to 125°C
LTC1865CS8	LTC1865CS8#TR	1865	8-Lead Plastic SO	0°C to 70°C
LTC1865IS8	LTC1865IS8#TR	18651	8-Lead Plastic SO	-40°C to 85°C
LTC1865ACS8	LTC1865ACS8#TR	1865A	8-Lead Plastic SO	0°C to 70°C
LTC1865AIS8	LTC1865AIS8#TR	1865AI	8-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/ For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/



CONVERTER AND MULTIPILEXER CHARACTERISTICS

The \bullet denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}C$. V_{CC} = 5V, V_{REF} = 5V, f_{SCK} = f_{SCK(MAX)} as defined in Recommended Operating Conditions, unless otherwise noted.

			LTC1864/LTC1865			LTC1864A/LTC1865A				
PARAMETER	CONDITIONS		MIN	ТҮР	MAX	MIN	ТҮР	MAX	UNITS	
Resolution		•	16			16			Bits	
No Missing Codes Resolution		•	14			15			Bits	
INL	Note 3) I-Grade (Note 3)				±8 ±8.5			±6 ±6.5	LSB LSB	
Transition Noise				1.1			1.1		LSB _{RMS}	
Gain Error		•			±20			±20	mV	
Offset Error	LTC1864 SO-8 and MSOP, LTC1865 MSOP LTC1865 SO-8	•		±2 ±3	±5 ±7		±2 ±3	±5 ±7	mV mV	
Input Differential Voltage Range	$V_{IN} = IN^+ - IN^-$	•	0		V _{REF}	0		V _{REF}	V	
Absolute Input Range	IN ⁺ Input IN [−] Input		-0.05 -0.05		V _{CC} + 0.05 V _{CC} /2	-0.05 -0.05		V _{CC} + 0.05 V _{CC} /2	V V	
V _{REF} Input Range	LTC1864 SO-8 and MSOP, LTC1865 MSOP		1		V _{CC}	1		V _{CC}	V	
Analog Input Leakage Current	(Note 4)	•			±1			±1	μA	
C _{IN} Input Capacitance	In Sample Mode During Conversion			12 5			12 5		pF pF	

DYNAMIC ACCURACY

 $T_A = 25^{\circ}C$. $V_{CC} = 5V$, $V_{REF} = 5V$, $f_{SAMPLE} = 250kHz$, unless otherwise noted.

			LTC	LTC1864/LTC1865			
SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS	
SNR	Signal-to-Noise Ratio			87		dB	
S/(N + D)	Signal-to-Noise Plus Distortion Ratio	10kHz Input Signal 100kHz Input Signal	83 76			dB dB	
THD	Total Harmonic Distortion Up to 5th Harmonic	10kHz Input Signal 100kHz Input Signal	88 77			dB dB	
	Full Power Bandwidth			20		MHz	
	Full Linear Bandwidth	$S/(N+D) \ge 75dB$		125		kHz	



DIGITAL AND DC ELECTRICAL CHARACTERISTICS The • denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^{\circ}C$. $V_{CC} = 5V$, $V_{REF} = 5V$, unless otherwise noted.

			LTC1864/LTC1865				
SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
V _{IH}	High Level Input Voltage	V _{CC} = 5.25V		2.4			V
V _{IL}	Low Level Input Voltage	V _{CC} = 4.75V				0.8	V
I _{IH}	High Level Input Current	V _{IN} = V _{CC}	•			2.5	μA
IIL	Low Level Input Current	V _{IN} = 0V				-2.5	μA
V _{OH}	High Level Output Voltage	V _{CC} = 4.75V, I _O = 10μA V _{CC} = 4.75V, I _O = 360μA	•	4.5 2.4	4.74 4.72		V V
V _{OL}	Low Level Output Voltage	V _{CC} = 4.75V, I _O = 1.6mA	•			0.4	V
I _{OZ}	Hi-Z Output Leakage	CONV = V _{CC}	•			±3	μA
I _{SOURCE}	Output Source Current	V _{OUT} = 0V			-25		mA
I _{SINK}	Output Sink Current	$V_{OUT} = V_{CC}$			20		mA
I _{REF}	Reference Current (LTC1864 SO-8 and MSOP, LTC1865 MSOP)	CONV = VCC f _{SMPL} = f _{SMPL(MAX)}	•		0.001 0.05	3 0.1	μA mA
I _{CC}	Supply Current	CONV = V _{CC} After Conversion CONV = V _{CC} After Conversion, H-Grade f _{SMPL} = f _{SMPL(MAX)}	•		0.001 0.001 0.85	3 5 1.3	μΑ μΑ mA
P _D	Power Dissipation	$f_{SMPL} = f_{SMPL(MAX)}$			4.25		mW

RECOMMENDED OPERATING CONDITIONS The \bullet denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^{\circ}C$.

			LTC1864				
SYMBOL	PARAMETER	CONDITIONS		MIN	ТҮР	MAX	UNITS
V _{CC}	Supply Voltage			4.75		5.25	V
f _{SCK}	Clock Frequency	H-Grade	•			20 16.7	MHz MHz
t _{CYC}	Total Cycle Time			16 • SCK + t _{CONV}			μs
t _{SMPL}	Analog Input Sampling Time	LTC1864 (Note 5) LTC1865 (Note 5)		16 14			SCK SCK
t _{suCONV}	Setup Time CONV↓ Before First SCK↑ (See Figure 1)	H-Grade		60 65	30 30		ns ns
t _{hDI}	Hold Time SDI After SCK↑	LTC1865		15			ns
t _{suDI}	Setup Time SSDI Stable Before SCK↑	LTC1865		15			ns
t _{WHCLK}	SCK High Time	$f_{SCK} = f_{SCK(MAX)}$		40%			1/f _{SCK}
t _{WLCLK}	SCK Low Time	$f_{SCK} = f_{SCK(MAX)}$		40%			1/f _{SCK}
twhconv	CONV High Time Between Data Transfer Cycles	(Note 5)		t _{CONV}			μs
t _{WLCONV}	CONV Low Time During Data Transfer	(Note 5)		16			SCK
t _{hCONV}	Hold Time CONV Low After Last SCK↑				13		ns



TIMING CHARACTERISTICS The • denotes specifications which apply over the full operating temperature range, otherwise specifications are $T_A = 25^{\circ}$ C. $V_{CC} = 5$ V, $V_{REF} = 5$ V, $f_{SCK} = f_{SCK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

			LTC18				
SYMBOL	PARAMETER	CONDITIONS	MIN	ТҮР	MAX	UNITS	
t _{CONV}	Conversion Time (See Figure 1)	H-Grade	•		2.75 2.75	3.2 3.3	μs μs
f _{SMPL(MAX)}	Maximum Sampling Frequency	H-Grade	•	250 234			kHz kHz
t _{dDO}	Delay Time, SCK↓ to SDO Data Valid	C _{LOAD} = 20pF C _{LOAD} = 20pF C _{LOAD} = 20pF, H-Grade	•		15	20 25 30	ns ns ns
t _{dis}	Delay Time, CONV↑ to SDO Hi-Z	H-Grade	•		30 30	60 65	ns ns
t _{en}	Delay Time, CONV↓ to SDO Enabled	C _{LOAD} = 20pF C _{LOAD} = 20pF, H-Grade	•		30 30	60 65	ns ns
t _{hDO}	Time Output Data Remains Valid After SCK↓	C _{LOAD} = 20pF	•	5	10		ns
t _r	SDO Rise Time	C _{LOAD} = 20pF			8		ns
t _f	SDO Fall Time	C _{LOAD} = 20pF			4		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Channel leakage current is measured while the part is in sample mode.

Note 5: Guaranteed by design, not subject to test.



TYPICAL PERFORMANCE CHARACTERISTICS





TYPICAL PERFORMANCE CHARACTERISTICS







Change in Gain Error vs Temperature



Histogram of 4096 Conversions of a DC Input Voltage



4096 Point FFT Nonaveraged



SINAD vs Frequency 100 90 SNR 80 70 SINAD 60 SINAD (dB) 50 40 30 i II∏ V_{CC} = 5V 20 $V_{REF} = 5V$ $T_A = 25^{\circ}C$ $V_{IN} = 0dB$ 10 0 1 10 100 1000 F_{IN} (kHz) 18645 G16

THD vs Frequency



SFDR vs Frequency





PIN FUNCTIONS

LTC1864

 V_{REF} (Pin 1): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

IN⁺, IN⁻ (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

CONV (Pin 5): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part

LTC1865 (MSOP Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CHO, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to AGND.

AGND (Pin 4): Analog Ground. AGND should be tied directly to an analog ground plane.

DGND (Pin 5): Digital Ground. DGND should be tied directly to an analog ground plane.

SDI (Pin 6): Digital Data Input. The A/D configuration word is shifted into this input.

LTC1865 (SO-8 Package)

CONV (Pin 1): Convert Input. A logic high on this input starts the A/D conversion process. If the CONV input is left high after the A/D conversion is finished, the part powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

CHO, **CH1** (**Pins 2, 3**): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

powers down. A logic low on this input enables the SDO pin, allowing the data to be shifted out.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this pin.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

 V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

SDO (Pin 7): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 8): Shift Clock Input. This clock synchronizes the serial data transfer.

V_{CC} (Pin 9): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

V_{REF} (Pin 10): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to AGND.

SDI (Pin 5): Digital Data Input. The A/D configuration word is shifted into this input.

SDO (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

SCK (Pin 7): Shift Clock Input. This clock synchronizes the serial data transfer.

 V_{CC} (Pin 8): Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. V_{REF} is tied internally to this pin.





FUNCTIONAL BLOCK DIAGRAM





LTC1864/LTC1865

TEST CIRCUITS

Load Circuit for $t_{dDO},\,t_r^{},\,t_f^{},\,t_{dis}^{}$ and $t_{en}^{}$



Voltage Waveforms for ten



Voltage Waveforms for SDO Delay Times, t_{dDO} and t_{hDO}



Voltage Waveforms for SDO Rise and Fall Times, t_r , t_f







NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL 18645 TODS



LTC1864 OPERATION

Operating Sequence

The LTC1864 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV} , the conversion is finished. If CONV is left high after this time, the LTC1864 goes into sleep mode drawing only leakage current. On the falling edge of CONV, the LTC1864 goes into sample mode and SDO is enabled. SCK synchronizes the data transfer with each bit being transmitted from SDO on the falling SCK edge. The receiving system should capture the data from SDO on the rising edge of SCK. After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 1.

Analog Inputs

The LTC1864 has a unipolar differential analog input. The converter will measure the voltage between the "IN+" and "IN⁻" inputs. A zero code will occur when IN⁺ minus IN⁻ equals zero. Full scale occurs when IN⁺ minus IN⁻ equals V_{REF} minus 1LSB. See Figure 2. Both the "IN+" and "IN⁻" inputs are sampled at the same time, so common mode noise on the inputs is rejected by the ADC. If "IN⁻" is grounded and V_{REF} is tied to V_{CC}, a rail-to-rail input span will result on "IN⁺" as shown in Figure 3.

Reference Input

The voltage on the reference input of the LTC1864 defines the full-scale range of the A/D converter. The LTC1864 can operate with reference voltages from V_{CC} to 1V.













LTC1865 OPERATION

Operating Sequence

The LTC1865 conversion cycle begins with the rising edge of CONV. After a period equal to t_{CONV} , the conversion is finished. If CONV is left high after this time, the LTC1865 goes into sleep mode drawing only leakage current. The LTC1865's 2-bit data word is clocked into the SDI input on the rising edge of SCK after CONV goes low. Additional inputs on the SDI pin are then ignored until the next CONV cycle. The shift clock (SCK) synchronizes the data transfer with each bit being transmitted on the falling SCK edge and captured on the rising SCK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex). After completing the data transfer, if further SCK clocks are applied with CONV low, SDO will output zeros indefinitely. See Figure 4.

Analog Inputs

The two bits of the input word (SDI) assign the MUX configuration for the next requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "-" signs in the selected row of the following table. In

single-ended mode, all input channels are measured with respect to GND. A zero code will occur when the "+" input minus the "-" input equals zero. Full scale occurs when the "+" input minus the "-" input equals V_{REF} minus 1LSB. See Figure 5. Both the "+" and "-" inputs are sampled at the same time so common mode noise is rejected. The input span in the SO-8 package is fixed at $V_{REF} = V_{CC}$. If the "-" input in differential mode is grounded, a rail-to-rail input span will result on the "+" input.

Reference Input

The reference input of the LTC1865 SO-8 package is internally tied to V_{CC}. The span of the A/D converter is therefore equal to V_{CC}. The voltage on the reference input of the LTC1865 MSOP package defines the span of the A/D converter. The LTC1865 MSOP package can operate with reference voltages from 1V to V_{CC}.

	Table 1. Multiplexer Channel Selection					
	MUX AI	CHAN	NEL #			
	SGL/DIFF	ODD/SIGN	0	1	GND	
SINGLE-ENDED	1	0	+		-	
MUX MODE [1	1		+	_	
DIFFERENTIAL	0	0	+	_		
MUX MODE	0	1	_	+		
					18645 TBL1	



Figure 4. LTC1865 Operating Sequence

18645 F04



GENERAL ANALOG CONSIDERATIONS

Grounding

The LTC1864/LTC1865 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a printed circuit board. The ground pins (AGND and DGND for the LTC1865 MSOP package and GND for the LTC1864 and LTC1865 SO-8 package) should be tied directly to the analog ground plane with minimum lead length.

Bypassing

For good performance, the V_{CC} and V_{REF} pins must be free of noise and ripple. Any changes in the V_{CC}/V_{REF} voltage with respect to ground during the conversion cycle can

induce errors or noise in the output code. Bypass the V_{CC} and V_{REF} pins directly to the analog ground plane with a minimum of $1\mu F$ tantalum. Keep the bypass capacitor leads as short as possible.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1864/LTC1865 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200 Ω or high speed op amps are used (e.g., the LT®1211, LT1469, LT1807, LT1810, LT1630, LT1226 or LT1215). But if large source resistances are used, or if slow settling op amps drive the inputs, take care to ensure the transients caused by the current spikes settle completely before the conversion begins.



Figure 5. LTC1865 Transfer Curve



LTC1864/LTC1865

APPLICATIONS INFORMATION



LTC1864 Evaluation Circuit Schematic



18645fb

16



Component Side Silk Screen for LTC1864 Evaluation Circuit



Component Side Showing Traces (Note Sider Traces on Analog Side)



Ground Layer with Separate Analog and Digital Grounds



Bottom Side Showing Traces (Note Almost No Analog Traces on Board Bottom)



Supply Layer with 5V Digital Supply and Analog Ground Repeated





Figure 6. LTC1864 Manchester Transmitter





Figure 7. LTC1864 Manchester Receiver



Transmit LTC1864 Data Over Modular Telephone Wire Using Simple Transmitter/Receiver

Figure 6 shows a simple Manchester encoder and differential transmitter suitable for use with the LTC1864. This circuit allows transmission of data over inexpensive telephone wire. This is useful for measuring a remote sensor, particularly when the cost of preserving the analog signal over a long distance is high.

Manchester encoding is a clock signal that is modulated by exclusive ORing with the data signal. The resulting signal contains both clock and data information and has an average duty cycle of 50%, that also allows transformer coupling. In practice, generating a Manchester encoded signal with an XOR gate will often produce glitches due to the skew between data and clock transitions. The D flip-flops in this encoder retime the clock and data such that the respective edges are closely aligned, effectively suppressing glitches. The retimed data and clock are then XORed to produce the Manchester encoded data, which is interfaced to telephone wire with an LTC1485 RS485 transceiver.

In order to synchronize to incoming data, the receiver needs a sequence to indicate the start of a data word. The transmitter schematic shows logic that will produce 31 zeros, a start bit, followed by the 16 data bits (one sample every 48 clock cycles) at a clock frequency of 1MHz set by the LTC1799 oscillator. Sending at least 18 zeros before each start bit ensures that if synchronization is lost, the receiver can resynchronize to a start bit under all conditions. The serial to parallel converter shown in Figure 7 requires 18 zeros to avoid triggering on data bits.

The Manchester receiver shown in Figure 7 was adopted from Xilinx application note 17-30 and would typically be implemented in an FPGA. The decoder clock frequency is nominally 8 times the transmit clock frequency and is very tolerant of frequency errors. The outputs of the decoder are data and a strobe that indicates a valid data bit. The data can be deserialized using shift registers as shown. The start bit resets the J-K/flip-flop on its way into the first shift register. When it appears at the QH_{IN} output of the second shift register, it sets the flip-flop that loads the parallel data into the output register.

With AC family CMOS logic at 5V the receiver clock frequency is limited to 20MHz; the corresponding transmitter clock frequency is 2.5MHz. If the receiver is implemented in an FPGA that can be clocked at 160MHz, the LTC1864 can be clocked at its rated clock frequency of 20MHz.



PACKAGE DESCRIPTION



MS8 Package 8-Lead Plastic MSOP (Reference LTC DWG # 05-08-1660)

DIAWING NOT TO SOLL
DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX



LTC1864/LTC1865

PACKAGE DESCRIPTION



MS Package **10-Lead Plastic MSOP** (Reference LTC DWG # 05-08-1661)

3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE

5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX







PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)



*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE **DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD

FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE



TYPICAL APPLICATION

Sample Two Channels Simultaneously with a Single Input ADC



RELATED PARTS

PART NUMBER	SAMPLE RATE POWER DISSIPATION		DESCRIPTION			
14-Bit Serial I/O A	DCs					
LTC1417	400ksps	20mW	16-Pin SSOP, Unipolar or Bipolar, Reference, 5V or ±5V			
LTC1418	200ksps	15mW	Serial/Parallel I/O, Internal Reference, 5V or ±5V			
16-Bit Serial I/O ADCs						
LTC1609	200ksps	65mW	Configurable Bipolar or Unipolar Input Ranges, 5V			
References	ŀ					
LT1460	Micropower Precision	Series Reference	Bandgap, 130µA Supply Current, 10ppm/°C, Available in SOT-23			
LT1790	Micropower Low Drop	out Reference	60µA Supply Current, 10ppm/°C, SOT-23			
Op Amps						
LT1468/LT1469	Single/Dual 90MHz, 16-Bit Accurate Op Amps		22V/µs Slew Rate, 75µV/125µV Offset			
LT1806/LT1807	Single/Dual 325MHz L	ow Noise Op Amps	140V/µs Slew Rate, 3.5nV/√Hz Noise, -80dBc Distortion			
LT1809/LT1810	Single/Dual 180MHz L	ow Distortion Op Amps	350V/µs Slew Rate, –90dBc Distortion at 5MHz			



4096 Point FFT of Output

Mouser Electronics

Authorized Distributor

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Analog Devices Inc.:

LTC1864AHMS8#PBF LTC1864AIS8#TRPBF LTC1864IMS8#TRPBF LTC1864AIMS8#PBF LTC1864CMS8#TRPBF LTC1864ACMS8#TRPBF LTC1864ACMS8#PBF LTC1864AIMS8#TRPBF LTC1864AIS8#PBF LTC1864CS8#TRPBF LTC1864IS8#TRPBF LTC1864ACS8#TRPBF LTC1864ACS8#PBF LTC1864IS8#PBF LTC1864CS8#PBF LTC1864CMS8#PBF LTC1864HMS8#PBF LTC1864IMS8#PBF LTC1864AHMS8#TRPBF LTC1864HMS8#TRPBF DC416A