8-Bit, SO-8, 1Msps ADCs with Auto-Shutdown Options

FEATURES

- **High Sampling Rates: 1MHz (LTC1196)**
  750kHz (LTC1198)
- **Low Cost**
- Single Supply 3V and 5V Specifications
- Low Power: 10mW at 3V Supply
  50mW at 5V Supply
- Auto-Shutdown: 1nA Typical (LTC1198)
- ±1/2LSB Total Unadjusted Error over Temperature
- 3-Wire Serial I/O
- 1V to 5V Input Span Range (LTC1196)
- Converts 1MHz Inputs to 7 Effective Bits
- Differential Inputs (LTC1196)
- 2-Channel MUX (LTC1198)
- SO-8 Plastic Package

APPLICATIONS

- High Speed Data Acquisition
- Disk Drives
- Portable or Compact Instrumentation
- Low Power or Battery-Operated Systems

DESCRIPTION

The LTC®1196/LTC1198 are 600ns, 8-bit A/D converters with sampling rates up to 1MHz. They are offered in 8-pin SO packages and operate on 3V to 6V supplies. Power dissipation is only 10mW with a 3V supply or 50mW with a 5V supply. The LTC1198 automatically powers down to a typical supply current of 1nA whenever it is not performing conversions. These 8-bit switched-capacitor successive approximation ADCs include sample-and-holds. The LTC1196 has a differential analog input; the LTC1198 offers a software selectable 2-channel MUX.

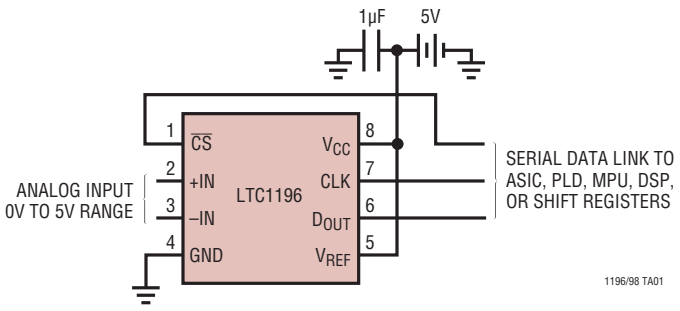
The 3-wire serial I/O, SO-8 packages, 3V operation and extremely high sample rate-to-power ratio make these ADCs an ideal choice for compact, high speed systems.

These ADCs can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans below 1V full scale (LTC1196) allow direct connection to signal sources in many applications, eliminating the need for gain stages.

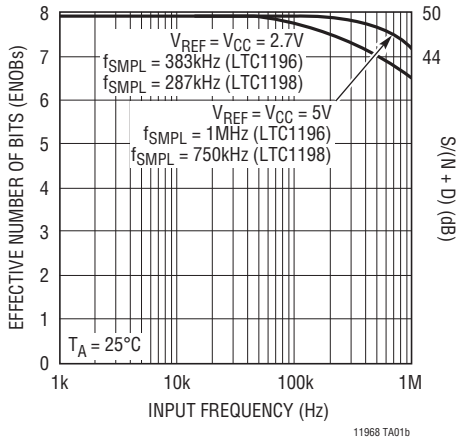
The A-grade devices are specified with total unadjusted error of ±1/2LSB maximum over temperature.

TYPICAL APPLICATION

Single 5V Supply, 1Msps, 8-Bit Sampling ADC



Effective Bits and S/(N + D) vs Input Frequency



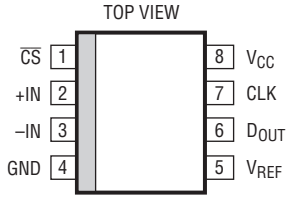
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) to GND 7V
Voltage
  Analog Reference ..... –0.3V to V_{CC} + 0.3V
  Digital Inputs ..... –0.3V to 7V
  Digital Outputs ..... –0.3V to V_{CC} + 0.3V
Power Dissipation 500mW

Operating Temperature Range
  LTC1196-1AC, LTC1198-1AC, LTC1196-1BC,
  LTC1198-1BC, LTC1196-2AC, LTC1198-2AC,
  LTC1196-2BC, LTC1198-2BC ..... 0°C to 70°C
Storage Temperature Range..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION

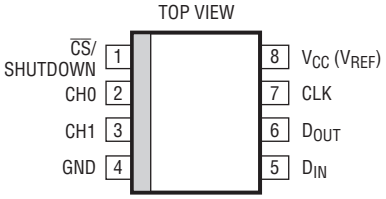
LTC1196



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

LTC1198



S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 150°C, θ_{JA} = 175°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1196-1ACS8#PBF	LTC1196-1ACS8#TRPBF	11961A	8-Lead Plastic SO	0°C to 70°C
LTC1196-1BCS8#PBF	LTC1196-1BCS8#TRPBF	11961B	8-Lead Plastic SO	0°C to 70°C
LTC1196-2ACS8#PBF	LTC1196-2ACS8#TRPBF	11962A	8-Lead Plastic SO	0°C to 70°C
LTC1196-2BCS8#PBF	LTC1196-2BCS8#TRPBF	11962B	8-Lead Plastic SO	0°C to 70°C
LTC1198-1ACS8#PBF	LTC1198-1ACS8#TRPBF	11981A	8-Lead Plastic SO	0°C to 70°C
LTC1198-1BCS8#PBF	LTC1198-1BCS8#TRPBF	11981B	8-Lead Plastic SO	0°C to 70°C
LTC1198-2ACS8#PBF	LTC1198-2ACS8#TRPBF	11982A	8-Lead Plastic SO	0°C to 70°C
LTC1198-2BCS8#PBF	LTC1198-2BCS8#TRPBF	11982B	8-Lead Plastic SO	0°C to 70°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage			2.7		6	2.7		6	V
V_{CC} = 5V Operation										
f_{CLK}	Clock Frequency		 ●	0.01 0.01		14.4 12.0	0.01 0.01		12.0 9.6	MHz MHz
t_{CYC}	Total Cycle Time	LTC1196 LTC1198		12 16			12 16			CLK CLK
t_{SMPL}	Analog Input Sampling Time			2.5			2.5			CLK
$t_{h\overline{CS}}$	Hold Time $\overline{CS}$ LOW After Last CLK↑			10			13			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1, 2)			20			26			ns
t_{hDI}	Hold Time D_{IN} After CLK↑	LTC1198		20			26			ns
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	LTC1198		20			26			ns
t_{WHCLK}	CLK HIGH Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
t_{WLCLK}	CLK LOW Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
$t_{WH\overline{CS}}$	$\overline{CS}$ HIGH Time Between Data Transfer Cycles			25			32			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ LOW Time During Data Transfer	LTC1196 LTC1198		11 15			11 15			CLK CLK

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, $f_{CLK} = f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1196-1A/LTC1196-2A LTC1198-1A/LTC1198-2A MIN	TYP	MAX	LTC1196-1B/LTC1196-2B LTC1198-1B/LTC1198-2B MIN	TYP	MAX	UNITS
No Missing Codes Resolution		●	8			8			Bits
Offset Error		●			±1/2			±1	LSB
Linearity Error	(Note 3)	●			±1/2			±1	LSB
Full-Scale Error		●			±1/2			±1	LSB
Total Unadjusted Error (Note 4)	LTC1196, V_{REF} = 5.000V LTC1198, V_{CC} = 5.000V	●			±1/2			±1	LSB
Analog and REF Input Range	LTC1196			–0.05V to V_{CC} + 0.05V					V
Analog Input Leakage Current	(Note 5)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_O = 10µA V_{CC} = 4.75V, I_O = 360µA	● ●	4.5 2.4	4.74 4.71		V V

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_O = 1.6mA	●			0.4	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = HIGH	●			±3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–25		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			45		mA
I_{REF}	Reference Current, LTC1196	$\overline{CS}$ = V_{CC} f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.001 0.5	3 1	µA mA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC}, LTC1198 (Shutdown) $\overline{CS}$ = V_{CC}, LTC1196 f_{SMPL} = $f_{SMPL(MAX)}$, LTC1196/LTC1198	● ● ●		0.001 7 11	3 15 20	µA mA mA

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196 MIN	LTC1196 TYP	LTC1196 MAX	LTC1198 MIN	LTC1198 TYP	LTC1198 MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion	500kHz/1MHz Input Signal			47/45			47/45		dB
THD	Total Harmonic Distortion	500kHz/1MHz Input Signal			49/47			49/47		dB
	Peak Harmonic or Spurious Noise	500kHz/1MHz Input Signal			55/48			55/48		dB
IMD	Intermodulation Distortion	f_{IN1} = 499.37kHz f_{IN2} = 502.446kHz			51			51		dB
	Full-Power Bandwidth				8			8		MHz
	Full Linear Bandwidth [S/(N + D) > 44dB				1			1		MHz

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V, V_{REF} = 5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
t_{CONV}	Conversion Time (See Figures 1, 2)		 ●			600 710			710 900	ns ns
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1196 LTC1196 LTC1198 LTC1198	 ● ●	1.20 1.00 0.90 0.75			1.00 0.80 0.75 0.60			MHz MHz MHz MHz
t_{dDO}	Delay Time, CLK↑ to D_{OUT} Data Valid	C_{LOAD} = 20pF	 ●		55	64 73		68	78 94	ns ns
t_{DIS}	Delay Time $\overline{CS}$↑ to D_{OUT} Hi-Z		●		70	120		88	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 20pF	●		30	50		43	63	ns
t_{hDO}	Time Output Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	30	45		30	55		ns
t_f	D_{OUT} Fall Time	C_{LOAD} = 20pF	●		5	15		10	20	ns
t_r	D_{OUT} Rise	C_{LOAD} = 20pF	●		5	15		10	20	ns
C_{IN}	Input Capacitance	Analog Input On Channel Analog Input Off Channel Digital Input			30 5 5			30 5 5		pF pF pF

RECOMMENDED OPERATING CONDITIONS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V operation.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	TYP	MAX	LTC1196-2 LTC1198-2 MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency		 ●	0.01 0.01		5.4 4.6	0.01 0.01		4 3	MHz MHz
t_{CYC}	Total Cycle Time	LTC1196 LTC1198		12 16			12 16			CLK CLK
t_{SMPL}	Analog Input Sampling Time			2.5			2.5			CLK
$t_{h\overline{CS}}$	Hold Time $\overline{CS}$ LOW After Last CLK↑			20			40			ns
$t_{su\overline{CS}}$	Setup Time $\overline{CS}$↓ Before First CLK↑ (See Figures 1, 2)			40			78			ns
t_{hDI}	Hold Time D_{IN} After CLK↑	LTC1198		40			78			ns
t_{suDI}	Setup Time D_{IN} Stable Before CLK↑	LTC1198		40			78			ns
t_{WHCLK}	CLK HIGH Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
t_{WLCLK}	CLK LOW Time	$f_{CLK} = f_{CLK(MAX)}$		40%			40%			$1/f_{CLK}$
$t_{WH\overline{CS}}$	$\overline{CS}$ HIGH Time Between Data Transfer Cycles			50			96			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ LOW Time During Data Transfer	LTC1196 LTC1198		11 15			11 15			CLK CLK

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, $f_{CLK} = f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

PARAMETER	CONDITIONS		LTC1196-1A/LTC1196-2A LTC1198-1A/LTC1198-2A MIN	TYP	MAX	LTC1196-1B/LTC1196-2B LTC1198-1B/LTC1198-2B MIN	TYP	MAX	UNITS
No Missing Codes Resolution		●	8			8			Bits
Offset Error		●			±1/2			±1	LSB
Linearity Error	(Note 3)	●			±1/2			±1	LSB
Full-Scale Error		●			±1/2			±1	LSB
Total Unadjusted Error (Note 4)	LTC1196, V_{REF} = 2.5.000V LTC1198, V_{CC} = 2.700V	●			±1/2			±1	LSB
Analog and REF Input Range	LTC1196		–0.05V to V_{CC} + 0.05V						V
Analog Input Leakage Current	(Note 5)	●			±1			±1	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 3.6V	●	1.9			V
V_{IL}	Low Level Input Voltage	V_{CC} = 2.7V	●			0.45	V
I_{IH}	High Level Input Current	$V_{IN} = V_{CC}$	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 2.7V, I_O = 10µA V_{CC} = 2.7V, I_O = 360µA	● ●	2.3 2.1	2.60 2.45		V V
V_{OL}	Low Level Output Voltage	V_{CC} = 2.7V, I_O = 400µA	●			0.3	V
I_{OZ}	Hi-Z Output Leakage	$\overline{CS}$ = HIGH	●			±3	µA

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			15		mA
I_{REF}	Reference Current, LTC1196	$\overline{CS}$ = V_{CC} f_{SMPL} = $f_{SMPL(MAX)}$	● ●		0.001 0.25	3.0 0.5	µA mA
I_{CC}	Supply Current	$\overline{CS}$ = V_{CC} = 3.3V, LTC1198 (Shutdown) $\overline{CS}$ = V_{CC} = 3.3V, LTC1196 f_{SMPL} = $f_{SMPL(MAX)}$, LTC1196/LTC1198	● ● ●		0.001 1.5 2.0	3.0 4.5 6.0	µA mA mA

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196 MIN	LTC1196 TYP	LTC1196 MAX	LTC1198 MIN	LTC1198 TYP	LTC1198 MAX	UNITS
S/(N + D)	Signal-to-Noise Plus Distortion	190kHz/380kHz Input Signal			47/45			47/45		dB
THD	Total Harmonic Distortion	190kHz/380kHz Input Signal			49/47			49/47		dB
	Peak Harmonic or Spurious Noise	190kHz/380kHz Input Signal			53/46			53/46		dB
IMD	Intermodulation Distortion	f_{IN1} = 189.37kHz f_{IN2} = 192.446kHz			51			51		dB
	Full-Power Bandwidth				5			5		MHz
	Full Linear Bandwidth [S/(N + D) > 44dB				0.5			0.5		MHz

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V, V_{REF} = 2.5V, f_{CLK} = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		LTC1196-1 LTC1198-1 MIN	LTC1196-1 LTC1198-1 TYP	LTC1196-1 LTC1198-1 MAX	LTC1196-2 LTC1198-2 MIN	LTC1196-2 LTC1198-2 TYP	LTC1196-2 LTC1198-2 MAX	UNITS
t_{CONV}	Conversion Time (See Figures 1, 2)		 ●			1.58 1.85			2.13 2.84	µs µs
$f_{SMPL(MAX)}$	Maximum Sampling Frequency	LTC1196 LTC1196 LTC1198 LTC1198	 ● ●	450 383 337 287			333 250 250 187			kHz kHz kHz kHz
t_{dDO}	Delay Time, CLK↑ to D_{OUT} Data Valid	C_{LOAD} = 20pF	 ●		100	150 180		130	200 250	ns ns
t_{DIS}	Delay Time $\overline{CS}$↑ to D_{OUT} Hi-Z		●		110	220		120	250	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	C_{LOAD} = 20pF	●		80	130		100	200	ns
t_{hDO}	Time Output Data Remains Valid After CLK↑	C_{LOAD} = 20pF	●	45	90		45	120		ns
t_f	D_{OUT} Fall Time	C_{LOAD} = 20pF	●		10	30		15	40	ns
t_r	D_{OUT} Rise	C_{LOAD} = 20pF	●		10	30		15	40	ns
C_{IN}	Input Capacitance	Analog Input On Channel Analog Input Off Channel Digital Input			30 5 5			30 5 5		pF pF pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ELECTRICAL CHARACTERISTICS

Note 2: All voltage values are with respect to GND.

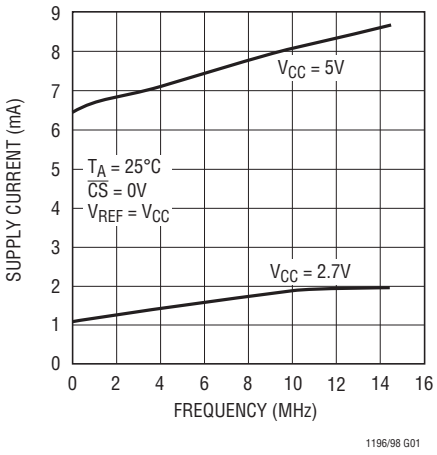
Note 3: Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 4: Total unadjusted error includes offset, full scale, linearity, multiplexer and hold step errors.

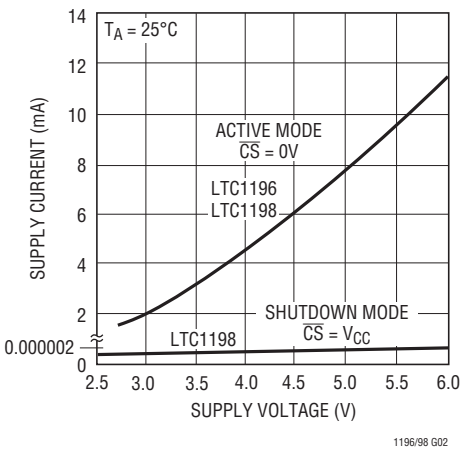
Note 5: Channel leakage current is measured after the channel selection.

TYPICAL PERFORMANCE CHARACTERISTICS

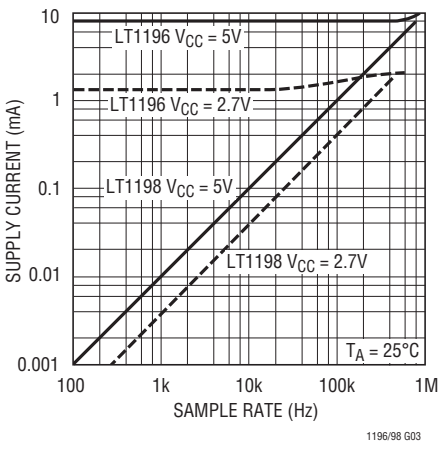
Supply Current vs Clock Rate



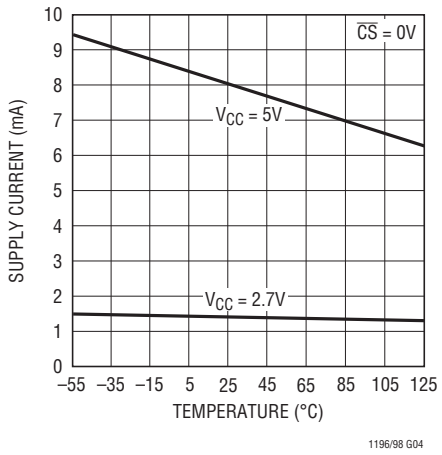
Supply Current vs Supply Voltage



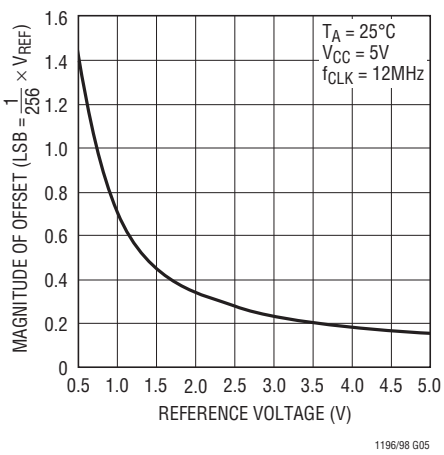
Supply Current vs Sample Rate



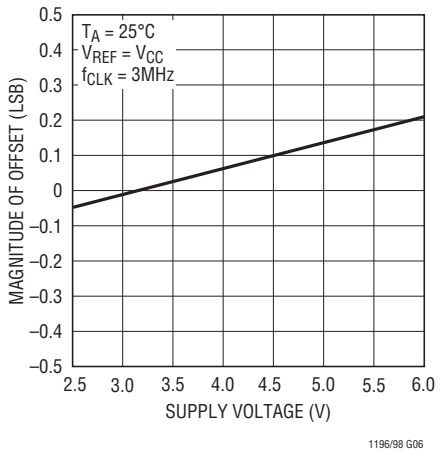
Supply Current vs Temperature



Offset vs Reference Voltage

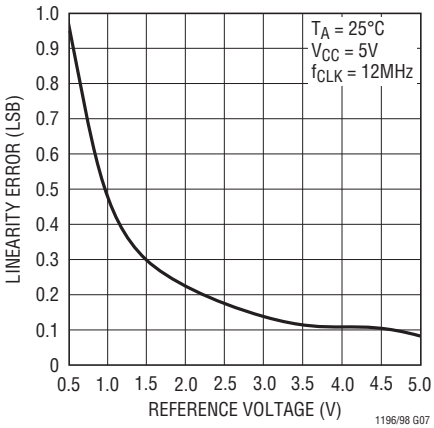


Offset vs Supply Voltage

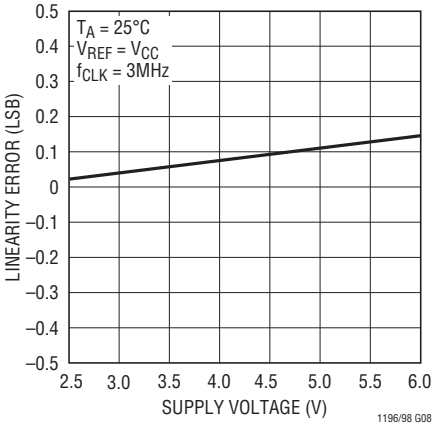


TYPICAL PERFORMANCE CHARACTERISTICS

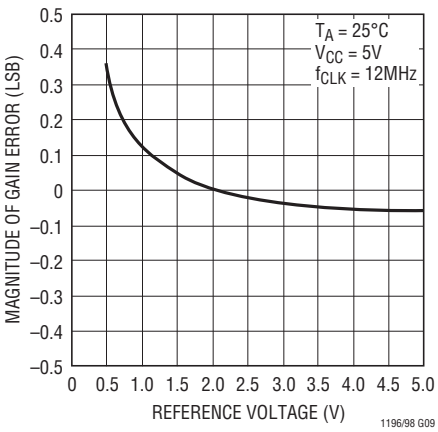
Linearity Error vs Reference Voltage



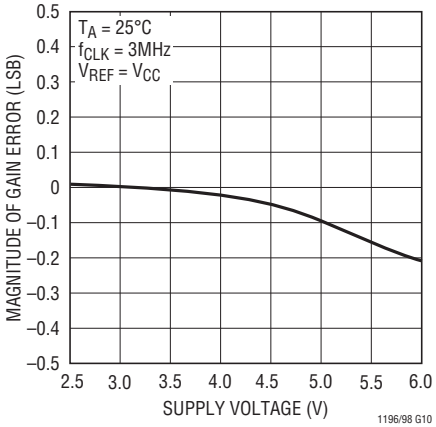
Linearity Error vs Supply Voltage



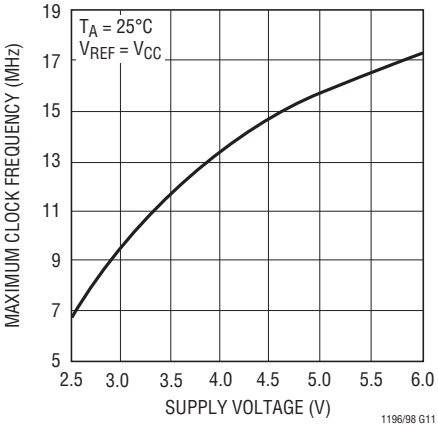
Supply Current vs Sample Rate



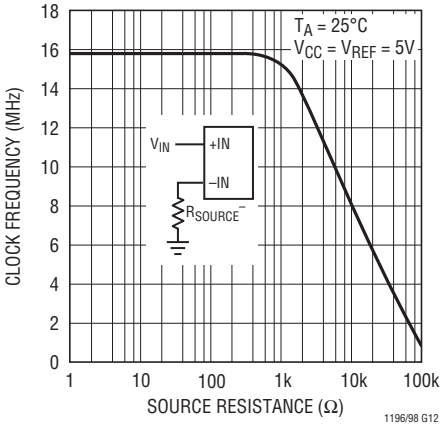
Gain vs Supply Voltage



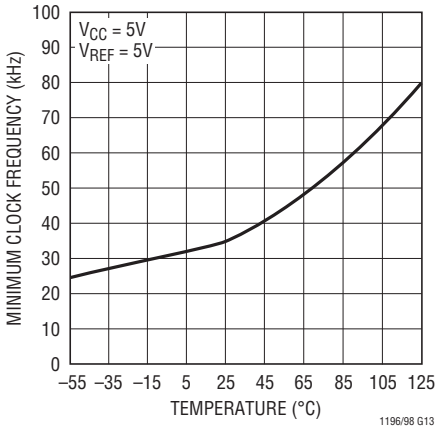
Maximum Clock Frequency vs Supply Voltage



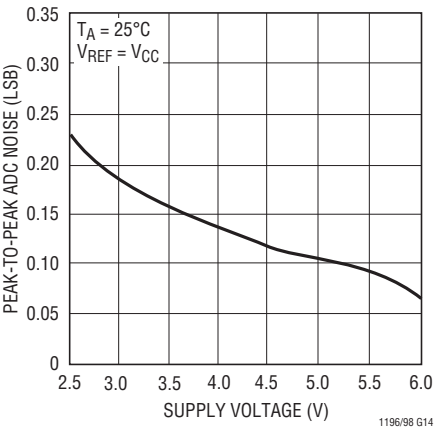
Maximum Clock Frequency vs Source Resistance



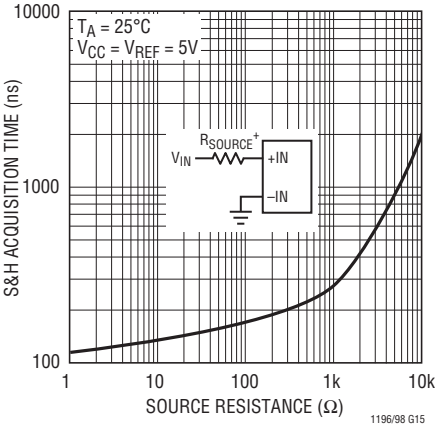
Minimum Clock Rate for 0.1LSB* Error



ADC Noise vs Referenced and Supply Voltage



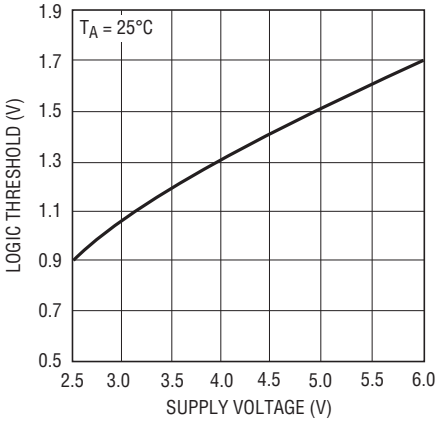
Sample-and-Hold Acquisition Time vs Source Resistance



*AS THE FREQUENCY IS DECREASED FROM 12MHz, MINIMUM CLOCK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 12MHz VALUE IS FIRST DETECTED.

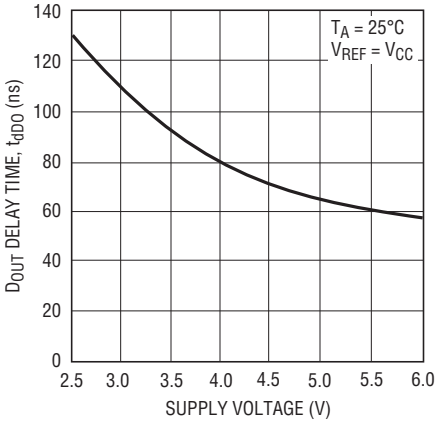
TYPICAL PERFORMANCE CHARACTERISTICS

Digital Input Logic Threshold vs Supply Voltage



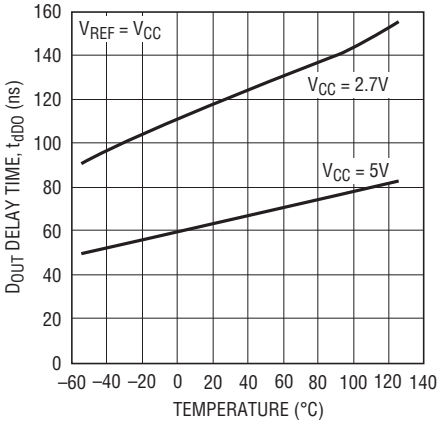
1196/98 G16

D_{OUT} Delay Time vs Supply Voltage



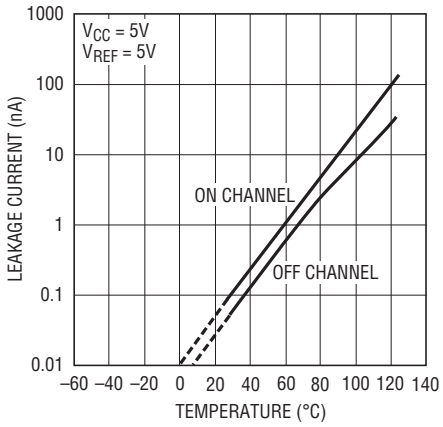
1196/98 G17

D_{OUT} Delay Time vs Temperature



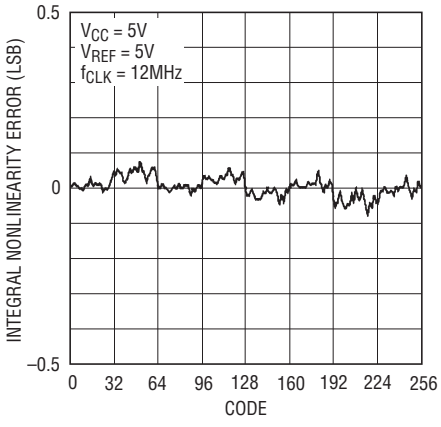
1196/98 G18

Input Channel Leakage Current vs Temperature



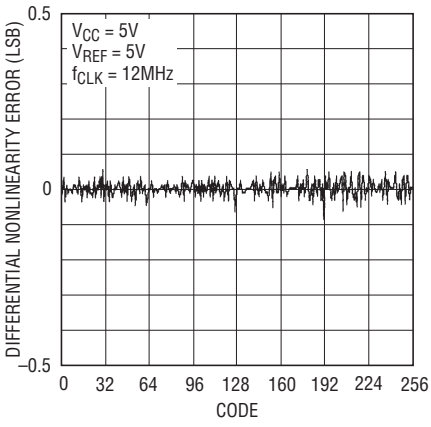
1196/98 G19

Integral Nonlinearity vs Code at 5V



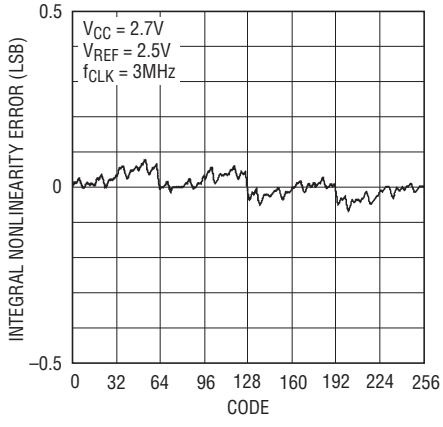
1196/98 G20

Differential Nonlinearity vs Code at 5V



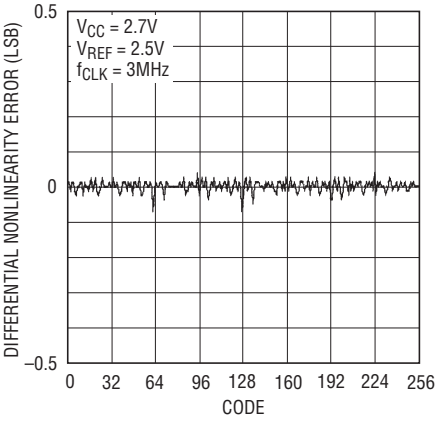
1196/98 G21

Integral Nonlinearity vs Code at 2.7V



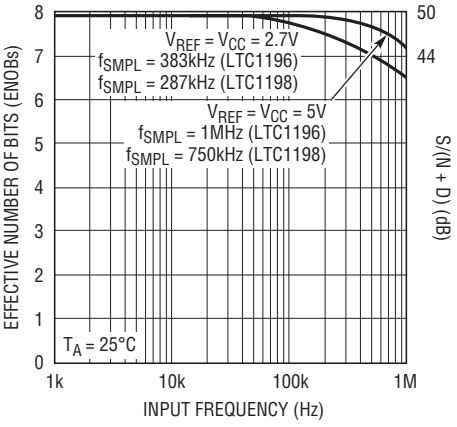
1196/98 G22

Differential Nonlinearity vs Code at 2.7V



1196/98 G23

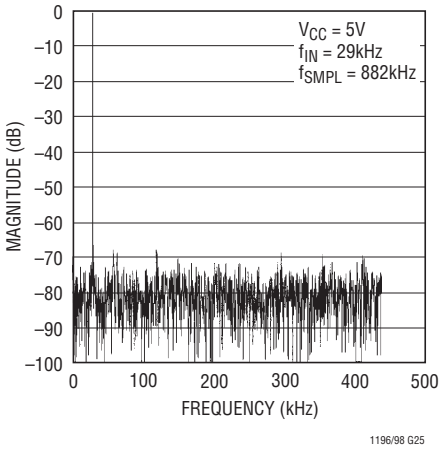
Effective Bits and S/(N + D) vs Input Frequency



1196/98 G24

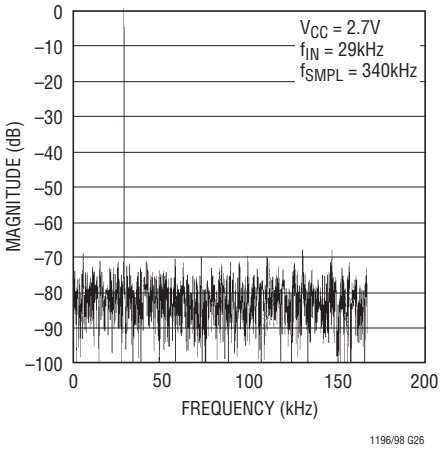
TYPICAL PERFORMANCE CHARACTERISTICS

4096 Point FFT Plot at 5V



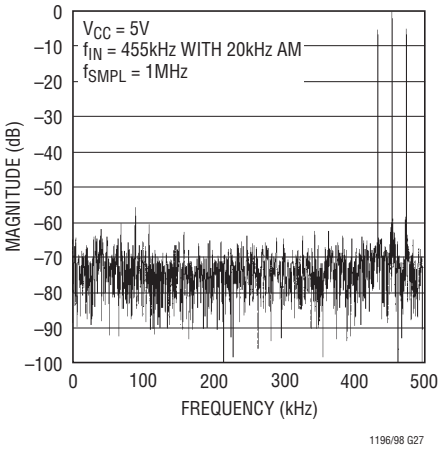
1196/98 G25

4096 Point FFT Plot at 2.7V



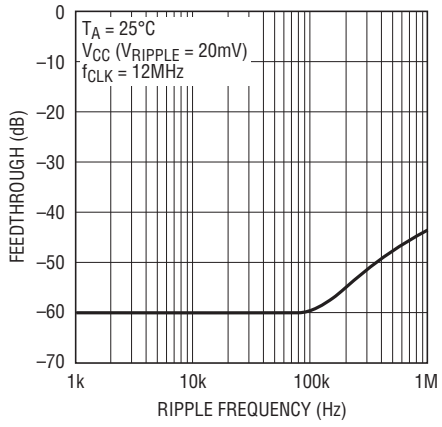
1196/98 G26

FFT Output of 455kHz AM Signal Digitized at 1Msps



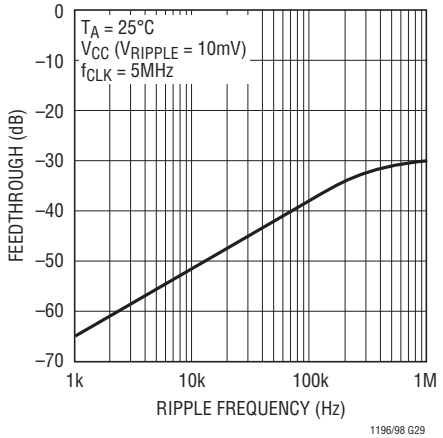
1196/98 G27

Power Supply Feedthrough vs Ripple Frequency



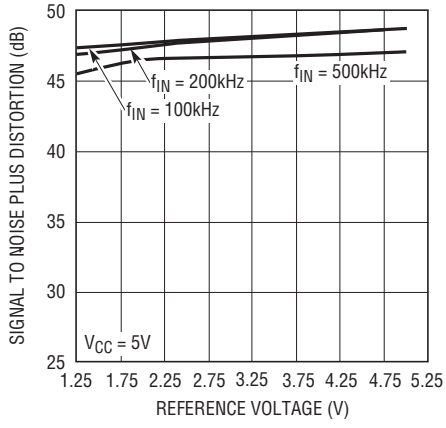
1196/98 G28

Power Supply Feedthrough vs Ripple Frequency



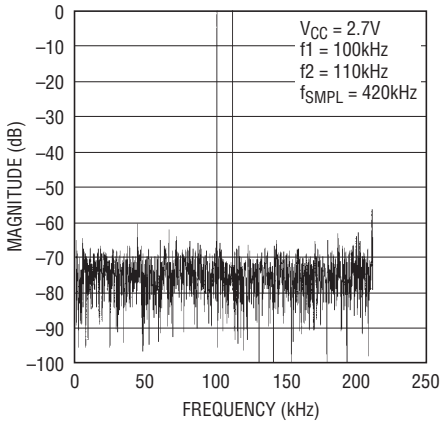
1196/98 G29

S/(N + D) vs Reference Voltage and Input Frequency



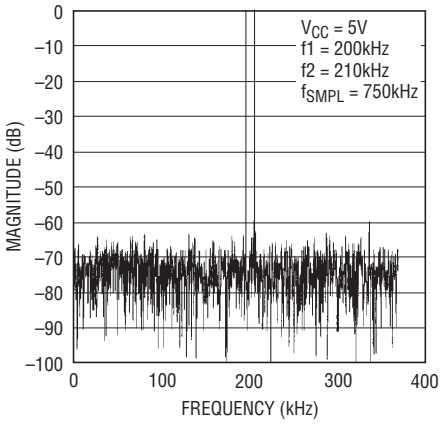
1196/98 G30

Intermodulation Distortion at 2.7V



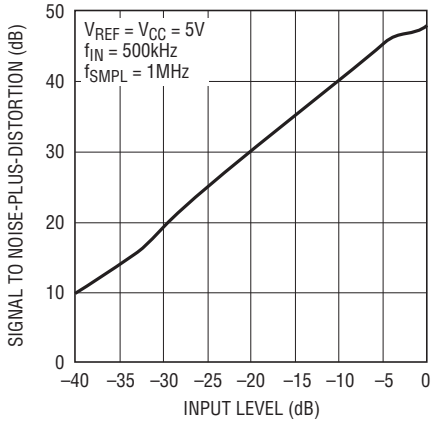
1196/98 G31

Intermodulation Distortion at 5V



1196/98 G32

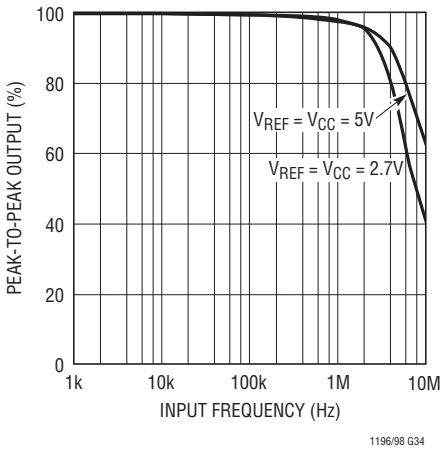
S/(N + D) vs Input Level



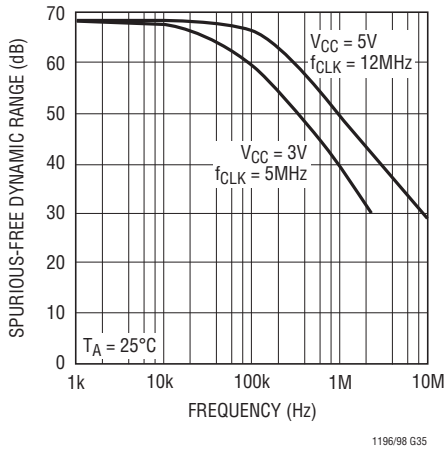
1196/98 G33

TYPICAL PERFORMANCE CHARACTERISTICS

Output Amplitude vs Input Frequency



Spurious-Free Dynamic Range vs Frequency



PIN FUNCTIONS

LTC1196

$\overline{CS}$ (Pin 1): Chip Select Input. A logic LOW on this input enables the LTC1196. A logic HIGH on this input disables the LTC1196.

IN^+ (Pin 2): Analog Input. This input must be free of noise with respect to GND.

IN^- (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

V_{REF} (Pin 5): Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

V_{CC} (Pin 8): Power Supply Voltage. This pin provides power to the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

LTC1198

$\overline{CS}$/SHUTDOWN (Pin 1): Chip Select Input. A logic LOW on this input enables the LTC1198. A logic HIGH on this input disables the LTC1198 and disconnects the power to THE LTC1198.

CHO (Pin 2): Analog Input. This input must be free of noise with respect to GND.

CH1 (Pin 3): Analog Input. This input must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

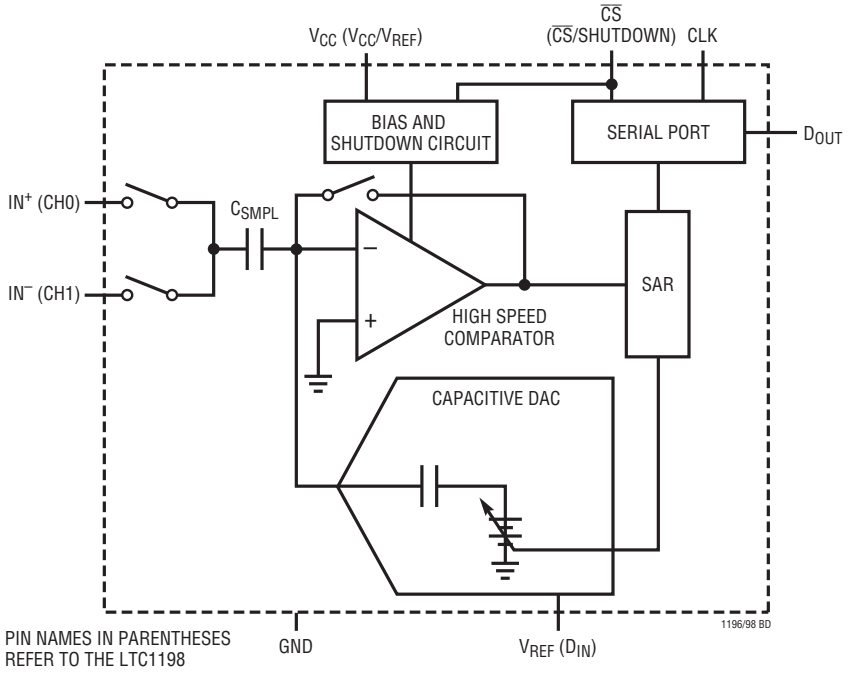
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

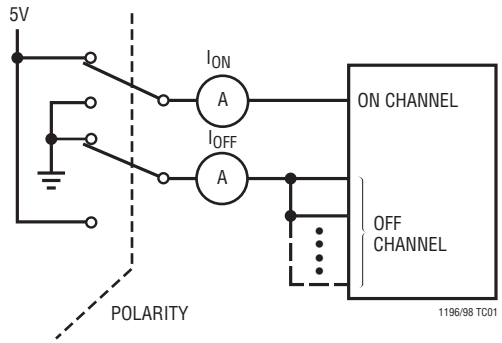
V_{CC} (V_{REF}) (Pin 8): Power Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. It must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

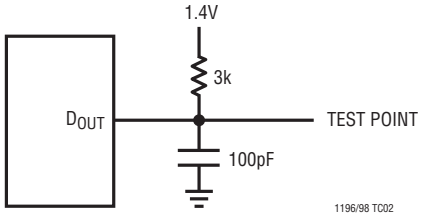


TEST CIRCUITS

On and Off Channel Leakage Current

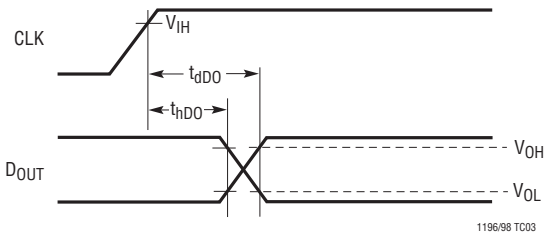


Load Circuit for t_{dDO}, t_r and t_f



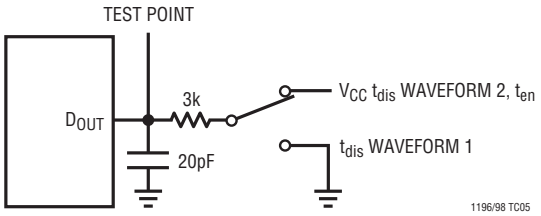
Voltage Waveform for D_{OUT} Rise and Fall Times, t_r, t_f

Voltage Waveform for D_{OUT} Delay Time, t_{dDO}, t_{hDO}

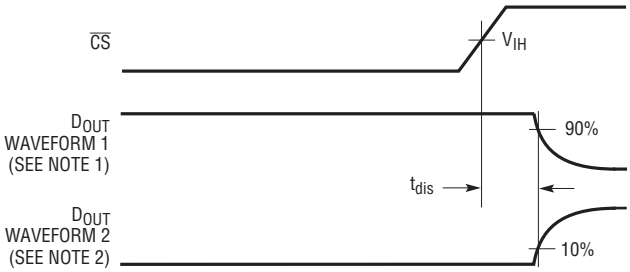


TEST CIRCUITS

Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

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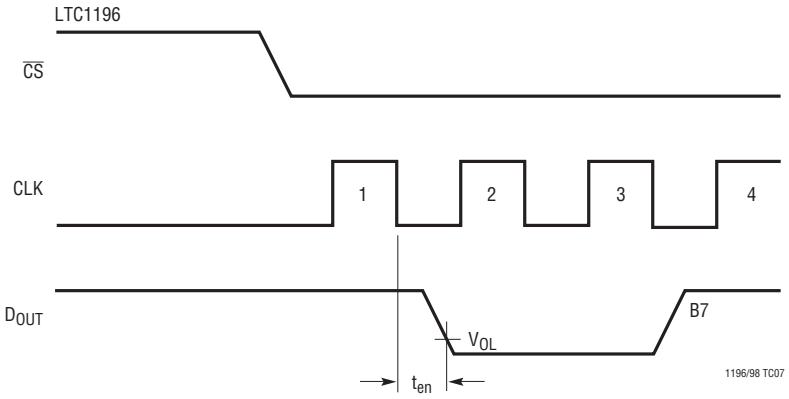
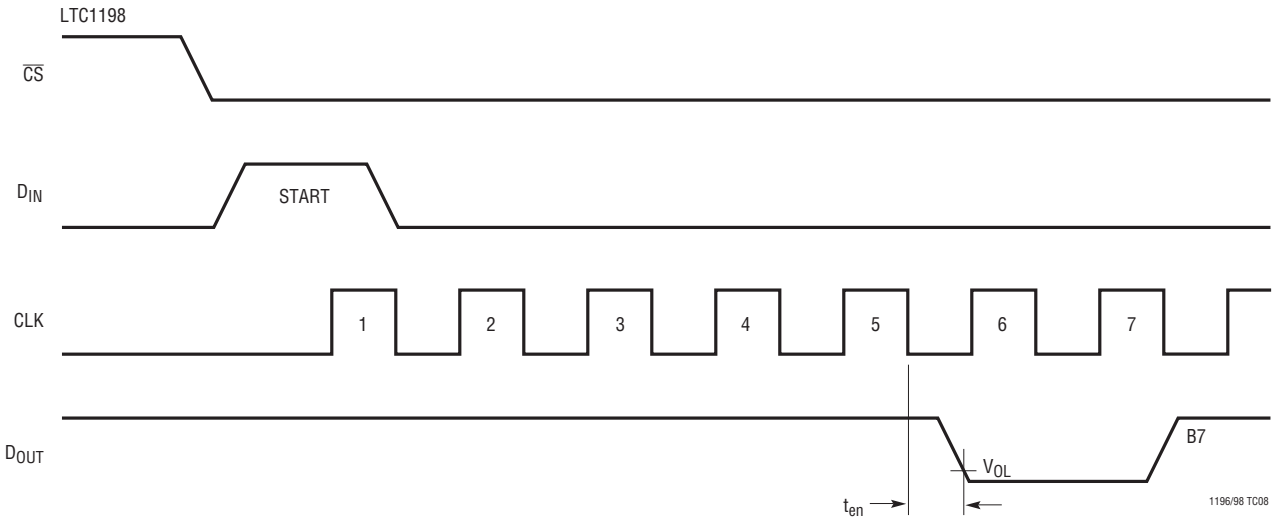
Voltage Waveforms for t_{en}



Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

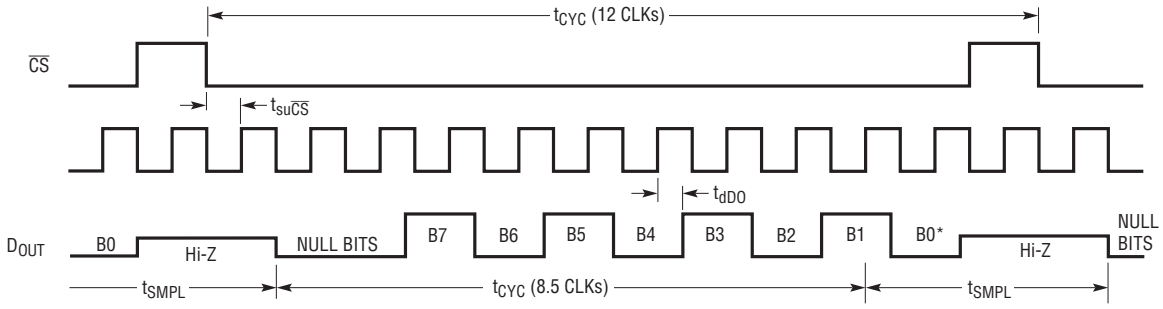
OVERVIEW

The LTC1196/LTC1198 are 600ns sampling 8-bit A/D converters packaged in tiny 8-pin SO packages and operating on 3V to 6V supplies. The ADCs draw only 10mW from a 3V supply or 50mW from a 5V supply.

Both the LTC1196 and the LTC1198 contain an 8-bit, switched-capacitor ADC, a sample-and-hold, and a serial port (see the Block Diagram). The on-chip sample-and-holds have full-accuracy input bandwidths of 1MHz. Although they share the same basic design, the LTC1196 and LTC1198 differ in some respects. The LTC1196 has a differential input and has an external reference input pin. It can measure signals floating on a DC common mode voltage and can operate with reduced spans below 1V. The LTC1198 has a 2-channel input multiplexer and can convert either channel with respect to ground or the difference between the two. It also automatically powers down when not performing conversion, drawing only leakage current.

SERIAL INTERFACE

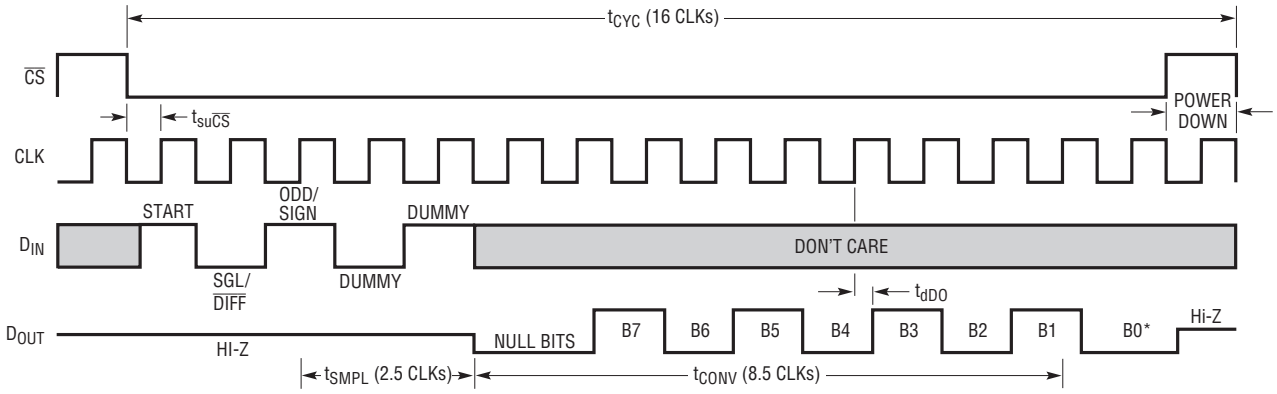
The LTC1196/LTC1198 will interface via three or four wires to ASICs, PLDs, microprocessors, DSPs, or shift registers (see Operating Sequence in Figures 1 and 2). To run at their fastest conversion rates (600ns), they must be clocked at 14.4MHz. HC logic families and any high speed ASIC or PLD will easily interface to the ADCs at that speed (see Data Transfer and Typical Application sections). Full speed operation from a 3V supply can still be achieved with 3V ASICs, PLDs or HC logic circuits.



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY

1196/98 F01

Figure 1. LTC1196 Operating Sequence



*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY

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Figure 2. LTC1198 Operating Sequence Example: Differential Inputs (CH1, CH0)

APPLICATIONS INFORMATION

Connection to a microprocessor or a DSP serial port is quite simple (see the Data Transfer section). It requires no additional hardware, but the speed will be limited by the clock rate of the microprocessor or the DSP which limits the conversion time of the LTC1196/LTC1198.

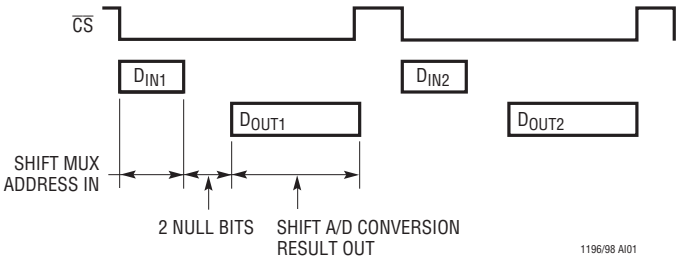
Data Transfer

Data transfer differs slightly between the LTC1196 and the LTC1198. The LTC1196 interfaces over three lines: $\overline{CS}$, CLK and D_{OUT}. A falling $\overline{CS}$ initiates data transfer as depicted by the LTC1196 Operating Sequence in Figure 1. After $\overline{CS}$ falls, the first CLK pulse enables D_{OUT}. After two null bits, the A/D conversion result is output on the D_{OUT} line. Bringing $\overline{CS}$ HIGH resets the LTC1196 for the next data exchange.

The LTC1198 can transfer data with three or four wires. The additional input, D_{IN}, is used to select the 2-channel MUX configuration.

The data transfer between the LTC1198 and the digital systems can be broken into two sections: Input Data Word and A/D Conversion Result. First, each bit of the input data word is captured on the rising CLK edge by the LTC1198. Second, each bit of the A/D conversion result on the D_{OUT} line is updated on the rising CLK edge by the LTC1198. This bit should be captured on the next rising CLK edge by the digital systems (see the A/D Conversion Result section).

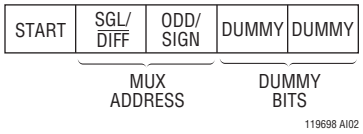
Data transfer is initiated by a falling chip select ($\overline{CS}$) signal as depicted by the LTC1198 Operating Sequence in Figure 2. After $\overline{CS}$ falls, the LTC1198 looks for a START bit. After the START bit is received, the 4-bit input word is shifted into the D_{IN} input. The first two bits of the input word configure the LTC1198. The last two bits of the input word allow the ADC to acquire the input voltage by 2.5 clocks before the conversion starts. After the conversion starts, two null bits and the conversion result are output on the D_{OUT} line. At the end of the data exchange $\overline{CS}$ should be brought HIGH. This resets the LTC1198 in preparation for the next data exchange.



Input Data Word

The LTC1196 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result is output on the D_{OUT} line in an MSB-first sequence, followed by zeros indefinitely if clocks are continuously applied with $\overline{CS}$ LOW.

The LTC1198 clocks data into the D_{IN} input on the rising edge of the clock. The input data word is defined as follows:



START Bit

The first *logical one* clocked into the D_{IN} input after $\overline{CS}$ goes LOW is the START bit. The START bit initiates the data transfer. The LTC1198 will ignore all leading zeros which precede this *logical one*. After the START bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The two bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND.

LTC1198 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/DIFF	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

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APPLICATIONS INFORMATION

Dummy Bits

The last two bits of the input word following the MUX address are dummy bits. Either bit can be a *logical one* or a *logical zero*. These two bits allow the ADC 2.5 clocks to acquire the input signal after the channel selection.

A/D Conversion Result

Both the LTC1196 and the LTC1198 have the A/D conversion result appear on the D_{OUT} line after two null bits (see the operating sequences in Figures 1 and 2). Data on the D_{OUT} line is updated on the rising edge of the CLK line. The D_{OUT} data should also be captured on the rising CLK edge by the digital systems. Data on the D_{OUT} line remains valid for a minimum time of t_{hDO} (30ns at 5V) to allow the capture to occur (see Figure 3).

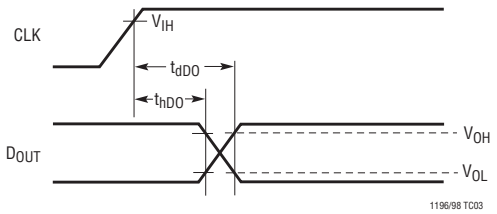


Figure 3. Voltage Waveform for D_{OUT} Delay Time, t_{dDO} and t_{hDO}

Unipolar Transfer Curve

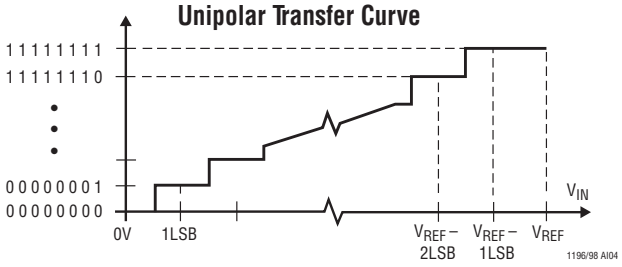
The LTC1196/LTC1198 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
11111111	V_{REF} – 1LSB	4.9805V
11111110	V_{REF} – 2LSB	4.9609V
•	•	•
•	•	•
•	•	•
00000001	1LSB	0.0195V
00000000	0V	0V

1196/98 AI05

Unipolar Transfer Curve



Operation with D_{IN} and D_{OUT} Tied Together

The LTC1198 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the digital systems. Data is transmitted in both directions on a single wire. The pin of the digital systems connected to this data line should be configurable as either an input or an output. The LTC1198 will take control of the data line and drive it LOW on the fifth falling CLK edge after the START bit is received (see Figure 4). Therefore, the port line of the digital systems must be switched to an input before this happens to avoid a conflict.

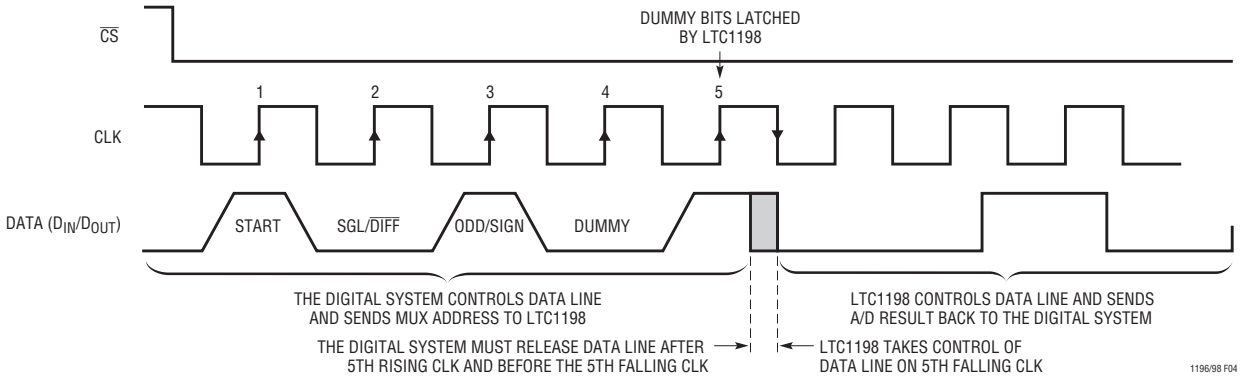


Figure 4. LTC1198 Operation with D_{IN} and D_{OUT} Tied Together

APPLICATIONS INFORMATION

REDUCING POWER CONSUMPTION

The LTC1196/LTC1198 can sample at up to a 1MHz rate, drawing only 50mW from a 5V supply. Power consumption can be reduced in two ways. Using a 3V supply lowers the power consumption on both devices by a factor of five, to 10mW. The LTC1198 can reduce power even further because it shuts down whenever it is not converting. Figure 5 shows the supply current versus sample rate for the LTC1196 and LTC1198 on 3V and 5V. To achieve such a low power consumption, especially for the LTC1198, several things must be taken into consideration.

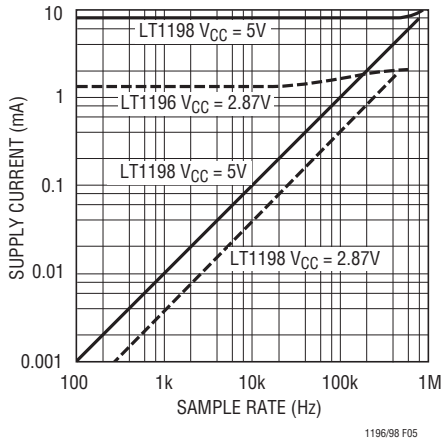


Figure 5. Supply Current vs Sample Rate for LTC1196/LTC1198 Operating on 5V and 2.7V Supplies

Shutdown (LTC1198)

Figure 2 shows the operating sequence of the LTC1198. The converter draws power when the $\overline{CS}$ pin is LOW and powers itself down when that pin is HIGH. For lowest power consumption in shutdown, the $\overline{CS}$ pin should be driven with CMOS levels (0V to V_{CC}) so that the $\overline{CS}$ input buffer of the converter will not draw current.

When the $\overline{CS}$ pin is HIGH (= supply voltage), the LTC1198 is in shutdown mode and draws only leakage current. The status of the D_{IN} and CLK input has no effect on the supply current during this time. There is no need to stop D_{IN} and CLK with $\overline{CS}$ = HIGH; they can continue to run without drawing current.

Minimize $\overline{CS}$ LOW Time (LTC1198)

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ LOW time. Bringing $\overline{CS}$ LOW, transferring data as quickly as possible, then bringing it back HIGH will result in the lowest current drain. This minimizes the amount of time the device draws power.

OPERATING ON OTHER THAN 5V SUPPLIES

The LTC1196/LTC1198 operate from single 2.7V to 6V supplies. To operate the LTC1196/LTC1198 on other than 5V supplies, a few things must be kept in mind.

Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and D_{IN} are made to meet TTL on 5V supply. When the supply voltage varies, the input logic levels also change (see the Digital Input Logic Threshold vs Supply Voltage curve in the Typical Performance Characteristics section). For these two ADCs to sample and convert correctly, the digital inputs have to be in the logical LOW and HIGH relative to the operating supply voltage. If achieving micropower consumption is desirable on the LTC1198, the digital inputs must go rail-to-rail between supply voltage and ground (see the Reducing Power Consumption section).

Clock Frequency

The maximum recommended clock frequency is 14.4MHz at 25°C for the LTC1196/LTC1198 running off a 5V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the Maximum Clock Rate vs Supply Voltage curve in the Typical Performance Characteristics section). If the supply is reduced, the clock rate must also be reduced. At 3V, the devices are specified with a 5.4MHz clock at 25°C.

APPLICATIONS INFORMATION

Mixed Supplies

It is possible to have a digital system running off a 5V supply and communicate with the LTC1196/LTC1198 operating on a 3V supply. Achieving this reduces the outputs of D_{OUT} from the ADCs to toggle the equivalent input of the digital system. The $\overline{CS}$, CLK and D_{IN} inputs of the ADCs will take 5V signals from the digital system without causing any problem (see the Digital Input Logic Threshold vs Supply Voltage curve in the Typical Performance Characteristics section). With the LTC1196 operating on a 3V supply, the output of D_{OUT} only goes between 0V and 3V. This signal easily meets TTL levels (see Figure 6).

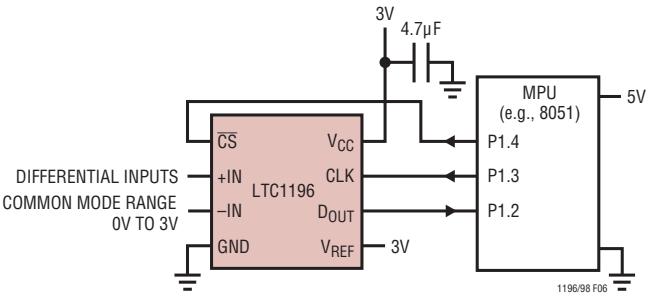


Figure 6. Interfacing a 3V Powered LTC1196 to a 5V System

BOARD LAYOUT CONSIDERATIONS

Grounding and Bypassing

The LTC1196/LTC1198 are easy to use if some care is taken. They should be used with an analog ground plane and single-point grounding techniques. The GND pin should be tied directly to the ground plane.

The V_{CC} pin should be bypassed to the ground plane with a 1µF tantalum with leads as short as possible. If the power supply is clean, the LTC1196/LTC1198 can also operate with smaller 0.1µF surface mount or ceramic bypass capacitors. All analog inputs should be referenced directly to the single-point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

SAMPLE-AND-HOLD

Both the LTC1196 and the LTC1198 provide a built-in sample-and-hold (S&H) function to acquire the input signal. The S&H acquires the input signal from "+" input during t_{SMPL} as shown in Figures 1 and 2. The S&H of the LTC1198 can sample input signals in either single-ended or differential mode (see Figure 7).

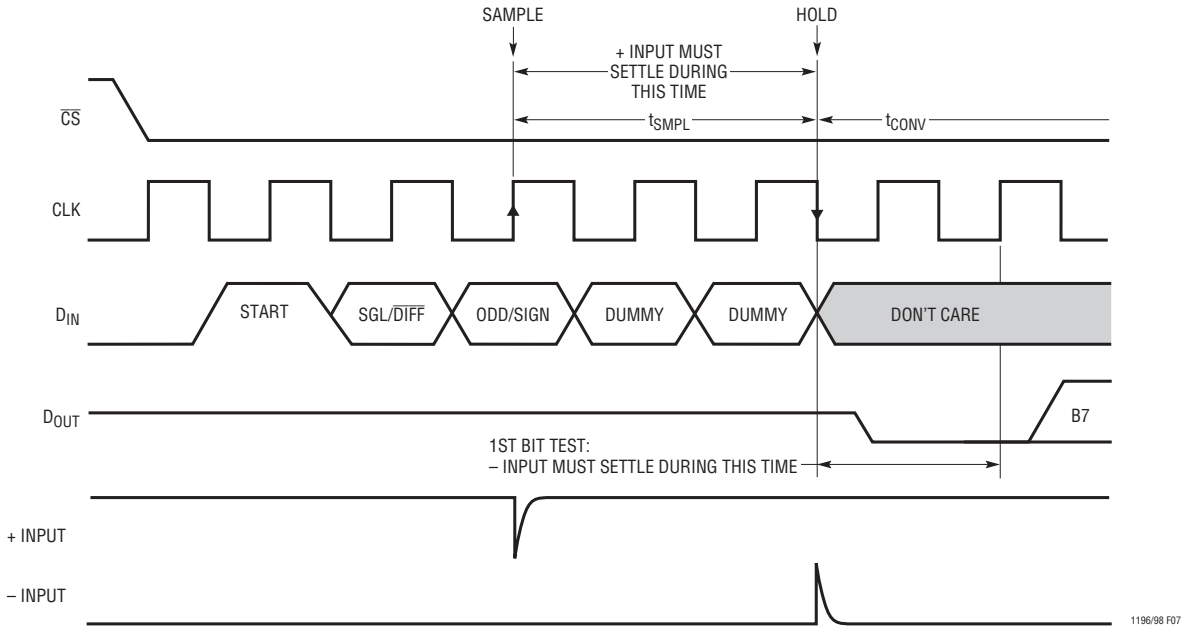


Figure 7. LTC1198 "+" and "–" Input Settling Windows

APPLICATIONS INFORMATION

Single-Ended Inputs

The sample-and-hold of the LTC1198 allows conversion of rapidly varying signals. The input voltage is sampled during the t_{SMPL} time as shown in Figure 7. The sampling interval begins as the bit preceding the first dummy bit is shifted in and continues until the falling CLK edge after the second dummy bit is received. On this falling edge, the S&H goes into hold mode and the conversion begins.

Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 8.5 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input, this error would be:

$$V_{ERROR(MAX)} = V_{PEAK} \bullet 2 \bullet \pi \bullet f(-) \bullet 8.5/fCLK$$

where f("–") is the frequency of the "–" input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. V_{ERROR} is proportional to f(–) and inversely proportional to f_{CLK}. For a 60Hz signal on the "–" input to generate a 1/4LSB error (5mV) with the converter running at CLK = 12MHz, its peak value would have to be 18.7V.

ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1196/LTC1198 have one capacitive switching input current spike per conversion. These current spikes settle quickly and do not cause a problem. However, if source resistances larger than 100Ω are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

"+" Input Settling

The input capacitor of the LTC1196 is switched onto "+" input at the end of the conversion and samples the input signal until the conversion begins (see Figure 1). The input capacitor of the LTC1198 is switched onto "+" input during the sample phase (t_{SMPL}, see Figure 7). The sample phase is 2.5 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within t_{SMPL} for the LTC1196/LTC1198. Minimizing R_{SOURCE}^+ will improve the input settling time. If a large "+" input source resistance must be used, the sample time can be increased by allowing more time between conversions for the LTC1196 or by using a slower CLK frequency for the LTC1198.

"–" Input Settling

At the end of the t_{SMPL}, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 7). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. However, it is critical that the "–" input voltage settle completely during the first CLK cycle of the conversion time and be free of noise. Minimizing R_{SOURCE}^- will improve settling time. If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figures 1 and 7). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps.

To achieve the full sampling rate, the analog input should be driven with a low impedance source (<100Ω) or a high speed op amp (e.g., the LT1223, LT1191 or LT1226). Higher impedance sources or slower op amps can easily be accommodated by allowing more time for the analog input to settle as described above.

APPLICATIONS INFORMATION

Source Resistance

The analog inputs of the LTC1196/LTC1198 look like a 25pF capacitor (C_{IN}) in series with a 120Ω resistor (R_{ON}) as shown in Figure 8. C_{IN} gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within t_{SMPL}.

REFERENCE INPUT

The voltage on the reference input of the LTC1196 defines the voltage span of the A/D converter. The reference input has transient capacitive switching currents which are due to the switched-capacitor conversion technique (see Figure 9). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the ADC. These high frequency current spikes will settle quickly and do not cause a problem if the reference input is bypassed with at least a 0.1µF capacitor.

The reference input can be driven with standard voltage references. Bypassing the reference with a 0.1µF capacitor is recommended to keep the high frequency impedance low as described above. Some references require a small resistor in series with the bypass capacitor for frequency stability. See the individual reference data sheet for details.

Reduced Reference Operation

The minimum reference voltage of the LTC1198 is limited to 2.7V because the V_{CC} supply and reference are internally tied together. However, the LTC1196 can operate with reference voltages below 1V.

The effective resolution of the LTC1196 can be increased by reducing the input span of the converter. The LTC1196 exhibits good linearity and gain over a wide range of reference voltages (see the Linearity and Full-Scale Error vs Reference Voltage curves in the Typical Performance Characteristics section). However, care must be taken when operating at low values of V_{REF} because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low V_{REF} values.

1. Offset
2. Noise

Offset with Reduced V_{REF}

The offset of the LTC1196 has a larger effect on the output code when the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The Unadjusted Offset Error vs Reference Voltage curve in the Typical Performance Characteristics section depicts how offset in LSBs is related to reference voltage for a typical value of V_{OS}. For example, a V_{OS} of 2mV which is 0.1LSB with a 5V reference becomes 0.5LSB with a 1V reference and 2.5LSB with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1196.

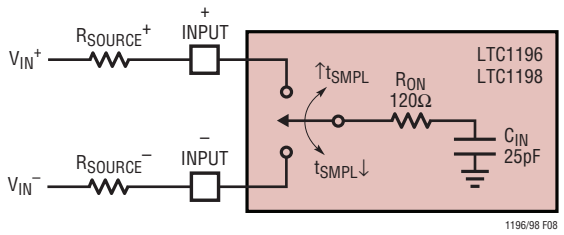


Figure 8. Analog Input Equivalent Circuit

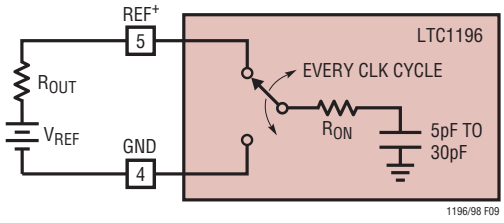


Figure 9. Reference Input Equivalent Circuit

APPLICATIONS INFORMATION

Noise with Reduced V_{REF}

The total input referred noise of the LTC1196 can be reduced to approximately $2mV_{P-P}$ using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 2mV noise is only 0.1LSB peak-to-peak. In this case, the LTC1196 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 2mV noise is 0.5LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved by 1LSB. If the reference is further reduced to 200mV, the 2mV noise becomes equal to 2.5LSB and a stable code is difficult to achieve. In this case averaging readings is necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on V_{CC}, V_{REF} or V_{IN}) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

DYNAMIC PERFORMANCE

The LTC1196/LTC1198 have exceptionally high speed sampling capability. Fast Fourier Transform (FFT) test techniques are used to characterize the ADC's frequency response, distortion and noise at the rated throughput. By applying a low distortion sine wave and analyzing the digital output using a FFT algorithm, the ADC's spectral content can be examined for frequencies outside the fundamental. Figure 10 shows a typical LTC1196 FFT plot.

Signal-to-Noise Ratio

The Signal-to-Noise plus Distortion Ratio [S/(N + D)] is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the ADC's output. The output is band limited to frequencies above DC and below one half the sampling frequency. Figure 10 shows a typical spectral content with a 882kHz sampling rate.

Effective Number of Bits

The Effective Number of Bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to S/(N + D) by the equation:

$$N = [S/(N + D) - 1.76]/6.02$$

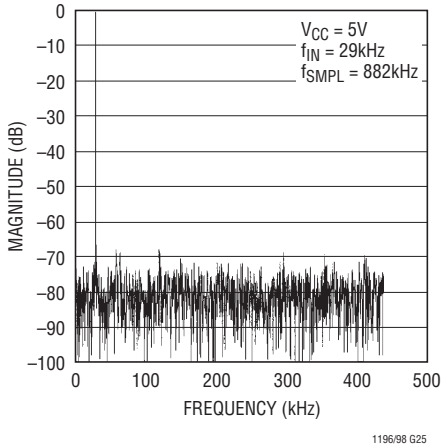


Figure 10. LTC1196 Nonaveraged, 4096 Point FFT Plot

APPLICATIONS INFORMATION

where N is the effective number of bits of resolution and S/(N + D) is expressed in dB. At the maximum sampling rate of 1.2MHz with a 5V supply the LTC1196 maintains above 7.5 ENOBs at 400kHz input frequency. Above 500kHz the ENOBs gradually decline, as shown in Figure 11, due to increasing second harmonic distortion. The noise floor remains low.

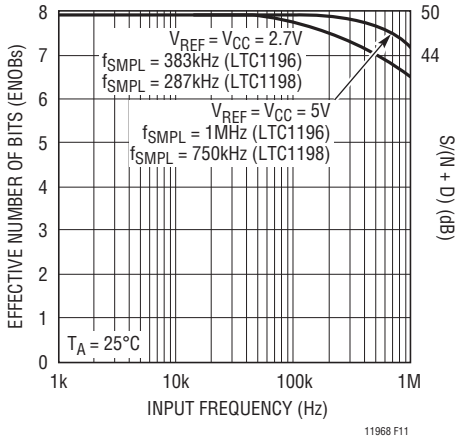


Figure 11. Effective Bits and S/(N + D) vs Input Frequency

Total Harmonic Distortion

Total Harmonic Distortion (THD) is the ratio of the RMS sum of all harmonics of the input signal to the fundamental itself. The out-of-band harmonics alias into the frequency band between DC and half of the sampling frequency. THD is defined as:

$$THD = 20\log\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \ldots + V_N^2}}{V_1}$$

where V_1 is the RMS amplitude of the fundamental frequency and V_2 through V_N are the amplitudes of the second through the Nth harmonics. The typical THD specification in the Dynamic Accuracy table (see the Electrical Characteristics section) includes the 2nd through 5th harmonics. With a 100kHz input signal, the LTC1196/LTC1198 have typical THD of 50dB and 49dB with V_{CC} = 5V and V_{CC} = 3V, respectively.

Intermodulation Distortion

If the ADC input signal consists of more than one spectral component, the ADC transfer function nonlinearity can produce intermodulation distortion (IMD) in addition to THD. IMD is the change in one sinusoidal input caused by the presence of another sinusoidal input at a different frequency.

If two pure sine waves of frequencies f_a and f_b are applied to the ADC input, nonlinearities in the ADC transfer function can create distortion products at sum and difference frequencies of $mf_a \pm nf_b$, where m and n = 0, 1, 2, 3, etc. For example, the 2nd order IMD terms include $(f_a + f_b)$ and $(f_a - f_b)$ while 3rd order IMD terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$ and $(f_a - 2f_b)$. If the two input sine waves are equal in magnitudes, the value (in dB) of the 2nd order IMD products can be expressed by the following formula:

$$IMD\left(f_a \pm f_b\right) = 20\log\left[\frac{\text{amplitude}\left(f_a \pm f_b\right)}{\text{amplitude at } f_a}\right]$$

For input frequencies of 499kHz and 502kHz, the IMD of the LTC1196/LTC1198 is 51dB with a 5V supply.

Peak Harmonic or Spurious Noise

The peak harmonic or spurious noise is the largest spectral component excluding the input signal and DC. This value is expressed in dBs relative to the RMS value of a full-scale input signal.

Full-Power and Full-Linear Bandwidth

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3dB for a full-scale input.

The full-linear bandwidth is the input frequency at which the effective bits rating of the ADC falls to 7 bits. Beyond this frequency, distortion of the sampled input signal increases. The LTC1196/LTC1198 have been designed to optimize input bandwidth, allowing the ADCs to undersample input signals with frequencies above the converters' Nyquist frequency.

APPLICATIONS INFORMATION

3V VERSUS 5V PERFORMANCE COMPARISON

Table 1 shows the performance comparison between 3V and 5V supplies. The power dissipation drops by a factor of five when the supply is reduced to 3V. The converter slows down somewhat but still gives excellent performance on a 3V rail. With a 3V supply, the LTC1196 converts in 1.6µs, samples at 450kHz, and provides a 500kHz linear-input bandwidth.

Dynamic accuracy is excellent on both 5V and 3V. The ADCs typically provide 49.3dB of 7.9 ENOBs of dynamic accuracy at both 3V and 5V. The noise floor is extremely low, corresponding to a transition noise of less than 0.1LSB. DC accuracy includes ±0.5LSB total unadjusted error at 5V. At 3V, linearity error is ±0.5LSB while total unadjusted error increases to ±1LSB.

Table 1. 5V/3V Performance Comparison

LTC1196-1	**5V**	**3V**
P_{DISS}	50mW	10mW
Max f_{SMPL}	1MHz	383kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 at 300kHz	7.9 at 100kHz
Linear Input Bandwidth (ENOBs > 7)	1MHz	500kHz
LTC1198-1		
P_{DISS}	50mW	10mW
P_{DISS} (Shutdown)	15µW	9µW
Max f_{SMPL}	750kHz	287kHz
Min t_{CONV}	600ns	1.6µs
INL (Max)	0.5LSB	0.5LSB
Typical ENOBs	7.9 at 300kHz	7.9 at 100kHz
Linear Input Bandwidth (ENOBs > 7)	1MHz	500kHz

TYPICAL APPLICATIONS

PLD Interface Using the Altera EPM5064

The Altera EPM5064 has been chosen to demonstrate the interface between the LTC1196 and a PLD. The EPM5064 is programmed to be a 12-bit counter and an equivalent 74HC595 8-bit shift register, as shown in Figure 12. The circuit works as follows: bringing ENA HIGH makes the $\overline{CS}$ output HIGH and the EN input LOW to reset the LTC1196 and disable the shift register. Bringing ENA LOW, the $\overline{CS}$ output goes HIGH for one CLK cycle with every 12 CLK cycles. The inverted signal, EN, of the $\overline{CS}$ output makes the 8-bit data available on the B0-B7 lines. Figures 13 and 14 show the interconnection between the LTC1196 and EPM5064 and the timing diagram of the signals between these two devices. The CLK frequency in this circuit can run up to $f_{CLK(MAX)}$ of the LTC1196.

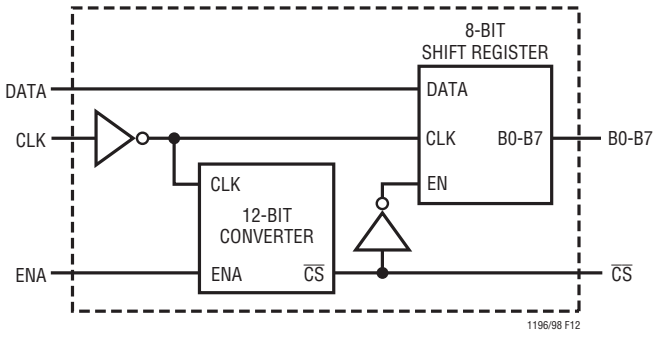


Figure 12. An Equivalent Circuit of the EPM5064

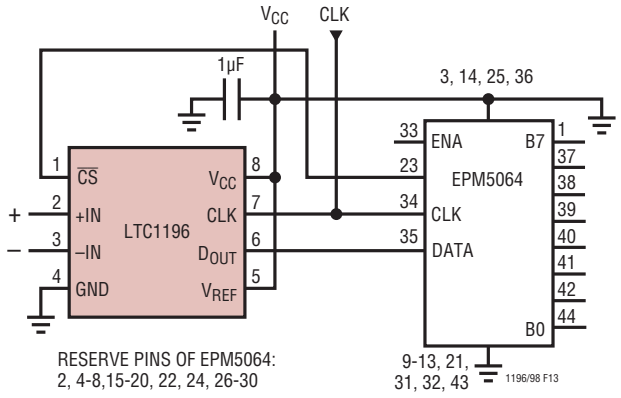


Figure 13. Interfacing the LTC1196 to the Altera EMP5064 PLD

TYPICAL APPLICATIONS

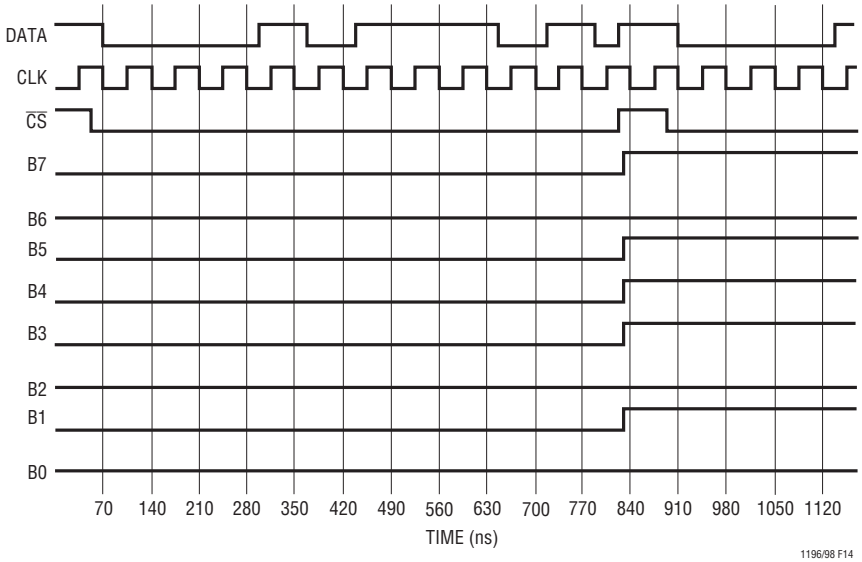


Figure 14. The Timing Diagram

Interfacing the LTC1198 to the TMS320C25 DSP

Figure 15 illustrates the interface between the LTC1198 8-bit data acquisition system and the TMS320C25 digital signal processor (DSP). The interface, which is optimized for speed of transfer and minimum processor supervision, can complete a conversion and shift the data in 4µs with f_{CLK} = 5MHz. The cycle time, 4µs, of each conversion is limited by maximum clock frequency of the serial port of the TMS320C25 which is 5MHz. The supply voltage for the LTC1198 in Figure 15 can be 2.7V to 6V with f_{CLK} = 5MHz. At 2.7V, f_{CLK} = 5MHz will work at 25°C. See the Recommended Operating Conditions table in the Electrical Characteristics section for limits over temperature.

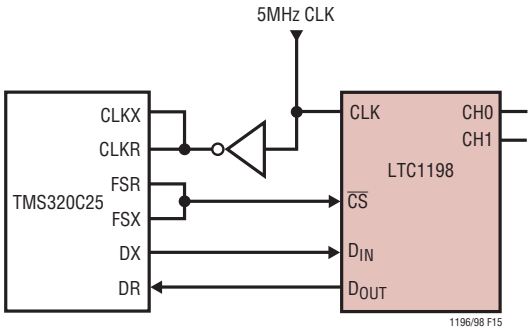


Figure 15. Interfacing the LTC1198 to the TMS320C25 DSP

Hardware Description

The circuit works as follows: the LTC1198 clock line controls the A/D conversion rate and the data shift rate. Data is transferred in a synchronous format over D_{IN} and D_{OUT}. The serial port of the TMS320C25 is compatible with that of the LTC1198. The data shift clock lines (CLKR, CLKX) are inputs only. The data shift clock comes from an external source. Inverting the shift clock is necessary because the LTC1198 and the TMS320C25 clock the input data on opposite edges.

The schematic of Figure 15 is fed by an external clock source. The signal is fed into the CLK pin of the LTC1198 directly. The signal is inverted with a 74HC04 and then applied to the data shift clock lines (CLKR, CLKX). The framing pulse of the TMS320C25 is fed directly to the $\overline{CS}$ of the LTC1198. DX and DR are tied directly to D_{IN} and D_{OUT}, respectively.

TYPICAL APPLICATIONS

The timing diagram of Figure 16 was obtained from the circuit of Figure 15. The CLK was 5MHz for the timing diagram and the TMS320C25 clock rate was 40MHz. Figure 17 shows the timing diagram with the LTC1198 running off a 2.7V supply and 5MHz CLK.

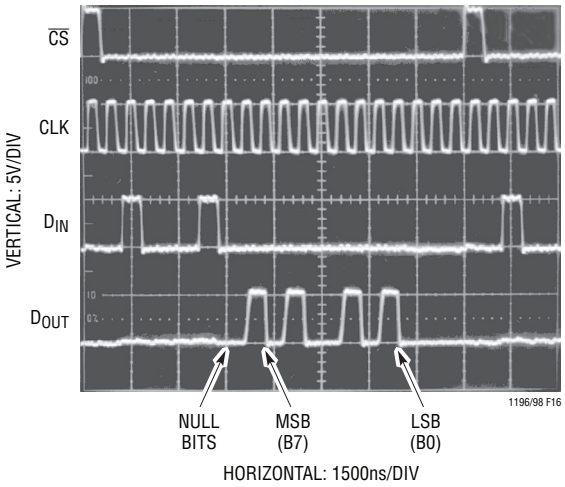


Figure 16. Scope Trace the LTC1198 Running Off 5V Supply in the Circuit of Figure 15

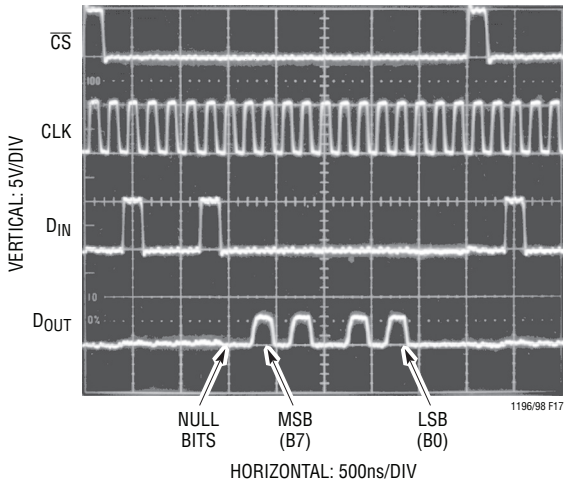


Figure 17. Scope Trace the LTC1198 Running Off 1.7V Supply in the Circuit of Figure 15

Software Description

The software configures and controls the serial port of the TMS320C25.

The code first sets up the interrupt and reset vectors. On reset the TMS320C25 starts executing code at the label INIT. Upon completion of a 16-bit data transfer, an interrupt is generated and the DSP will begin executing code at the label RINT.

In the beginning, the code initializes registers in the TMS320C25 that will be used in the transfer routine. The interrupts are temporarily disabled. The data memory page pointer register is set to zero. The auxiliary register pointer is loaded with one and auxiliary register one is loaded with the value 200 hexadecimal. This is the data memory location where the data from the LTC1198 will be stored. The interrupt mask register (IMR) is configured to recognize the RINT interrupt, which is generated after receiving the last of 16 bits on the serial port. This interrupt is still disabled at this time. The transmit framing synchronization pin (FSX) is configured to be an output. The F0 bit of the status register ST1, is initialized to zero which sets up the serial port to operate in the 16-bit mode.

Next, the code in TXRX routine starts to transmit and receive data. The DIN word is loaded into the ACC and shifted left eight times so that it appears as in Figure 18. This D_{IN} word configures the LTC1198 for CH0 with respect to CH1. The D_{IN} word is then put in the transmit register and the RINT interrupt is enabled. The NOP is repeated 3 times to mask out the interrupts and minimize the cycle time of the conversion to be 20 clock cycles. All clocking and $\overline{CS}$ functions are performed by the hardware.

B15							B8
0	1 START	0 S/$\overline{D}$	0 O/S	0 DUMMY	1 DUMMY	0	0

L1196/98 F18

Figure 18. D_{IN} Word in ACC of TMS20C25 for the Circuit in Figure 15

TYPICAL APPLICATIONS

Once RINT is generated the code begins execution at the label RINT. This code stores the D_{OUT} word from the LTC1198 in the ACC and then stores it in location 200 hex. The data appears in location 200 hex right-justified as shown in Figure 19. The code is set up to continually loop, so at this point the code jumps to label TXRX and repeats from here.

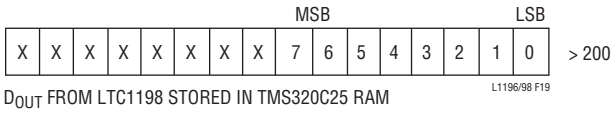


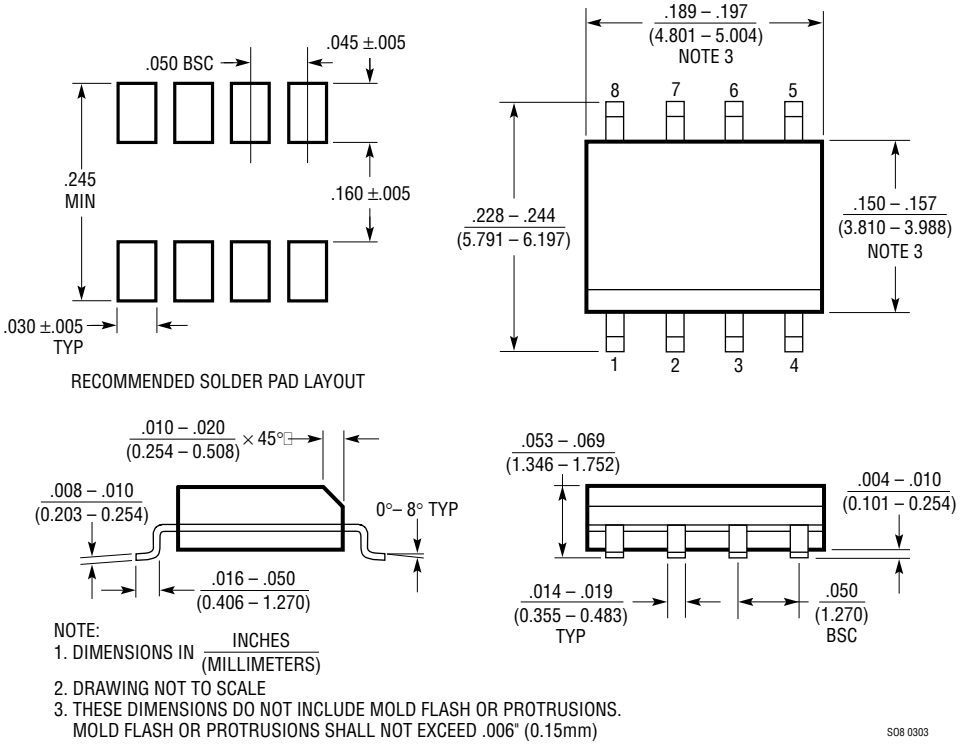
Figure 19. Memory Map for the Circuit in Figure 15

LABEL	MNEMONIC		COMMENTS
	AORG	0	ON RESET CODE EXECUTION STARTS AT 0
	B	INIT	BRANCH TO INITIALIZATION ROUTINE
	AORG	>26	ADDRESS TO RINT INTERRUPT VECTOR
	B	RINT	BRANCH TO RINT SERVICE ROUTINE
	AORG	>32	MAIN PROGRAM STARTS HERE
INIT	DINT		DISABLE INTERRUPTS
	LDPK	>0	SET DATA MEMORY PAGE POINTER TO 0
	LARP	>1	SET AUXILIARY REGISTER POINTER TO 1
	LRLK	AR1, >200	SET AUXILIARY REGISTER 1 TO >200
	LACK	>10	LOAD IMR CONFIG WORD INTO ACC
	SACL	>4	STORE IMR CONFIG WORD INTO IMR
	STXM		CONFIGURE FSX AS AN OUTPUT
	FORT	0	SET SERIAL PORT TO 16-BIT MODE
TXRX	LACK	>44	LOAD LTC1198 D_{IN} WORD INTO ACC
	SFSM		FSX PULSES GENERATED ON XSR LOAD
	RPTK	7	REPEAT NEXT INSTRUCTION 8 TIMES
	SFL		SHIFTS D_{IN} WORD TO RIGHT POSITION
	SACL	>1	PUT D_{IN} WORD IN TRANSMIT REGISTER
	EINT		ENABLE INTERRUPT (DISABLE ON RINT)
	RPTK	2	MINIMIZE THE CONVERSION CYCLE TIME
	NOP		TO BE 20 CLOCK CYCLES
RINT	ZALS	>0	STORE LTC1198 D_{OUT} WORD IN ACC
	SACL	*, 0	STORE ACC IN LOCATION >200
	B	TXRX	BRANCH TO TRANSMIT RECEIVE ROUTINE
	END		

Figure 20. TMS320C25 Code for the Circuit in Figure 15

PACKAGE DESCRIPTION

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

SO8 0303

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
ADCs		
LTC1402	12-Bit, 2.2Msps Serial ADC	5V or ±5V Supply, 4.096V or ±2.5V Span
LTC1403/LTC1403A	12-/14-Bit, 2.8Msps Serial ADCs	3V, 15mW, Unipolar Inputs, MSOP Package
LTC1403-1/LTC1403A-1	12-/14-Bit, 2.8Msps Serial ADCs	3V, 15mW, Bipolar Inputs, MSOP Package
LTC1405	12-Bit, 5Msps Parallel ADC	5V, Selectable Spans, 115mW
LTC1407/LTC1407A	12-/14-Bit, 3Msps Simultaneous Sampling ADCs	3V, 2-Channel Differential, Unipolar Inputs, 14mW, MSOP Package
LTC1407-1/LTC1407A-1	12-/14-Bit, 3Msps Simultaneous Sampling ADCs	3V, 2-Channel Differential, Bipolar Inputs, 14mW, MSOP Package
LTC1411	14-Bit, 2.5Msps Parallel ADC	5V, Selectable Spans, 80dB SINAD
LTC1412	12-Bit, 3Msps Parallel ADC	±5V Supply, ±2.5V Span, 72dB SINAD
LCT1414	14-Bit, 2.2Msps Parallel ADC	±5V Supply, ±2.5V Span, 78dB SINAD
LTC1420	12-Bit, 10Msps Parallel ADC	5V, Selectable Spans, 72dB SINAD
LTC1604	16-Bit, 333ksps Parallel ADC	±5V Supply, ±2.5V Span, 90dB SINAD
LTC1608	16-Bit, 500ksps Parallel ADC	±5V Supply, ±2.5V Span, 90dB SINAD
LTC1609	16-Bit, 250ksps Serial ADC	5V, Configurable Bipolar/Unipolar Inputs
LTC1864/LTC1865	16-Bit, 250ksps Serial ADCs	5V Supply, 1 and 2 Channel, 4.3mW, MSOP Package
LTC2355-12/ LTC2355-14	12-Bit, 3.5Msps Serial ADCs	3.3V Supply, 0V to 2.5V Span, MSOP Package
LTC2356-12/LTC2356-14	12-/14-Bit, 3.5Msps Serial ADCs	3.3V Supply, ±1.25V Span, MSOP Package
DACs		
LTC1666/LTC1667/LTC1668	12-/14-/16-Bit, 50Msps DACs	87dB SFDR, 20ns Settling Time
LTC1592	16-Bit, Serial SoftSpan™ I_{OUT} DAC	±1LSB INL/DNL, Software Selectable Spans
References		
LT1790-2.5	Micropower Series Reference in SOT-23	0.05% Initial Accuracy, 10ppm Drift
LT1461-2.5	Precision Voltage Reference	0.04% Initial Accuracy, 3ppm Drift
LT1460-2.5	Micropower Series Voltage Reference	0.1% Initial Accuracy, 10ppm Drift

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