Rail-to-Rail, Very Low Noise Universal Dual Filter Building Block

FEATURES

- **Rail-to-Rail Input and Output Operation**
- **Operates from a Single 3V to ±5V Supply**
- **Dual 2nd Order Filter in a 16-Lead SSOP Package**
- > 80dB Dynamic Range on Single 3.3V Supply
- Clock-to-Center Frequency Ratio of 100:1 for the LTC1067 and 50:1 for the LTC1067-50
- Internal Sampling-to-Center Frequency Ratio of 200:1 for the LTC1067 and 100:1 for the LTC1067-50
- Center Frequency Error < ±0.2% Typ
- Low Noise: < 40μV_{RMS}, Q ≤ 5
- Customizable with Internal Resistors

APPLICATIONS

- Notch Filters
- Narrowband Bandpass Filters
- Tone Detection
- Noise Reduction Systems

DESCRIPTION

The LTC®1067/LTC1067-50 consist of two identical rail-to-rail, high accuracy and very wide dynamic range 2nd order switched-capacitor building blocks. Each building block, together with three to five resistors, provides 2nd order filter functions such as bandpass, highpass, lowpass, notch and allpass. High precision 4th order filters are easily designed.

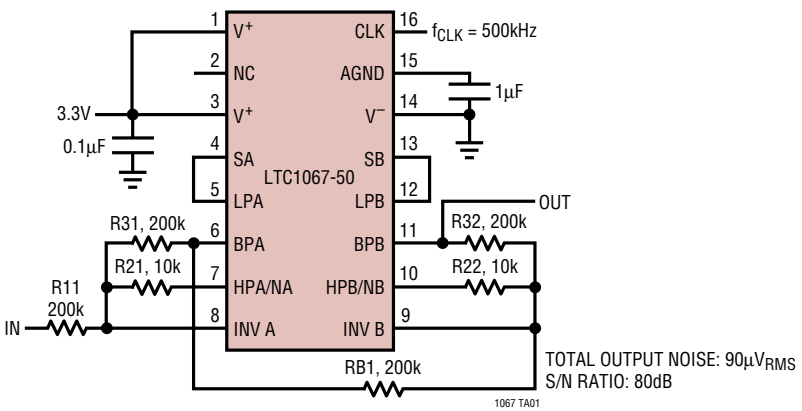
The center frequency of each 2nd order section is tuned by the external clock frequency. The internal clock-to-center frequency ratio (100:1 for the LTC1067 and 50:1 for the LTC1067-50) can be modified by the external resistors. These devices have a double sampled architecture which places aliasing and imaging components at twice the clock frequency. The LTC1067-50 is a low power device consuming about one half the current of the LTC1067. The LTC1067-50's typical supply current is about 1mA from a 3.3V supply.

The LTC1067 and LTC1067-50 are available in 16-pin narrow SSOP and SO packages.

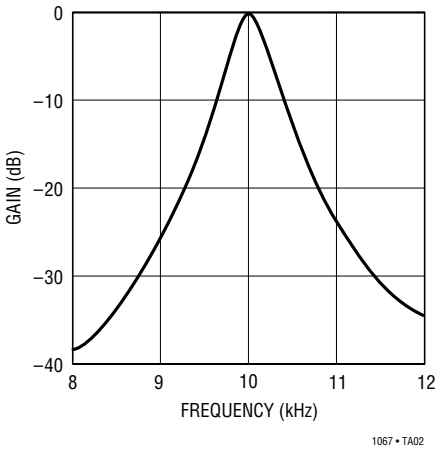
Mask programmable versions of the LTC1067 and LTC1067-50, with thin film resistors on-chip and custom clock-to-cutoff frequency ratios, can be designed in an SO-8 package to realize application specific monolithic filters. Please contact LTC Marketing for more details.

TYPICAL APPLICATION

Single 3.3V Supply Rail-to-Rail, 4th Order, 10kHz Bandpass Filter



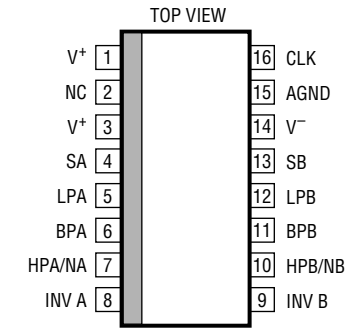
Frequency Response



ABSOLUTE MAXIMUM RATINGS

Total Voltage Supply (V^+ to V^-) 12V
Input Voltage ..... (V^+ + 0.3V) to (V^- – 0.3V)
Output Short-Circuit Duration ..... Indefinite
Power Dissipation 500mV
Operating Temperature Range
LTC1067C ..... 0°C to 70°C
LTC1067I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



GN PACKAGE
16-LEAD PLASTIC SSOP

S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 110°C, θ_{JA} = 135°C/W (GN)
T_{JMAX} = 110°C, θ_{JA} = 115°C/W (S)

ORDER PART NUMBER

LTC1067CGN
LTC1067-50CGN
LTC1067IGN
LTC1067-50IGN
LTC1067CS
LTC1067-50CS
LTC1067IS
LTC1067-50IS

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

LTC1067 (internal op amps) V_S = 4.75V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range			3		11	V
Positive Output Voltage Swing	V_S = 3V, R_L = 10k	●	2.65	2.80		V
	V_S = 4.75V, R_L = 10k	●	4.25	4.50		V
	V_S = ±5V, R_L = 10k	●	4.15	4.50		V
Negative Output Voltage Swing	V_S = 3V, R_L = 10k	●		0.020	0.200	V
	V_S = 4.75V, R_L = 10k	●		0.025	0.225	V
	V_S = ±5V, R_L = 10k	●		–4.96	–4.80	V
Output Short-Circuit Current (Source/Sink)	V_S = 3V			16/1.0		mA
	V_S = 4.75V			33/2.2		mA
	V_S = ±5V			70/7.2		mA
DC Open-Loop Gain	R_L = 10k			90		dB
GBW Product	R_L = 10k			2.8		MHz
Slew Rate	R_L = 10k			2.25		V/µs

LTC1067 (complete filter) V_S = 4.75V, f_{CLK} = 250kHz, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_O (Note 1)				0.001 to 20		kHz
Input Frequency Range				0 to 1		MHz
Clock-to-Center Frequency, f_{CLK}/f_O	V_S = 3V, f_{CLK} = 250kHz, Mode 1, f_O = 2.5kHz, Q = 5			100:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.70	%
	V_S = 4.75V, f_{CLK} = 250kHz, Mode 1, f_O = 2.5kHz, Q = 5			100:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.70	%
	V_S = ±5V, f_{CLK} = 500kHz, Mode 1, f_O = 5kHz, Q = 5			100:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.70	%
Clock-to-Center Frequency Ratio, Side-to-Side Matching	V_S = 3V, f_{CLK} = 250kHz, Q = 5	●		±0.1	±0.35	%
	V_S = 4.75V, f_{CLK} = 250kHz, Q = 5	●		±0.1	±0.35	%
	V_S = ±5V, f_{CLK} = 500kHz, Q = 5	●		±0.1	±0.35	%

ELECTRICAL CHARACTERISTICS

LTC1067 (complete filter) V_S = 4.75V, f_{CLK} = 250kHz, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Q Accuracy	V_S = 3V, f_{CLK} = 250kHz, Q = 5	●		±0.5	±2	%
	V_S = 4.75V, f_{CLK} = 250kHz, Q = 5	●		±0.5	±2	%
	V_S = ±5V, f_{CLK} = 500kHz, Q = 5	●		±0.5	±2	%
f_0 Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (See Table 2)	V_{OS1} (DC Offset of Input Inverter)	●		±3	±18	mV
	V_{OS2} (DC Offset of First Integrator)	●		±4	±22	mV
	V_{OS3} (DC Offset of Second Integrator)	●		±4	±22	mV
Clock Feedthrough				150		μV_{RMS}
Maximum Clock Frequency	Q < 2.5, V_S = ±5V			2.0		MHz
Power Supply Current	V_S = 3V, f_{CLK} = 250kHz	●		2.50	4.5	mA
	V_S = 4.75V, f_{CLK} = 250kHz	●		3.00	5.5	mA
	V_S = ±5V, f_{CLK} = 500kHz	●		4.35	7.5	mA

LTC1067-50 (internal op amps) V_S = 4.75V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Supply Range			2.7		11	V
Positive Output Voltage Swing	V_S = 3V, R_L = 10k	●	2.65	2.80		V
	V_S = 4.75V, R_L = 10k	●	4.25	4.50		V
	V_S = ±5V, R_L = 10k	●	4.15	4.50		V
Negative Output Voltage Swing	V_S = 3V, R_L = 10k	●		0.020	0.200	V
	V_S = 4.75V, R_L = 10k	●		0.025	0.225	V
	V_S = ±5V, R_L = 10k	●		–4.96	–4.80	V
Output Short-Circuit Current (Source/Sink)	V_S = 3V			16/0.6		mA
	V_S = 4.75V			33/1.2		mA
	V_S = ±5V			70/5.7		mA
DC Open-Loop Gain	R_L = 10k			90		dB
GBW Product	R_L = 10k			1.9		MHz
Slew Rate	R_L = 10k			0.8		V/µs

LTC1067-50 (complete filter) V_S = 4.75V, f_{CLK} = 125kHz, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Center Frequency Range, f_0 (Note 1)				0.001 to 40		kHz
Input Frequency Range				0 to 1		MHz
Clock-to-Center Frequency, f_{CLK}/f_0	V_S = 3V, f_{CLK} = 125kHz, Mode 1, f_0 = 2.5kHz, Q = 5			50:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.75	%
	V_S = 4.75V, f_{CLK} = 125kHz, Mode 1, f_0 = 2.5kHz, Q = 5			50:1 ±0.2		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.75	%
	V_S = ±5V, f_{CLK} = 250kHz, Mode 1, f_0 = 5kHz, Q = 5			50:1 ±0.3		%
	R1 = R3 = 49.9k, R2 = 10k	●			±0.75	%
Clock-to-Center Frequency Ratio, Side-to-Side Matching	V_S = 3V, f_{CLK} = 125kHz, Q = 5	●		±0.2	±0.55	%
	V_S = 4.75V, f_{CLK} = 125kHz, Q = 5	●		±0.2	±0.55	%
	V_S = ±5V, f_{CLK} = 250kHz, Q = 5	●		±0.2	±0.55	%
Q Accuracy	V_S = 3V, f_{CLK} = 125kHz, Q = 5	●		±0.5	±2	%
	V_S = 4.75V, f_{CLK} = 125kHz, Q = 5	●		±0.5	±2	%
	V_S = ±5V, f_{CLK} = 250kHz, Q = 5	●		±0.5	±2	%

ELECTRICAL CHARACTERISTICS

LTC1067-50 (complete filter) V_S = 4.75V, f_{CLK} = 125kHz, T_A = 25°C, unless otherwise noted.

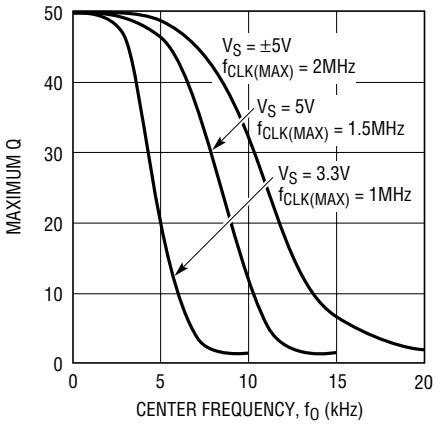
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_0 Temperature Coefficient				±1		ppm/°C
Q Temperature Coefficient				±5		ppm/°C
DC Offset Voltage (See Table 2)	V_{OS1} (DC Offset of Input Inverter)	●		±3	±18	mV
	V_{OS2} (DC Offset of First Integrator)	●		±4	±22	mV
	V_{OS3} (DC Offset of Second Integrator)	●		±4	±22	mV
Clock Feedthrough				150		μV_{RMS}
Maximum Clock Frequency	Q < 2.5, V_S = ±5V			2.0		MHz
Power Supply Current	V_S = 3V, f_{CLK} = 125kHz	●		1.00	2.5	mA
	V_S = 4.75V, f_{CLK} = 125kHz	●		1.45	3.0	mA
	V_S = ±5V, f_{CLK} = 250kHz	●		2.35	4.0	mA

The ● denotes the specifications which apply over the full operating temperature range.

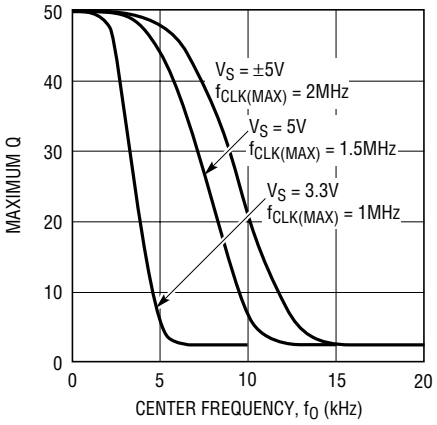
Note 1: See Typical Performance Characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

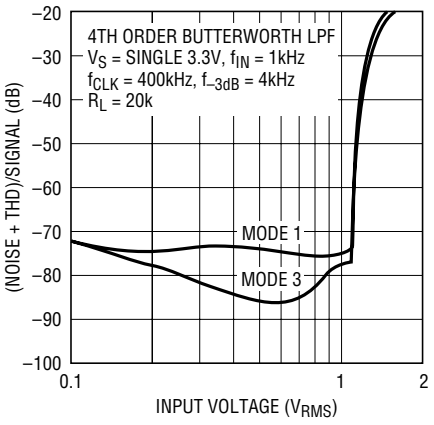
LTC1067 Maximum Q vs Center Frequency (Modes 1, 1B, 2 where R4 ≥ 10R2)



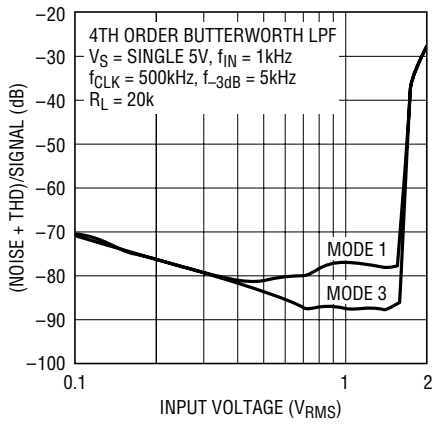
LTC1067 Maximum Q vs Center Frequency (Modes 2 where R4 < 10R2, 3)



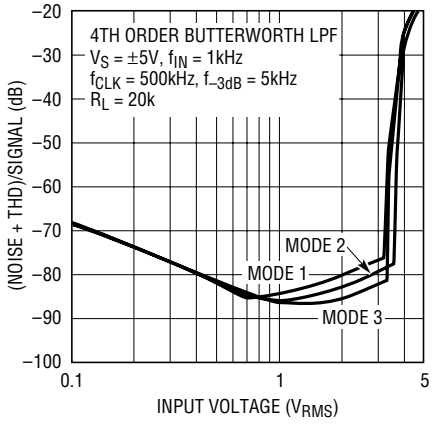
LTC1067 Noise + THD vs Input Voltage



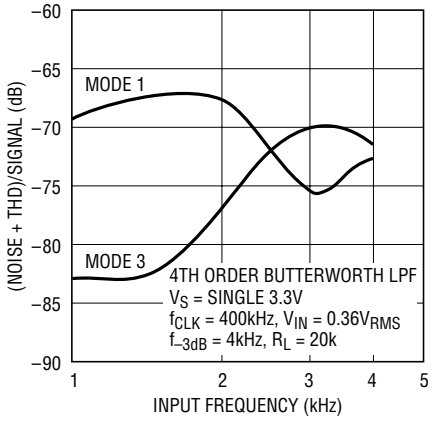
LTC1067 Noise + THD vs Input Voltage



LTC1067 Noise + THD vs Input Voltage

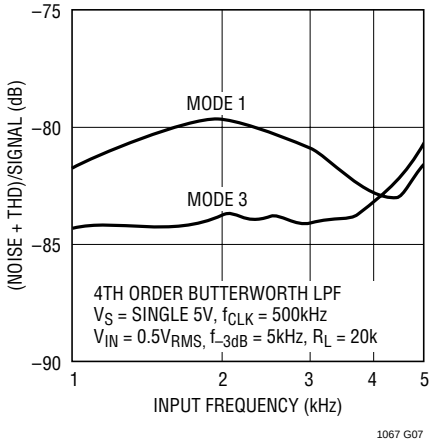


LTC1067 Noise + THD vs Input Frequency

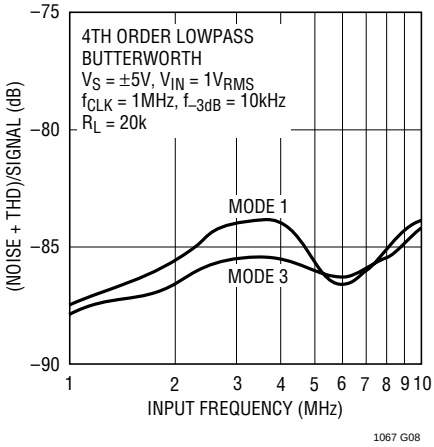


TYPICAL PERFORMANCE CHARACTERISTICS

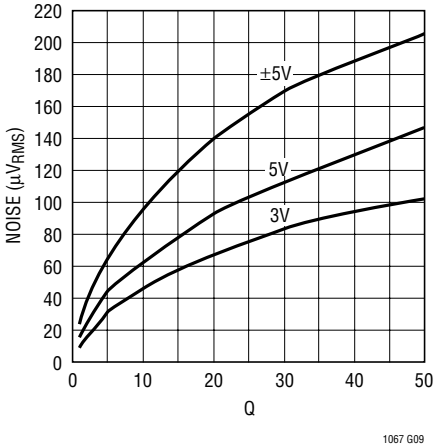
LTC1067
Noise + THD vs Input Frequency



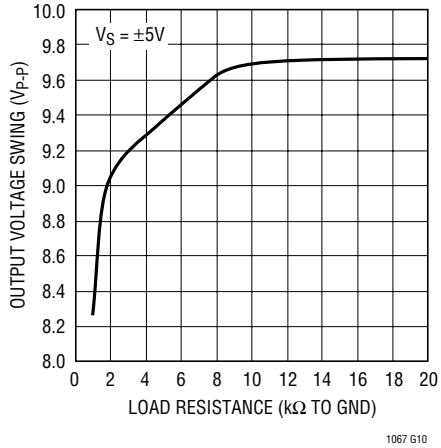
LTC1067
Noise + THD vs Input Frequency



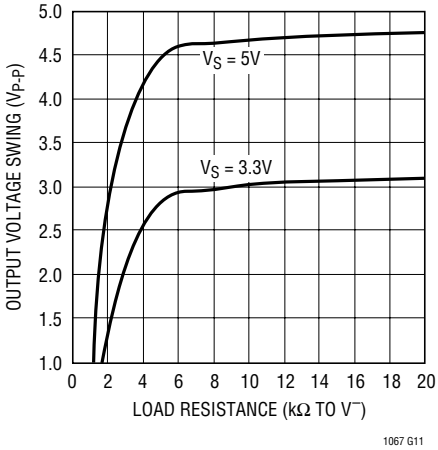
LTC1067
Noise vs Q



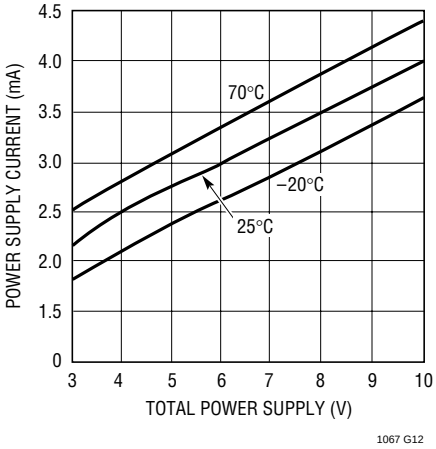
LTC1067
Output Voltage Swing vs Load Resistance, ±5V Supply Voltage



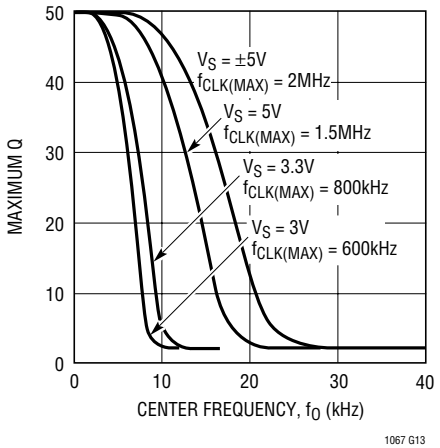
LTC1067
Output Voltage Swing vs Load Resistance, Single Supply Voltage



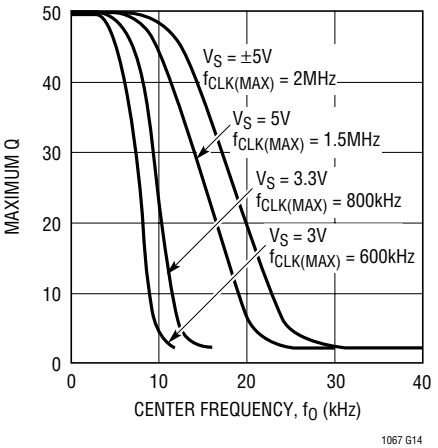
LTC1067
Power Supply Current vs Power Supply



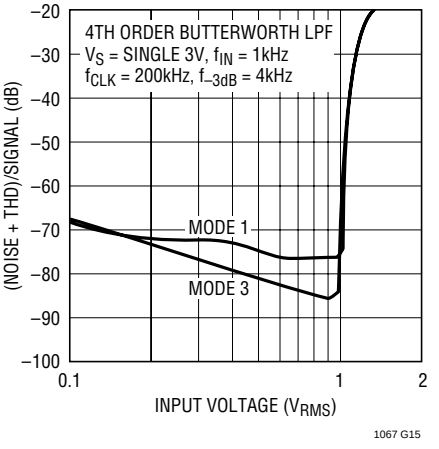
LTC1067-50
Maximum Q vs Center Frequency (Modes 2 Where R4 < 10R2, 3)



LTC1067-50
Maximum Q vs Center Frequency (Modes 1, 1B, 2 Where R4 ≥ 10R2)

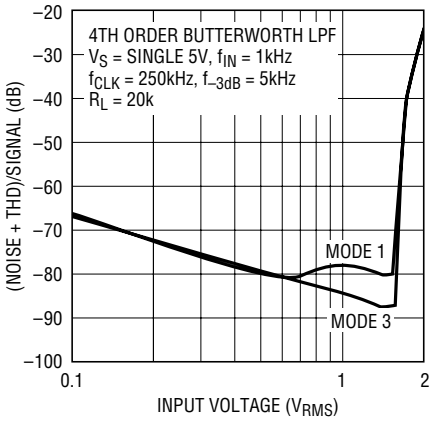


LTC1067-50
Noise + THD vs Input Voltage

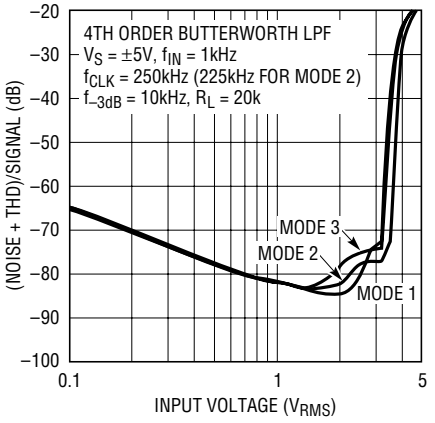


TYPICAL PERFORMANCE CHARACTERISTICS

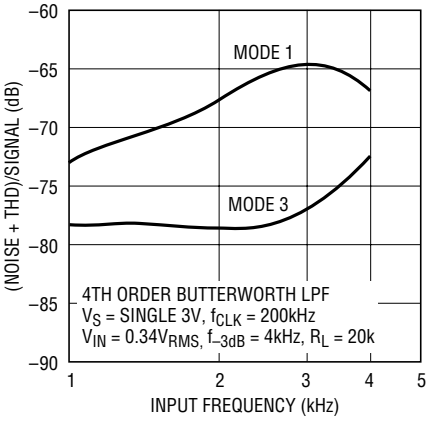
LTC1067-50
Noise + THD vs Input Voltage



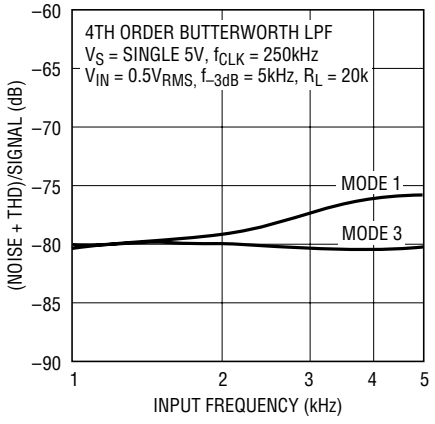
LTC1067-50
Noise + THD vs Input Voltage



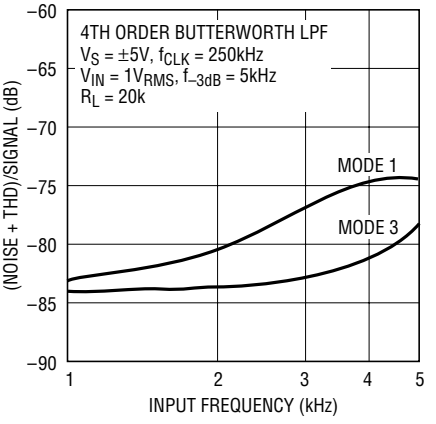
LTC1067-50
Noise + THD vs Input Frequency



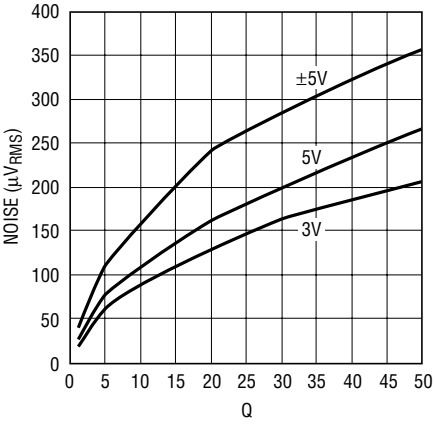
LTC1067-50
Noise + THD vs Input Frequency



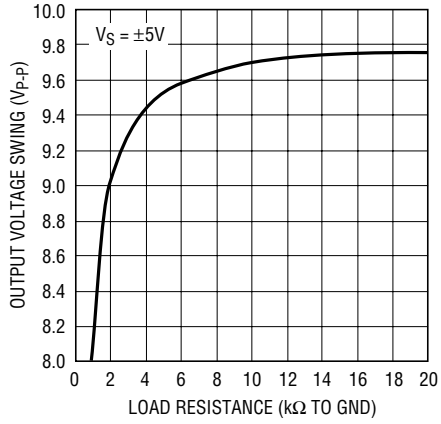
LTC1067-50
Noise + THD vs Input Frequency



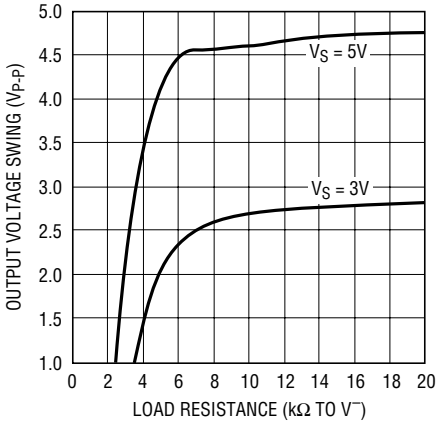
LTC1067-50
Noise vs Q



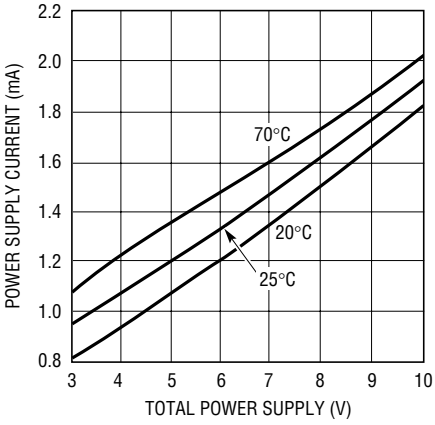
LTC1067-50
Output Voltage Swing vs Load Resistance, ±5V Supply Voltage



LTC1067-50
Output Voltage Swing vs Load Resistance, Single Supply Voltage

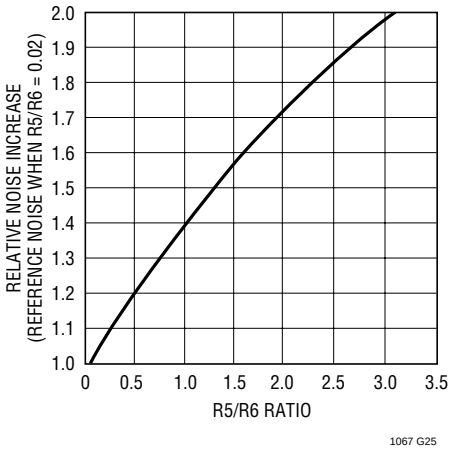


LTC1067-50
Power Supply Current vs Power Supply

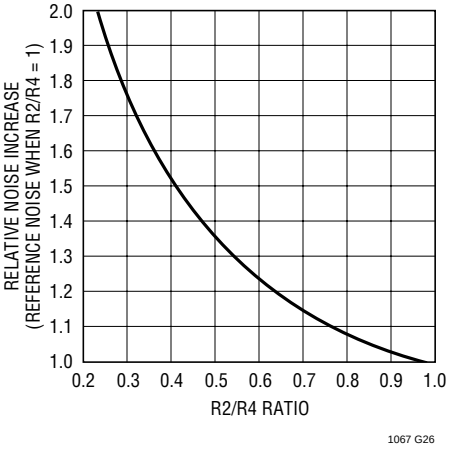


TYPICAL PERFORMANCE CHARACTERISTICS

LTC1067/LTC1067-50 Mode 1B
Noise Increase vs R5/R6 Ratio



LTC1067/LTC1067-50 Mode 3
Noise Increase vs R2/R4 Ratio



PIN FUNCTIONS

V⁺, V⁻ (Pins 1, 3,14): The V⁺ (Pins 1, 3) and the V⁻ (Pin 14) should each be bypassed with a 0.1µF capacitor to an adequate analog ground. The filter's power supplies should be isolated from other digital or high voltage analog supplies. A low noise linear supply is recommended. Using a switching power supply will lower the signal-to-noise ratio of the filter. The supply's power-up slew rate should be less than 1V/µs. When V⁺ is applied before V⁻, and V⁻ is allowed to go above ground, a diode should clamp V⁻ to prevent latch-up. Figures 1 and 2 show typical connections for dual and single supply operation.

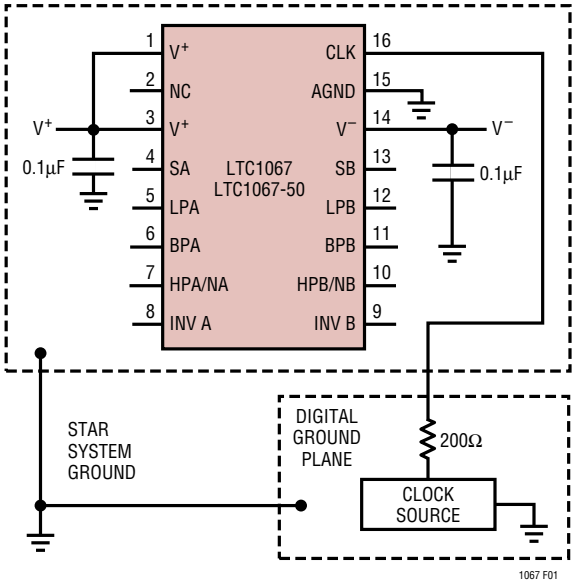
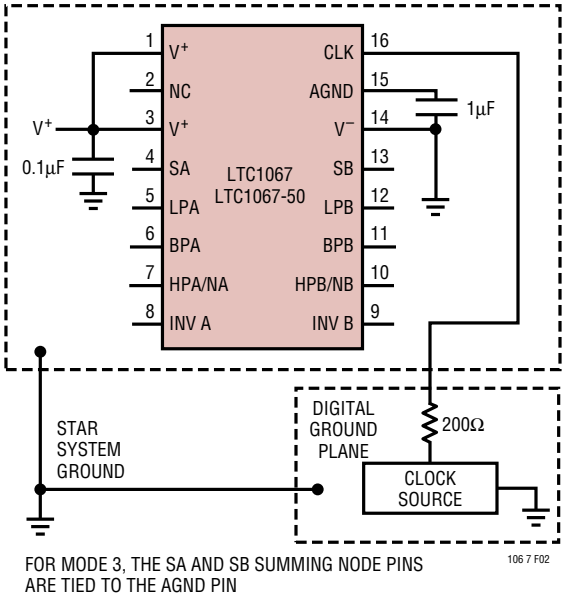


Figure 1. Dual Supply Ground Plane Connections



FOR MODE 3, THE SA AND SB SUMMING NODE PINS ARE TIED TO THE AGND PIN

Figure 2. Single Supply Ground Plane Connections

PIN FUNCTIONS

SA, SB (Pins 4, 13): Summing Inputs. The summing pins' connection, along with the other resistor connections, determine the circuit topology (mode) of each 2nd order section. These pins should never be left floating.

LPA, BPA, HPA/NA, HPB/NB, BPB, LPB (Pins 5, 6, 7, 10, 11, 12): Output Pins. Each 2nd order section of the LTC1067 has three outputs which typically source 33mA and sink 2mA. Driving coaxial cable, capacitive loads or resistive loads less than 10k will degrade the total harmonic distortion performance of any filter design. Refer to Output Loading in the Applications Information section for more details. When evaluating the distortion or noise performance of a filter, the output should be buffered with a wideband amplifier.

INV A, INV B (Pins 8, 9): Inverting Input. These pins are the high impedance inverting inputs of internal op amps. They are susceptible to stray capacitance coupling to low impedance nodes such as signal outputs and power supply lines. Resistors that are connected from a signal output to the inverting input pin should be located as close to the inverting input as possible.

AGND (Pin 15): Analog Ground. The filter performance depends on the quality of the analog signal ground. For either dual or single supply operation, an analog ground plane surrounding the package is recommended. The analog ground plane should be connected to any digital ground at a single point. For dual supply operation Pin 15 is connected to the analog ground plane. For single supply operation Pin 15 should be bypassed to the analog ground plane with at least a 1μF capacitor. An on-chip resistive voltage divider sets the bias at one-half of the supply.

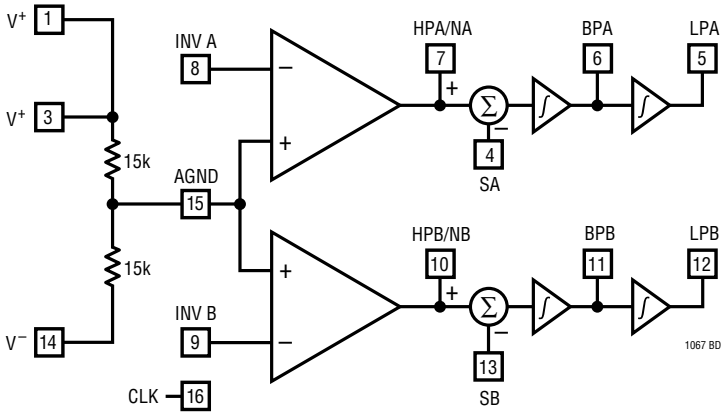
CLK (Pin 16): Clock Input. Any CMOS logic clock source with a square-wave output and a 50% duty cycle (±10%) is an adequate clock source for the device. The power supply for the clock source should not be the filter's power supply. The analog ground for the filter should be connected to the clock's ground at a single point only. Table 1 shows the clock's low and high level threshold values for dual supply or single supply operation. Logic low level signals must be greater than the negative supply voltage. With a ±5V power supply, the clock levels may be either ±5V or 0V to 5V. Logic high level signals should be less than the positive supply voltage. However, when the positive supply voltage is either 3V or 3.3V, the clock signal can be as high as 5.5V.

Table 1. Clock Source High and Low Threshold Levels

POWER SUPPLY	HIGH LEVEL	LOW LEVEL
±5V	≥ 2.2V	≤ 0.50V
Single 5V	≥ 2.2V	≤ 0.50V
Single 3V, 3.3V	≥ 2V	≤ 0.40V

Sine waves are not recommended for the clock input. The clock signal should be routed from the right side of the IC package to avoid coupling to any power supply lines or input or output signal paths. A 200Ω resistor between the clock source and Pin 16 will slow down the rise and fall times of the clock to reduce charge coupling of the clock. This will result in less clock feedthrough noise on the output signal.

BLOCK DIAGRAM



MODES OF OPERATION

Linear Technology's universal switched-capacitor filters are designed with a fixed internal, nominal f_{CLK}/f_O ratio. The LTC1067 has a 100:1 f_{CLK}/f_O ratio and the LTC1067-50 has a 50:1 f_{CLK}/f_O ratio. Filter designs often require the f_{CLK}/f_O ratio of each section to be different from the nominal ratio and in most cases different from each other. Ratios other than the nominal value are possible with external resistors. Operating modes use external resistors, connected in different arrangements to realize different f_{CLK}/f_O ratios. By choosing the proper mode, the f_{CLK}/f_O ratio can be increased or decreased from the part's nominal ratio.

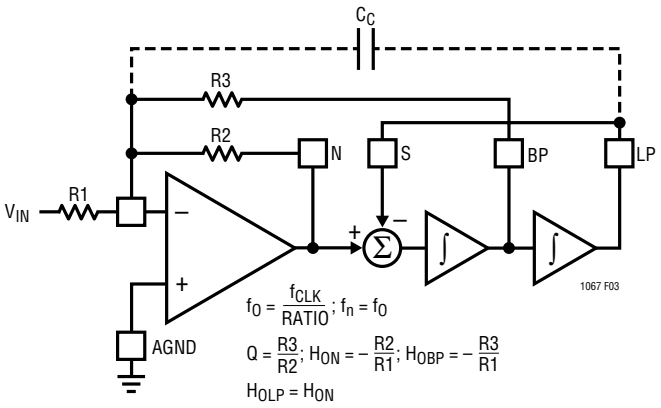
The choice of operating mode also effects the transfer function at the HP/N pins. The LP and BP pins always give the lowpass and bandpass transfer functions respectively, regardless of the mode utilized. The HP/N pins have a different transfer function depending on the mode used. Mode 1 yields a notch transfer function. Mode 3 yields a highpass transfer function. Mode 2 yields a highpass-notch transfer function (i.e., a highpass with a stopband notch). More complex transfer functions, such as lowpass-notch, allpass or complex zeros, are achieved by summing two or more of the LP, BP or HP/N outputs. This is illustrated in sections Mode 2n and Mode 3a.

Choosing the proper mode(s) for a particular application is not trivial and involves much more than just adjusting the f_{CLK}/f_O ratio. Listed here are six of the nearly twenty modes available. To make the design process simpler and quicker, Linear Technology has developed the FilterCAD™ for Windows® design software. FilterCAD is an easy-to-use, powerful and interactive filter design program. The designer can enter a few filter specifications and the program produces a full schematic. FilterCAD allows the designer to concentrate on the filter's transfer function and not get bogged down in the details of the design. Alternatively, those who have experience with the Linear Technology family of parts can control all of the details themselves. For a complete listing of all the operating modes, consult the appendices of the FilterCAD manual or the Help files in FilterCAD. FilterCAD can be obtained free of charge on the Linear Technology web site (http://www.linear-tech.com) or you can order the FilterCAD CD-ROM by contacting Linear Technology's marketing department.

Mode 1

In Mode 1, the ratio of the external clock frequency to the center frequency of each 2nd order section is internally fixed at the part's nominal ratio. Figure 3 illustrates Mode 1 providing 2nd order notch, lowpass and bandpass outputs. Mode 1 can be used to make high order Butterworth lowpass filters; it can also be used to make low Q notches and for cascading 2nd order bandpass functions tuned at the same center frequency. Mode 1 is faster than Mode 3.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.



NOTE: RATIO = 100 FOR LTC1067
= 50 FOR LTC1067-50

Figure 3. Mode 1, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

Mode 1b

Mode 1b is derived from Mode 1. In Mode 1b (Figure 4) two additional resistors R5 and R6 are added to lower the amount of voltage fed back from the lowpass output into the input of the SA (or SB) switched-capacitor summer. This allows the filter's clock-to-center frequency ratio to be adjusted beyond the part's nominal ratio. Mode 1b maintains the speed advantages of Mode 1 and should be considered an optimum mode for high Q designs with f_{CLK} to f_{CUTOFF} (or f_{CENTER}) ratios greater than the part's nominal ratio.

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Windows is a registered trademark of Microsoft Corporation.

MODES OF OPERATION

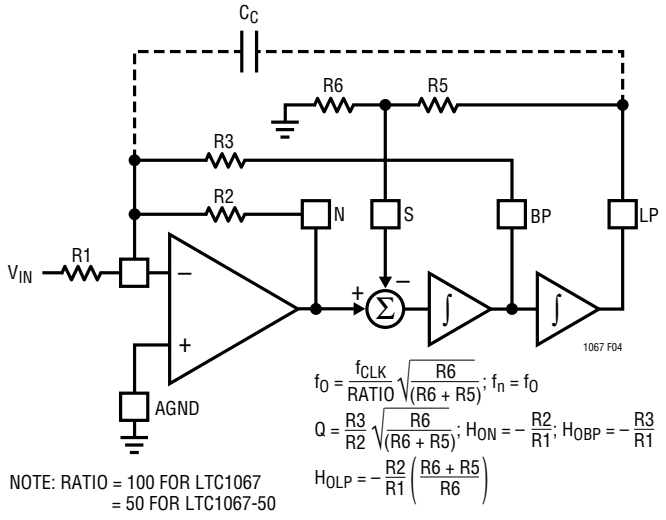


Figure 4. Mode 1b, 2nd Order Filter Providing Notch, Bandpass and Lowpass Outputs

The parallel combination of R5 and R6 should be kept below 5k.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 3

In Mode 3, the ratio of the external clock frequency to the center frequency of each 2nd order section can be adjusted above or below the part's nominal ratio. Figure 5 illustrates Mode 3, the classical state variable configuration, providing highpass, bandpass and lowpass 2nd order filter functions. Mode 3 is slower than Mode 1. Mode 3 can be used to make high order all-pole bandpass, lowpass and highpass filters.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2

Mode 2 is a combination of Mode 1 and Mode 3, shown in Figure 6. With Mode 2, the clock-to-center frequency ratio, f_{CLK}/f_O, is always less than the part's nominal ratio. The advantage of Mode 2 is that it provides less sensitivity to resistor tolerances than does Mode 3. Mode 2 has a highpass-notch output where the notch frequency depends solely on the clock frequency and is therefore less than the center frequency, f_O.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

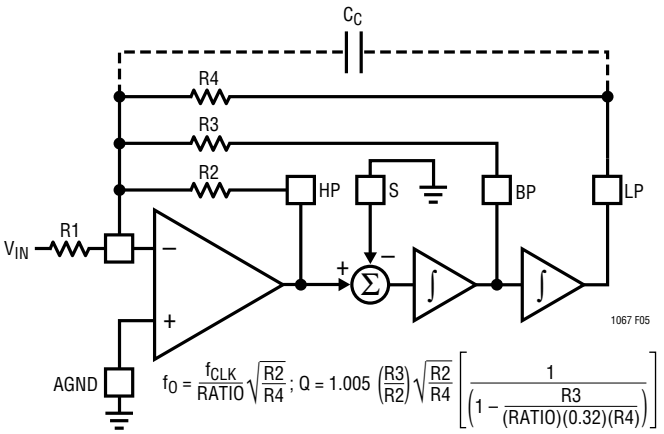
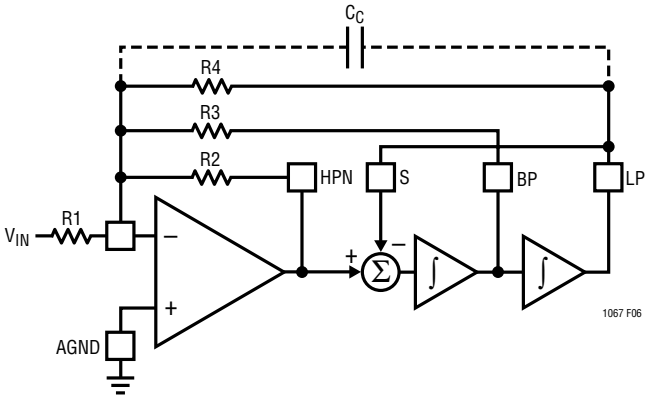


Figure 5. Mode 3, 2nd Order Section Providing Highpass, Bandpass and Lowpass Outputs



$f_O = \frac{f_{CLK}}{RATIO}\sqrt{1+\frac{R2}{R4}}$; $f_n = \frac{f_{CLK}}{RATIO}$

$Q = 1.005\left(\frac{R3}{R2}\right)\sqrt{1+\frac{R2}{R4}}\left[\frac{1}{\left(1-\frac{R3}{(RATIO)(0.32)(R4)}\right)}\right]$

$H_{OHPN} = -\frac{R2}{R1}$ (AC GAIN, $f >> f_O$); $H_{OHPN} = -\frac{R2}{R1}\left[\frac{1}{\left(1+\frac{R2}{R4}\right)}\right]$ (DC GAIN)

$H_{OBP} = -\frac{R3}{R1}\left[\frac{1}{\left(1-\frac{R3}{(RATIO)(0.32)(R4)}\right)}\right]$; $H_{OLP} = -\frac{R2}{R1}\left[\frac{1}{\left(1+\frac{R2}{R4}\right)}\right]$

NOTE: RATIO = 100 FOR LTC1067
= 50 FOR LTC1067-50

Figure 6. Mode 2, 2nd Order Filter Providing Highpass Notch, Bandpass and Lowpass Outputs

MODES OF OPERATION

Mode 3a

This is an extension of Mode 3 where the highpass and lowpass outputs are summed through two external resistors, R_H and R_L, to create a notch (see Figure 7). Mode 3a is more versatile than Mode 2 because the notch frequency can be higher or lower than the center frequency of the 2nd order section. The external op amp of Figure 7 is not always required. When cascading the sections of the LTC1067, the highpass and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

Mode 2n

This mode extends the circuit topology of Mode 3a to Mode 2 (Figure 8) where the highpass-notch and lowpass outputs are summed through two external resistors, R_H and R_L, to create a lowpass output with a notch higher in frequency than the notch in Mode 2. This mode, shown in Figure 8, is most useful in lowpass elliptic designs. When cascading the sections of the LTC1067, the highpass-notch and lowpass outputs can be summed directly into the inverting input of the next section.

Please refer to the Operating Limits paragraph under Applications Information for a guide to the use of capacitor C_C.

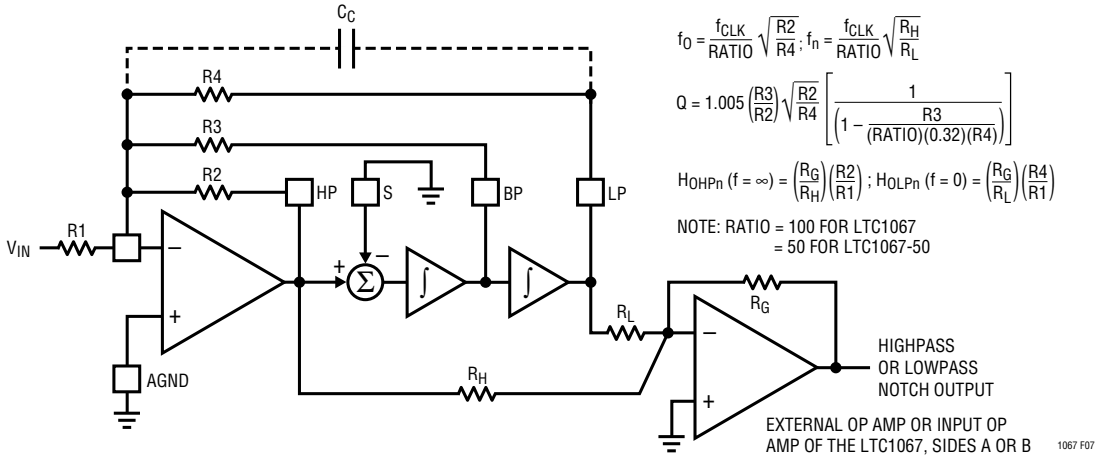


Figure 7. Mode 3a, 2nd Order Filter Providing a Highpass Notch or Lowpass Notch Output

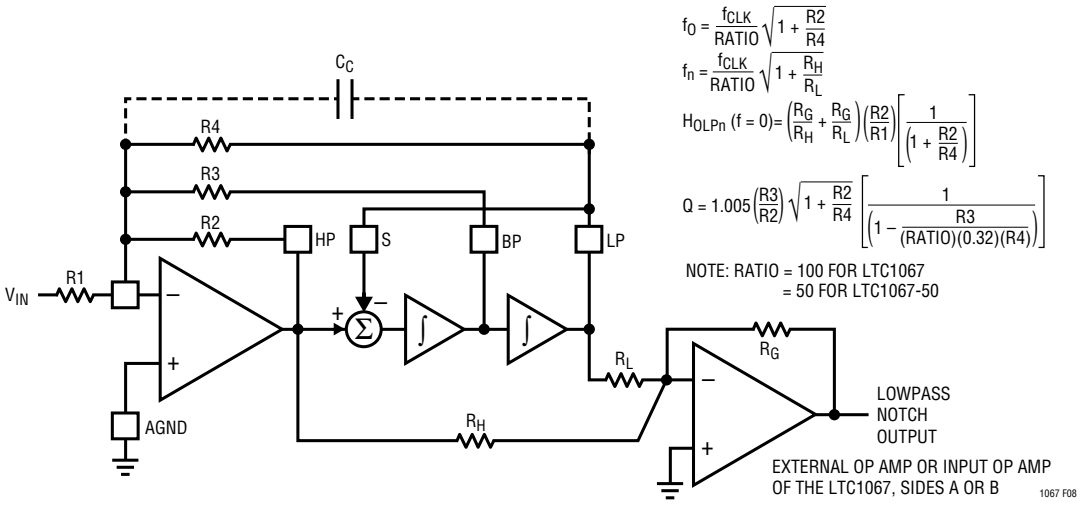


Figure 8. Mode 2n, 2nd Order Filter Providing a Lowpass Notch Output

APPLICATIONS INFORMATION

A switched-capacitor integrator generally exhibits a higher input offset than a discrete RC integrator. The larger offset is mainly due to the charge injection from the CMOS switches into the integrated capacitor. The integrator's op amp offset, typically a couple of millivolts, also adds to the overall offset value. Figure 9 shows the input offsets from a single 2nd order section. Table 2 lists the formula for the output offset voltage for various modes and output pins.

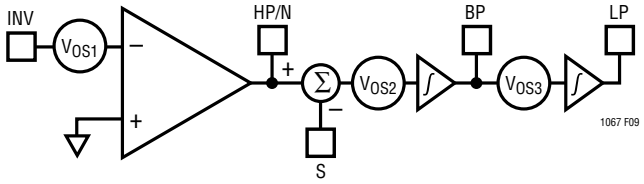


Figure 9. Block Diagram of a 2nd Order Section Showing the Input Offsets

Operating Limits

The Maximum Q vs Frequency (f_0) graphs, under Typical Performance Characteristics, define an upper limit of operating Q for each LTC1067 (or LTC1067-50) 2nd order section. These graphs indicate the power supply, f_0 and Q value conditions under which a filter implemented with an LTC1067 will remain stable when operated at temperatures of 70°C or less. For a 2nd order section, a bandpass gain error of 3dB or less is arbitrarily defined as a condition for stability.

When the passband gain error begins to exceed 1dB, the use of capacitor C_C will reduce the gain error (capacitor C_C is connected from the lowpass node to the inverting node of a 2nd order section). Please refer to Figures 3 through 8. The value of C_C can be best determined experimentally, and as a guide it should be about 5pF for each 1dB of gain error and not to exceed 15pF. When operating the LTC1067 near the limits defined by the Typical Performance Characteristics graphs, passband gain variations of 2dB or more should be expected.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output pins. The clock feedthrough is tested with the filter's input grounded and depends on PC board layout and on the value of the power supplies. With proper layout techniques, the typical values of clock feedthrough are listed under Electrical Characteristics.

Any parasitic switching transients during the rising and falling edges of the incoming clock are not part of the clock feedthrough specifications. Switching transients have frequency contents much higher than the applied clock; their amplitude strongly depends on scope probing techniques as well as grounding and power supply bypassing. The clock feedthrough, can be greatly reduced by adding a simple RC lowpass network at the final filter output. This RC will completely eliminate any switching transients.

Wideband Noise

The wideband noise of the filter is the total RMS value of the device's noise spectral density and is used to determine the operating signal-to-noise ratio. Most of its frequency contents lie within the filter passband and cannot be reduced with post filtering. For a notch filter the noise of the filter is centered at the notch frequency.

The total wideband noise (μV_{RMS}) is nearly independent of the value of the clock. The clock feedthrough specifications are not part of the wideband noise.

For a specific filter design, the total noise depends on the Q of each section and the cascade sequence.

Table 2. Output DC Offsets for a Second Order Section

MODE	$V_{OSHP/N}$	V_{OSBP}	V_{OSLP}
1	V_{OS1} [1 + (R2/R3) + (R2/R1)] – (V_{OS3})(R2/R3)	V_{OS3}	$V_{OSHP/N} – V_{OS2}$
1b	V_{OS1} [1 + (R2/R3) + (R2/R1)] – (V_{OS3})(R2/R3)	V_{OS3}	($V_{OSHP/N} – V_{OS2}$)[1 + (R5/R6)]
2	V_{OS1} [1 + (R2/R3) + (R2/R1) + (R2/R4) – (V_{OS3}) (R2/R3)](R4/R2 + R4) + (V_{OS2})(R2/R2 + R4)	V_{OS3}	$V_{OSHP/N} – V_{OS2}$
3	V_{OS2}	V_{OS3}	V_{OS1} [1 + (R4/R1) + (R4/R2) + (R4/R3)] – (V_{OS2}) (R4/R2) – (V_{OS3})(R4/R3)

APPLICATIONS INFORMATION

Aliasing

Aliasing is an inherent phenomenon of switched-capacitor filters and occurs when the frequency of the input signals that produce the strongest aliased components have a frequency, f_{IN}, such as ($f_{SAMPLING} - f_{IN}$) that falls into the filter's passband. For both the LTC1067 and the LTC1067-50, the sampling frequency is twice f_{CLK}. If the input signal spectrum is not band limited, aliasing may occur.

Output Loading

The op amps on the LTC1067/LTC1067-50 have a rail-to-rail output stage. The output loading issues can be divided into resistive loading effects and capacitive loading effects.

Resistive loading effects the maximum output signal swing. This effect is shown in the typical performance curves. Note that the load on the output must include both the feedback resistor and any external load resistor. For example, consider the following situation: the part is running on split power supplies, the section is configured in Mode 3, the R4 resistor is 20k and an external 20k load is connected from the LP node to ground. The load on the LP output is 20k in parallel with 20k, or 10k. All testing on the LTC1067/LTC1067-50 is done with a 10k load. For the best results, the load resistance on all output pins should be at least 10k.

Capacitive loading reduces the stability of the op amps. The signal at the output of a switched-capacitor filter is composed of a series of very small steps. The op amp must respond to a step and fully settle before the next step. As the stability of the op amp is decreased, the output step response has increased ringing and a much longer settling time. This longer settling time drastically lowers the maximum usable clock speed and introduces errors. If the capacitive loading is sufficiently high, the stability will be decreased to the point of oscillation at the output.

The LTC1067/LTC1067-50 are sensitive to capacitive loading. Capacitive loading should be kept below 20pF. Good, tight layout techniques should be maintained at all times. These parts should not drive long traces and never drive a long coaxial cable. *When probing the LTC1067 or LTC1067-50, always use a 10× probe. Never use a 1× probe.* A standard 10× probe has a capacitance of 10pF to 15pF while a 1× probe's capacitance can be as high as 150pF. The 1× probe will probably cause oscillation.

What to Do with an Unused Section

If the LTC1067 or LTC1067-50 is used as a single 2nd order filter, the other 2nd order section is not used. Do not leave this section unconnected. If the section is unconnected, inputs and outputs are left to float to undetermined levels and oscillation may occur. The unused section should be connected as shown in Figure 10.

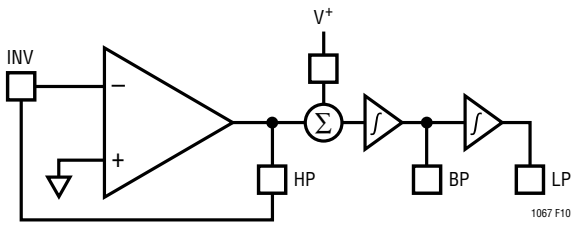


Figure 10. Connections for an Unused Section

Output Voltage Swing on a Single Supply Voltage

The typical performance curves show the output voltage swing limitations. The curves show the output signal swing, in volts peak-to-peak, versus the output load resistance. The peak-to-peak swing is limited by the following three considerations: the op amp's output swings closer to the negative supply than the positive supply, the AGND pin is biased at the midpoint of the supplies and all operating modes are inverting.

The op amps in the LTC1067/LTC1067-50 swing closer to the negative supply rail than the positive supply rail. The positive output voltage swing for single supply operation is shown in Figures 11 and 12. The negative output voltage swing is about 15mV for the LTC1067 and 10mV for the LTC1067-50. The negative output voltage swing is nearly independent of load resistance since the load in this case is connected to the V^- supply rail.

For single supply applications, the on-chip resistor divider sets the voltage at the AGND pin to the midpoint of the V^+ and V^- potentials. The AGND voltage is the reference for all internal op amps. If the input to the filter is at the V^- rail,

APPLICATIONS INFORMATION

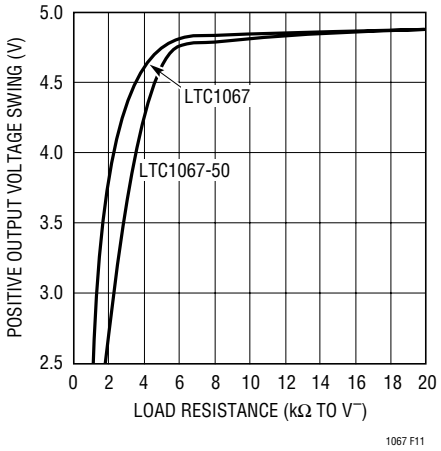


Figure 11. LTC1067/LTC1067-50 Positive Output Voltage Swing vs Load Resistance, 5V Supply

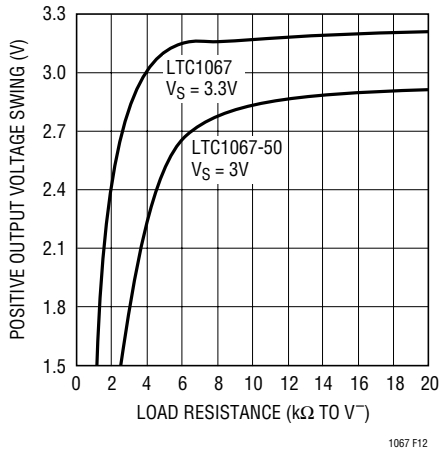


Figure 12. LTC1067/LTC1067-50 Positive Output Voltage Swing vs Load Resistance, 3.3V/3V Supplies

the output of the first section is near the positive rail (operating modes invert the signal). The output of the first stage will saturate at about 250mV (typical for 5V supply) from positive supply. The output from the second stage will be 250mV from the negative supply rail (assuming inversion again) even though the op amp's output is capable of swinging to within 15mV.

The positive output voltage swing being less than the negative swing, coupled with the AGND potential set at the midpoint of the supplies and inverting of the signal, yields the following equation for peak-to-peak output swing:

$$V_{P-P}\ \text{Swing} = (V^+ - V^-) - 2(V^+ - V_{POSITIVE\ SWING})$$

Many applications are more concerned with the negative output swing than the positive output swing. Interfacing to an ADC running on a single 5V supply with a 4.096 reference voltage is a standard example. The LTC1067 or LTC1067-50 will easily reach the 4.096V level for a full-scale reading. The issue is how close does the output go to ground. The further the output is from ground, the more codes that are essentially lost. The previous example demonstrated that the lowest output voltage would be about 250mV, although, as is shown below, 15mV is achievable.

To achieve a lower negative output swing voltage, the AGND voltage must be adjusted down below the midpoint. The AGND voltage is determined by two equal, on-chip resistors. These resistors are typically 15k each. While the ratio of these two resistors is tightly matched, the absolute value of the resistors is not tightly controlled. Adjusting the AGND voltage by simply adding an external resistor can be done, but caution must be exercised.

In Figure 13, a resistor is used to adjust the AGND voltage for use with a 5V powered ADC with a full-scale input of 4.096V. The resistor value was chosen carefully to assure that a 4.096V input signal to the filter yields a full-scale reading from the ADC and a 0V input signal gives the lowest possible value (15mV for the LTC1067 and 10mV for the LTC1067-50). The circuit works well over temperature and part variations. For this application, the 5V supply must be above 4.75V.

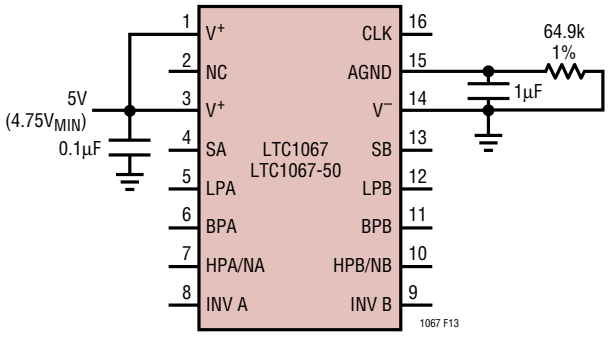


Figure 13. Power and AGND Connections for 5V ADC with 4.096V Full Scale

APPLICATIONS INFORMATION

Figure 14 illustrates how a resistor adjusts the AGND voltage for use with a 3V/3.3V powered ADC with a full-scale input of 2.048V. As in the previous circuit, the resistor value was chosen carefully to assure that a 2.048V input signal to the filter yields a full-scale reading from the ADC and a 0V input signal gives the lowest possible value. For this application, the power supply must be above 2.7V for an LTC1067-50 filter and above 3V for an LTC1067 filter.

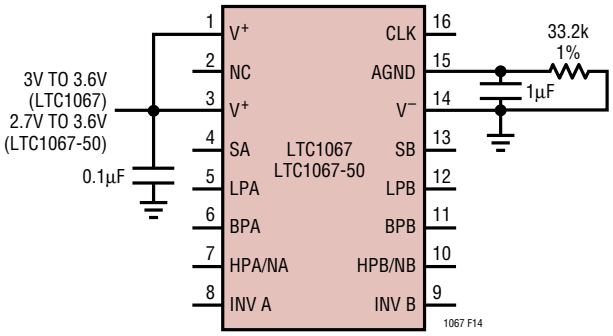


Figure 14. Power and AGND Connections for 3V/3.3V ADC with 2.048V Full Scale

Semi-Custom Filter Program

Linear Technology has in place a program to deliver fully integrated filters, custom designed for any specified application. These semi-custom filters are based on an existing universal filter product with integrated, on-chip resistors. The final filter is then tested to the exact parameters defined for the application. The final result is a fully integrated, accurately tested solution in a smaller package. For the LTC1067 or LTC1067-50 parts, a semi-custom filter comes in the SO-8 package and requires only a clock and a decoupling capacitor. For more details on the semi-custom filter program, contact Linear Technology's marketing department.

Demonstration Board

There is a demonstration board available for the LTC1067/LTC1067-50. Demonstration board 150A has the LTC1067 part installed and the board 150B has the LTC1067-50 installed. The schematic for the board is shown in Figure 15 and the assembly drawing is shown in Figure 16. To obtain a demonstration board, call your local representative or Linear Technology's marketing department.

The demonstration board has all integrated circuits, connectors and decoupling capacitors installed. The board is ready to be configured with the appropriate resistors and jumper connections.

There are two sets of power supply connections. One is for the LTC1067/LTC1067-50 and the other is for the buffering op amp on the board. Having separate connections gives the board the most flexibility. The two sets of supplies can be connected together if a common supply is desired.

When configuring the board for split supply operation, a jumper wire must be installed in the JPAGND position. This connects the AGND pin of the device to the ground plane of the board. The JPVNEG jumper must be left open. The power supply is then connected to V^+, V^- and GND turrets (all of the GND turrets on the board are the same). For single supply operation, insert a wire in the JPVNEG jumper and leave the JPAGND jumper open. This connects the V^- pin to the board's ground plane. The JPAGND jumper must be left open so that the on-chip resistor network can set the AGND potential at the midpoint of the supply. Connect the power supply to V^+ and any GND turret. The V^- turret can be left open or shorted to the adjacent GND turret. If the buffering op amp is run on the same single voltage supply, the VOA^+ turret and the V^+ turrets must be connected together and the VOA^- turret must be shorted to the adjacent GND turret.

The J1 BNC connector is the clock input. There is a 200Ω series resistor connected between the connector and the CLK pin of the part. This resistor, coupled with the CLK pin's input capacitance, slows down the rise and fall times of the clock signal and decreases high frequency coupling. The clock input is not terminated to 50Ω or 75Ω. An external terminator should be used.

Jumpers JP51 and JP61 are connected in parallel with R51 and R61 respectively. Jumper JP51 connects the LPA pin of the part with the SA pin. This can be used for operating modes 1 or 2. Alternatively, a 0Ω resistor in the R51 position fulfills the same requirement. The JP61 jumper connects the SA pin of the part to the AGND pin.

APPLICATIONS INFORMATION

This would be used for operating Mode 3. Here, a 0Ω resistor in the R61 position also works. Jumpers JP52 and JP62 perform the same functions on the B side of the part.

The buffering amplifier can be configured for inverting or noninverting operation. For inverting applications, connect jumper JP2 positions 1 and 2. Additionally, connect jumper JP4 for split supply applications or JP8 for a single supply. For a noninverting application, connect jumper JP2 positions 2 and 3.

Several other jumpers should be connected as follows:

JP1: Install a jumper wire from position 1 to position 2, leave the other positions open.

JP5: Install a jumper wire if split supply, leave open if single supply.

JP6: Leave open.

JP7: Install a jumper wire.

JP9: Install a jumper wire if single supply, leave open if split supply.

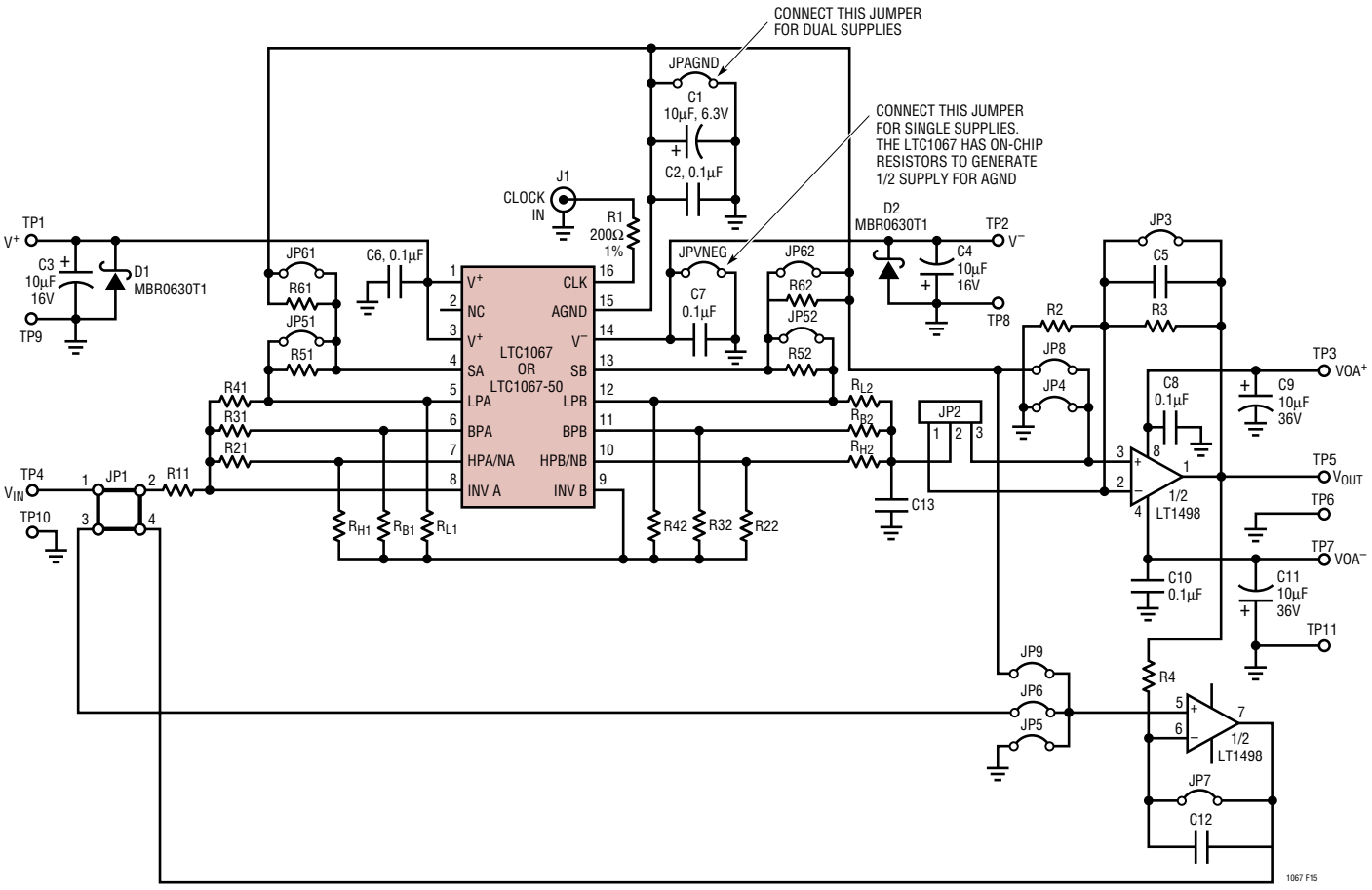


Figure 15. Schematic for the LTC1067/LTC1067-50 Demo Board

APPLICATIONS INFORMATION

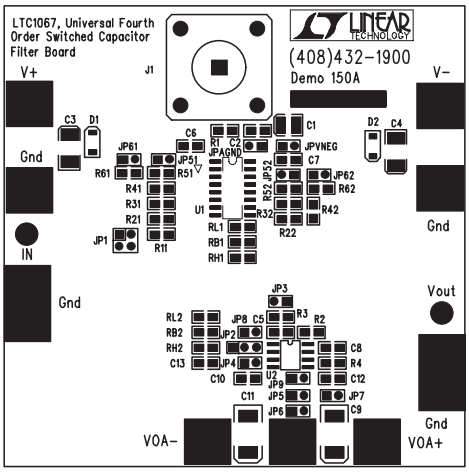
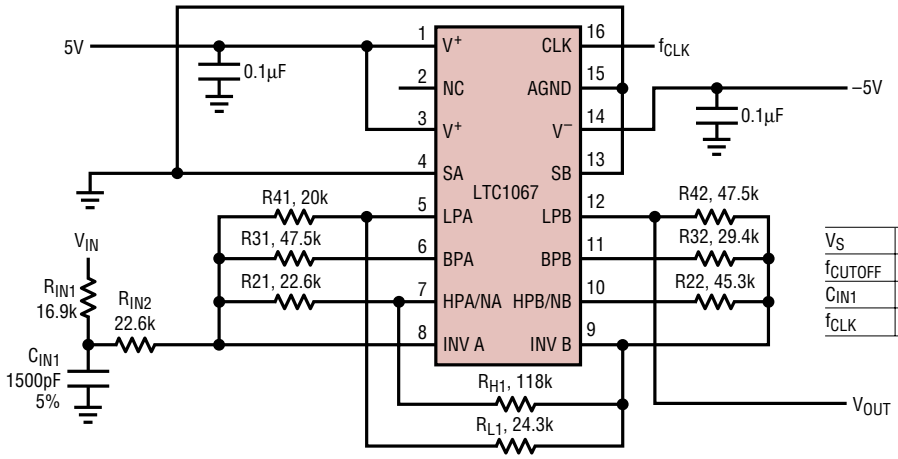


Figure 16. Silkscreen for the LTC1067/LTC1067-50 Demo Board

TYPICAL APPLICATIONS

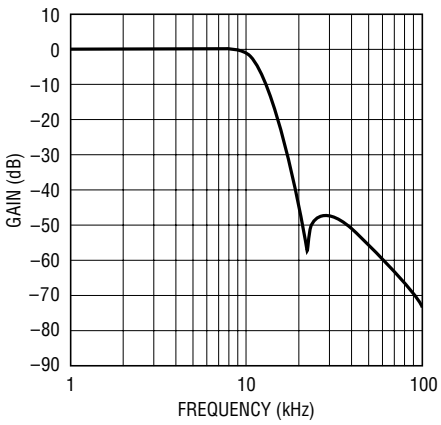
5th Order Lowpass with Input RC (Fixed Frequency)



V_S	±5V		5V	3V
f_{CUTOFF}	20k	15k	10k	5k
C_{IN1}	750pF	1000pF	1500pF	3000pF
f_{CLK}	2MHz	1.5MHz	1MHz	500kHz

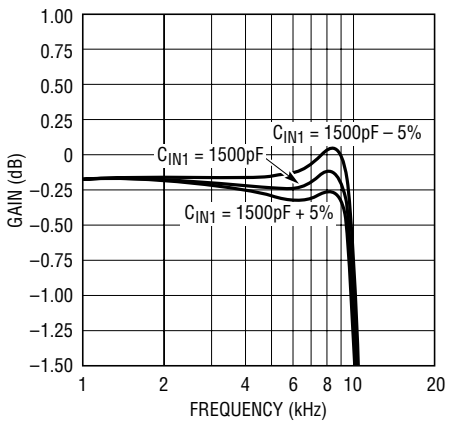
1067 TA05a

Frequency Response (f_{CUTOFF} = 10kHz)



1067 TA05b

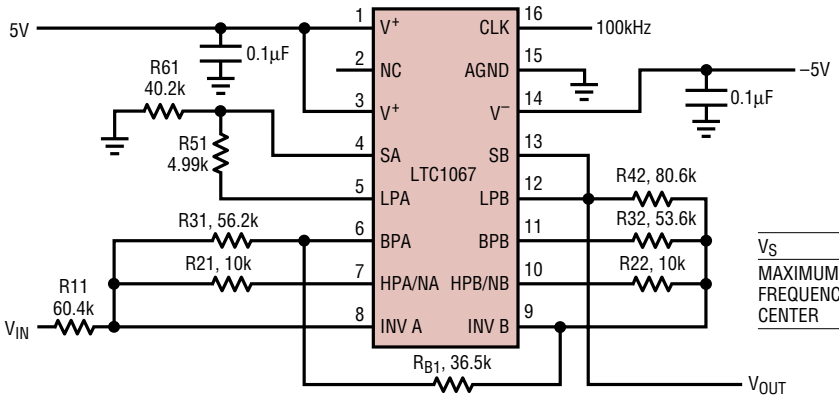
Passband Gain Variation Due to C_{IN}



1067 TA05c

TYPICAL APPLICATIONS

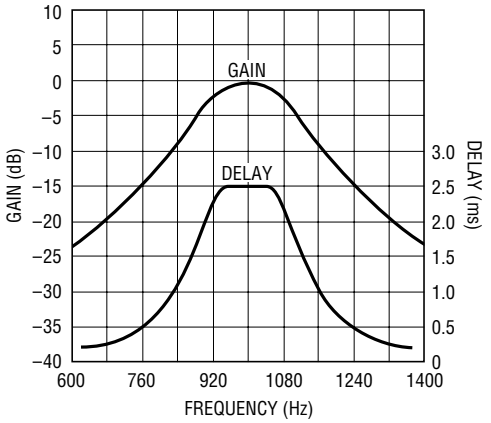
1kHz Linear Phase Bandpass Filter



V_S	±5V	5V (OR ±2.5V)	3V (OR ±1.5V)
MAXIMUM FREQUENCY CENTER	5kHz	2.5kHz	2.2kHz

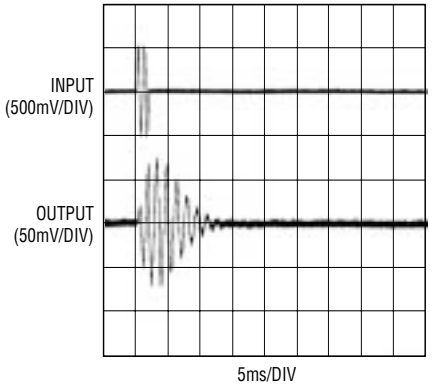
1067 TA06a

Gain and Group Delay vs Frequency



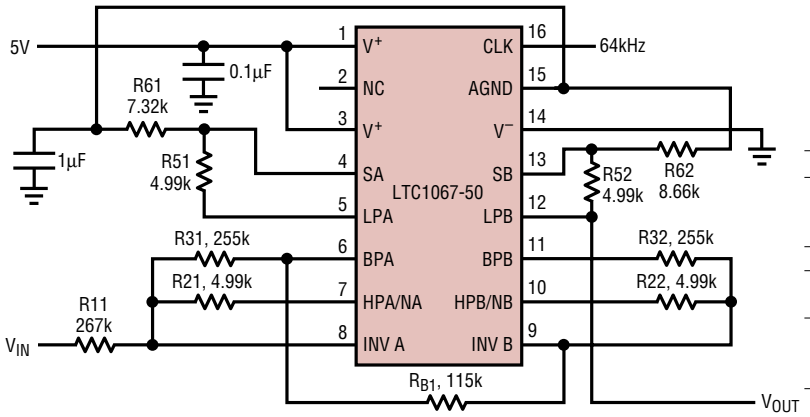
1067 TA06b

Sine Burst Response



1067 TA06c

Single Supply, 4th Order Bandpass Filter
$f_{CENTER} = f_{CLK}/64$, –3dB BW = $f_{CENTER}/20$



V_S	MAXIMUM f_{CENTER}
SINGLE 5V	12kHz
SINGLE 3.3V	7.5kHz
SINGLE 3V	5.5kHz

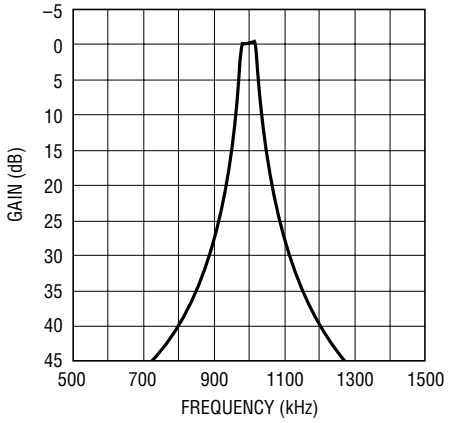
V_S	NOISE (FILTER INPUT AT $V^+/2$)
SINGLE 5V	426µV_{RMS}
SINGLE 3.3V	333µV_{RMS}
SINGLE 3V	290µV_{RMS}

1067 TA07a

TYPICAL APPLICATIONS

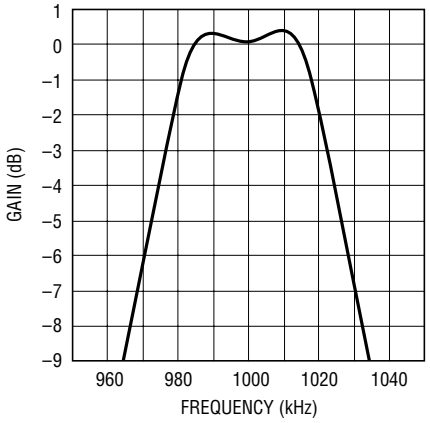
Single Supply, 4th Order Bandpass Filter
V_S = 5V, f_{CLK} = 64kHz

Gain vs Frequency



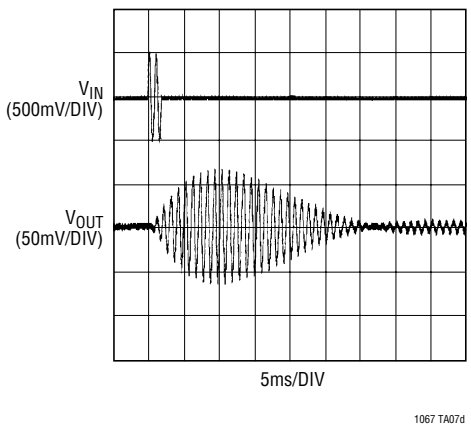
1067 TA07b

Gain vs Frequency



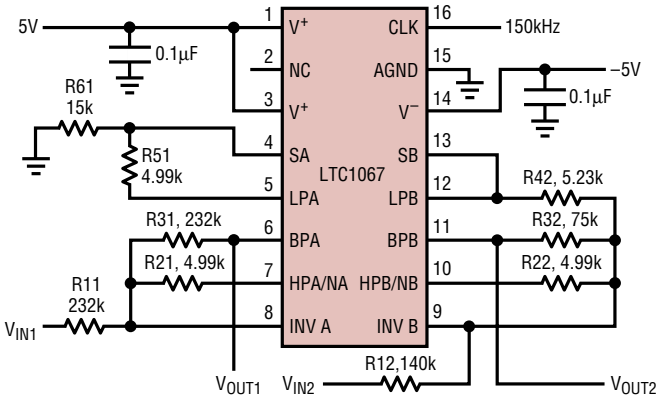
1067 TA07b

Sine Burst Response



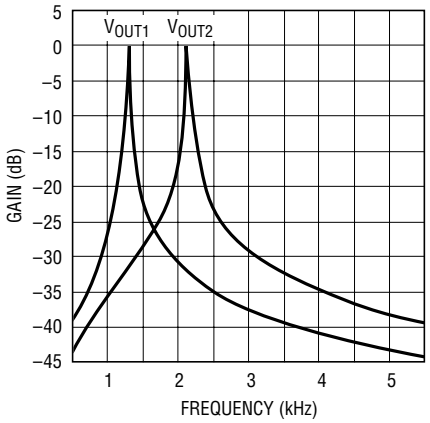
1067 TA07d

LTC1067 Dual Bandpass Filters
V_S = ±5V, f_{CLK} = 150kHz ($f_{CENTER1}$ =1.3kHz, $f_{CENTER2}$ = 2.1kHz)



1067 TA08a

Frequency Response

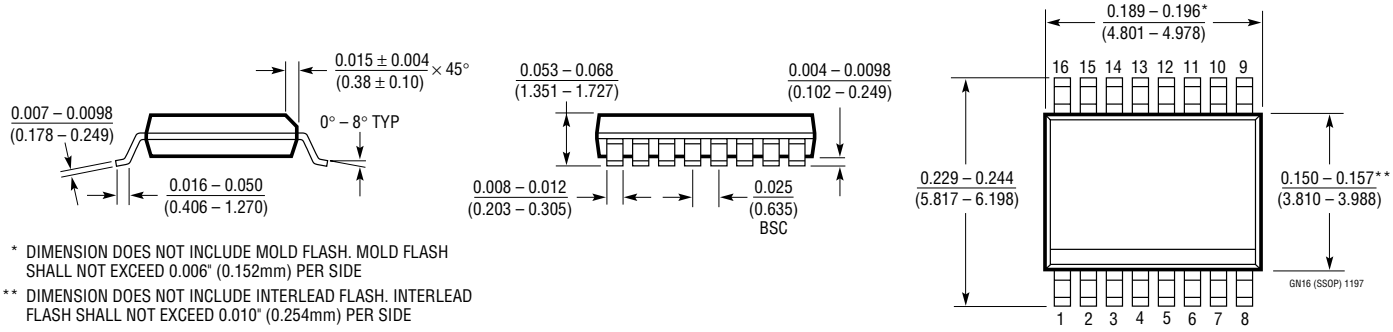


1067 TA08b

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

GN Package
16-Lead Plastic SSOP (Narrow 0.150)
(LTC DWG # 05-08-1641)



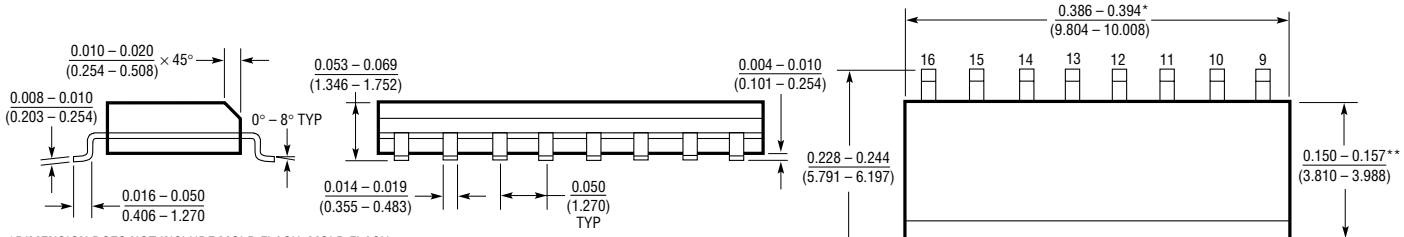
* DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

S Package
16-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)

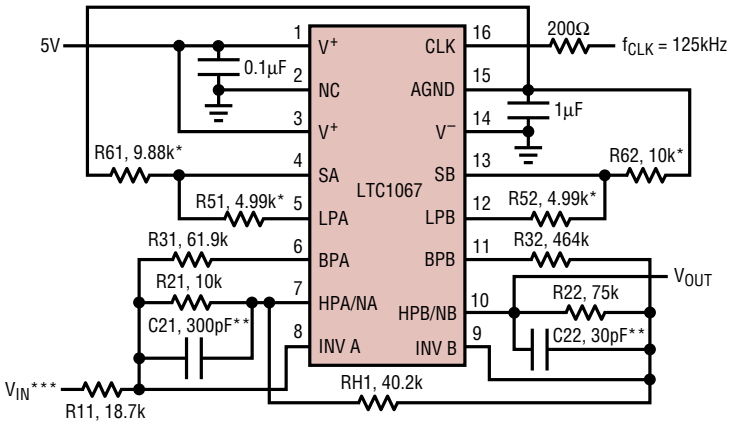


*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

TYPICAL APPLICATION

1.02kHz Notch Filter for Telecom System



* R51, R61, R52, R62 ARE 0.1% TOLERANCE RESISTORS

** C21 AND C22 IMPROVE THE NOTCH DEPTH WHERE

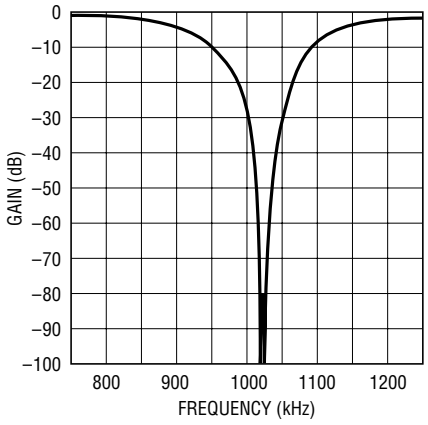
$$(30)(f_{NOTCH}) < \frac{1}{2\pi(R2x)(C2X)} < (75)(f_{NOTCH})$$

WITHOUT C21 AND C22 THE NOTCH DEPTH IS LIMITED TO –35dB

*** $V_{IN} \leq 1.25V_{P-P}$

1067 TA03

Frequency Response



1067 TA04

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1068-25	High Speed Quad Universal Building Block Filter	25:1 Clock-to-f_0 Ratio
LTC1068-50	Low Power Quad Universal Building Block Filter	50:1 Clock-to-f_0 Ratio
LTC1068-200	Low Noise, Oversampled Quad Universal Building Block Filter	200:1 Clock-to-f_0 Ratio
LTC1068	Quad Universal Building Block Filter	100:1 Clock-to-f_0 Ratio
LTC1562	Quad, Universal, Continuous Time Building Block	10kHz < f_C < 150kHz

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