BANG-BANG Controller

FEATURES

- Micropower 1.5µW (1 Sample/Second)
- Wide Supply Range 2.8V to 16V
- High Accuracy
  - *Guaranteed* SET POINT Error ±0.5mV Max
  - *Guaranteed* Deadband ±0.1% of Value Max
- Wide Input Voltage Range V⁺ to Ground
- TTL Outputs with 5V Supply
- Two *Independent* Ground-Referred Control Inputs
- Small Size 8-Pin SO

APPLICATIONS

- Temperature Control (Thermostats)
- Motor Speed Control
- Battery Charger
- Any ON-OFF Control Loop

DESCRIPTION

The LTC®1041 is a monolithic CMOS BANG-BANG controller manufactured using Linear Technology's enhanced LTCMOS™ silicon gate process. BANG-BANG loops are characterized by turning the control element fully ON or fully OFF to regulate the average value of the parameter to be controlled. The SET POINT input determines the average control value and the DELTA input sets the deadband. The deadband is always 2 x DELTA and is centered around the SET POINT. Independent control of the SET POINT and deadband, with no interaction, is made possible by the unique sampling input structure of the LTC1041.

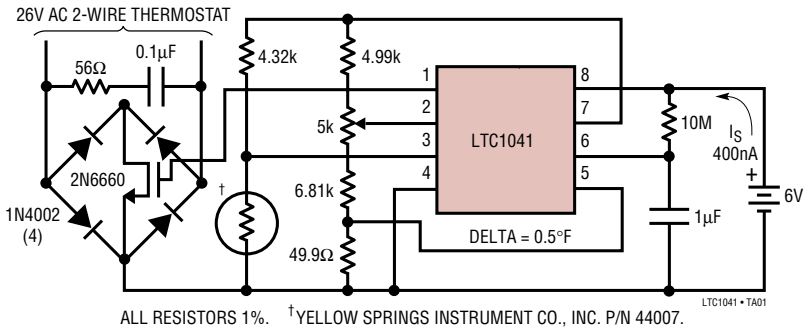
An external RC connected to the OSC pin sets the sampling rate. At the start of each sample, internal power to the analog section is switched on for ≈ 80µs. During this time, the analog inputs are sampled and compared. After the comparison is complete, power is switched off. This achieves extremely low average power consumption at low sampling rates. CMOS logic holds the output continuously while consuming virtually no power.

To keep system power at an absolute minimum, a switched power output (V_{P-P}) is provided. External loads, such as bridge networks and resistive dividers, can be driven by this switched output.

The output logic sense (i.e., ON = V⁺) can be reversed (i.e., ON = GND) by interchanging the V_{IN} and SET POINT inputs. This has no other effect on the operation of the LTC1041.

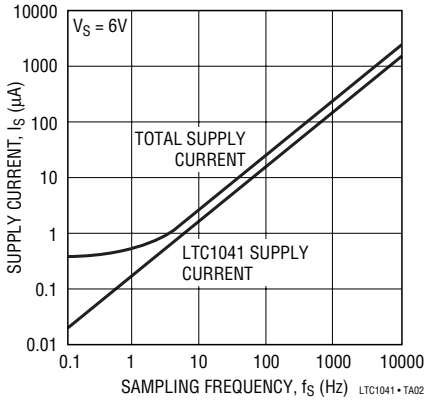
TYPICAL APPLICATION

Ultralow Power 50°F to 100°F (2.4µW) Thermostat



ALL RESISTORS 1%. †YELLOW SPRINGS INSTRUMENT CO., INC. P/N 44007.
DRIVING THERMISTOR WITH V_{P-P} ELIMINATES 3.8°F ERROR DUE TO SELF-HEATING

Supply Current vs Sampling Frequency

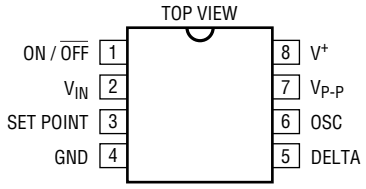


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 18V
Input Voltage ..... (V^+ + 0.3V) to (V^- – 0.3V)
Operating Temperature Range
LTC1041C ..... –40°C to 85°C
LTC1041M **(OBSOLETE)** ..... –55°C to125°C
Storage Temperature Range ..... –55°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C
Output Short Circuit Duration ..... Continuous

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PDIP

T_{JMAX} = 110°C, θ_{JA} = 150°C/W (N8)
T_{JMAX} = 150°C, θ_{JA} = 150°C/W (S8)

J8 PACKAGE
8-LEAD CERDIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W

OBSOLETE PACKAGE
Consider the N8 Package as an Alternate Source

ORDER PART NUMBER
LTC1041CN8 LTC1041CS8
LTC1041MJ8

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. Test Conditions: V^+ = 5V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		TC1041M/LTC1041C MIN	TYP	MAX	UNITS
	SET POINT Error (Note 3)	V^+ = 2.8V to 6V (Note 2)	●		±0.3 + ±0.05	±0.5 + ±0.1	mV % of DELTA
		V^+ = 6V to 15V (Note 2)	●		±1 + ±0.05	±3 + ±0.1	mV % of DELTA
	Deadband Error (Note 4)	V^+ = 2.8V to 6V (Note 2)	●		±0.6 + ±0.1	±1 + ±0.2	mV % of DELTA
		V^+ = 6V to 15V (Note 2)	●		±2 + ±0.1	±6 + ±0.2	 % of DELTA
I_{OS}	Input Current	V^+ = 5V, T_A = 25°C, OSC = GND (V_{IN}, SET POINT and DELTA Inputs)			±0.3		nA
R_{IN}	Equivalent Input Resistance	f_S = 1kHz (Note 5)	●	10	15		MΩ
	Input Voltage Range		●	GND		V^+	V
P_{SR}	Power Supply Range		●	2.8		16	V
$I_{S(ON)}$	Power Supply ON Current (Note 6)	V^+ = 5V, V_{P-P} ON	●		1.2	3	mA
$I_{S(OFF)}$	Power Supply OFF Current (Note 6)	V^+ = 5V, V_{P-P} OFF LTC1041C LTC1041M	● ●		0.001 0.001	0.5 5	µA µA
t_D	Response Time (Note 7)	V^+ = 5V		60	80	100	µs
V_{OH} V_{OL}	ON/$\overline{OFF}$ Output (Note 8) Logical "1" Output Voltage Logical "0" Output Voltage	 V^+ = 4.75V, I_{OUT} = –360µA V^+ = 4.75V, I_{OUT} = 1.6mA	 ●	 2.4	 4.4 0.25	 0.4	 V V
R_{EXT}	External Timing Resistor	Resistor Connected between V^+ and OSC Pin	●	100		10,000	kΩ
f_S	Sampling Frequency	V^+ = 5V, T_A = 25°C, R_{EXT} = 1M C_{EXT} = 0.1µF			5		Hz

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: Applies over input voltage range limit and includes gain uncertainty.

ELECTRICAL CHARACTERISTICS

Note 3: SET POINT error $\equiv \left(\frac{V_U + V_L}{2}\right)$ – SET POINT

where V_U = upper band limit and V_L = lower band limit.

Note 4: Deadband error $\equiv (V_U - V_L) - 2 \bullet$ DELTA where V_U = upper band limit and V_L = lower band limit.

Note 5: R_{IN} is guaranteed by design and is not tested.
$R_{IN} = 1/(f_S \times 66pF)$.

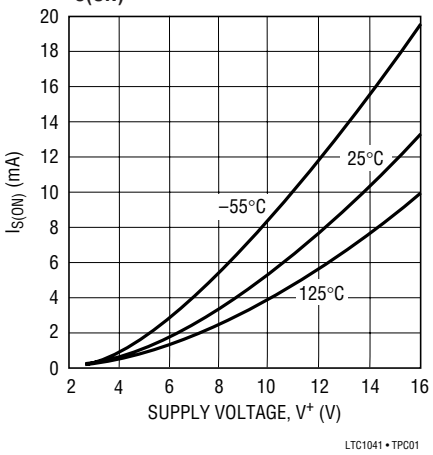
Note 6: Average supply current = $t_D \bullet I_{S(ON)} \bullet f_S + (1 - t_D \bullet f_S)\, I_{S(OFF)}$.

Note 7: Response time is set by an internal oscillator and is independent of overdrive voltage. $t_D = V_{P-P}$ pulse width.

Note 8: Output also capable of meeting EIA/JEDEC standard B series CMOS drive specifications.

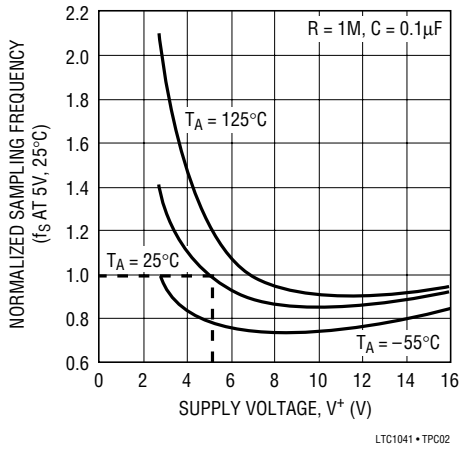
TYPICAL PERFORMANCE CHARACTERISTICS

$I_{S(ON)}$ vs V^+



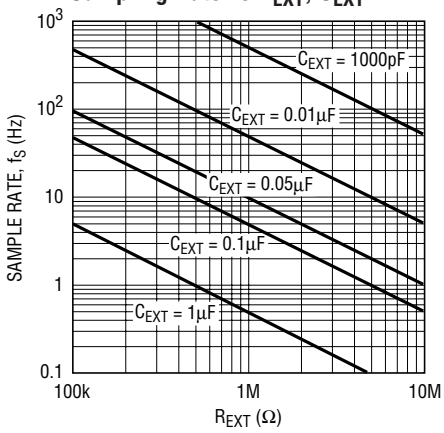
LTC1041 • TPC01

Normalized Sampling Frequency vs V^+, Temperature



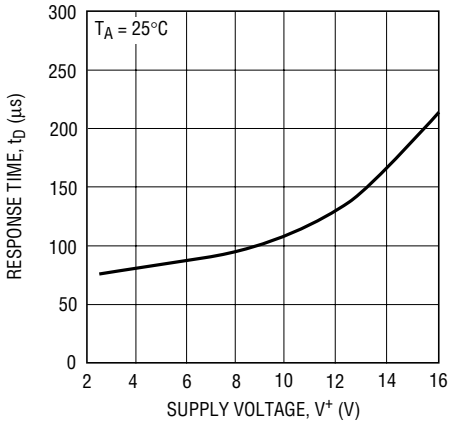
LTC1041 • TPC02

Sampling Rate vs R_{EXT}, C_{EXT}



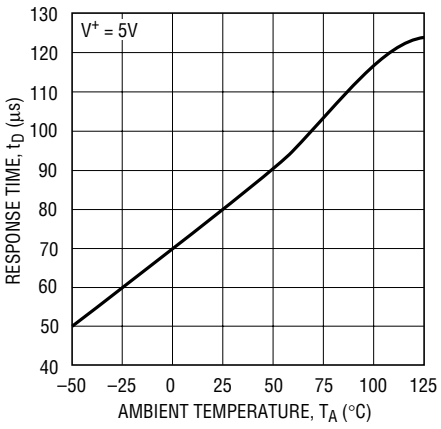
LTC1041 • TPC03

Response Time vs Supply Voltage



LTC1041 • TPC04

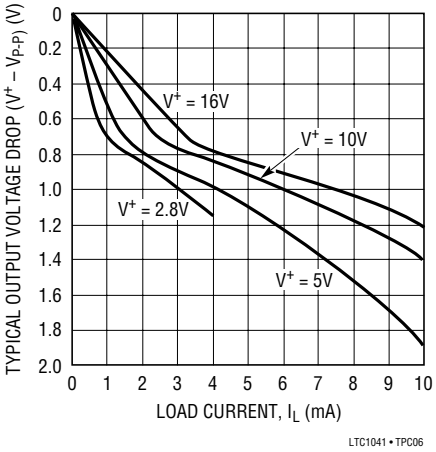
Response Time vs Temperature



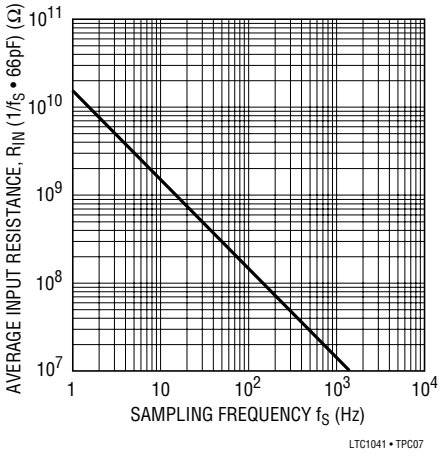
LTC1041 • TPC05

TYPICAL PERFORMANCE CHARACTERISTICS

V_{P-P} Output Voltage vs Load Current



R_{IN} vs Sampling Frequency

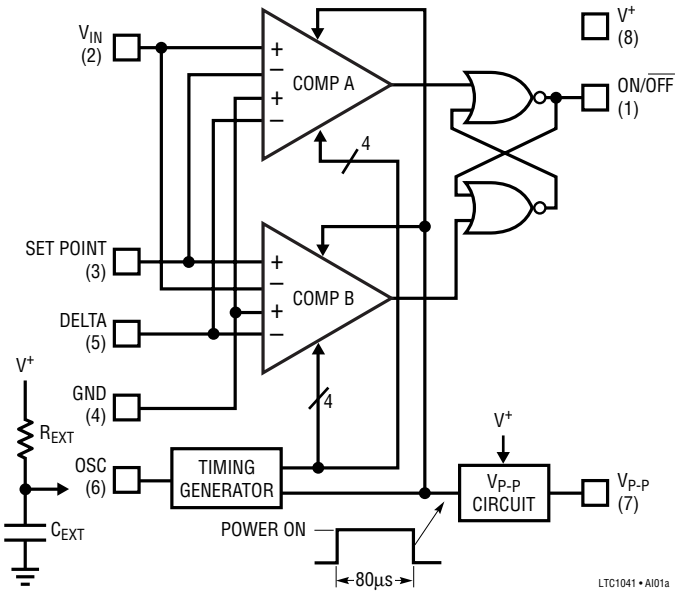


APPLICATIONS INFORMATION

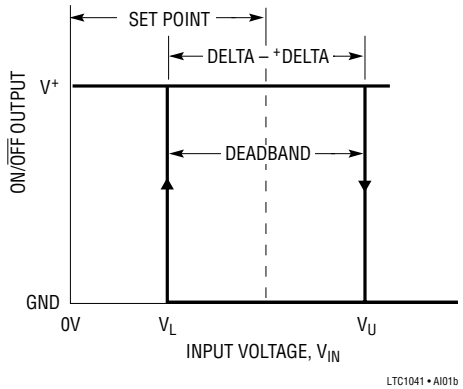
The LTC1041 uses sampled data techniques to achieve its unique characteristics. It consists of two comparators, each of which has two differential inputs (Figure 1a). When the sum of the voltages on a comparator's inputs is positive, the output is high and when the sum is negative, the output is low. The inputs are interconnected such that the R_S flip-flop is reset (ON/$\overline{OFF}$ = GND) when V_{IN} > (SET POINT + DELTA) and is set (ON/$\overline{OFF}$ = V^+) when V_{IN} < (SET POINT – DELTA). This makes a very precise hysteresis loop of 2 • DELTA centered around the SET POINT. (See Figure 1b.)

For R_S < 10kΩ

The dual differential input structure is made with CMOS switches and a precision capacitor array. Input impedance characteristics of the LTC1041 can be determined from the equivalent circuit shown in Figure 2. The input capacitance will charge with a time constant of



(a)



(b)

Figure 1. LTC1041 Block Diagram

APPLICATIONS INFORMATION

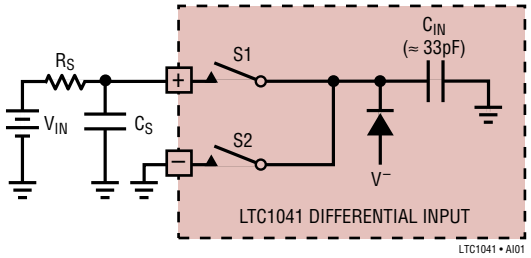


Figure 2. Equivalent Input Circuit

$R_S \bullet C_{IN}$. The ability to fully charge C_{IN} from the signal source during the controller's active time is critical in determining errors caused by the input charging current. For source resistances less than 10kΩ, C_{IN} fully charges and no error is caused by the charging current.

For R_S > 10kΩ

For source resistances greater than 10kΩ, C_{IN} cannot fully charge, causing voltage errors. To minimize these errors, an input bypass capacitor, C_S, should be used. Charge is shared between C_{IN} and C_S, causing a small voltage error. The magnitude of this error is $A_V = V_{IN} \bullet C_{IN} (C_{IN} + C_S)$. This error can be made arbitrarily small by increasing C_S.

The averaging effect of the bypass capacitor, C_S, causes another error term. Each time the input switches cycle between the plus and minus inputs, C_{IN} is charged and discharged. The average input current due to this is $I_{AVG} = V_{IN} \bullet C_{IN} \bullet f_S$, where f_S is the sampling frequency. Because the input current is directly proportional to the differential input voltage, the LTC1041 can be said to have an average input resistance of $R_{IN} = V_{IN}/I_{AVG} = I/(f_S \bullet C_{IN})$.

Since two comparator inputs are connected in parallel, R_{IN} is one half of this value (see typical curve of R_{IN} versus Sampling Frequency). This finite input resistance causes an error due to the voltage divider between R_S and R_{IN}.

The input voltage error caused by both of these effects is $V_{ERROR} = V_{IN} [2C_{IN}/(2C_{IN} + C_S) + R_S/(R_S + R_{IN})]$.

Example: assume f_S = 10Hz, R_S = 1M, C_S = 1µF, V_{IN} = 1V, V_{ERROR} = 1V(66µV + 660µV) = 726µV. Notice that most of the error is caused by R_{IN}. If the sampling frequency is reduced to 1Hz, the voltage error from the input impedance effects is reduced to 136µV.

Input Voltage Range

The input switches of the LTC1041 are capable of switching either to the V^+ supply or ground. Consequently, the input voltage range includes both supply rails. This is a further benefit of the sampling input structure.

Error Specifications

The only measurable errors on the LTC1041 are the deviations from "ideal" of the upper and lower switching levels (Figure 1b). From a control standpoint, the error in the SET POINT and deadband is critical. These errors may be defined in terms of V_U and V_L.

$$\text{SET POINT error} \equiv \left(\frac{V_U + V_L}{2}\right) - \text{SET POINT}$$

$$\text{deadband error} \equiv (V_U - V_L) - 2 \bullet \text{DELTA}$$

The specified error limits (see electrical characteristics) include error due to offset, power supply variation, gain, time and temperature.

Pulsed Power (V_{P-P}) Output

It is often desirable to use the LTC1041 with resistive networks such as bridges and voltage dividers. The power consumed by these resistive networks can far exceed that of the LTC1041 itself.

At low sample rates the LTC1041 spends most of its time off. A switched power output, V_{P-P}, is provided to drive the input network, reducing its average power as well. V_{P-P} is switched to V^+ during the controller's active time (≈ 80µs) and to a high impedance (open circuit) when internal power is switched off.

Figure 3 shows the V_{P-P} output circuit. The V_{P-P} output voltage is not precisely controlled when driving a load (see typical curve of V_{P-P} Output Voltage vs Load Current). In spite of this, high precision can be achieved in two ways: (1) driving ratiometric networks and (2) driving fast settling references.

In ratiometric networks all the inputs are proportional to V_{P-P} (Figure 4). Consequently, the absolute value of V_{P-P} does not affect accuracy.

APPLICATIONS INFORMATION

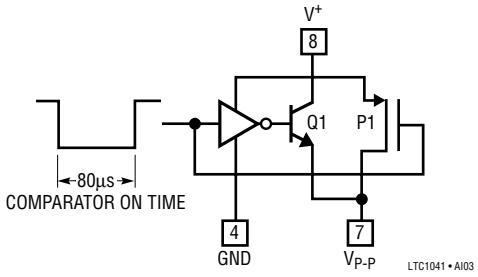


Figure 3. V_{P-P} Output Switch

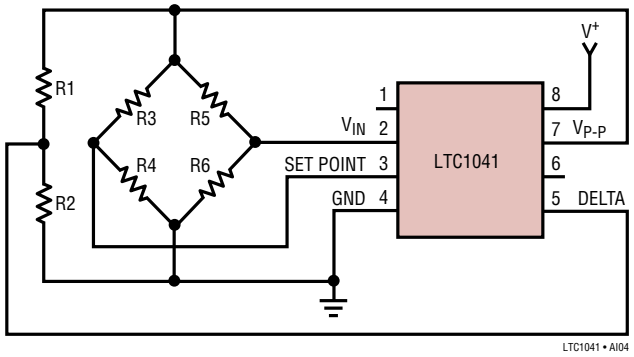


Figure 4. Ratiometric Network Driven by V_{P-P}

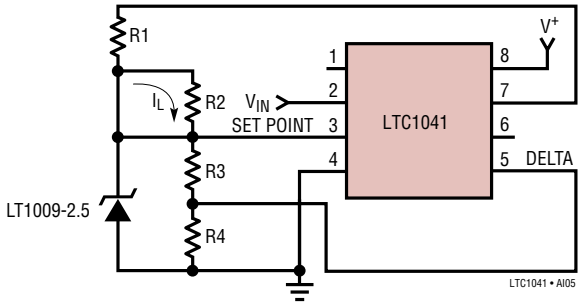


Figure 5. Driving Reference with V_{P-P} Output

If the best possible performance is needed, the inputs to the LTC1041 must completely settle within 4µs of the start of the comparison cycle (V_{P-P} high impedance to V^+ transition). Also, it is critical that the input voltages do not change during the 80µs active time. When driving resistive input networks with V_{P-P}, capacitive loading should be minimized to meet the 4µs settling time requirement. Further, care should be exercised in layout when driving networks with source impedances, as seen by the LTC1041, of greater than 10kΩ (see For R_S > 10kΩ).

In applications where an absolute reference is required, the V_{P-P} output can be used to drive a fast settling reference. The LTC1009 2.5V reference settles in ≈ 2µs and is ideal for this application (Figure 5). The current through R1 must be large enough to supply the LT1009 minimum bias current (≈ 1mA) and the load current, I_L.

Internal Oscillator

An internal oscillator allows the LTC1041 to strobe itself. The frequency of the oscillation, and hence the sampling rate, is set with an external RC network (see typical curve, Sampling Rate R_{EXT}, C_{EXT}). R_{EXT} and C_{EXT} are connected as shown in Figure 1. To assure oscillation, R_{EXT} must be between 100kΩ and 10MΩ. There is no limit to the size of C_{EXT}.

At low sampling rates, R_{EXT} is very important in determining the power consumption. R_{EXT} consumes power continuously. The average voltage at the OSC pin is approximately $V^+/2$, giving a power dissipation of $P_{REXT} = (V^+/2)^2/R_{EXT}$.

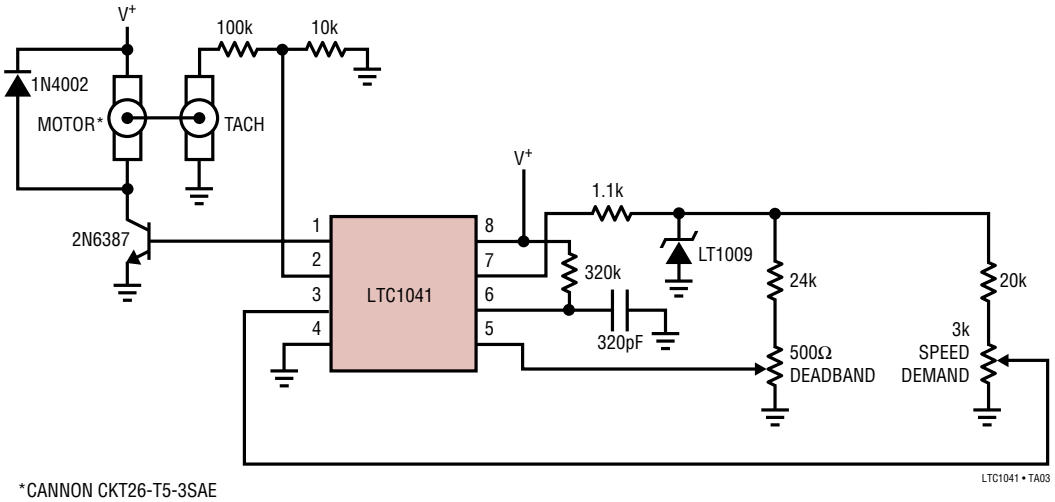
Example: assume R_{EXT} = 1MΩ, V^+ = 5V, $P_{REXT} = (2.5)^2/10^6 = 6.25/\mu W$. This is approximately four times the power consumed by the LTC1041 at V^+ = 5V and f_S = 1 sample/second. Where power is a premium, R_{EXT} should be made as large as possible. Note that the power dissipated by R_{EXT} is *not* a function of f_S or C_{EXT}.

If high sampling rates are needed and power consumption is of secondary importance, a convenient way to get the maximum possible sampling rate is to make R_{EXT} = 100kΩ and C_{EXT} = 0. The sampling rate, set by the controller's active time, will nominally be ≈ 10kHz.

To synchronize the Sampling of the LTC1041 to an external frequency source, the OSC pin can be driven by a CMOS gate. A CMOS gate is necessary because the input trip points of the oscillator are close to the supply rails and TTL does not have enough output swing. Externally driven, there will be a delay from the rising edge of the OSC input and the start of the sampling cycle of approximately 5µs.

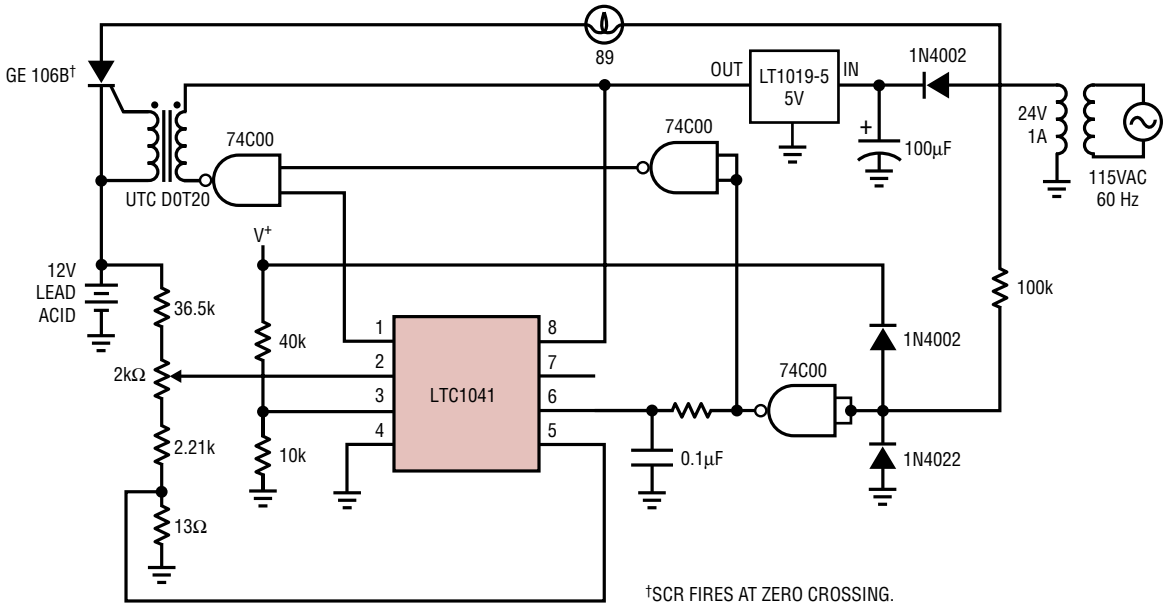
TYPICAL APPLICATIONS

Motor Speed Controller



*CANNON CKT26-T5-3SAE

Battery Charger

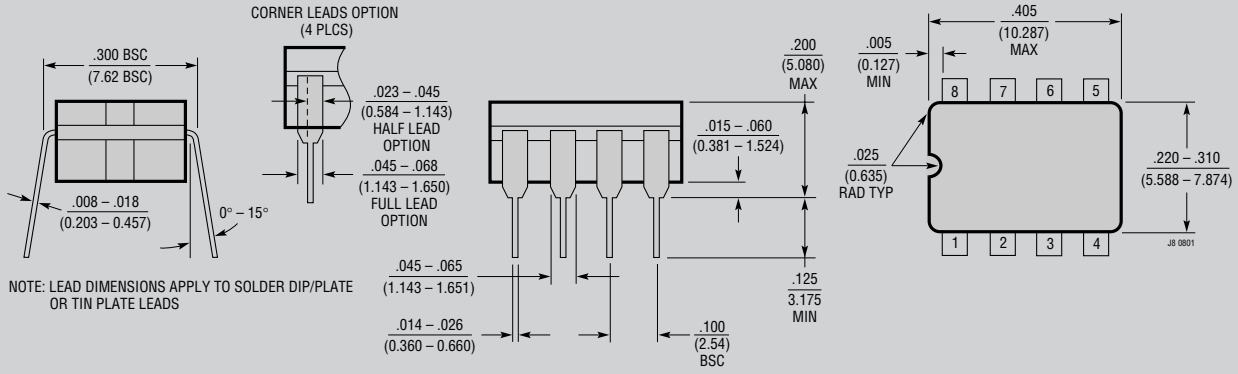


†SCR FIRES AT ZERO CROSSING.
*SET BATTERY VOLTAGE. BATTERY IS MEASURED WITH ZERO CHARGE CURRENT

LTC1041 • TA04

PACKAGE DESCRIPTION

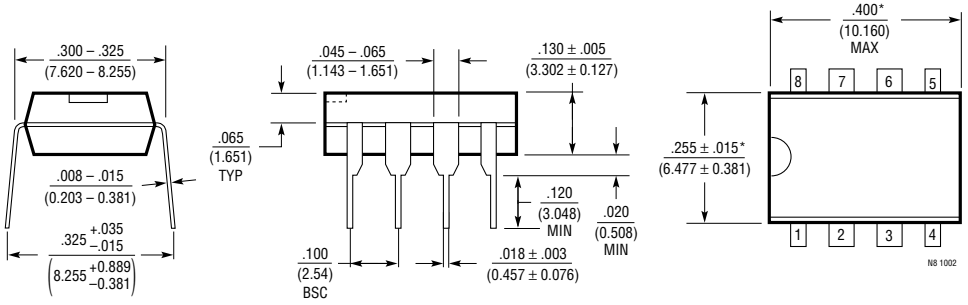
J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGE

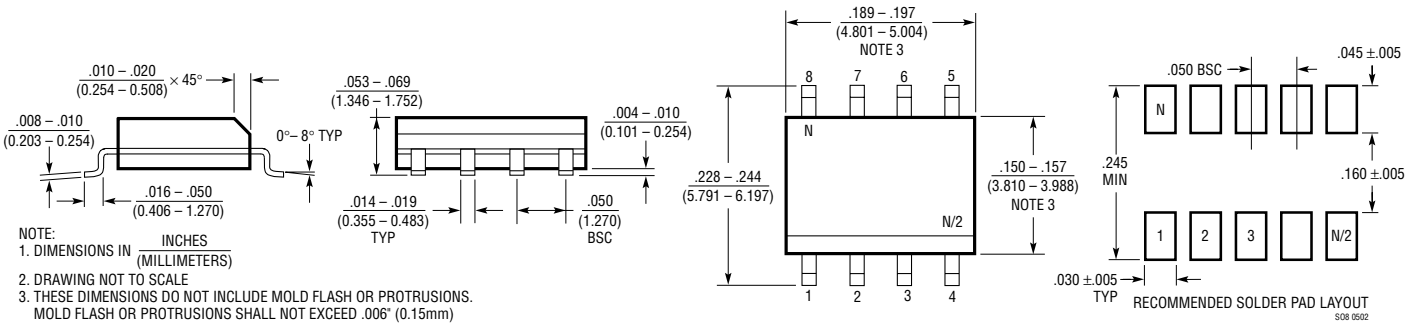
N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610)



NOTE:
1. DIMENSIONS IN INCHES / (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)

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