Precision Signal Conditioning AFE for Pressure Sensor Applications

MAX40109

General Description

The MAX40109 is a low-power, precision sensor interface SoC that includes a high-precision, programmable Analog frontend (AFE), Analog-to-Digital Converter (ADC), calibration memory, and digital signal processing. It also includes a Digital-to-Analog Converter (DAC) with an output buffer to support analog voltage output and a 4mA–20mA current loop. It is designed for sensor applications such as strain gauges, pressure, force, and temperature.

This Sensor AFE has both analog and digital outputs. The digital 1-Wire/I^2C interfaces program the calibration memory, the front-end Programmable gain amplifier (PGA)'s gain, and the internal current source that drives the sensors' bridge. The digital I^2C interface can also be used to retrieve the digital output data and generate alarms.

The MAX40109 operates from 3V to 36V, is available in the thin quad flat no-lead (TQFN) package and wafer level package (WLP). It is specified over the -40°C to +125°C operating temperature range.

Applications

- Pressure Sensors
- Strain Gauges
- Force Sensors
- Temperature Sensors
- Wheatstone-Bridge

Benefits and Features

- Analog Front-End to Interface with Resistive Bridge-Based Pressure Sensors
- Temperature Measurement either directly from the Resistive Bridge or from an External Thermistor
- Analog Zero-Pressure Offset Compensation
- High-Precision PGA Front-End with 20 Gain Options
- Analog and Digital Outputs
- Digital 1-Wire, Power Line Communication (PLC) and I^2C interfaces
- Calibration Memory with Third-Order Polynomial for Compensation from Temperature and Non-Linearity
- Internal Electromagnetic Interference (EMI) Rejection
- Supply Voltage Range: 3V to 36V
- Low 2mA (typ) Supply Current
- Available in TQFN and WLP Packages

Ordering Information appears at end of data sheet.

19-101790; Rev 3; 4/25

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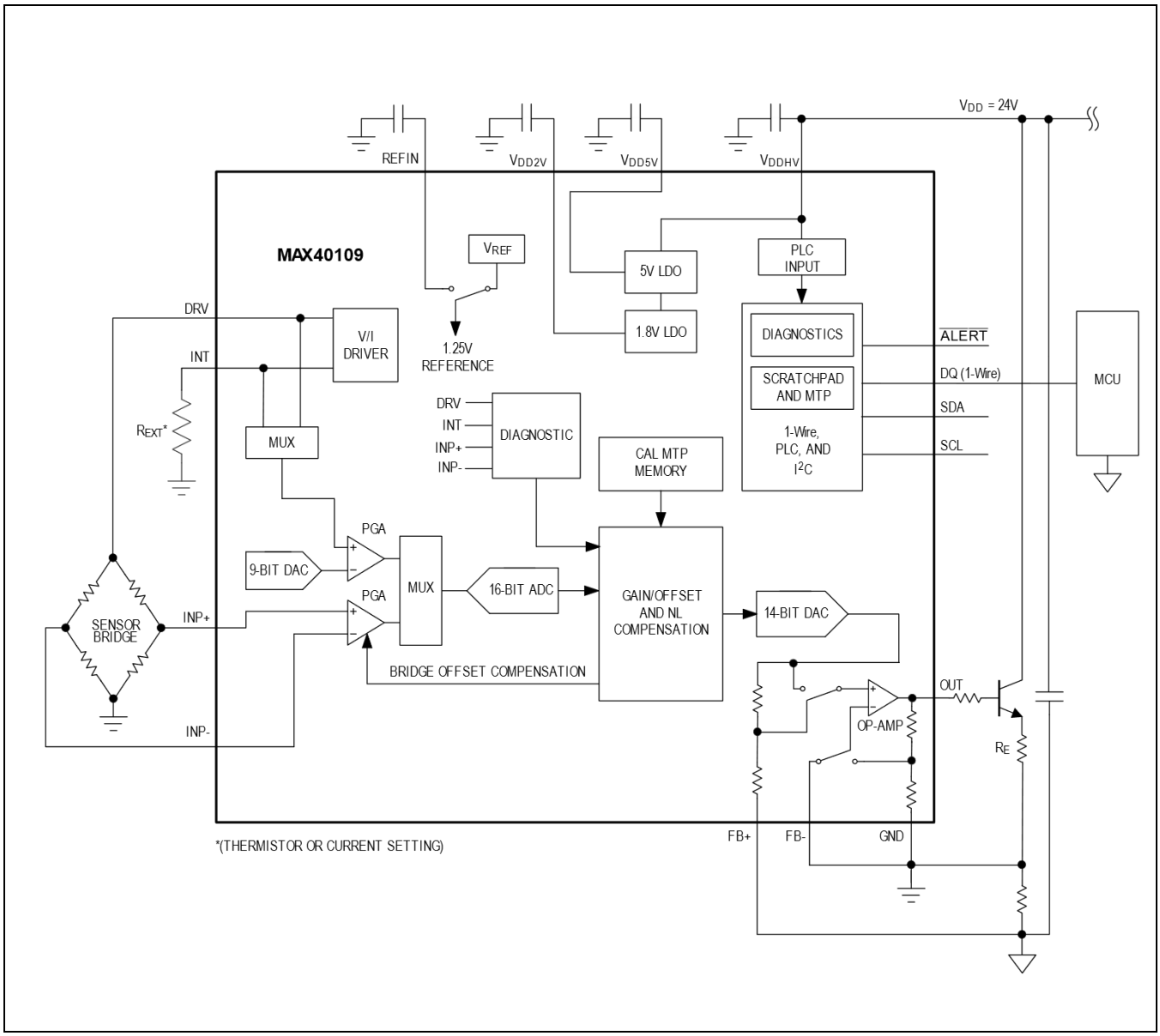
Simplified Block Diagram



Absolute Maximum Ratings

V_{DDHV} to GND ..... -40V to +40V

OUT to GND ..... -40V to +40V

Pin Voltage Differential (Voltage between any of these two pins: V_{DD}, OUT, GND) ..... -40V to +40V

V_{DD5V}, DRV, FB-, INP+, INP-, INT, SCL, SDA, $\overline{ALERT}$ to GND ..... -0.3V to +6V

V_{DD2V}, REFIN to GND ..... -0.3V to +2V

FB+ to GND ..... -1.5V to +5V

DQ to GND ..... -1.5V to +6V

Continuous current into any input/output pin 10mA Continuous Power Dissipation TQFN (Single Layer Board) (T_A = +70°C, derate 20.8 mW/°C above +70°C.) 1666.70mW

Continuous Power Dissipation TQFN (Four-Layer Board) (Derate 30.3 mW/°C above +70°C.) 2,424.20mW

Operating Temperature Range ..... -40°C to 125°C

Junction Temperature ..... +150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

TQFN	
Package Code	T2044-5C
Outline Number	*21-0139*
Land Pattern Number	*90-0429*
Thermal Resistance, Single Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four Layer Board:	
Junction to Ambient (θ_{JA})	33°C/W
Junction to Case (θ_{JC})	2°C/W

WLP	
Package Code	W162Q2+1
Outline Number	*21-100604*
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four Layer Board:	
Junction to Ambient (θ_{JA})	49.13°C/W
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html.* Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html.*

Electrical Characteristics

(Global conditions unless otherwise stated. V_{DDHV} = 5V, V_{DRV} = 4V, V_{IN}+ = V_{IN}- = V_{DRV}/2, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40°C ≤ T_A ≤ +125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
System Level Performance: Noise-Free Effective Resolution		V_{DRV} = 4V, 10kΩ bridge, V_{INP}+ –V_{INP}- = 4mV (DC), G = 252V/V, Noise BW 3dB = 1kHz, G_{OUT} = 4V/V			12.4		bits
		I_{DRV} = 500µA, 3.5kΩ bridge, V_{INP}+ – V_{INP}- = 75mV (DC), G = 15V/V, Noise BW 3dB = 1kHz, G_{OUT} = 1V/V			12.8		
INPUT PGA							
Input Offset Voltage	V_{OS}	G = 15V/V Zero-pressure offset compensation disabled	0.6V < V_{CM} < 1.7V		180	850	µV
			1.7V < V_{CM} < 2.8V		440	2000	
		G = 144V/V Zero-pressure offset compensation disabled	0.6V < V_{CM} < 2.8V		76	450	
Input Offset Drift	TCV_{OS}	V_{CM} > 1.7V			0.062	1.6	µV/°C
		V_{CM} < 1.7V			0.018	0.8	
Input Bias Current	I_B	T_A = +25°C			60	400	pA
		-40°C ≤ T_A ≤ +125°C				3860	
Input Offset Current	I_{OS}				9.2	400	pA
Input Common Mode Range	V_{CM}	Zero-pressure offset compensation disabled	V_{DDHV} ≥ 4.4V	0.6		2.8	
			3.8V ≤ V_{DDHV} ≤ 4.4V	0.6		2.6	
			V_{DDHV} ≤ 3.8V	0.6		V_{VDDHV} -1.2	
		Zero-pressure offset compensation enabled		0.37 x V_{DRV}		0.63 x V_{DRV}	V
Range of Gain	G	Programmable through 1-wire and/or I²C	Internal ADC Input Full-Scale Range is 1.25V		5, 10, 15, 20, 24, 40, 60, 72, 90, 108, 126, 144, 160, 180, 200, 252, 540, 1080, 1440, 2520		V/V
Gain Selection Settling Time					10		ms

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PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Error	GE	G = 15V/V			0.15	0.9	%
		G = 144V/V			0.45	1.4	
Gain Error Temperature Coefficient	TC_{GE}	G = 15V/V			4		ppm/ºC
		G = 144V/V			9		
INPUT PGA/AC SPECIFICATIONS							
Signal Bandwidth	BW_{3dB}	G = 15V/V			55		kHz
		G = 144V/V			24.5		
Input Voltage-Noise	V_N	0.1Hz ≤ f ≤ 1kHz, G = 15V/V	Zero-pressure offset compensation disabled		2.5		μV_{RMS}
			Zero-pressure offset compensation enabled (at 30mV/V)		2.7		
		0.1Hz ≤ f ≤ 10Hz, G = 144V/V	Zero-pressure offset compensation disabled		0.23		
			Zero-pressure offset compensation enabled (at 80mV/V)		0.78		
EMI Rejection Ratio	EMIRR	V_{RFpeak} = 100mVp, f = 400MHz, 900MHz, 1800MHz, 2400MHz, both IN+ and IN-			80		dB
INPUT PGA/ZERO-PRESSURE OFFSET COMPENSATION							
Resolution		Including sign	Corresponds to 44µV/V		12		bits
Offset Range				80	93		mV/V
TEMPERATURE MEASUREMENT							
Current Source Range		Sourced at INT pin V_{INT} = 0V to 1.6V			150, 250, 500, 750		uA
Input Common Mode Range	V_{CM}	Guaranteed by CMRR parameter		0.25		1.6	V
Common Mode Rejection Rate	CMRR	V_{CM} = 0.25V to 1.6V			95		dB
Range of Gain	G	Programmable through 1-wire and/or I^2C	G = 1, 1.5, and 2 are for single-ended only. G = 3 is for differential only		1.5, 2, 3, 5, 6, 10, 15, 20, 24, 30, 36, 40, 45, 60, 72, 90		V/V
Input Offset Voltage	V_{OS}				50	2,000	µV
Gain Error	GE	Gain = 10V/V			±0.4	±2.5	%

(Global conditions unless otherwise stated. V_{DDHV} = 5V, V_{DRV} = 4V, $V_{IN}+ = V_{IN}- = V_{DRV}/2$, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40°C ≤ T_A ≤ +125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain-Bandwidth Product	GBW				200		kHz
Input Voltage-Noise Density	V_N	f = 1kHz			180		nV/√Hz
BRIDGE DIAGNOSTICS							
Diagnostic Voltage Threshold Resolution		Applies to all: OV_INP+, OV_INP-, UV_INP+, UV_INP-, OV_DRV, UV_DRV, OV_INT, UV_INT			8		bits
Diagnostic Voltage Threshold Accuracy		Applies to all: OV_INP+, OV_INP-, UV_INP+, UV_INP-, OV_DRV, UV_DRV, OV_INT, UV_INT	From 0% to 90% of V_{DD5V}		±3		LSB
		Applies to all: OV_INP+, OV_INP-, UV_INP+, UV_INP, OV_DRV, UV_DRV, OV_INT, UV_INT	Above 90% of V_{DD5V}		-3 ±2		
ANALOG-TO-DIGITAL CONVERTER							
Sample Frequency					1, 2, 4, 8, 16		ksps
SENSOR BRIDGE VOLTAGE SOURCE							
Voltage Source Range	V_{DRV}	Programmable through Digital Interfaces	I_{DRV} = 0mA to 2mA		1.8, 2.3, 3.3, 4.0		V
Voltage Source Range Accuracy	ΔV_{DRV}	I_{DRV} = 0mA to 2mA				3.5	%
SENSOR BRIDGE CURRENT SOURCE							
Current Source Range	I_{DRV}	Programmable through 1-wire and/or I^2C	V_{DRV} = 4V		250, 300, 400, 450, 500, 550, 650, 750		µA
Current Source Range Accuracy	ΔI_{DRV}	V_{DRV} = 0V to 4V				5	%

(Global conditions unless otherwise stated. V_{DDHV} = 5V, V_{DRV} = 4V, V_{IN}+ = V_{IN}- = V_{DRV}/2, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40°C ≤ T_A ≤ +125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Range at Bridge Top	V_{DRV}	V_{DDHV} ≥ 4.65V	Zero-pressure compensation offset enabled Guaranteed by Input Referred Residual Voltage	1.8		4.2	V
		3V ≤ V_{DDHV} ≤ 4.65V	Zero-pressure compensation offset enabled Guaranteed by Input Referred Residual Voltage	1.8		3 x ln (V_{DDHV}) -0.41	
Input Referred Residual Voltage	V_{RES}	Applies over "Voltage Range at Bridge Top" specification. Zero-pressure compensation offset = FS/4 Input PGA Gain = 15				±3	mV
INTERNAL/EXTERNAL REFERENCE							
Reference Voltage	V_{REF}				1.25		V
Internal Reference Voltage Temp-Co	V_{REFTC}				15		ppm/ºC
OUTPUT AMPLIFIER AND DIGITAL TO ANALOG CONVERTER							
Gain	G_{OUT}	Current (4mA–20mA) Output	DAC Full-Scale 1.25V		1		V/V
		Voltage Output, 5V	DAC Full-Scale 1.25V, V_{DDHV} = 5.5V		4		
		Voltage Output, 3V	DAC Full-Scale 0.5V, V_{DDHV} = 3.3V		6		
Output Voltage High	V_{OH}	V_{DD5V} - V_{OUT}	R_L= 10KΩ to GND		94	160	mV
Output Voltage Low	V_{OL}	V_{OUT} - GND	R_L = 10KΩ to GND		3	15	mV
Slew Rate	SR				0.12		V/µs
Capacitive Loading Stability	C_{LOAD}	A_V = 4V/V			500		pF
POWER SUPPLY							
Supply Voltage	V_{DDHV}	Guaranteed by PSRR, -40°C < T_A < +125°C		3		36	V
Internal Digital Supply Voltage	V_{DD2V}			1.7	1.8	1.9	V
Internal Analog Supply Voltage	V_{DD5V}	V_{DDHV} ≥ 6V		5.05	5.28	5.5	V
Internal Analog Supply LDO Dropout	V_{DDHV} – V_{DD5V}	V_{DDHV} = 5V			121	201	mV
	V_{DDHV} – V_{DD5V}	V_{DDHV} = 3V			121	199	
Power Supply Rejection Ratio	PSRR	6 ≤ V_{DDHV}≤ 36V			105		dB

(Global conditions unless otherwise stated. V_{DDHV} = 5V, V_{DRV} = 4V, V_{IN}+ = V_{IN}- = V_{DRV}/2, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40°C ≤ T_A ≤ +125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Current	I_{DD}				2	2.57	mA
Power-Up Time	t_{ON}	V_{DDHV} = 0V to 5V	Communication ready		2		ms
			ADC Calibration completed – Ready for Measurements		140		
Low-Power Mode Supply Current	I_{SHDN}	-40ºC ≤ T_A ≤ +125ºC				250	µA
Turn-On Time	t_{ONSD}	From Low-Power Mode (through I^2C)			50		µs
I^2C LOGIC DC CHARACTERISTICS							
Input High Voltage	V_{IH}			0.7 x V_{DD5V}			V
Input Low Voltage	V_{IL}					0.3 x V_{DD5V}	V
Input High Leakage Current	I_{IH}	Logic Input to V_{DD5V}		-1	±0.005	+1	µA
Input Low Leakage Current	I_{IL}	Logic Input to 0V		-1	±0.005	+1	µA
Input Capacitance	C_{IN}				5		pF
Output Low Voltage	V_{OL}	I_{OL} = 3mA		0		0.3	V
Output High Leakage Current		V_{OUT} = V_{DD5V}			±0.005	1	µA
I^2C TIMING							
Serial Clock Frequency	f_{SCL}			50		1M	Hz
Bus Free Time Between Start and Stop Conditions	t_{BUF}			0.5			µs
START Condition Hold Time	$t_{HD:STA}$			0.26			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SCL to 10% of SDA		0.26			µs
Clock Low Period	t_{LOW}			0.5			µs
Clock High Period	t_{HIGH}			0.26			µs
START Condition Setup Time	$t_{SU:STA}$	90% of SCL to 90% of SDA		0.26			µs
Data Setup Time	$t_{SU:DAT}$	10% of SDA to 10% of SCL		50			ns
Data In Hold Time	$t_{HD:DAT}$	10% of SCL to 10% of SDA		0			µs
SCL/SDA Rise Time	t_R					120	ns
SCL/SDA Fall Time	t_F			20		120	ns
Transmit SDA Fall Time	t_F	Bus capacitance = 550pF. V_{DD} ≥ 2.4V		20 x (V_{DD} /5.5V)		120	ns
SCL Time Low for Reset of Serial Interface	$t_{TIMEOUT}$			20		45	ms
Maximum Pulse Width of Spikes That Must Be Suppressed by the Input Filter					50		ns

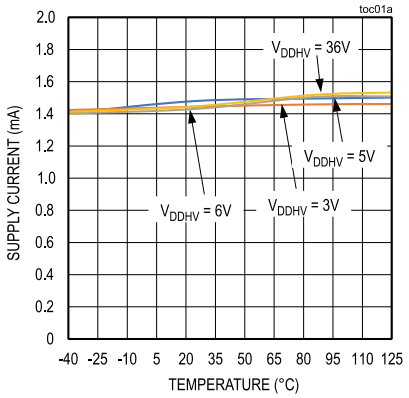
(Global conditions unless otherwise stated. V_{DDHV} = 5V, V_{DRV} = 4V, $V_{IN}+ = V_{IN}- = V_{DRV}/2$, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40°C ≤ T_A ≤ +125°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Capacitive Load for Each Bus Line	C_B				550		pF
1-Wire LOGIC DC CHARACTERISTICS (DQ)							
Input Voltage Level High	V_{IH}	DQ only	V_{DDHV} = 3V to 5.5V	0.8 x V_{DD5V}			V
Input Voltage Level Low	V_{IL}	DQ only	V_{DDHV} = 3V to 5.5V			0.2 x V_{DD5V}	V
Output Voltage Level High	V_{OH}	DQ only	V_{DDHV} = 3V to 5.5V	0.75 x V_{DD5V}		4	V
Output Voltage Level Low	V_{OL}	DQ only	V_{DDHV} = 3V to 5.5V, I_{SINK} = 500µA			200	mV
PLC LOGIC DC CHARACTERISTICS (INPUT V_{DDHV}, OUTPUT OUT)							
Input Voltage Level High	V_{IN_HIGH}			31			V
Input Voltage Level Low	V_{IN_LOW}					24	V
Output Voltage Level High	V_{OH}	Analog OUT only	DAC output ≥ 0x3665 (85% of full-scale)	0.82 x FS			V
Output Voltage Level Low	V_{OL}	Analog OUT only	DAC output ≤ 0x0999 (15% of full-scale)	0		0.18 x FS	V
1-Wire TIMING ON DQ							
Time Slot	t_{SLOT}			60		120	µs
Recovery Time	t_{REC}			1			µs
Write-Zero Low Time	t_{LOW0}			60		120	µs
Write-One Low Time	t_{LOW1}			1		15	µs
Read Data Valid	t_{RDV}					20	µs
Reset Time High	t_{RSTH}			480			µs
Reset Time Low	t_{RSTL}			480			µs
Presence-Detect High	t_{PDHIGH}			15		60	µs
Presence-Detect Low	t_{PDLOW}			60		240	µs
DQ (Data) Capacitance	$C_{IN/OUT}$				25		pF
PLC TIMING WITH V_{DDHV} AS INPUT AND OUT AS OUTPUT							
Time Slot	t_{SLOT}			480		960	µs
Recovery Time	t_{REC}			8			µs
Write-Zero Low Time	t_{LOW0}			480		960	µs
Write-One Low Time	t_{LOW1}			100		120	µs
Read Data Valid	t_{RDV}					120	µs
Reset Time High	t_{RSTH}			3.84			ms
Reset Time Low	t_{RSTL}			3.84			ms
Presence-Detect High	t_{PDHIGH}			120		480	µs
Presence-Detect Low	t_{PDLOW}			480		1920	µs

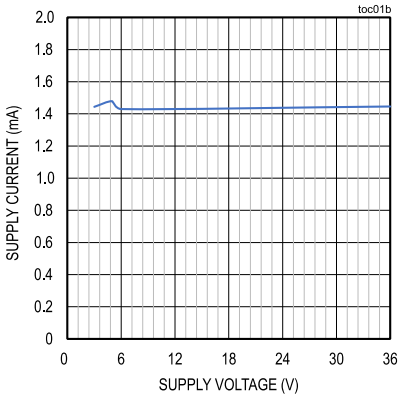
Typical Operating Characteristics

V_{DDHV} = 5V, V_{DRV} = 4V, V_{IN}+ = V_{IN}- = V_{DRV}/2, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40ºC ≤ T_A ≤ +125ºC.

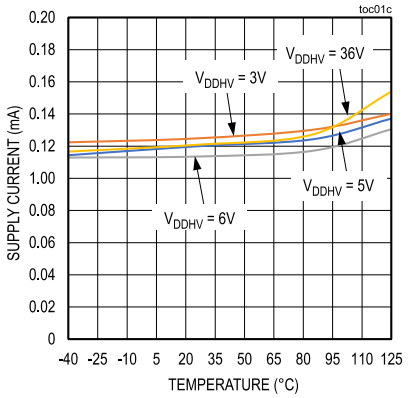
SUPPLY CURRENT vs. TEMPERATURE



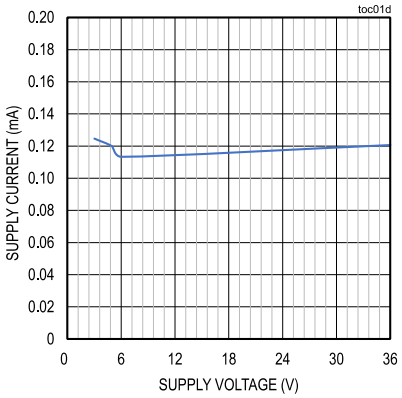
SUPPLY CURRENT vs. SUPPLY VOLTAGE



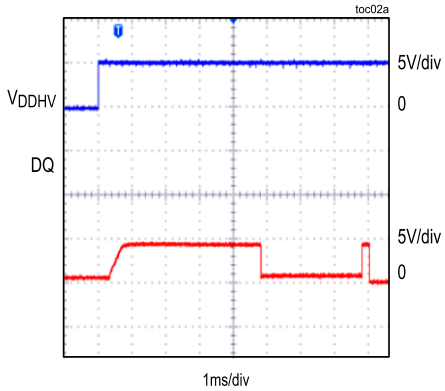
SHUTDOWN CURRENT vs. TEMPERATURE



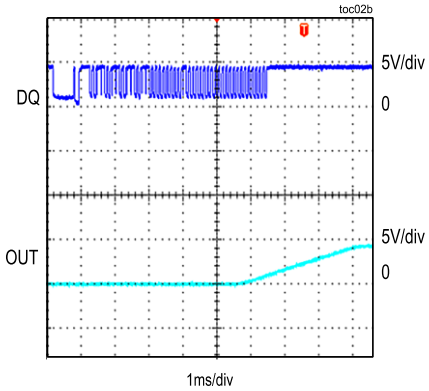
SUPPLY CURRENT vs. SUPPLY VOLTAGE



POWER-UP RESPONSE



TURN-ON TIME FROM SHUTDOWN



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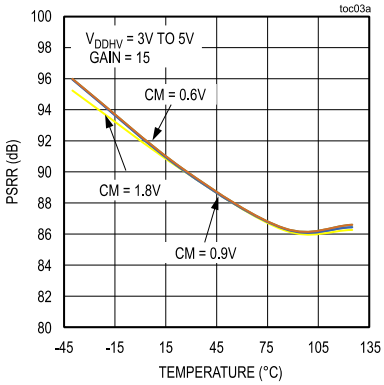
POWER SUPPLY REJECTION RATIO vs. TEMPERATURE



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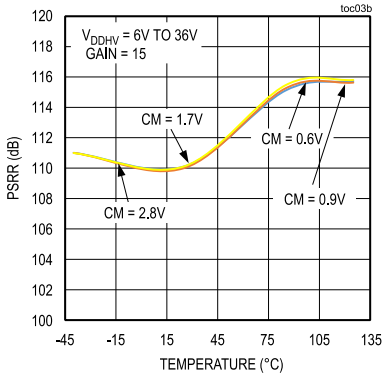
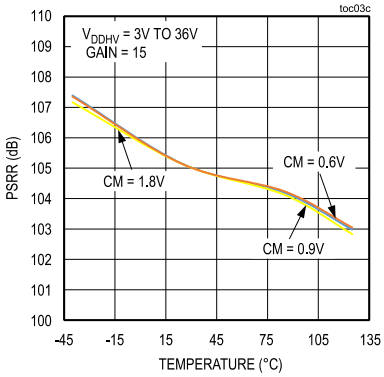
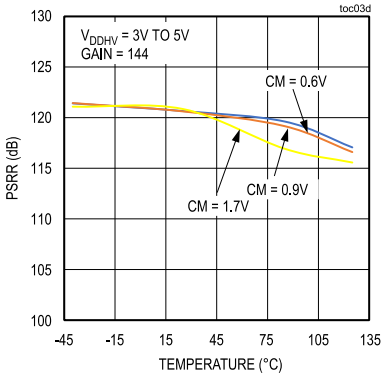


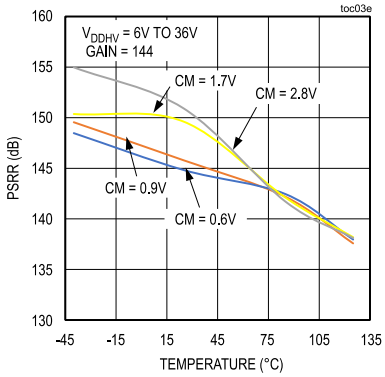
POWER SUPPLY REJECTION RATIO vs. TEMPERATURE



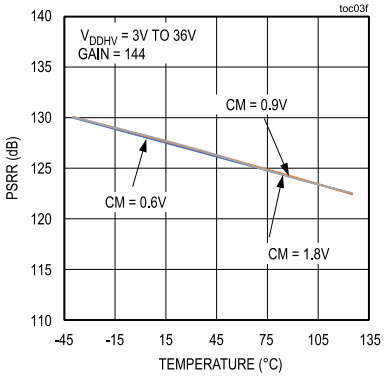
POWER SUPPLY REJECTION RATIO vs. TEMPERATURE



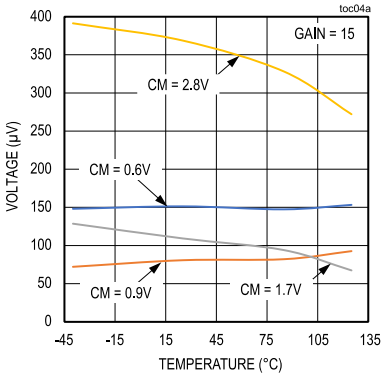
POWER SUPPLY REJECTION RATIO vs. TEMPERATURE



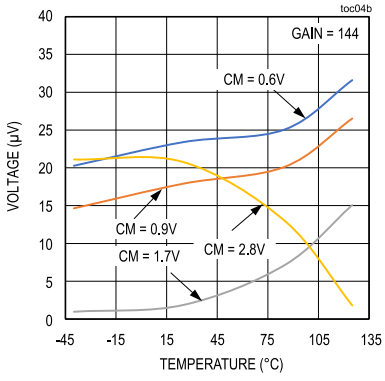
POWER SUPPLY REJECTION RATIO vs. TEMPERATURE



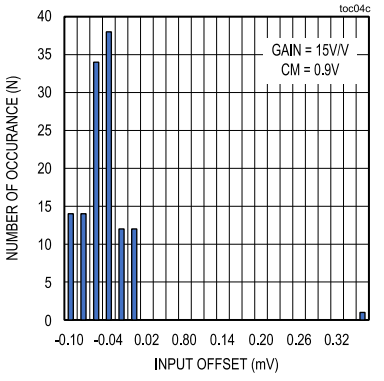
INPUT OFFSET VOLTAGE vs. TEMPERATURE



INPUT OFFSET VOLTAGE vs. TEMPERATURE

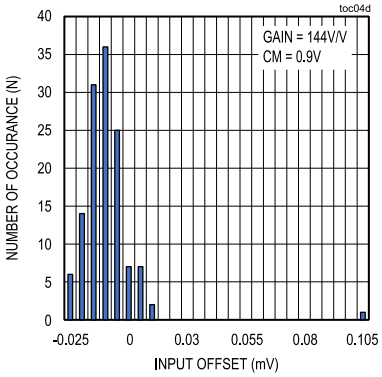


INPUT OFFSET HISTOGRAM

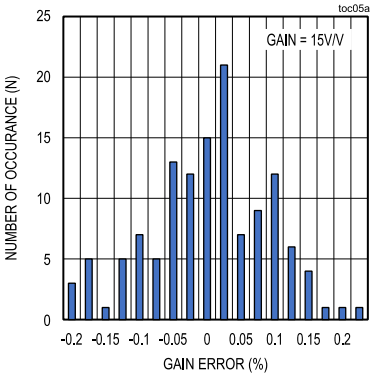


V_{DDHV} = 5V, V_{DRV} = 4V, V_{IN}+ = V_{IN}- = V_{DRV}/2, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40ºC ≤ T_A ≤ +125ºC.

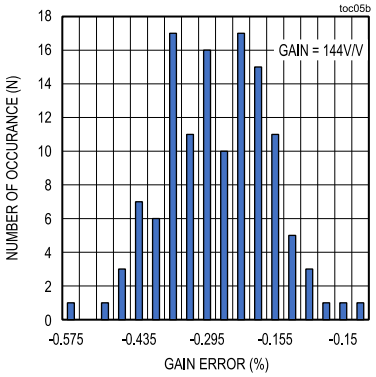
INPUT OFFSET HISTOGRAM



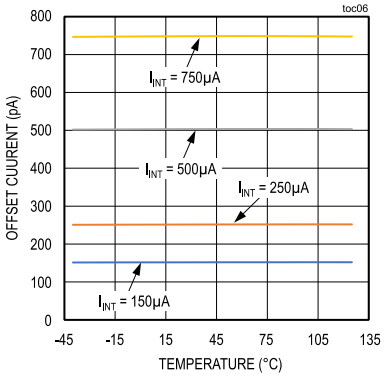
GAIN ERROR HISTOGRAM



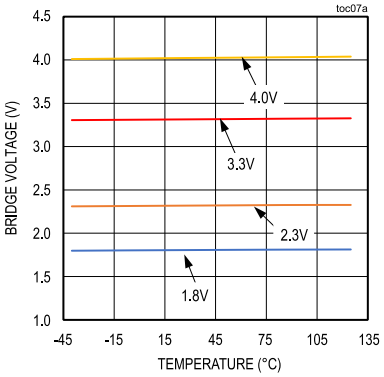
GAIN ERROR HISTOGRAM



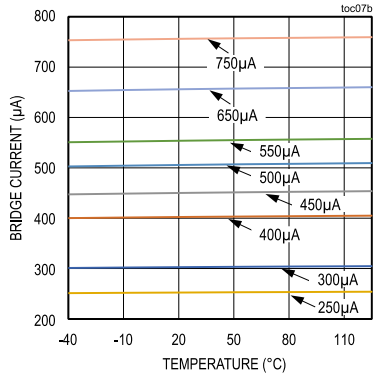
INT CURRENT vs. TEMPERATURE



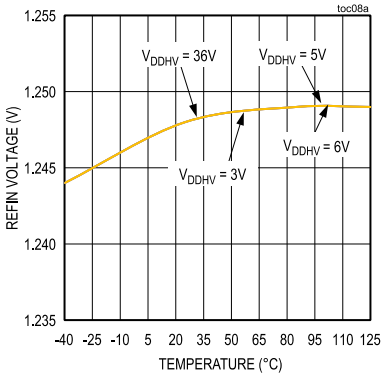
SENSOR BRIDGE VOLTAGE SOURCE vs. TEMPERATURE



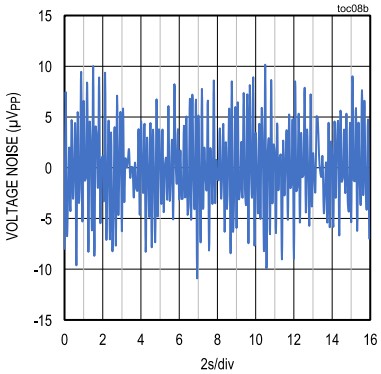
SENSOR BRIDGE CURRENT SOURCE vs. TEMPERATURE



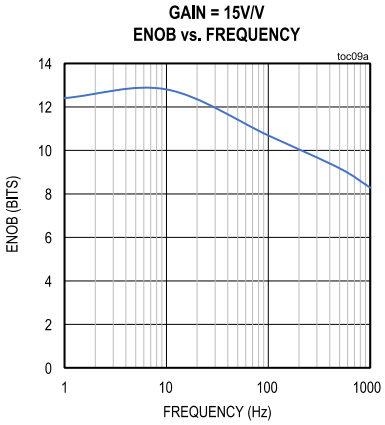
REFIN vs. TEMPERATURE

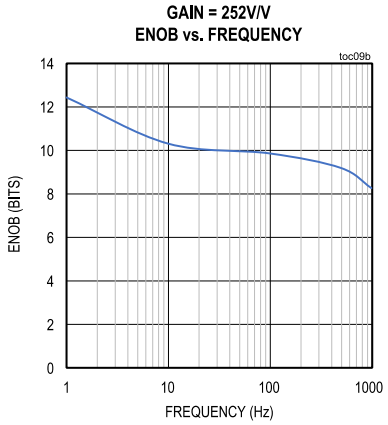


REFIN PEAK-PEAK VOLTAGE NOISE (0.1Hz TO 10Hz)

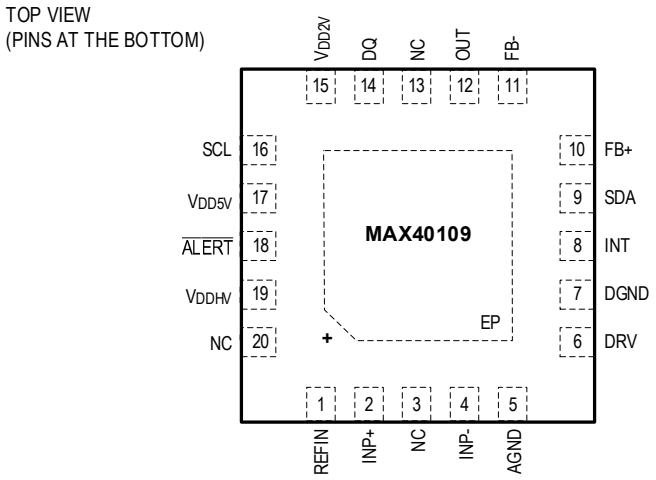


V_{DDHV} = 5V, V_{DRV} = 4V, V_{IN}+ = V_{IN}- = V_{DRV}/2, Analog Filter BW = 1.2kHz, Typical values at 25°C, Min\Max Temperature = -40ºC ≤ T_A ≤ +125ºC.

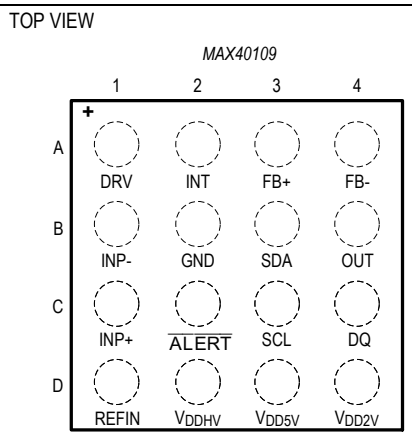




Pin Configurations



20-PIN TQFN
(4mm × 4mm)



16-WLP

Pin Descriptions

PIN		NAME	FUNCTION
TQFN	WLP		
6	A1	DRV	Sensor Bridge Drive: Drive either current or voltage. It is also used to measure the temperature (as a voltage) from the bridge.
2	C1	INP+	Non-inverting Pressure Sensor Input. Users can connect up to 10nF between INP+ and INP-.
4	B1	INP-	Inverting Pressure Sensor Input. Users can connect up to 10nF between INP+ and INP-.
n/a	B2	GND	Ground
5	—	AGND	Analog Ground
7	—	DGND	Digital Ground

19	D2	V_{DDHV}	Main positive supply voltage and power line communication serial interface input. The range is from 3V to 36V. The suggested (but not required) bypass capacitor for voltage output mode is from 10nF to 100nF. In current output mode, the maximum bypass capacitor is 10nF.
8	A2	INT	Input Temperature: Connect to either a diode or a thermistor.
1	D1	REFIN	Input reference and also bypass capacitor (100nF) for the Internal reference: A bit in the Config Register selects between external and internal voltage reference.
9	B3	SDA	I^2C Data
16	C3	SCL	I^2C Clock
14	C4	DQ	1-Wire Serial Input/Output. It must be held to a logic level high when idle.
18	C2	$\overline{ALERT}$	Active Low Alert Interrupt Output. See the *ALERT Mode* section for the functionality of this output.
10	A3	FB+	Output Amplifier Feedback Input, Positive.
11	A4	FB-	Output Amplifier Feedback Input, Negative.
12	B4	OUT	Analog output, as well as PLC serial interface output.
17	D3	V_{DD5V}	Internal 5V output from LDO: Bypass with a 220nF capacitor.
15	D4	V_{DD2V}	Internal 1.8V output from LDO: Bypass with a 220nF capacitor.
3, 13, 20	—	NC	Do not connect.
EP	—	EP	Exposed Pad. Connect to analog ground.

Detailed Description

The MAX40109 is a low-power, precision sensor interface SoC that includes a high-precision, programmable AFE, ADC, calibration memory, and digital signal processing. It also includes a DAC with an output buffer to support analog voltage output and a 4mA–20mA current loop. It is designed for sensor applications such as strain gauges, pressure, force, and temperature.

Register Function

The registers are accessible from all digital interfaces such as 1-Wire, I^2C, and PLC.

All digital interfaces follow the same sequence of sending the register address first (command field), followed by the data field. Data can be either one byte or two bytes, depending on the type of register.

Upon power-up, all registers listed in *Table 1* as both Random-access memory (RAM) and Multi-time programmable (MTP) memory will initialize with the last saved content in the MTP memory. Such content can be overwritten during normal functionality, but unless saved in the MTP memory, this new content will be lost once the device is powered down. See the section *Burning to MTP* for the procedure of saving the register content in the MTP memory.

Table 1. Register Functions and POR States

REGISTER NAME	ADDRESS (HEX)	NUMBER OF BITS	POR STATE (HEX)	READ/WRITE	DESCRIPTION
Configuration	00h	16	0000h	R/W	The configuration register contains bit control for MTP enable, temperature calibration enable, digital filter, reference input, current source reference resistor, shutdown, temperature current, alert mode, and PGA input mux.
Status	02h	12	000h	R/W	The status register reports all the anomalies that generate an interrupt on the $\overline{ALERT}$ output pin.
PGA Pressure Gain	04h	8	00h	R/W	The PGA pressure gain register selects between 20 settings.
Current Source	05h	3	0h	R/W	The current source register selects between 8 settings.
Uncalibrated Pressure	06h	16	0000h	RO	The uncalibrated pressure register holds the last pressure measurement data from the ADC before the digital calibration.
Uncalibrated Temperature	08h	16	0000h	RO	The uncalibrated temperature register holds the last temperature measurement from the ADC before the digital calibration.
ADC Sample Rate	0Ah	4	0h	R/W	The ADC sample rate register contains bits to control the sample rate pressure, sample rate temperature, and system switch time between samples.
Interrupt Enable	0Bh	10	3FFh	R/W	The interrupt enable register includes the enables for interrupt generation flags with the same bit order as the status register.
Bridge Drive	0Dh	3	0h	R/W	The bridge drive register connects the sensor bridge to either a current or a voltage source.

REGISTER NAME	ADDRESS (HEX)	NUMBER OF BITS	POR STATE (HEX)	READ/WRITE	DESCRIPTION
PGA Temperature Gain	0Eh	8	0h	R/W	The PGA temperature gain register selects between 16 settings.
Calibrated Pressure	0Fh	16	0000h	RO	The calibrated pressure register holds the last pressure measurement after the digital calibration.
Calibrated Temperature	11h	16	0000h	RO	The calibrated temperature register holds the last temperature measurement after the digital calibration.
Temp Mode	13h	5	00h	R/W	The temp mode register configures the temperature channel at the INT and DRV pins.
Sensor Offset Cal Config	14h	3	0h	R/W	The sensor offset cal configuration register is used during the sensor offset calibration procedure to cancel out the sensor offset.
Analog Filter BW	15h	2	0h	R/W	The analog filter BW register is used to select the internal analog filter for the pressure channel.
Zero Pressure Offset RAM Override	1Ah	16	0000h	R/W	The zero pressure filter offset RAM override register can override and replace the content of the MTP register "zero pressure offset". This register is only temporary since it is a RAM register.
Zero Pressure Offset Select	1Ch	1	0h	R/W	Sets the zero pressure offset RAM override value.
Analog Output Stage	1Eh	4	0h	R/W	The analog output stage register sets the signal at the OUT pin.
SLP_MR	9Bh	16	0000h	R/W	Register for initializing MTP.
SLP_MREF	9Dh	16	0000h	R/W	Register for initializing MTP.
CP_Control_1	9Fh	8	00h	R/W	Control register 1.
CP_Control_2	A0h	8	00h	R/W	Control register 2.
MTP_Control	A2h	8	00h	R/W	MTP control.
MTP_Status	A3h	8	00h	R/W	MTP status.
MTP_PROT_ADDR	A4h	8	00h	R/W	MTP prototyping write address.
MTP_PROT_WDATA	A5h	16	0000h	R/W	MTP prototyping write data.
MTP_PROT_RDATA	A7h	16	0000h	RO	MTP prototyping read data
MTP_LEVEL	A9h	16	00h	RO	MTP burn count.
SLP_MRV	ABh	16	0000h	R/W	Register for initializing MTP.
SLP_MREFV	ADh	16	0000h	R/W	Register for initializing MTP.
MTP_DATA0	AFh	16	0000h	R/W	Setting MTP data.
MTP_ADDR	B1h	8	00h	R/W	Setting MTP address.

Configuration Register

The configuration register contains 16 bits of data. When entering shutdown in Power Line Communication, the device will not be able to exit shutdown since it relies on the OUT pin to be active.

Table 2. Configuration Register

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
MTP_EN	Temp Cal Bypass	Pressure Cal Bypass	Digital Filter	Digital Filter	Digital Filter	REFIN internal/external selection	Current Source Reference Resistor
BIT 7	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Shutdown	Reserved	Temp Current	Temp Current	$\overline{\text{ALERT}}$ Mode	$\overline{\text{ALERT}}$ Mode	$\overline{\text{ALERT}}$ Mode	PGA Input MUX

PGA Input Mux

Bit 0 is used to select the input MUX in front of the PGA.

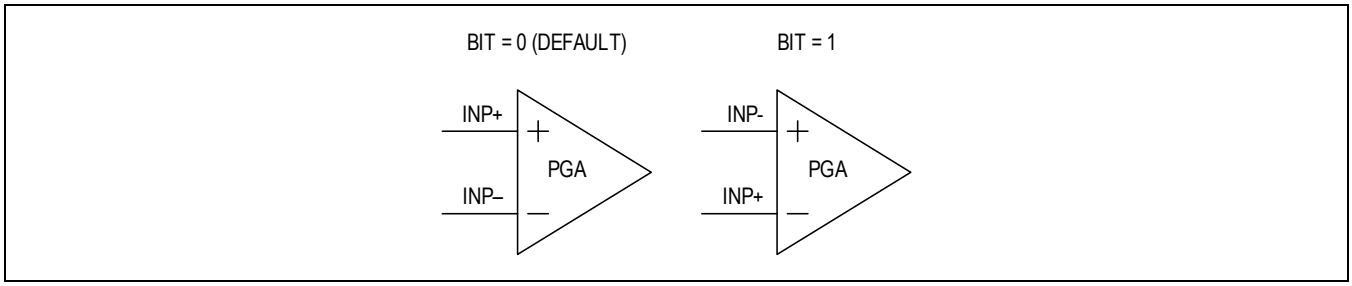


Figure 1. PGA Mux Input

$\overline{\text{ALERT}}$ Mode

The $\overline{\text{ALERT}}$ mode contains 3-bit of data, as shown in *Table 3*.

Table 3. $\overline{\text{ALERT}}$ [3:1]

BIT 3	BIT 2	BIT 1	$\overline{\text{ALERT}}$ MODE
0	0	0	$\overline{\text{ALERT}}$ issues interrupts
0	0	1	$\overline{\text{ALERT}}$ issues temperature data in PWM fashion
0	1	0	$\overline{\text{ALERT}}$ issues pressure digital output - case 1
0	1	1	$\overline{\text{ALERT}}$ issues pressure digital output - case 2
1	0	0	$\overline{\text{ALERT}}$ issues pressure digital output - case 3
1	0	1	$\overline{\text{ALERT}}$ issues pressure digital output - case 4
1	1	0	Not Used
1	1	1	Not Used

000: The $\overline{\text{ALERT}}$ output is used to issue interrupts as defined in the "Status" register by using the "Interrupt Enable" register as a mask.

001: The $\overline{\text{ALERT}}$ output generates a PWM signal based on the most significant 12-bit of the data from the "Calibrated Temperature" register. The PWM frequency is fixed at 2MHz / 4,096 = 488Hz.

Pressure Digital Output cases:

Table 4. Cases for Alert

CASE #	THRESHOLD 1 (PRIMARY)	THRESHOLD 2 (HYSTERESIS)	OUTPUT STATE
1	Rising above threshold		Low to high
		Falling below threshold	High to low
2	Rising above threshold		High to low
		Falling below threshold	Low to high
3	Falling below threshold		Low to high
		Rising above threshold	High to low
4	Falling below threshold		High to low
		Rising above threshold	Low to high

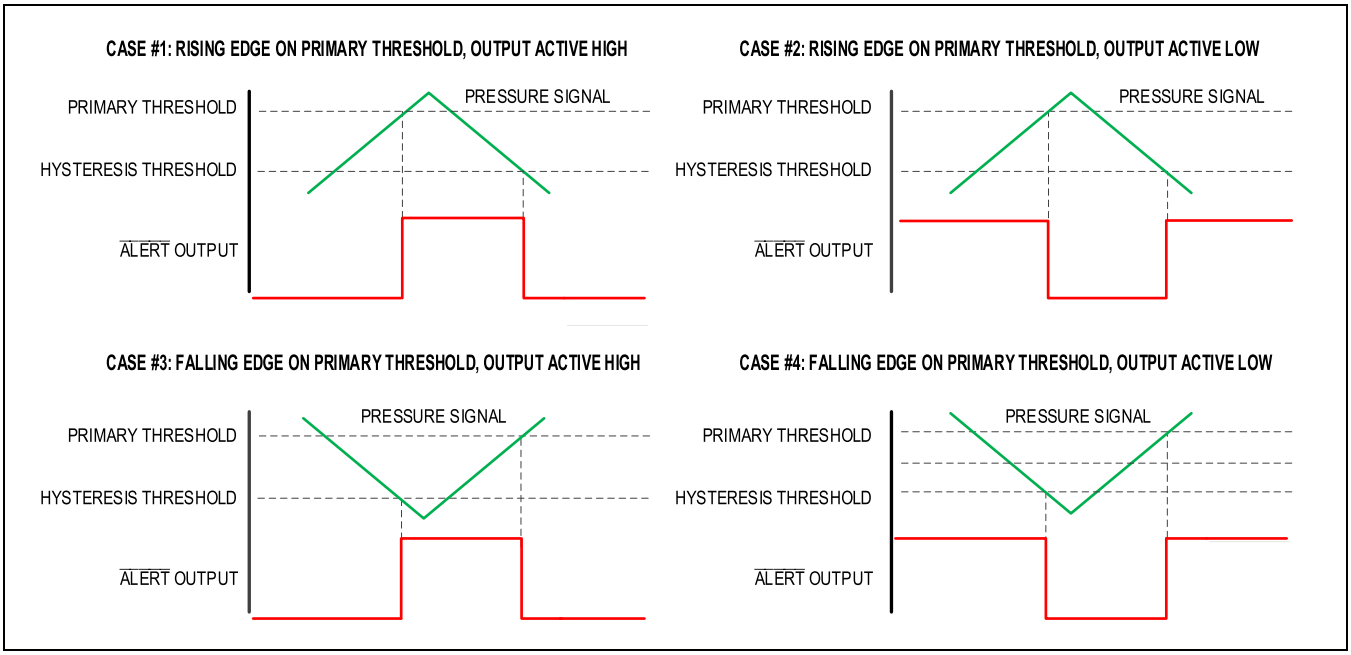


Figure 2. $\overline{\text{ALERT}}$ Cases

Temp Current

Current Source for temperature measurement. This current is generated to the INT pin when an external thermistor is used.

Table 5. Source Current [5:4]

BIT 5	BIT 4	SOURCE CURRENT (µA)
0	0	150
0	1	250
1	0	500

1	1	750

Shutdown

Bit 7 is used to shutdown the MAX40109.

Bit 7 = 0: The MAX40109 is active (default).

Bit 7 = 1: The MAX40109 is in shutdown mode. In this mode, all analog functionality is disabled, and the device only responds to 1-Wire and I^2C commands.

Current Source Reference Resistor

Bit 8 is used to select a reference resistor for the current source between the internal resistor and the external resistor connected to the INT pin.

See the *Applications Information* section "*Use External Resistor for Bridge Current Source*" for more details.

Bit 8 = 0: Internal resistor (default).

Bit 8 = 1: External resistor.

If an external resistor is selected, it is not possible to set the temp mode to thermistor.

Reference

Bit 9 is used to select between the internal and external references.

Bit 9 = 0: Use internal reference (default).

Bit 9 = 1: Use external reference.

Digital Filter

This option calculates the average among samples. See *Table 6* for more details.

Table 6. Digital Filter [12:10]

BIT 12	BIT 11	BIT 10	FUNCTION
0	0	0	No Average
0	0	1	Average among 4 samples
0	1	0	Average among 8 samples
0	1	1	Average among 16 samples
1	0	0	Average among 32 samples
1	0	1	Average among 64 samples
1	1	0	Average among 128 samples

The output data rate is as follows:

Table 7. Output Data Rate

OPTION #	ADC SAMPLE RATE OPTIONS (ksps)	OUTPUT DATA RATE						
		NO FILTER	x4	x8	x16	x32	x64	x128
1	1	1	0.25	0.125	0.0625	0.03125	0.015625	0.0078125
2	2	2	0.5	0.25	0.125	0.0625	0.03125	0.015625
3	4	4	1	0.5	0.25	0.125	0.0625	0.03125
4	8	8	2	1	0.5	0.25	0.125	0.0625

5	16	16	4	2	1	0.5	0.25	0.125

Pressure Cal Bypass

Bit 13 = 0: Pressure calibration is enabled (default).

Bit 13 = 1: Pressure calibration is bypassed (Raw Mode).

In this Raw Mode, the MAX40109 only measures pressure (no temperature) and provides at the analog output (OUT) the raw sensor data without any digital correction. Analog chain settings must be programmed (PGA gain, coarse offset correction, bridge current/voltage, ADC sample rate).

Temp Cal Bypass

Bit 14 = 0: Temperature calibration is enabled (default).

Bit 14 = 1: Temperature calibration is bypassed (Raw Mode) In this Raw Mode, the MAX40109 only measures temperature (no pressure) and provides at the analog output (OUT) the raw temp sensor data (either from the sensor bridge or from the external thermistor) without any digital correction. Analog chain settings must be programmed (PGA gain, coarse offset correction, bridge current/voltage, and ADC sample rate).

MTP_EN

Bit 15 = 0: User can access MTP memory for read/write via any Interfaces (1-Wire and I^2C) – Default at power up.

Bit 15 = 1: MTP memory is disabled (to save power in the digital interface).

Status Register

The status register reports all anomalies. The ones enabled in the "Interrupt Enable" register will also generate an interrupt on the $\overline{\text{ALERT}}$ output pin.

Pressure Data Ready is not an anomaly. It informs the Host Processor that new data is available in the Pressure register. Temperature Data Ready is not an anomaly either. It informs the Host Processor that new data is available in the register Temperature. Each alert can be masked out with the register Interrupt Enable with the exception of DRV Fault and INT Fault. These two faults are not masked because they must be reported whenever they occur.

- DRV Fault: Occurs when the voltage at the DRV pin exceeds 4.25V or when the inputs INP+ and INP- wander away from the DRV/2 point by more than 30%. The latter condition, combined with checking the levels at INP+ and INP- (through OV_INP+, UV_INP+, OV_INP-, UV_INP-) enables detecting whether or not the inputs INP+ and/or INP- are open (not connected to the sensor bridge).
- INT Fault: Occurs when the voltage at the INT pin exceeds 2V.

In case any of these faults happen, the user has the possibility to shutdown the MAX40109 by accessing the shutdown bit in the Configuration register. The user can select which faults to receive on the $\overline{\text{ALERT}}$ pin by using the Interrupt Enable register.

Table 8. Status Register

BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DRV Fault	INT Fault	Temp Data Ready	Pressure Data Ready	UV_DRV	OV_DRV	UV_INT	OV_INT	UV_INP-	OV_INP-	UV_INP+	OV_INP+

To clear each flag in bits D11 to D0, a write to this register with the same word that was read is required. Writing 1 will clear the bit that reads 1. When doing this flag clearing, what is written in the upper byte is meaningless and will not affect this register.

PGA Pressure Gain

This register selects the PGA Pressure Gain.

Bits [7:6] are reserved bits.

Table 9. PGA Pressure Gain

BIT [7:6]	BIT [5:4]	BIT 3	BIT 2	BIT 1	BIT 0	GAIN (V/V)
xx	00	1	1	1	1	5
xx	00	0	0	0	0	10
xx	00	0	0	0	1	15
xx	00	0	0	1	0	20
xx	00	0	0	1	1	24
xx	00	0	1	0	0	40
xx	00	0	1	0	1	60
xx	00	0	1	1	0	72
xx	00	0	1	1	1	90
xx	00	1	0	0	0	108
xx	00	1	0	0	1	126
xx	00	1	0	1	0	144
xx	00	1	0	1	1	160
xx	00	1	1	0	0	180
x	00	1	1	0	1	200
xx	00	1	1	1	0	252
xx	01	0	0	0	0	540
xx	01	0	0	0	1	1080
xx	01	0	0	1	0	1440
xx	01	0	0	1	1	2520

Current Source

This register selects the current source values.

Table 10. Current Source

BIT 2	BIT 1	BIT 0	CURRENT (µA)
0	0	0	250
0	0	1	300
0	1	0	400
0	1	1	450
1	0	0	500
1	0	1	550
1	1	0	650
1	1	1	750

Uncalibrated Pressure

16-bit read-only register that holds the last pressure measurement data from the ADC before the digital calibration.

The pressure format is normalized. The smallest pressure is 1.0/32768 (0x0001), and the largest is 32767/32768 (0x7FFF).

Table 11. Uncalibrated Pressure Format

SIGN	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Two's complement format:

- 0x7FFF (equates to 32,767): corresponds to pressure max positive range.
- 0x0000 (equates to 0): corresponds to mid-scale or zero-pressure.
- 0x8000 (equates to -32,768): corresponds to pressure max negative range.

Uncalibrated Temperature

16-bit read-only register that holds the last temperature measurement data from the ADC prior to the calibration.

The temperature measurement is effectively a voltage measurement performed by the MAX40109.

See the *Applications Information* section for more details.

Users can choose the unit scale (°C or °K) in their MCU firmware. The MAX40109 is agnostic to the unit scale.

Table 12. Uncalibrated Temperature Format

SIGN	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Units

ADC Sample Rate

Select ADC Sample Frequency

Table 13. Sample Rate Selection

BIT 3	BIT 2	BIT 1	BIT 0	SAMPLE RATE PRESSURE (ksps)	SAMPLE RATE TEMPERATURE (sps)	SYSTEM SWITCH TIME BETWEEN P SAMPLE AND T SAMPLE (µs)
0	0	0	0	1	1	500
0	0	0	1	1	10	500
0	0	1	0	2	1	250
0	0	1	1	2	10	250
0	1	0	0	4	1	125
0	1	0	1	4	10	125
0	1	1	0	8	1	62.5
0	1	1	1	8	10	62.5
1	0	0	0	16	1	31.25
1	0	0	1	16	10	31.26

The temperature sample must be interleaved between two pressure samples seamlessly, meaning that the pressure data-rate must never be interrupted.

Interrupt Enable

This register includes the enables for interrupt generation flags with the same bit order as they are reported in the status register. 1 = Interrupt is enable (default). 0 = Interrupt is disabled POR condition is 0xFF.

Table 14. Interrupt Register

BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Temp Data Ready	Pressure Data Ready	UV_DRV	OV_DRV	UV_INT	OV_INT	UV_INP-	OV_INP-	UV_INP+	OV_INP+

Bridge Drive

Table 15. Bridge Drive

BRIDGE DRIVE	BIT 2	BIT 1	BIT 0	COMMENT
Disconnected	0	0	0	Default mode at device power up
Current Source	0	0	1	The ADC reference is connected to the internal reference
Voltage Source at 4V	0	1	0	The ADC reference is connected to the bridge voltage
Voltage Source at 3.3V	0	1	1	The ADC reference is connected to the bridge voltage
Voltage Source at 1.8V	1	0	0	The ADC reference is connected to the bridge voltage
Voltage Source at 2.3V	1	0	1	The ADC reference is connected to the bridge voltage

PGA Temperature Gain

This register selects the PGA Temperature Gain.

Bits [7:4] are spare bits for future use.

Table 16. PGA Temperature Gain

BITS [7:4]	BIT 3	BIT 2	BIT 1	BIT 0	Gain (V/V)
xxxx	0	0	0	0	1.5
xxxx	0	0	0	1	2
xxxx	0	0	1	0	3
xxxx	0	0	1	1	5
xxxx	0	1	0	0	6
xxxx	0	1	0	1	10
xxxx	0	1	1	0	15
xxxx	0	1	1	1	20
xxxx	1	0	0	0	24
xxxx	1	0	0	1	30
xxxx	1	0	1	0	36
xxxx	1	0	1	1	40
xxxx	1	1	0	0	45
xxxx	1	1	0	1	60
xxxx	1	1	1	0	72
xxxx	1	1	1	1	90

Calibrated Pressure

16-bit read-only register that holds the last pressure measurement data after the digital calibration.

The pressure format is normalized. The smallest pressure is 1.0/32768 (0x0001), and the largest is 32767/32768 (0x7FFF).

Table 17. Calibrated Pressure Format

SIGN	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Two's complement format:

- 0x7FFF (equates to 32,767): corresponds to pressure max positive range.
- 0x0000 (equates to 0): corresponds to mid-scale or zero-pressure.
- 0x8000 (equates to -32,768): corresponds to pressure max negative range.

Calibrated Temperature

16-bit read-only register that holds the last temperature measurement data after the digital temp calibration.

The temperature measurement is effectively a voltage measurement performed by the MAX40109.

See the *Applications Information* section for more details.

The user may choose the unit scale (°C or °K) in their MCU firmware. The MAX40109 is agnostic to the unit scale.

Table 18. Calibrated Temperature Format

SIGN	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Units

Temp Mode

Select how to configure the temperature channel at INT and DRV pins.

See the *Temperature Measurement* section *Applications Information* for more details.

Table 19. Temp Mode

BITS [4:3]	BITS [2:0]
Voltage Divider (DRV input only)	Temp Mode

Table 20. Temp Mode [2:0]

BIT 2	BIT 1	BIT 0	INPUT PIN INVOLVED	FUNCTION
0	0	0	INT	Single-ended with G = 1.
0	0	1	INT	Single-ended with G>1.
0	1	0	INT	Differential with DAC's Offset.
0	1	1	DRV	Single-ended with G = 1.
1	0	0	DRV	Differential with DAC's Offset.
1	0	1	n/a	Not Used.
1	1	0	n/a	Not Used.
1	1	1	n/a	Not Used.

Table 21. Temp Mode [4:3]

BIT 4	BIT 3	INPUT PIN INVOLVED	FUNCTION
0	0	DRV	Scale Input Voltage at DRV by 1.
0	1	DRV	Scale Input Voltage at DRV by 0.5.
1	0	DRV	Scale Input Voltage at DRV by 0.375.
1	1	DRV	Scale Input Voltage at DRV by 0.25.

Sensor Offset Cal Config

This register is used during the sensor offset calibration procedure with the purpose of cancelling out the sensor offset. See the *Sensor Offset Calibration* section in *Applications Information* for more details.

Table 22. Sensor Offset Calibration Configuration

BIT 2	BIT 1	BIT 0
1 = Connect Trim Resistor 0 = Short out Trim Resistor (default)	1 = Connect Offset Calibration Current Source 0 = Disconnect Offset Calibration Current Source (default)	1 = Set Pressure PGA into bypass mode (G = 2V/V) 0 = Normal PGA functionality (default)

Analog Filter BW

This register is used to select the internal analog filter for the pressure channel.

Table 23. Analog Filter Bandwidth

BIT 1	BIT 0	ANALOG FILTER BANDWIDTH (-3dB)
0	0	1.2kHz
0	1	9kHz
1	0	37kHz
1	1	45kHz

Zero Pressure Offset RAM Override

This register can override and replace the content of the MTP register "Zero Pressure Offset". This replacement is only temporary since this is a RAM register. At the next power cycle, the content of the MTP register "Zero Pressure Offset" is restored.

The replacement only happens if the Zero Pressure Offset Select register is set to 1 and Zero Pressure Offset is enabled in the MTP memory. The Zero Pressure Offset feature should only be used when a current or voltage is selected in the Bridge Drive register of the MAX40109.The input common mode must be approximately DRV/2 for proper functionality.

16-bit register that sets the amount of bridge sensor offset that feeds the offset cancellation circuit in the analog PGA.

The format for ZERO_PRESSURE_OFFSET:

- 0x7FFF corresponds to an applied offset of -90mV/V.
- 0x0000 corresponds to mid-scale or 0mV/V.
- 0xFFFF corresponds to an applied offset of +90mV/V.

The most significant bit controls the sign of the applied offset (0 = negative, 1 = positive). See *Table 31* for the weight of each bit from [14:0].

Zero Pressure Offset Select

Bit 0 is used to select a zero pressure offset value from the RAM.

Analog Output Stage

The MAX40109 uses four bits to configure the analog output stage as follows.

See the *Analog Output Stage* section in *Applications Information*.

Table 24. Analog Output Setting (AOS)

AOS [3:0] BITS	FUNCTION	RESISTOR	V_{DDHV} (MIN)	FULL SCALE V/I	COMMENTS	UNITS
0x0	shutdown	—	3V	—	—	—
0x1	reserved	—	—	—	—	—
Either of the following: 0x2, 0xD, 0xE, 0xF	ratio-metric voltage	Int	3V	1 x V_{DD5V}	—	V
0x3				0.91 x V_{DD5V}	Use when V_{DDHV} = 3.3V	
0x4				0.6 * V_{DD5V}	Use when V_{DDHV} = 5.0V	
0x5		Ext	3V	0.1515 x V_{DD5V} x extGain	—	
0x6				0.25 x V_{DD5V} x extGain	—	
0x7	absolute current	—	5V	0.96 x REFIN/R_{SENSE}	—	A
0x8	absolute voltage	Int	3V	4 x REFIN	REFIN = 1.25V, 5V FS	V
0x9, 0xA				6 x REFIN	REFIN = 0.5V, 3V FS	
0xB		Ext	3V	0.4 x REFIN x extGain	—	
0xC				1 x REFIN x extGain	—	

SLP_MR

16-bit register reserved for MTP initialization.

SLP_MREF

16-bit register reserved for MTP initialization.

CP_Control_1

8-bit register reserved for MTP burning.

CP_Control_2

8-bit register reserved for MTP burning.

MTP_Control

Table 25. MTP_Control Register

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MTP_RESTORE	RESERVED	RESERVED	MTP_PROT_EN	RESERVED	RESERVED	STOP_PROG	SRT_PROG

The MTP_Control register is used in MTP prototyping to the shadow register and burning to the MTP registers.

SRT_PROG: Used to start MTP burn.

STOP_PROG: Used to stop MTP burn.

MTP_PROT_EN: Used for prototype an MTP write to the shadow registers before burning to the MTP registers.

MTP_RESTORE: Used for restoring the MTP registers during prototyping of an MTP write to the shadow registers.

MTP_Status

Table 26. MTP_Status

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONE	ECC_ERR_2BIT	ECC_ERR_1BIT	RESERVED	VPP_INIT_FAIL	MTP_FULL	VERI_FAIL	VPP_ACT

The MTP_Status register provides MTP status during a burn procedure.

VPP_ACT: VPP is high (or low) voltage before the burn starts. Therefore, we abandoned the burn as we cannot control over external programming voltage.

VERI_FAIL: The burn was attempted three times, but all three times, the verification failed.

MTP_FULL: There is no space left in the MTP to burn.

VPP_INIT_FAIL: VPP does not reach the desired voltage before the burn starts, so the burn is abandoned.

ECC_ERR_1BIT: One or more active records that were loaded on boot have a 1-bit error that was corrected. If a record contains a 1-bit error, but a new record comes and overwrites the data, the 1-bit error status will be cleared.

ECC_ERR_2BIT: The records that were loaded on boot have a 2-bit error that was detected and not corrected. This indicates a catastrophic failure that needs to be dealt with at the system level (eg: go to a safe mode). Once any record contains a 2-bit error, this status bull will never get cleared by another record.

DONE: Indicates a burn is completed.

MTP_PROT_ADDR

MTP_PROT_ADDR is used to prototype a desired 8-bit MTP address.

MTP_PROT_WDATA

MTP_PROT_WDATA is used to prototype a desired 16-bit data before burning into MTP.

MTP_PROT_RDATA

MTP_PROT_RDATA is used to read the 16-bit prototype data before burning to MTP.

MTP_LEVEL

The MTP_LEVEL register indicates the number of burns remaining in the MTP register.

SLP_MRV

16-bit register reserved for MTP initialization.

SLP_MREFV

16-bit register reserved for MTP initialization

MTP_DATA0

MTP_DATA0 is the 16-bit data to burn into the desired MTP register.

MTP_ADDR

The MTP_ADDR register is the desired 8-bit MTP register to burn

MTP Memory and Functions

An MTP (Multi-Time-Programmable) memory is used to perform the functions in the following paragraphs.

Table 27. MTP Registers

REGISTER NAME	ADDRESS (HEX)	NUMBER OF BITS	POR STATE	READ/WRITE	DESCRIPTION
CAL_DATA0	00h	16	0000h	R/W	K_0 Coefficient [15:0].
CAL_DATA1	01h	16	0000h	R/W	K_0 Coefficient [31:16].
CAL_DATA2	02h	16	0001h	R/W	K_1 Coefficient [15:0].
CAL_DATA3	03h	16	0000h	R/W	K_1 Coefficient [31:16].
CAL_DATA4	04h	16	0000h	R/W	K_2 Coefficient [15:0].
CAL_DATA5	05h	16	0000h	R/W	K_2 Coefficient [31:16].
CAL_DATA6	06h	16	0000h	R/W	K_3 Coefficient [15:0].
CAL_DATA7	07h	16	0000h	R/W	K_3 Coefficient [31:16].
CAL_DATA8	08h	16	0000h	R/W	H_0 Coefficient [15:0].
CAL_DATA9	09h	16	0000h	R/W	H_0 Coefficient [31:16].
CAL_DATA10	0Ah	16	0000h	R/W	H_1 Coefficient [15:0].
CAL_DATA11	0Bh	16	0000h	R/W	H_1 Coefficient [31:16].
CAL_DATA12	0Ch	16	0000h	R/W	H_2 Coefficient [15:0].
CAL_DATA13	0Dh	16	0000h	R/W	H_2 Coefficient [31:16].
CAL_DATA14	0Eh	16	0000h	R/W	H_3 Coefficient [15:0].
CAL_DATA15	0Fh	16	0000h	R/W	H_3 Coefficient [31:16].
CAL_DATA16	10h	16	0001h	R/W	G_0 Coefficient [15:0].
CAL_DATA17	11h	16	0000h	R/W	G_0 Coefficient [31:16].
CAL_DATA18	12h	16	0000h	R/W	G_1 Coefficient [15:0].
CAL_DATA19	13h	16	0000h	R/W	G_1 Coefficient [31:16].
CAL_DATA20	14h	16	0000h	R/W	G_2 Coefficient [15:0].
CAL_DATA21	15h	16	0000h	R/W	G_2 Coefficient [31:16].
CAL_DATA22	16h	16	0000h	R/W	G_3 Coefficient [15:0].
CAL_DATA23	17h	16	0000h	R/W	G_3 Coefficient [31:16].
CAL_DATA24	18h	16	0000h	R/W	N_0 Coefficient [15:0].
CAL_DATA25	19h	16	0000h	R/W	N_0 Coefficient [31:16].
CAL_DATA26	1Ah	16	0000h	R/W	N_1 Coefficient [15:0].
CAL_DATA27	1Bh	16	0000h	R/W	N_1 Coefficient [31:16].
CAL_DATA28	1Ch	16	0000h	R/W	N_2 Coefficient [15:0].
CAL_DATA29	1Dh	16	0000h	R/W	N_2 Coefficient [31:16]
CAL_DATA30	1Eh	16	0000h	R/W	N_3 Coefficient [15:0].
CAL_DATA31	1Fh	16	0000h	R/W	N_3 Coefficient [31:16].
CAL_DATA32	20h	16	0000h	R/W	M_0 Coefficient [15:0].
CAL_DATA33	21h	16	0000h	R/W	M_0 Coefficient [31:16].
CAL_DATA34	22h	16	0000h	R/W	M_1 Coefficient [15:0].

REGISTER NAME	ADDRESS (HEX)	NUMBER OF BITS	POR STATE	READ/WRITE	DESCRIPTION
CAL_DATA35	23h	16	0000h	R/W	M_1 Coefficient [31:16].
CAL_DATA36	24h	16	0000h	R/W	M_2 Coefficient [15:0]..
CAL_DATA37	25h	16	0000h	R/W	M_2 Coefficient [31:16]
CAL_DATA38	26h	16	0000h	R/W	M_3 Coefficient [15:0].
CAL_DATA39	27h	16	0000h	R/W	M_3 Coefficient [31:16].
SP_DATA0	28h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA1	29h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA2	2Ah	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA3	2Bh	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA4	2Ch	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA5	2Dh	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA6	2Eh	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA7	2Fh	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA8	30h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA9	31h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA10	32h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA11	33h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA12	34h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA13	35h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA14	36h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
SP_DATA15	37h	16	0000h	R/W	Scratchpad memory for general purpose and device identification.
DIAG_DATA0	38h	16	FF00h	R/W	bits [5:8]: overpressure +, bits [7:0]: under pressure +
DIAG_DATA1	39h	16	FF00h	R/W	bits [15:8]: overpressure -, bits [7:0]: under pressure -

REGISTER NAME	ADDRESS (HEX)	NUMBER OF BITS	POR STATE	READ/WRITE	DESCRIPTION
DIAG_DATA2	3Ah	16	FF00h	R/W	bits [15:8]: overvoltage temperature, bits [7:0]: under voltage temperature
DIAG_DATA3	3Bh	16	FF00h	R/W	bits [15:8]: overvoltage drive, bits [7:0]: under voltage drive.
PRESSURE_THRESOLD	3Ch	16	0000h	R/W	bits [15:8]: primary threshold pressure value, bits [7:0]: hysteresis threshold pressure value.
ZERO_PRESSURE_OFFSET	3Dh	16	0000h	R/W	PGA sensor offset.
TEMP_OFFSET	3Eh	16	0000h	R/W	bits [8:0]: temperature offset.
CLIPPING_THRESHOLD	3Fh	16	0000h	R/W	bit 10: clipping threshold enabled, bits [9:5]: upper, bits [4:0]: lower
DIAGNOSTIC_RANGE	40h	16	0000h	R/W	bit 8: diagnostic range enabled, bits [7:4]: upper, bits [3:0]: lower
FUNC_CONFIGURATION	41h	16	0000h	R/W	bit 14: temperature bypass calibration, bit 13: pressure bypass calibration, bit [12:10]: digital filter, bit 9: reference input, bit 8: current source reference resistor, bits [5:4]: temperature current, bits [3:1]: alert mode, bit 0: PGA input mux
PGA_TEMP_PRES_GAIN	42h	16	0000h	R/W	bits [11:8]: PGA temperature, bits [5:0]: PGA pressure gain
MISCELLANEOUS	43h	16	0000h	R/W	bits [14:13]: voltage divider, bits [12:10]: temperature mode, bits [9:7]: bridge drive, bits [6:3]: ADC sample rate, bits [2:0]: current source
CONFIG MTP	44h	16	004Dh	R/W	bit 15: MTP lock, bit 14: zero pressure offset enabled, bit 13: sensor polarity, bits [12:9]: analog output stage, bits [6:0]: I^2C client address

Bridge Sensor Calibration

A small digital signal processor (DSP) is used for processing the converted bridge sensor data and perform temperature and non-linearity corrections (calibration).

The MAX40109 uses an MTP (Multi-Time Programmable) memory to store the calibration coefficients for pressure and temperature measurements.

The coefficients in the memory are used to build a third-order polynomial correction for both pressure and temperature non-linearity:

$T_0 = (k_0 + k_1 \times T + k_2 \times T^2 + k_3 \times T^3)$

$P_{OUT} = (h_0 + h_1 \times T_0 + h_2 \times T_0{}^2 + h_3 \times T_0{}^3) + (g_0 + g_1 \times T_0 + g_2 \times T_0{}^2 + g_3 \times T_0{}^3) \times P + (n_0 + n1 \times T_0 + n_2 \times T_0{}^2 + n_3 \times T_0{}^3) \times P^2 + (m_0 + m_1 \times T_0 + m_2 \times T_0{}^2 + m_3 \times T_0{}^3) \times P^3$

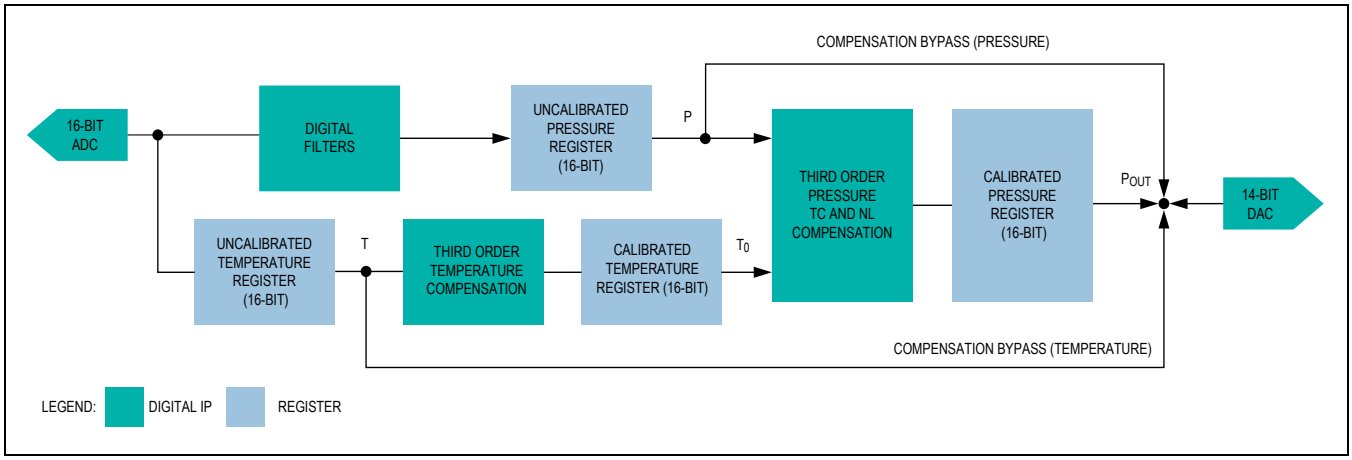


Figure 3. Bridge Sensor Calibration Diagram

The calibration can be bypassed through the Configuration Register. By bypassing the calibration the MAX40109 is providing raw sensor data (Raw Mode).

The format of the coefficients is shown in *Table 28*.

Table 28. Offset Coefficients, k_0 and h_0:

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Sign	Data														
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Data															

- All other coefficients.

Table 29. All Other Coefficients

BIT 31	BIT 30	BIT 29	BIT 28	BIT 27	BIT 26	BIT 25	BIT 24	BIT 23	BIT 22	BIT 21	BIT 20	BIT 19	BIT 18	BIT 17	BIT 16
Sign	Integer								Fraction						
BIT 15	**BIT 14**	**BIT 13**	**BIT 12**	**BIT 11**	**BIT 10**	**BIT 9**	**BIT 8**	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
Fraction															

See *Figure 4* for the calibration DSP block diagram.

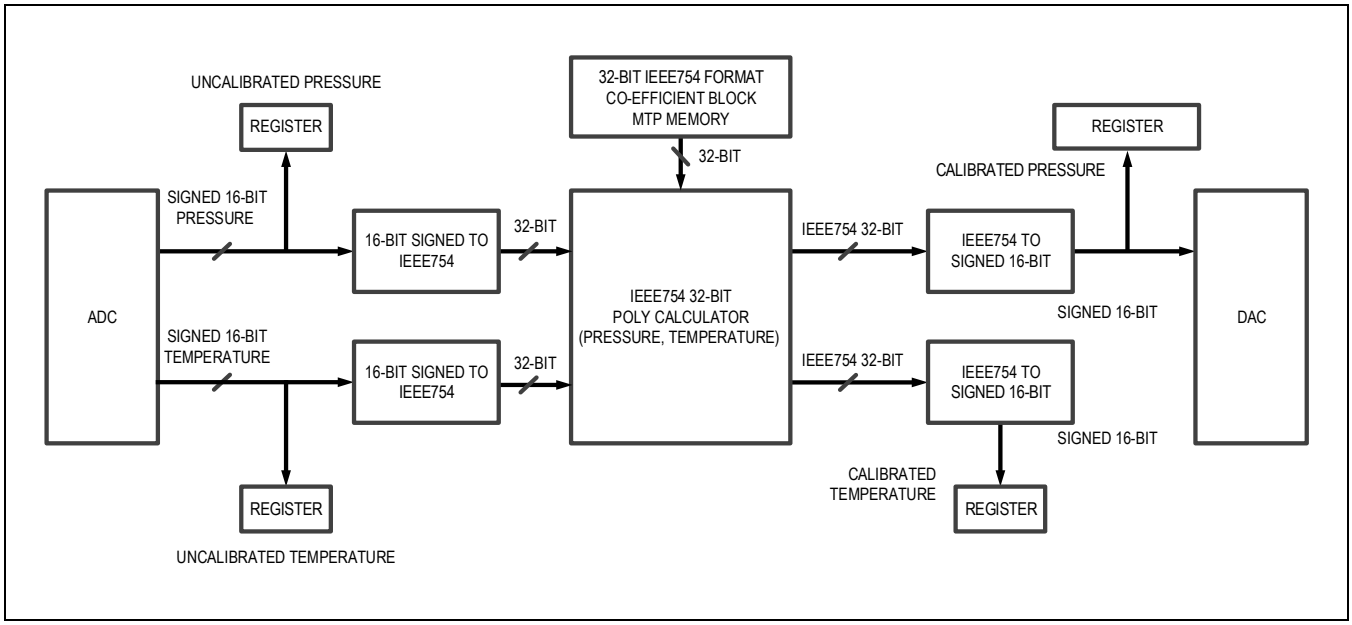


Figure 4. Calibration DSP Block Diagram

Scratch Pad Memory

The MAX40109 features 32 bytes of Scratch Pad memory (SP) for general purpose and device identification. This is a 16x16 memory-free for the user.

Diagnostics

The MAX40109 performs voltage out-of-bounds monitoring/diagnostics on the four critical sensor signals: DRV, INP+, INP-, and INT. Internally, it has an 8-bit reference DAC, which has a full-scale that is automatically set to either 5.5V or 3.6V, based on the Analog Output Stage (AOS) register bits. There are 4 AOS settings which will select the 3.6V full-scale: AOS<0×3>, AOS<0×5>, AOS<0×9>, AOS<0×B>. All other AOS settings will select the 5.5V full-scale. Note that this diagnostic reference DAC has fixed LSB steps for its full-scale voltage, LSB(V) = full-scale(V)/255, but V_{DD5V} voltage likely will bound the upper range of this DAC. Code 0xFF, which is the out-of-the-way default for overvoltage monitoring, is set to V_{DD5V}, independent of full-scale setting.

The diagnostics are as follows:

- Bridge sensor under/over voltage to monitor for sensor connectivity faults. The device compares the voltage at INP+ and INP– pins with programmable (thorough MTP memory registers) over-voltage and under-voltage thresholds:
  - OV_INP+
  - OV_INP-
  - UV_INP+
  - UV_INP-
- Bridge supply under/over voltage to monitor for sensor connectivity faults. The device compares the voltage at the DRV pin with programmable (thorough MTP memory registers) over-voltage and under-voltage thresholds:
  - OV_DRV
  - UV_DRV
- Temperature sensor under/over voltage to monitor for sensor connectivity faults. The device compares the voltage at INT with the programmable (thorough MTP memory registers) over-voltage and under-voltage thresholds:
  - OV_INT
  - UV_INT

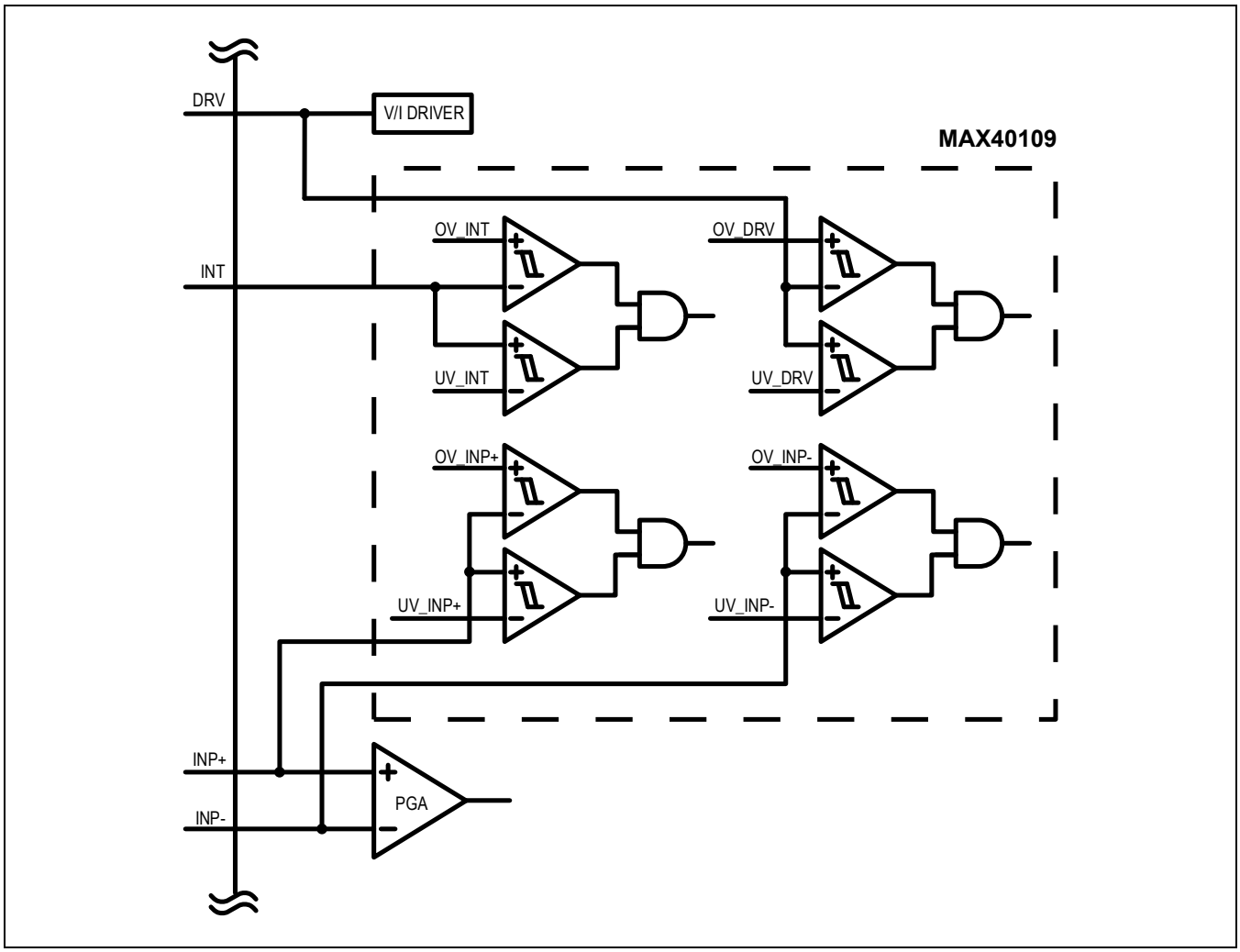


Figure 5. Diagnostic Diagram

Pressure Thresholds on $\overline{\text{ALERT}}$

The MAX40109 uses two 8-bit MTP registers to store primary/hysteresis thresholds compared against the measurements collected in the upper 8-bit of the register "Pressure".

The output of this comparison is routed to the pin $\overline{\text{ALERT}}$ if such a feature is enabled in the *Configuration* Register. See the description in that register for more details.

Zero Pressure Offset

In pressure measurement systems, some bridge offset from the sensor interferes with the desired signal. MAX40109 offers a solution to calibrate this offset out. This is done by sourcing and sinking a current through a resistor at the input of the front-end amplifier.

There are 16 total bits reserved for bridge offset calibration (br_trim<15:0>), *Table 30* describes the function of each bit:

Table 30. Zero Sensor Offset Register

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Sign	7 bits shared by both p and n sides							P-side specific trim bits				N-side trim specific trim bits			

As shown in *Table 30*, there are four bits, each reserved for both the p- and n- sides of the trim. Together with 7 bits shared by both p- and n- sides, we have 11 total bits of offset trim for each side.

The independently controlled/programmable "LSB" bits for p- and n- sides can be used to minimize the mismatch between p- and n- currents. If the p/n current mismatch residue after the trim is 0 then the sensor offset compensation remains valid for any gain setting.

If this is important, then this residue must be minimized and confirmed for the required gain values.

Table 31 shows the typical value of bridge offset compensation bit-weights. For example, when the bridge sensor input has zero pressure, if we set sign bit to 0, B14 to 1, and B13-B0 to 0 (0x4000), the typical value of offset compensation is 4.5e-2 V/V, for 2.3V bridge drive voltage, we see an effective input voltage of -103.5mV at the input. For the 1.8V bridge drive voltage, we are seeing an effective input voltage of -81mV.

Table 31. Typical Value of Bridge Offset Compensation Bit-weights (V/V)

B0, B4	B1, B5	B2, B6	B3, B7	B8	B9	B10	B11	B12	B13	B14
4.395e-05	8.789e-05	1.758e-04	3.516e-04	7.031e-04	1.406e-03	2.813e-03	5.625e-03	1.125e-02	2.250e-02	4.500e-02

This feature can be enabled/disabled with the zero-pressure offset enable MTP bit, which by default is disabled.

Config Register

Configuration register includes miscellaneous functions.

I²C Client Address

The MAX40109 uses a 7-bit MTP register to store the I²C address.

Such a register can only be written and read through the 1-wire interface.

Table 32. I²C Address

BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT1	BIT 0
7-bit I²C register accessible only by 1-wire interface						

Default value at power up is binary 100_1101

Lock MTP

The MTP lock bit is located in the MTP register CONFIG MTP (0x44), bit 15.

0 = MTP memory is not locked (default).

1 = MTP memory is locked, and no further changes are possible.

Once the MTP lock bit is burned in memory, it will stay locked and cannot be changed. MTP registers will be read-only.

Zero-pressure Offset Enable

The zero-pressure offset enable bit is located in the MTP register COMFIG MTP (0x44), bit 14.

0 = The "Zero-pressure offset" compensation is disabled.

1 = The "Zero-pressure offset" compensation is enabled.

Sensor Polarity

The sensor polarity bit is in the MTP register CONFIG MTP (0x44), bit 13.

0 = The sensor is unipolar (default).

1 = The sensor is bipolar.

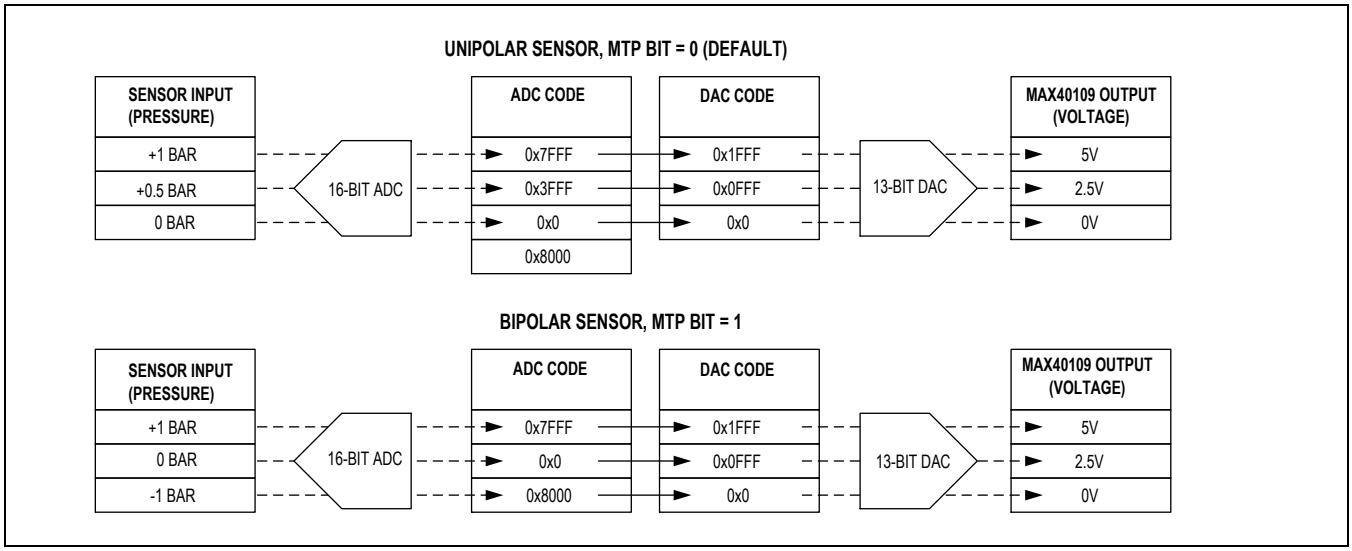


Figure 6. Sensor Polarity Data Flow

Output Clipping Enable

The output clipping enable bit is located in the MTP register CLIPPING_THRESHOLD (0x3F), bit 10.

0 = No clipping.

1 = Analog output clipping is enabled. See lower/upper clipping thresholds in the MTP memory space.

Analog Diagnostic Enable

The analog diagnostic enable bit is located in the MTP register DIAGNOSTIC_RANGE (0x40), bit 8.

0 = No analog diagnostics ($\overline{\text{ALERT}}$ and status register)

1 = Analog diagnostic is enabled. See LDR/UDR in the MTP memory space.

Temperature Offset

The MAX40109 uses 9 MTP bits to provide a DC offset value for the temperature channel when used in differential mode.

See also Configuration Register "Temp Input" bit and *Temperature Measurement* section in *Applications Information* for more details.

Table 33. Temperature Offset

MTP REGISTER NAME	MTP REGISTER DATA FIELD (9 BITS)
TEMP_OFFSET	Data. Default is 0x000

MTP Re-programmability

The MTP memory can be re-programmed a finite number of times.

In particular, the calibration memory (see "*Bridge Sensor Calibration*") can be re-programmed 40 times.

All other memories and registers can be re-programmed ten times.

Output Clipping Thresholds

The MAX40109 uses two thresholds (upper and lower) to program the analog output clipping levels.

Each of the two thresholds is a 5-bit register.

See the MTP register "*Analog Output* Stage" to determine whether the analog output is in voltage mode or current mode. The clipping range is different in the two cases.

See "*Output Clipping Enable*" to see whether this feature is enabled.

Table 34. MTP Register

MTP REGISTER NAME	DATA FIELD (BITS)	V-OUTPUT	I-OUTPUT
Lower Clipping Threshold	0_0000	2.5% of FS	3.8mA
	1_1111	25% of FS	4mA
Upper Clipping Threshold	0_0000	75% of FS	20mA
	1_1111	100% of FS	24mA

Analog Output Diagnostic Levels

The MAX40109 uses an 8-bit diagnostic register (upper and lower diagnostic range) to program the analog output diagnostic levels.

Any conditions that generate an $\overline{\text{ALERT}}$ interrupt due to a fault are usually reported to the *Status Register*. In addition to that, it will also generate an analog output alert condition by forcing the analog output (OUT) to either of the two diagnostic levels.

Table 35. Diagnostic Register

MTP REGISTER NAME	DATA FIELD (BITS)	V-OUTPUT	I-OUTPUT
Lower Diagnostic Range (LDR)	0000	0% of FS	3.6mA
	1111	2.5% of FS	3.9mA
Upper Diagnostic Range (UDR)	0000	97.5% of FS	21mA
	1111	100% of FS	24mA

Initializing MTP

When the user is ready to burn to MTP, the user will need to apply a minimum of 12V at the V_{DDHV} supply pin. The following I²C/1-Wire sequence of commands must be performed.

- Write CP_Control_1 register with 8'h80.
- Write CP_Control_2 register with 8'h1B.
- Write SLP_MR register with 16'h0302.
- Write SLP_MREF register with 16'h0200.
- Write SLP_MRV register with 16'h0300.
- Write SLP_MREFV register with 16'h0401.

Burning to MTP

When burning to MTP, 12V is the minimum supply voltage at V_{DDHV}. For each register, the user will need to burn in the data by using the following procedure.

- Write to the MTP_ADDR register with 8'hxx where xx is the desired MTP register.
- Write to the MTP_DATA0 register with 16'hxxxx where xxxx is the desired MTP data.
- Write to the MTP_Control register with 8'h01.

Example: To set the TEMP_OFFSET register in MTP, the user would set the MTP_ADDR0 register to 0x3E. Next, write 0x0FF to set the MTP_DATA register to half scale of the 9-bit DAC. Lastly, write 0x01 to the MTP_Control register.

Repeat the above steps until all the MTP registers are burned to the desired settings. Once completed, the user should power down and power up to check the MTP settings. To confirm the settings, a read must be performed.

- Write to the MTP_Control with 8'h10;
- Set the MTP_PROT_ADDR to the desired MTP address to read.
- Read from the MTP_PROT_RDATA register.

Digital Interface Management

All internal RAM registers as well as various MTP memories and registers can be accessed by any of the digital interfaces.

The only exceptions are the MTP register for I²C address that can only be accessed through 1-wire.

The MAX40109 responds to either of its digital interfaces, meaning either to 1-wire or I²C. In case of concurrent access, 1-Wire takes the priority. If the user initiates an I²C transaction during a 1-wire transaction, I²C takes priority.

1-Wire Interface

The MAX40109 1-Wire interface is a bi-directional communication through the DQ pin. The DQ line should be held to the logic level when 1-Wire is idle.

Power Line Communication (PLC)

The MAX40109 power line communication is a two-wire uni-directional interface that takes input data on the V_{DDHV} line and output data coming out from the analog OUT pin. The DQ line must also be held high to enable PLC functions. These protocols do not function if DQ is low ever.

To use the PLC, the digital signal must have a V_{IH} above 31V and a V_{IL} below 24V. DQ must be connected to a high logic level. V_{DDHV} one-wire is activated if a particular key-code is entered within 1 second of the power applied.

The V_{DDHV} key-code timer starts with a rising edge of V_{DDHV} through the V_{IH} level. There are three 50ms periods from that rising edge point in time.

In the first 50ms period, the sequence starts from a rising edge at 0ms, and there must be exactly four pulses of ≥1ms high and ≥1ms low in the first 45ms. At least the last 5ms of the 50ms period must be low for timing tolerance.

In the second 50ms period, there must be at least 5ms of low time before pulses, again, a minimum of 1ms high and 1ms low and a minimum 5ms low before the 100ms time. In this second period, there must be 1 to 4 whole pulses applied. The pulse count, 1-4, will override the 2 LSB bits of Analog Output Stage register bits (in a shadow temporary register).

In the third 50ms period, there must be at least 5ms of low time before pulses, again, a minimum of 1ms high and 1ms low. In this third period, there must be 1.5 to 4.5 pulses applied, ending at a high state. There must be a minimum of 10ms high time before the 150ms time, and 10ms held past the 150ms time to accommodate timing tolerances. The pulse count, 1.5-4.5, will override the 2 MSB bits of Analog Output Stage register bits (in a shadow temporary register).

The overall number of pulses in the second and third 50ms periods will determine the analog output configuration by overriding the Analog Output Stage MTP register with a shadow 4-bit RAM register, as follows:

In Group 2, 50ms duration:

- if we have 1 pulse (high +low) then AOS[1:0] = 00.
- if we have 2 pulses (high +low) then AOS[1:0] = 01.
- if we have 3 pulses (high +low) then AOS[1:0] = 10.
- if we have 4 pulses (high +low) then AOS[1:0] = 11.

In Group 3, 50ms duration:

- if we have 1.5 pulse then AOS[3:2] = 00.
- if we have 2.5 pulses then AOS[3:2] = 01.
- if we have 3.5 pulses then AOS[3:2] = 10.
- if we have 4.5 pulses then AOS[3:2] = 11.

where AOS is equivalent to Analog Output Stage.

See the *Analog Output Stage* register in the MTP section for more details of what each code corresponds to regarding analogue output functionality.

After the V_{DDHV} one-wire activation is complete, the V_{DDHV} one-wire protocol follows the DQ protocol but at 8x slower timing in both directions. So, the initialization sequence is the next step, with a reset pulse from the bus host and a presence pulse returned from the OUT pin. All read data will be present on the OUT pin.

To exit the PLC and activate the bi-directional communication on DQ, create a transition from high to low on the DQ line.

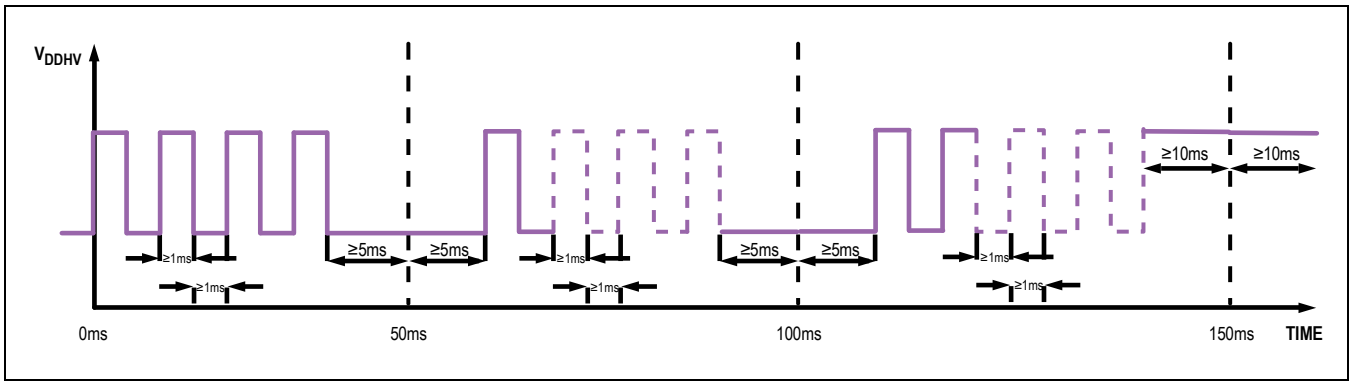


Figure 7. Power Line Communication Activation Timing

I²C-Compatible Bus Interface

A standard I²C-compatible 2-wire serial interface reads current/voltage data from the current and voltage registers and reads and writes control bits to and from the configuration registers. The DQ line must also be held high to enable I²C functions.

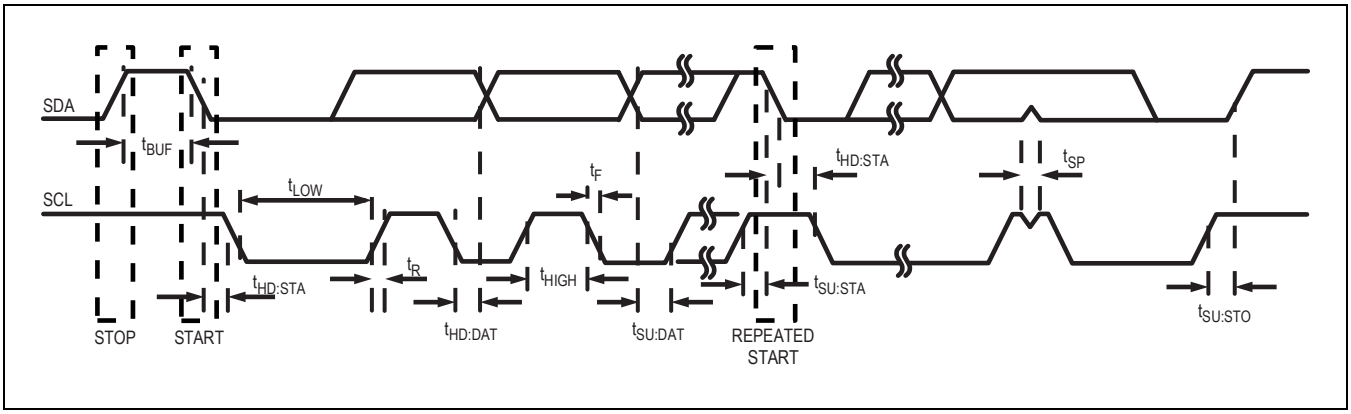


Figure 8. I²C Timing Diagram

Normal transactions consist of 2-byte writes and reads, however some registers are single byte read. Attempting longer transactions is not recommended. A transaction always begins with a START (S) condition followed by the client address and the Write/Read bit.

A 2-byte write transaction (Write Word) begins with the host generating a START condition and then transmitting the MAX40109's client address, followed by the Write bit. The MAX40109 acknowledges with an ACK (A) bit, and the host transmits the target register, followed by another ACK from the MAX40109. The host then writes the two data bytes, and the MAX40109 ACKs each. The host ends the transaction by generating a STOP (P) condition. Writing more bytes (not recommended) will overwrite the register (e.g., DATA HIGH - DATA LOW - DATA HIGH - DATA LOW for a 4-byte write).

DIRECTION	H→C	H→C	H→C	C→H	H→C	C→H	H→C	C→H	H→C	C→H	H→C
BITS	1	7	1	1	8	1	8	1	8	1	1
CONTENT	S	CLIENT ADDRESS	WR	A	REGISTER SELECT	A	DATA HIGH	A	DATA LOW	A	P

Figure 9. 2-Byte Write (Write Word)

A 2-byte read (Read Word) is more complex than a write. After transmitting the register byte and receiving an ACK from the MAX40109, the host generates a REPEAT START (Sr) and writes the address and a Read bit. The MAX40109 then ACKs the address/read byte and transmits the two data bytes. The host ACKs the first and NACKs the second, signaling that the transaction is complete, and generating the STOP condition.

DIRECTION	H→C	H→C	H→C	C→H	H→C	C→H
BITS	1	7	1	1	8	1
CONTENT	S	CLIENT ADDRESS	WR	A	REGISTER SELECT	A

•••

H→C	H→C	H→C	C→H	C→H	H→C	C→H	H→C	H→C
1	7	1	1	8	1	8	1	1
Sr	CLIENT ADDRESS	RD	A	DATA HIGH	A	DATA LOW	N	P

Figure 10. 2-Byte Read (Read Word)

A one-byte read is similar to the Read Word above, but only one byte is read; see *Figure 11*.

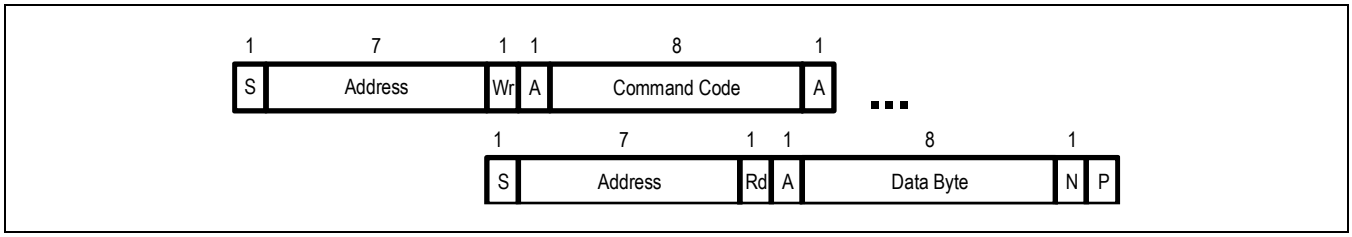


Figure 11. One-Byte Read

1-Wire Bus System

The 1-Wire bus system uses a single bus host to control one or more client devices. The MAX40109 is always a client. When there is only one client on the bus, the system is called as a single-drop system; the system is multidrop if there are multiple clients on the bus. All data and commands are transmitted the least significant bit first over the 1-Wire bus.

The following discussion of the 1-Wire bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing).

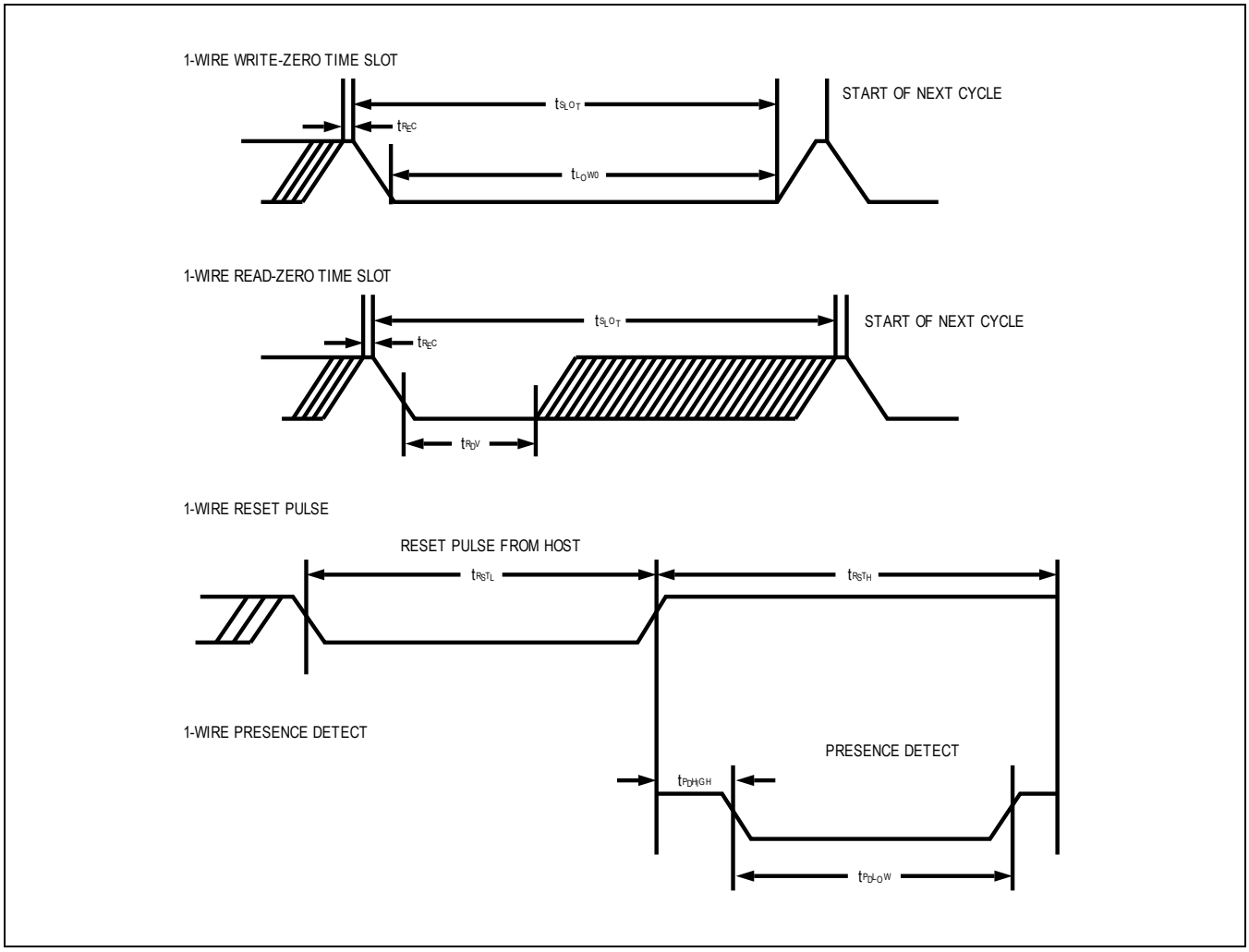


Figure 12. 1-Wire Bus Timing Diagram

64-Bit ROM Code

Each 1-Wire component contains a unique 64-bit code stored in ROM (*Figure 13*). The least significant 8 bits of the ROM code have the sensor's 1-Wire family code, 76h. The following 48 bits contain a unique serial number. The most significant 8 bits contain a cyclic redundancy check (CRC) byte that is calculated from the first 56 bits of the ROM code. See CRC Generation for a detailed explanation of the CRC bits. The 64-bit ROM code and associated ROM function control logic allow the device to operate as a 1-Wire device using the protocol detailed in the 1-Wire Bus System.

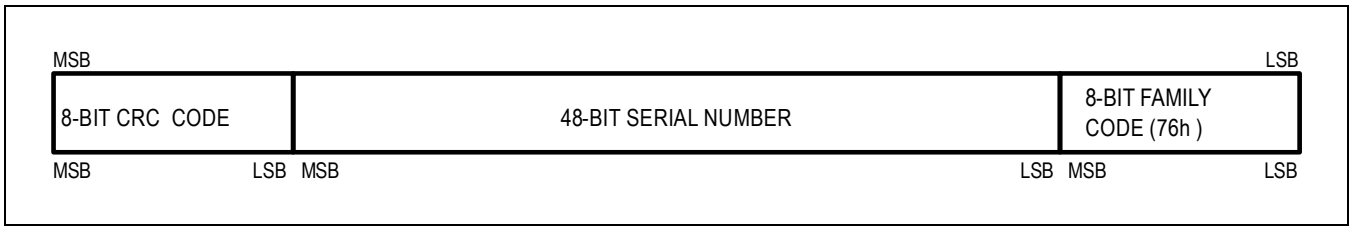


Figure 13. 64-bit ROM Code

CRC Generation

CRC bytes are provided as part of the device's 64-bit ROM code. The ROM code CRC is calculated from the first 56 bits of the ROM code and is contained in the most significant byte of the ROM. The CRC provides the bus host with a method of data validation when data is read from the device. To verify that data has been read correctly, the bus host must recalculate the CRC from the received data and then compare this value to either the ROM code CRC (for ROM reads). If the calculated CRC matches the read CRC, the data has been received error-free. The comparison of CRC values and the decision to continue with an operation are determined entirely by the bus host. No circuitry inside the device prevents a command sequence from proceeding if the CRC (ROM or scratchpad) does not match the value generated by the bus host.

The equivalent polynomial function of the CRC (ROM) is:

$$CRC = X^8 + X^5 + X^4 + 1$$

The bus host can recalculate the CRC and compare it to the CRC values from the device using the polynomial generator, as shown in *Figure 14*. This circuit consists of a shift register and XOR gates, and the shift register bits are initialized to 0. Starting with the least significant bit of the ROM code, one bit at a time should shifted into the shift register. After shifting in the 56th bit from the ROM, the polynomial generator contains the recalculated CRC. Next, the device's 8-bit ROM code must be shifted into the circuit. At this point, if the recalculated CRC was correct, the shift register contains all zeros. Additional information about the Maxim 1-Wire CRC is available in Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim iButton® Products.

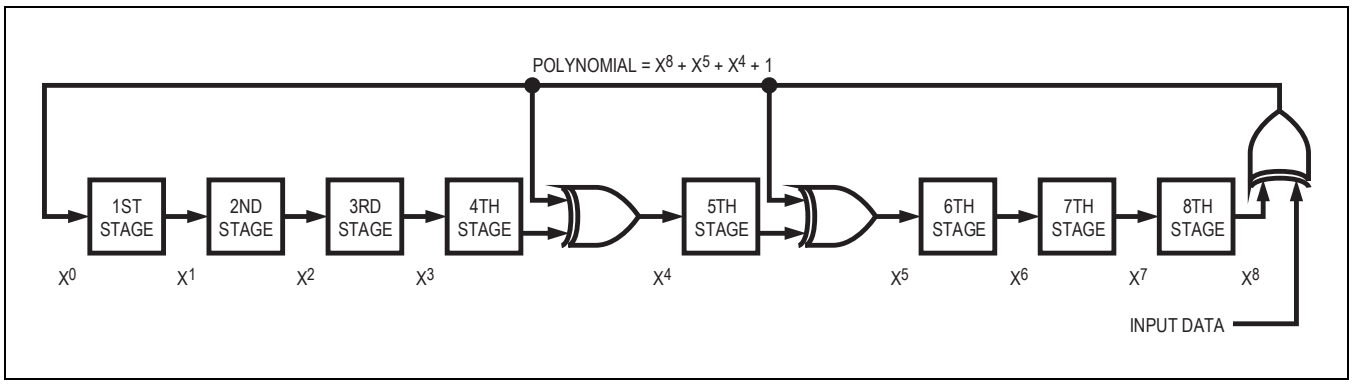


Figure 14. CRC Polynomial Generator

Hardware Configuration

The MAX40109 supports two hardware options using asynchronous serial data interfaces.

These options are one-time programmed at the factory.

1. 1-Wire serial data has an independent input/output pin (DQ).

2. Serial data input is shared with V_{DDHV}, and serial data output is shared with the analog voltage output (OUT).

The 1-Wire bus has, by definition, only a single data line. Each device (host or client) interfaces to the data line using an open-drain or three-state port. This allows each device to “release” the data line when the device is not transmitting data, making the bus available for use by another device. The device’s 1-Wire port (DQ) is an open drain with an internal circuit equivalent to that shown in [[Hardware Configuration]].

The 1-Wire bus requires an external pullup resistor of approximately 5kΩ; thus, the idle state for the 1-Wire bus is high. If, for any reason, a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. Infinite recovery time can occur between bits so long as the 1-Wire bus is in the inactive (high) state during the recovery period. If the bus is held low for more than 480µs, all components on the bus are reset.

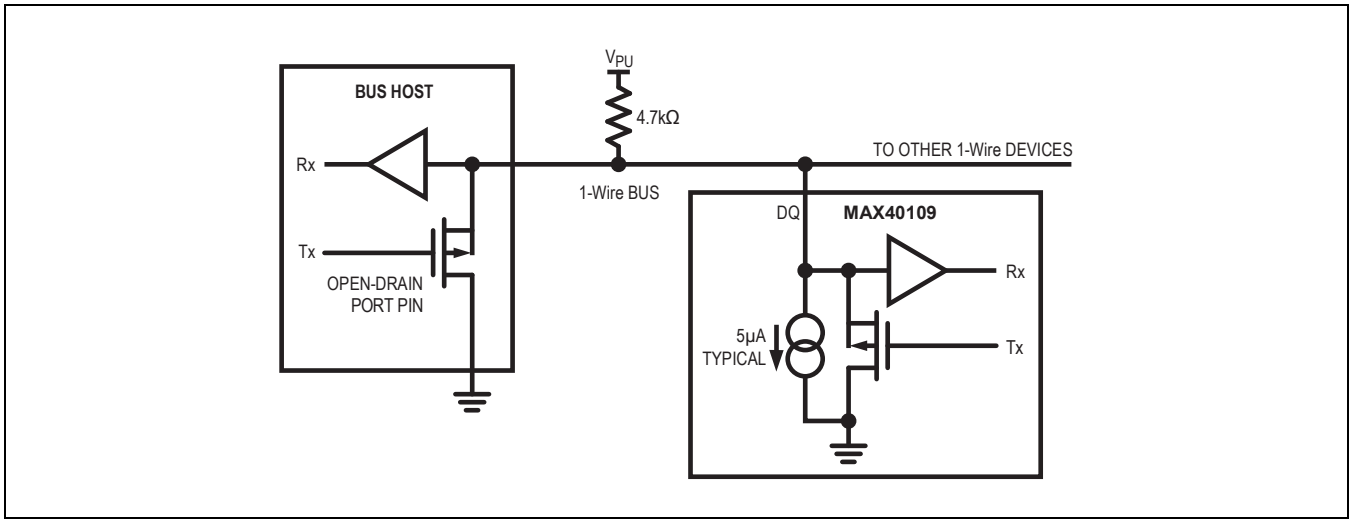


Figure 15. 1-Wire Hardware Configuration

Transaction Sequence

The transaction sequence for accessing the device is as follows:

Step 1: Initialization.

Step 2: ROM Command (followed by any required data exchange).

Step 3: Function Command (followed by any required data exchange).

It is very important to follow this sequence every time the MAX40109 is accessed, as the MAX40109 only responds if any steps in the sequence are in order. An exception to this rule is the Search ROM command. After issuing this ROM command, the host must return to step 1 in the sequence.

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus host followed by a presence pulse(s) transmitted by the client(s). The presence pulse lets the bus host know that client devices (MAX40109) are on the bus and are ready to operate. Timing for the reset and presence pulses is detailed in *1-Wire Signaling* section.

ROM Commands

After the bus host has detected a presence pulse, it can issue a ROM command. These commands operate on the unique 64-bit ROM codes of each client device and allow the host to single out a specific device if many are present on the 1-Wire bus. These commands also allow the host to determine how many and what types of devices are present on the bus. There are four ROM commands, and each command is 8 bits long. The host device must issue an appropriate ROM command before issuing a MAX40109 function command. An exception to the rule is when the detect address is used to

communicate with devices. ROM commands are not used when selecting an address to communicate. [[MAX40109 ROMs Command Flowchart]] shows a flowchart for the operation of the ROM commands.

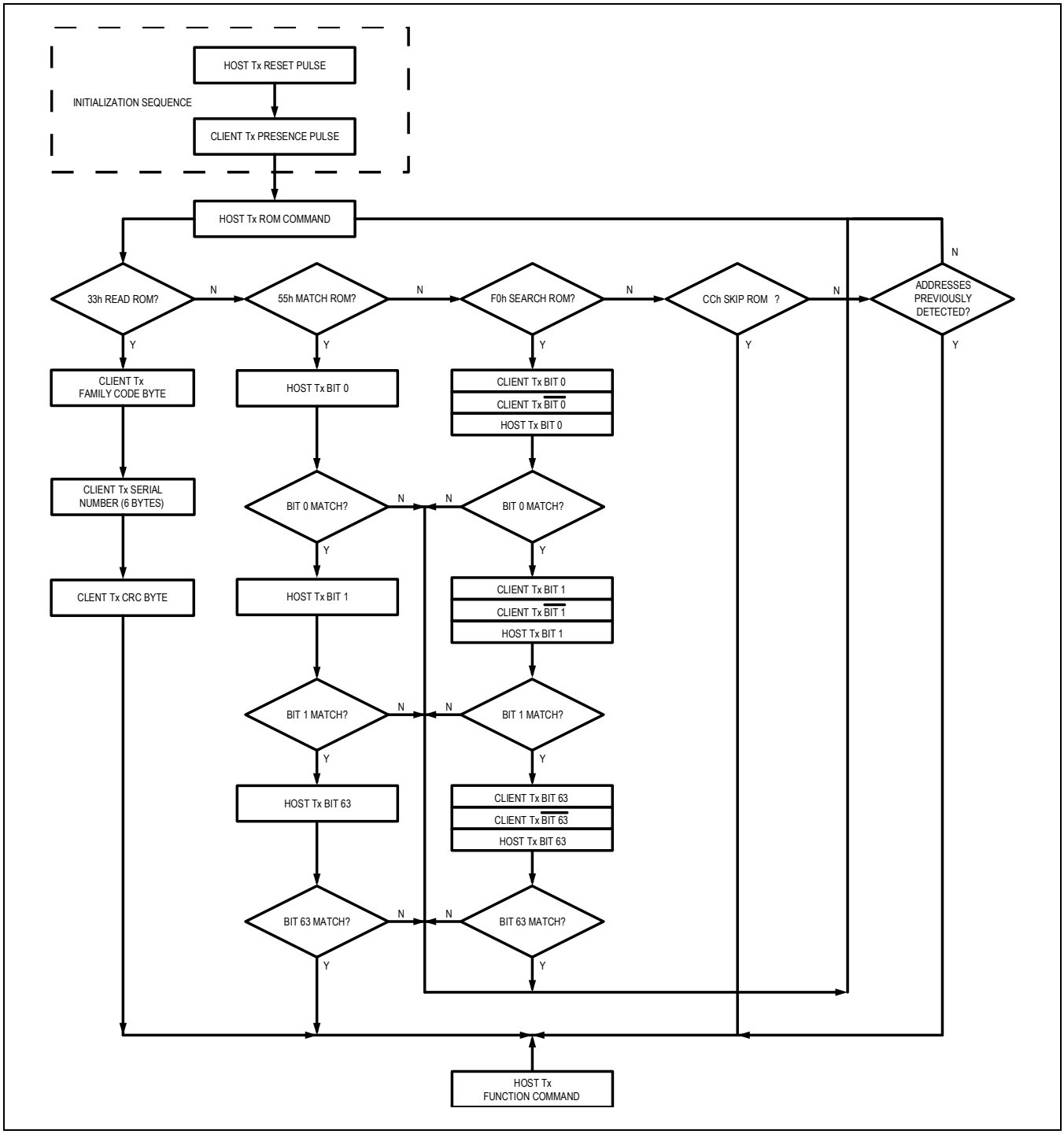


Figure 16. MAX40109 ROMs Command Flowchart

Search ROM [F0h]

When a system is initially powered up, the host must identify the ROM codes of all client devices on the bus, which allows the host to determine the number of clients and their device types. The host learns the ROM codes through a process of

elimination that requires the host to perform a Search ROM cycle (i.e., Search ROM command followed by data exchange) as many times as necessary to identify all the client devices. If there is only one client on the bus, the simpler Read ROM command can be used in place of the Search ROM process. For a detailed explanation of the Search ROM command procedure, refer to Application Note 937: Book of iButton® Standards. After every Search ROM cycle, the bus host must return to step 1 (initialization) in the transaction sequence.

Read ROM [33h]

This command can be used only when one client on the bus. The bus host can read the client's 64-bit ROM code without using the Search ROM command procedure. If this command is used when there is more than one client present on the bus, a data collision occurs when all the clients attempt to respond at the same time.

Match ROM [55h]

The Match ROM command, followed by a 64-bit ROM code sequence, allows the bus host to address a specific client device on a multidrop or single-drop bus. Only the client that exactly matches the 64-bit ROM code sequence responds to the function command issued by the host; all other clients on the bus wait for a reset pulse.

Skip ROM[CCh]

The host can use this command to address all devices on the bus simultaneously without sending out any ROM code information.

Note that the Read Scratchpad command can follow the Skip ROM command only if there is a single client device on the bus. In this case, time is saved by allowing the host to read from the client without sending the device's 64-bit ROM code. A Skip ROM command followed by a Read Scratchpad command causes a data collision on the bus if there is more than one client because multiple devices attempt to transmit data simultaneously.

Function Command

After the bus host has used a ROM command to address the MAX40109 with which it wishes to communicate, the host can issue one of the MAX40109 function commands. These commands allow the host to write and read the device's MTP memories as well as write and read all the RAM registers. See the MTP Memory and Functions and Internal Registers (Volatile, RAM) sections for more details of all the MAX40109 functions.

Function Commands are used to access the registers mapped with the device. Here, function commands are used to access the MTP and RAM registers of the OZ98. The following commands can be used to access registers.

- Write Register (CCh)
- Read Register (33h)

Table 36. Command Format

Command (CCh)	Address (A)	Length (n)	Data (byte(A), byte(A+1), …., byte(A+(n-1)))

Command: Will indicate whether it is writing or read.

Address: Start address of the write/read operation.

Length: How many bytes of data need to be written (length = length + 1).

Data: Write/Read data.

Data Format

The data format for a Command Field (either ROM or Function Command) is shown in *Figure 17* and *Figure 18*.

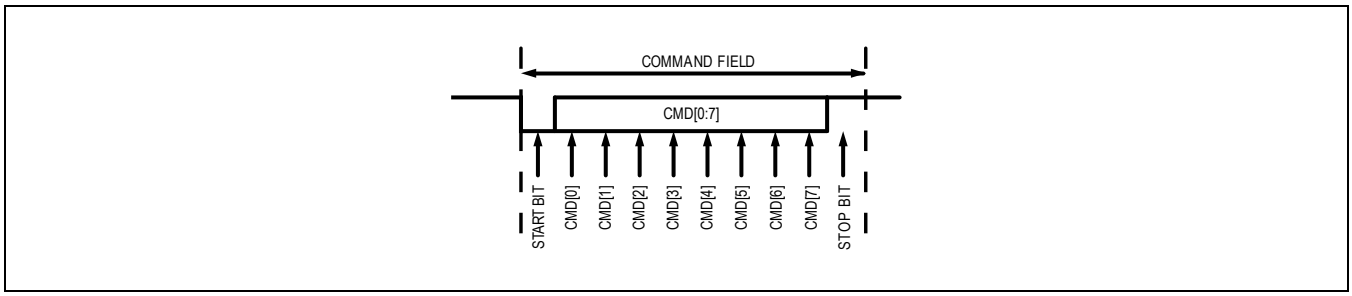


Figure 17. Command Field

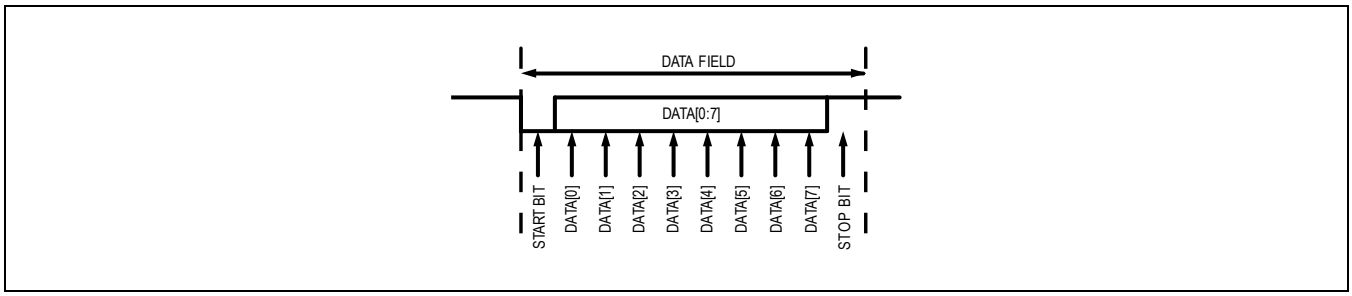


Figure 18. Data Field

1-Wire Signaling

Using a strict 1-Wire communication protocol helps to ensure data integrity. This protocol defines several signal types: reset pulse, presence pulse, write-zero, write-one, read-zero, and read-one. The bus host initiates all these signals except the presence pulse.

Initialization Procedure: Reset and Presence Pulses

All communication with the device begins with an initialization sequence that consists of a reset pulse from the host followed by a presence pulse from the device (illustrated in [[Initialization Timing]]). When the device sends the presence pulse in response to the reset, it indicates to the host that it is on the bus and ready to operate.

During the initialization sequence, the bus host transmits (Tx) the reset pulse by pulling the 1-Wire bus low for 480µs (min). The bus host then releases the bus and enters receive mode (Rx). When the bus is released, the pullup resistor pulls the 1-Wire bus high. When the device detects this rising edge, it waits for 15µs to 60µs and then transmits a presence pulse by pulling the 1-Wire bus low for 60µs to 240µs.

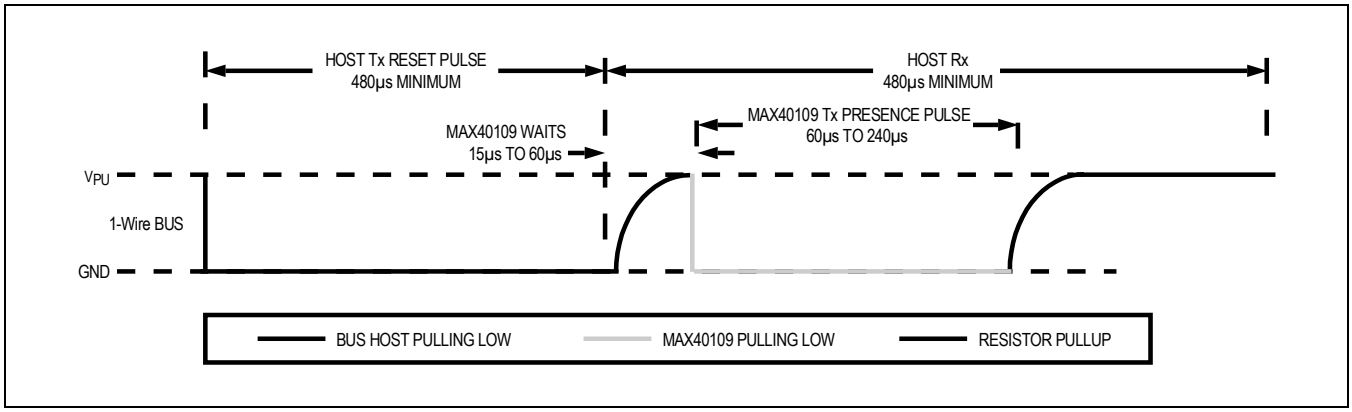


Figure 19. 1-Wire Initialization Timing

Read/ Write Time Slots

The bus host writes data to the device during write time slots and reads data from the device during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

Write Time Slots

There are two types of write time slots: write-one time slots and write-zero time slots. The bus host uses a write-one time slot to write a logic 1 to the device and a write-zero time slot to write a logic 0 to the device. All write time slots must have a 60µs (min) duration with a 1µs (min) recovery time between individual write slots. Both types of write time slots are initiated by the host pulling the 1-Wire bus low [[Read/Write Time Slot Timing Diagram]].

To generate a write-one time slot, after pulling the 1-Wire bus low, the bus host must release the 1-Wire bus within 15µs. When the bus is released, the pullup resistor pulls the bus high. To generate a write-zero time slot, after pulling the 1-Wire bus low, the bus host must continue to hold the bus low for the duration of the time slot (at least 60µs).

The device samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the host initiates the write time slot. If the bus is high during the sampling window, 1 is written to the device. If the line is low, a 0 is written to the device.

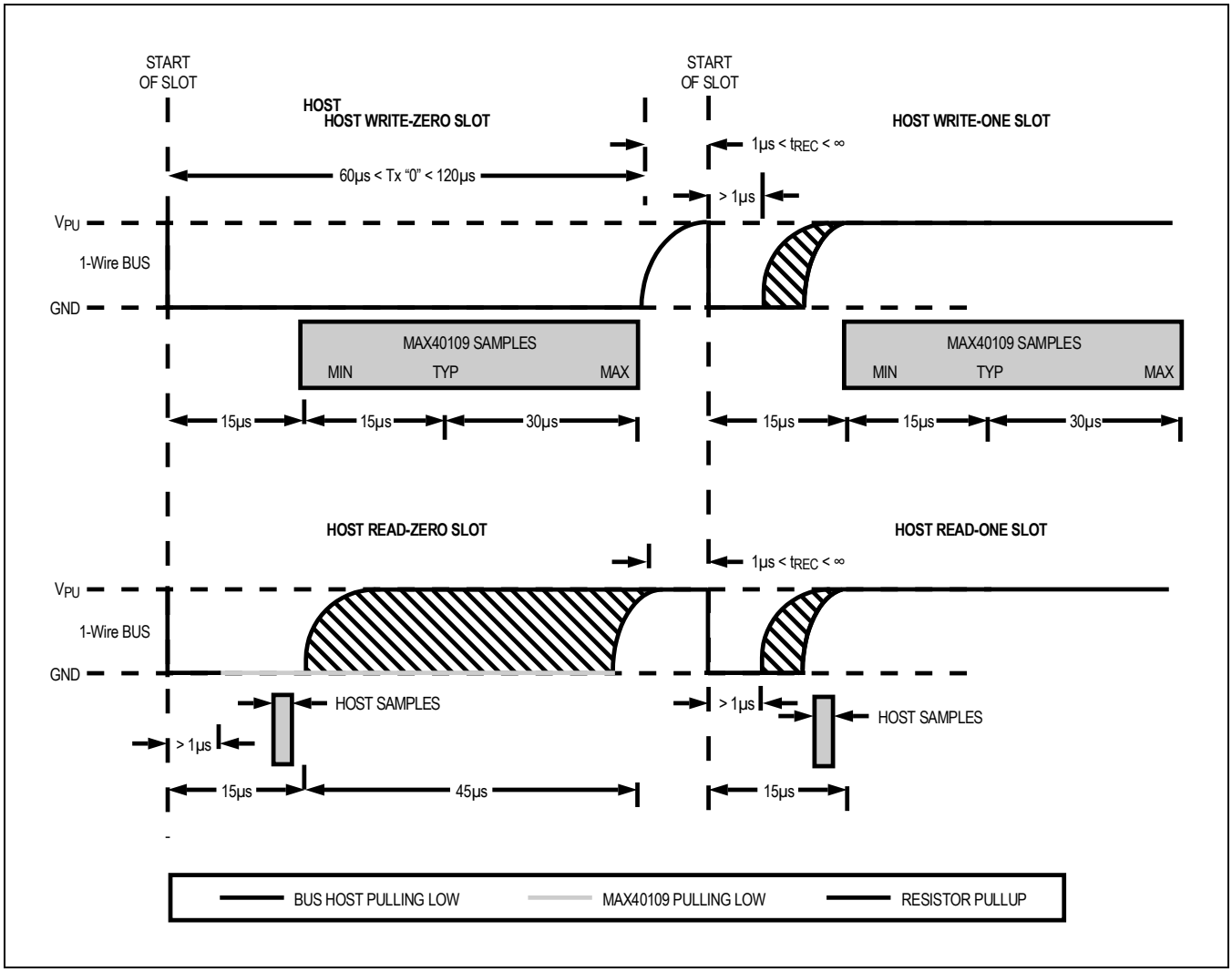


Figure 20. 1-Wire Read/Write Time Slot Timing Diagram

Read Time Slots

The device can only transmit data to the master when the master issues read time slots. Therefore, the master must generate read time slots immediately after issuing a Read Scratchpad command so that the device can provide the requested data.

All read time slots must be 60µs (min) in duration with a 1µs (min) recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs (t_{INIT}) and then releasing the bus ([[Read/Write Time Slot Timing Diagram]]). After the master initiates the read time slot, the device begins transmitting a 1 or 0 on the bus. The device transmits a 1 by leaving the bus high and transmits a 0 by pulling the bus low. When transmitting a 0, the device releases the bus by the end of the time slot, and the pullup resistor pulls the bus back to its high idle state. Output data from the device is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot. *Figure 21* illustrates that the sum of t_{INIT}, t_{RC}, and the master sample window must be less than 15µs for a read time slot. t_{RC} is the rise time due to the resistive and capacitive characteristics of the bus. *Figure 22* shows that the system timing margin is maximized by keeping t_{INIT} and t_{RC} as short as possible and by locating the master sample time during read time slots near the end of the 15µs period.

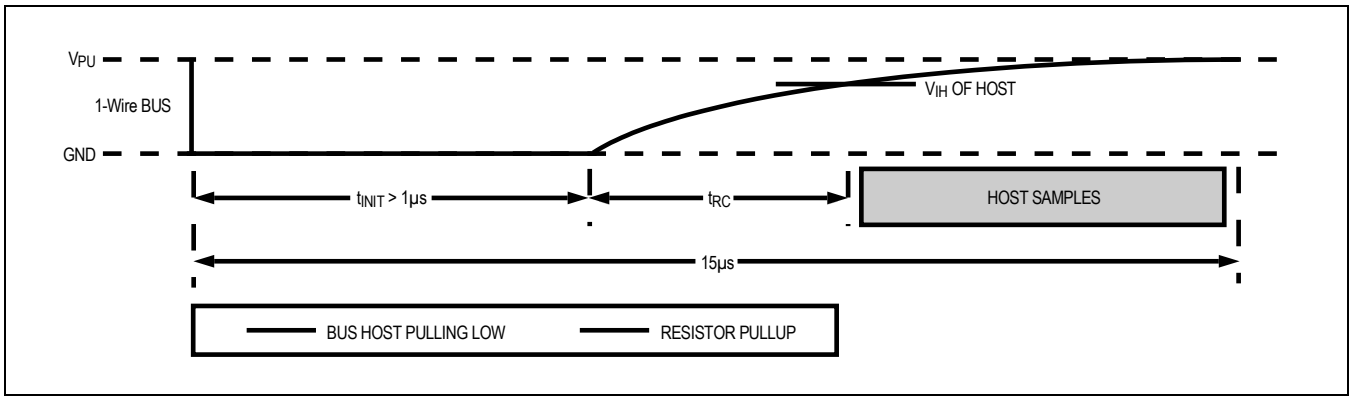


Figure 21. Detailed Master Read-One Timing

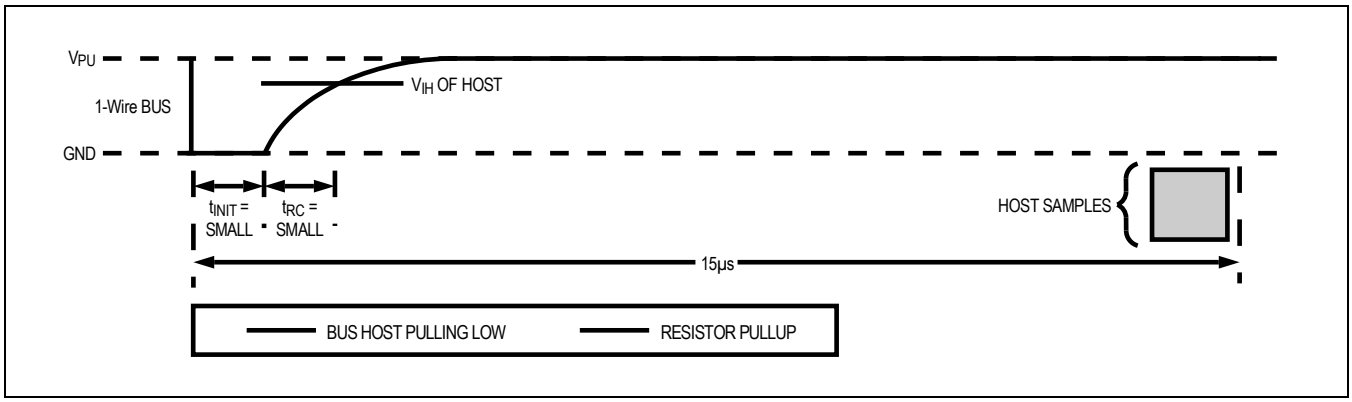


Figure 22. Recommended Master Read-One Timing

Applications Information

Temperature Measurement

The MAX40109 offers two modes to collect temperature measurements:

1. Directly from the bridge resistance. In this mode, the sensor bridge must be driven with current through the DRV output pin. The device measures the voltage directly at DRV. Temperature measurements from DRV (as voltage signals) are collected seamlessly from pressure measurements by automatically inserting a temperature measurement within two pressure measurements. The data rate ratio between pressure and temperature samples is determined in the register *ADC Sample Rate*.
2. By connecting a thermistor to the input INT.

See register *Temp Mode* for details on enabling each mode and the "Configuration" register for the driving current at the INT pin.

In addition, the temperature channel input amplifier may be configured as either single-ended or differential, as shown in *Figure 23*.

Table 37. Temperature Channel Input Configuration

INPUT PIN	CONFIGURATION	ADC	K1	K2	K6	K7	K8
INT	Single-ended with G = 1	SE	X			X	
	Single-ended with G > 1	SE	X			X	
	Differential-ended with DAC's offset	DE	X		X		X
DRV	Single-ended with G = 1	SE		X		X	
	Differential-ended with DAC's offset and G = 1	DE		X	X		X

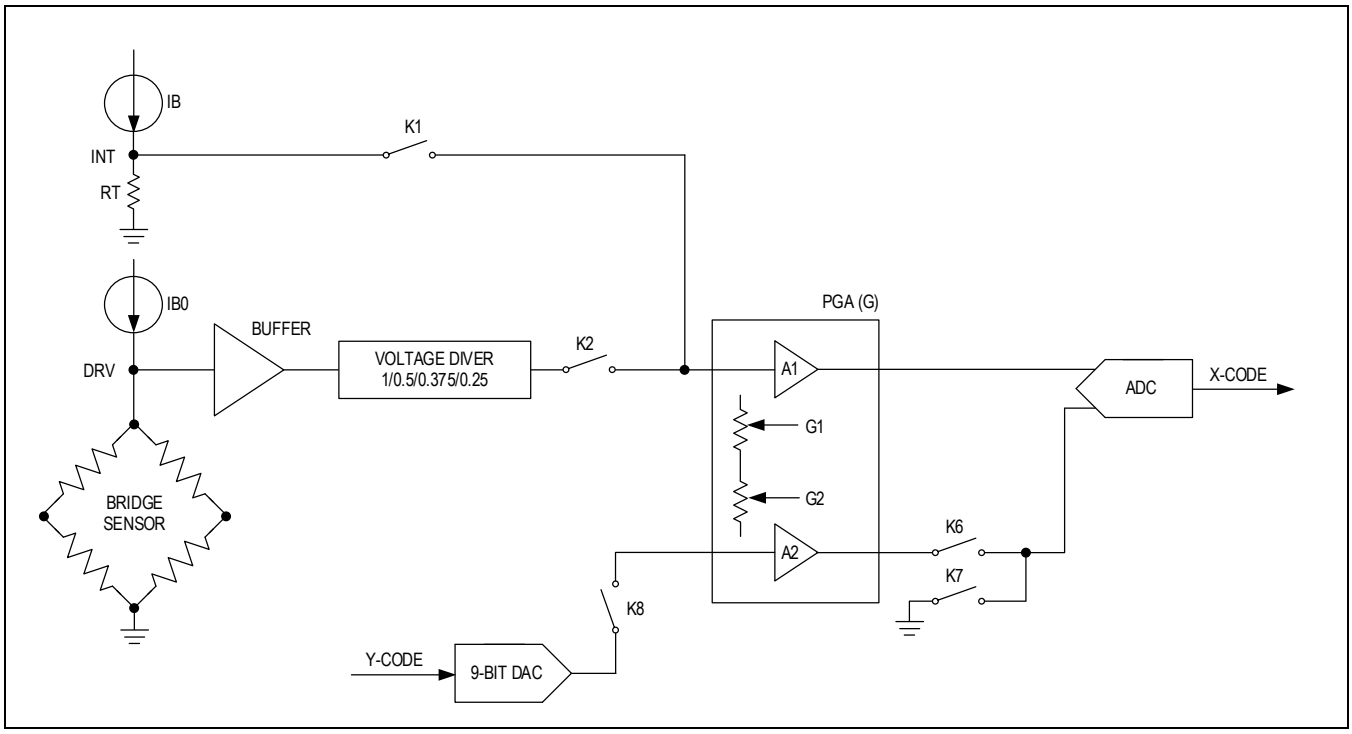


Figure 23. Temperature Circuit

Use External Resistor for Bridge Current Source

The MAX40109 can drive the sensor bridge with either voltage or current.

When driving with current, the current source is integrated into the device. The temperature coefficient of the current source is dominated by the temperature drift of the internal resistor, which is 50ppm/°C (typ).

The user may use an external resistor with a lower temperature coefficient, as shown in the following diagram. The external sense resistor (R_{EXT}) is connected to the input pin INT. **Its nominal value should be 100kΩ**. The internal resistor (R_{INT}) is 50kΩ nominally. In this case, it will not be possible to connect a thermistor to INT. However, the temperature measurement from the bridge resistor (through DRV) is still allowed.

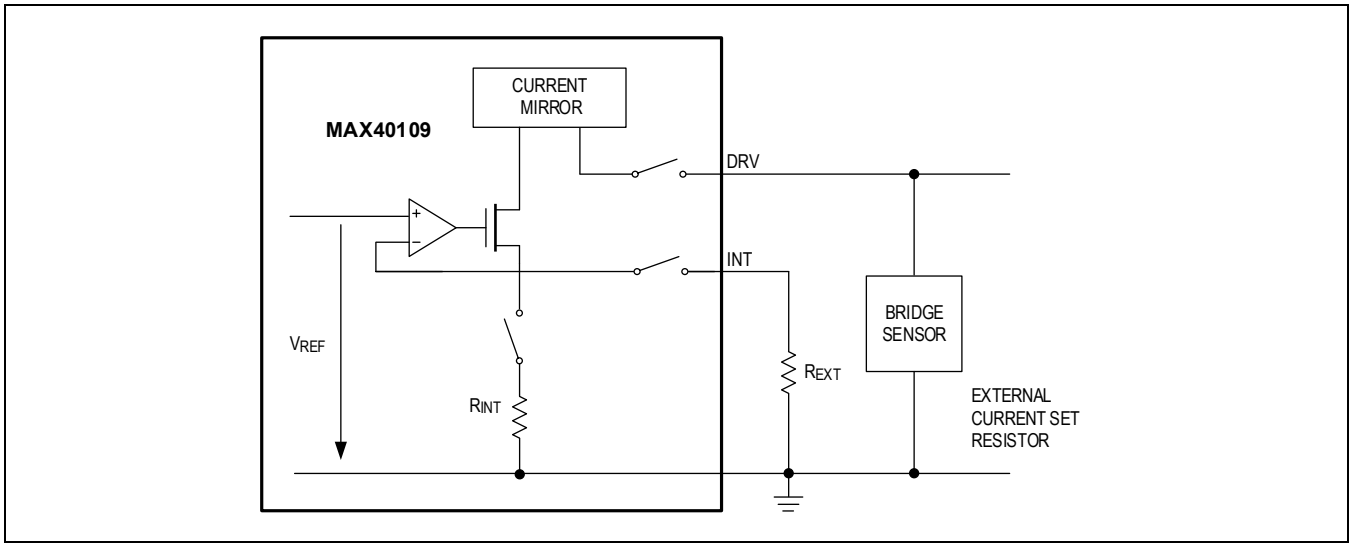


Figure 24. External Resistor for Current Bridge Source

Ratio-metric Voltage Output

To create a 0-5V voltage output that is ratio-metric with the supply voltage, the following step is required:

- Program the MTP memory register *Analog Output Stage* to select option 0x1.

It is possible to drop V_{DDHV} to a level below the internal LDO output voltage of V_{DD5V}. In this case, the internal LDO is in drop-out mode. See the *Electrical Characteristics* table for the drop-out voltage.

Sensor Offset Calibration

This section describes the procedure required to calibrate the sensor offset.

- User activates “pressure_cal_bypass” (configuration register, bit 13) to enter bridge offset calibration mode. Start at room temp.
- Bypass the pressure PGA gain (see register *Sensor Offset Cal Config*).
- User measures offset with a default setting of gain = 2V/V.
- If preferred, for more accuracy, the user can adjust gain such that the signal at the input of the ADC is within ½ ADC full-scale and ADC full-scale.
- User determines the correct offset calibration code.
- Highly recommended: If the user wants to check offset calibration code accuracy without writing to MTP, they can load trim code into a register “ZERO_PRESSURE_OFFSET<15:0>” and reconnect the internal trim resistor and the offset calibration current source to measure the residue (set bits 2 and 1 of Sensor Offset Cal Config).
- Adjust trim code to achieve acceptable residue. It is highly recommended to confirm residue with the final trim code.
- User deactivates “pressure_cal_bypass”
- Write trim code into MTP.

Using the MAX40109 to Perform Sensor Calibration

All the following calibration steps are performed through the 1-Wire interface. The first calibration step is to calibrate the external temperature sensor:

- Set the device into Temp Cal Bypass (through Configuration Register).
- Default temperature coefficients are already preset with $k_0 = 0$, $k_1 = 1$, $k_2 = 0$, and $k_3 = 0$. Set PGA gain, Bridge Drive, ADC sample rate, and sensor offset correction.
- Collect all required temperature measurements.
- User calculates the k_0—k_3 coefficient with own software/algorithm.
- User programs k_0—k_3 coefficients in the MTP memory. The second step is to calibrate the sensor bridge pressure measurement.
- Set the device into Pressure Cal Bypass (through Configuration Register).
- Measure the zero-pressure sensor offset.
- Correct the zero-pressure sensor offset using the MTP register "ZERO_PRESSURE_OFFSET".
- Set PGA gain, Bridge Drive, and ADC sample rate.
- Collect all required pressure measurements.
- User calculates the 16 coefficients h_x, g_x, m_x, and n_x with own software/algorithm.
- The user programs the 16 coefficients in the MTP memory. See the *Bridge Sensor Calibration* section for additional details.

Analog Output Stage

The analog output stage can provide either current output (4mA–20mA) or voltage output in many fashions, either with internal gain or external resistors to set a custom gain. See MTP register *Analog Output Stage* for more details. See *Typical Application Circuits* for examples.

The internal circuit at that output will vary depending on the analog output stage settings. R1 = 395kΩ and R2 = 379kΩ applies for all AOS, R3 = 279kΩ (AOS = 8) or 310kΩ (AOS = 9, A), R4 = 93kΩ (AOS = 8) or 62kΩ (AOS = 9, A). Resistors R1, R2, R3, and R4 are properly matched to achieve a typical drift of 25ppm/°C (Typ).

The external resistor in a 4-20mA output configuration (*Figure 25*) would have a typical R_{OUT} = 1kΩ and R_{SENSE} = 49.9Ω. Resistor R_E enhances the circuit stability and its value is transistor dependent.

For ratio-metric analog output voltage with external gain resistors (*Figure 26*) the gain will be 1 + R_{1EXT}/R_{2EXT}.

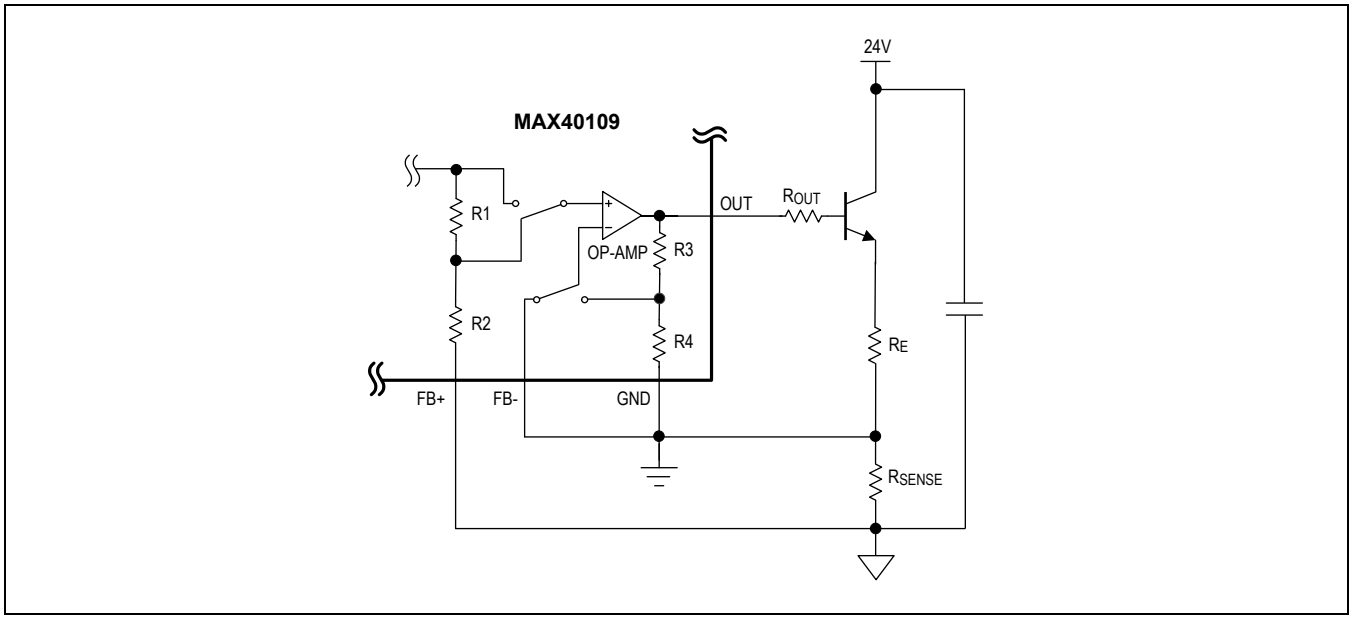


Figure 25. 4mA-20mA Output Setting

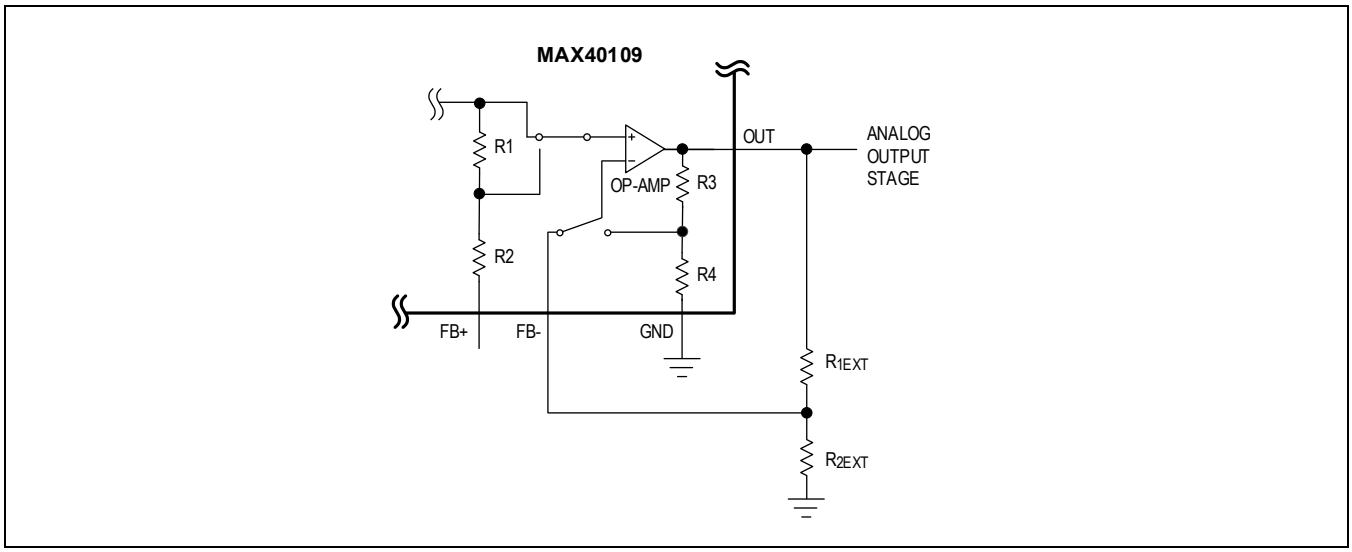


Figure 26. Ratio-Metric Voltage Output with External Resistors Setting

Layout Recommendations

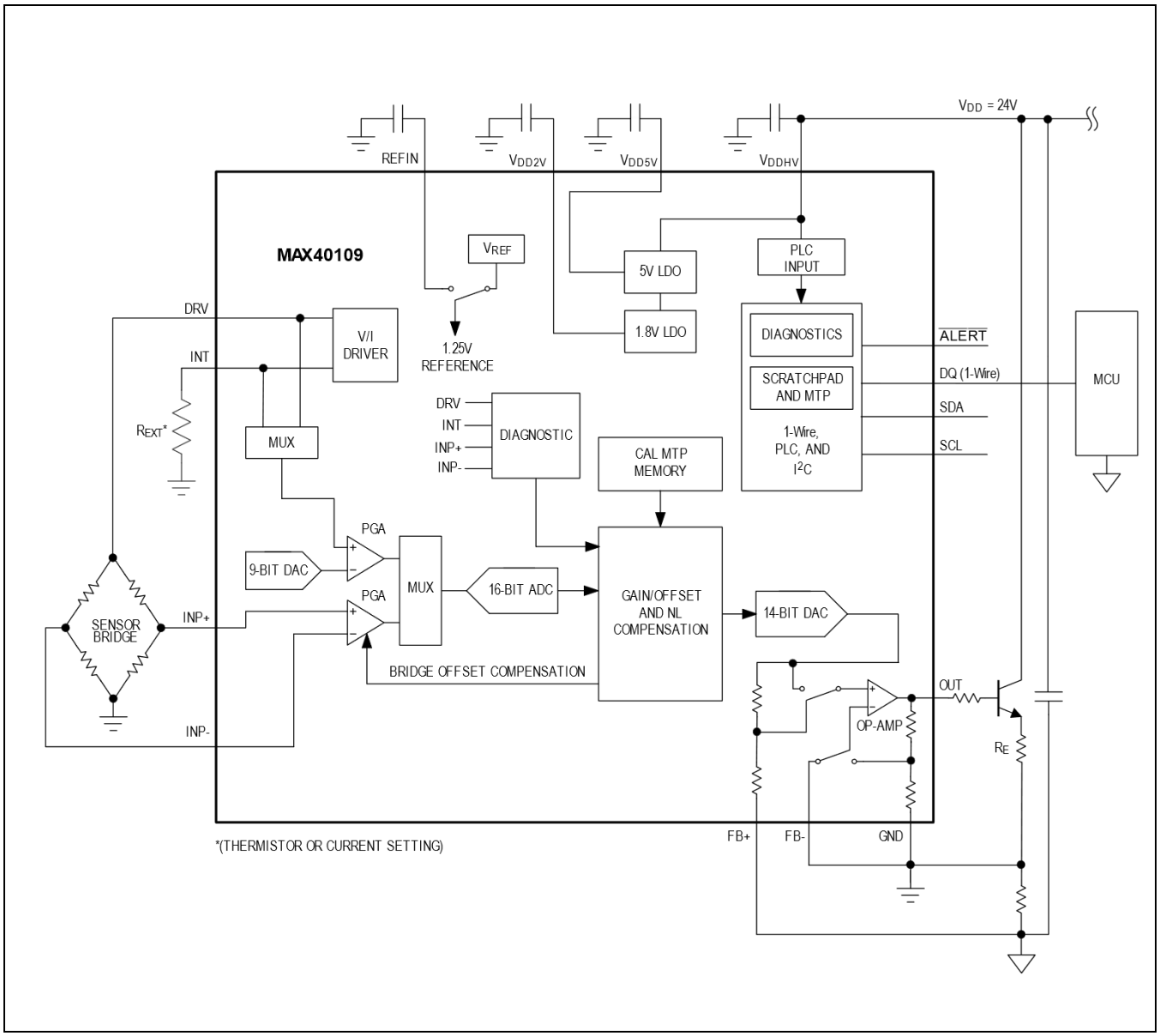
Some critical layout guidelines are as follows.

- Place bypass capacitors near supply and reference pins (V_{DDHV}, V_{DD5V}, V_{DD2V}, REFIN).
- Use PCB with ground planes when possible. Avoid crossing analog and digital signals.
- Connect the EP to the analog ground.
- Create a star connection between AGND and DGND (TQFN package only).

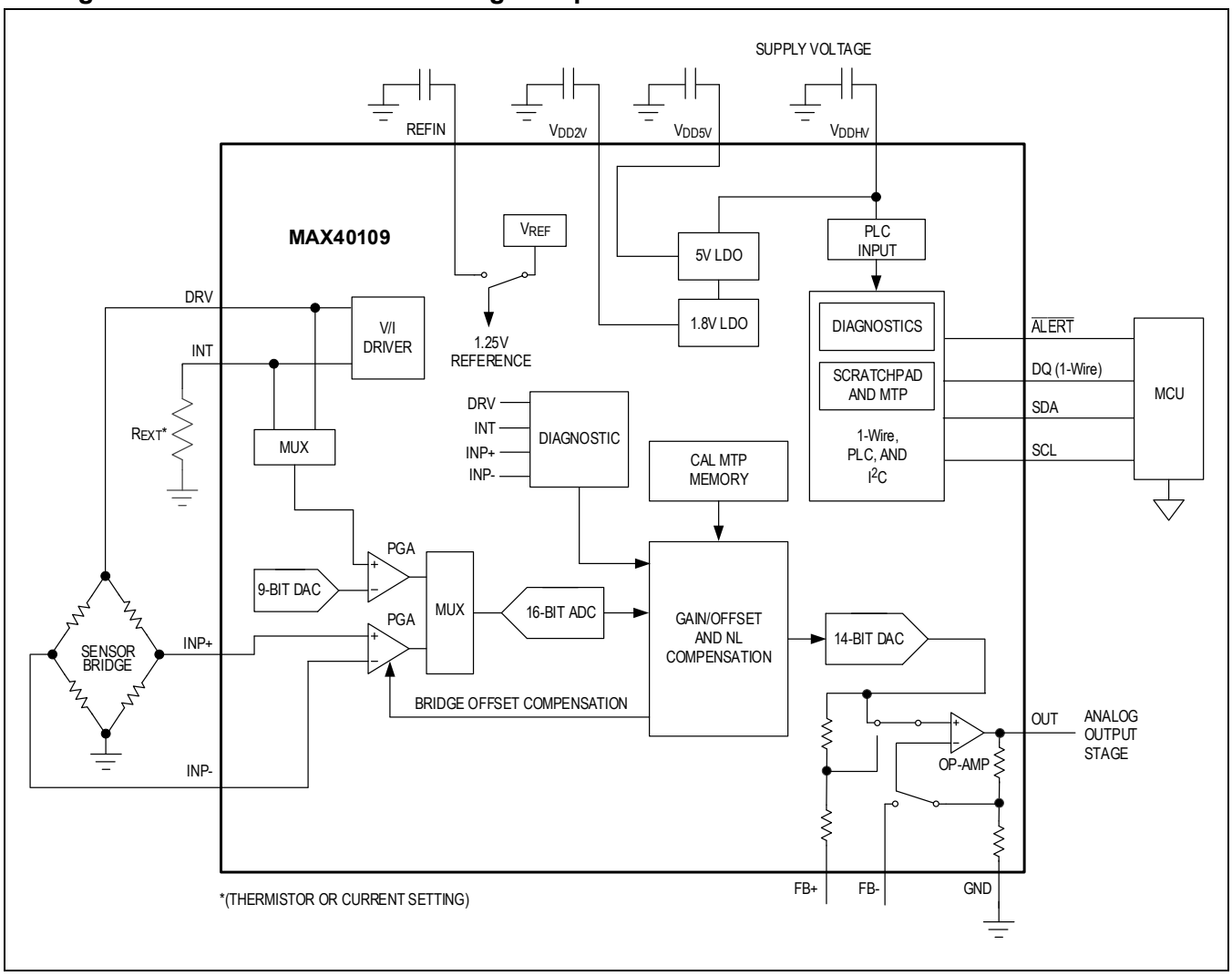
Typical Application Circuits

Analog Sensor with 4mA–20mA Output and 1-Wire Communication through DQ

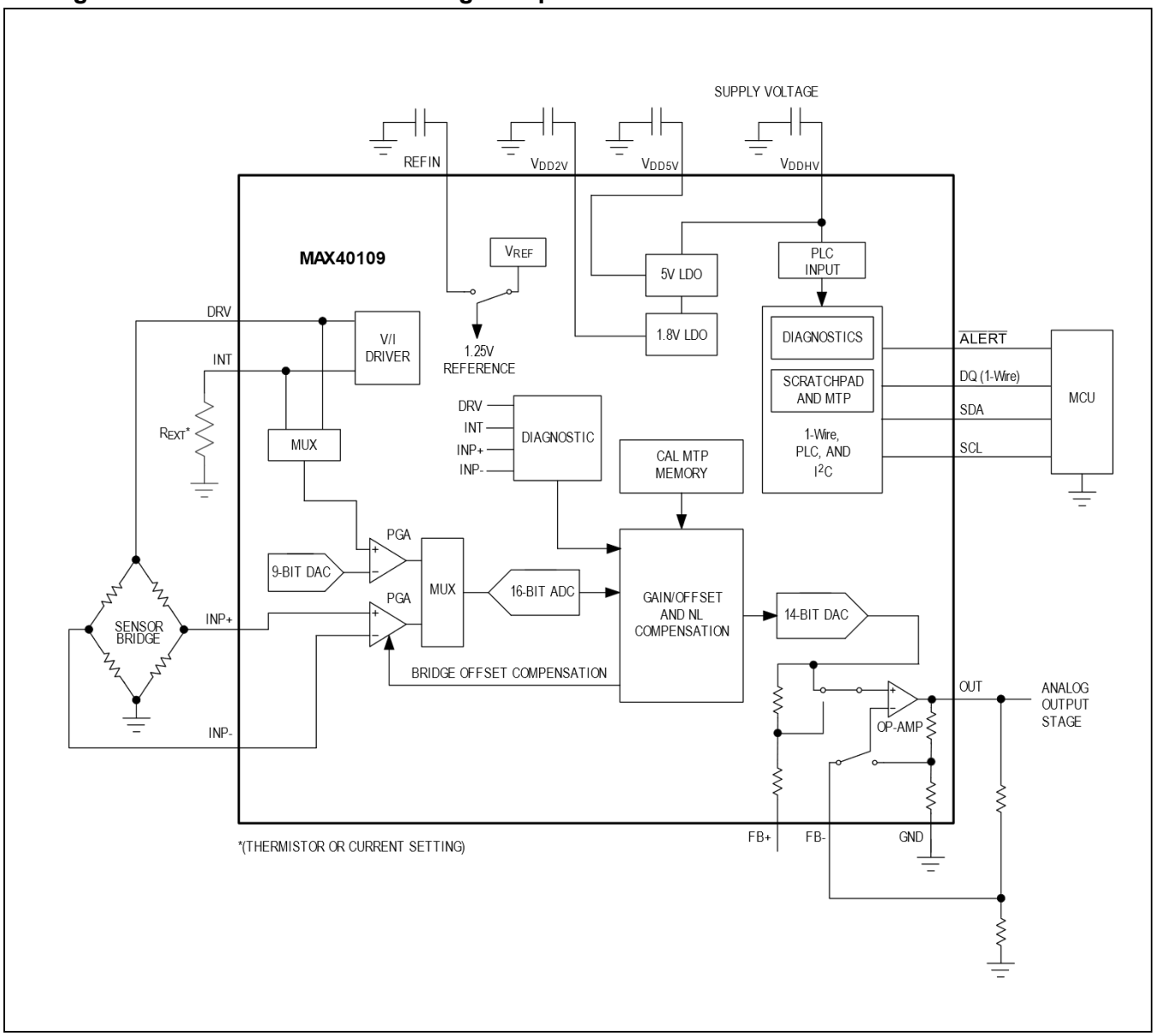
Resistor R_E enhances the circuit stability and its value is transistor dependent.



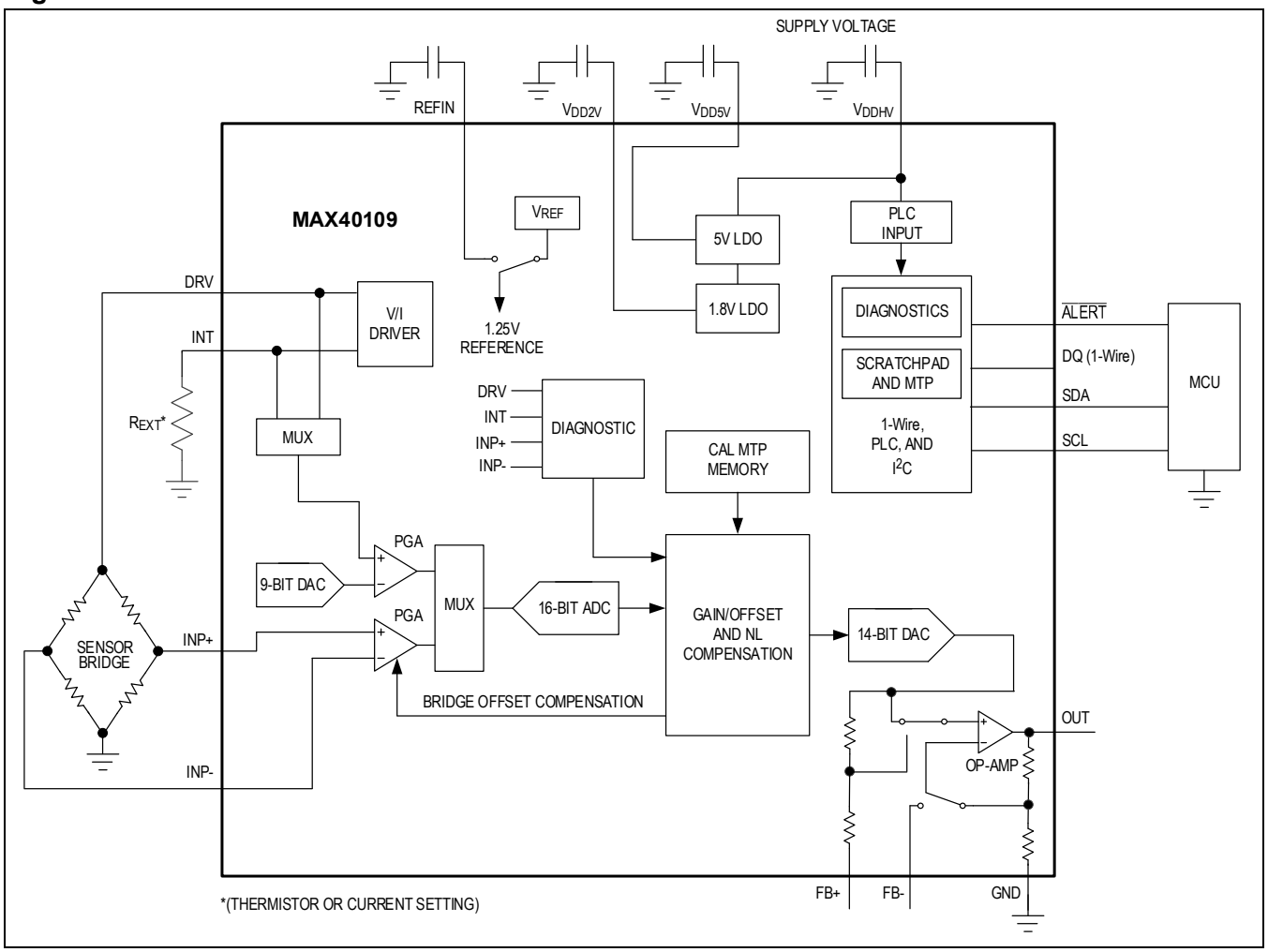
Analog Sensor with Ratio-metric Voltage Output



Analog Sensor with Ratio-metric Voltage Output and External Resistors to Set the Gain



Digital Sensor with I²C Interface



Ordering Information

PART NUMBER	PIN-PACKAGE	DIGITAL INTERFACES
MAX40109IATP+	20-TQFN	I²C, 1-Wire, and PLC
MAX40109IAWE+	16-WLP	I²C, 1-Wire, and PLC

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/23	Initial release	—
1	3/24	Updated Block Diagram and Typical Application Circuits	5, 55–58
2	7/24	Added WLP package in the General Description, Benefits and Features, Package Information, Pin Configuration, Pin Description, and Ordering Information sections	1, 4, 16, 17, 56
3	4/25	Updated Simplified Block Diagram, Electrical Characteristics table, Pin Description table, Table 3 title, Zero Pressure Offset RAM Override section, Table 24, Table 27, Figure 3, Figure 6, Analog Output Stage section, Figure 25, and Typical Application Circuits section	5, 10, 12, 18, 21, 29, 31, 34–36, 40, 55, 57

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