3V to 80V, 7A, Current-Limiter with OV/Surge, UV, Reverse Polarity, Loss of Ground Protection and PMBus Interface

MAX17616/MAX17616A

Product Highlights

- Robust Protection Reduces System Downtime
  - Wide Input Supply Range: +3V to +80V (without Reverse Current Protection)
  - Wide Input Supply Range: +3V to +75V (with Reverse Current Protection)
  - ±3% Accurate Programmable Current Limit between 3A to 7A across Full Temperature Range
  - ±4% Accurate Programmable Current Limit between 2A to 3A across Full Temperature Range
  - ±7% Accurate Programmable Current Limit between 0.7A to 2A across Full Temperature Range
  - Input-Voltage Reverse-Polarity Protection (with External nFET)
  - Dual Stage Reverse Current Protection (with External nFET) with Fast 100ns Response Time
  - Low R_{ON} Internal nFET (20mΩ typ)
  - Output-Voltage Reverse-Polarity Tolerant
  - Loss of Ground Protection
  - 200% Short Term Overload capability
  - Programmable Overvoltage Surge Protection (MAX17616A)
- PMBus Interface
  - Real Time Operating Conditions Monitoring, Voltage and Current Readout
  - Fault Registry Access and Management
  - Device ON/OFF Control
  - Current Limit Mode Selection
  - Startup Inrush Current Limit Selection
  - Short Term Over Current Limit and Time Selection
- Flexible Design to Maximize Reuse and Minimize Requalification
  - Adjustable UVLO and OVLO/OVFB Thresholds
  - ±2% Accurate Bandwidth Current Monitoring Read-Out, IMON (3A to 7A, up to +85ºC)
  - Programmable Startup Inrush Current Limit
  - Programmable Current Limit Fault Response: Continuous, Autoretry, and Latch-off Modes
  - Logic Level Enable Input (EN)
  - Protected External n-type field effect transistor (nFET) Gate Drive
  - Power Good Output (PGOOD)
  - Programmable Output Under Voltage Sense (OUTUV)
  - Junction Temperature Monitoring (T_J)
  - Thermal Foldback Current Limit
- Reduced Solution Footprint
  - 4.5mm x 5.75mm, 23-Pin FCQFN package
  - Integrated nFET for Common-Use Protection Requirements

Key Applications

- Input Voltage and Output Overcurrent Protections:

The MAX17616/MAX17616A interrupts load current and disconnects the output from the input in input voltage faults and output overcurrent faults.

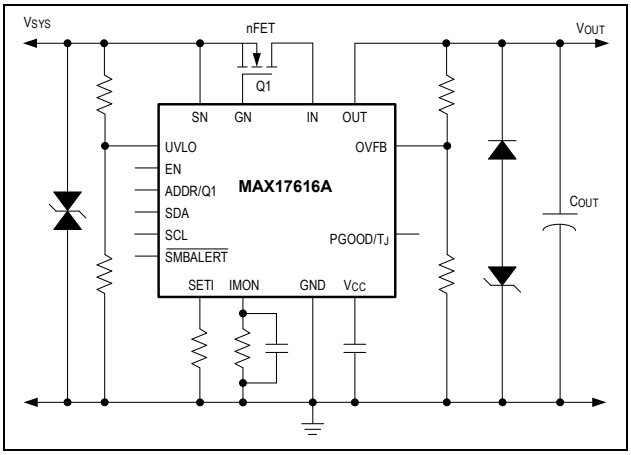
- Loss of Ground Protection:

The MAX17616/MAX17616A interrupts load current and disconnects the output from the input in a Loss of Ground event, such as when the single-fault safety fuse on its ground path opens up.

- Surge Protection:

The MAX17616A features an output voltage limiting regulation during transient surges in input voltage to protect connected loads from short-duration input voltage surge events.

Simplified Application Diagram



Ordering Information ***appears at end of data sheet***

19-101929; Rev 0; 10/24

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Absolute Maximum Ratings

IN to GND ..... -0.3V to +85V

SN to GND (Reverse Current Protection is used) ..... -85V to +78V

SN to GND (Reverse Current Protection is not used) ..... -85V to +85V

OUT to GND ..... -85V to +85V

IN to OUT (DC) ..... -0.3V to +85V

UVLO, OVLO, OVFB, $\overline{\text{SMBALERT}}$ to GND ..... -0.3V to +33V

EN, PGOOD/T_J, SDA, SCL, ADDR to GND ..... -0.3V to +6V

V_{CC} to GND ..... -0.3V to +2V

SETI, IMON to GND ..... -0.3V to (V_{CC} + 0.3)V

GN to SN ..... -0.3V to +10V

GN to GND ..... -85V to +85V

IN to SN ..... -1V to +85V

IN Current (DC) 8A

Continuous Power Dissipation (T_A = +70°C, derate at 36.5mW/°C above +70°C) 3469.7mW

Operating Temperature Range ..... -40°C to +125°C

Junction Temperature ((Note 1)) ..... -40°C to +150°C

Storage Temperature ..... -65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... +300°C

Soldering Temperature (Reflow) ..... +260°C

Note 1: Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

Package Code	F234A5F+1F
Outline Number	*21-100606*
Land Pattern Number	*90-100213*
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	27.38°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	1.81°C/W

For the latest package outline information and land patterns (footprints), go to *https://www.analog.com/en/design-center/packaging-quality-symbols-footprints/package-index.html*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html*.

Electrical Characteristics

(V_{IN} = V_{SN} = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON = OPEN, PGOOD/T_J, $\overline{SMBALERT}$, SDA, SCL, ADDR = GND, R_{SETI} = 2.13kΩ, V_{CC} = 2.2µF to GND, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are V_{IN} = 48V, T_A = +25°C (See *Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Section						
IN Voltage Range	V_{IN}	Without Reverse Current Protection	3		80	V
		With Reverse Current Protection	3		75	
Shutdown IN Current	I_{INSHDN}	V_{EN} = 0V, V_{OUT} = GND, T_A = +125°C		20	80	µA
		V_{EN} = 0V, V_{OUT} = GND, T_A = +85°C		20	50	µA
Shutdown SN Current		V_{EN} = 0V, V_{SN} = -80V		-53	-105	µA
Shutdown IN to OUT Current		V_{EN} = 0V, V_{IN} – V_{OUT} = 80V		30	110	µA
Shutdown IN, GN, SN shorted		V_{EN} = 0V, V_{OUT} = GND, T_A = +125°C		30	90	µA
		V_{EN} = 0V, V_{OUT} = GND, T_A = +85°C		30	60	µA
Supply Current	I_{IN}			2	3	mA
Internal IN Undervoltage Trip level	$V_{INUVLOR}$	V_{IN} Rising	2.74	2.80	2.86	V
	$V_{INUVLOF}$	V_{IN} Falling	2.64	2.70	2.76	
Enable (EN)						
EN Input-Logic High	V_{ENH}		1.4			V
EN Input-Logic Low	V_{ENL}				0.4	V
EN Internal Pullup Voltage		3V < V_{IN} < 80V	1.3		2.05	V
EN Input Current		V_{EN} = 5V			20	µA
EN Pullup Current		V_{EN} = 0V	2.74	5	9.56	µA
V_{CC} (LDO)						
V_{CC} Output Voltage Range	V_{CC}	1mA < I_{VCC} < 10mA	1.7	1.8	1.86	V
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	1.62	1.66	1.7	V
	V_{CC_UVF}	V_{CC} falling	1.54	1.58	1.62	
V_{CC} current limit	I_{VCC}		15	29	48	mA
Undervoltage Lockout (UVLO)						
UVLO Threshold		UVLO Rising	0.911	0.93	0.948	V
		UVLO Falling	0.882	0.90	0.918	
UVLO Leakage Current	I_{UVLO_LEAK}	V_{UVLO} = 1V, T_A = +25°C	-100		+100	nA
Overvoltage Lockout (OVLO) (MAX17616 only)						
OVLO Threshold		OVLO Rising	0.911	0.93	0.948	V
		OVLO Falling	0.882	0.90	0.918	
OVLO Leakage Current	I_{OVLO_LEAK}	V_{OVLO} = 1V, T_A = +25°C	-100		+100	nA

(V_{IN} = V_{SN} = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON = OPEN, PGOOD/T_J, $\overline{SMBALERT}$, SDA, SCL, ADDR = GND, R_{SETI} = 2.13kΩ, V_{CC} = 2.2µF to GND, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are V_{IN} = 48V, T_A = +25°C (See *Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Overvoltage Clamp (OVFB) (MAX17616A only)							
Overvoltage Clamp Reference	$OVFB_{REF}$			0.784	0.800	0.816	V
Overshoot on OVFB		IN Slew Rate < 0.1V/µs	C_{LOAD} = 4.7µF, I_{LIM} = 7A, I_{LOAD} = 1A		0		mV
		IN Slew Rate < 1V/µs	C_{LOAD} = 4.7µF, I_{LIM} = 7A, I_{LOAD} = 1A		0		
Current Limit and Monitoring (SETI and IMON)							
Current Limit Adjustment Range	I_{LIM}			0.7		7.0	A
Current Limit Threshold Accuracy	I_{LIM_ACC}	0.7A < I_{LIM} < 2A		-7		+7	%
		2A ≤ I_{LIM} < 3A		-4		+4	
		3A ≤ I_{LIM} ≤ 7A		-3		+3	
Overcurrent Response Time	t_{SOC}	I_{LIM} = 1A, I_{OUT} step from 0.5A to 3A, Time to regulate I_{OUT} to Current Limit			20		µs
Short-Term Over Current Limit	I_{STLIM}				2 x I_{LIM}		A
Short-Term Over Current Limit Blanking Time	t_{STOC}				400		µs
Overcurrent Protection Threshold	I_{OCP}	(See *Figure 16* in the *Short Circuit Protection* Section)	(See *Note 3*)	22	30	36	A
Overcurrent Protection Response Time	t_{OCP}	I_{LIM} = 7A, I_{OUT} step from 3.5A to 40A, Time to turn off the switch once I_{OUT} > I_{OCP}	(See *Note 3*)		1		µs
IMON Accuracy	I_{MON_ACC}	0.7A < I_{LIM} < 2A	I_{OUT} < I_{LIM}	-6		+6	%
		2A ≤ I_{LIM} < 3A	I_{OUT} < I_{LIM}	-3		+3	
		3A ≤ I_{LIM} ≤ 7A	I_{OUT} < I_{LIM}, T_A = +125°C	-2.5		+2.5	
			I_{OUT} < I_{LIM}, T_A = +85°C	-2		+2	
IMON Range				0		1.25	V
SETI/IMON Current Ratio					21300		A/A
SETI Clamp				1.59		1.81	V
IMON Clamp				1.49		1.69	V
SETI Fault					400		mV
SETI Resistance		I_{LIM} = 7A		2.13			kΩ
SETI Regulation Voltage					0.7		V
SETI Range				0		1.4	V

(V_{IN} = V_{SN} = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON = OPEN, PGOOD/T_J, $\overline{SMBALERT}$, SDA, SCL, ADDR = GND, R_{SETI} = 2.13kΩ, V_{CC} = 2.2µF to GND, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are V_{IN} = 48V, T_A = +25°C (See *Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Current Protection						
Slow Reverse Current Blocking Threshold	V_{RIB_SLOW}	(V_{IN} – V_{OUT}) falling	-1	-5	-10	mV
Slow Reverse Current Blocking Response Time	t_{RIB_SLOW}	(See *Figure 1*), CGN-SN = 20nF		20	30	µs
Fast Reverse Current Blocking Threshold	V_{RIB_FAST}	(V_{IN} – V_{OUT}) falling	-70	-100	-130	mV
Fast Reverse Current Blocking Response Time	t_{RIB_FAST}	(See *Figure 2*), CGN-SN = 20nF		100	160	ns
Reverse Current Blocking Rising Threshold Voltage	V_{RIB_RISING}	(V_{SN} – V_{OUT}) Rising	70	100	130	mV
Reverse Output Current drawn from OUT	I_{OUT_REV}	V_{SN} = 0V, V_{OUT} = 48V, IN = OPEN			9	mA
Gate Drive (GN, SN)						
External Reverse Protection nFET Gate Drive Voltage	V_{GN_SN}	EN = High, No-Fault Condition, V_{IN} ≥ 10V	6	6.5	7	V
Gate Active Pullup Current		EN = High, V_{GN} = V_{SN}, No Reverse Fault Condition	80	100	120	µA
Gate Pulldown Resistance		EN = High, External nFET OFF		60	120	Ω
		Always present		3		MΩ
Internal FET						
Internal nFET ON Resistance	R_{ON}	I_{LOAD} = 100mA		20	40	mΩ
Power Good Output (PGOOD/T_J)						
Logic-Low Voltage		I_{SINK} = 1mA			0.4	V
Leakage Current		V_{PULLUP} = 5V, PGOOD/T_J Open-Drain OFF			1	µA
Junction Temperature Monitoring (PGOOD/T_J)						
Accuracy		T_A = +25°C	-9		9	°C
T_J voltage		T_A = +25°C, R_{TJ} = 10kΩ to GND		652		mV
		T_A = +125°C, R_{TJ} = 10kΩ to GND		854		
dV/dTemp		T_A = +25°C to +125°C		2		mV/°C
T_J Current Limit			100		600	µA
Timing characteristics						
IN Debounce Time	t_{DEB}	Time from V_{IN} > V_{UVLO_R} and Internal FET turn-on starts	0.9	1	1.1	ms
INUVLO Blanking Time	$t_{INUVLOBLANK}$	Power-up $\overline{SMBALERT}$ assertion blanking time		0.5		ms
EN Turn-On Time		Delay from EN = 1 for the part to turn on Internal FET (provided V_{IN} > V_{UVLO_R})		2.5		ms
Internal nFET Turn-On Time	t_{ON_SWITCH}	From No Fault to I_{OUT} = 1A		150		µs

(V_{IN} = V_{SN} = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON = OPEN, PGOOD/T_J, $\overline{SMBALERT}$, SDA, SCL, ADDR = GND, R_{SETI} = 2.13kΩ, V_{CC} = 2.2µF to GND, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are V_{IN} = 48V, T_A = +25°C (See *Note 2*)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Delay between Internal nFET Turn-On and External nFET Turn-On	t_{DR}			90	100	110	µs
The delay between Internal nFET Turn-OFF and External nFET Turn-OFF	t_{DF}			90	100	110	µs
Undervoltage Lock Out Turn OFF Time	t_{OFF_UVLO}	V_{UVLO} falling from 1V to 0.8V			1		µs
Overvoltage Lock Out Turn OFF Time	t_{OFF_OVLO}	V_{OVLO} rising from 0.8V to 1V			1		µs
Undervoltage Lock Out Rising Edge Debounce Time	t_{DEB_UVLO}	V_{IN} rising			10		µs
Overvoltage Lock Out Falling Edge Debounce Time	t_{DEB_OVLO}	V_{IN} falling			10		µs
Auto Retry Tme	t_{RETRY}				800		ms
Blanking Time	t_{BLANK}			21.8	24.0	26.4	ms
Startup Timeout	t_{STO}			1080	1200	1320	ms
Loss of Ground Switch Turn OFF Time		C_{VCC} = 2.2µF			100		ms
ADC and Variables Read Out (PMBus)							
Resolution					12		bits
V_{SN}, V_{OUT} Range				3		80	V
V_{SN}, V_{OUT} Accuracy		3V ≤ V_{SN}, V_{OUT} ≤ 12V		-3.5		+3.5	%
		12V < V_{SN}, V_{OUT} < 80V		-1.5		+1.5	
I_{OUT} Range				0.7		7.0	A
I_{OUT} Accuracy		0.7A ≤ I_{OUT} < 2A	I_{OUT} < I_{LIM}, C_{IMON} = 100nF	-6		+6	%
		2A ≤ I_{OUT} < 3A	I_{OUT} < I_{LIM}, C_{IMON} = 100nF	-3		+3	
		3A ≤ I_{OUT} ≤ 7A	I_{OUT} < I_{LIM}, C_{IMON} = 100nF, T_A = +125°C	-2.5		+2.5	
			I_{OUT} < I_{LIM}, C_{IMON} = 100nF, T_A = +85°C	-2		+2	
True I_{OUT} Range = ADC Full Scale				0		1.25	V
T_J Range				0		150	°C
T_J Accuracy		T_A = +25°C		-9		+9	°C
Sampling Rate					2500		Hz
PMBus Interface Specifications							
Clock Frequency	f_{CLK}	(See *Note 3*)				1000	kHz
Bus Free Time between STOP and START	t_{BUF}			0.5			µs

(V_{IN} = V_{SN} = 3V to 80V, GN = OPEN, UVLO, OVLO/OVFB, EN, IMON = OPEN, PGOOD/T_J, $\overline{SMBALERT}$, SDA, SCL, ADDR = GND, R_{SETI} = 2.13kΩ, V_{CC} = 2.2µF to GND, T_A = -40°C to +125°C, unless otherwise noted. Typical Values are V_{IN} = 48V, T_A = +25°C (See *Note 2*)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time after Repeated Start Condition	$t_{HD;STA}$	After this period, the first clock is generated	0.26			µs
Repeated Start Condition Setup Time	$t_{SU;STA}$		0.26			µs
STOP Condition Setup Time	$t_{SU;STO}$		0.26			µs
Data Hold Time	$t_{HD;DAT}$	(See *Note 4*)	300			ns
Data Setup Time	$t_{SU;DAT}$		100			ns
Detect Clock Low Timeout	$t_{TIMEOUT}$	(See *Note 5*)	25		35	ms
Clock Low Period	t_{LOW}		0.5			µs
Clock High Period	t_{HIGH}	(See *Note 6*)	0.5			µs
Clock/Data Rise Time	t_R	(See *Note 7*)			120	ns
Clock/Data Fall Time	t_F	(See *Note 7*)			120	ns
Noise Spike Suppression Time	t_{SPIKE}	(See *Note 8*)	0		50	ns
Data, Clock, Input Low Voltage	V_{IL}				0.8	V
Data, Clock, Input High Voltage	V_{IH}		1.35		5.5	V
Data, Output Low Voltage	V_{OL}		0		0.4	V
SCL, SDA input current			-1		1	µA
Thermal Protection						
Thermal Foldback	$T_{J(FB)}$			150		°C
Thermal Shutdown	T_J			165		°C
Thermal Shutdown Hysteresis	$T_{J(HYS)}$			20		°C

Note 2: All devices are 100% production-tested at T_A = +25°C. Limits over the operating-temperature range are guaranteed by design, not production tested.

Note 3: Guaranteed by design, not production tested.

Note 4: A controller shall not drive the clock at a frequency below the minimum f_{CLK}. Further, the operating clock frequency shall not be reduced below the minimum value of f_{CLK} due to the periodic clock extending by a device. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW;SEXT}$, and $t_{LOW;MEXT}$ limits.

Note 5: Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the controller in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. A timeout condition can only be ensured if the device that is forcing the timeout holds the CLK low for $t_{TIMEOUT,MAX}$, or longer.

Note 6: $t_{HIGH,MAX}$ provides a simple guaranteed method for controllers to detect bus idle conditions. A controller can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.

Note 7: The rise and fall time measurement limits are defined as follows:
Rise Time Limits: ($V_{IL,MAX}$ - 0.15V) to ($V_{IH,MIN}$ + 0.15V)
Fall Time Limits: ($V_{IH,MIN}$ + 0.15V) to ($V_{IL,MAX}$ - 0.15V)

Note 8: Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

Timing Diagrams

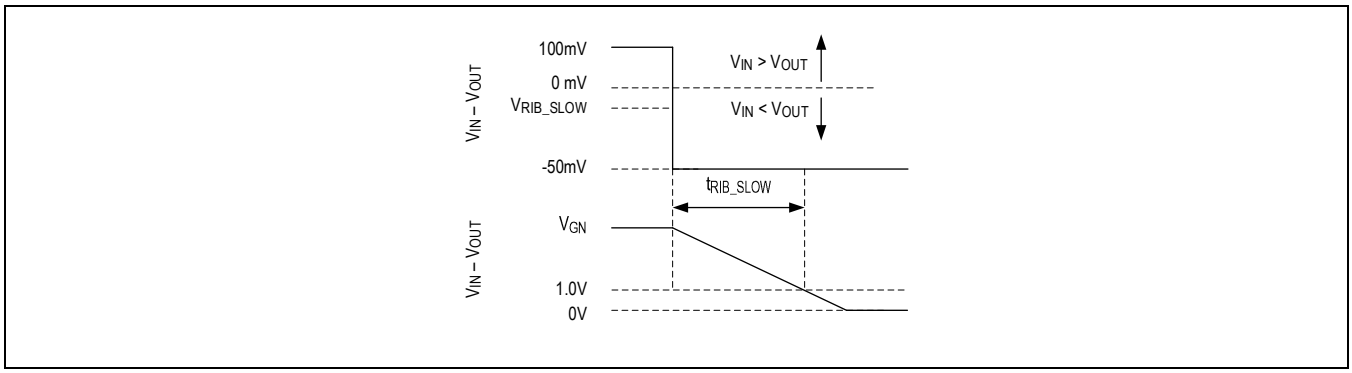


Figure 1. Slow Reverse Current Blocking Response Time

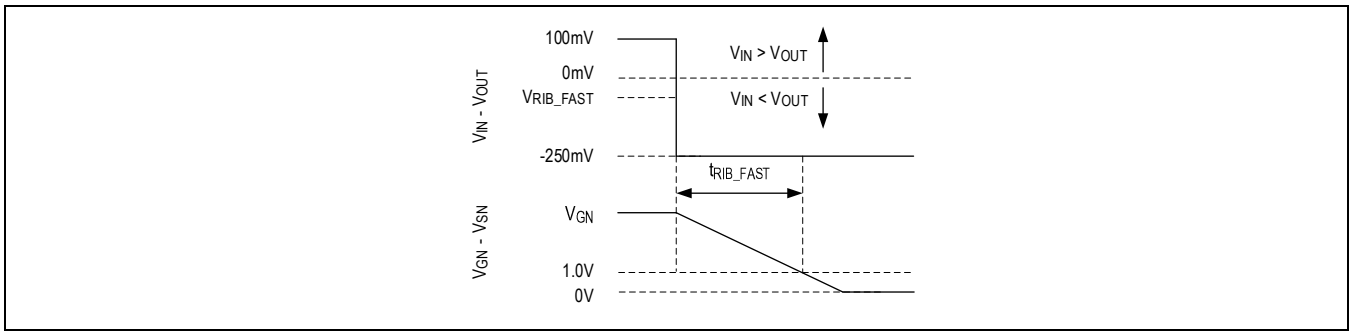
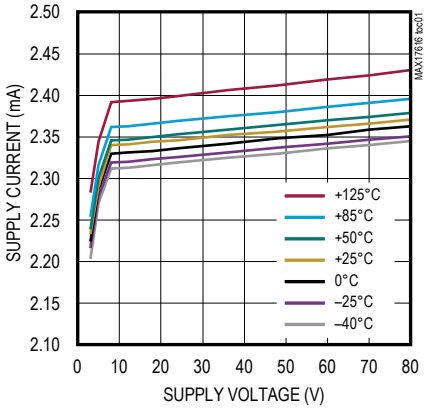


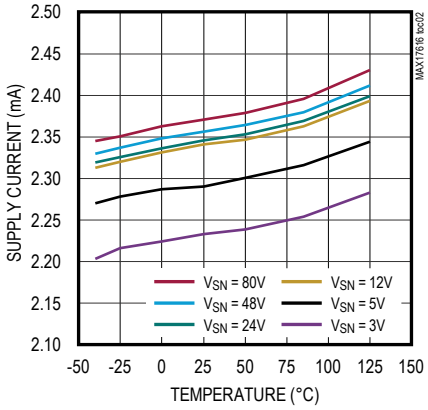
Figure 2. Fast Reverse Current Blocking Response Time

Typical Operating Characteristics

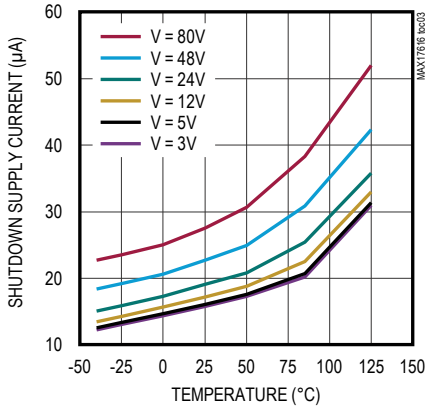
SUPPLY CURRENT vs. SUPPLY VOLTAGE



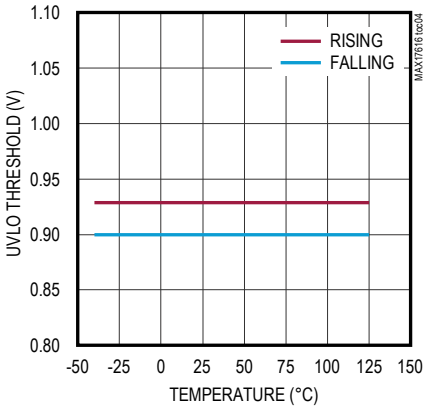
SUPPLY CURRENT vs. TEMPERATURE



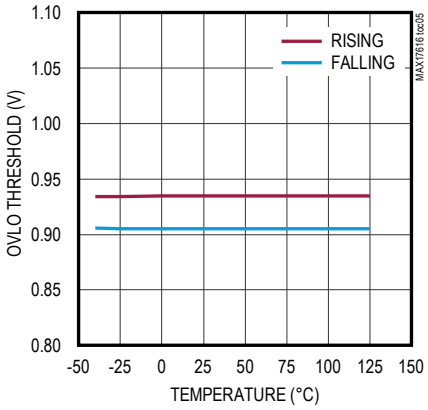
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



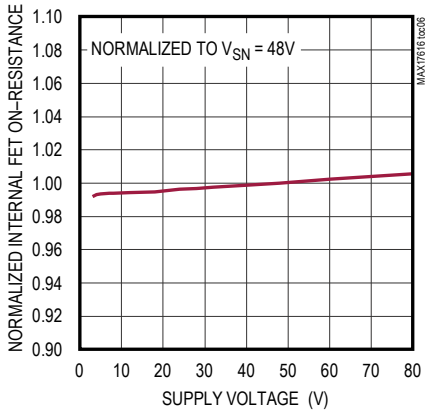
UVLO THRESHOLD vs. TEMPERATURE



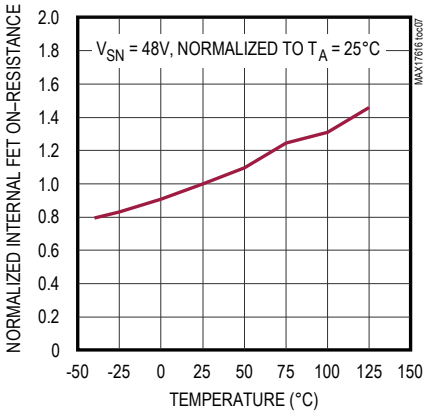
OVLO THRESHOLD vs. TEMPERATURE



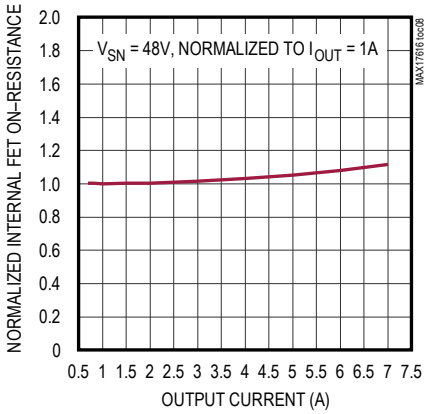
NORMALIZED INTERNAL FET ON–RESISTANCE vs. SUPPLY VOLTAGE



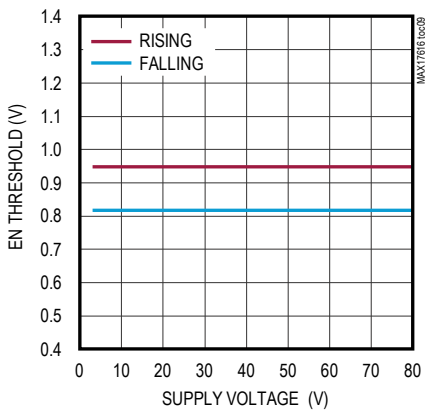
NORMALIZED INTERNAL FET ON–RESISTANCE vs. TEMPERATURE



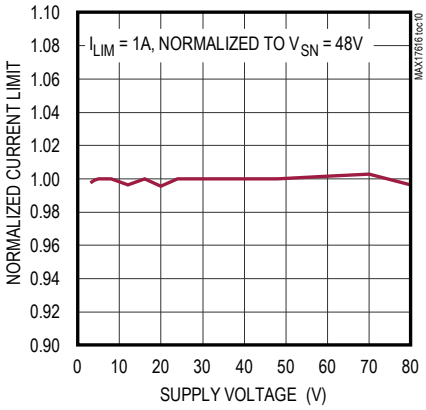
NORMALIZED INTERNAL FET ON–RESISTANCE vs. OUTPUT CURRENT



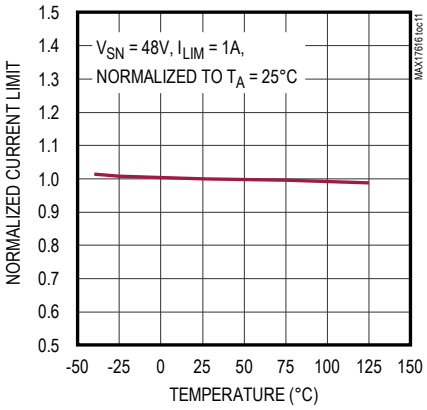
EN THRESHOLD vs. SUPPLY VOLTAGE



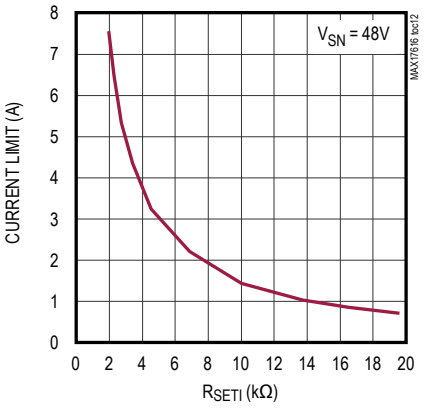
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



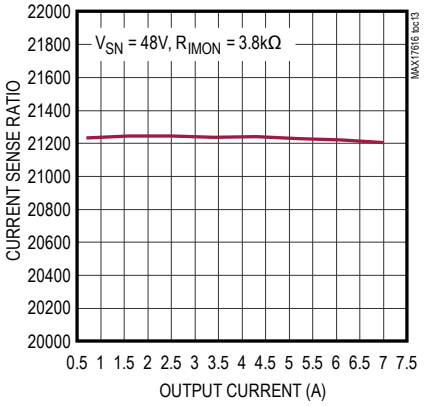
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



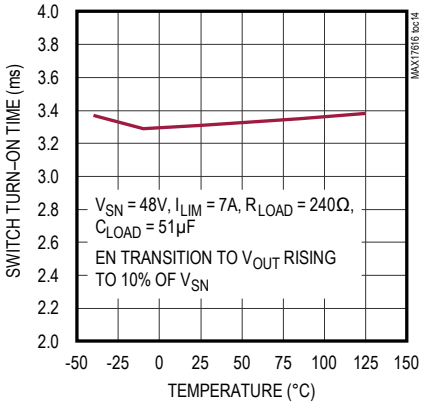
CURRENT LIMIT vs. R_{SETI}



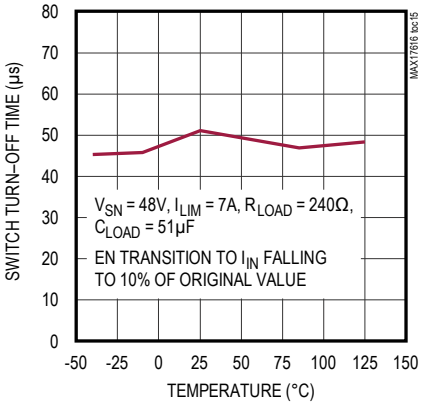
CURRENT SENSE RATIO vs. OUTPUT CURRENT



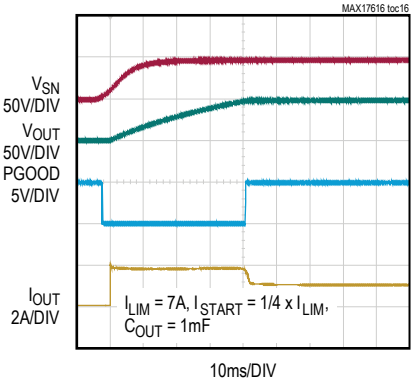
SWITCH TURN–ON TIME vs. TEMPERATURE



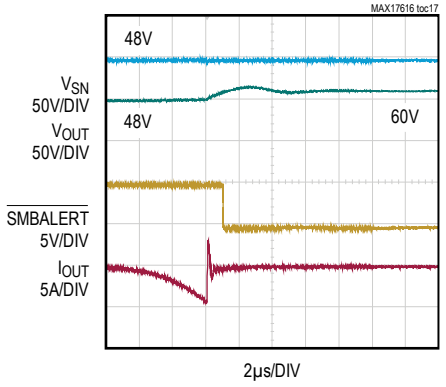
SWITCH TURN–OFF TIME vs. TEMPERATURE



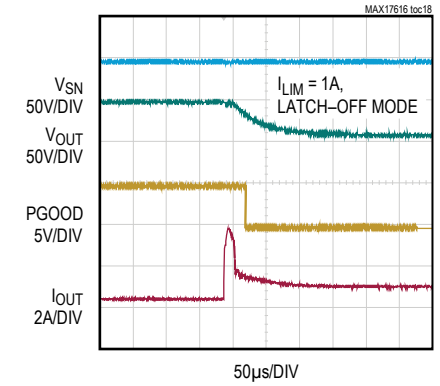
POWER–UP RESPONSE



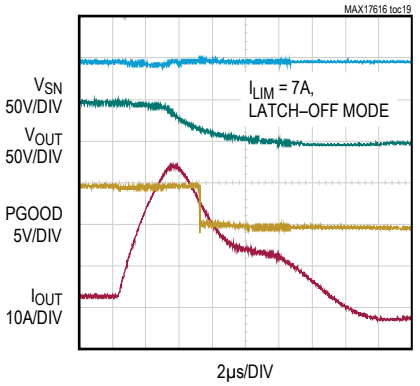
REVERSE–BLOCKING RESPONSE



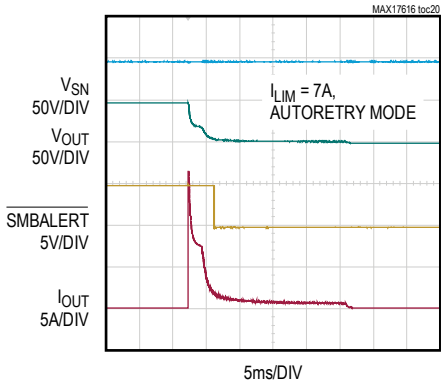
CURRENT LIMIT RESPONSE



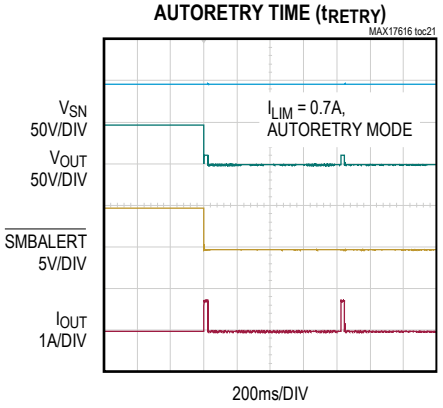
OUTPUT SHORT–CIRCUIT RESPONSE



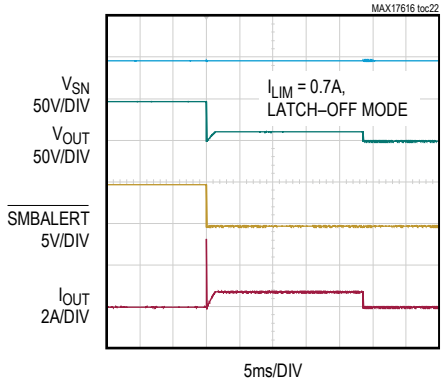
THERMAL FOLDBACK DUE TO OUTPUT SHORT–CIRCUIT



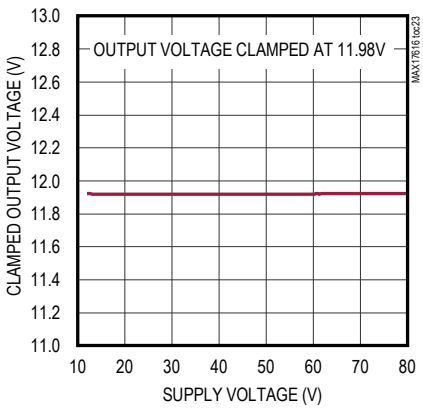
AUTORETRY TIME (t_{RETRY})



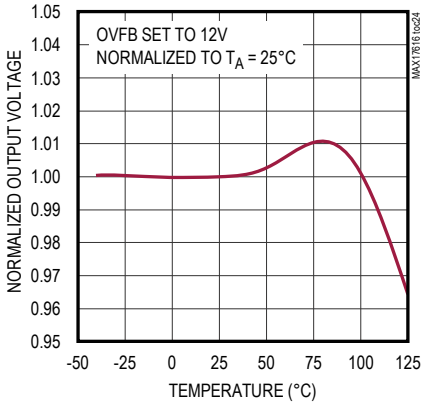
LATCH–OFF CURRENT LIMIT



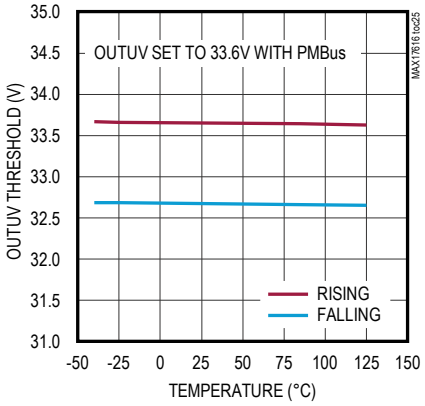
CLAMPED OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



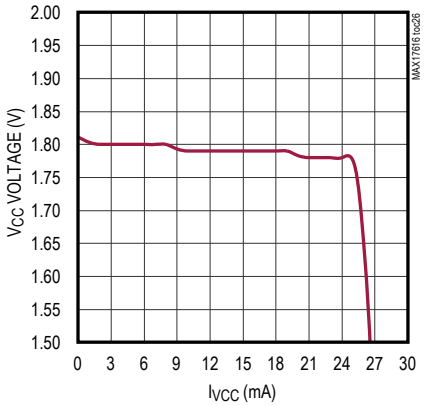
NORMALIZED CLAMPED OUTPUT VOLTAGE vs. TEMPERATURE



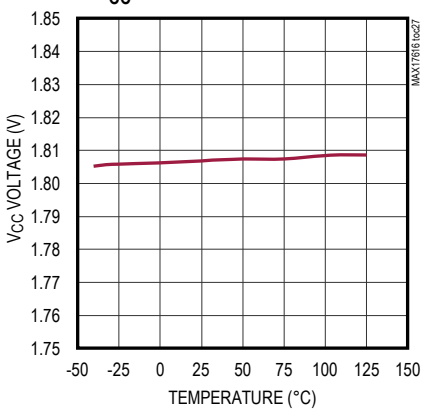
OUTUV THRESHOLD vs. TEMPERATURE



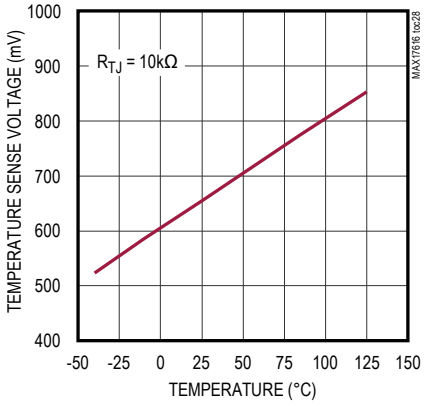
V_{CC} VOLTAGE vs. I_{VCC}



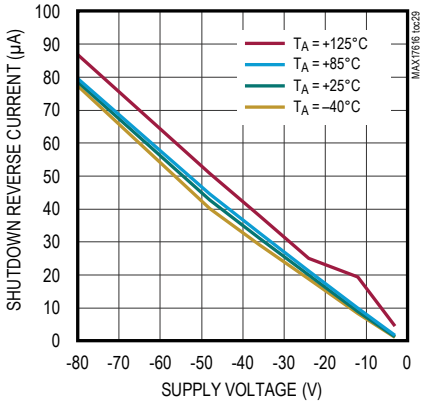
V_{CC} VOLTAGE vs. TEMPERATURE



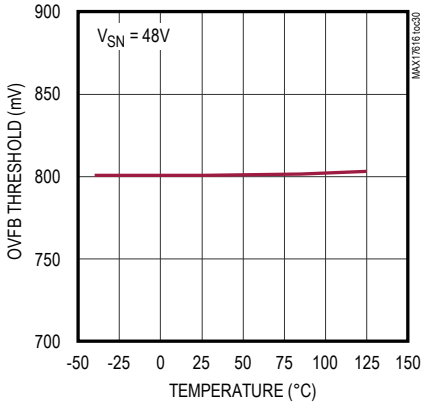
TEMPERATURE SENSE VOLTAGE vs. TEMPERATURE



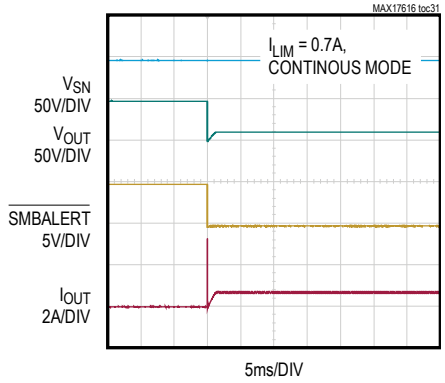
SHUTDOWN REVERSE CURRENT INTO SUPPLY vs. SUPPLY VOLTAGE



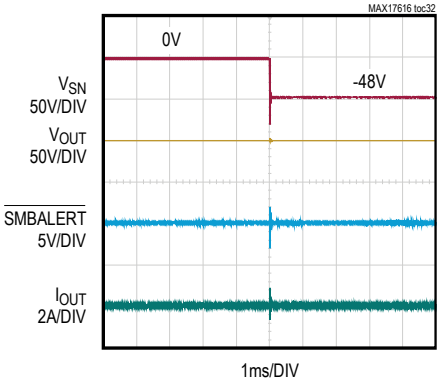
OVFB THRESHOLD vs. TEMPERATURE



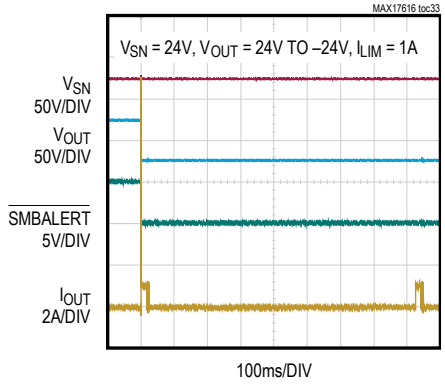
CONTINOUS CURRENT LIMIT



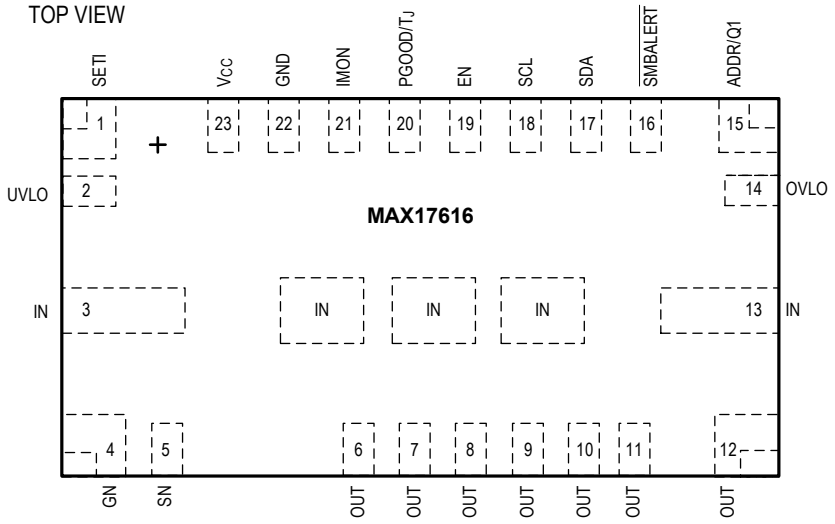
REVERSE INPUT SUPPLY PROTECTION



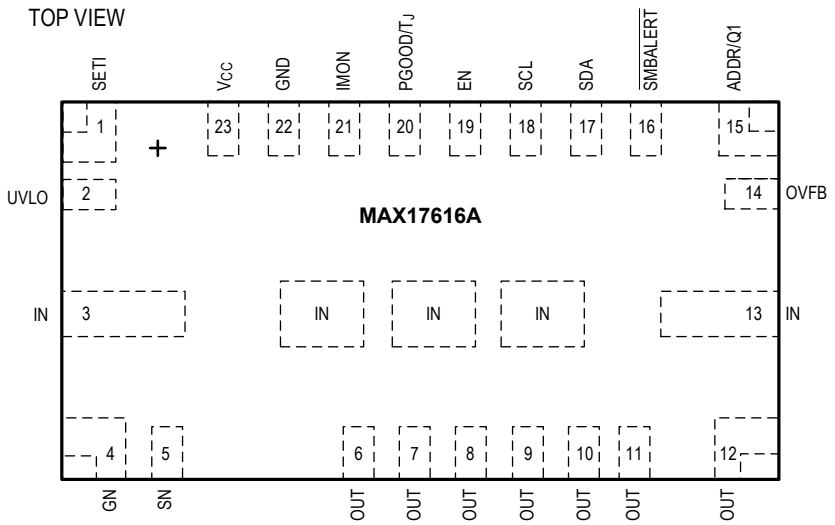
OUTPUT REVERSE POLARITY PROTECTION



Pin Configurations



23-PIN FCQFN
(4.5mm x 5.75mm)

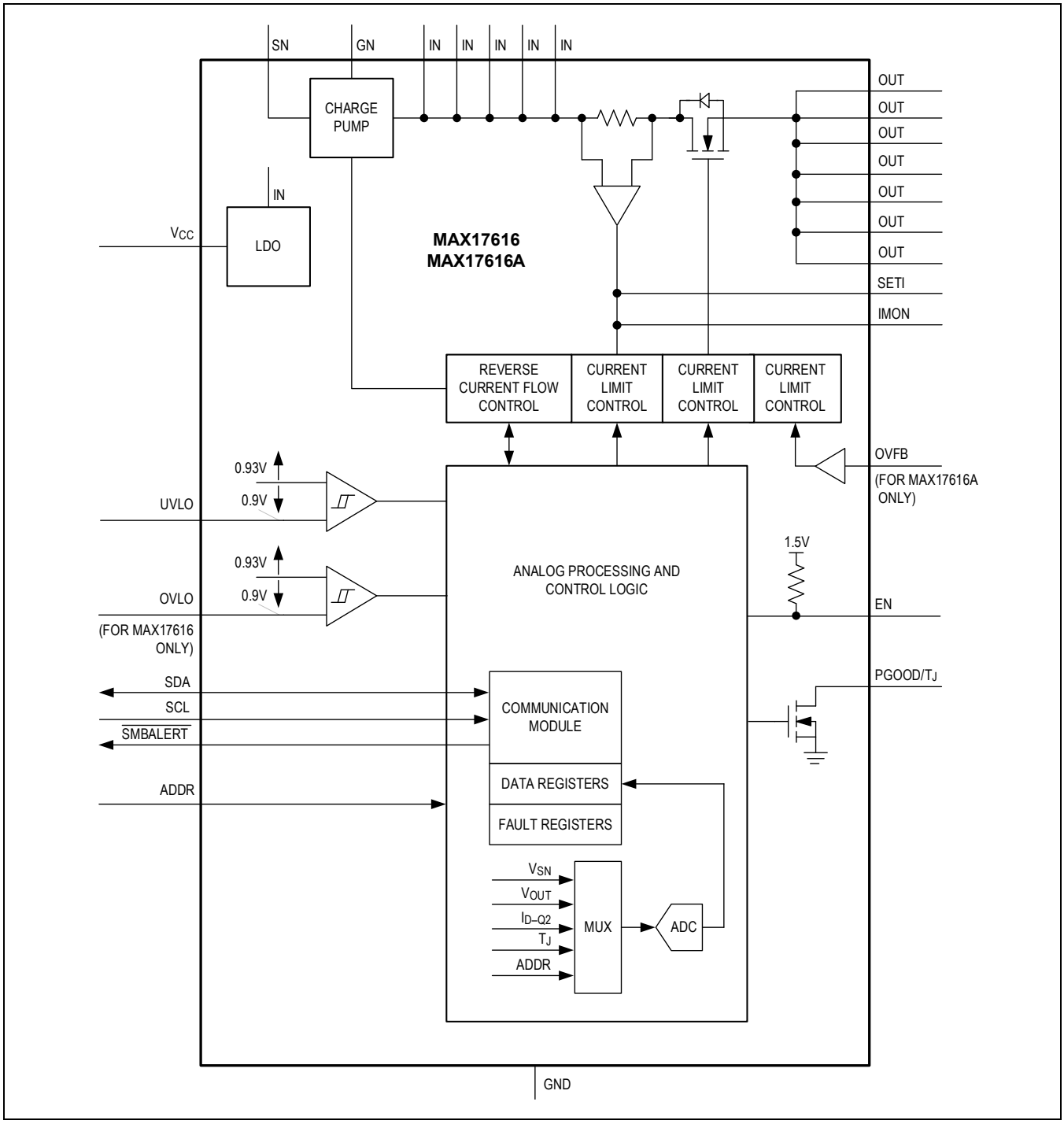


23-PIN FCQFN
(4.5mm x 5.75mm)

Pin Descriptions

PIN		NAME	FUNCTION
MAX17616	MAX17616A		
1	1	SETI	Current Limit Adjustment Pin. Connect a resistor from SETI to GND to set the current limit. See *Setting the Current-Limit Threshold* section. Do not connect more than 30pF to SETI.
2	2	UVLO	Input Under Voltage Lockout (UVLO) Adjustment Pin. Connect resistive potential divider from SN/IN to GND pin to set the UVLO threshold. Tie UVLO to a voltage higher than the UVLO threshold if the UVLO function is not used.
3, 13	3, 13	IN	Input Pins. For Hot Plug-In applications, see the *Applications Information* section.
4	4	GN	Gate Driver Output for External Reverse Protection nFET. Connect SN and GN terminals to IN, if external nFET is not used.
5	5	SN	Return for External Reverse Protection nFET and Input Voltage Sense Pin. Connect to the source of external nFET as shown in the *Typical Application Circuits*. Connect SN and GN terminals to IN, if external nFET is not used.
6–12	6–12	OUT	Output Pins. For a long output cable or inductive load, see the Applications Information section.
14	–	OVLO	OVLO Adjustment Pin. Connect resistive potential divider from SN/IN to GND pin to set the OVLO threshold. Connect OVLO to GND to disable the OVLO function.
–	14	OVFB	Output Voltage feedback pin for Over Voltage Clamp function. Connect the resistive potential divider from OUT to GND to set the output voltage clamp threshold. Connect OVFB to GND when not used. See the *Input Voltage Surge Stopping and Output Overvoltage Feedback Regulation (OVFB)* section.
15	15	ADDR/Q1	SMBus device address programming and Reverse Protection FET presence programming pin. Connect a resistor from ADDR to GND to program the device address. See the *Device Addressing and Reverse Protection (Q1) Decoding* section.
16	16	$\overline{\text{SMBALERT}}$	Active-Low SMBus Interface Line. Logic output pin. See the *Fault Output (SMBALERT)* section.
17	17	SDA	SMBus Data Line.
18	18	SCL	SMBus Clock Line.
19	19	EN	Active-High Enable Input. Internally pulled up to 1.5V. Leave unconnected for always-on the operation.
20	20	PGOOD/ T_J	Open-Drain Power Good Output or Die Temperature Monitor Output. Pull the PGOOD/T_J to an external bias voltage for the PGOOD function. PGOOD is pulled high when: • V_{OUT} exceeds OUTUV rising threshold and (V_{IN} –V_{OUT}) satisfies < VFA condition. PGOOD is pulled low when: • V_{OUT} falls below OUTUV falling threshold. This pin can also be used to monitor the die temperature. Connect a 10kΩ–20kΩ resistor from PGOOD/T_J to GND to measure device temperature. See the *Die Temperature Monitoring (PGOOD/TJ)* for more details.
21	21	IMON	Output Pin for Current Monitoring. Connect a resistor from IMON to GND to program the current monitor readout. Connect a 100nF ceramic capacitor from IMON to GND. See the Current Monitoring (IMON) section.
22	22	GND	Ground Pin. Reference pin for all control signals.
23	23	V_{CC}	Internal LDO Output. Connect a minimum of 2.2µF/0603, low-ESR ceramic capacitor from V_{CC} to GND.

Functional Diagram



Detailed Description

The MAX17616/MAX17616A offers highly versatile and programmable protection boundaries for systems against input voltage faults and output overcurrent faults. Input-voltage faults (with positive polarity) are protected up to +80V (without Reverse Current Protection)/+75V (with Reverse Current Protection), by an internal nFET featuring low ON-resistance (20mΩ typ). The devices feature a programmable undervoltage-lockout (UVLO) thresholds by using external voltage-dividers. The MAX17616 features a programmable overvoltage-lockout (OVLO) while MAX17616A offers a programmable output voltage clamp function through the OVFB pin that features an output voltage limiting regulation during input transient surge events. Input undervoltage and overvoltage protection (MAX17616)/output voltage clamp function (MAX17616A) can be programmed across the entire 3V to 80V operating range.

Input reverse-polarity protection is realized using an external nFET that is controlled by the devices. The magnitude of reverse-polarity voltage protection is dependent on the operating load-bus voltage (V_{OUT}) and the voltage-blocking capability of the external nFET. For example, for protection down to a -55V input range with V_{OUT} = 30V, an external nFET rated at 85V is needed. The external nFET is also needed for the optional reverse-current protection. When used with a Reverse Protection external nFET (Q1), the devices prevent reverse current flow from load to source by turning off Q1. The reverse current thresholds and forward bias characteristics of the reverse current protection feature are tuned to achieve an ideal diode function suited for OR-ing and Power Multiplexer applications. If reverse polarity protection and reverse-current protection are not needed, SN and GN pins must be connected to IN. The devices are tolerant against accidental output reverse-polarity application due to incorrect wiring across the output terminals.

The current limit of the devices is programmed by connecting a resistor from the SETI pin to GND. The current limit can be programmed from 0.7A to 7.0A. When the current through the devices reaches or exceeds the set current limit, the resistance of the internal nFET is modulated to limit the current. The devices offer three current-limit behavioral modes: Continuous, Auto-retry, and Latch-off modes. In addition, the devices allow programmable startup inrush current limit during startup events, to prevent inrush current from limited power sources flowing into capacitive or negative impedance output loads.

The IMON pin presents a current proportional to the device current under normal operation. Together with the IMON resistor (between IMON and GND), the IMON pin presents a voltage that is proportional to the device current. This voltage can be read by a monitoring system to record the instantaneous current of the device. Place a 100nF ceramic capacitor from IMON to GND.

The device can be turned ON or OFF by enabling input EN by a controller supervisory system. This allows the controller supervisory system to Turn ON or OFF the power delivery to connected loads.

The devices offer loss-of-ground protection where it safely turns OFF the device operation during a loss-of-ground fault event, i.e., when the safety ground fuse opens in a redundant safety application.

The devices offer a status announcement signal ($\overline{SMBALERT}$) to indicate operational and fault signals. The devices also offer a Power Good Signal (PGOOD/T_J) that may be used by a supervisory system to enable/disable the downstream loads. PGOOD/T_J is an open drain pin and requires an external pullup resistor to the appropriate system interface.

The devices offer a programmable output undervoltage sense threshold that governs the restart response after the output voltage drops below the OUTUV Rising threshold. The device also offers internal thermal shutdown protection against excessive power dissipation.

The devices offer a PMBus compatible Serial Peripheral Interface, with commands to control the device operation and observe system level parameters.

Input Undervoltage Lockout (UVLO)

The devices have a UVLO adjustment range from 3V to 79V. Connect an external resistive potential divider to the UVLO pin, as shown in the *Figure 3*, to adjust the UVLO threshold voltage. Use the following equation to adjust the UVLO threshold. For low-bias current applications, such as a battery supply, the recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{UVLO\_RISING}\ x\ \left(1 + \frac{R_1}{R_2}\right)$$

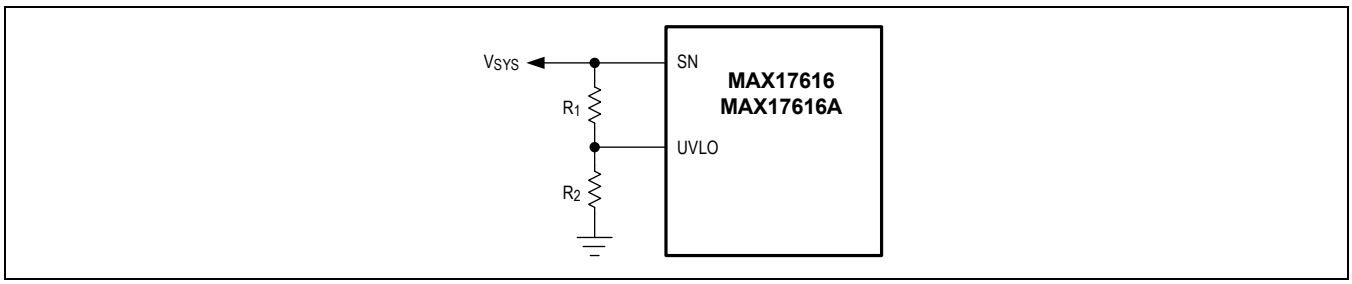


Figure 3. Adjustable Input UVLO

A 30mV (typ) hysteresis is provided on the UVLO pin, thus causing the devices to enter and exit undervoltage conditions in a deterministic manner. When the UVLO pin voltage falls below 0.9V (typ), the internal nFET turns OFF, and $\overline{\text{SMBALERT}}$ is asserted low. The external nFET, if used, turns OFF after a delay time (t_{DF}) of 100µs. When the Undervoltage condition is removed, and the UVLO pin voltage rises above 0.93V (typ), the devices take undervoltage lockout rising to debounce time (t_{DEB_UVLO}) to start the switch turn ON process. The internal nFET turns ON, and the external nFET turns ON after a delay time (t_{DR}) of 100µs, and $\overline{\text{SMBALERT}}$ is de-asserted. The UVLO pin must not be left unconnected.

A typical undervoltage turn-on and turn-off sequence when the voltage on the UVLO pin increases above the rising threshold and decreases below the falling threshold. See *Figure 4* for more details.

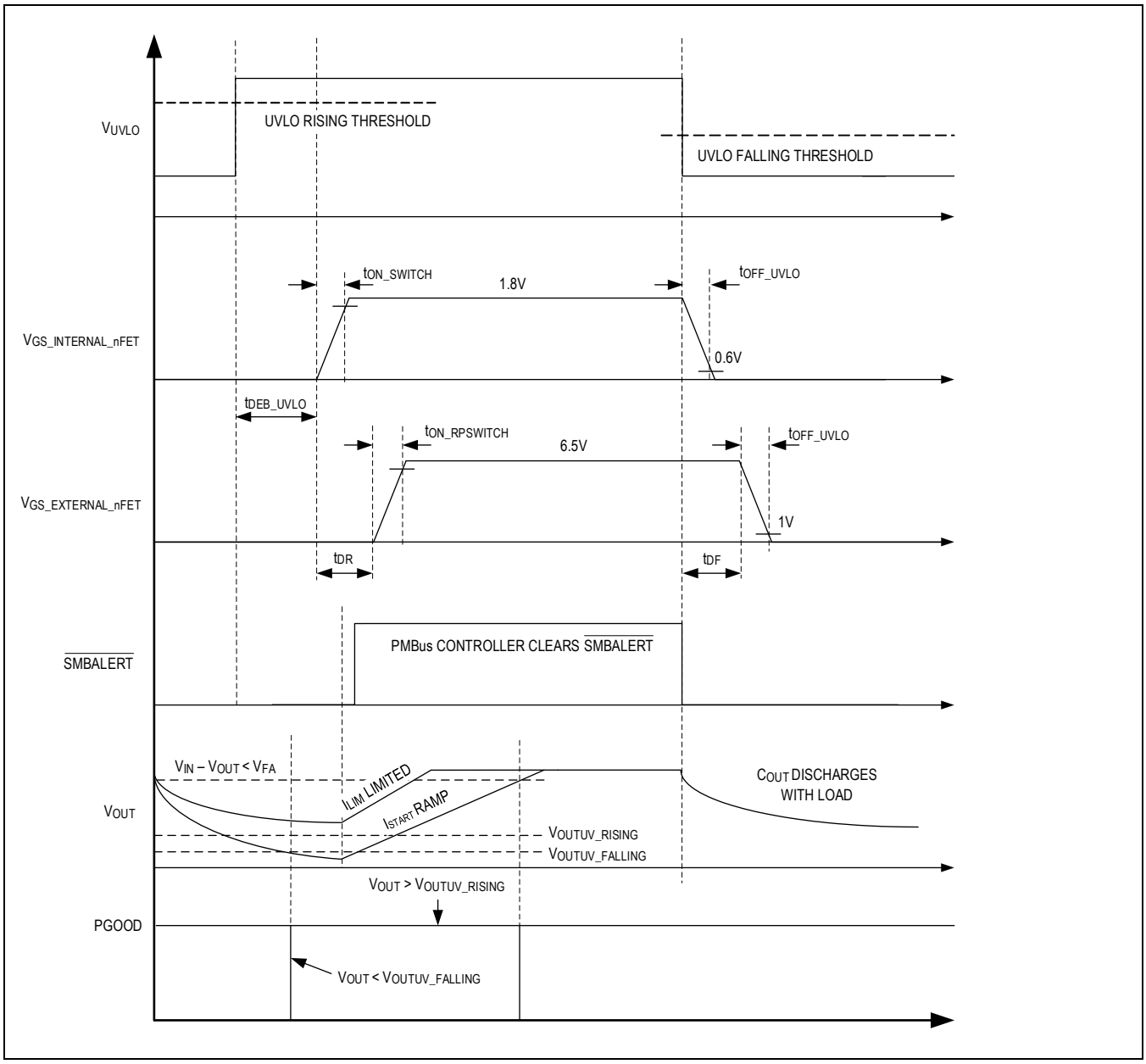


Figure 4. Input Undervoltage Fault Timing Diagram

Input Overvoltage Lockout (OVLO)

The MAX17616 has an OVLO adjustment range from 3.5V to 80V. Connect an external resistive potential divider to the OVLO pin, as shown in the *Figure 5*, to adjust the OVLO threshold voltage. Use the following equation to adjust the OVLO threshold. For low-bias current applications, such as a battery supply, the recommended value of R3 is 2.2MΩ.

$$V_{OVLO} = V_{OVLO\_RISING}\, x\, \left(1 + \frac{R_3}{R_4}\right)$$

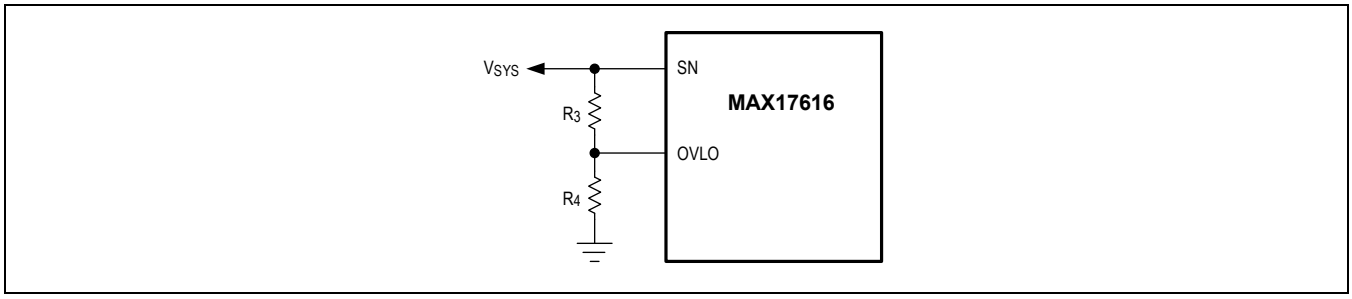


Figure 5. Adjustable Input OVLO

A 30mV (typ) hysteresis is provided on the OVLO pin, thus causing the devices to enter and exit overvoltage conditions in a deterministic manner. When the OVLO pin voltage rises above 0.93V (typ), the internal nFET turns OFF, and $\overline{\text{SMBALERT}}$ is asserted low. The external nFET, if used, turns OFF after a delay time (t_{DF}) of 100µs. When the overvoltage condition is removed, and the OVLO pin voltage falls below 0.9V (typ), the MAX17616 takes overvoltage lockout rising debounce time (t_{DEB_OVLO}) to start the switch turn-on process. The internal nFET turns ON, and the external nFET turns ON after a delay time (t_{DR}) of 100µs, and $\overline{\text{SMBALERT}}$ is de-asserted. If the OVLO function is not used, the OVLO pin must be connected to GND. The OVLO pin must not be left unconnected.

A typical overvoltage turn-off and turn-on sequence when the voltage on the OVLO pin increases above the rising threshold and decreases below the falling threshold. See *Figure 6* for more details.

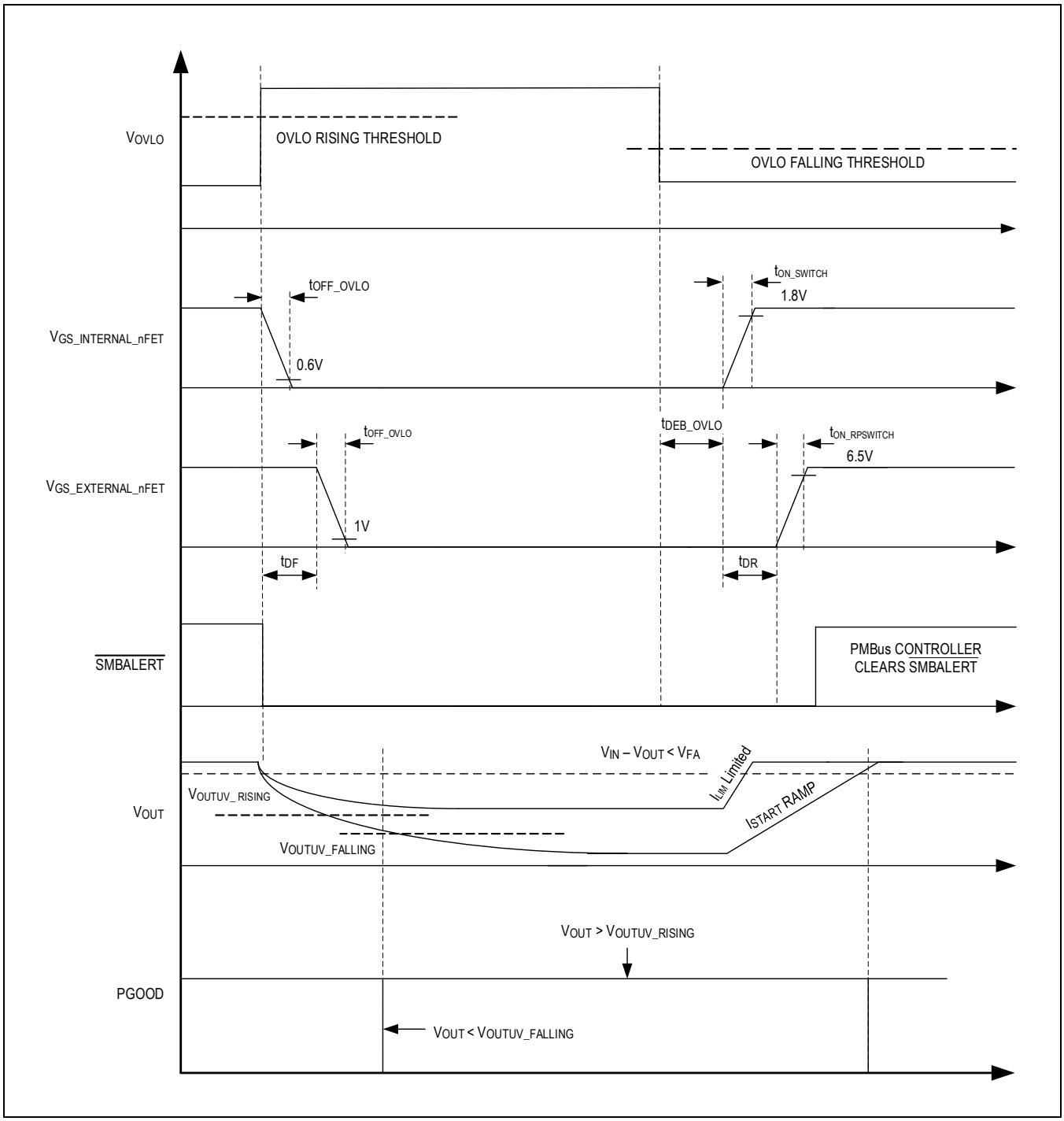


Figure 6. Input Overvoltage Fault Timing Diagram

Input Debounce Protection

The devices provide input debounce protection. The devices start operation (by turning on the nFETs) only if the IN pin voltage is higher than the $V_{IN\_UVLO(R)}$ rising threshold for a period greater than the debounce time (t_{DEB}). If the voltage at the IN pin falls below the $V_{IN\_UVLO(F)}$ falling threshold before t_{DEB} has elapsed, the devices remain off. When the devices are turned ON through EN, t_{DEB} + EN turn-on time is always present. *Figure 7* shows a typical Input power-up timing sequence.

During initial power up (either hot plug-in, controlled input voltage slew rate, or otherwise), when the input voltage crosses INUVLOR (2.86V Max), If the input voltage does not reach the UVLO pin programmed voltage until INUVLO_Blanking_Time ($t_{INUVLOBLANK}$) = 500µs(typ), then the part shall declare UVLO fault by pulling $\overline{SMBALERT}$ low.

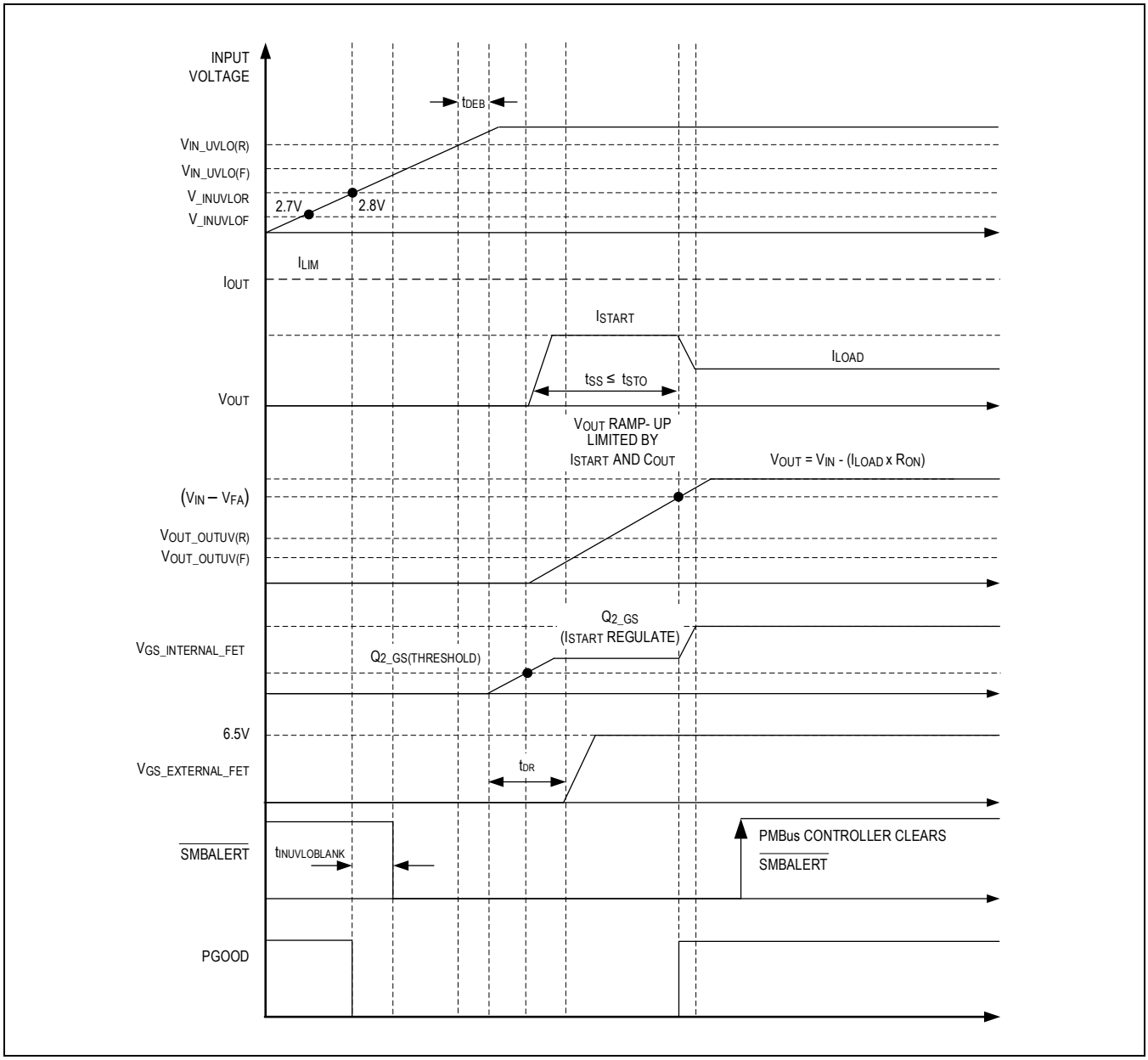


Figure 7. Input Power-up Timing Diagram

Enable

The MAX17616/MAX17616A can be turned ON or OFF using the enable input pin (EN) to control the power delivery to connected loads. The OPERATION command works in conjunction with the EN pin to turn the devices ON or OFF. In Latch-Off Mode, the EN pin must be pulled low below 0.4V for at least 10µs to reset the fault condition and the devices resume operation. The EN pin is internally pulled up to 1.5V to have an always-on option when it is left open.

Figure 8 and *Figure 9* show turn-on and turn-off control with EN.

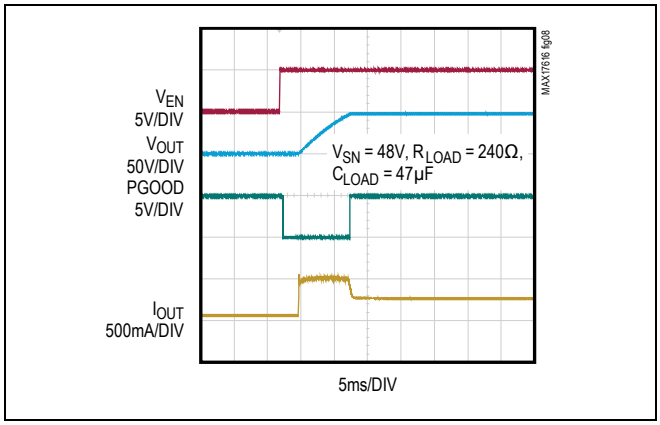


Figure 8. Turn-on Control through EN Pin

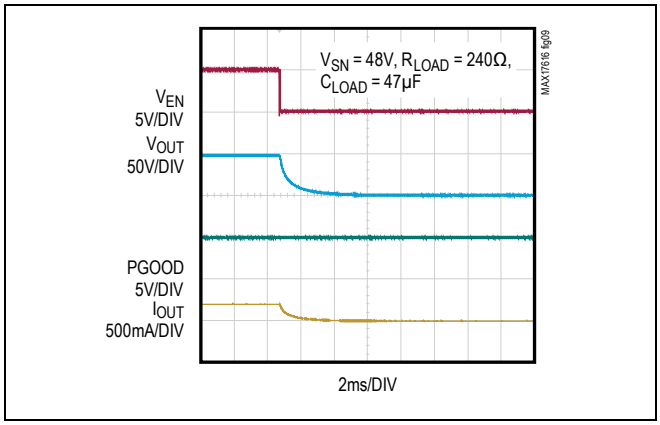


Figure 9. Turn-off Control through EN Pin

Startup Inrush Current Limit (I_{START})

The devices offer a programmable startup inrush current limit feature to limit the inrush current drawn from the power source and delivered to large capacitive loads. During the startup timeout period (t_{STO}), the current delivered to the output is limited to I_{START} when $V_{OUT} < V_{IN} – V_{FA}$. The t_{STO} timeout period is applied when there is a restart after a turn-off event caused by POR, EN, UVLO, or OVLO. If the output is not charged to ($V_{IN} – V_{FA}$) level within t_{STO}, the devices turn off, and IN or EN must be toggled to resume normal device operation, irrespective of CLMODE selected.

I_{START} is programmed using the SET_ISTART_RATIO command. The inrush current limit during startup (I_{START}) is calculated as:

$$I_{START} = I_{LIM} \, x \, I_{START\_RATIO}$$

where I_{LIM} is the current limit programmed using SETI pin and

I_{START_RATIO} is a value between (1/16, 1/8,1/4,1/2,1).

The startup time for large capacitive loads may be calculated using the following equation:

$$t_{SS} = \frac{V_{IN} \, x \, C_{OUT}}{I_{START}}$$

where t_{SS} is the required startup charging time in seconds.

Figure 10 shows a typical Startup Timing Sequence during powerup.

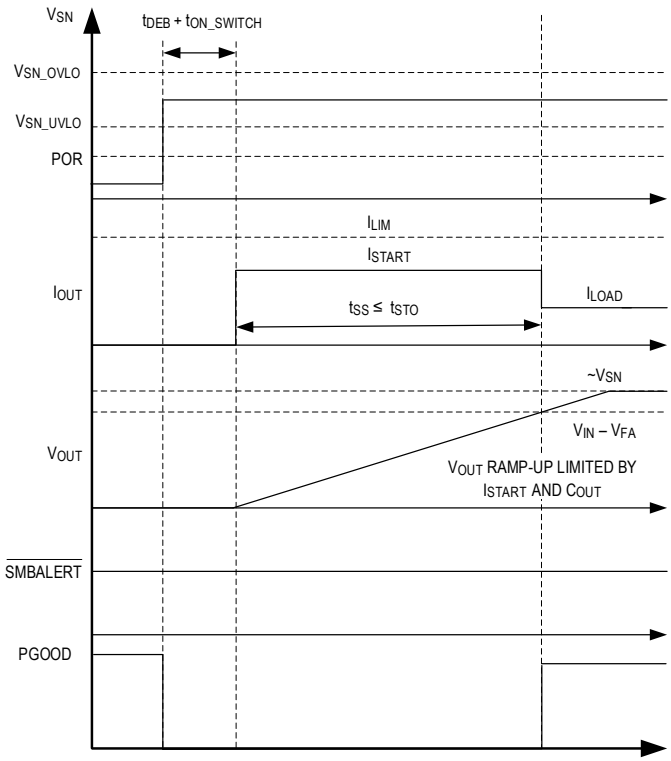


Figure 10. I_{START} Timing Diagram

PGOOD remains asserted low during the soft start period. As the output voltage increases, when the voltage drop across the internal nFET (measured across IN and OUT pins) falls below an internal threshold V_{FA}, PGOOD is de-asserted.

Setting the Current-Limit Threshold (I_{LIM})

Connect a resistor between SETI and GND to program the current-limit threshold in the device. Use the following equation to calculate the current limit-setting resistor:

$$R_{SETI}(k\Omega) = \frac{14910}{I_{LIM}(mA)}$$

where I_{LIM} is the desired current limit in mA.

Do not use an R_{SETI} smaller than 1.86kΩ. *Table 1* shows current-limit thresholds for different resistor values.

Table 1. Current-Limit Threshold vs. Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT I_{LIM} (A)
21.0	0.7
14.7	1
7.32	2
4.87	3
3.65	4
2.94	5
2.43	6
2.10	7

If SETI is left unconnected, $V_{SETI} \geq 1.5V$, and the current regulator does not allow any current to flow. The devices perform a check on the SETI pin for the first time, and it exits a shutdown condition. If the resistor placed on SETI is below 1kΩ, the switch remains off, and the $\overline{SMBALERT}$ asserts. *Figure 11* shows the SETI response during a load step event.

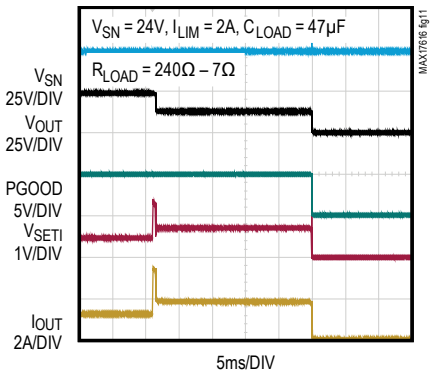


Figure 11. SETI Response during a Load Step Event

Current Monitoring (IMON)

The devices offer a dedicated IMON pin to monitor the load current flowing through the internal nFET.

Connect a 100nF ceramic capacitor from the IMON pin to GND. Connect a resistor (R_{IMON}) between IMON and GND to monitor the device current. Use the following equation to calculate the monitoring resistor R_{IMON}:

$$R_{IMON} = \frac{26625}{I_{LIM}(mA)}$$

where R_{IMON} is the resistance from IMON to GND in kΩ.

The voltage on the IMON pin (V_{IMON}) is calculated using the following formula:

$$V_{IMON} = \frac{I_{nFET}}{21300} \times R_{IMON}$$

where I_{nFET} is the load current through the internal FET.

Current-Limit and Short-Term Over Current features

The devices feature Short-Term Over Current Loading Capability (I_{STLIM}) to support load current profiles that contain short-term overload currents during normal operation. The I_{STLIM} is set to two times the programmed current limit (I_{LIM}) on the SETI pin, and the short-term over the current duration(t_{STOC}) is set to 400µs.

1) If the load current exceeds I_{LIM} but stays lower than I_{STLIM} for a duration < t_{STOC}, the devices do not limit the current, and normal operation continues.
2) If the load current exceeds I_{LIM} but stays lower than I_{STLIM} for duration > t_{STOC}, or If the load current exceeds I_{STLIM} but stays lower than I_{OCP}, the devices limit the current to the programmed current limit (I_{LIM}) within ~100µs.

Once the devices enter the current limit (ILIM), the devices' operation is decided by the current limit mode as described in the *Current-Limit Type Select* section.

The short-term over the current limit is set using the SET_ISTLIM command, and the short-term over the current duration is set using the SET_TSTOC command.

Figure 12 shows the Current Limit and Short-Term Overcurrent timing diagram.

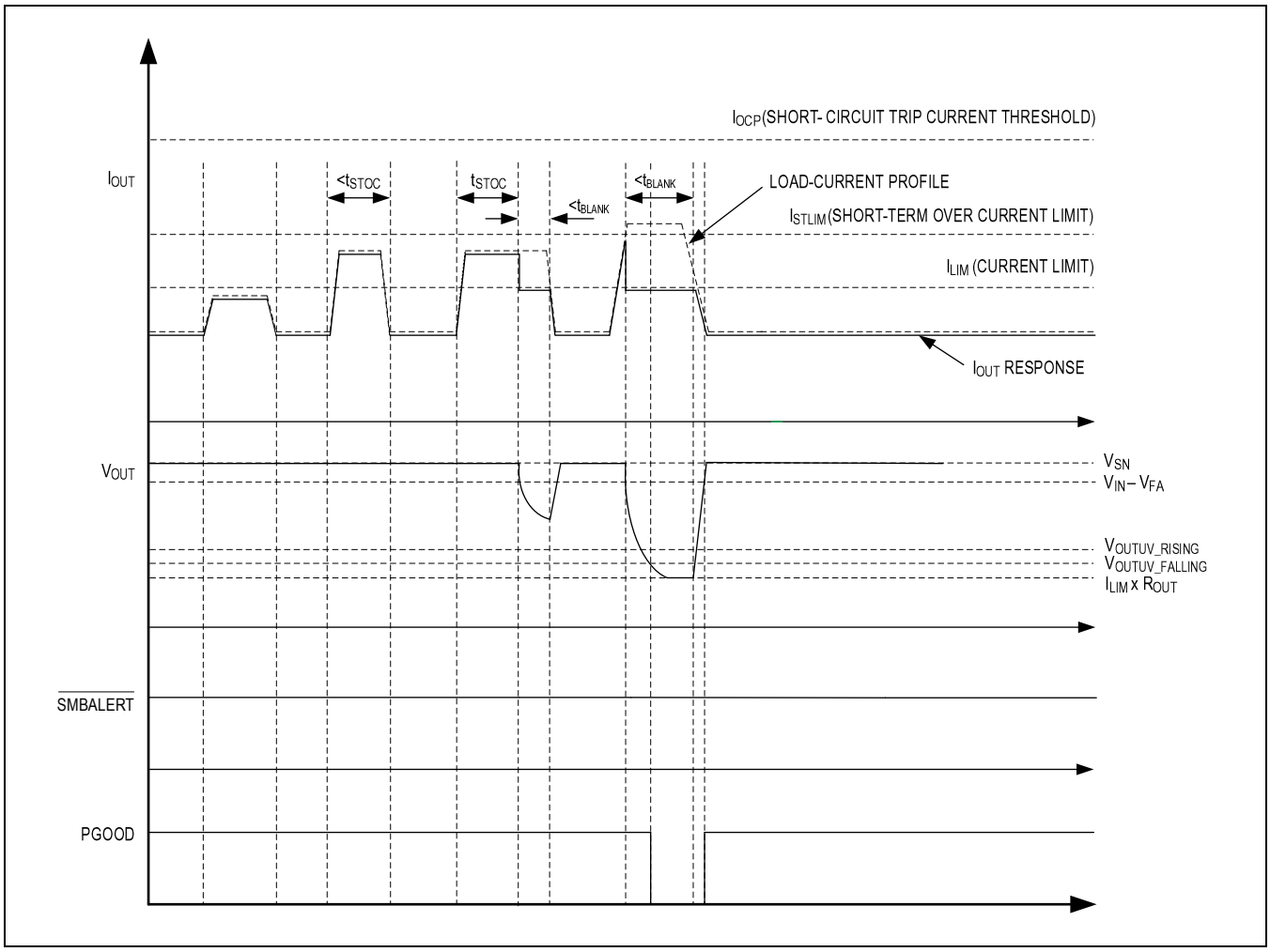


Figure 12. Current Limit and Short-Term Overcurrent Timing Diagram

Current-Limit Type Select

The MAX17616/MAX17616A features three selectable current limit modes, namely, Continuous, Auto-Retry, and Latch-Off modes. The current limit mode is programmed through the SET_CLMODE PMBus command. If the (V_{IN} – V_{OUT} < V_{FA}) condition is not met within t_{STO}, the devices enter a Latch-Off state, irrespective of the CLMODE selected.

Continuous Current Limit

In Continuous current-limit mode, the devices limit the current continuously. The $\overline{\text{SMBALERT}}$ asserts when the current limit exceeds t_{BLANK} duration, and deasserts when voltage drop across the internal switch falls below V_{FA}. *Figure 13* depicts typical behavior in continuous current-limit mode.

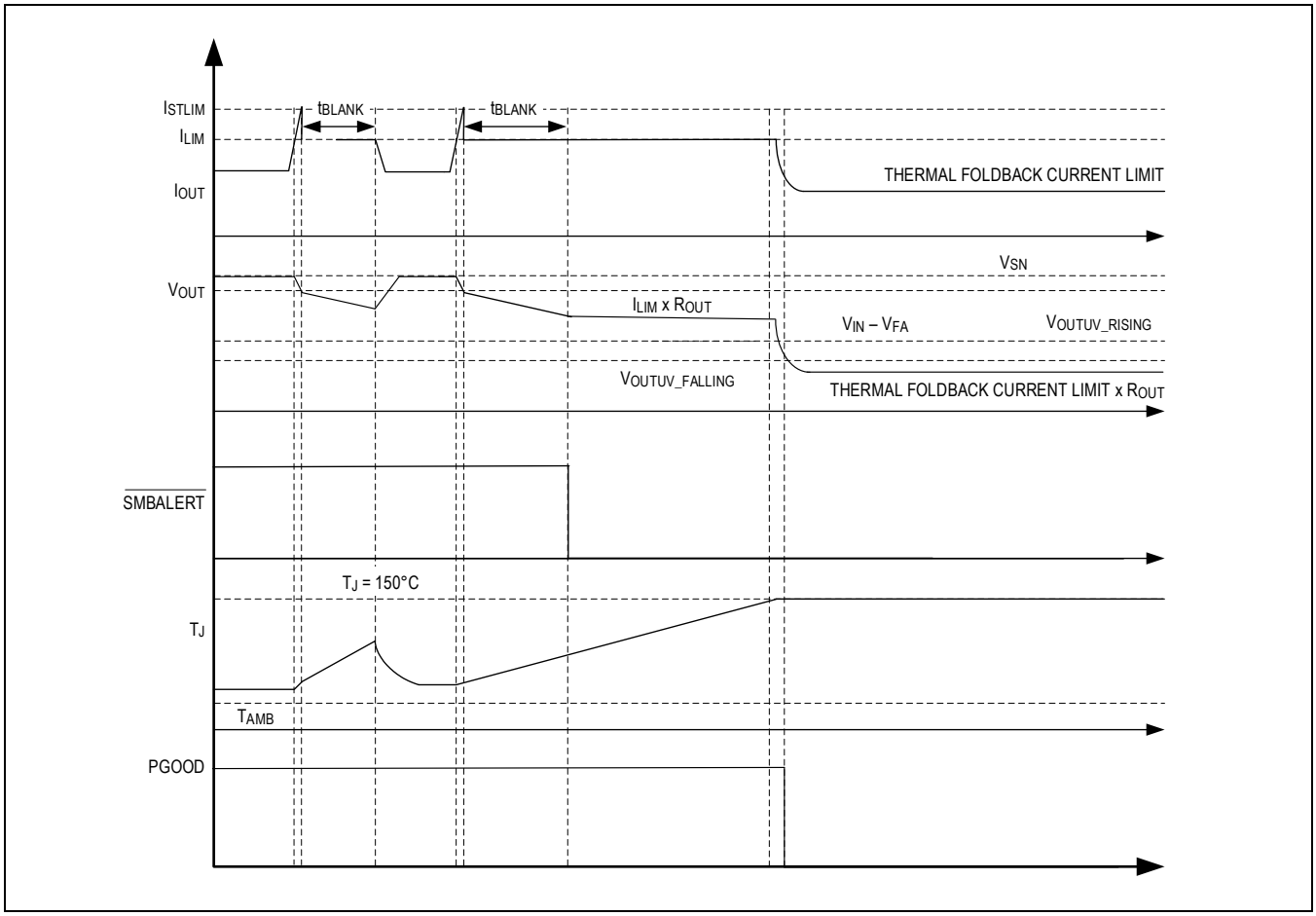


Figure 13. Continuous-Fault Timing Diagram

Autoretry Current Limit

In Autoretry current limit mode, the devices attempt to restart operation after an internally fixed Autoretry period (t_{RETRY}). The internal Autoretry timer is activated when an overcurrent event condition remains for the blanking timer period (t_{BLANK}). The blanking timer resets if the overcurrent condition resolves before t_{BLANK} has elapsed. During the t_{RETRY} period, the switch remains OFF. Once t_{RETRY} has elapsed, the device restarts with I_{LIM}. If the fault exists, the cycle repeats, and $\overline{\text{SMBALERT}}$ remains asserted. If the overcurrent condition is resolved, the switch stays ON. The $\overline{\text{SMBALERT}}$ pin asserts when the current limit exceeds t_{BLANK} duration and desserts, when voltage drops across the internal switch, and falls below V_{FA}.

The Autoretry feature reduces system power in case of overcurrent or short-circuit conditions. When the switch is ON during t_{BLANK} time, the supply current is held at the current limit. During t_{RETRY} time, there is no current through the switch. Thus, the average output current is much less than the programmed current limit. The average output current can be calculated using the following equation:

$$I_{LOAD} = I_{LIM} \times \frac{t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

With a 24ms (typ) t_{BLANK} and 800ms (typ) t_{RETRY}, the duty cycle is 2.9%, resulting in a 97.1% power reduction when compared to the switch being on the entire time. *Figure 14* shows typical behavior in the Autoretry Current-Limit mode.

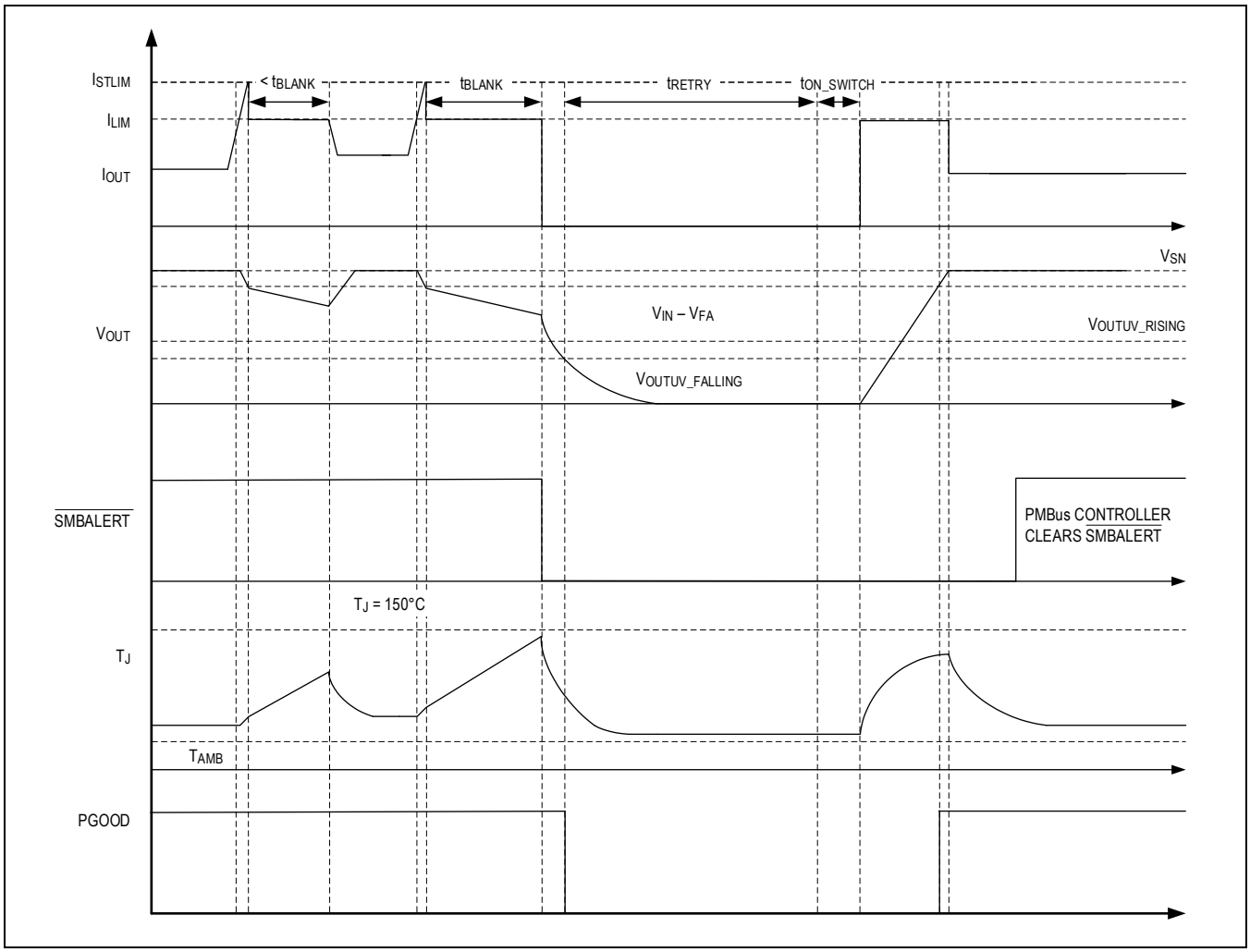


Figure 14. Autoretry Fault Timing Diagram

Latch-Off Current Limit

In Latch-Off current limit mode, the devices remain OFF and latched, if an overcurrent event remains for the blanking timer period (t_{BLANK}). The blanking timer resets if the overcurrent condition resolves before t_{BLANK} has elapsed.

The device operation may be reset by sending the OPERATION command. *Figure 15* shows typical behavior in latch-off current-limit mode.

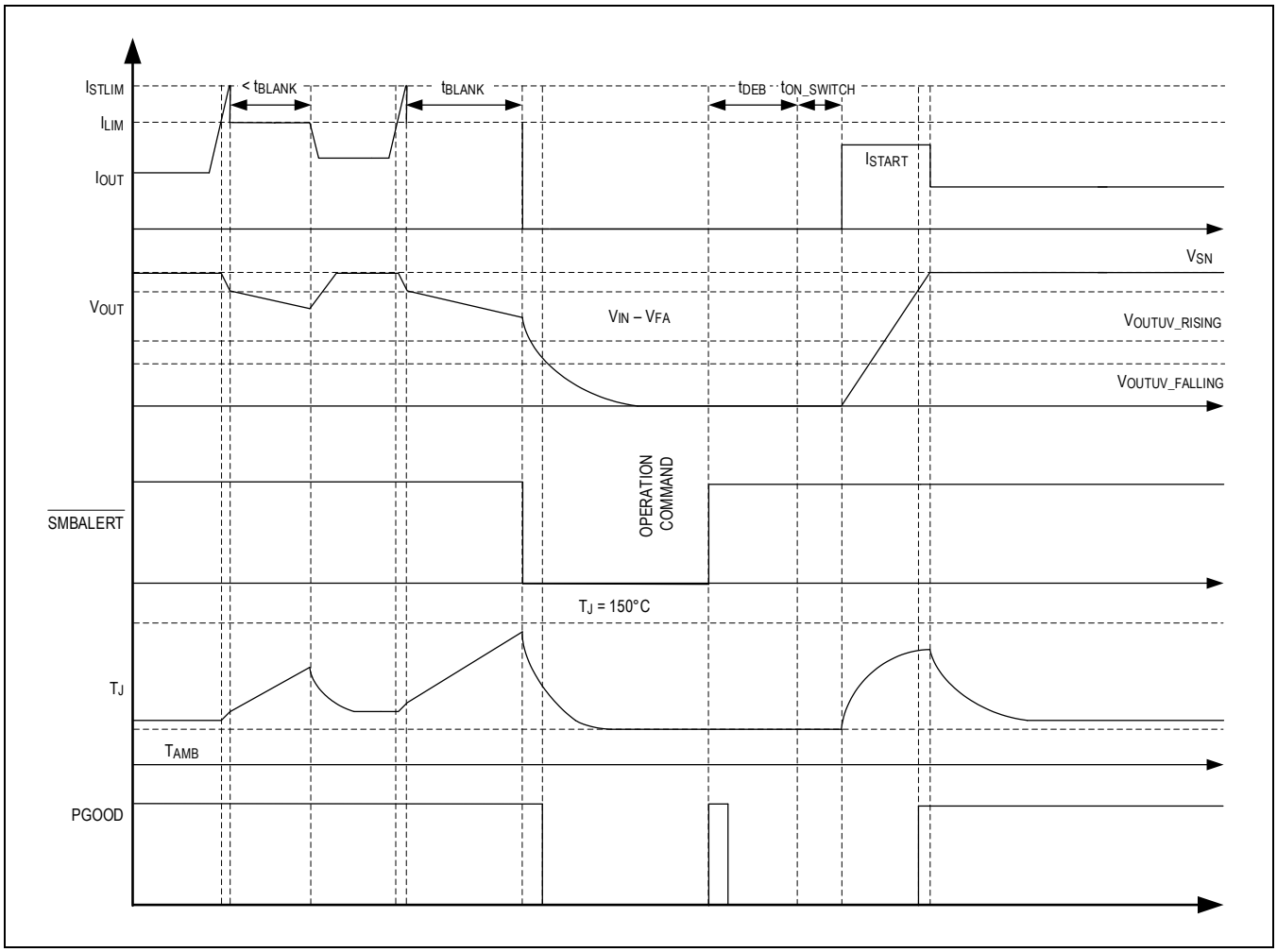


Figure 15. Latch-off Fault Timing Diagram

Short Circuit Protection

During an output short circuit event, the current through the device increases very rapidly. The devices incorporate a fast-trip current comparator to limit the output short circuit peak current. The fast-trip current comparator turns off the internal nFET within 1µs (t_{DELAY1}) when the current through the internal FET exceeds I_{OCP}. The I_{OCP} is internally set to 30A (typ). After a time delay of 200µs (t_{DELAY2}), the device turns back ON and limits the output current to the programmed current limit, and operates as described in earlier current limit mode sections. *Figure 16* illustrates the behavior of the system when the current exceeds the I_{OCP} threshold.

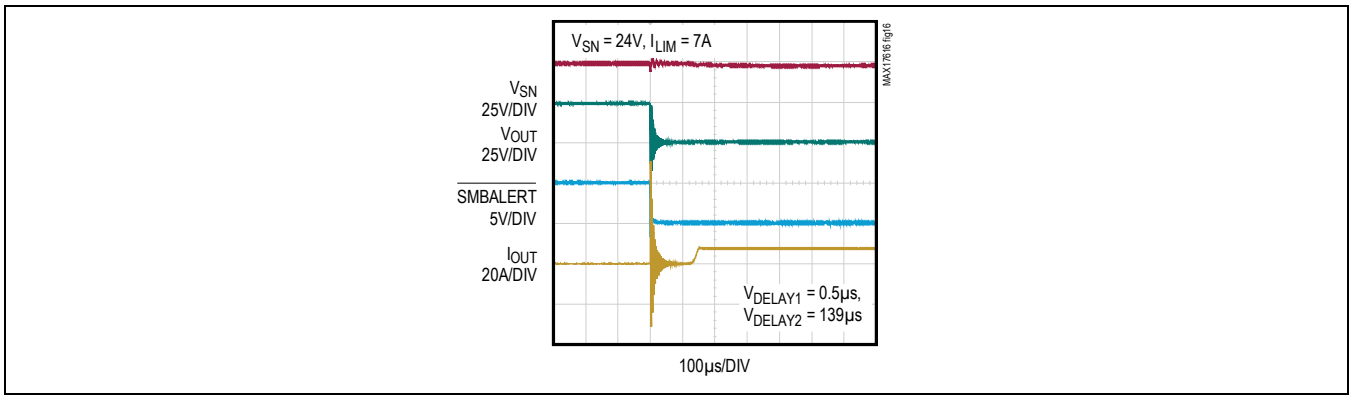


Figure 16. Short Circuit Response

Reverse Current Protection

The reverse current-protection feature is enabled when used with external nFET. The devices prevent reverse current flow from OUT to IN pins.

If a reverse current condition is detected (V_{IN} - V_{OUT}) < $V_{RIB\_}$), the external nFET is turned OFF. When the reverse current condition no longer exists (V_{SN} - V_{OUT}) > V_{RIB_RISING}), the external nFET is turned back ON after $t_{ON\_RPSWITCH}$. If the reverse-current condition is the only fault (no UVLO, no OVLO, no thermal fault, no forward overcurrent fault), then the internal nFET is kept ON. Otherwise, the internal nFET is also turned OFF. *Figure 17* shows typical behavior in a slow- or fast-reverse-current condition.

The device contains two reverse-current thresholds with slow (20µs typ) and fast (100ns typ) response times for reverse-current protection. The threshold value for slow reverse is -5mV (typ), whereas for fast reverse, it is -100mV (typ). This feature results in robust operation in a noisy environment while still delivering fast protection for a severe fault, such as input short-circuit or hot plug-in at the OUT pins. The $\overline{SMBALERT}$ pin asserts during a reverse current condition.

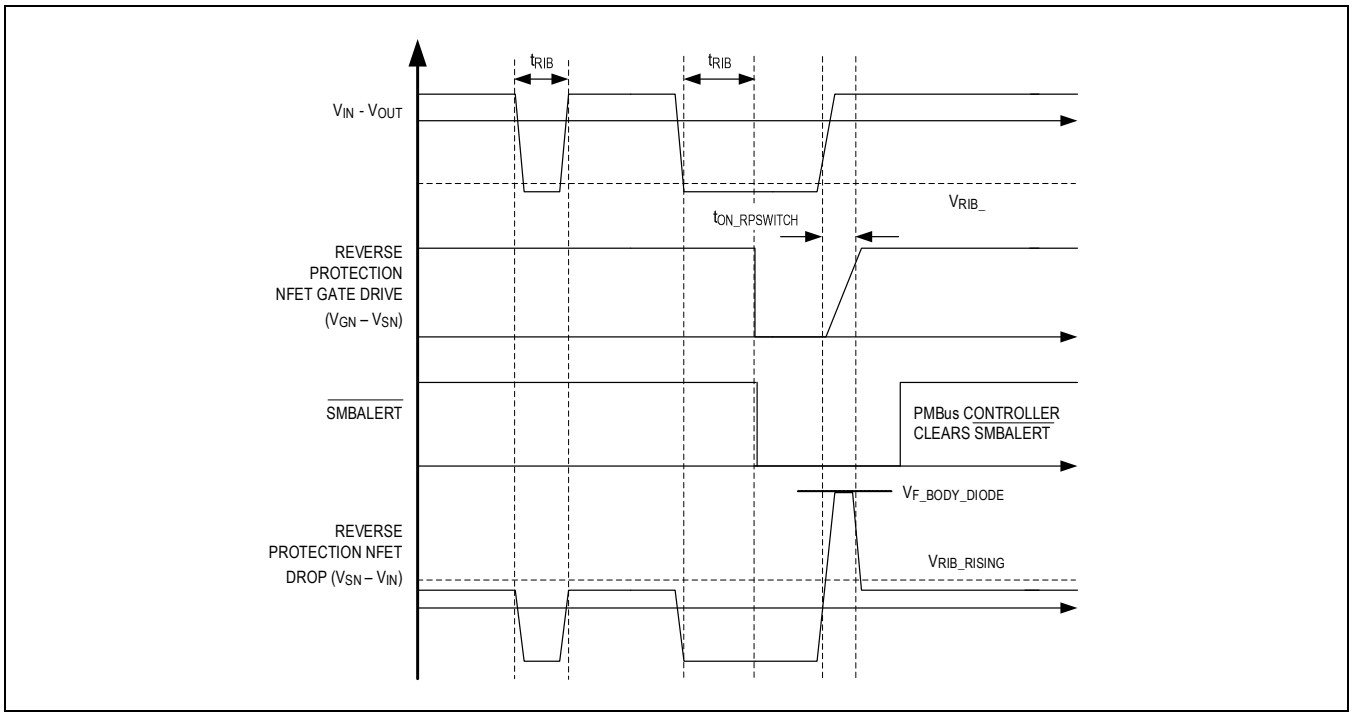


Figure 17. Reverse Current Fault Timing Diagram

Input Voltage Surge Stopping and Output Overvoltage Feedback Regulation (OVFB)

The MAX17616A offers a surge protection feature whereby the output voltage is limited to a programmable voltage level during input voltage surge events. When the input voltage surges above a set threshold, the output overvoltage feedback loop (OVFB) modulates the drain to source resistance of the internal Control nFET and limits the output voltage. A simplified internal block diagram of the overvoltage clamp function is depicted in *Figure 18*.

There is no timer for the OVFB condition. The part can regulate OUT to be below IN indefinitely, depending on load conditions.

1. Part shall operate in OVFB mode as long as no other condition (overcurrent, thermal foldback, etc) kicks in. This is true even if (V_{IN} - V_{OUT}) exceeds V_{FA}, provided only the OVFB condition is present.

2. The OVFB condition may trigger t_{BLANK} (when a consequential thermal foldback condition kicks in), and the part needs to follow programmed CLMODE after t_{BLANK}. As the OVFB threshold is triggered, the $V_{OUT\_OV\_WARNING}$ bit of the STATUS_VOUT register is set high, and $\overline{SMBALERT}$ is asserted.

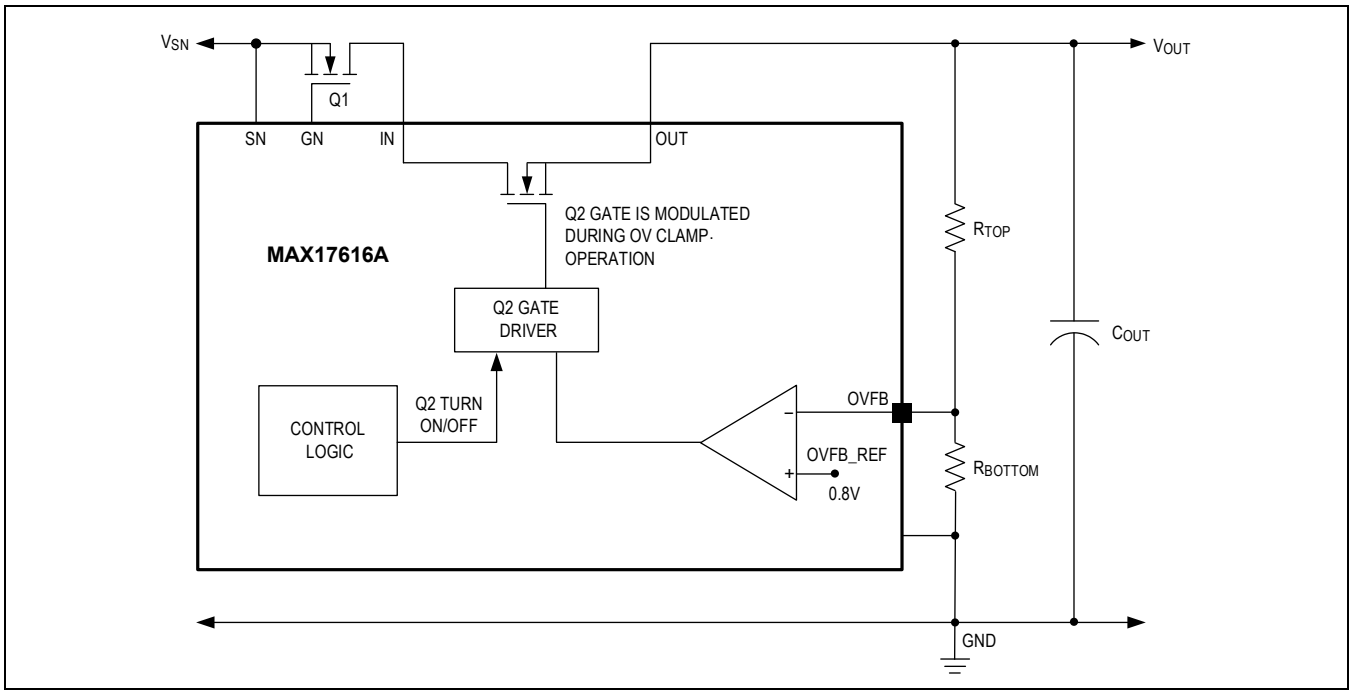


Figure 18. Overvoltage Clamp through OVFB

A typical overvoltage clamp operation and recovery sequence are shown in *Figure 19*.

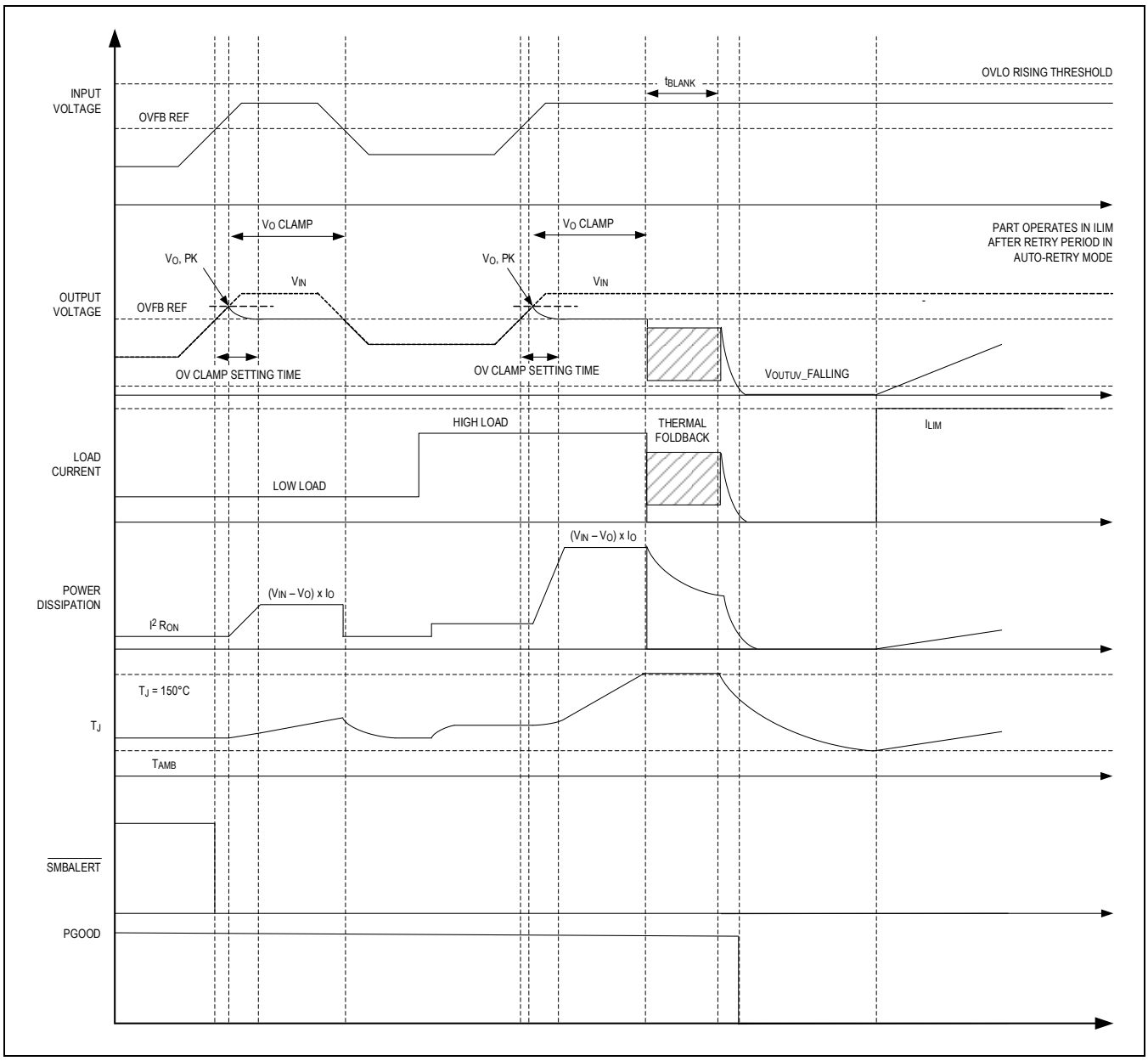


Figure 19. Overvoltage Clamp Operation and Recovery

Figure 20 shows overvoltage clamp response for MAX17616A during an input surge event.

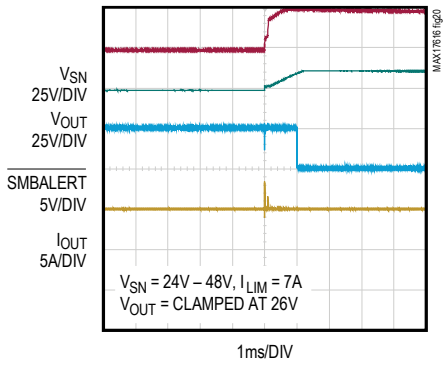


Figure 20. Overvoltage Clamp Response

Input Reverse-Polarity Protection

Input reverse-polarity protection is realized using an external nFET that is controlled by MAX17616/MAX17616A. Due to incorrect wiring on the input power supply terminals, a negative supply can appear on the devices' input pins. Connect an external nFET (Q1) with the source connected to the SN pin, drain to the IN pin, and gate to the GN pin, as shown in the Typical Application Circuits. During an input reverse polarity voltage fault, this external nFET turns OFF and protects the load. The external nFET is also needed for the optional reverse-current protection. If reverse polarity protection and reverse-current protection are not needed, the SN and GN pins must be connected to the IN pin.

The magnitude of reverse-polarity voltage protection is dependent on the operating load bus voltage (V_{OUT}) and the voltage-blocking capability of the external nFET. For example, for protection down to a -55V input voltage with V_{OUT} = 30V, an external nFET rated for 85V is needed. The devices provide a gate drive (GN) of 6.5V (typ). Figure 21 shows the reverse-polarity protection of MAX17616 with V_{OUT} = 0V and V_{SN} = -24V. Figure 22 shows the reverse-polarity protection of MAX17616 with V_{OUT} = +24V and V_{SN} = -24V.

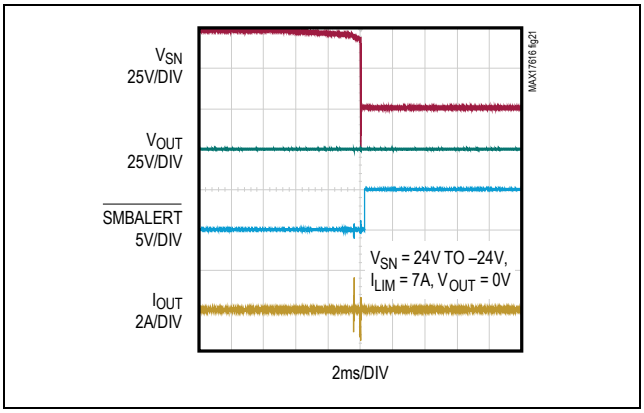


Figure 21. Input Reverse-Polarity Protection at V_{OUT} = 0V and V_{SN} = -24V

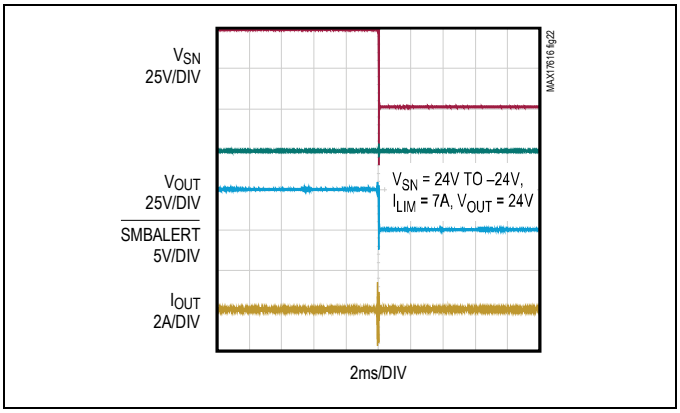


Figure 22. Input Reverse-Polarity Protection at V_{OUT} = +24V and V_{SN} = -24V

Output Reverse-Polarity Protection

MAX17616/MAX17616A protects itself and the input-power connections from accidental reverse output-voltage polarity connections. Reverse output voltage can appear across the OUT and GND pins due to inductive loads or incorrect wiring connections of live loads across the output terminals.

Figure 23 shows the output reverse-polarity protection of the MAX17616 with V_{OUT} = -24V and V_{SN} = 24V and *Figure 24* shows the response with V_{OUT} = -24V, and V_{SN} = 0V. The devices can protect the circuit's negative output voltage up to – (85 – V_{IN}) V. *Figure 25* shows the recovery performance from an output reverse polarity fault condition.

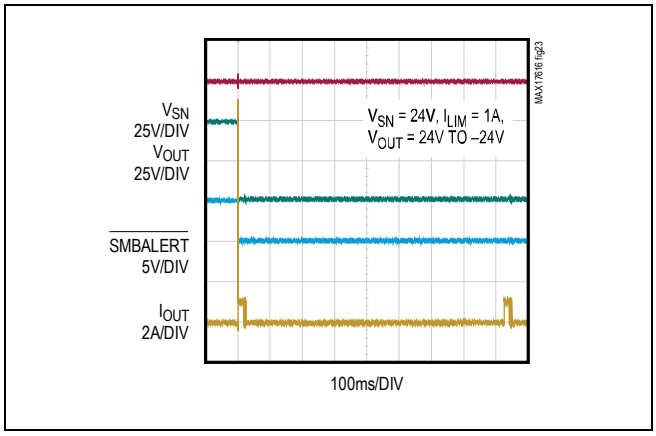


Figure 23. Output Reverse-Polarity Protection with Auto-Retry Mode with V_{OUT} = -24V and V_{SN} = 24V

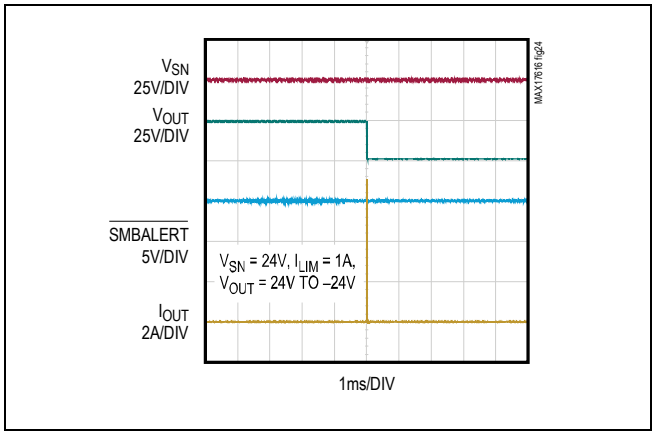


Figure 24. Output Reverse-Polarity Protection with Auto-Retry Mode with V_{OUT} = -24V and V_{SN} = 0V

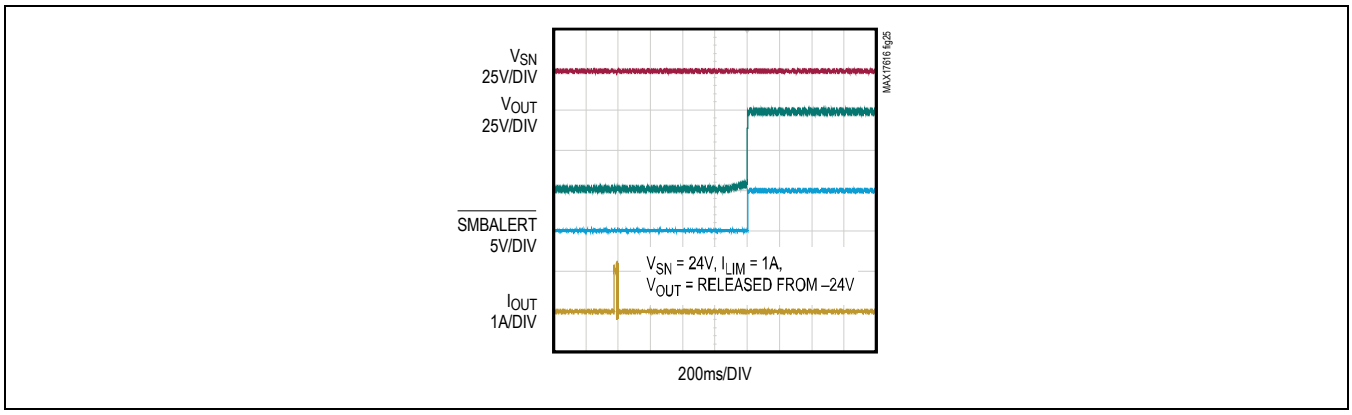


Figure 25. Recovery Performance from an Output Reverse-Polarity Fault with V_{OUT} = -24V Initial Condition and V_{SN} = 24V

Output Undervoltage Sensing (OUTUV)

The devices offer a programmable output undervoltage sensing threshold (OUTUV). When the voltage on the OUT pin falls below the OUTUV falling threshold due to any fault condition, the internal control logic affects a restart cycle with a soft start. If during any fault condition, the output voltage does not fall below the OUTUV falling threshold, then restart cycle is affected without soft-start. This is particularly useful during transient input source fault conditions that do not discharge the output voltage below the programmed OUTUV threshold, where the devices recover without going through a soft-start cycle.

The devices have an OUTUV adjustment range from 3.5V (typ) to 64.8V (typ). OUTUV's rising threshold can be set using the VOUT_UV_FAULT_LIMIT command. OUTUV's falling threshold is 3% below the rising threshold.

Fault Output ($\overline{SMBALERT}$)

The devices offer an open drain fault signal $\overline{SMBALERT}$. The fault signal requires an external pullup resistor and bias supply. The $\overline{SMBALERT}$ pin is asserted low during the following fault conditions:

- Soft Start, when ($V_{IN} – V_{OUT}$) > V_{FA} at the end of t_{STO}.
- Overcurrent and short circuit conditions once the current limit exceeds t_{BLANK} duration.
- Reverse current condition when Reverse Protection external nFET is turned OFF.
- Thermal Shutdown.
- Input UVLO.
- Input OVLO.

The $\overline{SMBALERT}$ shall not be deasserted once the above fault conditions observed by the device are cleared. The PMBus Controller needs to clear the $\overline{SMBALERT}$ signal intentionally by sending the CLEAR_FAULT command.

Table 2 shows the status of the nFETs and the status of the fault signal under various operating conditions.

Table 2. FETs Status During Faults

CONDITION	EXTERNAL nFET STATUS	INTERNAL nFET STATUS	$\overline{SMBALERT}$ STATUS
EN Disabled	OFF	OFF	High
Normal Operation (No Fault)	ON	ON	High
Input UVLO	OFF	OFF	Low
Input OVLO	OFF	OFF	Low
Soft Start (During I_{START}/t_{STO} period)	ON	ON	High
Output Overcurrent	ON	Regulate	Low (After t_{BLANK})
Short Circuit	OFF	OFF	Low
Reverse current with No Other Fault	OFF	ON	Low
Over Voltage Clamp	ON	Regulate	Low
Loss of Ground	OFF	OFF	High
Output Undervoltage	ON	ON	High at power-up until (V_{IN}-V_{OUT}) > V_{FA}. Low after power-up.†
Thermal Regulation	ON	Regulate	High (Automatically low after t_{BLANK} due to current regulation)
Thermal Shutdown	OFF	OFF	Low
SETI Grounded (First Power ON)	OFF	OFF	Low
(V_{IN}-V_{OUT}) > V_{FA} at the end of t_{STO} (during startup)	OFF	OFF	Low
PMBus Fault	OFF	OFF	Low

†*$\overline{SMBALERT}$ behavior on OUTUV fault*.

When the output voltage falls below the value set in the VOUT_UV_FAULT_LIMIT register, the following functions are required:

- $\overline{SMBALERT}$ shall be pulled low with no delay.
- Bit 0 of STATUS_BYTE is set high.
- Bit 0 and Bit 15 of STATUS_WORD are set high.

- Bit 5 of STATUS_VOUT is set high.
- PGOOD is pulled low.

Startup condition: The assertion of output under-voltage fault shall not be active during startup until the "(V_{IN} - V_{OUT}) < V_{FA}" is reached. This includes not asserting $\overline{SMBALERT}$ and not registering any bits until the "(V_{IN} - V_{OUT}) < V_{FA}" condition is satisfied. However, PGOOD shall be active during the startup phase. This is required because the downstream electronics would rely on the PGOOD signal to know that the output voltage of MAX17616/MAX17616A is healthy enough to start their operations.

Linear Regulator (V_{CC})

The MAX17616/MAX17616A has an internal low dropout (LDO) regulator that powers V_{CC} from V_{IN}. This LDO is enabled during power-up or when EN is cycled. The typical V_{CC} output voltage is 1.8V. Bypass V_{CC} to GND with a 2.2µF low-ESR ceramic capacitor.

Gate Driver for Reverse Protection External nFET

The devices offer an integrated gate driver circuit to drive the Reverse Protection external nFET. The gate drive is protected internally from accidental short circuit between the gate and source terminals. The devices provide a gate drive (GN) of 6.5V (typ). The gate drive has passive resistive behavior across gate and source terminals of external nFET when the operation of the devices is disabled by de-asserting EN pin, or through an OPERATION command from the PMBus interface.

If the reverse protection function is not used, and the external nFET is not installed, connect SN and GN terminals to IN pins.

Loss of Ground Protection

The devices protect loads by turning OFF the internal and external nFETs in a loss-of-ground event. A loss-of-ground event can be caused by a break in connectivity between the ground reference of the system control and the IC ground net around MAX17616/MAX17616A. This feature eliminates the requirement for additional external circuits to protect from loss-of-ground events. Additional components are required for the protection of signal pins (EN, IMON, $\overline{SMBALERT}$, PGOOD), as shown in the *Typical Application Circuits*. *Figure 26* shows the typical behavior during a loss-of-ground event.

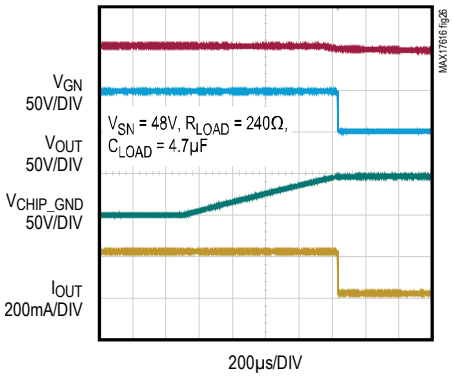


Figure 26. Load Current Interruption During a Loss of Ground Event

Power Good Output (PGOOD/T_J)

The devices include a PGOOD comparator to monitor the status of output voltage and to enable/disable the downstream loads. The power good open-drain output requires an external pullup resistor and bias supply. The functionality of PGOOD is explained as follows.

1) PGOOD goes high when the output voltage exceeds the OUTUV rising threshold and the (V_{IN} - V_{OUT}) < V_{FA} condition is satisfied.
2) PGOOD goes low when the output voltage falls below the OUTUV falling threshold.
3) At system power-up, PGOOD remains high if V_{OUT} > V_{OUTUV} and (V_{IN} - V_{OUT}) < V_{FA}; otherwise, it is low.

Die Temperature Monitoring (PGOOD/T_J)

The devices offer a die temperature monitoring feature. Connect a 10kΩ ~ 20kΩ resistor from PGOOD/T_J to GND to monitor the internal die temperature on the PGOOD/T_J pin.

The PGOOD/T_J pin provides 652mV at 25°C and 854mV at +125°C of die (hot spot) temperature, with a temperature slope of 2mV/°C. The die (hot spot) temperature is expressed using the following equation:

$$V_{TJ} = (T_{DIE} - 25°C) \times 2mV + 652mV$$

$$T_{DIE} = \frac{V_{TJ} - 652mV}{2mV} + 25°C$$

where,

T_{DIE} is the die temperature,

V_{TJ} is the voltage at the pin PGOOD/T_J.

Thermal Shutdown Protection

The devices have a thermal-shutdown feature to protect against overheating, and a thermal foldback current limit control. When the junction temperature reaches 150°C (typ), the current limit is internally lowered to reduce the power dissipation on the internal nFET, and regulate the junction temperature at around 150°C. In extreme conditions, the devices turn off and assert the $\overline{\text{SMBALERT}}$ pin when the junction temperature exceeds +165°C (typ). The devices exit thermal shutdown and resume normal operation after the junction temperature cools by 20°C (typ), except when in a latch-off mode, where the devices remain latched off.

PMBus Interface

The devices support the PMBus interface. From a software perspective, the devices can execute a subset of PMBus commands. The devices use the SMBus version 3.1 for transport protocol and respond to the SMBus devices address. In this datasheet, the term SMBus refers to the electrical characteristics of the PMBus communication using the SMBus physical layer. The term PMBus refers to the PMBus command protocol. The devices employ standard SMBus protocols (see *Figure 27*) to read monitored data, warning/faults, and provide access to all manufacturer-specific commands.

Figure 27 uses the following abbreviations:

S: Start Condition

Sr: Repeated Start Condition

P: Stop Condition

R: Read Byte

W: Write Byte

A: Acknowledge Bit

N: Not Acknowledge Bit

The acknowledge bit is active low if the transmitted byte is received successfully by a device. If the receiving device is the bus controller, the acknowledge bit for the last byte read is high and indicated by the N (Not Acknowledge) bit.

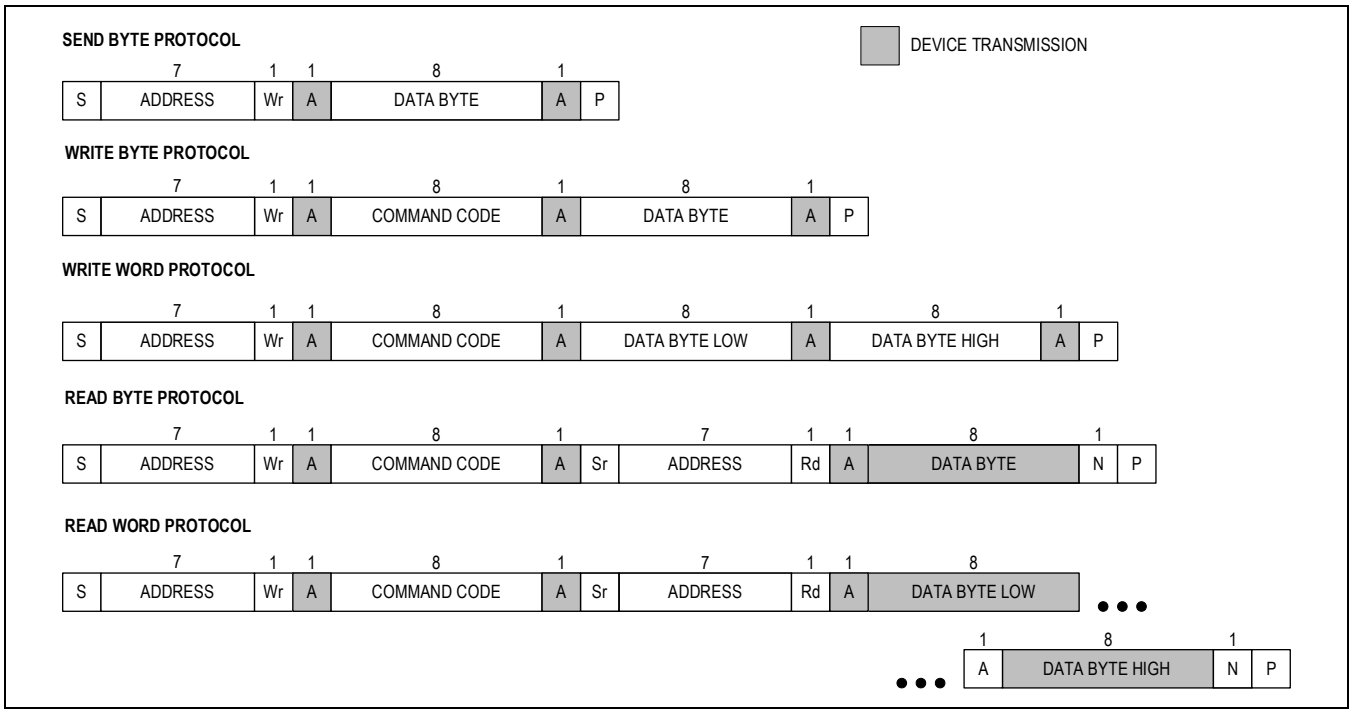


Figure 27. SMBus Command Protocols

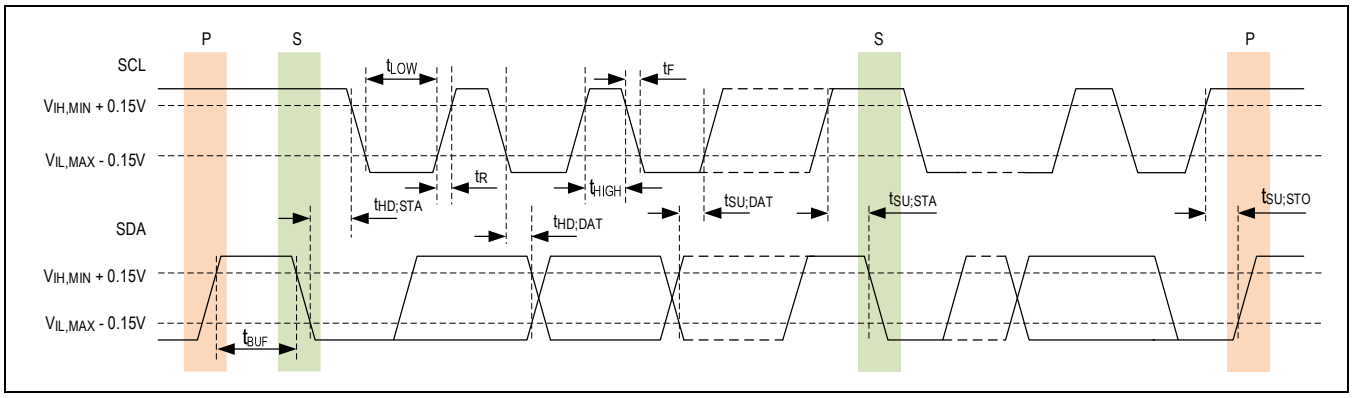


Figure 28. SMBus Timing Measurements

In Power Distribution Architectures with the Controllers powered by an upstream power supply, the devices can be initialized to accept control commands and read commands (See *Figure 29*). In this architecture, the Controller can Enable and turn ON/OFF the device from the Controller.

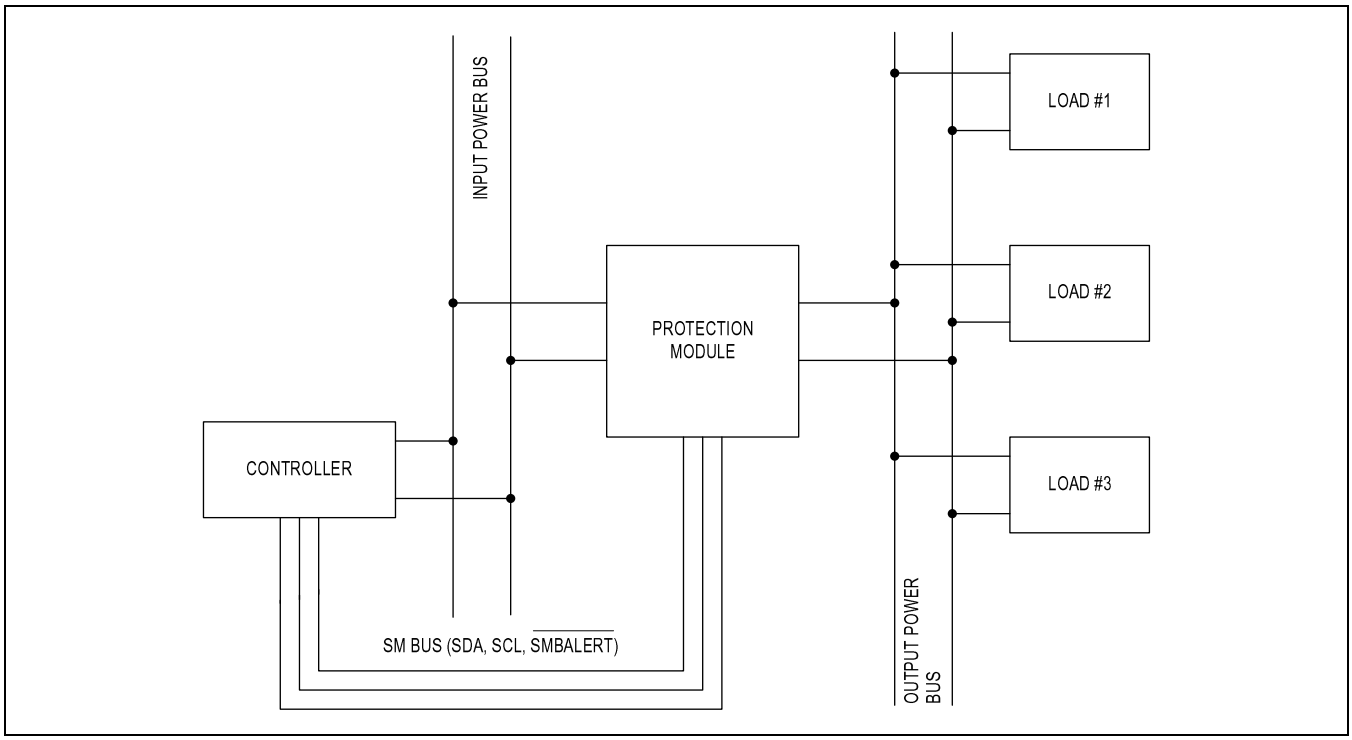


Figure 29. System Architecture

Device Addressing and Reverse Protection (Q1) Decoding

ADDR/Q1 pin is available for setting the physical PMBus address of the device. The PMBus address is 7 bits long. The upper 3 bits (MSBs) are set as **001**†, and the lower four bits can be configured through this pin. During the initial power-up sequence, the ADDR/Q1 pin sends a 10µA/400µA current, and the voltage at the ADDR/Q1 pin is sensed to get the value of the resistor connected to the pin. ADDR/Q1 pin is also used to program if the external reverse protection nFET (Q1) is being used or not. Based on the resistor value, the address is set as shown in *Table 3* (Resistor Values for setting PMBus Address).

Of all the addresses, 00h is reserved for broadcast to all the devices connected to the bus. Hence, 15 devices can be configured with different device addresses on the same bus.

See *Table 3* for the address set by the pins. Note that the presence or absence of reverse protection nFET (Q1) is not announced on the PMBus physical address. Hence, programming resistors from 24.3Ω to 1.87kΩ will give out the same physical PMBus address as programming resistors from 3.16kΩ to 86.6kΩ.

† *The default address space is, therefore, 001.0001 to 001.1111.*
MSB=000 has been dropped to avoid conflict with reserved ARA address 000.1100.

Table 3. Resistor Values for setting PMBus Address

RESISTOR VALUE E96 1% [Ω]	LOW NIBBLE IN DECIMAL FORMAT	PMBus ADDRESS	EXTERNAL REVERSE PROTECTION nFET Q1
RESERVED FOR BROADCAST		0000000	–
24.3	1	0010001	No
78.7	2	0010010	No
147.0	3	0010011	No
226.0	4	0010100	No
309.0	5	0010101	No
402.0	6	0010110	No
499.0	7	0010111	No
604.0	8	0011000	No
732.0	9	0011001	No
866.0	10	0011010	No
1000	11	0011011	No
1210	12	0011100	No
1400	13	0011101	No
1620	14	0011110	No
1870	15	0011111	No
3160	1	0010001	Yes
5760	2	0010010	Yes
9090	3	0010011	Yes
12400	4	0010100	Yes
16200	5	0010101	Yes
20000	6	0010110	Yes
24300	7	0010111	Yes
28700	8	0011000	Yes
34800	9	0011001	Yes
41200	10	0011010	Yes
48700	11	0011011	Yes
56200	12	0011100	Yes
64900	13	0011101	Yes
75000	14	0011110	Yes
86600	15	0011111	Yes

DIRECT Data Format

The devices use DIRECT Data format to report input voltage, output voltage, output current, and temperature. The DIRECT format is used for any value:

$$X = \frac{1}{m}\, x\, (Y.10^{-R} - b)$$

where
X is the real-world value.
Y is a two-byte 2's complement integer sent over the bus.
m is the slope coefficient, a two-byte 2's complement integer.
b is the offset, a two-byte 2's complement integer.
R is the exponent, a one-byte 2's complement integer.

Output data is a 2-byte word, the first 12 bits of which contain the Y value that can be converted into the real-world quantity by using the above formula and the following coefficients:

	UNIT	m	R	b	MAX ERROR[1]
V_{IN} or V_{OUT}	V	512	-1	-18	3.5% @ 3V
I_{OUT}[2]	A	5845	-1	80	6% @ 0.7A
Die Temperature	°C	71	-1	19653	9°C @ 25°C

[1] includes analog readout, ADC conversion (10bit ENOB), and DIRECT conversion.

[2] current is measured as voltage on IMON pin. The considered range is 124.8mV to 1.25V, corresponding to 0.7A to 7A with R_IMON = 3.8kΩ.

PMBus Commands

The devices support the following subset of commands defined in the Power System Management Protocol Specification Part II – Command Language Revision 1.3.1. For detailed specifications and the complete list of PMBus commands, refer to Part II of the PMBus specification available at *pmbus.org*.

Table 4. PMBus Commands used in MAX17616 and MAX17616A

COMMAND CODE	COMMAND NAME	COMMAND DESCRIPTION	TRANSACTION TYPE	NO. OF BYTES	SCALING FACTOR (N)
01h	OPERATION	Retrieves or stores the operation status.	R/W Byte	1	–
03h	CLEAR_FAULTS	Clears any fault bits that have been set. This command clears all bits in all status registers simultaneously.	Send Byte	0	–
19h	CAPABILITY	Retrieves the device capability.	Read Byte	1	–
1Bh	SMBALERT_MASK	Stores $\overline{\text{SMBALERT}}$ fault mask.	Block Write-Block Read Process Call	1	–
44h	VOUT_UV_FAULT_LIMIT	Retrieves or stores output undervoltage fault threshold.	R/W Byte	1	–
78h	STATUS_BYTE	Returns one-byte information about the part operating status.	Read Byte	1	–

COMMAND CODE	COMMAND NAME	COMMAND DESCRIPTION	TRANSACTION TYPE	NO. OF BYTES	SCALING FACTOR (N)
79h	STATUS_WORD	Returns two bytes of information with a summary of the fault conditions.	Read Word	2	–
7Ah	STATUS_VOUT	Returns one byte of information about the status of the output voltage.	Read Byte	1	–
7Bh	STATUS_IOUT	Returns one byte of information about the status of the output current.	Read Byte	1	–
7Ch	STATUS_INPUT	Returns one byte of information about the status of the input.	Read Byte	1	–
7Dh	STATUS_TEMPERATURE	Returns one byte of information about the status of the temperature.	Read Byte	1	–
7Eh	STATUS_CML	Retrieves information about communications status.	Read Byte	1	–
80h	STATUS_MFR_SPECIFIC	Returns two bytes of information about specific fault conditions.	Read Byte	1	–
88h	READ_VIN	Returns measured input voltage value on SN pin.	Read Word	2	See Note 1
8Bh	READ_VOUT	Returns measured output voltage value on OUT pin.	Read Word	2	See Note 1
8Ch	READ_IOUT	Returns measured output current	Read Word	2	See Note 1
8Dh	READ_TEMPERATURE_1	Returns measured temperature value.	Read Word	2	See Note 1
98h	PMBus_REVISION	Returns revision of PMBus specification to which the device is compliant.	Read Byte	1	–
99h	MFR_ID	Returns manufacturer ID in ASCII.	Read Byte	6	–
9Ah	MFR_MODEL	Returns part number in ASCII.	Read Byte	10	–
9Bh	MFR_REVISION	Returns part revision letter or number in ASCII.	Read Byte	3	–
C4h	SET_CLMODE	Retrieves or stores the response mode during a fault.	R/W Byte	1	–
C5h	SET_ISTART_RATIO	Retrieves or stores ISTART_RATIO value.	R/W Byte	1	–
C6h	SET_TSTOC	Retrieves or stores the short-term overcurrent limit time.	R/W Byte	1	–
C7h	SET_ISTLIM	Retrieves or stores the short-term overcurrent limit.	R/W Byte	1	–
ADh	IC_DEVICE_ID		Read Byte	10	
AEh	IC_DEVICE_REV		Read Byte	3	

Note 1: See the DIRECT Data Format Section.

OPERATION

- Command Code: 01h
- Number of data bytes: 1
- Number of bits used: 1/8
- Protocol: Read Byte/Write Byte

The OPERATION command is used to configure the operational state of the controller, if the EN pin is high. The OPERATION command turns the PMBus device output on and off with commands sent over the PMBus.

EN PIN	BIT NUMBER		DEVICE STATE/ RESPONSE	INTERNAL CIRCUITRY OF MAX17616/MAX17616A	PMBus INTERFACE	Q1/Q2 STATUS
	7	[6:0]	ON/OFF			
LOW	X	XX	OFF	Low I_Q mode; Control circuits OFF	Disabled	OFF
HIGH	0	XX	OFF	Normal operation	Active	OFF
HIGH	1	XX	ON	Normal operation	Active	Operation enabled

If a PMBus device receives an OPERATION command data byte that attempts to configure or operate the device in an unsupported manner, then the device shall treat this as invalid data and declare a communications fault.

Bits [6:0] shall be set to 0000000 internally. Bit [7] shall be set to 1 as default.

CLEAR_FAULT

- Command Code: 03h
- Number of data bytes: N/A
- Number of bits used: N/A
- Protocol: Send Byte

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its $\overline{\text{SMBALERT}}$ signal output if the device is asserting the $\overline{\text{SMBALERT}}$ signal.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. Units that have shut down for a fault condition are restarted.

If the fault is still present when the bit is cleared, the fault bit shall immediately be set again, and the host will be notified by the usual means.

This command is write only. There is no data byte for this command.

CAPABILITY

- Command Code: 19h
- Number of data bytes: 1
- Number of bits used: 4/8
- Protocol: Read Byte

This command provides a way for a host system to determine some key capabilities of the device. The CAPABILITY command returns the information about the device, as shown in the following table.

BITS	DESCRIPTION	MEANING	DEFAULT VALUE
7	Packet Error Checking	The bit is set to 1 if Packet Error Checking (PEC) is supported.	1
6:5	Maximum Bus Speed	00: 100kHz 01: 400kHz 10: 1MHz 11: Reserved	10
4	$\overline{\text{SMBALERT}}$	The bit is set to 1 if the device has an $\overline{\text{SMBALERT}}$ pin and supports the SMBus Alert response protocol.	1
3:0	–	Not supported.	0000

SMBALERT_MASK

- Command Code: 1Bh
- Number of data bytes: 1
- Number of bits used: 8/8
- Protocol: Block Write–Block Read Process Call

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the $\overline{\text{SMBALERT}}$ signal.

The command format is used to block a status bit or bits from causing the $\overline{\text{SMBALERT}}$ signal to be asserted, as shown in *Figure 30*. The bits in the mask byte align with the bits in the corresponding status register. For example, if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an overtemperature warning condition would be blocked from asserting $\overline{\text{SMBALERT}}$.

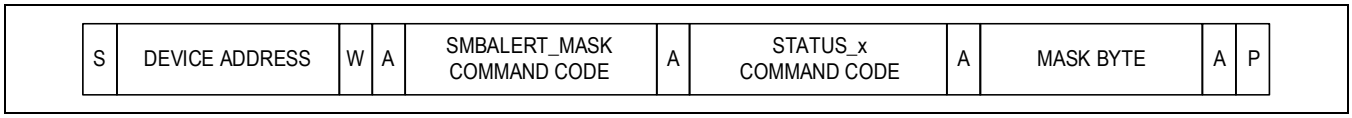


Figure 30. Block Write-Block Read Process Call

VOUT_UV_FAULT_LIMIT

- Command Code: 44h
- Number of data bytes: 1
- Data Format: bit_field
- Protocol: Read Byte/Write Byte

The VOUT_UV_FAULT_LIMIT command sets or retrieves the undervoltage threshold on output in voltage. See the following table to set the values for the OUTUV threshold.

BITS	DESCRIPTION	MEANING	DEFAULT VALUE
7:5	NA		
4:2	Nominal voltage selection	000 5V 001 9V 010 12V 011 24V 100 36V 101 48V 110 60V 111 72V	000
1:0	PGOOD **rising** threshold selection	00 -10% 01 -20% 10 -30%	00

The OUTUV falling threshold will be automatically set 3% below the rising one.

STATUS_BYTE

- Command Code: 78h
- Number of data bytes: 1
- Number of bits used: 6/8
- Protocol: Read Byte

The STATUS_BYTE command returns one byte of information with a summary of the unit's fault condition. Based on the information in this byte, the host can get more information by reading the appropriate status registers.

The STATUS_BYTE message content is shown in the following table:

BIT	NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond. Not used. Reserved bit.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output over-voltage fault has occurred. Not used.
4	IOUT_OC_FAULT	An output over-current fault has occurred.
3	VIN_UV_FAULT	An input under-voltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF ABOVE	A fault or warning not listed in bits [7:1] of this byte has occurred.

STATUS_WORD

Command Code: 79h

- Number of data bytes: 2
- Number of bits used: 11/16
- Protocol: Read Word

The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers.

The STATUS_WORD message content is shown in the following table:

BYTE	BIT	NAME	MEANING
LOW	7	BUSY	A fault was declared because the device was busy and unable to respond. Not used. Reserved bit.
	6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
	5	VOUT_OV_FAULT	An output over-voltage fault has occurred. Not used.
	4	IOUT_OC_FAULT	An output over-current fault has occurred.
	3	VIN_UV_FAULT	An input under-voltage fault has occurred.
	2	TEMPERATURE	A temperature fault or warning has occurred.
	1	CML	A communications, memory, or logic fault has occurred.
	0	NONE OF ABOVE	A fault or warning not listed in bits [7:1] of this byte has occurred.

BYTE	BIT	NAME	MEANING
HIGH	7	V_{OUT}	An output voltage fault or warning has occurred.
	6	I_{OUT}/P_{OUT}	An output current or output power fault or warning has occurred.
	5	INPUT	An input voltage, input current, or input power fault or warning has occurred.
	4	MFR	A manufacturer-specific fault or warning has occurred.
	3	POWER_GOOD	Not supported, always 0.
	2	FANS	Not supported, always 0.
	1	OTHER	Not supported, always 0.
	0	STARTUP	Asserted during STARTUP (before V_{OUT} reaches V_{IN} - V_{FA}), it is set to 0 after STARTUP is complete.

Note: The IOUT_OC_FAULT and I_{OUT}/P_{OUT} bits shall be set only after a delay of t_{STOC}.

STATUS_VOUT

- Command Code: 7Ah
- Number of data bytes: 1
- Number of bits used: 2/8
- Protocol: Read Byte

The STATUS_VOUT command returns one byte of information with a summary of the unit's output voltage fault condition.

The STATUS_VOUT message content is shown in the following table:

BIT	NAME	MEANING
7	VOUT_OV_FAULT	Not supported, always 0.
6	VOUT_OV_WARNING	An output regulation event has occurred (valid only with the OVFB part variant).
5	VOUT_UV_WARNING	Output has gone below the OUTUV threshold.
4	VOUT_UV_FAULT	Not supported, always 0.
3	VOUT_MAX_WARNING	Not supported, always 0.
2	TON_MAX_FAULT	Not supported, always 0.
1	TOFF_MAX_WARNING	Not supported, always 0.
0	VOUT Tracking Error	Not supported, always 0.

STATUS_IOUT

- Command Code: 7Bh
- Number of data bytes: 1
- Number of bits used: 2/8
- Protocol: Read Byte

The STATUS_IOUT command returns one data byte with information about the fault conditions related to the output current.

The STATUS_IOUT message content is shown in the following table:

BIT	MEANING
7	An output overcurrent fault has occurred.
6	An output overcurrent and low voltage fault has occurred simultaneously. (output overcurrent = part entered current limit operation, Low voltage fault = UVLO fault).
5	An output overcurrent warning has occurred ($I_{LIM} < I_{OUT} < I_{STLIM}$). Not used.
4	Not supported, always 0.
3	Not supported, always 0.
2	Not supported, always 0.
1	Not supported, always 0.
0	Not supported, always 0.

Note: During an overcurrent fault, bits [7:6] shall be set only after a delay of t_{STOC}. During an overcurrent fault, bit [5] shall be set when the OUT current exceeds I_{LIM}.

STATUS_INPUT

- Command Code: 7Ch
- Number of data bytes: 1
- Number of bits used: 2/8
- Protocol: Read Byte

The STATUS_INPUT command returns one byte of information with a summary of the unit's input fault condition.

The STATUS_INPUT message content is shown in the following table:

BIT	NAME	MEANING
7	VIN_OV_FAULT	An input over-voltage fault has occurred.
6	VIN_OV_WARNING	Not supported, always 0.
5	VIN_UV_WARNING	Not supported, always 0.
4	VIN_UV_FAULT	An input under-voltage fault has occurred.
3	Unit Off for Insufficient Input Voltage	Not supported, always 0.
2	IIN_OC_FAULT	Not supported, always 0.
1	IIN_OC_WARNING	Not supported, always 0.
0	PIN_OP_WARNING	Not supported, always 0.

STATUS_TEMPERATURE

- Command Code: 7Dh
- Number of data bytes: 1
- Number of bits used: 1/8
- Protocol: Read Byte

The STATUS_TEMPERATURE command returns one byte of information with a summary of the unit's temperature fault condition.

The STATUS_TEMPERATURE message content is shown in the following table:

BIT	NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	Not supported, always 0.
5	UT_WARNING	Not supported, always 0.
4	UT_FAULT	Not supported, always 0.
3	Reserved	Not supported, always 0.
2	Reserved	Not supported, always 0.
1	Reserved	Not supported, always 0.
0	Reserved	Not supported, always 0.

STATUS_CML

- Command Code: 7Eh
- Number of data bytes: 1
- Number of bits used: 5/8
- Protocol: Read Byte

The STATUS_CML command returns one data byte with information about the fault conditions related to communication.

The STATUS_CML message content is shown in the following table:

BIT	MEANING
7	Invalid or unsupported Command Received.
6	Invalid or unsupported Data Received.
5	Packet Error Check Failed.
4	Memory Error Detected.
3	Not supported.
2	Not supported.
1	A communication fault other than the ones listed in this table has occurred.
0	Not supported.

STATUS_OTHER

- Command Code: 7Fh
- Number of data bytes: 1
- Number of bits used: 0/8
- Protocol: Read Byte

This command is used to identify the device that asserted $\overline{\text{SMBALERT}}$ first. Not supported. For future use always 0.

STATUS_MFR_SPECIFIC

- Command Code: 80h
- Number of data bytes: 1
- Number of bits used: 4/8
- Protocol: Read Byte

The STATUS_MFR_SPECIFIC command returns one data byte with information about specific fault conditions shown in the following table:

BIT	MEANING
7	SETI Pin fault.
6	IMON Pin fault. Not supported.
5	The soft start failed.
4	Not Used.
3	An output short circuit fault has occurred.
2	A reverse current fault has occurred.
1	Not supported, always 0.
0	Not supported, always 0.

Note: Bit [7:6] shall be set only after a delay of t_{STOC}, after an overcurrent fault.

READ_VIN

- Command Code: 88h
- Number of data bytes: 2
- Data Format: DIRECT
- Protocol: Read Word

The READ_VIN command returns the input voltage measured at the SN pin in Volt. The two data bytes are encoded in DIRECT format.

The input voltage range is 3V to 80V. See the *Direct Data Format* section for input voltage scaling.

READ_VOUT

- Command Code: 8Bh
- Number of data bytes: 2
- Data Format: DIRECT
- Protocol: Read Word

The READ_VOUT command returns the actual, measured output voltage at the OUT pin in Voltage. The two data bytes are encoded in DIRECT format.

The output voltage range is 3V to 80V. See the DIRECT Data Format section for output voltage scaling.

READ_IOUT

- Command Code: 8Ch
- Number of data bytes: 2
- Data Format: DIRECT
- Protocol: Read Word

The READ_IOUT command returns the measured current across the internal control nFET in A. The two data bytes are encoded in DIRECT format.

The output current range is 0A to 7A. See the *Direct Data Format* section for output current scaling.

READ_TEMPERATURE_1

- Command Code: 8Dh
- Number of data bytes: 2
- Data Format: DIRECT
- Protocol: Read Word

The READ_TEMPERATURE_1 command returns the measured output temperature in degrees Celsius. The two data bytes are encoded in DIRECT format.

The temperature range is -40°C to +150°C. See the *Direct Data Format* section for temperature scaling.

PMBus_REVISION

- Command Code: 98h
- Number of data bytes: N/A
- Number of bits used: N/A
- Protocol: Read Byte

PMBus_REVISION command stores or reads the revision of the PMBus to which the device is compliant.

The command has one data byte. Bits [7:4] indicate the revision of PMBus specification Part I to which the device is compliant. Bits [3:0] indicate the revision of PMBus specification Part II to which the device is compliant. The command returns 33h, which corresponds to Revision 1.3 of Part I and Part II.

MFR_ID

- Command Code: 99h
- Number of data bytes: 6
- Protocol: Read Byte

The MFR_ID command is used to either set or read the manufacturer's ID (name, abbreviation, or symbol that identifies the unit's manufacturer). Each manufacturer chooses their identifier. MFR_ID is typically only set once at the time of manufacture.
The MFR_ID for the MAX17616/MAX17616A is "0x 05 4D 41 58 49 4D".

MFR_MODEL

- Command Code: 9Ah
- Number of data bytes: 10
- Protocol: Read Byte

The MFR_MODEL command is used to either set or read the manufacturer's model number. MFR_MODEL is typically set once, at the time of manufacture.

The manufacturer ID for the MAX17616 is "0x 09 4D 41 58 31 37 36 31 36 20".

The manufacturer ID for the MAX17616A is "0x 09 4D 41 58 31 37 36 31 36 41".

MFR_REVISION

- Command Code: 9Bh
- Number of data bytes: 3
- Protocol: Read Byte

The MFR_REVISION command is used to either set or read the manufacturer's revision number. Each manufacturer uses the format of their choice for the revision number. MFR_REVISION is typically set at the time of manufacture or if the device is updated to a later revision.

The model review for the MAX17616/MAX17616A is "02 30 31".

IC_DEVICE_ID

- Command Code: ADh
- Number of data bytes: 10
- Protocol: Read-only Byte

The IC_DEVICE_ID command is used to read the manufacturer's model number.

The manufacturer ID for the MAX17616 is "0x 09 4D 41 58 31 37 36 31 36 20".

The manufacturer ID for the MAX17616A is "0x 09 4D 41 58 31 37 36 31 36 41".

IC_DEVICE_REV

- Command Code: AEh
- Number of data bytes: 3
- Protocol: Read-only Byte

The IC_DEVICE_REV command is used to read the manufacturer's revision number. Each manufacturer uses the format of their choice for the revision number.

The model review for the MAX17616/MAX17616A is "02 30 31".

SET_CLMODE

- Command Code: C4h
- Number of data bytes: 1
- Number of bits used: 2/8
- Protocol: Read Byte/Write Byte

The SET_CLMODE mode command is used to set the mode of operation during a fault. For Auto-retry mode, [7:6] is set to 0b10. For Latch-off mode, bit [7:6] is set to 0b00. For Continuous mode, bit [7:6] is set to 0b01.

Bit [5:0] are set to 0. The default value of bits [7:6] is set to 0b10.

SET_ISTART_RATIO

- Command Code: C5h
- Number of data bytes: 1
- Number of bits used: 4/8
- Protocol: Read byte/Write byte

The SET_ISTART_RATIO command is used to set the current limit ratio during start-up, as a function of the current limit (ILIM) programmed using the SETI pin resistor. See the following table to set the current limit ratio:

BIT [7:3]	BIT [3:0]	CURRENT LIMIT DURING START-UP
XXXXX	000	I_{LIM}
XXXXX	001	I_{LIM} x 1/2
XXXXX	010	I_{LIM} x 1/4 [Default selection]
XXXXX	011	I_{LIM} x 1/8
XXXXX	100	I_{LIM} x 1/16

SET_TSTOC

- Command Code: C6h
- Number of data bytes: 1
- Number of bits used: 2/8
- Protocol: Read Byte/Write Byte

The SET_TSTOC mode command is used to set the time for the short-term overcurrent limit. See the following table to set t_{STOC}.

BIT [7:2]	BIT [1:0]	t_{STOC}
XXXXXX	00	400µs [Default selection]
XXXXXX	01	1ms
XXXXXX	10	4ms
XXXXXX	11	24ms

SET_ISTLIM

- Command Code: C7h
- Number of data bytes: 1
- Number of bits used: 2/8
- Protocol: Read Byte/Write Byte

The SET_ISTLIM mode command is used to set the short-term overcurrent limit ratio. See the following table to set ISTLIM.

BIT [7:2]	BIT [1:0]	ISTLIM
XXXXXX	00	1.25:1
XXXXXX	01	1.50:1
XXXXXX	10	1.75:1
XXXXXX	11	2.00:1 [Default selection]

Fault Management

For reporting faults/warnings to the controller on a real-time basis, the MAX17616 and MAX17616A assert the open-drain $\overline{\text{SMBALERT}}$ pin and set the appropriate bit in the STATUS_WORD register. $\overline{\text{SMBALERT}}$ is used in conjunction with the SMBus Alert Response Address (ARA).

On recognition of the $\overline{\text{SMBALERT}}$ assertion, the controller is expected to access all devices through an Alert Response Address (ARA). Only the device(s) that pulled $\overline{\text{SMBALERT}}$ low will acknowledge the Alert Response Address. The host performs a modified Receive Byte operation. The 7-bit device address provided by the device transmit device is placed in the 7 most significant bits of the byte. The eighth bit can be a zero or one.

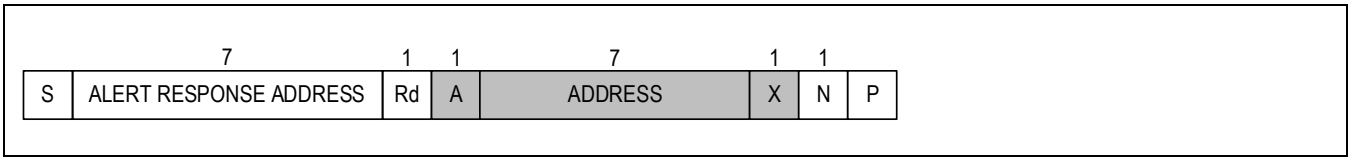


Figure 31. A 7-Bit Addressable Device Response to an ARA

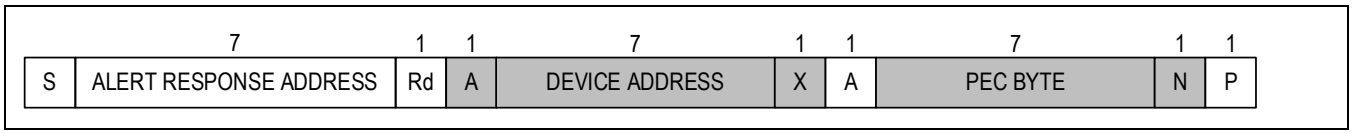


Figure 32. A 7-Bit Addressable Device Response to an ARA with PEC

If more than one device pulls $\overline{\text{SMBALERT}}$ low, the highest priority (lowest address) device will win communication rights via standard arbitration during the device address transfer. After receiving an acknowledge bit from the controller in response to its address, that device must stop pulling down on the $\overline{\text{SMBALERT}}$ signal. If the host still sees $\overline{\text{SMBALERT}}$ low when the message transfer is complete, it knows to read the ARA again. A host that does not implement the $\overline{\text{SMBALERT}}$ signal may periodically access the ARA.

Faults/warnings are cleared when any CLEAR_FAULTS command is received.

See the following table to see the fault mapping:

COMMAND	BIT	NAME	INPUT UVLO	INPUT OVLO	OUTPUT UVLO	OVFB	OUTPUT OVERCURRENT (V_{FA})	REVERSE CURRENT	SHORT CIRCUIT (I_{OUT} > OCP)	THERMAL SHUTDOWN	SETI FAULT	PMBUS FAULT	OTHER
STATUS WORD	15	V_{OUT}			x	x							
	14	I_{OUT}/P_{OUT}					x						
	13	INPUT	x	x									
	12	MFR						x	x		x		
	11	POWER_GOOD											NOT USED
	10	FANS											NOT USED
	9	OTHER											NOT USED
	8	UNKNOWN											NOT USED
	7	BUSY											NOT USED
	6	OFF											
	5	VOUT_OV_FAULT											
	4	IOUT_OC_FAULT					x						
	3	VIN_UV_FAULT	x										
	2	TEMPERATURE								x			
	1	CML										x	
	0	NONE OF ABOVE		x	x	x		x	x		x		
STATUS BYTE	7	BUSY											NOT USED
	6	OFF											
	5	VOUT_OV_FAULT											

COMMAND	BIT	NAME	INPUT UVLO	INPUT OVLO	OUTPUT UVLO	OVFB	OUTPUT OVERCURRENT (V_{FA})	REVERSE CURRENT	SHORT CIRCUIT (I_{OUT} > OCP)	THERMAL SHUTDOWN	SETI FAULT	PMBUS FAULT	OTHER
	4	IOUT_OC_FAULT					x						
	3	VIN_UV_FAULT	x										
	2	TEMPERATURE								x			
	1	CML										x	
	0	NONE OF ABOVE		x	x	x		x	x		x		
STATUS VOUT	7	VOUT_OV_FAULT											
	6	VOUT_OV_ WARNING				x							
	5	VOUT_UV_ WARNING			x								
	4	VOUT_UV_FAULT											NOT USED
	3	VOUT_MAX_MIN											NOT USED
	2	TON_MAX_FAULT											NOT USED
	1	TOFF_MAX_ WARNING											NOT USED
	0	VOUT Tracking Error											NOT USED
STATUS INPUT	7	VIN_OV_FAULT		x									
	6	VIN_OV_WARNING											NOT USED
	5	VIN_UV_WARNING											NOT USED
	4	VIN_UV_FAULT	x										
	3	Unit Off For Insufficient Input Voltage											NOT USED
	2	IIN_OC_FAULT (Input Overcurrent Fault)											NOT USED
	1	IIN_OC_WARNING (Input Overcurrent Warning)											NOT USED
	0	PIN_OP_WARNING (Input Overpower Warning)											NOT USED

COMMAND	BIT	NAME	INPUT UVLO	INPUT OVLO	OUTPUT UVLO	OVFB	OUTPUT OVERCURRENT (V_{FA})	REVERSE CURRENT	SHORT CIRCUIT (I_{OUT} > OCP)	THERMAL SHUTDOWN	SETI FAULT	PMBUS FAULT	OTHER
STATUS IOUT	7	Output overcurrent fault					x						After T_{BLANK}
	6	Output overcurrent and low-voltage fault			x								Set when Output overcurrent and Output undervoltage
	5	Output overcurrent warning											NOT USED
	4	Output undercurrent fault											NOT USED
	3	Current share fault											NOT USED
	2	The device is operating in power-limiting mode											NOT USED
	1	Output overpower fault											NOT USED
	0	Output overpower warning											NOT USED
STATUS MFR SPECIFIC	7	SETI fault									x		
	6	Not Used											NOT USED
	5	Not Used											NOT USED
	4	Not Used											NOT USED
	3	Output Short Circuit							x				
	2	Reverse Current						x					
	1	**RFU**											NOT USED
	0	**RFU**											NOT USED
STATUS TEMPERATURE	7	OT_FAULT (Overtemperature Fault)								x			

COMMAND	BIT	NAME	INPUT UVLO	INPUT OVLO	OUTPUT UVLO	OVFB	OUTPUT OVERCURRENT (V_{FA})	REVERSE CURRENT	SHORT CIRCUIT (I_{OUT} > OCP)	THERMAL SHUTDOWN	SETI FAULT	PMBUS FAULT	OTHER
	6	OT_WARNING (Overtemperature Warning)											NOT USED
	5												
	4												
	3												
	2												
	1												
	0												
STATUS CML	7	Invalid or Unsupported Command Received											
	6	Invalid or Unsupported Data Received											
	5	Packet Error Check Failed											
	4	Memory Error Detected											
	3	—											
	2	— (Reserved, per PMBus specification)											
	1	A communication fault other than the ones listed in this table has occurred											
	0	—											
STATUS OTHER	7	—											
	6	—											
	5	—											
	4	—											
	3	—											
	2	—											
	1	—											

COMMAND	BIT	NAME	INPUT UVLO	INPUT OVLO	OUTPUT UVLO	OVFB	OUTPUT OVERCURRENT (V_{FA})	REVERSE CURRENT	SHORT CIRCUIT (I_{OUT} > OCP)	THERMAL SHUTDOWN	SETI FAULT	PMBUS FAULT	OTHER
	0	First to assert $\overline{\text{SMBALERT}}$											Not Supported. For future use.
$\overline{\text{SMBALERT}}$	Pin	Assert $\overline{\text{SMBALERT}}$ Open-Drain to Low status	x	x	x	x	x	x	x	x	x	**x**	
t_{BLANK} for $\overline{\text{SMBALERT}}$		Blanking Time before pulling $\overline{\text{SMBALERT}}$ Low	0s	0s	0s	0s	t_{BLANK}	0s	0s	0s	0s	**0s**	

Applications Information

IN Capacitor

A 1µF capacitor from the IN pin to GND is recommended to hold input voltage during sudden load-current changes.

Hot Plug-In at IN Terminal

In many powering applications, an input-filtering capacitor is required to lower the radiated emission and enhance the ESD capability. In hot plug-in applications, parasitic cable inductance, and the input capacitor cause overshoot and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that can limit surge voltage to a maximum of 80V shall be placed close to the input terminals for enhanced protection.

Input Hard Short to Ground

In many system applications, an input short-circuit protection is required. The device detects reverse current entering at the OUT pin and flowing out of the IN pin and turns off the external nFET. The magnitude of the reverse current depends on the inductance of the input circuitry and any capacitance installed near the IN pins.

Voltage Interruption Response

MAX17616/MAX17616A features fast recovery after voltage interruption during input-supply brownout tests. The device takes 150µs (typ) to turn on the internal nFET and 100µs (typ) to start turning on the external nFET when recovering from a brownout fault. *Figure 33* illustrates the performance of voltage interruption and recovery response.

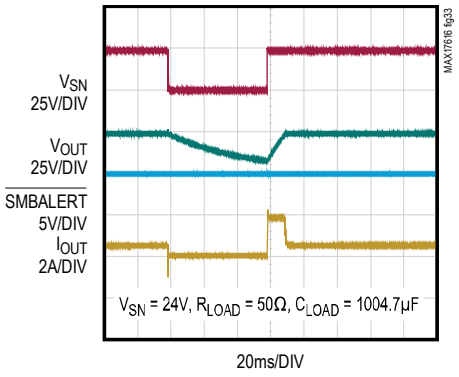


Figure 33. Voltage Interruption Response

OUT Capacitor

The maximum capacitive load (C_{MAX}) that can be connected is a function of the current-limit setting (I_{LIM} in A), the startup timeout (t_{STO} in ms), and the input voltage (V_{SN}). The C_{MAX} is calculated using the following equation:

$$C_{MAX}\ (mF) = \frac{I_{LIM} \times t_{STO}}{V_{SN}}$$

For example, for V_{SN} = 24V, t_{STO} (typ) = 1200ms, and I_{LIM} = 1A, C_{MAX} is 50mF

Output capacitor values over C_{MAX} can trigger false overcurrent conditions. Note that the above equation assumes that no-load current is drawn from the OUT pins. Any load current drawn would offset the capacitor charging current, resulting in a large charging period and, hence, the possibility of a false overcurrent condition.

In practical applications, the C_{MAX} value is limited by the thermal performance of the Printed Circuit Board (PCB). Poor thermal design can cause the thermal foldback current-limiting function of the device to kick in too early, which can further limit the maximum capacitance that can be charged. Therefore, a good thermal PCB design is imperative for charging large capacitor banks.

Hot Plug-In at OUT Terminal

In some applications, an external voltage at the OUT terminal of the devices can be applied with or without the presence of an input voltage. During these conditions, the devices detect any reverse current entering the OUT pin, flowing out of the IN pin, and turn off the external nFET. Parasitic cable inductance, along with input and output capacitors, cause overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection devices to see up to twice the applied voltage, which can damage the devices. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the *Absolute Maximum Ratings*.

OUT Clamping Diode for inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, an output clamp is recommended. This clamp can be implemented with a TVS, and a diode as shown in the *Typical Application Circuits*. This is required to clamp the negative spike on the OUT pin due to the inductive kickback during an output short-circuit event within the safe operating region. The maximum negative clamping voltage of the TVS for a maximum input voltage of V_{INMAX} is limited to (80 – V_{INMAX}) V to ensure IN to OUT pin voltage does not exceed 80V.

Layout and Thermal Dissipation

Place input and output capacitors as close as possible to the device. The IN and OUT pins must be connected with wide, short traces to the power bus. During normal operation, the power dissipation is small, and the package temperature change is minimal.

Power dissipation under steady-state normal operation may be calculated as:

$$P_{SS} = I_{OUT}^2 \times R_{ON}$$

See the *Electrical Characteristics Table* and *Typical Operating Characteristics* for R_{ON} values at various operating temperatures. Thermal vias from the exposed pad to the ground plane should be used to provide adequate heatsinking to internal ground planes.

ESD Protection

No capacitor is required for ±2kV (type) (HBM) ESD on IN. All pins have ±2kV (HBM) ESD protection. In applications in which an external nFET is used, see the IN Capacitor section.

Figure 34 shows the Human Body Model and *Figure 35* shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

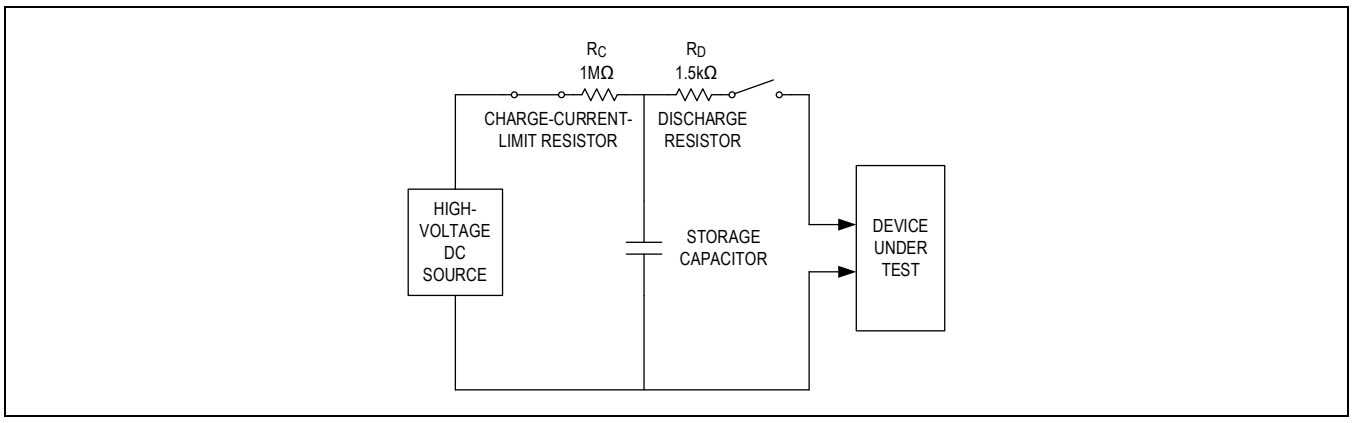


Figure 34. Human Body ESD Test Model

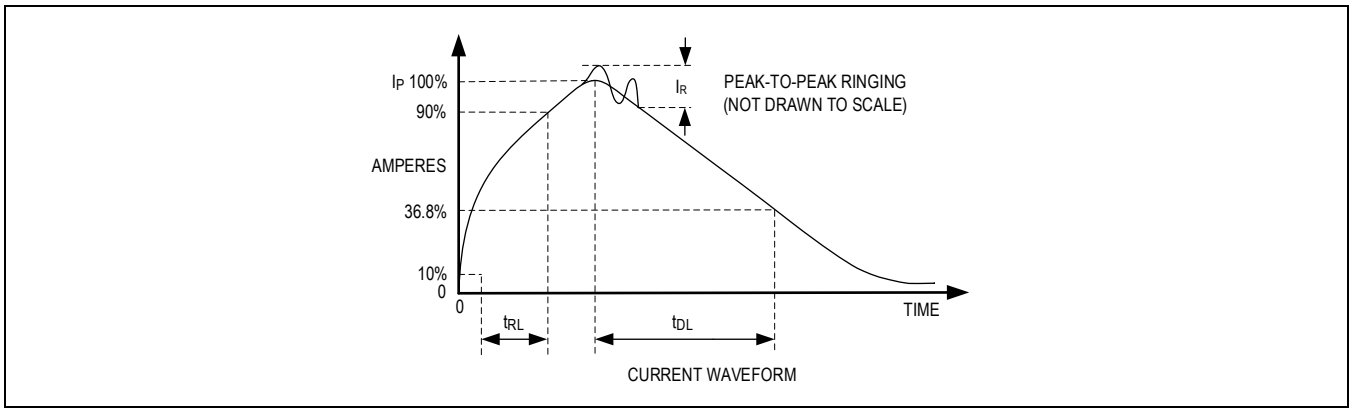
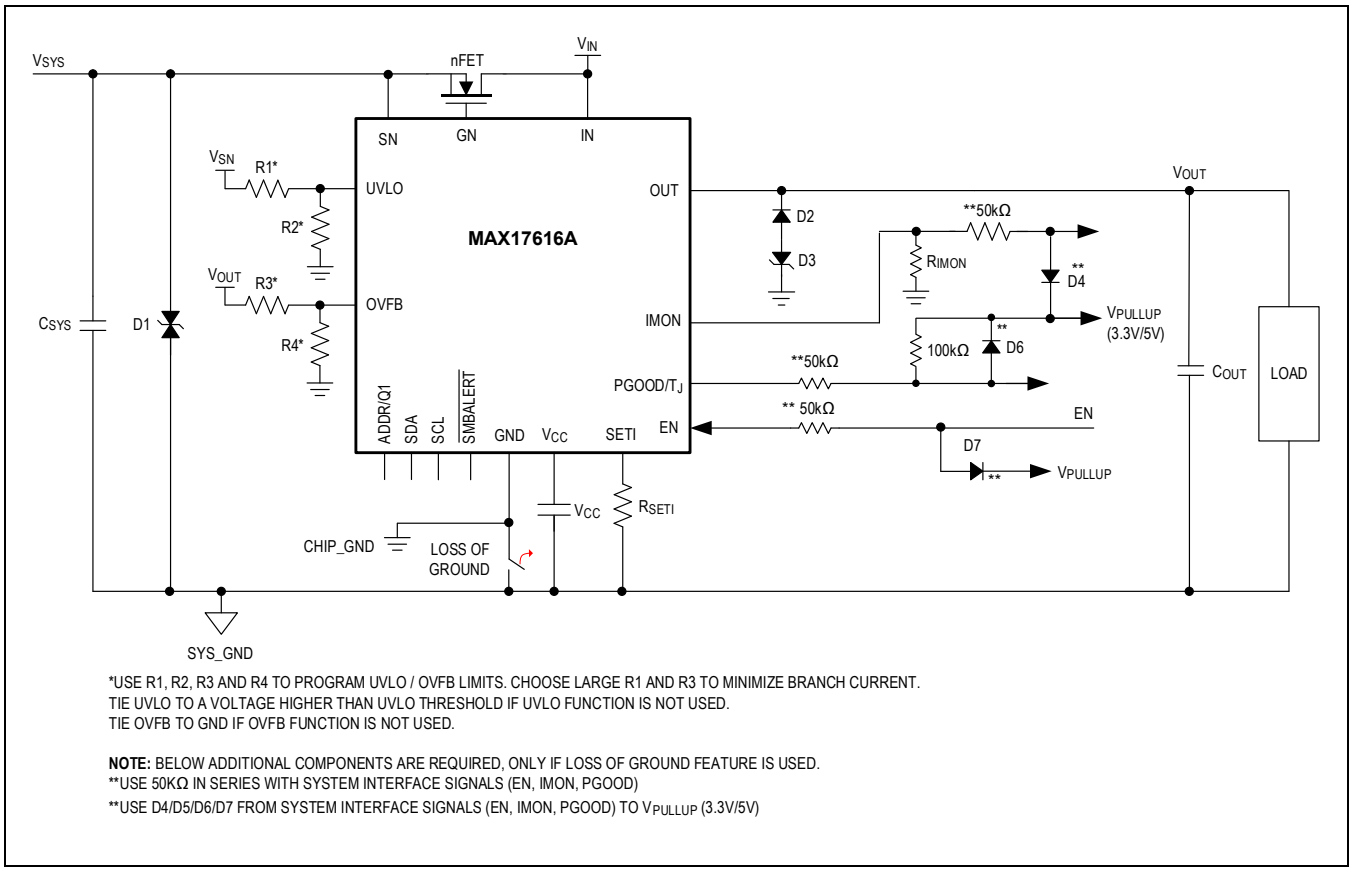


Figure 35. Human Body Current Waveform

Typical Application Circuits

MAX17616A Application Circuit



*USE R1, R2, R3 AND R4 TO PROGRAM UVLO / OVFB LIMITS. CHOOSE LARGE R1 AND R3 TO MINIMIZE BRANCH CURRENT.
TIE UVLO TO A VOLTAGE HIGHER THAN UVLO THRESHOLD IF UVLO FUNCTION IS NOT USED.
TIE OVFB TO GND IF OVFB FUNCTION IS NOT USED.

NOTE: BELOW ADDITIONAL COMPONENTS ARE REQUIRED, ONLY IF LOSS OF GROUND FEATURE IS USED.
**USE 50KΩ IN SERIES WITH SYSTEM INTERFACE SIGNALS (EN, IMON, PGOOD)
**USE D4/D5/D6/D7 FROM SYSTEM INTERFACE SIGNALS (EN, IMON, PGOOD) TO V_{PULLUP} (3.3V/5V)

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	FEATURES
MAX17616AFD+	-40°C to +125°C	23-Pin FCQFN	PMBus, OVLO
MAX17616AFD+T	-40°C to +125°C	23-Pin FCQFN	PMBus, OVLO
MAX17616AAFD+	-40°C to +125°C	23-Pin FCQFN	PMBus, OVFB
MAX17616AAFD+T	-40°C to +125°C	23-Pin FCQFN	PMBus, OVFB

+Denotes a lead (Pb)-free/RoHS-compliant package.
T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/24	Initial release	—

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Analog Devices Inc.:

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