Ultrathin, Low V_{IN} 10A Step-Down DC/DC µModule Regulator

FEATURES

- **Tiny Surface Mount, 4mm × 4mm × 1.43mm LGA**
- **Silent Switcher®2 Architecture**
- **Ultralow EMI Noise**
- Input Voltage Range: 2.25V to 5.5V
- Output Voltage Range: 0.5V to V_{IN}
- 10A DC Output Current
- Current Mode Control, Fast Transient Response
- Multiphase Parallel Current Sharing with Multiple LTM4659s
- Output Soft-Start with Voltage Tracking
- External Frequency Synchronization
- Selectable Pulse-Skipping Mode
- Power Good Indicator
- Die Temperature Monitoring Output
- Overvoltage, Overcurrent, and Overtemperature Protection

APPLICATIONS

- Telecom, Datacom, Networking System
- Optical Module
- Industrial Equipment
- Point-of-Load Regulation

DESCRIPTION

The LTM®4659 is a complete 10A step-down switch-ing mode µModule® regulator in a tiny 4mm × 4mm × 1.43mm LGA package. The package includes the switch-ing controller, power MOSFETs, inductor and all support components. Operating over an input voltage range of 2.25V to 5.5V, the LTM4659 supports an output volt-age range of 0.5V to V_{IN} set by external resistors. Its high-efficiency design delivers 10A continuous output cur-rent. Only ceramic input and output capacitors are needed.

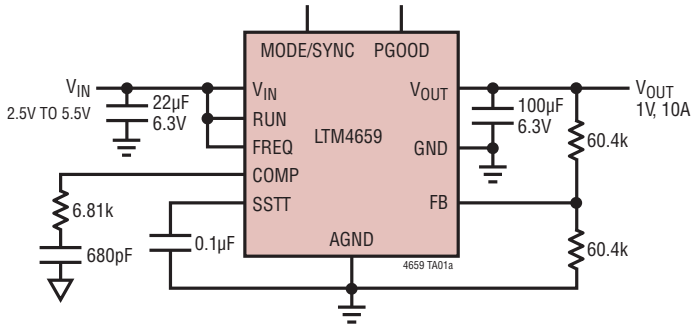
The LTM4659 employs a Silent Switcher 2 architecture with internal hot loop bypass capacitors to achieve both low EMI and high efficiency at high switching frequencies.

The LTM4659 also supports frequency synchronization, mul-tiphase operation, selectable pulse-skipping mode (PSM) operation, and output voltage tracking for supply rail sequencing. Its high switching frequency and a current mode architecture enables a very fast transient response to line and load changes without sacrificing stability.

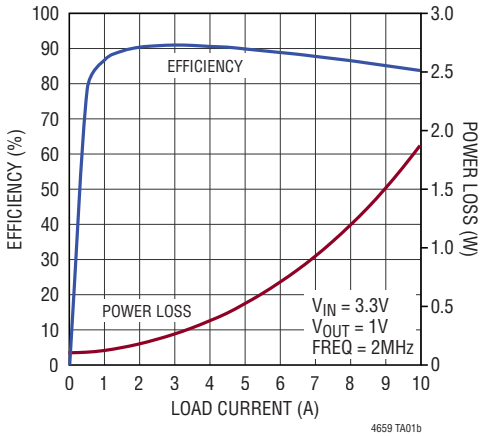
Fault protection features include overvoltage, overcur-rent, and overtemperature protection. The LTM4659 is lead(Pb)-Free and RoHS-compliant.

TYPICAL APPLICATION

Single 10A, 1V Output DC/DC µModule Regulator



Efficiency vs Load Current



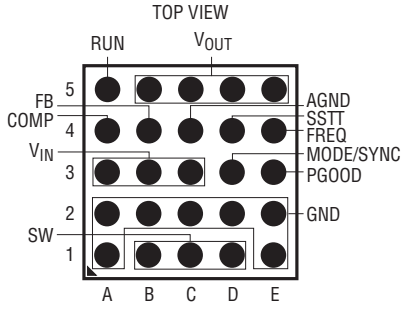
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 6V
V_{OUT} ..... –0.3V to V_{IN}
PGOOD ..... –0.3V to 6V
RUN, SSTT, MODE/SYNC,
FB, COMP, FREQ ..... –0.3V to V_{IN}
Operating Junction Temperature
(Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 260°C
Note that the peak reflow temperature must not exceed 260°C, including the reworking process.

PIN CONFIGURATION

(See Pin Functions and Table 9)



LGA PACKAGE
25-PIN (4mm × 4mm × 1.43mm)
T_{JMAX} = 125°C, θ_{JA} = 23°C/W,
θ_{JCtop} = 27.8°C/W, θ_{JCbot} = 5.7°C/W
WEIGHT = 86mg

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH*	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (SEE Note 2)
		DEVICE	FINISH CODE			
LTM4659EV#PBF	Au (RoHS)	4659	4	LGA	4	–40°C to 125°C
LTM4659IV#PBF	Au (RoHS)	4659	4	LGA	4	–40°C to 125°C

- Contact the factory for parts specified with wider operating temperature ranges. *Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 3.3V per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	2.25		5.5	V
$V_{OUT(RANGE)}$	Output Voltage Range	MODE/SYNC = 1MHz, FREQ = V_{IN}	●	0.5		V_{IN}	V
$V_{OUT(DC)}$	Output Voltage	MODE/SYNC = 1MHz, FREQ = V_{IN}, V_{OUT} = 0.5V	●	0.4925	0.5	0.5075	V
V_{IN_UVLO}	V_{IN} Undervoltage Lockout	V_{IN} Rising		2.0	2.1	2.2	V
$V_{IN\_UVLO\_HYS}$	V_{IN} Undervoltage Lockout Hysteresis				150		mV
V_{RUN}	RUN Pin on Threshold	V_{RUN} Rising		0.375	0.4	0.425	V
V_{RUN_HYS}	RUN Pin Hysteresis				60		mV
I_{RUN}	RUN Pin Leakage Current	RUN = 0.4V				±200	nA
$I_{Q(VIN)}$	Input Supply Bias Current Pulse-Skipping Mode Forced Continuous Mode Shutdown	 MODE/SYNC = FREQ = V_{IN}, V_{OUT} = 1.5V MODE/SYNC = 0V, FREQ = V_{IN}, V_{OUT} = 1.5V RUN = 0V (Note 4)			 1.6 70 1		 mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{OUT} = 0.5V, I_{OUT} = 10A			2.3		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating temperature range, otherwise specifications are at T_A = 25°C, (Note 2). V_{IN} = 3.3V per the typical application.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{OUT(DC)}$	Output Continuous Current Range	V_{OUT} = 0.5V (Note 4)				10	A
$\Delta V_{OUT(LINE)}/V_{OUT}$	Line Regulation Accuracy	FREQ = V_{IN}, V_{OUT} = 1.5V, V_{IN} = 5.5V, I_{OUT} = 0A	●		0.001	0.8	%/V
$\Delta V_{OUT(LOAD)}/V_{OUT}$	Load Regulation Accuracy	V_{IN} = FREQ = 3.3V, SYNC = 1.0MHz, V_{OUT} = 0.5V, I_{OUT} = 0A to 10A	●			1	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF + 22µF ×2 Ceramic, (Notes 4)			2		mV
$\Delta V_{OUT(START)}$	Turn-On Overshoot	I_{OUT} = 0A, C_{OUT} = 100µF + 22µF ×2 Ceramic, (Notes 4)			5		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF + 22µF ×2 Ceramic, No Load, SSTT = 0.1µF (Note 4)			5		ms
I_{SSTT}	Track Pin Soft-Start Pull-Up Current	SSTT = 0.5V		7	10	13	µA
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF + 22µF ×2 Ceramic (Note 4)			157		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF + 22µF ×2 Ceramic, (Note 4)			15		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 3.3V, V_{OUT} = 0.5V			18		A
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.495	0.50	0.505	V
I_{FB}	Current at V_{FB} Pin					±20	nA
V_{PGOOD}	PGOOD Trip Level Undervoltage Falling Threshold Overvoltage Rising Threshold	As a Percentage of Regulated V_{OUT} V_{FB} Ramping Negative V_{FB} Ramping Positive		 –4 7	 –3 10	 –2 13	 % %
I_{PGOOD}	PGOOD Leakage	V_{PGOOD} = 5.5V				50	nA
f_{OSC}	Oscillator Frequency				2		MHz
SYNC_RANGE	Sync Frequency Range	FREQ = V_{IN}		1.0		2.6	MHz
SYNC_LEVEL	Clock Level High on SYNC Clock Level Low on SYNC			1.2		 0.4	V V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

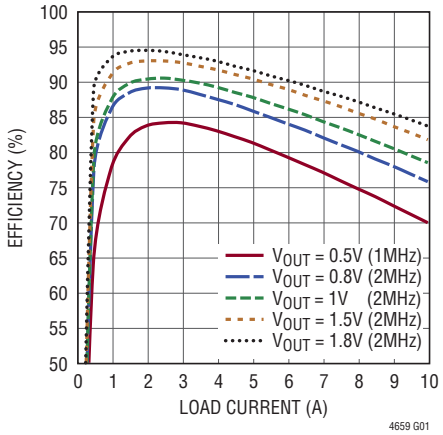
Note 2: The LTM4659 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4659E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4659I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

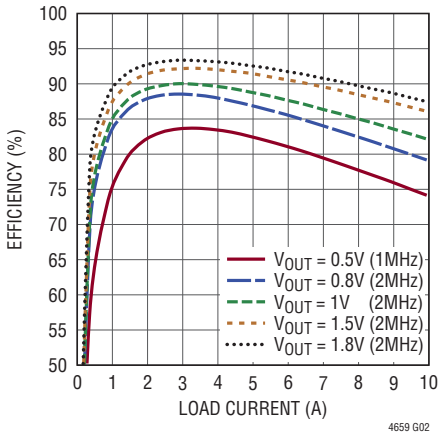
Note 4: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

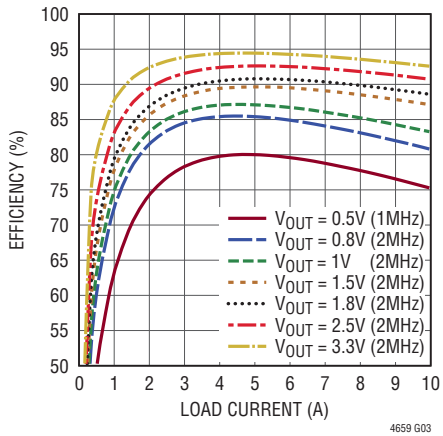
Efficiency vs Load Current at $2.5V_{IN}$



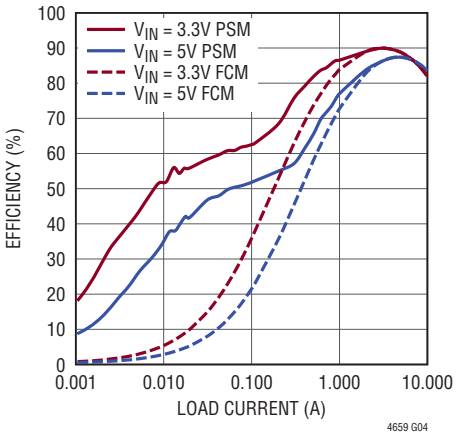
Efficiency vs Load Current at $3.3V_{IN}$



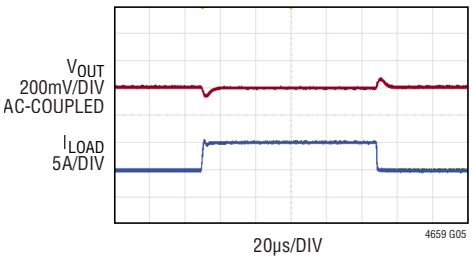
Efficiency vs Load Current at $5V_{IN}$



Efficiency vs Load Current at Different Modes of Operation

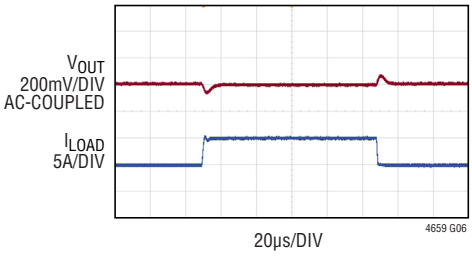


Output Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.0V



I_{OUT} = 2.5A TO 7.5A,
OUTPUT CAPACITOR = 100µF + 22µF ×2
f_{SW} = 2MHz

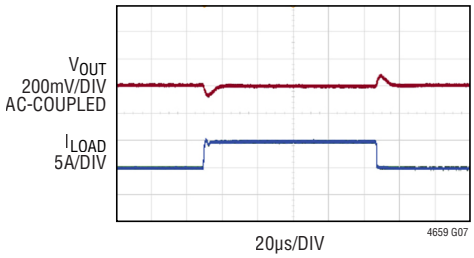
Output Transient Response, V_{IN} = 5V, V_{OUT} = 1.0V



I_{OUT} = 2.5A TO 7.5A,
OUTPUT CAPACITOR = 100µF + 22µF ×2
f_{SW} = 2MHz

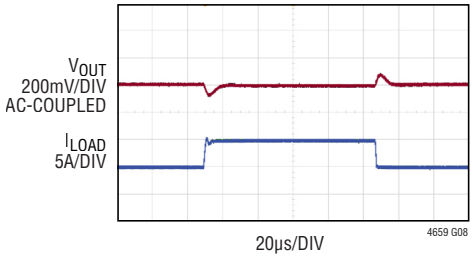
TYPICAL PERFORMANCE CHARACTERISTICS

Output Transient Response, V_{IN} = 3.3V, V_{OUT} = 1.5V



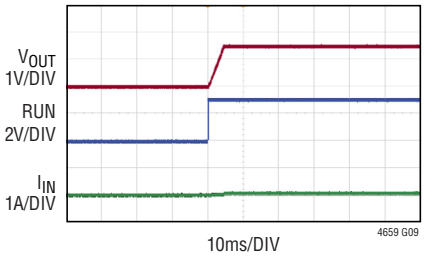
I_{OUT} = 2.5A TO 7.5A,
OUTPUT CAPACITOR = 100µF + 22µF ×2
f_{SW} = 2MHz

Output Transient Response, V_{IN} = 5V, V_{OUT} = 1.5V



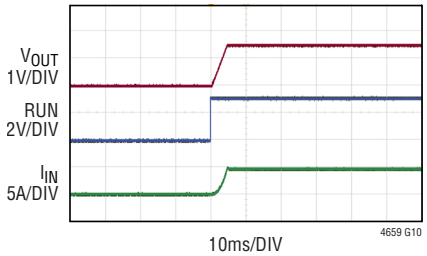
I_{OUT} = 2.5A TO 7.5A,
OUTPUT CAPACITOR = 100µF + 22µF ×2
f_{SW} = 2MHz

Start-Up with No Load



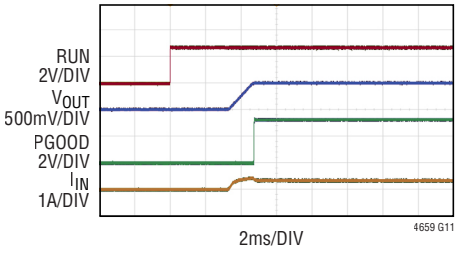
V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 0A,
f_{SW} = 2MHz

Start-Up with 10A Load



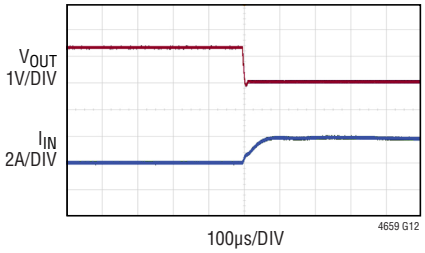
V_{IN} = 3.3V, V_{OUT} = 1.5V, R_{LOAD} = 0.15Ω,
f_{SW} = 2MHz

Start-Up with Prebiased Output



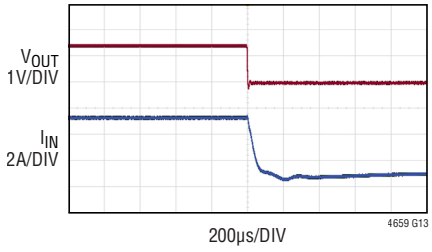
V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 0A,
f_{SW} = 2MHz

Short-Circuit with No Load



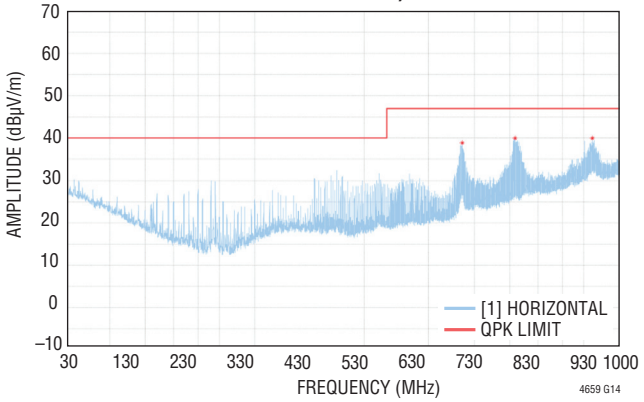
V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 0A,
f_{SW} = 2MHz

Short-Circuit with 10A Load



V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 10A,
f_{SW} = 2MHz

Conducted EMI Performance (CISPR32 Radiated Emission Test with Class B 10m)



DC3248A DEMO BOARD, NO INPUT
EMI FILTER INSTALLED, 3.3V_{IN} TO 1V_{OUT}, R_{LOAD} = 0.125Ω (8A)

PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

GND (Pins A1, A2, B2, C2, D2, E1, E2): Power Ground Pins for both Input and Output Returns.

V_{IN} (Pins A3, B3, C3): The V_{IN} pins supply current to the internal circuitry and topside power switch. All of the V_{IN} pins must be connected together with short, wide traces and bypassed to PGND with low ESR capacitors located as close as possible to the pins.

COMP (Pin A4): The COMP pin is the compensation node for the output voltage regulation control loop. Compensation components connected to this pin are referenced to AGND.

RUN (Pin A5): Run the Control Input of each Switching Mode Regulator Channel. Enables chip operation by connecting RUN above 0.4V. Connecting it to GND shuts down the part.

SW (Pins B1, C1, D1): Switching Node Internal High Current Path from MOSFET to Inductor. Connect with a solid cooper area or leave it floating.

FB (Pin B4): The negative input of the error amplifier for the switching mode regulator. The LTM4659 regulates the voltage between FB and AGND to 500mV. A resistor divider connecting to V_{OUT} sets the output voltage. In PolyPhase® operation, connecting the FB pins of the subordinate channels to V_{IN} to disable the internal error amplifier. See the Applications Information section for details.

V_{OUT} (Pins B5, C5, D5, E5): Power Output Pins of Each Switching Mode Regulator. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and the GND pins.

AGND (Pin C4): The AGND pin is the ground reference for the internal analog circuitry, including the bandgap voltage reference. To achieve good load regulation, connect the AGND pin to the negative terminal of the output capacitor (C_{OUT}) at the load. A drop in the high current power ground return path will be compensated. All of the signal components, such as the FB resistor dividers and soft-start capacitor, should be referenced to the AGND node. The AGND node carries very little current and, therefore, can be a minimal size trace.

MODE/SYNC (Pin D3): The MODE/SYNC pin facilitates multiphase operation and synchronization to an external clock. Depending on the mode of operation, the MODE/SYNC pin either accepts an input clock pulse or outputs a clock pulse at its operating frequency. (See Multiphase Operation in the Applications Information section). The MODE/SYNC pin also programs the mode of operation: pulse-skipping or forced continuous mode.

SSTT (Pin D4): Soft-Start, Tracking, and Temperature Monitor Pin. An internal 10µA current into an external capacitor on the soft-start pin programs the output voltage ramp rate during start-up. When SSTT is below 0.5V, the V_{FB} pin voltage will track the SSTT pin voltage. When SSTT is above 0.5V, the tracking function is disabled. The internal reference resumes control of the error amplifier and the SSTT pin servos to a voltage representative of junction temperature. For a clean recovery from an output short-circuit condition, the SSTT pin is pulled down to approximately 140mV above the V_{FB} voltage, and a new soft-start cycle is initiated. During shutdown and fault conditions, the SSTT pin is pulled to ground.

PGOOD (Pin E3): Output Power Good with Open-Drain Logic of the Switching Mode Regulator Channel. PGOOD is pulled to ground when the voltage on the FB pin is not within –3%/10% of the internal 0.5V reference.

FREQ (Pin E4): The FREQ pin sets the oscillator frequency with an external resistor to AGND or sets the phasing for multiphase operation. (See Multiphase Operation in the Applications Information section).

BLOCK DIAGRAM

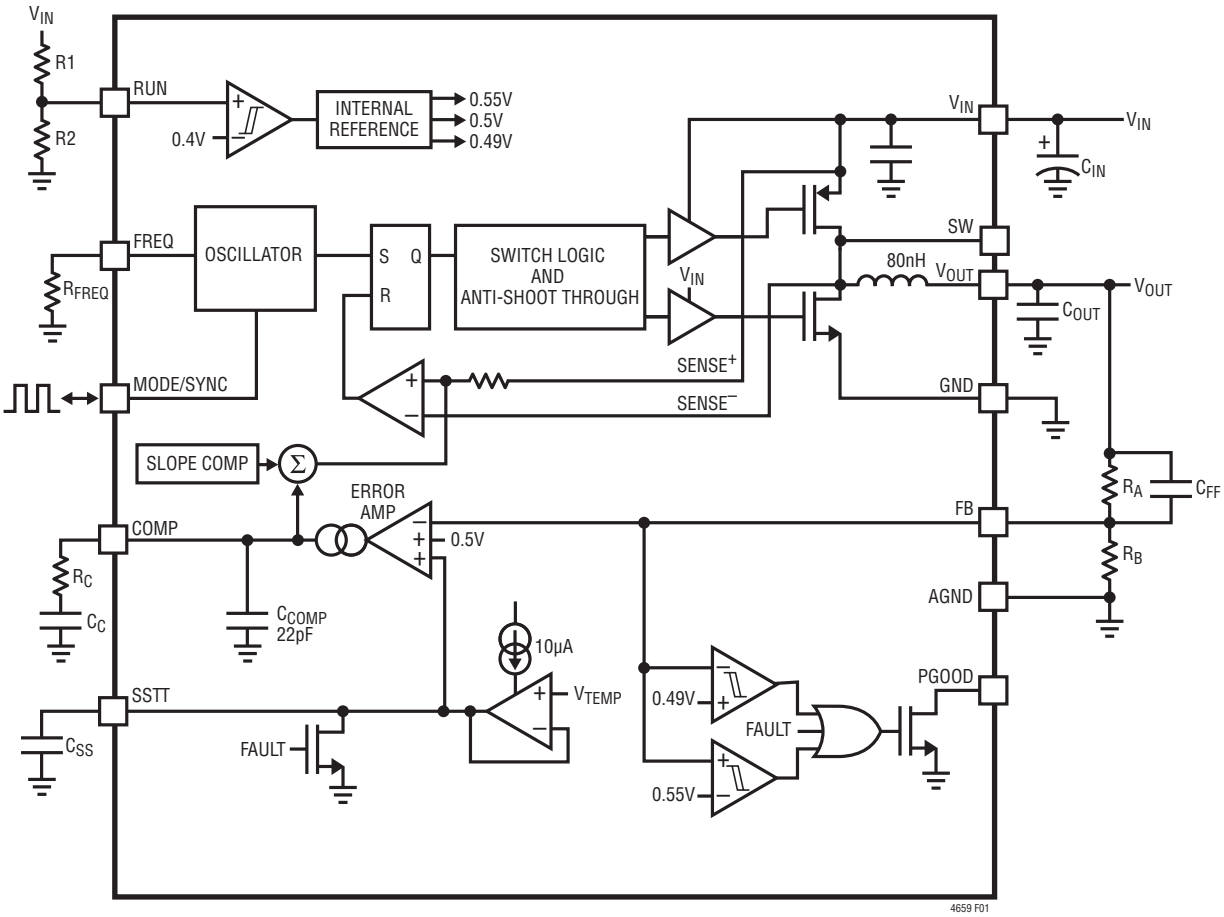


Figure 1. Simplified LTM4659 Block Diagram

DECOUPLING REQUIREMENTS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 10A	22			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 2.25V to 5.5V, V_{OUT} = 1.5V)	I_{OUT} = 10A	100			µF

OPERATION

The LTM4659 is a standalone nonisolated step-down µModule regulator. It can deliver up to 10A of DC output current with a few external input and output capacitors. This module provides precisely regulated output voltage from 0.5V to 5.5V over a 2.25V to 5.5V input voltage range. See Typical Application schematic for more details.

The LTM4659 has an integrated constant-frequency peak current mode step-down regulator with power MOSFETs, inductor, and other supporting discrete components. The default switching frequency is 2MHz. It can be externally synchronized to a clock from 1MHz to 2.60MHz. See the Applications Information section.

Current mode control provides cycle-by-cycle fast current limiting and overcurrent protection. Internal feedback loop compensation provides sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Internal undervoltage and overvoltage comparators pull the open-drain PGOOD output low if the feedback voltage exits a –3%/10% window around the regulation point. Furthermore, in an overvoltage condition, the internal top MOSFET is turned off, and the bottom MOSFET is turned on and held on until the overvoltage condition clears.

For systems with higher power requirements, multiphase operation can be easily employed with the synchronization and phase mode controls.

Pulling the RUN pin to GND forces the controller into its shutdown state, turning off both power MOSFETs and most of the internal control circuitry. At light load currents, PSM operation can be enabled to achieve higher efficiency compared to FCM by setting the MODE/SYNC pin to V_{IN}. The SSTT pin is used for power supply tracking, soft-start programming and die temperature monitoring. See the Applications Information section.

APPLICATIONS INFORMATION

See LTM4659 Typical Application circuit. External component selection is primarily determined by the input voltage, the output voltage and the maximum load current. See Table 8 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

The minimum V_{OUT} step-down ratio that can be achieved for a given input voltage is limited by the minimum on-time of the regulator.

The minimum on-time limit imposes a minimum duty cycle of the converter which can be calculated using Equation 1.

$$D_{MIN} = T_{ON(MIN)} \bullet f_{SW} \quad (1)$$

where $T_{ON(MIN)}$ is the minimum on-time, 45ns typical for the LTM4659. In the rare cases where the minimum duty cycle is surpassed, the output will overvoltage and a slower switching frequency is needed to accommodate the high V_{IN}/V_{OUT} ratio.

The LTM4659 is capable of a maximum duty cycle of 100%; therefore, the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch, the inductor DCR, and the load current.

Output Voltage Programming and Output Voltage Sensing

The PWM controller has an internal 0.5V reference voltage. The resistor divider from the V_{OUT} remote sensing point to the FB pin and from the FB pin to the AGND pin programs the output voltage (Equation 2). See the Block Diagram for more information.

$$V_{OUT} = 0.5V \bullet \frac{R_A + R_B}{R_B} \quad (2)$$

In high current operation, a ground offset may be present between the LTM4659 local ground and ground at the load. To overcome this offset, AGND should have a Kelvin connection to the load ground, and the lowest potential node of the resistor divider should be connected to AGND. The internal error amplifier senses the difference between this feedback voltage and a 0.5V AGND referenced voltage. This scheme overcomes any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. The LTM4659 allows for remote output ground deviations as much as ±100mV with respect to the local ground.

Input Decoupling Capacitors

The LTM4659 module should be connected to a low AC-impedance DC source. All of the V_{IN} pins must be connected together with short, wide traces and bypassed to PGND with low ESR capacitors located as close as possible to the pins. For the regulator, a one-piece 22µF input ceramic capacitor is recommended for RMS ripple current decoupling. A bulk input capacitor is only needed when the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. The bulk capacitor can be an electrolytic aluminum capacitor and polymer capacitor.

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated using Equation 3.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (3)$$

where $\eta\%$ is the estimated efficiency of the power module.

Output Decoupling Capacitors

With an optimized high-frequency, high-bandwidth design, only two pieces of 47µF low ESR output ceramic capacitors are required for LTM4659 to achieve low output voltage ripple and very good transient response. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 8 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 2.5A (25%) load-step transient.

The multiphase operation will reduce effective output ripple as a function of the number of phases. Analog Devices Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. The Analog Devices LTpowerCAD® design tool is available to download online for output ripple, stability and

APPLICATIONS INFORMATION

transient response analysis and calculation of the output ripple reduction as the number of phases implemented increases by N times.

Modes of Operation

The MODE/SYNC pin either synchronizes the external switching frequency, or a clock output, to set the PWM mode. The PWM modes of operation are either pulse-skipping (PSM) or forced continuous mode (FCM). See Table 1.

Table 1. LTM4659 Single-Phase Configuration

FREQ PIN CONNECTION	MODE/SYNC PIN CONNECTION	MODE OF OPERATION	SWITCHING FREQUENCY
V_{IN}	Clock Input	FCM	External Clock
V_{IN}	AGND	FCM	2MHz Default
V_{IN}	V_{IN}	PSM	2MHz Default
Resistor to AGND	Clock Output	FCM	R_{FREQ} Programmed

The LTM4659 operates in FCM for low noise or PSM for high efficiency at light load. The LTM4659 operates in PSM when both FREQ and MODE/SYNC pins are connected to V_{IN}. In PSM, switching cycles are skipped at light load to regulate the output voltage. The LTM4659 defaults to FCM in regulation and during synchronization. During FCM, the top switch turns on every cycle and light load regulation is achieved by allowing negative inductor current.

Setting the Operating Frequency

The operating frequency defaults to 2MHz when the FREQ pin is connected to V_{IN}. If any frequency higher than the default frequency is required, the frequency can be programmed by tying a resistor from the FREQ pin to AGND using Equation 4.

$$R_{FREQ} = 568 \bullet f_{(SW)}^{(-1.08)} \quad (4)$$

where R_{FREQ} is in kΩ and f_{SW} is the desired switching frequency in MHz.

The frequency can be programmed to switch from 1MHz to 3MHz. Table 2 shows the necessary R_{FREQ} value for a desired switching frequency.

Table 2. SW Frequency vs R_{FREQ} Value

f_{SW} (MHz)	R_{FREQ} (kΩ)
1	549
2	274
2.2	243
3	178

Synchronizing the Oscillator to an External Clock

The LTM4659 switching frequency can also be adjusted by synchronizing the internal PLL circuit to an external clock to the MODE/SYNC pin. The synchronization frequency range is 1MHz to 2.6MHz. The LTM4659 operates in FCM when synchronized to an external clock.

Connect the FREQ pin to V_{IN} configures the MODE/SYNC pin as a clock input. During synchronization, the top power switch turn-on is locked to the rising edge of the external frequency source. The slope compensation is automatically adapted to the external clock frequency.

At start-up, before the LTM4659 recognizes the external clock applied to MODE/SYNC, the LTM4659 will switch at its default frequency of 2MHz. Once the externally applied clock is recognized, the switching frequency will gradually transition from the default frequency to the applied frequency. If the external clock is removed, the LTM4659 will slowly transition back to the default frequency.

The synchronizing clock amplitude should be greater than 1.2V and less than 0.4V with a pulse width greater than 40ns. An internal 200k resistor on the MODE/SYNC pin to AGND allows the MODE/SYNC to be floating. Note that a low switching frequency will increase the inductor peak current and the output voltage ripple.

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Multiphase Operation

For output loads that demand more than 10A of current, multiple LTM4659s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. See Table 3.

To parallel multiple LTM4659 modules to achieve the same switching frequency, a perfect interleaved phase shift and an accurate current sharing between different modules, one of the LTM4659 will become the main module, and the rest of the LTM4659s need to be programmed to be subordinate modules. See Multiphase Operation in the Applications Information section.

1. Connect a resistor from the FREQ pin to the AGND of the main phase will program the frequency and configures the MODE/SYNC pin to become a clock output used to drive the MODE/SYNC pins of the subordinate phase(s).

   Connecting the FREQ pin of the main phase to V_{IN} configures the MODE/SYNC pin to become an input capable of accepting an external clock. The switching frequency defaults to the nominal 2MHz internal frequency when the external clock is unavailable, such as during start-up.

   Connecting the FB pin to V_{IN} configures a phase as a subordinate. The MODE/SYNC becomes an input, and the voltage control loop is disabled. The subordinate phase current control loop is still active, and the peak current is controlled via the shared COMP node. Careful consideration should be taken when routing the COMP node between phases. Routing the COMP and AGND nodes together is recommended to create a low inductance path.

   Connecting the PGOOD pins together and adding an external pull-up resistor allows the main phase to communicate with the subordinate phases on when start-up has been completed.

   The pull-up voltage should be greater than 0.49V for subordinate channels on multiphase operations.

2. The phasing of a subordinate phase relative to the main phase is programmed with a resistor divider on the FREQ pin (see Figure 2). Use of 1% resistors is recommended. See Table 4 for more information.

   When configured for main/subordinate operation, the subordinate phases operate in FCM.

Table 3. Multiphase Configuration

MAIN/SUBORDINATE	FREQ PIN	FB PIN	MODE/SYNC PIN	SWITCHING FREQUENCY (f_{SW})
Main	V_{IN}	V_{OUT} Divider	Clock Input	External Clock/2MHz Default
Main	Resistor to AGND	V_{OUT} Divider	Clock Output	FREQ Programmed
Subordinate	V_{IN} Divider	V_{IN}	Clock Input	External Clock

Table 4. Programming Subordinate Phase Angle

SYNC PHASE ANGLE	R3 RATIO	R4 RATIO	R3 EXAMPLE	R4 EXAMPLE
0°	0Ω	NA	0Ω	NA
90°	3 • R	R	301k	100k
120°	7 • R	5 • R	243k	174k
180°	NA	0Ω	NA	0Ω
240°	5 • R	7 • R	174k	243k
270°	R	3 • R	100k	301k

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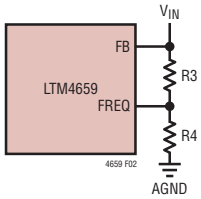

Figure 2. Phase Programming

The LTM4659 device is an inherently current mode-controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Connect the RUN and COMP pins of each paralleling channel together. Figure 17 through Figure 19 show examples of parallel operation and pin connections.

Input RMS Ripple Current Cancellation

The Analog Devices Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 3 shows this graph.

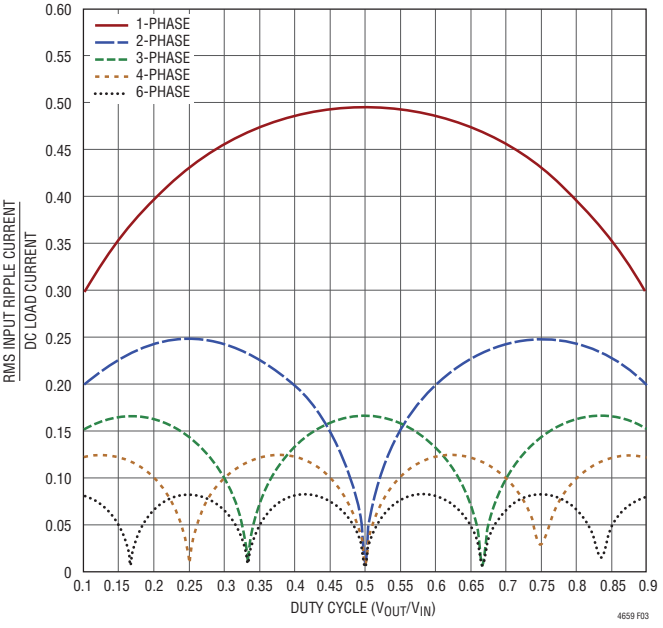

Figure 3. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

Soft-Start, Tracking, Temperature Monitor

The LTM4659 allows the user to program its output voltage ramp rate using the SSTT pin.

An internal 10µA pulls up the SSTT pin. Putting an external capacitor on SSTT enables soft-starting the output to prevent current surge on the input supply and output voltage overshoot. During the soft-start ramp, the output voltage will proportionally track the SSTT pin voltage. When the soft-start is complete, the pin will servo to a voltage proportional to the LTM4659 junction temperature. Figure 4 shows the SSTT pin operating range.

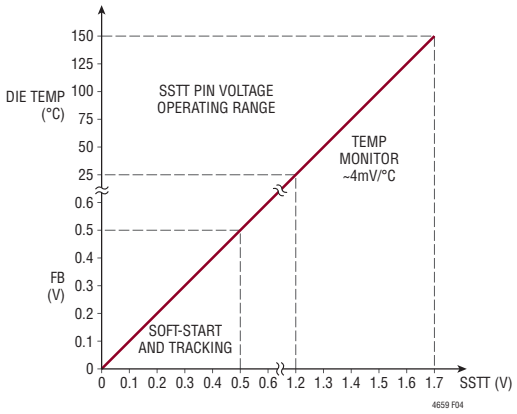

Figure 4. Soft-Start and Temperature Monitor Operation

The soft-start time is calculated using Equation 5.

$$T_{SS} = C_{SS} \bullet \frac{500mV}{10\mu A} \quad (5)$$

For output tracking applications, SSTT can be externally driven by another voltage source. From 0V to 0.5V, the SSTT voltage will override the internal 0.5V reference input to the error amplifier, thus regulating the FB pin voltage to that of the SSTT pin. When SSTT is above 0.5V, tracking is disabled and the feedback voltage will regulate the internal reference voltage.

An active pull-down circuit is connected to the SSTT pin to discharge the external soft-start capacitor in the case of fault conditions. The ramp will restart when the fault is cleared. Fault conditions that clear the soft-start capacitor are the RUN/UV pin transitioning low, V_{IN} voltage falling too low or thermal shutdown.

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Once the soft-start cycle has been completed and the output power good flag has been thrown, the SSTT pin reports the die junction temperature. The LTM4659 regulates the SSTT pin to a voltage proportional to the junction temperature. While reporting the temperature, the SSTT voltage is not valid below 1V. The junction temperature is calculated using Equation 6.

$$T_J\ (°C) = \frac{V_{SSTT}}{4mV} - 273 \quad (6)$$

The following procedure is used for a more accurate measurement of the junction temperature.

1. Measure the ambient temperature T_A.
2. Measure the SSTT voltage while in PSM with the V_{OUT} pulled up slightly higher than the regulated V_{OUT}.
3. Calculate the slope of the temperature sensing circuit using Equation 7.

$$Slope\left(\frac{mV}{°C}\right) = \frac{V_{SSTT}}{T_A + 273} \quad (7)$$

4. Calculate the junction temperature with the new calibrated slope.

When the output voltage goes out of regulation and the power good pin is pulled low, the soft-start pin no longer reports the temperature.

Power Good

The PGOOD pins are open-drain pins that can be used to monitor valid output voltage regulation. This pin monitors a –3/10% window around the regulation point. A resistor can be pulled up to a particular supply voltage for monitoring. To prevent unwanted PGOOD glitches during transients or dynamic V_{OUT} changes, the LTM4659's PGOOD falling edge includes a blanking delay of approximately 100µs. The PGOOD is also actively pulled low during fault conditions: RUN pin is low, V_{IN} is too low, or in thermal shutdown.

Transient Response and Loop Compensation

When determining the compensation components, C_{FF}, R_C, and C_C, control loop stability and transient response are the two main considerations. The LTM4659 has been designed to operate at high bandwidth for fast transient response capability. Operating at a high loop bandwidth reduces the output capacitance required to meet transient response requirements. Applying a load transient and monitoring the system's response or using a network analyzer to measure the actual loop response are two ways to verify and optimize LTM4659. For more information, refer to the Analog Devices technical article: "Understand Power Supply Loop Stability and Loop Compensation—Part 1: Basic Concepts and Tools". Analog Devices LTpowerCAD is a useful tool for optimizing the compensation components.

When using the load transient response method to stabilize the control loop, apply an output current pulse of 20% to 100% of the full load current having a rise time of 1µs. This will produce a transient on the output voltage and COMP pin waveforms.

Switching regulators take multiple cycles to respond to a step in load current. When a load step occurs, V_{OUT} is immediately perturbed, generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value.

During this recovery time, monitor V_{OUT} for overshoot or ringing indicating a stability problem. The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second-order overshoot/DC ratio cannot be used to determine the phase margin. The gain of the loop increases with the R_C, and the bandwidth of the loop increases with decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, adding a feedforward capacitor, C_{FF}, improves the high frequency response. Capacitor C_{FF} provides phase lead by creating a high-frequency zero with R_A to improve the phase margin. The compensation

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components of the typical application circuits are a good starting point for component values. The output voltage settling behavior is related to the stability of the closed-loop system. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to the Analog Devices Application Note 76.

RUN Threshold Programming

The LTM4659 has a precision threshold RUN pin to enable or disable switching. Pulling the RUN pin to ground forces the LTM4659 into its shutdown state, turning off both power MOSFETs and most of its internal control circuitry. Bringing the RUN pin above 0.4V will turn on the entire chip.

The rising threshold of the RUN comparator is 400mV with 60mV of hysteresis. Connect the RUN pin to V_{IN} if the shutdown feature is not used. Adding a resistor divider from V_{IN} to RUN programs the LTM4659 to regulate the output only when V_{IN} is above a desired voltage (see the Block Diagram). Typically, this threshold, $V_{IN(RUN)}$, is used in situations where the input supply is current limited or has a relatively high source resistance. A switching regulator draws constant power from the source, so the source current increases as the source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(RUN)}$ threshold prevents the regulator from operating at source voltages where problems may occur. This threshold can be adjusted by setting the values R1 and R2 such that they satisfy Equation 8.

$$V_{IN(RUN)} = \left(\frac{R_1}{R_2}+1\right) \bullet 400mV \quad (8)$$

where the LTM4659 will remain off until V_{IN} is above $V_{IN(RUN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(RUN)}$.

Alternatively, a resistor divider from an output of another regulator to the enable RUN pin of the LTM4659 provides event-based power up sequencing, enabling the LTM4659 when the output of the other regulator reaches a predetermined level.

Output Overvoltage Protection

During an output overvoltage event, when the FB pin voltage is greater than 110% of nominal, the LTM4659 top power switch will be turned off. If the output remains out of regulation for more than 100µs, the PGOOD pin will be pulled low. An output overvoltage event should not happen under normal operating conditions.

Output Short-Circuit Protection and Recovery

The peak inductor current at which the current comparator shuts off the top power switch is controlled by the voltage on the COMP pin. If the output current increases, the error amplifier raises the COMP pin voltage until the average inductor current matches the new load current. In normal operation, the LTM4659 clamps at the maximum COMP pin voltage.

When the output is shorted to ground, the inductor current decays very slowly during the switch-off time because of the low voltage across the inductor. To keep the current in control, a secondary limit is also imposed on the valley inductor current. If the inductor current measured through the bottom power switch increases beyond $I_{VALLEY(MAX)}$, the top power switch will be held off and switching cycles will be skipped until the inductor current is reduced.

Recovery from a short circuit can be abrupt, and because the output is shorted and below regulation, the regulator is requesting the maximum current to charge the output. When the short circuit condition is removed, the inductor current could cause an extreme voltage overshoot in the output. The LTM4659 addresses this potential issue by regulating the SSTT voltage just above the FB voltage when the output is out of regulation. Therefore, a recovery from an output short circuit goes through a soft-start cycle. The output ramp is controlled, and the overshoot is minimized.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section are consistent with those parameters defined by JESD51-9. They are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation

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to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 (“Test Boards for Area Array Surface Mount Package Thermal Measurements”). The motivation for providing these thermal coefficients is found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance on thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one’s application-usage, and can be adapted to correlate thermal performance to one’s own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below.

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in one cubic foot sealed enclosure. This environment is sometimes referred to as “still air” although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.
2. θ_{JCbot}, the thermal resistance from junction to bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical module regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages, but the test conditions don’t generally match the user’s application.
3. θ_{JCtop}, the thermal resistance from the junction to the top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages but the test conditions don’t generally match the user’s application.

A graphical representation of the aforementioned thermal resistances is shown in Figure 5; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

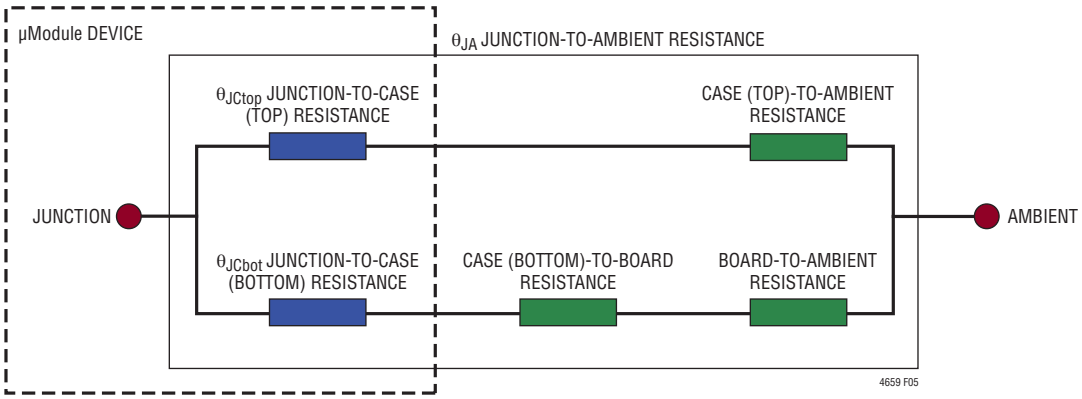

Figure 5. Graphical Representation of JESD51-12 Thermal Coefficients

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As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and θ_{JCbot}, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware that there are multiple power devices and components dissipating power, with the consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet.

The $2.5V_{IN}$, $3.3V_{IN}$ and $5V_{IN}$ power loss curves in Figure 6, Figure 7, and Figure 8 can be used in coordination with the load current derating curves in Figure 9 to Figure 14 for calculating an approximate θ_{JA} thermal resistance for the LTM4659 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the junction temperature. This approximate factor is ~1.2 assuming the junction temperature is reaching 120°C. The maximum load current is achievable while increasing ambient temperature as long as the junction temperature is less than 120°C, which is a 5°C guardband from the maximum junction temperature of 125°C. When the ambient temperature reaches a point where the junction temperature is 120°C, then the load current is lowered to maintain the junction at 120°C while increasing the ambient temperature up to 120°C. The derating curves are plotted with the output current starting at 10A and the ambient temperature at 30°C. The output voltages are 1.0V, 1.5V and 2.5V. These are chosen to include the lower and higher output voltage ranges to correlate the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber, along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. For example, to determine the maximum ambient temperature allowable when V_{IN} = 3.3V, V_{OUT} = 1V and 10A load current without a heat sink and airflow, find out the power loss from Figure 7, which equals to 2.24W in this case, then multiply by the 1.2 coefficient for 120°C junction temperature, If the 65.4°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 54.6°C divided by 2.7W equals a 20.2°C/W for θ_{JA} the system equivalent thermal resistance. Table 5 specifies a 21°C/W

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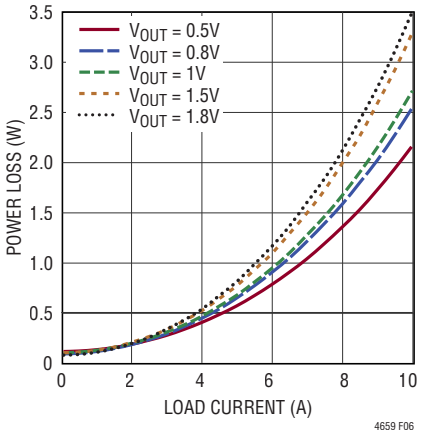

Figure 6. Power Loss vs Load Current at $2.5V_{IN}$

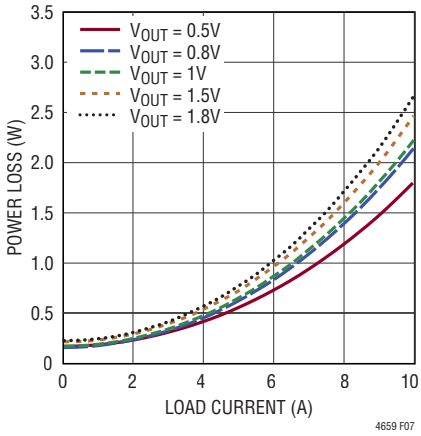

Figure 7. Power Loss vs Load Current at $3.3V_{IN}$

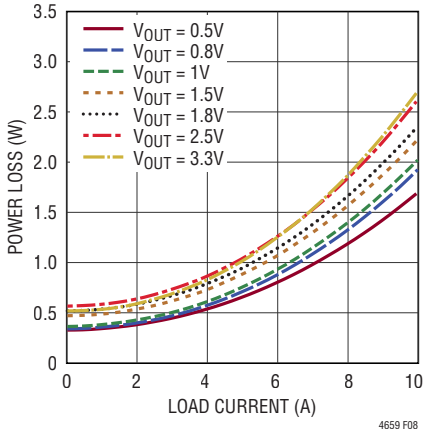

Figure 8. Power Loss vs Load Current at $5V_{IN}$

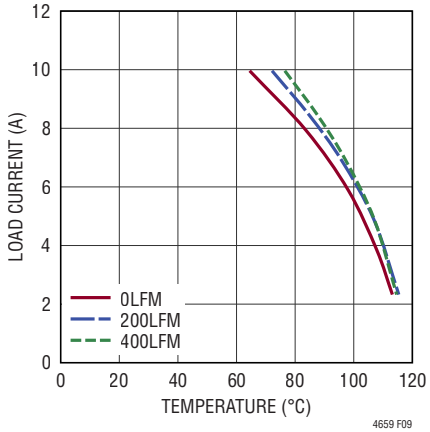

Figure 9. 3.3V to 1V Derating Curve, No Heat Sink

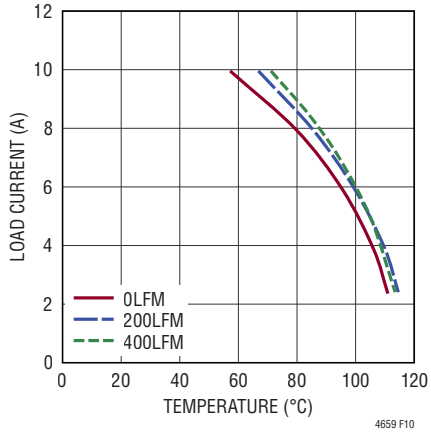

Figure 10. 3.3V to 1.5V Derating Curve, No Heat Sink

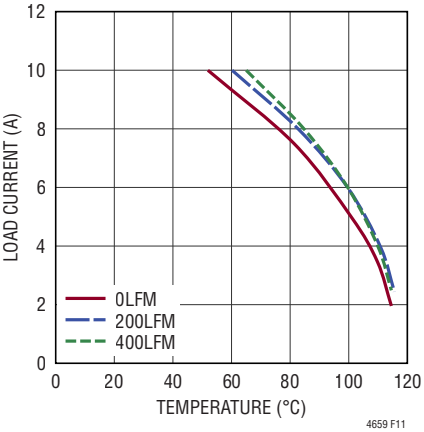

Figure 11. 3.3V to 2.5V Derating Curve, No Heat Sink

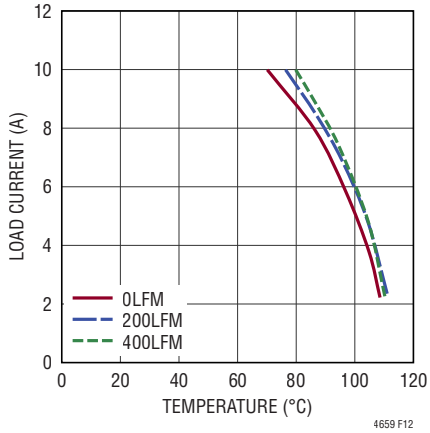

Figure 12. 5V to 1V Derating Curve, No Heat Sink

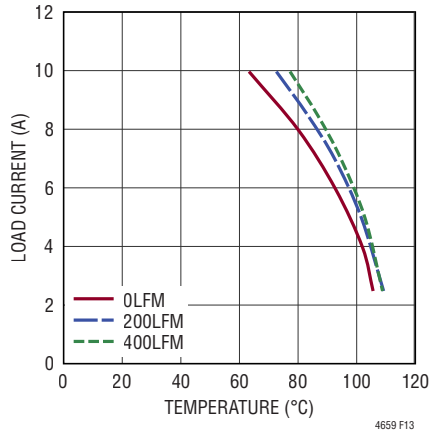

Figure 13. 5V to 1.5V Derating Curve, No Heat Sink

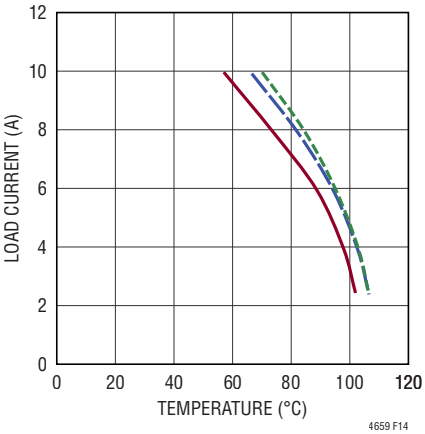

Figure 14. 5V to 2.5V Derating Curve, No Heat Sink

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value, which is very close. Table 6 and Table 7 provide equivalent thermal resistances for 1.5V and 2.5V outputs with and without airflow. **The Pin Configuration section shows the simulation data for the worst-case scenario.** Table 5 to Table 7 provide equivalent thermal resistances for 1.0V, 1.5V and 2.5V outputs with and without airflow. The derived thermal resistances in Table 5 to Table 7 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four-layer board with two ounces of copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 76mm × 76mm.

Table 5. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9, Figure 12	3.3, 5	Figure 7, Figure 8	0	None	21
Figure 9, Figure 12	3.3, 5	Figure 7, Figure 8	200	None	18
Figure 9, Figure 12	3.3, 5	Figure 7, Figure 8	400	None	17

Table 6. 1.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 10, Figure 13	3.3, 5	Figure 7, Figure 8	0	None	22
Figure 10, Figure 13	3.3, 5	Figure 7, Figure 8	200	None	19
Figure 10, Figure 13	3.3, 5	Figure 7, Figure 8	400	None	18

Table 7. 2.5V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 11, Figure 14	3.3, 5	Figure 7, Figure 8	0	None	23
Figure 11, Figure 14	3.3, 5	Figure 7, Figure 8	200	None	18
Figure 11, Figure 14	3.3, 5	Figure 7, Figure 8	400	None	17

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Table 8. Output Voltage Response vs Component Matrix (See Typical Application) 0A to 5A Load Step Typical Measured Values

C_{IN} CERAMIC VENDORS	VALUE (µF)	PART NUMBER	C_{OUT} VENDORS	VALUE (µF)	PART NUMBER
Taiyo Yuden	10	EMK212BB7106MG-T	Murata	22	GRM188R60J226MEA0D
Murata	22	GRM188R61A226ME15D	Murata	100	GRM21BR60J107ME15K

V_{OUT} (V)	C_{IN} (CERAMIC) (µF)	C_{IN} (BULK)	C_{OUT} (CERAMIC) (µF)	C_{FF} (pF)	V_{IN} (V)	DROOP (mV)	P-P Deviation (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	LOAD STEP SLEW RATE (A/µs)	FREQ. (kHz)
0.5	10 ×2	150	100 + 22 ×2	Open	3.3	40	78	5	5	5	1000
0.8	10 ×2	150	100 + 22 ×2	Open	3.3	45	92	10	5	5	2000
0.8	10 ×2	150	100 + 22 ×2	Open	5	45	90	10	5	5	2000
1	10 ×2	150	100 + 22 ×2	Open	3.3	55	109	10	5	5	2000
1	10 ×2	150	100 + 22 ×2	Open	5	55	105	10	5	5	2000
1.5	10 ×2	150	100 + 22 ×2	Open	3.3	80	157	10	5	5	2000
1.5	10 ×2	150	100 + 22 ×2	Open	5	80	156	10	5	5	2000
2.5	10 ×2	150	100 + 22 ×2	Open	3.3	120	239	15	5	5	2000
2.5	10 ×2	150	100 + 22 ×2	Open	5	120	241	15	5	5	2000
3.3	10 ×2	150	100 + 22 ×2	Open	5	120	291	15	5	5	2000

Safety Considerations

The LTM4659 modules do not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow-blow fuse with a rating twice the maximum input current must be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

Layout Checklist/Example

The high integration of LTM4659 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high-current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins as close as possible to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated GND ground copper area for components connected to signal pins. Connect the AGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, RUN, and COMP pins together. Use an internal layer to closely connect these pins together.
- Bring out test points on the signal pins for monitoring.

Figure 15 shows a good example of the recommended layout.

APPLICATIONS INFORMATION

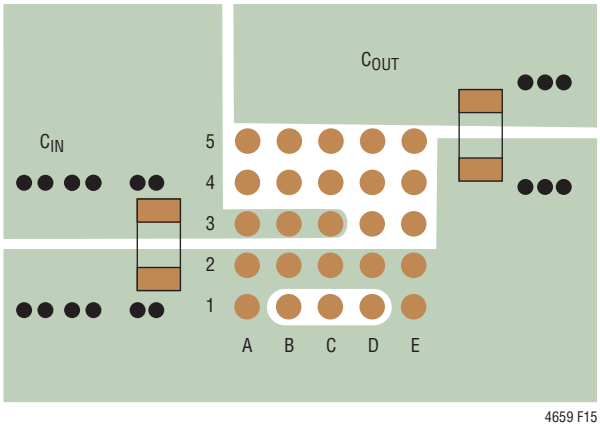


Figure 15. Recommended PCB Layout

TYPICAL APPLICATION

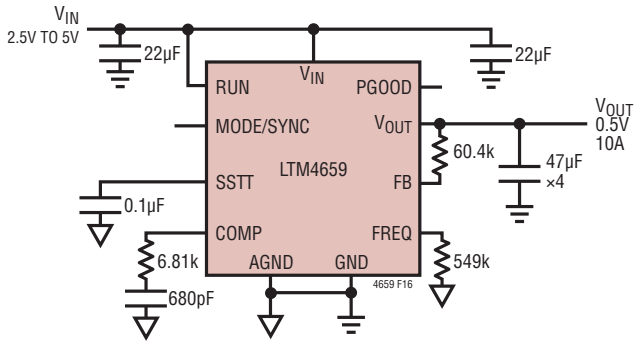


Figure 16. High Efficiency, 1MHz, 0.5V, 10A Forced Continuous Mode, Low Part Count

TYPICAL APPLICATIONS

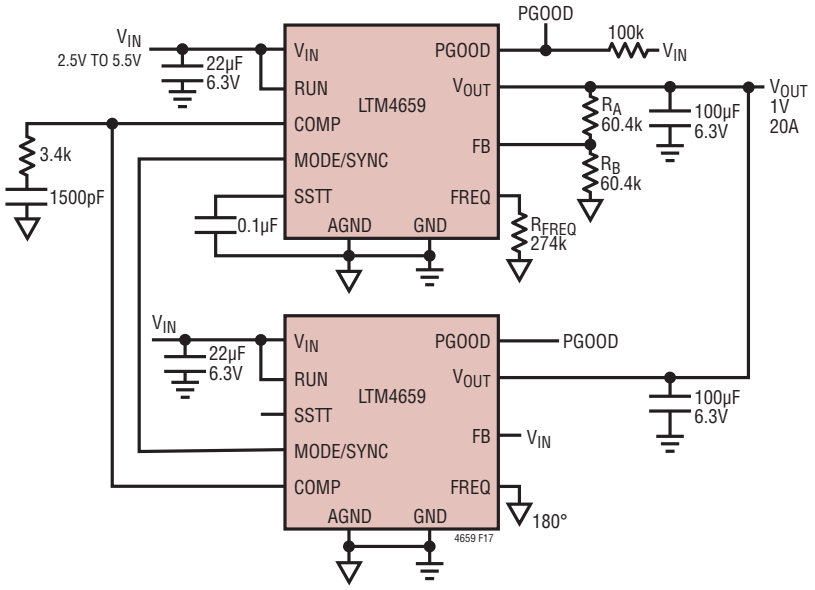


Figure 17. Dual-Phase Application with 180° Phase

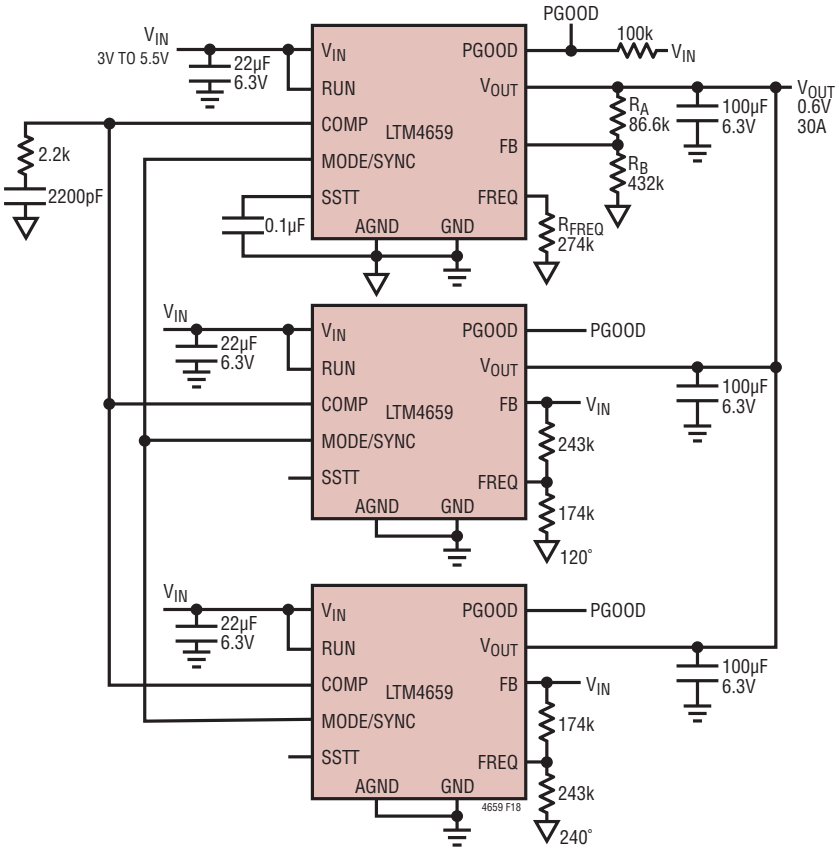


Figure 18. Three-Phase Application

TYPICAL APPLICATION

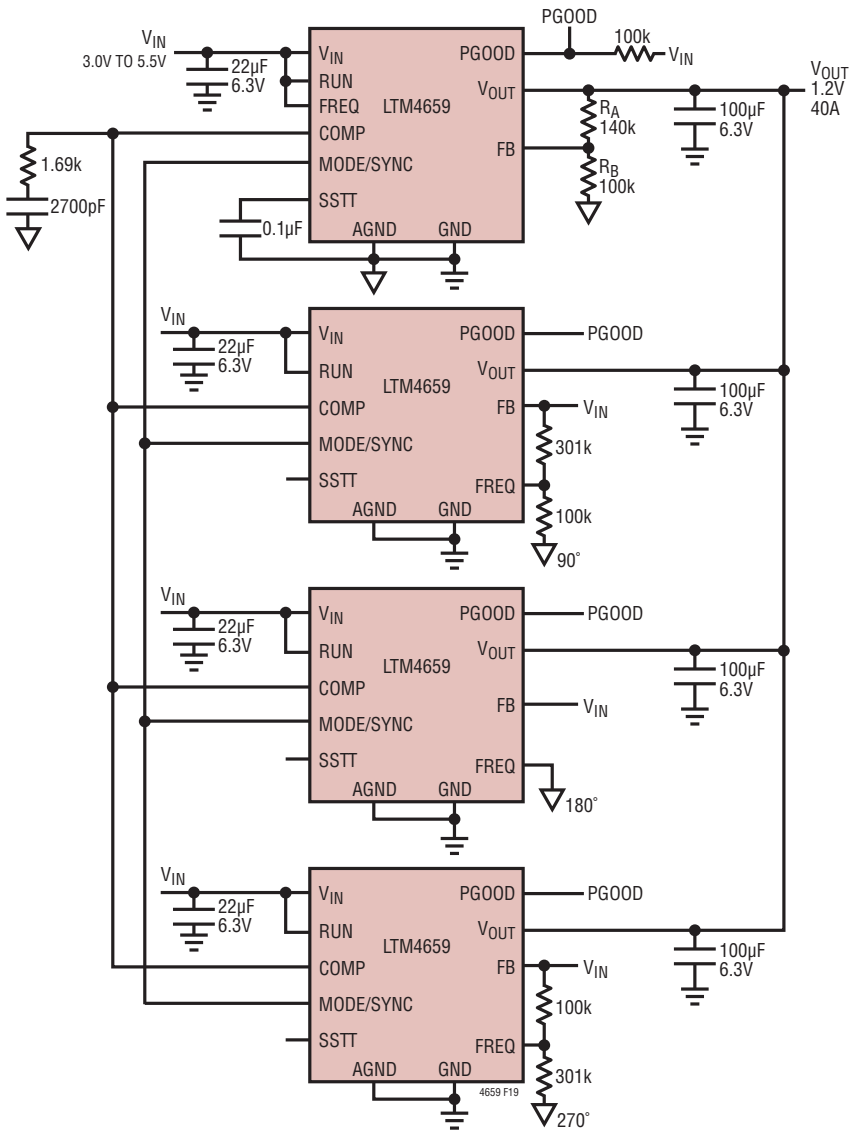


Figure 19. Four-Phase Application

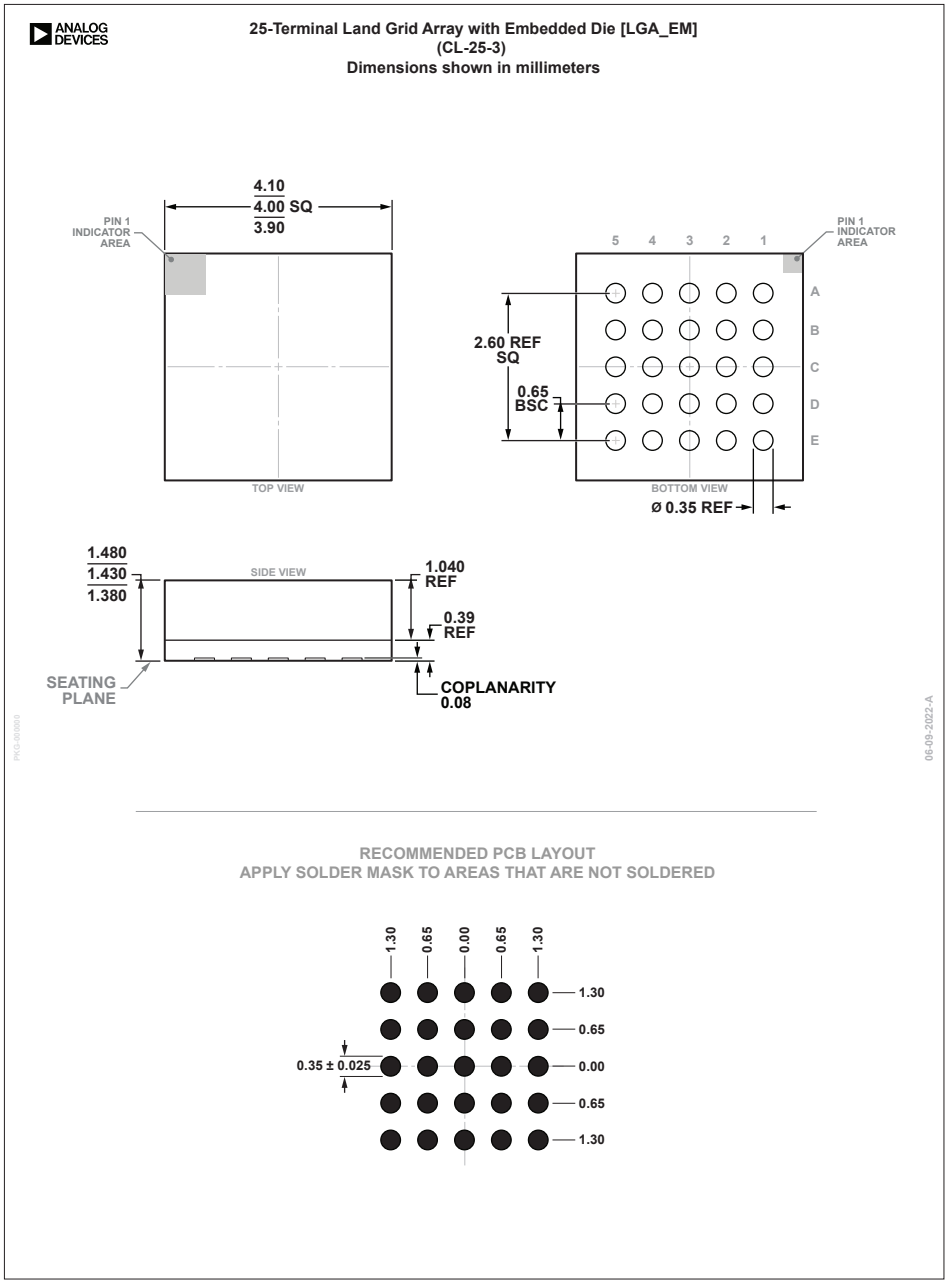
PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

Table 9. LTM4659 Component Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	GND	A2	GND	A3	V_{IN}	A4	COMP	A5	RUN
B1	SW	B2	GND	B3	V_{IN}	B4	FB	B5	V_{OUT}
C1	SW	C2	GND	C3	V_{IN}	C4	AGND	C5	V_{OUT}
D1	SW	D2	GND	D3	MODE/SYNC	D4	SSTT	D5	V_{OUT}
E1	GND	E2	GND	E3	PGOOD	E4	FREQ	E5	V_{OUT}

PACKAGE DESCRIPTION

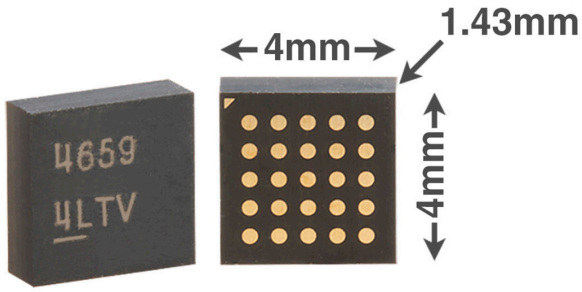


REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
0	04/24	Initial Release.	—

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4658	Low V_{IN}, 10A Silent Switcher 2 µModule Regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ V_{IN}, 4mm × 4mm × 4.32mm LGA, 4mm × 4mm × 4.62mm BGA
LTM4691	Low V_{IN}, Ultrathin, Dual 2A µModule Regulator	2.25V ≤ V_{IN} ≤ 3.6V, 0.5V ≤ V_{OUT} ≤ 2.5V, 3mm × 4mm × 1.18mm LGA, 3mm × 4mm × 1.48mm BGA
LTM4710-1	Low V_{IN}, Quad 8A Silent Switcher µModule Regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 3.6V, 6mm × 12mm × 3.54mm LGA
LTM4693	Low V_{IN}, Ultrathin, 2A Buck-Boost µModule Regulator	2.6V ≤ V_{IN} ≤ 5.5V, 1.8V ≤ V_{OUT} ≤ 5.5V, 3.5mm × 4mm × 1.25mm LGA
LTM4611	Ultralow V_{IN}, 15A µModule Regulator	1.5V ≤ V_{IN} ≤ 5.5V, 0.8V ≤ V_{OUT} ≤ 5V, 15mm × 15mm × 4.32mm LGA
LTM4670	Low V_{IN}, Quad 10A µModule Regulator	2.25V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ IN, 7.5mm × 15mm × 4.65mm BGA

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