Vol 56 No 1—March 2022

ANALOG DEVICES
AHEAD OF WHAT'S POSSIBLE™

AnalogDialogue

Level-Setting DAC Calibration for ATE Pin Electronics

Minhaaz Shaik, Product Applications Engineer

Abstract

This article provides the methodology to calibrate digital-to-analog converters (DACs) specifically for pin electronic drivers, comparators, load, PMU, and DPS. DACs have nonlinear properties such as differential nonlinearity (DNL) and integral nonlinearity (INL), which can be minimized with the use of gain and offset adjustments. This article describes how to make those corrections for improved level-setting performance.

Introduction

Automated test equipment (ATE) describes testing apparatuses designed to perform a single or sequence of tests on one device or multiple devices at a time. Different types of ATE tests electronics, hardware, and semiconductor devices. Timing devices, DACs, ADCs, multiplexers, relays, and switches are the supporting blocks in the tester or ATE system. These pin electronic devices can deliver signals and power with precise voltages and currents. These precision signals are configured by the level-setting DACs. In the ATE portfolio, some pin electronic devices have calibration registers, and some calibration settings are stored off-chip. This article describes the DACs' function, errors, and calibration via gain and offset adjustments.

Digital-to-Analog Converter (DAC)

A DAC is a type of data converter that converts digital inputs to corresponding analog output levels. An N-bit DAC can support 2^N output levels. A higher number of bits corresponds to a higher DAC output resolution.

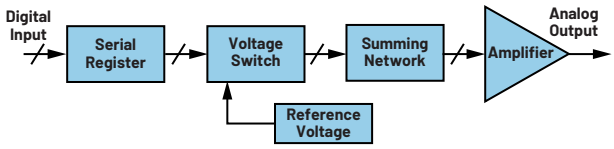

Figure 1. A digital-to-analog converter (DAC) block diagram.

First, the N-bit digital input is provided to a DAC serial register. The voltage switch and resistor summing network converts the digital inputs to analog output levels. The transfer characteristics of the DAC plot are shown in Figure 2. For a 3-bit DAC, 2^3 digital input yields eight analog output levels.

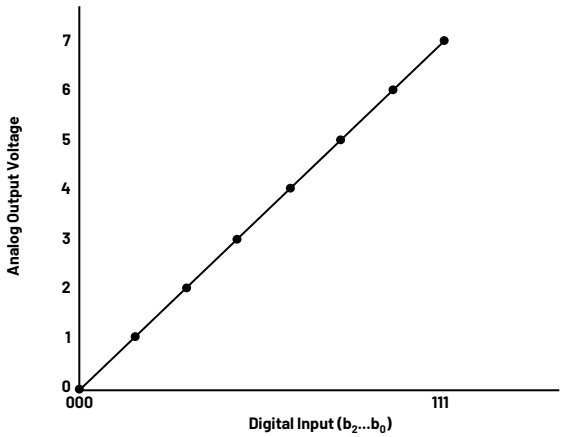

Figure 2. Ideal transfer function of a 3-bit DAC.

DAC Errors

In the real world, converters are not ideal. Because of the variance in resistance values, interpolation, and sampling, the DAC transfer function will not be a straight line, or linear. These errors are namely referred to as differential nonlinearity (DNL) and integral nonlinearity (INL). DNL is the maximum deviation of the output levels from ideal step sizes. It is derived from the difference between two successive output voltage levels. INL is the maximum deviation of the input/output characteristic from the ideal transfer function. With the gain and offset corrections, the INL errors can be reduced.

The INL in Figure 3 shows the deviation between actual transfer function and ideal transfer function. The gain error of the DAC indicates how well the slope of the linear approximation of the actual transfer function matches the slope of the ideal transfer function. Adjusting the gain will affect the angle of the linear approximation when graphed. The offset error is the difference between the measured value and chosen desired zero-offset point. Adjusting the offset will shift the entire linear approximation up or down accordingly. The INL of a single code is the sum of both gain error and offset error at any given point. After calibration, the transfer function can be a line drawn between end points once the gain and offset errors have been minimized.

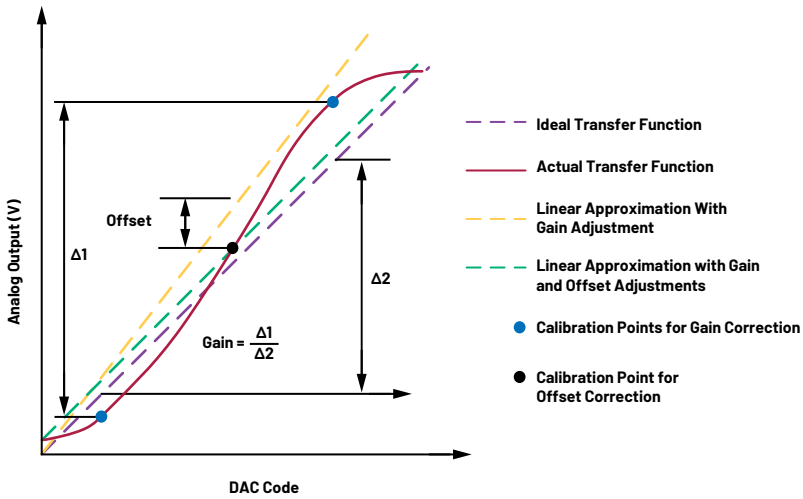

Figure 3. INL error transfer function.

Calibration Routine

The user can establish a calibration routine to reduce DAC nonlinearities using gain and offset corrections. The following procedure explains the step-by-step process of an example calibration routine.

For an N-bit DAC:

$$Maximum\ Code\ (MC) = (2^N - 1)$$

$$Voltage\ Range\ (V_{RANGE}) = Maximum\ DAC\ Output\ Voltage\ (V_{MAX}) - Minimum\ DAC\ Output\ Voltage\ (V_{MIN}) = 4 \times V_{REF}$$

$$DAC\ Input\ Code\ (Without\ Calibration) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN})$$

- Gain correction (GC):

DACs tend to become less linear at the lowest and highest binary values. Therefore, it is recommended to choose calibration points within 5% to 10% in between the outer binary values or EC table recommended calibration points. For the following calculation, we assume 5% calibration points.

- Set the DAC input to 5% above the lowest binary value. Calculate the expected voltage output and record it as IDEAL1. Measure the output voltage and record it as MEAS1.
- Set the DAC input 5% below the highest binary value. Calculate and record IDEAL2. Measure the output voltage and record it as MEAS2.
- $$GC = \frac{MEAS2 - MEAS1}{IDEAL2 - IDEAL1}$$

  $$DAC\ Input\ Code\ (with\ Gain\ Correction)$$
- $$= \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN}) \times \frac{1}{GC}$$

- Offset correction (OC):

The desired zero-offset point varies by application. The user should define the best value based on their application. Some users may prefer to use zero volts to get an exact ground reference point. Some users prefer to use the midpoint of their operating range to minimize the overall INL error.

- Apply the gain correction of the DAC to the slope of the voltage-to-code equation to establish unity gain.
- Choose the desired zero-offset voltage point and record it as IDEAL3. Calculate the code using your updated voltage-to-code equation. Program your calculated code, then measure the output voltage and record it as MEAS3.
- $$OC = MEAS3 - IDEAL3$$
- $$DAC\ Input\ Code\ (with\ Gain\ and\ Offset\ Correction) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN} - OC) \times \frac{1}{GC}$$

Example 1

Consider the MAX32007, an octal DCL with integrated level-setting DACs and PMU switches. The MAX32007 has internal DACs for level-setting VDH, VDL, VDT/VCOM, VCH, VCL, VCPH, and VCPL. These DACs do not have internal calibration registers. To calibrate the DACs, follow this procedure:

- Power up the MAX32007 evaluation (EV) kit by following the instructions in the EV kit data sheet.
- Connect the SMB connectors DATAOA and NTRMOA to 1.2 V.
- Connect the SMB connectors NDATAOA and TRMOA to ground through a 50 Ω terminator.
- Connect the EV kit to a Windows® 10 PC through a USB cable. Open the MAX32007 EV kit software (GUI).
- $$VDH\ DAC\ Resolution = N = 14$$

  $$Maximum\ Code = (MC) = 2^N - 1 = 16383$$

  $$Voltage\ Range\ (V_{RANGE}) = Maximum\ DAC\ Output\ Voltage\ (V_{MAX}) - Minimum\ DAC\ Output\ Voltage\ (V_{MIN}) = 7.5 - (-2.5) = 10$$

  $$VDH\ DAC\ Input\ Code\ (Without\ Calibration) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN})$$

Apply the DAC voltage levels and driver settings as shown in Figure 4. Note that the lowest operating VDH DAC value is -1.5 V, the highest operating value is 4.5 V; in this case, the zero-offset point value is 1.5 V.

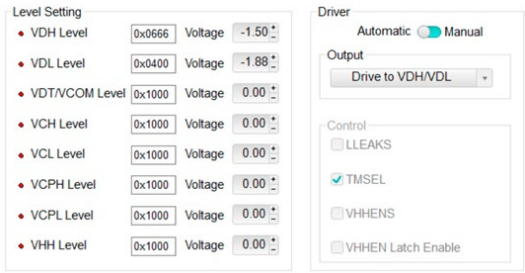

Figure 4. DAC-level setup of the MAX32007 using eval board software.

- Apply VDH = –1.5 V and measure the output voltage value.
- Apply VDH = 4.5 V and measure the output voltage value.
- Gain correction = Difference between measure output voltage values/difference between ideal values. For example, (4.501 – (–1.497)) / (4.5 – (–1.5)) = 0.999667
- After applying gain correction,

$$VDH\ DAC\ Input\ Code\ (with\ Gain\ Correction) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN}) \times \frac{1}{GC}$$

To apply gain correction, open **Menu → Options → Calibration**, as shown in Figure 5.

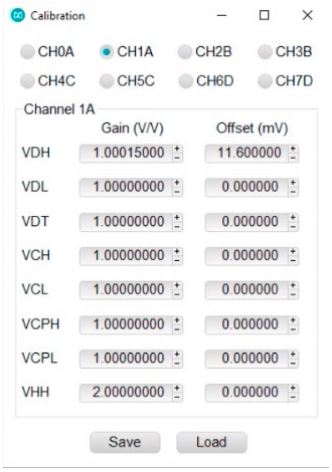

Figure 5. Calibration menu of the MAX32007 DAC.

- Apply VDH = 1.5 V (with gain correction code) and measure the output voltage value.
- Offset correction = Measure output value – Ideal value. For example, (1.502 – 1.5) = 0.002.
- After applying gain and offset correction,

$$VDH\ DAC\ Input\ Code\ (with\ Gain\ and\ Offset\ Correction) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN} + OC) \times \frac{1}{GC}$$

Example 2

Consider the MAX9979, a dual DCL with integrated level-setting DACs and PMU. The MAX9979 has internal DACs for level-setting VDH, VDL, VDT, VCH, VCL, VCPH, VCPL, VCOM, VLDH, VLDL, VIN, VIOS, CLAMPHI/VHH, and CLAMPLO. These DACs have internal calibration registers. In Example 1, the DAC input codes are adjusted to minimize the INL error. In Example 2, the DAC input code remains the same and the calibration registers adjust the output stage buffer to minimize the INL errors, as depicted in Figure 6. To calibrate the DACs, use the following procedure:

- Power up the MAX9979 EV kit by following the instructions in the EV kit data sheet.
- Connect the SMB connectors DATAOA and NTRMOA to 1.2 V.
- Connect the SMB connectors NDATAOA and TRMOA to ground through the 50 Ω terminator.
- Connect the EV kit to a Windows 10 PC through a USB cable. Open the MAX9979 EV kit software (GUI).
- $VDH\ DAC\ Resolution = N = 16$

  $Maximum\ Code = (MC) = 2^{16} - 1 = 65535$

  $Voltage\ Range\ (V_{RANGE}) = Maximum\ DAC\ Output\ Voltage\ (V_{MAX}) - Minimum\ DAC\ Output\ Voltage\ (V_{MIN}) = 7.5 - (-2.5) = 10$

  $VDH\ DAC\ Input\ Code\ (Without\ Gain\ Correction) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN})$
- Apply the DAC voltage levels and driver settings as shown in Figure 7. Note that the VDH DAC lowest recommended value is –1.5 V, the highest recommended value is 4.5 V, while the zero-offset point value is at 1.5 V.

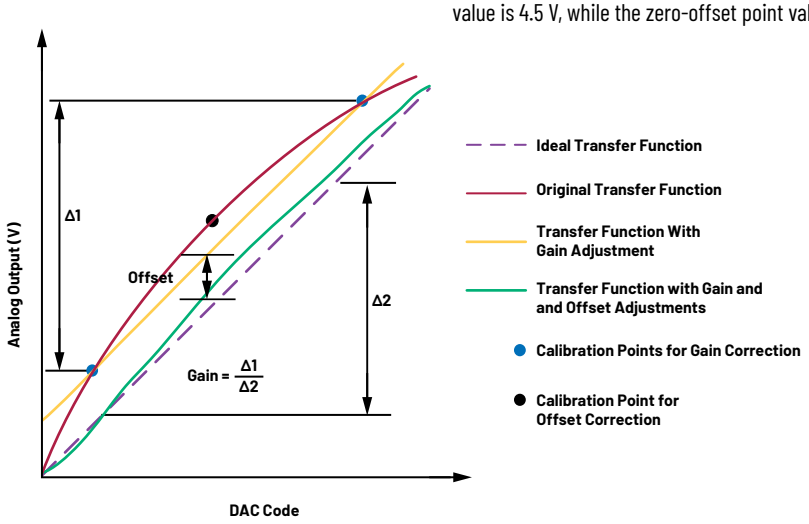

Figure 6. INL error correction for DACs with calibration registers.

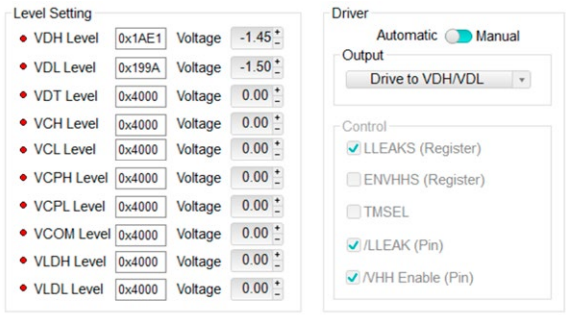

Figure 7. DAC-level setup of the MAX9979 using the eval board software.

- Apply VDH = –1.45 V and measure the output voltage value.
- Apply VDH = 6.5 V and measure the output voltage value.
- Gain correction = Difference between measure output voltage values/ Difference between ideal values. For example, (6.501 V – (–1.455 V))/(6.5 V – (–1.45 V)) = 1.0007 V.
- After applying gain correction,

$$VDH\ DAC\ Input\ Code\ (with\ Gain\ Correction) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN}) \times \frac{1}{GC}$$

- Apply VDH = 1.5 V (with gain correction code) and measure the output voltage value.
- Offset correction = Measure output value – Ideal value. For example (1.502 – 1.5) = 0.002.
- After applying gain and offset correction,

$$VDH\ DAC\ Input\ Code\ (with\ Gain\ and\ Offset\ Correction) = \left(\frac{MC}{V_{RANGE}}\right) \times (V_{OUT} - V_{MIN} + OC) \times \frac{1}{GC}$$

Note: gain and offset corrections can be applied on **Menu → Options → Change → Calibration**, as shown in Figure 8. Conversion of gain and offset corrections to gain and offset codes are given in the MAX9979 data sheet.

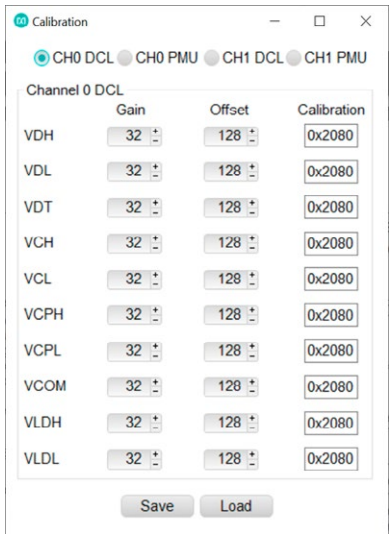

Figure 8. Calibration register setup for the MAX9979.

About the Author

Minhaaz Shaik is a member of the technical staff at Analog Devices with more than five years of experience as an applications/ systems engineer in the analog and mixed-signal domain. Minhaaz mainly focuses on product lines such as automated test equipment (ATE) pin electronics, ADCs, DACs, and supervisory and interface ICs. She is a highly skilled professional in electronic system design, lab evaluation, automation, customer support, and technical writing, and has significant knowledge in SPICE simulations and circuit design. She can be reached at minhaaz.shaik@analog.com.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

MAX32007EVKIT#