Evaluation Board User Guide

EVAL-LT8418-AZ

100V Half-Bridge GaN Driver with Smart Integrated Bootstrap Switch

General Description

The EVAL-LT8418-AZ evaluation circuit features the LT8418 driving two 100V enhanced Gallium Nitride (eGaN) FETs in a half-bridge configuration. The circuit is optimized as a buck converter, but it can be used as a boost converter or other converter topologies consisting of a half-bridge. The evaluation circuit can deliver up to 10A with good thermal management.

An external single or two PWM signals are required to drive the board, depending on the configuration. In the single-input setup, the dead time circuitry on the board is utilized to generate the complement signal and set the dead time. The dead time circuitry is bypassed in the dual-input setup.

The LT8418 driver has powerful 0.2Ω pull-down and 0.6Ω pull-up drivers driving two 100V GaN FETs. It also integrates a smart integrated bootstrap switch to generate a balanced bootstrap voltage from V_{CC} with a minimum dropout voltage. The LT8418 provides split gate drivers to adjust the turn-on and turn-off slew rates of GaN FETs to suppress ringing and optimize EMI performance.

Design files for this circuit board are available.

Performance Summary (T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage[1]	V_{IN}					80	V
Output Voltage	V_{OUT}					80	V
Output Current[2]	I_{OUT}					10	A
Auxiliary Supply Voltage	V_{AUX}			5.5		80	V
Gate Driver Supply Voltage	V_{CC}	V_{AUX} = 6V, R1 = 604kΩ, R4 = 200kΩ			5		V
PWM Logic Input Voltage Threshold	V_{PWM_TH}	V_{CC} = 5V	High PWM input	2.1		3.4	V
			Low PWM input	1.2		2.2	
PWM Logic Input Minimum Width	t_{PWM_MIN}				11		ns
Switching Frequency[3]	f_{SW}			0.1	1	10	MHz
Dead Time from BG Falling to TG Rising	$t_{d(BG\_TG)}$	Open V_{IN}, single PWM input signal, R3 = 30Ω, R6 = 47Ω			8.7		ns
Dead Time from TG Falling to BG Rising	$t_{d(TG\_BG)}$				4.4		ns
TG Rise Time	$t_{Rise(TG)}$	Open V_{IN}, single PWM input signal, R9 = 5.6 Ω, R12 = 3Ω			13.3		ns
TG Fall Time	$t_{Fall(TG)}$				0.8		ns
BG Rise Time	$t_{Rise(BG)}$				6.1		ns
BG Fall Time	$t_{Fall(BG)}$				0.9		ns
Efficiency	η	V_{IN} = 48V, I_{OUT} = 10A	V_{OUT} = 24V, 500kHz		97.5		%
			V_{OUT} = 24V, 1MHz		97.4		%
			V_{OUT} = 12V, 500kHz		96.2		%
			V_{OUT} = 12V, 1MHz		95.5		%

1. *Maximum input voltage depends on inductive loading. Maximum switch node ringing must be kept under 100V for INN100W070A.*
2. *Maximum output current depends on INN100W070A FET temperature, affected by switching frequency, input voltage, output voltage, and thermal management. Make sure to monitor the die temperature when setting the output current.*
3. *At high switching frequencies, switching loss is dominant. Input voltage and output current should be reduced to prevent overheating of the GaN FETs.*

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Quick Start Procedure

The EVAL-LT8418-AZ evaluation circuit is a power stage used to evaluate the performance of the LT8418. See *Figure 1* for proper measurement equipment setup and use the following procedure:

1. With power off, connect the input power supply to the board through the V_{IN} and GND terminals. Connect the auxiliary power supply to the AUX INPUT and GND terminals. Connect the load to the V_{OUT} and GND terminals. Connect the function generator output to the INT and GND pins of header J1.
2. Turn on the auxiliary power supply at 6V.
3. Set the function generator to output a 5V, 1MHz, 50% duty cycle, high-Z output pulse waveform.
4. Turn on the input power supply at 0V, 7A limit. Increase the voltage slowly to 48V.
5. Check for the proper output voltage, which should be 24V (±5%).
6. Once the proper output voltage is established, adjust the input voltage and load current within the operating range, and observe the gate signals, switch node voltage, voltage ripple, efficiency, and other parameters.
7. When testing finishes, turn off the equipment in the following order: electronic load, power supply, function generator, and auxiliary power supply at last.

NOTE: When probing the gate signals or switch node, it is recommended to use the ground spring to avoid parasitic inductance in the long ground lead. Measure the input or output voltage ripple by touching the probe tip directly across the V_{IN} (J2) and GND (J3), or V_{OUT} (J4) and GND (J5) terminals.

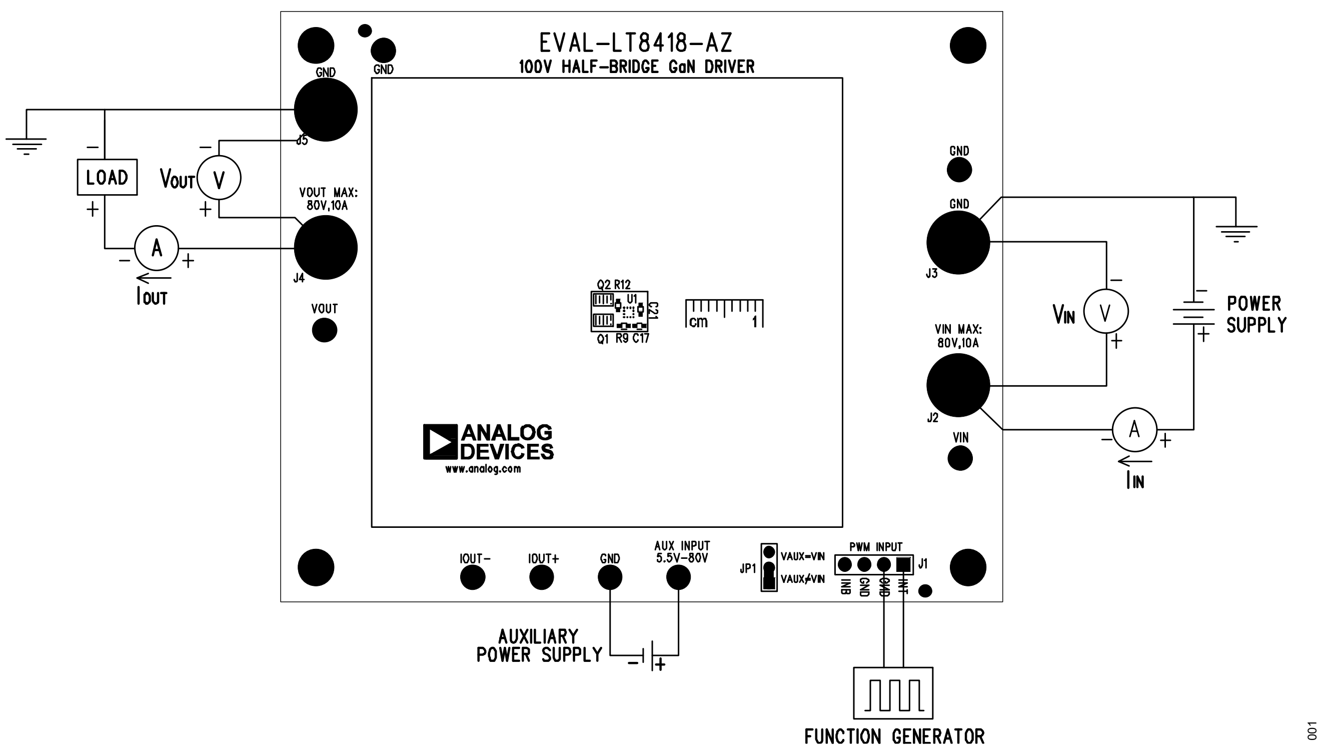

Figure 1. EVAL-LT8418-AZ Board Connections in Single-PWM-Input Control Mode [1]

[1] *GaN FETs and LT8418 are placed on the top layer. The inductor and capacitors are placed on the bottom layer.*

Output Voltage and Power

The EVAL-LT8418-AZ can be configured as either a buck or a boost converter, or other converter topologies consisting of a half-bridge with maximum input and output voltages of 80V. However, the converter is optimally designed to convert $48V_{IN}$ to $24V_{OUT}$ at 1MHZ, delivering up to 10A with a heat sink or forced airflow. At full load with forced airflow, although the board can deliver 240W, the top FET heats up significantly. Therefore, a heat sink is recommended if this operating condition is expected over an extended period. See the *Thermal Considerations* section for more details on using a heat sink.

The conversion ratio can be adjusted by changing the duty cycle of the PWM input signal(s), while the switching frequency is set by the PWM input signal frequency. To optimize the converter efficiency at a different power specification, passive power components inductors and input/output capacitors should be resized appropriately. The dead times must also be adjusted to minimize the loss during the dead time. *Figure 3* and *Figure 4* show the converter efficiency versus the load current at different operating conditions.

LDO Setting

An LDO (U3) is used to supply power to the LT8418 and dead time circuitry. The output voltage V_{CC} of the LDO is set to 5V in the default configuration, but it can be adjusted by changing R2 and R4 values. The input power of U3 comes from either a default auxiliary power supply, AUX INPUT, ranging from 5.5V to 80V, or directly from the board's input power supply, which can be selected by changing the position of jumper JP1.

Control Mode

The EVAL-LT8418-AZ circuit is an open-loop half-bridge converter without a feedback network and control loop. Hence, the board requires two complementary PWM signals to drive the INT and INB pins of the LT8418. These signals come from either one (in single-PWM-input mode) or two (in dual-PWM-input mode) external PWM signals provided by a function generator or microcontroller.

The single-PWM-input mode is the default control scheme of this evaluation board. In this mode, only a single PWM output of the function generator is connected to header J1, as shown in *Figure 1*. The positive terminal is tied to the leftmost pin (labeled INT), while the negative terminal is tied to the middle pin (labeled GND).

Alternatively, two separate PWM signals can be applied to header J1 to control INT and INB pins independently in the dual-PWM-input mode. To enable this control mode, some component-level modifications are required to bypass the RC filters. Specifically, R5 must be removed and R7, R3, and R6 must be shorted with 0Ω resistors. The positive sides of INT and INB inputs are applied at the leftmost pin (labeled INT) and rightmost pin (labeled INB) of header J1, respectively. As the dead time circuitry no longer generates dead times between INT and INB input signals, careful control must be taken in this control mode to prevent a shoot-through incident. *Table 1* lists the circuit configurations of two control modes.

Table 1. Circuit Configurations for Control Modes

Control Mode	R5	R7	R3	R6
Single PWM Input [1]	Shorted	Open	30Ω [2]	47Ω [2]
Dual PWM Inputs	Open	Shorted	Shorted	Shorted

[1] *Default configuration*

[2] *Resistance value can be changed to adjust the dead time*

Dead Time

In the single-PWM-input control mode, the dead times of gate signals are set by the dead-time circuitry consisting of two inverters and RC filters. The input PWM signal is first inverted and split into two complementary signals by the Schmitt-trigger inverter U2. The two signals are then delayed by the RC filters, setting the dead times before being inverted again by another inverter U4. These two resulting signals are applied to the INT and INB pins driving the LT8418. The default dead times on the board are optimized for $48V_{IN}$, $24V_{OUT}$, 1MHz f_{SW}, and 10A I_{OUT} operating conditions. However, the dead times can be adjusted by changing R3 and R6 values to evaluate the impact of dead time on efficiency. When changing the dead times, careful design must be taken to avoid a shoot-through condition. *Figure 2* shows the relationship between the resistor values and dead times between INT and INB signals.

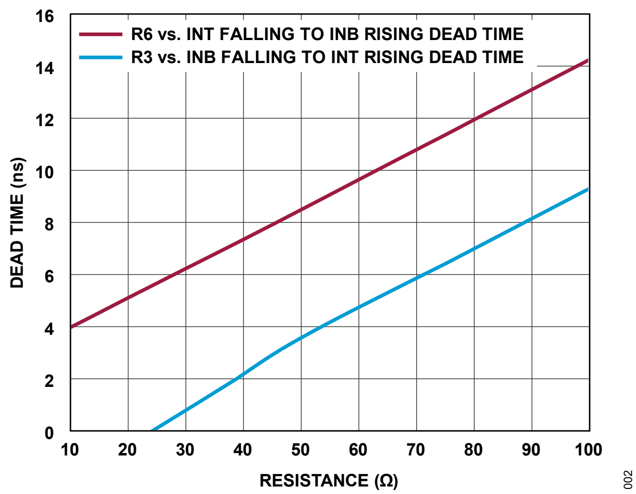

Figure 2. Dead Times vs. Resistor Values

Thermal Considerations

At high switching frequencies and high output power, care must be taken to prevent overheating on the GaN FETs. For better thermal management, the EVAL-LT8418-AZ is equipped with four mechanical spacers that can be used to attach a heat sink (527-45AB) to the top layer. Since all the high-profile components are placed on the bottom layer, the heat sink is easily placed on the top layer against the surface of GaN FETs and the LT8418. A thermal pad should be inserted under the heat sink to ensure good contact, improving thermal dissipation.

Measurement Considerations

A high-speed differential probe such as the IsoVu probe from Tektronix is recommended for measuring the high-side gate voltage at header TP10. It has low parasitic elements, suitable for measuring high-frequency waveforms. Low parasitic capacitance passive probes with ground springs are recommended for measuring voltage at other nodes. The surface-mount sockets (TP1-TP7) and headers (TP8-TP10) can be populated for easy probing.

Performance

(V_{IN} = 48V, T_A = 25°C, unless otherwise noted.)

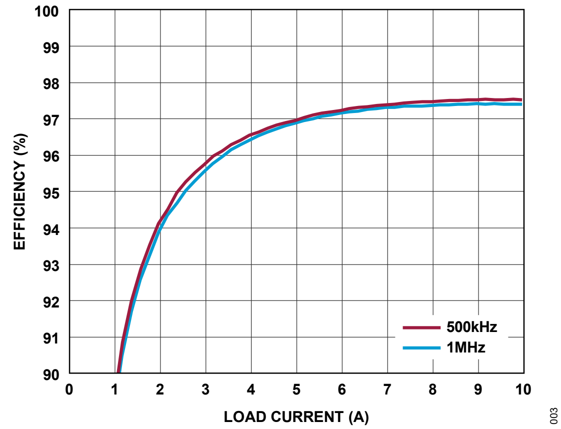

Figure 3. Efficiency vs. Load Current at V_{OUT} = 24V (with Heatsink)

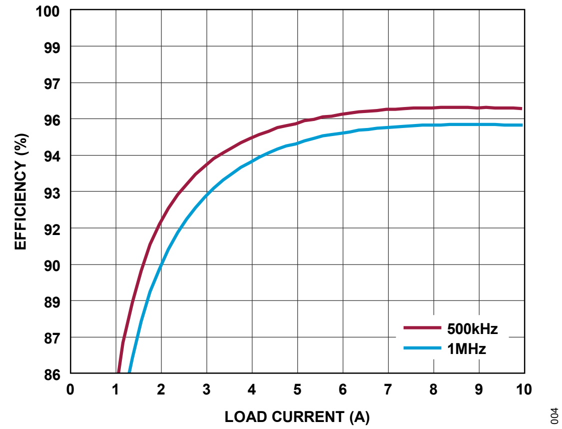

Figure 4. Efficiency vs. Load Current at V_{OUT} = 12V (with Heatsink)

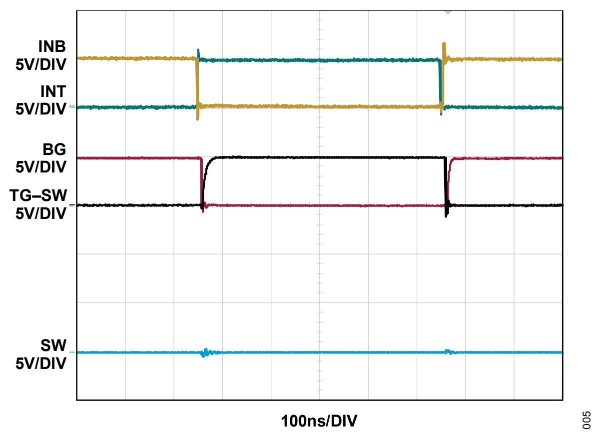

Figure 5. Steady-State Waveform at Open V_{IN}, F_{sw} = 1MHz

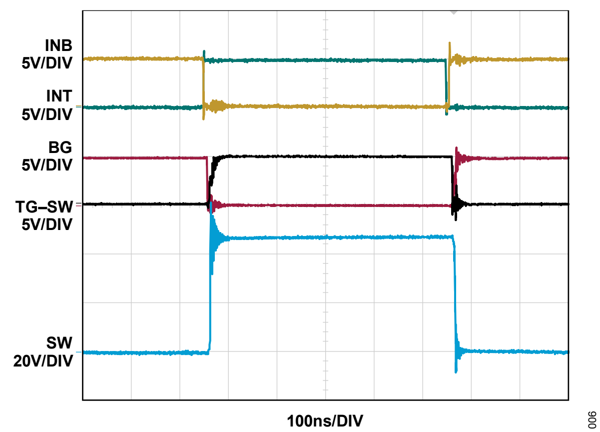

Figure 6. Steady-State Waveform at V_{OUT} = 24V, I_{OUT} = 0A, F_{sw} = 1MHz

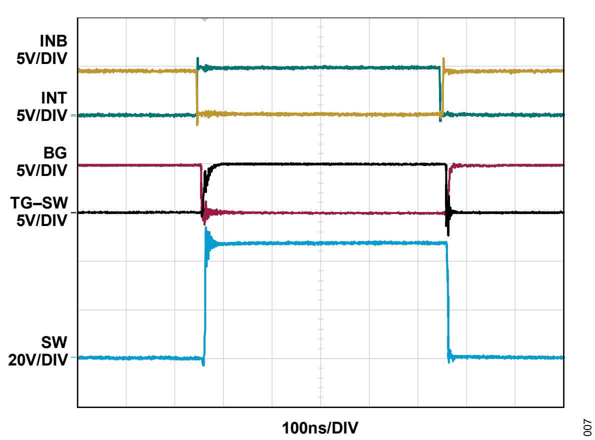

Figure 7. Steady-State Waveform at V_{OUT} = 24V, I_{OUT} = 10A, F_{sw} = 1MHz (with Heatsink)

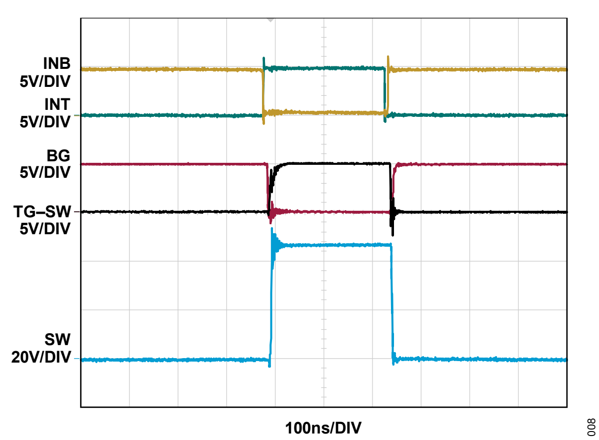

Figure 8. Steady-State Waveform at V_{OUT} = 12V, I_{OUT} = 10A, F_{sw} = 1MHz (with Heatsink)

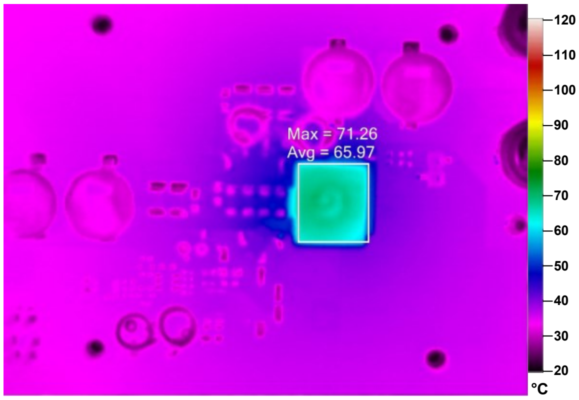

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Figure 9. Thermal Image of Bottom Layer at V_{OUT} = 24V, I_{OUT} = 6A, F_{sw} = 500kHz (Thermal Values are on L1)

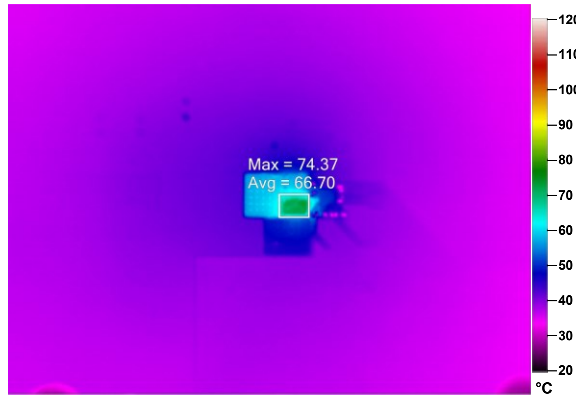

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Figure 10. Thermal Image of Top Layer at V_{OUT} = 24V, I_{OUT} = 6A, F_{sw} = 500kHz (Thermal Values are on Q1)

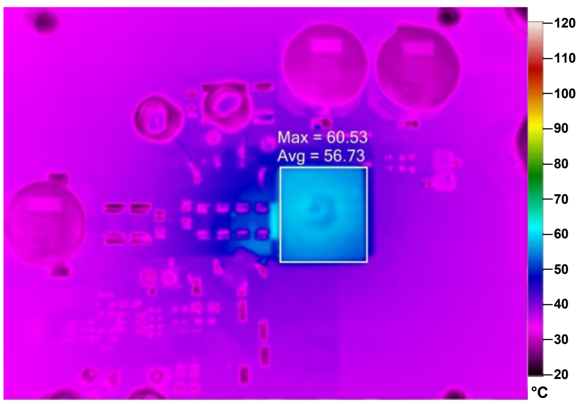

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Figure 11. Thermal Image of Bottom Layer at V_{OUT} = 24V, I_{OUT} = 6A, F_{sw} = 1MHz (Thermal Values are on L1)

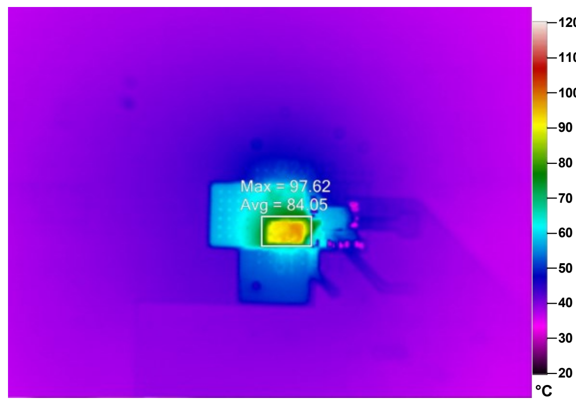

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Figure 12. Thermal Image of Top Layer at V_{OUT} = 24V, I_{OUT} = 6A, F_{sw} = 1MHz (Thermal Values are on Q1)

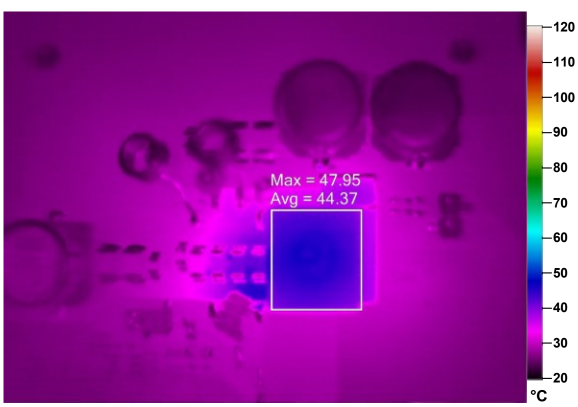

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Figure 13. Thermal Image of Bottom Layer at V_{OUT} = 24V, I_{OUT} = 8.5A, F_{sw} = 1MHz (with Airflow, Thermal Values are on L1)

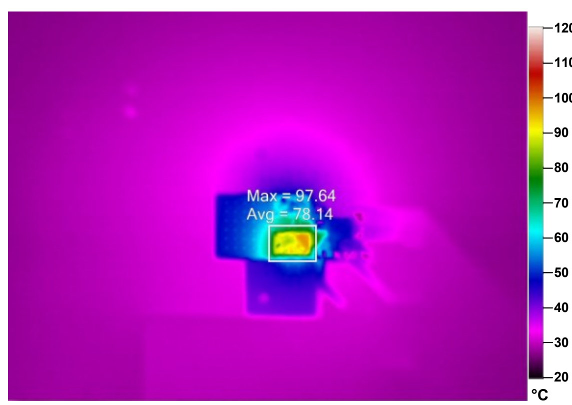

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Figure 14. Thermal Image of Top Layer at V_{OUT} = 24V, I_{OUT} = 6A, F_{sw} = 1MHz (with Airflow, Thermal Values are on Q1)

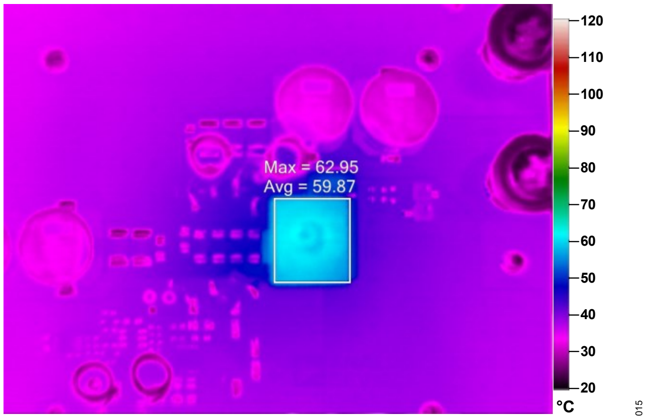

Figure 15. Thermal Image of Bottom Layer at V_{OUT} = 24V, I_{OUT} = 10A, F_{sw} = 1MHz (with Heat Sink, Thermal Values are on L1)

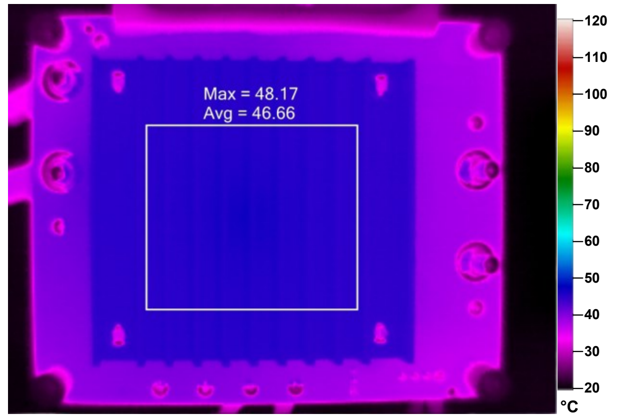

Figure 16. Thermal Image of Top Layer at V_{OUT} = 24V, I_{OUT} = 10A, F_{sw} = 1MHz (with Heat Sink, Thermal Values are on Heat Sink)

Bill of Materials

ITEM	QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER PART NUMBER
REQUIRED CIRCUIT COMPONENTS				
1	2	C1, C7	CAP., 100pF, C0G, 50V, 5%, 0402	MURATA, GRM1555C1H101JA01D
2	1	C2	CAP., 1µF, X7S, 100V, 10%, 0805, AEC-Q200	MURATA, GCM21BC72A105KE36L
3	3	C3, C16, C22	CAP., 0.1µF, X7R, 100V, 10%, 0805	TDK, C2012X7R2A104K125AA
4	2	C4, C20	CAP., 4.7µF, X7R, 16V, 10%, 0805	AVX, 0805YC475KAT2A
5	3	C5, C6, C18	CAP., 0.1µF, X7R, 16V, 10%, 0603	WURTH ELEKTRONIK, 885012206046
6	4	C8, C9, C10, C11	CAP., 4.7µF, X7S, 100V, 20%, 1206	MURATA, GRM31CC72A475ME11L
7	4	C12, C13, C26, C27	CAP., 47µF, ALUM ELECT, 100V, 20%, SMD, RADIAL, 1012, 150 CRZ Series, AEC-Q200	VISHAY, MAL215099905E3
8	5	C14, C15, C23, C24, C25	CAP., 4.7µF, X7S, 100V, 10%, 1210	MURATA, GRM32DC72A475KE01L
9	2	C17, C21	CAP., 0.1µF, X7R, 16V, 10%, 0402	MURATA, GRM155R71C104KA88D
10	2	C19, C28	CAP., 10pF, C0G, 50V, 5%, 0402	MURATA, GJM1555C1H100JB01D
11	2	D1, D2	DIODE, SCHOTTKY, 40V, 30mA, SOD-523	DIODES INC., SDM03U40-7
12	1	L1	IND., 4.7µH, PWR, 20%, 24A, 5.7mΩ, SMD, 11.8mm x 10.5mm x 10mm, AEC-Q200	COILCRAFT, XAL1010-472MEB
13	2	Q1, Q2	XSTR., ENHANCEMENT-MODE GaN FET, 100V, 29A, 2.5x1.5mm	INNOSCIENCE, INN100W070A
14	1	R1	RES., 604kΩ, 1%, 1/10W, 0603, AEC-Q200	VISHAY, CRCW0603604KFKEA
15	2	R2, R8	RES., 10kΩ, 1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW040210K0FKED
16	1	R3	RES., 30Ω, 1%, 1/16W, 0402	YAGEO, RC0402FR-0730RL
17	1	R4	RES.,200kΩ,1%,1/10W,0603	VISHAY, CRCW0603200KFKEA
18	3	R5, R10, R13	RES., 0Ω, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
19	1	R6	RES., 47Ω, 1%, 1/16W, 0402	VISHAY, CRCW040247R0FKED
20	1	R9	RES., 5.6Ω,1%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04025R60FNED
21	1	R11	RES., 0.005Ω, 1%, 2W, 2512, LONG-SIDE TERM, METAL, SENSE	OHMITE, FCSL64R005FER
23	1	R12	RES., 3Ω, 5%, 1/16W, 0402, AEC-Q200	VISHAY, CRCW04023R00FKED
24	2	R16, R17	RES., 0Ω, 1/10W, 0603, AEC-Q200	VISHAY, CRCW06030000Z0EA
25	1	U1	IC, 100V Half-Bridge GaN Driver, WLCSP-12	ANALOG DEVICES, LT8418ACBZ-R7
26	1	U2	IC, 3CH Schmitt-Trigger Inverter, VSSOP-8	TEXAS INSTRUMENTS, SN74LVC3G14DCUR
27	1	U3	IC, 250mA, 4V to 80V LDO Linear Reg, DFN-12	ANALOG DEVICES, LT3012EDE#PBF
28	1	U4	IC, Dual Schmitt-Trigger Inverter, SOT23-6	TEXAS INSTRUMENTS, SN74LVC2G14DBVR
OPTIONAL CIRCUIT COMPONENTS				
1	0	C29	CAP., OPTION, 0603	
2	2	D3, D4	LED, GREEN, WATER-CLEAR, 0805	LITE-ON, LTST-C170KGKT
3	1	R14	RES.,1kΩ, 5%, 1/10W,0603, AEC-Q200	VISHAY, CRCW06031K00JNEA
4	1	R15	RES., 100kΩ, 5%, 1/4W, 1206, AEC-Q200	VISHAY, CRCW1206100KJNEA
5	0	R7	RES., 0Ω, 1/16W, 0402	VISHAY, CRCW04020000Z0ED
HARDWARE – FOR DEMO BOARD ONLY				
1	8	E1 to E8	TEST POINT, TURRET, 0.064" MTG. HOLE, PCB 0.062" THK	MILL-MAX, 2308-2-00-80-00-00-07-0
2	1	J1	CONN., HDR., MALE, 1 x 4, 2.54mm, VERT, STR, THT	SAMTEC, TSW-104-07-L-S
3	4	J2 to J5	CONN., BANANA JACK, FEMALE, THT, NON-INSULATED, SWAGE, 0.218"	KEYSTONE, 575-4
4	1	JP1	CONN., HDR,MALE, 1 x 3, 2mm, VERT, ST, THT	WURTH ELEKTRONIK, 62000311121
5	4	MP1 to MP4	STANDOFF, NYLON, SNAP-ON, 0.625 (5/8"), 15.9mm	KEYSTONE, 8834

6	4	MP5 to MP8	STANDOFF, STEEL, ROUND, 5.1mm OD, 3.5mm ID, 1mm BODY LENGTH, 2.4mm OVERALL LENGTH, FEMALE, M2.5, THREADED, SMT	WURTH ELEKTRONIK, 9774010151R
7	0	MP9	HEATSINK, EXTRUDED, 1/2 BRICK DC/DC CVRTR, 2.28" x 2.40" x 0.45", HORZ, RECT, 11-FIN, ALUM, BLK ANODIZE	WAKEFIELD-VETTE, 527-45AB
8	0	MP10	HEAT SPREADER 100MMX100MM W/ADH	WURTH ELEKTRONIK, 4051100100017
9	0	TP1 to TP7	CONN., HDR, SOCKET, RCPT, FEMALE, 1 x 2, 2.54mm, VERT, ST, SMD	MILL-MAX, 310-43-102-41-105000
10	0	TP8, TP9, TP10	CONN., HDR,MALE, 1 x 2, 2.54mm, VERT, ST, SMD	SAMTEC, TSM-102-01-L-SV
11	1	XJP1	CONN., SHUNT, FEMALE, 2-POS, 2mm	WURTH ELEKTRONIK, 60800213421

Schematic

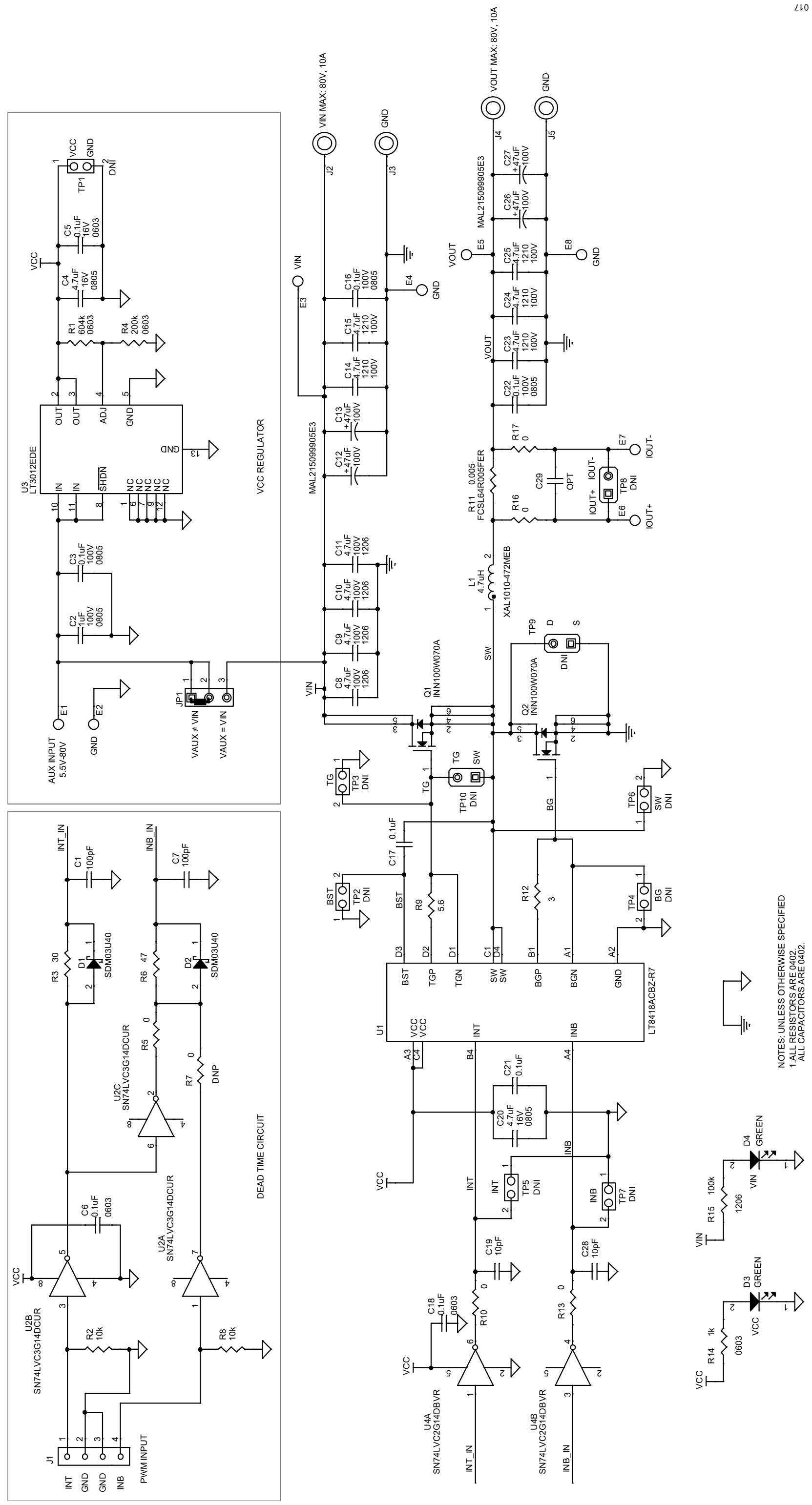

Figure 17. EVAL-LT8418-AZ Schematic

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGE NUMBER
Rev 0	04/2024	Initial Release	—

Notes