

Evaluating the ADGS6414D 0.56 Ω On Resistance High Density Octal SPST Switch**FEATURES**

- ▶ SPI with error detection
 - ▶ Includes CRC, invalid read and write addresses, and SCLK count error detection
- ▶ Analog supply voltages
 - ▶ Dual supply: $\pm 4.5\text{V}$ to $\pm 22\text{V}$
 - ▶ Single supply: 5V to 40V
- ▶ PC control in conjunction with the evaluation software
- ▶ EVAL-SDP-K1 (SDP-K1) system demonstration platform

EVALUATION BOARD KIT CONTENTS

- ▶ EVAL-ADGS6414DARDZ evaluation board

DOCUMENTS NEEDED

- ▶ [ADGS6414D](#) data sheet

EQUIPMENT NEEDED

- ▶ [EVAL-SDP-CK1Z \(SDP-K1\)](#) controller board
- ▶ DC voltage source
 - ▶ $\pm 20\text{V}$ (dual supply)
 - ▶ 36V (single supply)
- ▶ Optional 3.3V digital logic supply
- ▶ Analog signal source
- ▶ Method to measure voltage, such as a digital multimeter (DMM)

SOFTWARE NEEDED

- ▶ [ACE](#) software with EVAL-ADGS6414DARDZ plugin

GENERAL DESCRIPTION

The EVAL-ADGS6414DARDZ is the evaluation board for the ADGS6414D. The ADGS6414D is an octal SPST switch controlled by a serial peripheral interface (SPI). The SPI has robust error detection features, including cyclic redundancy check (CRC) error detection, invalid read and write address detection, and SCLK count error detection. The ADGS6414D also supports burst mode, which decreases the time between SPI commands.

[Figure 1](#) shows the EVAL-ADGS6414DARDZ in a typical evaluation setup. The EVAL-ADGS6414DARDZ is controlled by the system demonstration platform (SDP) EVAL-SDP-CK1Z (SDP-K1) that connects to a PC via a USB port. The ADGS6414D is in the center of the evaluation board, and wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals power the device, and a fourth terminal provides users with a defined digital logic-supply voltage, if required. Alternatively, the digital logic-supply voltage can be supplied from the SDP-K1. The EVAL-SDP-CK1Z (SDP-K1) controller board is available to order on the Analog Devices, Inc., website.

For full details on the ADGS6414D, refer to the ADGS6414D data sheet, which should be consulted in conjunction with this user guide when using the EVAL-ADGS6414DARDZ.

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REVISION HISTORY

12/2024—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

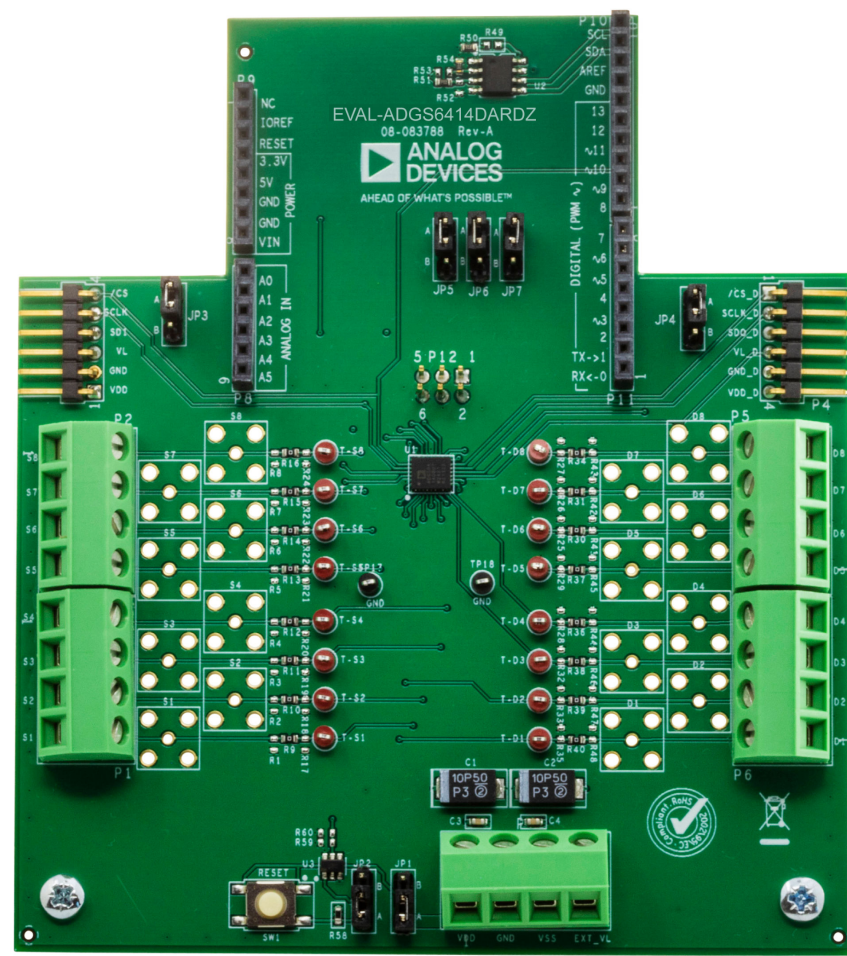


Figure 1. EVAL-ADGS6414DARDZ Evaluation Board Photograph

EVALUATION BOARD HARDWARE

POWER SUPPLIES

The P7 connector provides access to the supply pins of the ADGS6414D. V_{DD} , GND, and V_{SS} on P7 link to the appropriate pins on the ADGS6414D. For dual-supply voltages, the EVAL-ADGS6414DARDZ can be powered from $\pm 18V$ to $\pm 22V$. For single-supply voltages, the GND and V_{SS} terminals must be connected together and can power the EVAL-ADGS6414DARDZ with 18V to 39.6V. Additionally, 3.3V is supplied to the \overline{RESET}/V_L pins of the ADGS6414D by the SDP-K1 controller board when the JP1 link is in Position B. When controlling the ADGS6414D by a method other than the SDP-K1 controller board, supply between 2.7V and 5.5V to the \overline{RESET}/V_L pins of the ADGS6414D via the EXT_VL screw terminal input on P7. Ensure JP1 is in Position A.

INPUT SIGNALS

The P1, P2, P5, and P6 screw connectors connect to both the source and drain pins of the ADGS6414D. Additional Subminiature Version B (SMB) connector pads are available if extra connections are required.

Each trace on the source and drain sides of the EVAL-ADGS6414DARDZ includes two sets of 0603 pads that can place a load on the signal path to the ground. A 0 Ω resistor is placed in the signal path and can be replaced with a user-defined value. The resistor and the 0603 pads create a simple RC filter.

LINK OPTIONS

Ensure that the link options provided on the EVAL-ADGS6414DARDZ are set for the required operating conditions before using the evaluation board.

Table 1 details the positions of the links to control the evaluation board via the SDP-K1 controller board using a PC and external power supplies. The functions of these link options are detailed in Table 3.

Table 2 details the positions of the links to control the evaluation board via an Arduino controller using a PC and external power supplies. JP5, JP6, and JP7 should remain in Position A when the EVAL-ADGS6414DARDZ is being controlled using the SDP-K1 and when being controlled by Arduinos that do not require the alternative SPI connections.

When using the SDP-K1 controller board in conjunction with the EVAL-ADGS6414DARDZ, place JP1 in Position B to avoid damage to the SDP-K1.

Table 1. Link Options for SDP-K1 Control (Default)

Link Number	Option
JP1	B
JP2	B

Table 2. Link Options for Arduino Control (Default)

Link Number	Option
JP5	A
JP6	A
JP7	A

ROUTE THROUGH PINS FOR DAISY CHAINS

The P3 and P4 headers allow access to the route through pins of the ADGS6414D. Use the P3 and P4 headers to daisy-chain multiple EVAL-ADGS6414DARDZ devices together. To daisy-chain the EVAL-ADGS6414DARDZ devices, connect \overline{CS}_D , SCLK_D, and SDO_D on P4 of one EVAL-ADGS6414DARDZ to \overline{CS} , SCLK, and SDI on P3 of the next EVAL-ADGS6414DARDZ. V_L , GND, and V_{DD} can also be shared between these evaluation boards via the P3 and P4 headers. However, because V_{SS} is only accessible from P7, connect V_{SS} to each daisy-chained EVAL-ADGS6414DARDZ.

It is also possible to daisy-chain multiple EVAL-ADGS6414DARDZ devices together through stacking EVAL-ADGS6414DARDZ devices on top of each other using the P8, P9, P10, and P11 connectors. Using this method allows for great space saving on the work bench. To daisy-chain the EVAL-ADGS6414DARDZ devices, place JP3 of the first device to Position A to allow for the SDI signal to be received through the SPI source and JP4 to Position B to allow the SDO to be daisy-chained the next device through P4. For any subsequent EVAL-ADGS6414DARDZ devices in the daisy-chain, place JP3 to Position B to read from the previous device through P3, and JP4 will remain at Position B until the last device in the chain, which will be in Position A, allowing the signal to be read from P10. The \overline{CS} , SCLK, V_L , and GND pins will all be shared through the P9 and P10 connectors. V_{DD} can be shared through P3, P4, or P7, whereas V_{SS} is only accessible from P7.

Table 3. Link Functions

Link Number	Function
JP1	The JP1 link selects the source of the V_L voltage supplied to the ADGS6414D. Position A selects EXT_VL from P7. Position B selects 3.3V from the SDP-K1 controller board.
JP2	The JP2 link selects how a hardware reset is performed. Position A indicates the SW1 push-button performs a hardware reset. Position B indicates the SDP-K1 controller board performs a hardware reset.
JP3	The JP3 link selects the source of the SDI. Position A provides the SDI from the SDP-K1 controller board. Position B provides the SDI from the SDI_D spin used when connected to another board in the daisy-chain.
JP4	The JP4 link selects the source of the SDO. Position A sends the SDO to the SDP-K1 controller board. Position B sends the SDO to the SDO_D spin used when connected to another board in the daisy-chain.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-ADGS6414DARDZ uses the Analog Devices [Analysis, Control, Evaluation \(ACE\)](#) software. ACE is a desktop software application that allows users to evaluate and control multiple evaluation systems.

The ACE installer installs the necessary SDP drivers and .NET Framework 4 by default. Install ACE before connecting to the [SDP-K1](#) controller board. The full instructions on how to install and use the ACE software can be found on the Analog Devices website at www.analog.com/ace.

After ACE is installed, the EVAL-ADGS6414DARDZ plugin appears when opening the application.

INITIAL SET UP

To set up the EVAL-ADGS6414DARDZ, complete the following steps:

1. Connect the EVAL-ADGS6414DARDZ to the SDP-K1 controller board via the Arduino-compatible connector.
2. Connect the SDP-K1 controller board to the computer using the USB cable provided with the SDP-K1.
3. Power the EVAL-ADGS6414DARDZ as described in the [Power Supplies](#) section.
4. Run the ACE application. The EVAL-ADGS6414DARDZ plugin appears in the **Attached Hardware** section of the **Start** tab.
5. Double click the **ADGS6414D Board** evaluation board plugin to open the ADGS6414D chip view, as shown in [Figure 2](#).

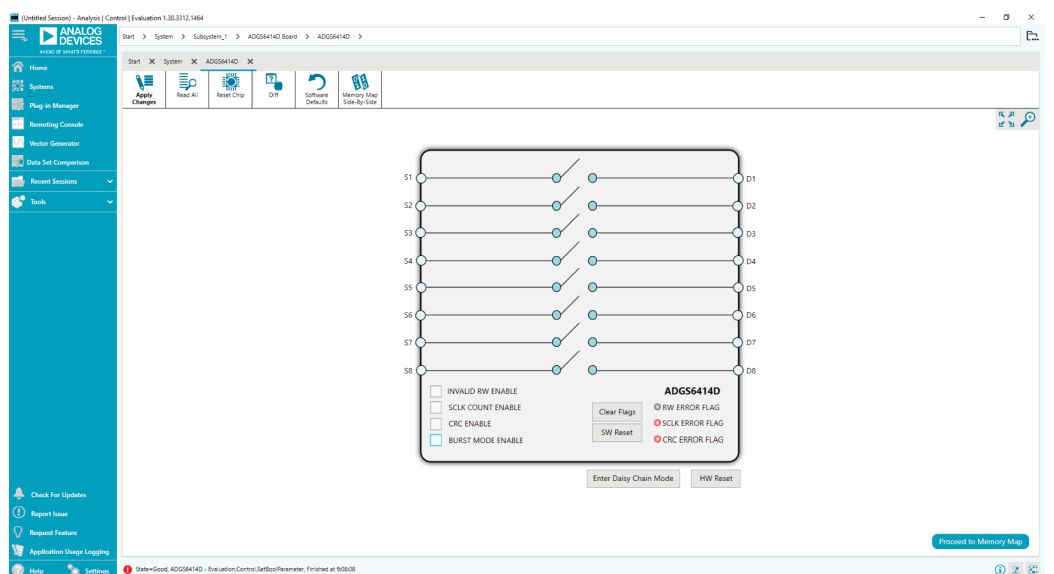


Figure 2. Chip View for the ADGS6414D

BLOCK DIAGRAM AND DESCRIPTION

The ADGS6414D chip view is similar to the functional block diagram shown in the ADGS6414D data sheet. Therefore, it is simple to correlate the functions on the EVAL-ADGS6414DARDZ with the descriptions in the data sheet. Refer to the ADGS6414D data sheet for a full description of each block, register, and setting.

Some of the blocks and their functions are described in this section as they pertain to the EVAL-ADGS6414DARDZ. Figure 3 shows the full screen block diagram (with labels), and Table 4 describes the functionality of each labeled block.

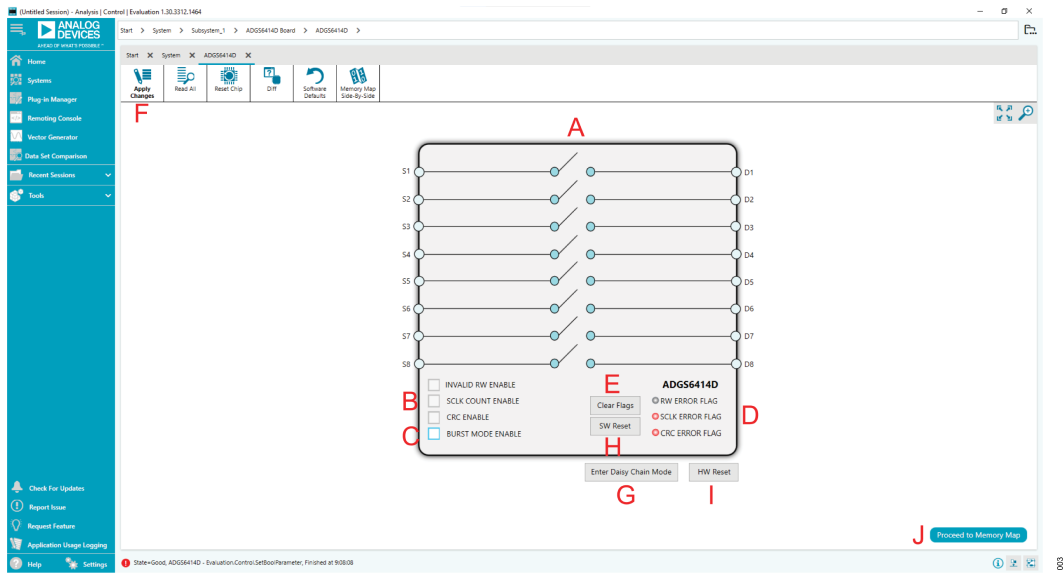


Figure 3. Chip View for the ADGS6414D with Labeled Block Diagram

Table 4. Block Diagram Functions

Label	Function
A	The eight switches configure SW1 to SW8 as open or closed. Click the switch to configure it.
B	INVALID RW ENABLE , SCLK COUNT ENABLE , and CRC ENABLE . Select or clear these check boxes to enable or disable the error detection features on the SPI.
C	BURST MODE ENABLE . Select or clear this check box to enable or disable burst mode.
D	RW ERROR FLAG , SCLK ERROR FLAG , and CRC ERROR FLAG . These indicators illuminate red if flags assert in the error flags register.
E	Clear Flags . Click this button to clear the error flags register.
F	Apply Changes . Click this button to apply all modified values to the devices.
G	Enter Daisy Chain Mode . Click this button to put all evaluation boards that are connected in a daisy-chain configuration into daisy-chain mode.
H	SW Reset . Click this button to perform a software reset on the ADGS6414D.
I	HW Reset . Click this button to perform a hardware reset on the ADGS6414D. JP2 must be set to Position B.
J	Proceed to Memory Map . Click this button to access the ADGS6414D Memory Map view.

BLOCK DIAGRAM AND DESCRIPTION

DAISY-CHAIN MODE

It is possible to daisy-chain multiple ADGS6414D devices together. Daisy-chain mode enables the configuration of multiple devices with a minimal amount of digital lines. The route of digital signals and supplies through the ADGS6414D allows an increase in channel density when using the device in daisy-chain mode. Integrated passive components eliminate the need for external passive components.

Click **Enter Daisy Chain Mode** to open the **Daisy Chain Mode** view, as shown in [Figure 4](#). Select the number of boards that are

connected in the daisy chain from the **Number of Devices in Daisy Chain** dropdown box. Select the checkboxes of the switches that are to be turned on. Click **Apply Changes** to write these values to the devices in the daisy chain. To exit daisy-chain mode, perform a hardware reset. To perform a hardware reset, click the **HW Reset** button in the **Daisy Chain Mode** view (JP2 must be set to Position B) or press the physical hardware reset button on the EVAL-ADGS6414DARDZ.

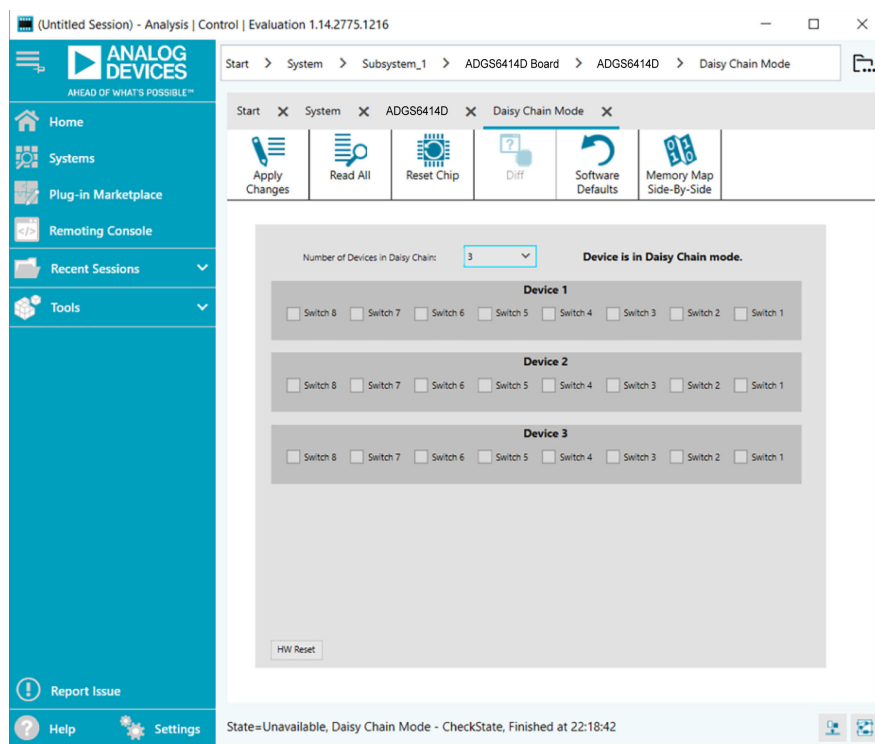


Figure 4. Daisy Chain Mode View

BLOCK DIAGRAM AND DESCRIPTION

MEMORY MAP

All registers are fully accessible from the **ADGS6414D Memory Map** view. To access the **ADGS6414D Memory Map** view, click **Proceed to Memory Map**. The **ADGS6414D Memory Map** view allows registers to be edited at a bit level (see [Figure 5](#) and [Figure 6](#)). The shaded bits are read-only bits and cannot be accessed in [ACE](#). All other bits are toggled. The bold bits or

registers are modified values that have not been transferred to the evaluation board. Click **Apply Changes** to transfer the data to the EVAL-ADGS6414DARDZ.

All changes made in the **ADGS6414D Memory Map** view correspond to the block diagram. For example, if the internal register bit is enabled, the bit displays as enabled on the block diagram.

Registers				
+ / -	Address (Hex)	Name	Data (Hex)	Data (Binary)
+	0001	* SW_DATA	00	0 0 0 0 0 0 0 0 0
+	0002	ERR_CONFIG	06	0 0 0 0 0 0 1 1 0
+	0003	* ERR_FLAGS	00	0 0 0 0 0 0 0 0 0
+	0005	BURST_EN	00	0 0 0 0 0 0 0 0 0

Figure 5. ADGS6414D Memory Map View

Registers				
+ / -	Address (Hex)	Name	Data (Hex)	Data (Binary)
+	0001	* SW_DATA	01	0 0 0 0 0 0 0 1
+	0002	ERR_CONFIG	06	0 0 0 0 0 0 1 1 0
+	0003	* ERR_FLAGS	00	0 0 0 0 0 0 0 0 0
+	0005	BURST_EN	00	0 0 0 0 0 0 0 0 0

Figure 6. ADGS6414D Memory Map View with Unapplied Changes in the SW_DATA Register

Figure 7. EVAL-ADGS6414DARDZ Schematic 1

EVALUATION BOARD SCHEMATICS AND ARTWORK

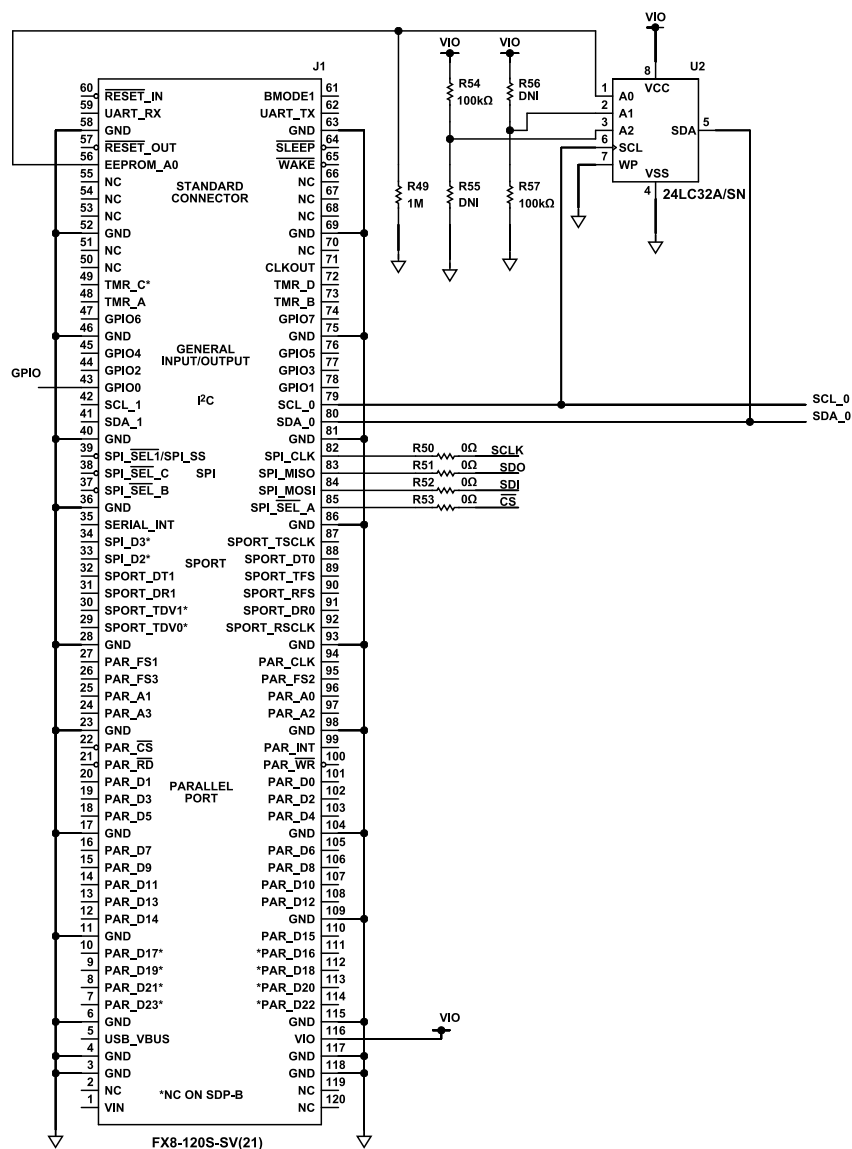


Figure 8. EVAL-ADGS6414DARDZ Schematic 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

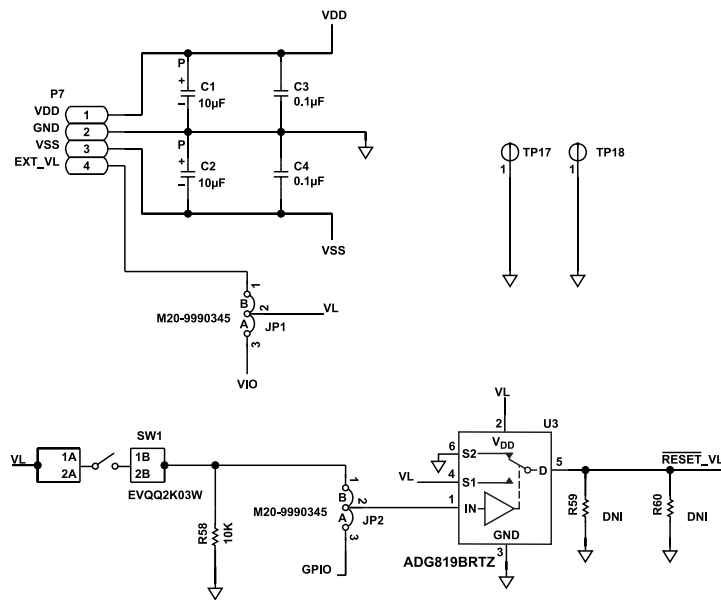


Figure 9. EVAL-ADGS6414DARDZ Schematic 3

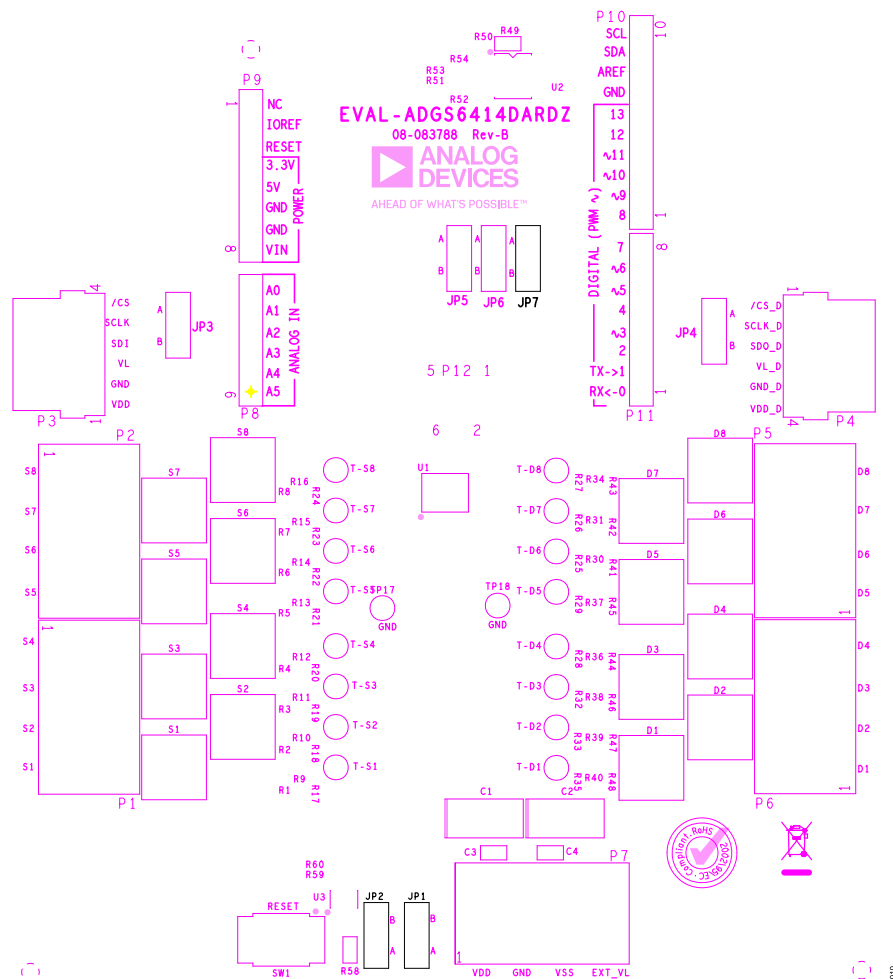


Figure 10. EVAL-ADGS6414DARDZ Silkscreen

EVALUATION BOARD SCHEMATICS AND ARTWORK

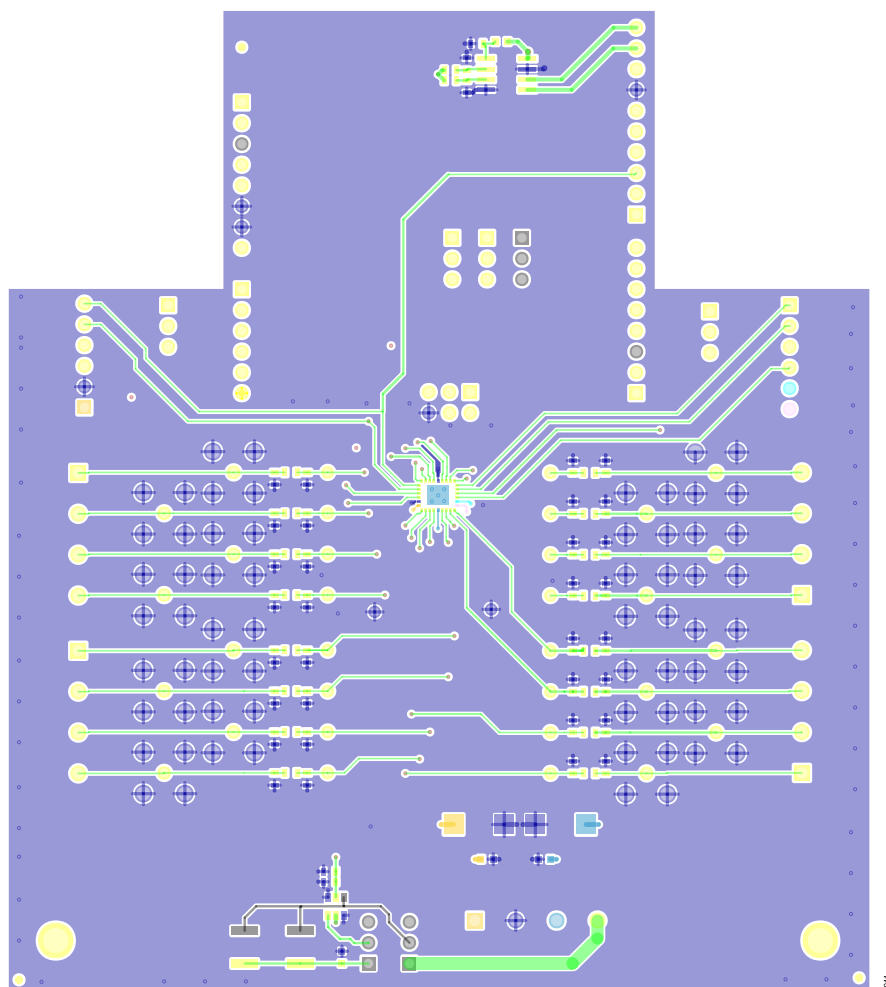


Figure 11. EVAL-ADGS6414DARDZ Top Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

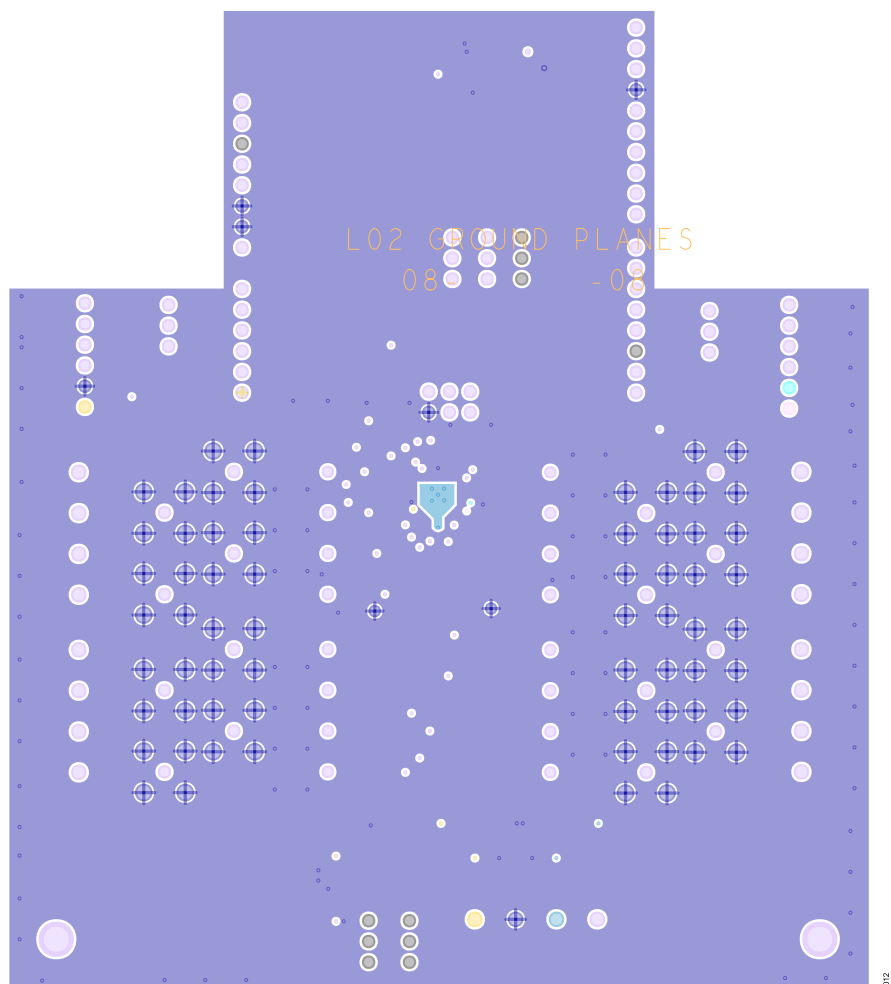


Figure 12. EVAL-ADGS6414DARDZ Layer 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

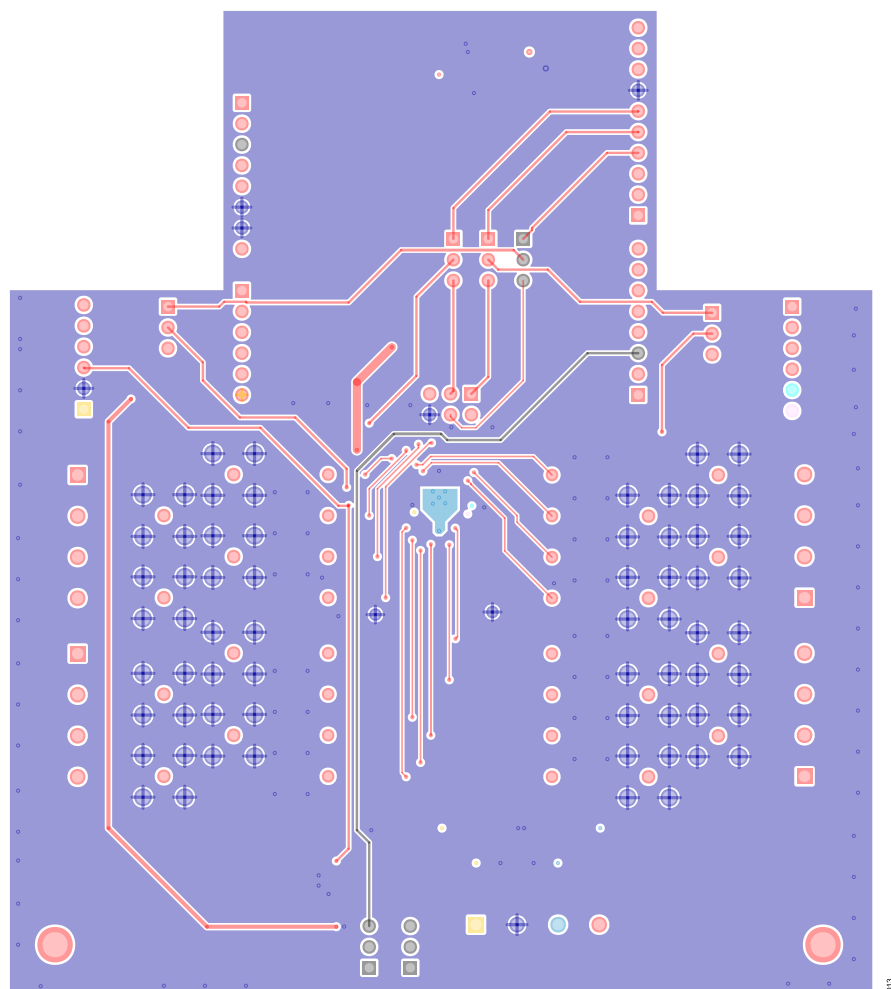


Figure 13. EVAL-ADGS6414DARDZ Layer 3

EVALUATION BOARD SCHEMATICS AND ARTWORK

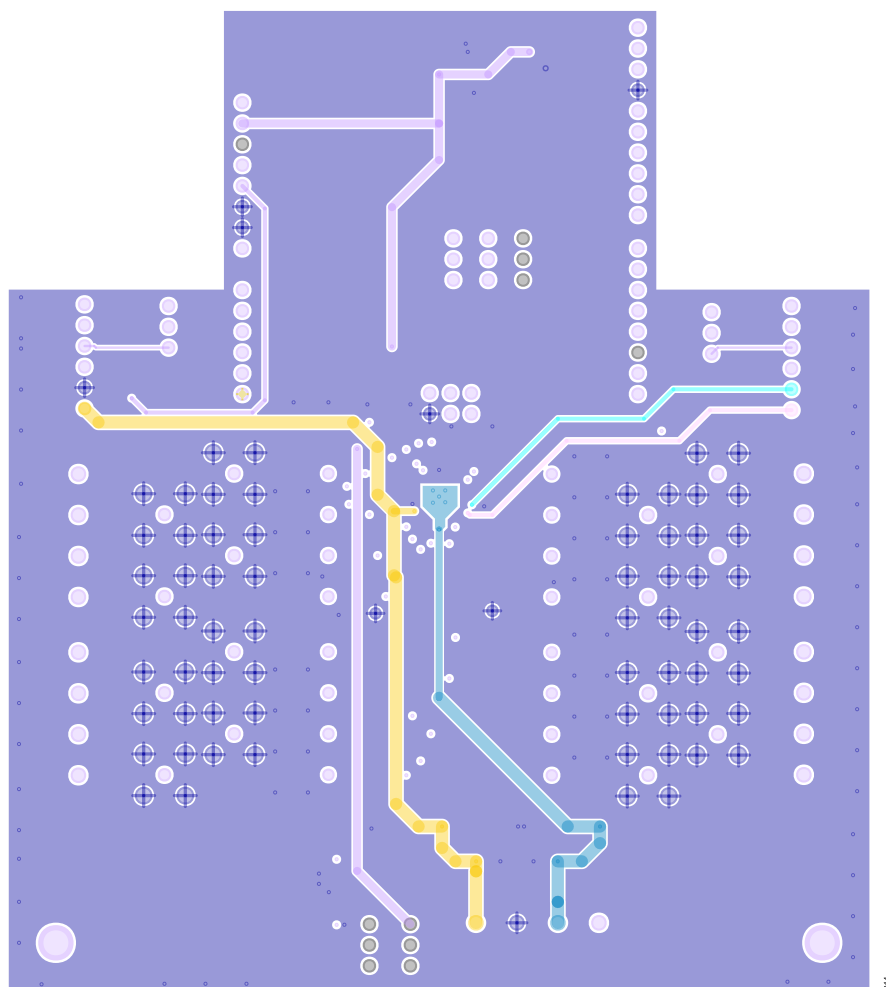


Figure 14. EVAL-ADGS6414DARDZ Bottom Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 5. Bill of Materials for EVAL-ADGS6414DARDZ

Reference Designator	Description
C1, C2	50V tantalum capacitor, 10µF, D size
C3, C4	50V, X7R, multilayer ceramic capacitor, 0.1µF, 0603
D1 to D8	Not placed
S1 to S8	Not placed
T-D1 to T-D8, T-S1 to T-S8	Red test point
TP17, TP18	Black test point
P1, P2, P5 to P7	4-pin terminal block, 5mm pitch
P3, P4	Through hole, right-angle header, 2.54mm pitch
P8	Through hole PCB socket, 6-contact, 2.54mm pitch
P9, P11	Through hole PCB socket, 8-contact, 2.54mm pitch
P10	Through hole PCB socket, 10-contact, 2.54mm pitch
P12	Through hole square PCB socket, 6-contact, 2.54mm pitch
JP1 to JP7	3-pin single inline (SIL) header and shorting link
R1 to R8, R17 to R29, R32, R33, R35, R41 to R48, R55, R56, R59, R60	Not placed
R49, R52, R53	Not placed
R9 to R16, R30, R31, R34, R36 to R40	Resistor, 0Ω, 0603, 1%
R58	Resistor, 10kΩ, 0.063 W, 1%, 0603
R50, R51, R54	Resistor, 100kΩ, 0.063 W, 1%, 0603
SW1	Surface-mount device (SMD) push-button switch
U1	ADGS6414D, SPI controlled, octal SPST switch
U2	32kΩ, 1 ² C serial electronically erasable programmable read only memory (EEPROM)
U3	ADG819, 1.8V to 5.5V, 2:1 multiplexer and SPDT switch

1²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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