Evaluating the AD4080 20-Bit, 40 MSPS, Differential SAR ADC

FEATURES

- Full featured evaluation board for the AD4080
- **Analysis | Control | Evaluation (ACE) Software** plug-in available for device configuration, data capture, and performance evaluation
- Flexible analog front end
- On-board power solution and precision reference
- On-board clock generation circuitry with sampling frequency control via the **ACE Software**
- FMC compatible

EVALUATION BOARD KIT CONTENTS

- EVAL-AD4080-FMCZ evaluation board
- Micro-SD memory card with SD adapter, containing system board boot software and Linux OS

EQUIPMENT NEEDED

- PC running Windows® 10 operating system or higher
- Digilent ZedBoard with 12 V wall adapter power supply
- Precision signal source
- SMA cables to connect a signal source to the EVAL-AD4080-FMCZ

GENERAL DESCRIPTION

The EVAL-AD4080-FMCZ is designed to demonstrate the AD4080 performance and provide access to a limited set of AD4080 features in the **ACE Software** environment. The EVAL-AD4080-FMCZ evaluation kit supports the following AD4080 features:

- Low voltage digital signaling (LVDS) data output interface
- Analog-to-digital converter (ADC) configuration via serial peripheral interface (SPI)
- Internal or external generation of 1.1 V regulated supply rails
- Sampling rate capability between 1.25 MSPS and 40 MSPS

The EVAL-AD4080-FMCZ evaluation board was designed for use with the Digilent ZedBoard via the field programmable gate array (FPGA) mezzanine card (FMC) connector. The ZedBoard uses a Xilinx Zynq7000 system on chip (SoC) that runs Analog Devices, Inc., Kuiper Linux and LIBIIO included on the SD card supplied in the evaluation board kit to facilitate communication with the EVAL-AD4080-FMCZ, enabling ADC configuration and data capture. The ZedBoard also provides the communication link to the host PC and the **ACE Software** plug-in.

EVALUATION BOARD PHOTOGRAPH

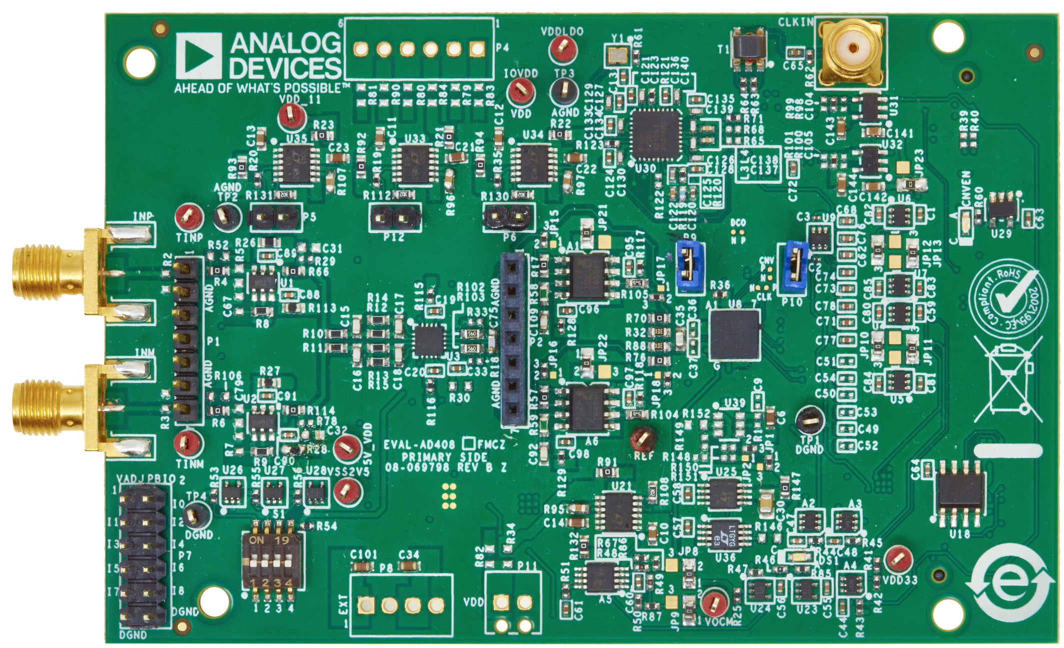

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Figure 1. EVAL-AD4080-FMCZ Photograph

TABLE OF CONTENTS

REVISION HISTORY

3/2024—Revision 0: Initial Version

EVALUATION BOARD HARDWARE GUIDE

HARDWARE OVERVIEW

A simplified block diagram of the EVAL-AD4080-FMCZ hardware is shown in Figure 2. This evaluation board showcases the performance and features of the AD4080 and highlights the recommended companion components.

The EVAL-AD4080-FMCZ enables simple evaluation of the AD4080. All circuitry necessary to operate the AD4080 is included on the EVAL-AD4080-FMCZ. See the Analog Input Circuit section, Voltage Reference section, Power Supplies section, Conversion and Data Clock Generation Circuit section, and Digital Interface section for detailed specifics on each circuit block shown in Figure 2. For those blocks that can be modified to achieve different configurations, see the Supported Configurations section for additional details on how to implement these changes.

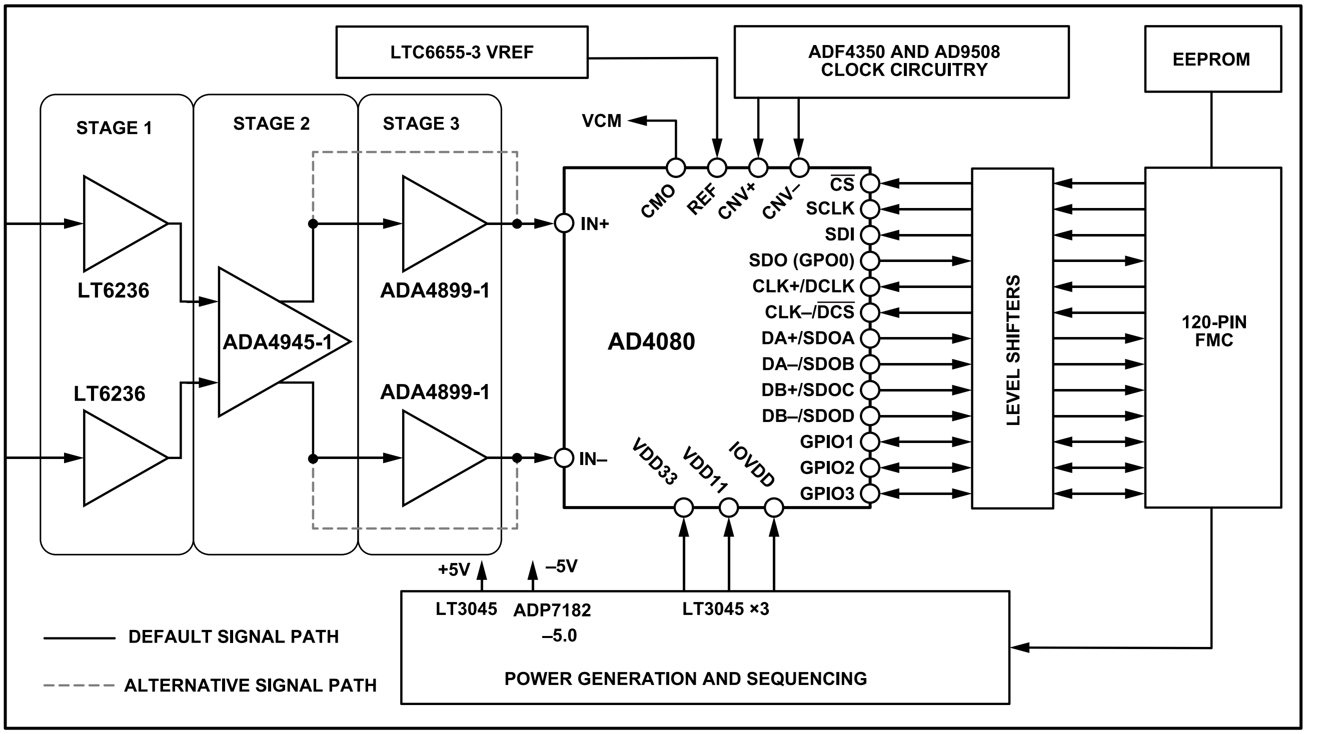

Figure 2. Simplified Block Diagram of the EVAL-AD4080-FMCZ

EVALUATION BOARD HARDWARE GUIDE

ANALOG INPUT CIRCUIT

The EVAL-AD4080-FMCZ includes a three stage, precision signal conditioning circuit. The design was partitioned in this fashion to allow the greatest flexibility in optimizing signal chain performance for the targeted signal bandwidth for both evaluation and prototyping.

With the default configuration of the evaluation hardware, a differential 6 V p-p input signal with the common mode set to 1.5 V results in a full-scale measurement from the ADC. The typical supported input frequency range is DC to 4 MHz.

Recommendations regarding signal chain configuration for particular signal bandwidths of interest can be found in the Analog Front End (AFE) Considerations section.

INPUT STAGE (STAGE 1)

The input stage consists of a pair of LT6236 op amps (U1 and U2). The LT6236 op amps were selected for its exceptional wideband (90 MHz), low noise, favorable distortion performance and low power consumption. The stage is configured for differential input, differential output, noninverting, unity-gain operation, ensuring that a preceding signal source or sensor is presented with a high impedance. With supply rail values of +5 V and −2.5 V, the valid range for the LT6236 inputs (INP and INM) is approximately −0.8 V to +4 V, which means that a common-mode voltage of 1.5 V (available at V_{OCM}) for the inputs is close to ideal to allow maximum voltage excursion and minimize distortion.

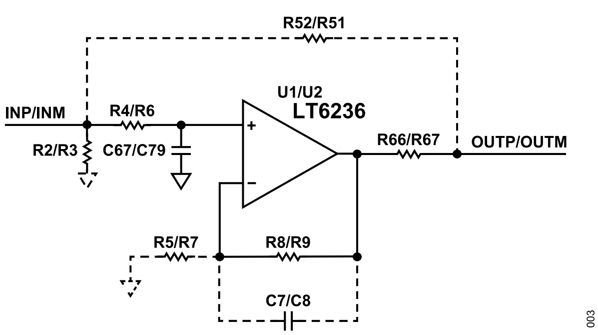

Figure 3. Stage 1 Simplified Schematic

The following can be configured in this stage:

- Stage bandwidth
  - No explicit bandwidth limiting (default)
  - Band limiting through RC input filter and/or capacitors across amplifier feedback
- Stage gain
  - Unity gain (default)
  - Noninverting gain setting
- Stage bypass
  - No bypass (default)
  - Bypass Stage 1
  - Bypass Stage 1 along with Stage 2 to use an amplifier mezzanine card (AMC) instead
- Input signal type
  - Differential (default)
  - Single-ended

FULLY DIFFERENTIAL AMPLIFIER STAGE (STAGE 2)

Stage 2 is based around an ADA4945-1 (U3) fully differential amplifier configured for unity gain.

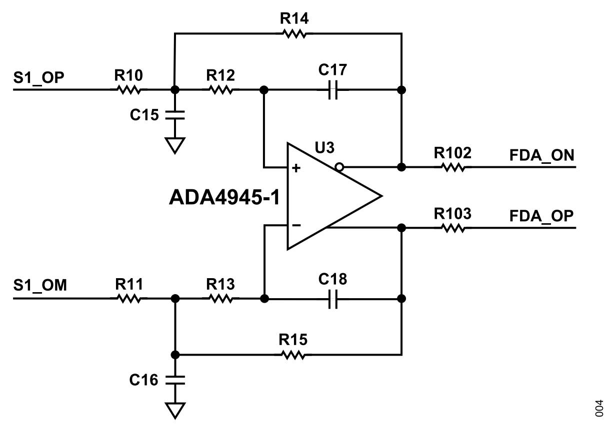

Figure 4. Stage 2 Simplified Schematic

The clamp pins of the ADA4945-1 ($-V_{CLAMP}$ and $+V_{CLAMP}$) are connected to the VREF and GND nodes, which results in a limitation of the range at the output of the fully differential amplifier (FDA) of ~500 mV beyond those nodes to protect the ADC from hard overdrive.

The common-mode input of the ADA4945-1 is floating by default, meaning that the output common-mode value is internally biased at a voltage equal to the midpoint between the output voltage clamps, that is, 1.5 V.

With the default configuration, this stage presents a 3 dB cutoff frequency of 5.5 MHz at the output (measured at FDA_ON and FDA_OP nodes).

The following can be configured in this stage:

- Stage bypass
  - No bypass (default)
  - Bypass Stage 2
- ADA4945-1 power mode
  - Full power mode (default) achieves the maximum device bandwidth and best distortion performance.
  - Low-power mode minimizes power at the cost of distortion performance and reduces the amplifier bandwidth.
- Alternative amplifier installation
  - ADA4940-1

EVALUATION BOARD HARDWARE GUIDE

- ADA4932-1
- Stage bypass
  - No bypass (default)
  - Bypass along with Stage 1 for using the AMC

ADDITIONAL ADC DRIVER STAGE (STAGE 3)

Stage 3 is an optional stage consisting of two ADA4899-1 (A1 and A6) high-speed, low distortion op amps. This stage allows users to achieve the lowest distortion possible; however, at the expense of higher power consumption. Stage 3 is enabled by default, but this stage can be disabled to save power.

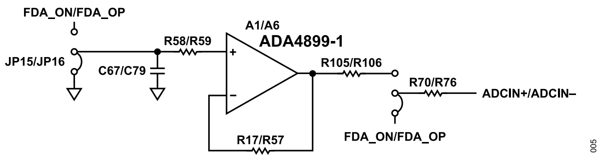

Figure 5. Stage 3 Simplified Schematic

The following can be configured in this stage:

- Stage bypass:
  - Bypass stage.
  - Enable stage (default).

VOLTAGE REFERENCE

The AD4080 requires an external 3 V voltage reference. To achieve the specified performance, a suitable precision, low noise voltage reference must be used. The AD4080 does include an internal reference buffer and capacitor, which makes reference selection easier and eliminates the need for an external buffer.

The following can be configured in this circuit:

- Reference selection
  - The LTC6655-3 is the default. The evaluation hardware includes LTC6655-3 (U25) as the primary recommended option, providing exceptional noise performance (0.1 Hz to 10 Hz noise specification of 0.25 ppm p-p), combined with an initial accuracy of 0.025%, and a low temperature drift of 2 ppm/°C.
  - The LT6657-3 (U36) is also mounted and provided as a second option. See Table 1 for a comparison of recommended references.

Table 1. 3 V Reference Comparison of the LT6657 and LTC6655

Parameter	LT6657	LTC6655
Accuracy	0.10%	0.025%
Temperature Coefficient (ppm/°C)	1.5	2
0.1 Hz to 10 Hz Noise (ppm p-p)	0.5	0.25
Maximum Load (mA)	±10	±5
Load Regulation (ppm/mA)	0.7	3
Maximum Supply	40 V	13.2 V
Shutdown	Yes	Yes

Table 1. 3 V Reference Comparison of the LT6657 and LTC6655 (Continued)

Parameter	LT6657	LTC6655
Reverse Supply Protected	Yes	No
Reverse Output Protected	Yes	No
Current Limit	Yes	Yes
Thermal Protection	Yes	No
Shunt Mode	Yes	No
Supply Current, I_S (mA)	1.2	5
T_A	−40°C to +125°C	−40°C to +125°C
100% Tested Temperatures	5	3

COMMON-MODE CIRCUIT

The AD4080 includes a common-mode voltage generation feature. The common-mode voltage is equal to reference voltage (V_{REF})/2, and this voltage is provided through the CMO pin of the AD4080. This feature is generally useful for biasing front-end stages. In this instance, it is optional to use this feature because the ADA4945-1 can use an internal biasing circuit to set the output common mode to the midpoint of the output clamping pins ($-V_{CLAMP}$ and $+V_{CLAMP}$).

The following can be configured in this circuit:

- FDA common-mode setting
  - Internal (default): The ADA4945-1 sets the output common-mode level to the output clamps midpoint.
  - External: Use the CMO voltage provided by the ADC to set the FDA output common-mode level.
- Common-mode signal buffering
  - No buffering (default).
  - Buffering through the ADA4807-2 (A5) amplifier, which is only necessary if additional load is placed on the AD4080 CMO output. Note that this output has an output impedance of 700 Ω; consult the AD4080 data sheet for additional details.

EVALUATION BOARD HARDWARE GUIDE

POWER SUPPLIES

The EVAL-AD4080-FMCZ is designed to operate from a 12 V supply provided from the host controller board via the FMC connector. The 12 V power supply is regulated down using a combination of switching regulators and linear dropout (LDOs) regulators to generate the necessary power rails for the on-board circuitry.

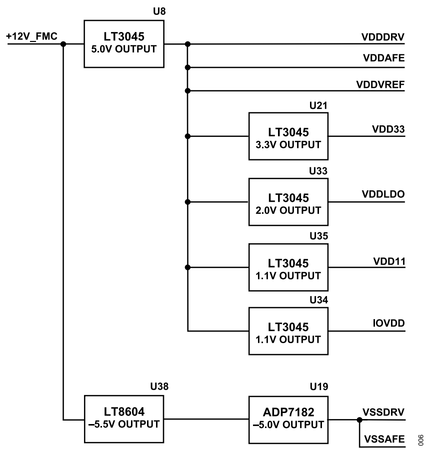

Figure 6. Power Circuitry Simplified Schematic

AD4080 POWER SUPPLY

The AD4080 requires three major power supplies:

- VDD33: 3.3 V analog supply rail.
- VDD11: 1.1 V ADC core supply.
- IOVDD: 1.1 V digital interface supply.

The AD4080 includes integrated power supply decoupling;therefore, no external power supply decoupling was included on-board for the AD4080 power supply rails.

The following can be configured in this circuit:

- 1.1 V rails (VDD11 and IOVDD) source
  - On-board generated rails (default): The rails are taken in from the LT3045 regulators (U34 and U35), as shown in Figure 6.
  - Internal AD4080 LDO regulator: An LDO internal to the AD4080 can be enabled and used to power both 1.1 V rails. Refer to the AD4080 data sheet for more details pertaining to the power supply rails and requirements.
  - Off-board external supply.
- 3.3 V rail source
  - On-board generated rail (default): The rail is supplied by an LT3045 LDO regulator (U21), as shown in Figure 6.
  - Off-board external supply.

AMPLIFIER POWER SUPPLY

The signal conditioning circuitry of the EVAL-AD4080-FMCZ was designed to operate from +5 V and −5V rails. The positive and negative rails of the U1 and U2 amplifiers are supplied from the +5 V VDDAFE rail and the −5 V VSSAFE rail.

The positive and negative rails of the fully differential U3 amplifier and the optional third stage A1 and A2 amplifiers are supplied from the +5 V VDDDRV rail and −5 V VSSDRV rail. The common-mode buffer A5 amplifier is configured for a unipolar power supply; the positive supply rail of A5 is provided from the +5 V VDDDRV rail, and the negative supply rail is connected to ground.

CONVERSION AND DATA CLOCK GENERATION CIRCUIT

The EVAL-AD4080-FMCZ contains the necessary circuits to generate low jitter data (CLK+ and CLK−) and conversion (CNV+ and CNV−) clocks across the full operating range of the AD4080. This low jitter circuitry allows processing with fidelity full-scale input signals up to 4 MHz.

The circuit consists of a 25 MHz complementary metal–oxide semiconductor (CMOS) reference oscillator (Y1), the ADF4350 wideband synthesizer, and the AD9508 clock fanout buffer as shown in Figure 7. The synthesizer takes in the 25 MHz signal from the oscillator and produces a higher frequency output with the frequency multiplication factor being programmable by the software. The synthesizer output is then fed to the clock buffer, which generates the clock (CLK+ and CLK−) and convert (CNV+ and CNV−) signals, from which, it can apply separate programmable frequency division factors. Therefore, the software sets the CLK and CNV signal frequencies by programming the ADF4350 and AD9508 through their serial interfaces. In practice, to change the sample rate, the user changes the **Sampling Frequency (MHz)** field in the **Board Level** view of the **ACE Software** as is detailed in Figure 10.

The 25 MHz oscillator and synthesizer can be bypassed, and an external data clock reference supplied instead (through the CLKIN SMA connector) to the AD9508 to allow synchronization with an existing system clock solution. See the Using an External Clock Source section for details regarding bypassing the oscillator and synthesizer circuits.

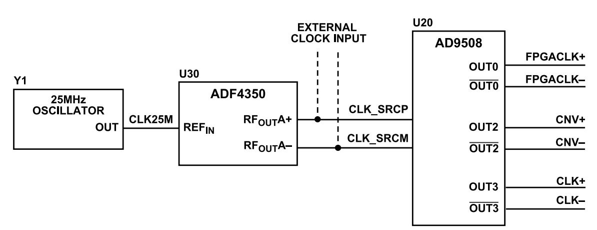

Figure 7. Simplified Diagram of the Clock Circuitry

Connectivity is established at the output of the AD9508 to optionally generate a third output signal, a synchronous FPGA reference

EVALUATION BOARD HARDWARE GUIDE

clock (FPGACLK+ and FPGACLK−). However, this function is not supported yet.

By default, the EVAL-AD4080-FMCZ conversion control is configured to operate in LVDS mode; therefore, the AD9508 drives the CNV+ and CNV− pins differentially. The hardware includes provisions to allow using a single-ended CMOS signal instead, see the Configuring for CMOS CNV Mode section for further details.

DIGITAL INTERFACE

The EVAL-AD4080-FMCZ utilizes the FMC connector (P3) from the ZedBoard to support ADC device configuration via the 4-wire SPI, conversion result access using the LVDS interface, and conversion control in LVDS mode. The ZedBoard acts as the conduit for communication between the **ACE Software** plug-in and the EVAL-AD4080-FMCZ hardware.

The AD4080 operates with a 1.1 V digital interface supply voltage. To translate between this 1.1 V level and the digital interface voltage level of the ZedBoard (VADJ), SN74AVC1T45DCKR bidirectional level translators (U4, U5, U6, U7, U11, U12, U13, U14, U15, U16, and U17) are used on the EVAL-AD4080-FMCZ hardware.

EVALUATION HARDWARE SETUP PROCEDURE

The following procedure must be followed to get the hardware ready for evaluation:

1. Insert the SD card from the EVAL-AD4080-FMCZ kit into the SD card slot (J12) of the ZedBoard.
2. Ensure that the ZedBoard boot configuration jumpers (JP7 to JP11) are set as shown in Figure 8.

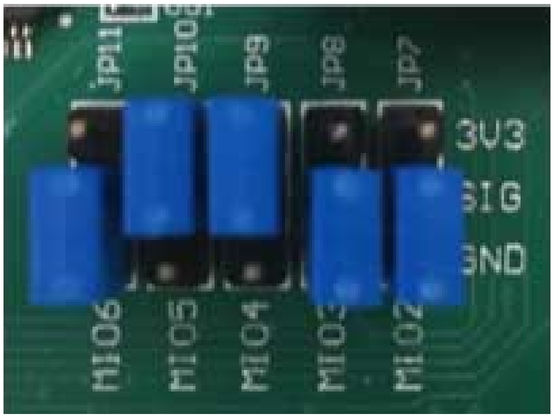

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Figure 8. ZedBoard JP7 to JP11 Settings for the SD Card Mode

3. Ensure that the VADJ SELECT jumper (J18) is in the **2V5** position.
4. Connect the FMC connector (P3) of the EVAL-AD4080-FMCZ to the FMC connector (J1) of the ZedBoard.
5. Connect the 12 V power supply included in the ZedBoard kit to the DC barrel jack (J20) of the ZedBoard, one USB cable between the PC and the USB on the go (OTG) connector (J13), and the other USB cable between the PC and the USB universal asynchronous receiver-transmitter (UART) connector (J14).
6. Slide the power switch (SW8) to the **ON** position to power up the ZedBoard and evaluation hardware.
   a. If using any external power supplies for the evaluation hardware, turn these supplies on with the ZedBoard.
7. The hardware is now ready to be used through the **ACE Software**.

EVALUATION SOFTWARE INSTALLATION

The **ACE Software** is a desktop software application that allows the evaluation and control of multiple evaluation systems from across the Analog Devices, Inc., product portfolio. The EVAL-AD4080-FMCZ hardware is controlled and configured through the **ACE Software**; however, an additional software plug-in that can be installed from within the ACE application is required.

Follow these steps to install the **ACE Software**:

1. Download the **ACE Software** package from the ACE Software web page on the Analog Devices website.
2. Click **Download ACE Installer** to download the installer file.
3. Run the installer and follow the instructions to complete the software installation process.

After ACE is successfully installed, the EVAL-AD4080-FMCZ plug-in can be installed as follows:

1. Run the **ACE Software** and click on the **Plug-in Manager** in the ACE sidebar, then select **Available Packages**.
2. From the list of plug-ins available, select the **Board.AD4080** (note that you can use the **Search** field to help filter the list of boards to find the relevant one), then click **Install selected**.

EVALUATING THE AD4080 WITH THE ACE SOFTWARE

After the hardware setup is complete as per the Evaluation Hardware Setup Procedure section, and the software is installed as specified in the Evaluation Software Installation section, the ACE software can be run for evaluation.

When ACE opens, the EVAL-AD4080-FMCZ is automatically detected and displayed in the **Attached Hardware** panel, as highlighted in yellow in Figure 9.

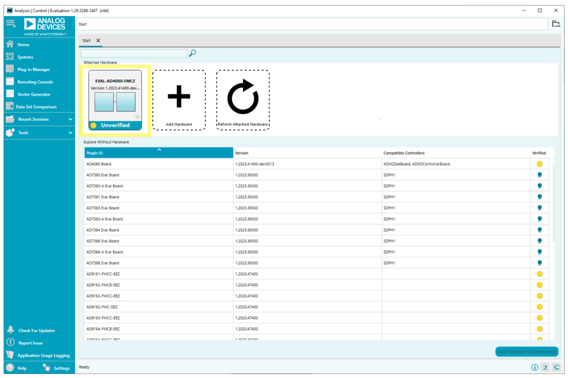

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Figure 9. Autodetection of the EVAL-AD4080-FMCZ in the ACE Start Tab

Double-click on the EVAL-AD4080-FMCZ icon and a new tab, **EVAL-AD4080-FMCZ**, opens that displays a block diagram of the EVAL-AD4080-FMCZ as shown in Figure 10.

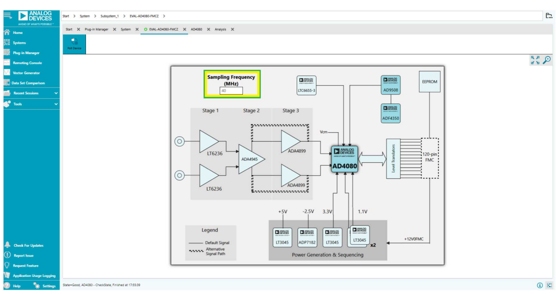

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Figure 10. EVAL-AD4080-FMCZ Tab Open in the ACE Software

This offers a **Board Level** view of EVAL-AD4080-FMCZ. The sampling frequency can be configured within this window because it can control the required configuration of the supporting clocking components, ADF4350 and AD9508, as well as controlling the synchronization of the EVAL-AD4080-FMCZ data with the ZedBoard. As a default, the **Sampling Frequency (MHz)** field is configured for 40 MHz. Any desired update to the sampling frequency, in the range of 1.25 MHz to 40 MHz, can be made to this field. When a new value is entered in this field, the supporting clock components are updated, and the ZedBoard interface is automatically resynchronized.

Double clicking on the AD4080 from the block diagram now opens an **AD4080** tab. This tab displays an **INITIAL CONFIGURATION** pane, a block diagram of the AD4080 chip, and two buttons in the lower-right corner (**Proceed to Memory Map** and **Proceed to Analysis**), which are highlighted in yellow in Figure 11.

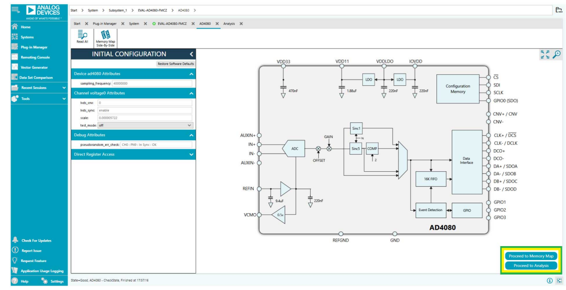

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Figure 11. AD4080 Tab in the ACE Software

The tabs that are accessed through these two buttons provide the means to evaluate the AD4080 chip. See the AD4080 Memory Map section and the ANALYSIS Tab section for additional details.

AD4080 MEMORY MAP

Click **Proceed to Memory Map** within the **AD4080** tab to open the **AD4080 Memory Map** tab, shown in Figure 12.

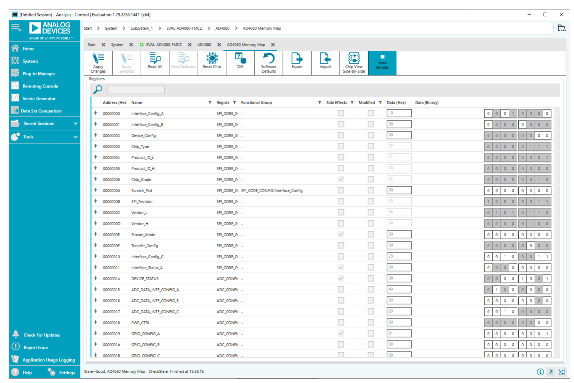

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Figure 12. AD4080 Memory Map Tab in the ACE Software

This tab displays the registers from the AD4080 and can be used to read and write (if applicable) their content. For normal operation of the evaluation kit, no modifications are required to the ADC registers.

ANALYSIS TAB

Click **Proceed to Analysis** within the **AD4080** tab to open the **ANALYSIS** tab. This tab is used for capturing data through the evaluation board and analyzing the obtained data.

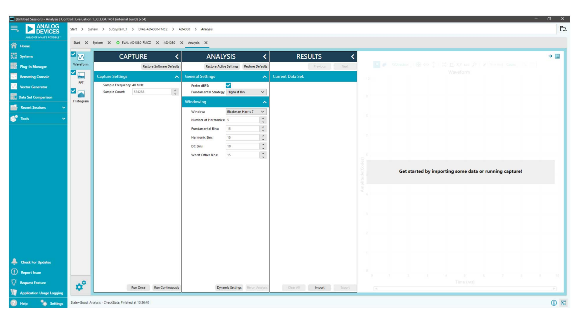

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Figure 13. Analysis Tab in the ACE Software

EVALUATING THE AD4080 WITH THE ACE SOFTWARE

The **ANALYSIS** tab contains three collapsible panels (**CAPTURE**, **ANALYSIS**, and **RESULTS**) and a data plot area to the right. Collapsing any of the three panels is done by clicking on the arrow located to the right of the panel name and is useful to leave more space for the data plot area when needed.

- The **CAPTURE** panel allows setting the number of samples to be captured per dataset, triggering the acquisition of a single dataset, and initiating or stopping the continuous acquisition of a dataset.
- The **ANALYSIS** panel displays options related to the frequency domain analysis.
- The **RESULTS** panel provides metrics for the current dataset being displayed in the plot area. Different metrics are provided depending on the kind of plot that was selected (see the Time Domain (Waveform) Plot section, Frequency Domain (FFT) Plot section, and Histogram Plot section for additional details). This panel also allows navigating between the datasets acquired during the session, and importing and exporting datasets in the internal format used by the **ACE Software** is also facilitated.

The user has the option to display the acquired datasets as a time domain waveform (default option), a frequency domain plot through a fast Fourier transform (FFT) or as a histogram, which is selected by clicking on any of the three corresponding buttons located to the left of the **CAPTURE** panel (see Figure 13).

TIME DOMAIN (WAVEFORM) PLOT

The active dataset can be displayed as a time domain waveform by clicking on the **Waveform** area highlighted in yellow in Figure 14, which is the default view. Note how the **CAPTURE** and **ANALYSIS** panels are collapsed for an improved display of the plot.

When the dataset is plotted as a time domain waveform, the **RESULTS** panel displays metrics relevant to time domain analysis: minimum, maximum, average, RMS, etc.

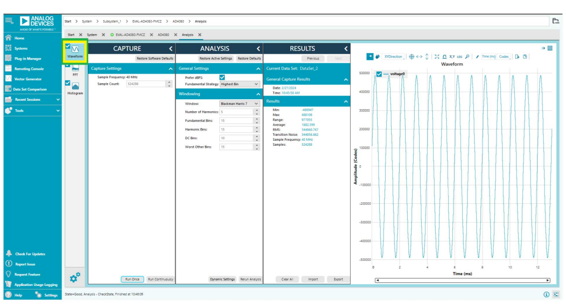

Figure 14. Dataset Plotted as Time Domain Waveform

FREQUENCY DOMAIN (FFT) PLOT

The active dataset can be displayed as a frequency domain waveform by clicking on the **FFT** area highlighted in yellow in Figure 15. The plot then displays the FFT of the active dataset. In this case, the **Log Scale** is selected for the **Frequency (MHz)** axis above the graph.

When the dataset is plotted as a frequency domain waveform, the **RESULTS** panel displays metrics relevant to frequency domain analysis: signal-to-noise ratio (SNR), total harmonic distortion (THD), etc.

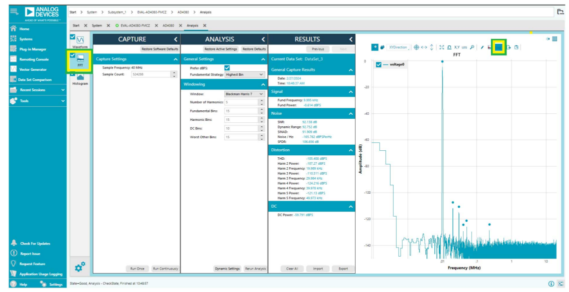

Figure 15. Dataset Plotted in the Frequency Domain

HISTOGRAM PLOT

The active dataset can be displayed as a histogram by clicking on the **Histogram** area highlighted in yellow in Figure 16. In this view, the vertical axis represents occurrences (bin hits) and the horizontal one can be set to display either code or volt amplitude bins.

When the dataset is plotted as a histogram, the **RESULTS** panel displays metrics relevant to histogram analysis, such as minimum code, maximum code, RMS, etc.

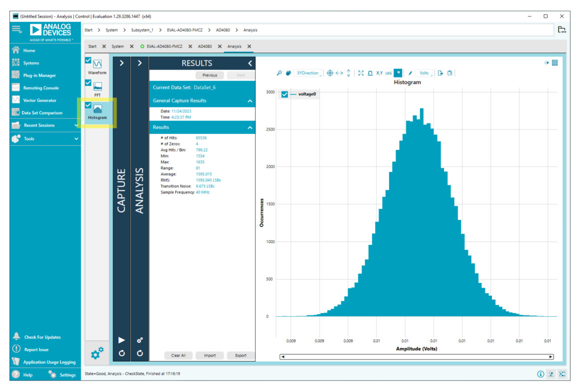

Figure 16. Dataset Plotted as a Histogram

SUPPORTED CONFIGURATIONS

The following sections describe the hardware and software configurations that the EVAL-AD4080-FMCZ supports.

ANALOG FRONT-END

Stage 1 Bypass

Stage 1 can be optionally bypassed to allow direct drive of the second stage (FDA) from the SMA connectors.

To bypass Stage 1, do the following:

- Remove R4, R6, R66 and R114 to disconnect the Stage 1 amplifiers from the stage input and output.
- Populate R52 and R106 with 0 Ω resistors to create the bypass path.
- Close Switch 1 and Switch 2 from the Switch Array S1 (see Table 3) to power down the now unused U1 and U2 amplifiers.

Stage 1 Gain

Stage 1 amplifiers are arranged for unity gain by default; however, this gain can be changed to a noninverting gain configuration.

To set the desired gain choose a feedback resistance (R_{FB}) to gain resistance (R_G) ratio according to the following equation:

$$\text{Gain} = 1 + \frac{R_{FB}}{R_G} \quad (1)$$

The necessary changes follow:

- Change the R8 and R9 feedback resistors for a value of R_{FB}.
- Populate R5 and R7 with a value of R_G.
- Populate 0 Ω R29 and R78 resistors.
- For the JP7 and JP14 solder links, link Pad 1 to Pad 2.

Stage 1 Filtering

A differential, first-order, RC filter can be implemented at the input of Stage 1 to bandwidth limit and reduce noise.

To obtain the desired 3 dB cutoff frequency sett values to the frequency capacitance (C_F) and frequency resistance (R_F) so that the following:

$$f_{3dB} = \frac{1}{2\pi R_F C_F} \quad (2)$$

The necessary changes follow:

- Change R4 and R6 to a R_F value.
- Populate C67 and C79 with a C_F value.

In addition to the RC filter (or instead of), the C7 and C8 capacitors across the feedback networks can be populated for further filtering.

Stage 1: Alternative Input Signal Sources

Differential Signal Source

In the default board configuration, the signal chain input (that is, Stage 1) is designed to be driven by a fully differential signal source with 0 V common mode applied at the SMA inputs (INP and INM). Because the default total gain of the signal chain is 1 by default, an amplitude of 6 V p-p in the differential signal results in a full-scale measurement at the ADC (−3 V to +3 V).

Note that the tight common-mode input requirement for the AD4080 (1.5 V ± 50 mV) does not apply to the signal at the input of the board because the ADA4945-1 driving the ADC sets its output common mode independently of the common mode at the input.

Single-Ended Input Source

A single-ended (ground referenced) AC signal can be fed to one of the EVAL-AD4080-FMCZ inputs (for example, INP), while the other input is grounded. An amplitude of 6 V p-p results in a full-scale measurement at the ADC (−3 V to +3 V).

When a single-ended signal source is applied at INP, the U2 amplifier that buffers the other input (INM) can be optionally disabled and bypassed. The necessary changes to do this follow:

- Remove R6 and R114 to disconnect the amplifier input and output from the circuit.
- Populate R106 with a 0 Ω resistor to enable the bypass path.
- Close Switch 2 (**ON** position) from Switch Array S1 (see Table 3) to power down the now unused U2 amplifier.

Stage 2 Alternative Amplifiers

By default, Stage 2 houses an ADA4945-1 low distortion, fully differential amplifier. Note that it is possible to use alternative amplifiers; however, these amplifiers are not included on the EVAL-AD4080-FMCZ.

The ADA4940-1 can be used to achieve the lowest power consumption in this stage. When using the ADA4940-1, the noise and distortion performance are expected to degrade relative to the ADA4945-1.

The ADA4932-1 can be used for applications where distortion performance is critical or applications where distortion performance is required up to 10 MHz. However, the improved distortion performance comes at the expense of higher power consumption.

Both the ADA4940-1 and ADA4932-1 are footprint compatible with ADA4945-1, although some pin connections must be changed. The necessary changes to use an alternative amplifier are as follows:

- Remove ADA4945-1 from the U3 footprint.
- Populate U3 with the ADA4940-1 or ADA4932-1.
- For the JP3, JP4, JP5, JP6 solder links, remove the default linkage (Pad 2 to Pad 3) and link Pad 1 to Pad 2 instead.

SUPPORTED CONFIGURATIONS

Stage 2 Bypass

By default, Stage 2 is enabled in the signal chain. To disable (bypass) Stage 2, the following hardware modifications are required:

- Remove R10 and R11 to disconnect the Stage 2 input from the Stage 1 output.
- Remove R102 and R03 to disconnect the Stage 2 output from the Stage 3 input.
- Remove C75.
- Populate R33 and R18 with 0 Ω resistors to bypass Stage 2.

Using an AMC (Stage 1 and Stage 2 Bypass)

The AMC is an Analog Devices, Inc., standard format for boards containing an amplifier stage. Some examples of amplifiers available on an AMC board follow:

- AMC-ADA4940-1ARZ
- AMC-ADA4896-2ARMZ
- AMC-ADA4807-2ARMZ
- AMC-ADA4805-2ARMZ
- AMC-ADA4841-2ARMZ

The EVAL-AD4080-FMCZ includes the necessary connectors so that an AMC can be fitted at the AFE, bypassing Stage 1 and Stage 2, which requires Stage 1 and Stage 2 to be disabled and disconnected.

The following must be done to use an AMC:

- Remove R4, R6, R102, R103 to disconnect Stage 1 from the signal chain input and Stage 2 from output.
- Remove the C75 capacitor.
- Populate the footprints of C67 and C79 with 0 Ω resistors to ground the inputs of Stage 1.
- Close Switch 1 and Switch 2 from Switch Array S1 (see Table 3) to power down the now unused U1 and U2 amplifiers.
- To provide the correct power supply to the AMC for the JP19 and JP20 solder links, do the following:
    - If using a fully differential amplifier AMC, link Pad 1 to Pad 2.
    - If using a single-ended amplifier AMC, link Pad 2 to Pad 3.

Stage 3 Bypass

By default, Stage 3 amplifiers are enabled in the signal chain. To disable Stage 3, the following hardware modifications are required:

- For the JP15, JP16, JP17, and JP18 solder links, remove the default linkage (Pad 2 to Pad 3) and link Pad 1 to Pad 2 instead.

COMMON-MODE CMO OUTPUT BUFFERING

By default, the common-mode voltage output from the ADC (CMO pin) is unbuffered and not connected to the V_{OCM} pin of the ADA4945-1. To make that connection, the following hardware modification is required:

- Populate R30 with a 0 Ω resistor.

To buffer the CMO output of the AD4080 using an ADA4807-2 amplifier, the following hardware modifications are required:

- For the JP8 and JP9 solder links, remove the default linkage (Pad 1 to Pad 2) and link Pad 2 to Pad 3 instead.
- Remove R86.

VOLTAGE REFERENCE

Secondary Voltage Reference, LT6657-3

The default reference is the LTC6655-3 (U25). To instead use the LT6657-3 (U36) secondary on-board reference, do the following:

- Remove the R147 resistor to disconnect the U25 output from the reference path.
- Populate R146 with a 0 Ω resistor to connect U36 to the reference path.

POWER SUPPLY RAILS

Internal AD4080 LDO Regulators for the 1.1 V Rails

By default, the two 1.1 V supply rails (VDD11 and IOVDD) required by the AD4080 are supplied by on-board LDO regulators (U34 and U35). The rails can be alternatively powered by two on-chip LDO regulators internal to the AD4080; however, this requires disconnecting the externally generated supplies from VDD11 and IOVDD and connecting a voltage source in the 1.5 V to 2.75 V range at the VDDLDO pin. The presence of this external voltage at the VDDLDO pin automatically triggers the start up of the internal regulators. A 2 V, LDO regulator (U33)-generated rail on the EVAL-AD4080-FMCZ is prepared for this function.

Therefore, to enable use of the on-chip LDO regulators, do the following:

- Remove the P9 and P10 jumpers to disconnect the AD4080 1.1 V supply inputs from the on-board generated rails.
- Place a jumper across P6 to connect the 2 V rail to the VDDLDO pin.

Off-Board Powering of Individual Power Rails

Any, or all of, the on-board power rails shown in the Power Supplies section can be externally supplied to the evaluation hardware, which can be useful for evaluating the AD4080 with different power solutions or for measuring the supply currents with benchtop equipment. When providing power to power rails individually from an alternative source, the user ensure that the source used can provide sufficient voltage and current to properly supply the rail. Failure to do so can result in damage to the on-board components.

SUPPORTED CONFIGURATIONS

CLOCK CIRCUITRY

Using an External Clock Source

The EVAL-AD4080-FMCZ allows bypassing of the ADF4350 synthesizer and supplying the AD9508 directly with an external clock. The following hardware changes must be applied:

- Remove the C137 and C138 capacitors.
- Populate R65 and R68 with 0 Ω resistors.

The user is still required to enter the desired sampling frequency in the **EVAL-AD4080-FMCZ** tab in the **ACE Software**. However, as the **ACE Software** plug-in is unaware of the external clock frequency, the user must take into account the divider factors that the **ACE Software** applies to the AD9508 and adjust the external clock frequency accordingly to effectively achieve the desired sampling rate. Table 2 describes how to choose the required external clock frequency for a desired sampling frequency. Entering a new sampling frequency in the **ACE Software** GUI also resynchronizes the AD4080 LVDS data with the ZedBoard host controller, which mandates that the external frequency be set before inputting the desired sample rate value through the **ACE Software** GUI. For example, for 40 MHz sampling, the input CLKIN frequency is first set to 400 MHz, and then, the **ACE Software** GUI is set to the desired 40 MHz frequency.

Table 2. Sampling Frequency Configuration with an External Clock Source (CLKIN)

Desired Sampling Frequency (Value Input in ACE Software GUI)	AD9508 Clock Dividers	Steps	External CLKIN Range
40 MSPS to 20 MSPS	CNV_P , CNV_N (OUT2, $\overline{\text{OUT2}}$): CLKIN divide by 10, CLK_P, CLK_N (OUT3, $\overline{\text{OUT3}}$): CLKIN divide by 1	**1.** Set the external CLKIN frequency to the desired sampling Frequency x10. **2.** Input the desired sampling frequency in MHz into the **ACE Software** GUI (see Figure 10).	400 MHz to 200 MHz, CLKIN = 400 MHz for 40 MSPS, CLKIN = 200 MHz for 20 MSPS
19.999 MSPS to 10 MSPS	CNV_P , CNV_N (OUT2, $\overline{\text{OUT2}}$): CLKIN divide by 20, CLK_P, CLK_N (OUT3, $\overline{\text{OUT3}}$): CLKIN divide by 2	**1.** Set the external CLKIN frequency to the desired sampling frequency x20. **2.** Input the desired sampling frequency in MHz into the **ACE Software** GUI (see Figure 10).	399.98 MHz to 200 MHz, CLKIN = 399.98 MHz for 19.999 MSPS, CLKIN = 200 MHz for 10 MSPS
9.999 MSPS to 5 MSPS	CNV_P , CNV_N (OUT2, $\overline{\text{OUT2}}$): CLKIN divide by 40, CLK_P, CLK_N (OUT3, $\overline{\text{OUT3}}$): CLKIN divide by 4	**1.** Set the external CLKIN frequency to the desired sampling frequency x40. **2.** Input the desired sampling frequency in MHz into the **ACE Software** GUI (see Figure 10).	399.96 MHz to 200 MHz, CLKIN = 399.96 MHz for 9.999 MSPS, CLKIN = 200 MHz for 5 MSPS
4.999 MSPS to 2.5 MSPS	CNV_P , CNV_N (OUT2, $\overline{\text{OUT2}}$): CLKIN divide by 80, CLK_P, CLK_N (OUT3, $\overline{\text{OUT3}}$): CLKIN divide by 8	**1.** Set the external CLKIN frequency to the desired sampling frequency x80. **2.** Input the desired sampling frequency in MHz into the **ACE Software** GUI (see Figure 10).	399.92 MHz to 200 MHz, CLKIN = 399.92 MHz for 4.999 MSPS, CLKIN = 200 MHz for 2.5 MSPS
2.499 MSPS to 1.25 MSPS	CNV_P , CNV_N (OUT2, $\overline{\text{OUT2}}$): CLKIN divide by 160, CLK_P, CLK_N (OUT3, $\overline{\text{OUT3}}$): CLKIN divide by 16	**1.** Set the external CLKIN frequency to the desired sampling frequency x160. **2.** Input the desired sampling frequency in MHz into the **ACE Software** GUI (see Figure 10).	399.84 MHz to 200 MHz, CLKIN = 399.84 MHz for 2.499 MSPS, CLKIN = 200 MHz for 1.25 MSPS

SUPPORTED CONFIGURATIONS

Configuring for CMOS CNV Mode

The hardware changes required to operate in CMOS CNV mode are as follows:

- Remove the 100 Ω termination resistor (RTCNV).
- Populate R38 with a 0 Ω resistor to tie CNV− to GND.
- Then both the AD4080 and AD9508 must be configured for CMOS input and output mode, respectively, as follows:
  - The AD4080 must be configured to accept CMOS level CNV signaling. Refer to the LVDS_CNV_EN bit in the ADC_DATA_INTF_CONFIG_B register (Register 0x16, Bit 0) in the AD4080 data sheet for additional details.
  - The AD9508 OUT2 channel must then be reconfigured for CMOS level signaling. Refer to Register 0x1F (OUT1 driver) and Register 0x20 (OUT1 CMOS) of the AD9508 data sheet for further detail on configuring the output drivers.

SUPPORTED CONFIGURATIONS

LINK CONFIGURATION OPTIONS

The EVAL-AD4080-FMCZ contains multiple solder links, jumpers, and a switch array to enable various configurations on the evaluation hardware. Table 3 through Table 8 summarize the functions and default settings of these components.

Table 3. Amplifier Power Mode and Power Down Switch Array (S1) Functionality

Switch	Function	S1 Closed (ON)
S1-1	Stage 1 amplifier U1 enable or disable	U1 disabled
S1-2	Stage 1 amplifier U2 enable or disable	U2 disabled
S1-3	Stage 3 A1 and A6 enable or disable	A1 and A6 disabled
S1-4	Stage 2 FDA power mode select	Low power mode

Table 4. Solder Link Settings: Analog Front End

Link	Default Pads	Function	Comment
JP3	Pad 2 to Pad 3	Selects the signal connected to Pin 16 (digital ground, D_{GND}) of the FDA (ADA4945-1, U3). This pin is the ground reference for the disable signal. By default, R124 is bridging Pad 2 to Pad 3; therefore, Pin 16 of U3 is connected to the AGND of the hardware.	Change the connection to Pad 1 to Pad2 to connect Pin 16 to VSSDRV and remove R124. Apply change when swapping the ADA4945-1 for ADA4932-1.
JP4	Pad 2 to Pad 3	Selects the signal connected to Pin 5 (power mode selection, MODE) of the FDA (ADA4945-1, U3).By default, R125 is bridging Pad 2 to Pad 3; therefore, Pin 5 of U3 is connected to the PMSEL signal.	Change the connection to 1-2 to connect Pin 5 to VDDDRV and remove R125. Apply change when swapping ADA4945-1 for ADA4932-1.
JP5	Pad 2 to Pad 3	Selects the signal connected to Pin 8 of the FDA. For the ADA4945-1 (U3), Pin 8 is used to select the positive clamp voltage. By default, R126 is bridging Pad 2 to Pad 3; therefore, Pin 8 of U3 is connected to REF.	Change to Pad 1 to Pad2 to connect Pin 8 to VDDDRV and remove R126. Apply change when swapping ADA4945-1 for ADA4932-1.
JP6	Pad 2 to Pad 3	Selects the signal connected to Pin 13 of the FDA. For the ADA4945-1 (U3), Pin 13 selects the negative clamp voltage. By default, R127 bridges Pin 2 to Pin 3; therefore, Pin 13 of U3 is connected to AGND.	Change to 1-2 to connect Pin 13 to VSSDRV and remove R127. Apply change when swapping ADA4945-1 for ADA4932-1.
JP7 and JP14	Pad 2 to Pad 3	Enables a path to AGND or VOCM at the negative input node of the FDA (U3). By default, this pin is connected to AGND.	Keep this link in the Pad 1 to Pad2 position. This position, along with the fitting of R78 and R29, can be used to apply gain in Stage 1 through the R5, R7, R8, and R9 resistors.
JP15 and JP16	Pad 2 to Pad 3	Selection of the input path to Stage 3 amplifiers (ADA4899-1, A1 and A6). By default, the input is connected to the output of Stage 2.	Connect both across Pad 1 to Pad 2 to ground the Stage 3 inputs. Apply this change when disabling Stage 3.
JP17 and JP18	Pad 2 to Pad 3	Selects the input path of the ADC to be connected to either the output of Stage 2 or the output of Stage 3. By default, Stage 3 is connected to the ADC input.	Change both to Pad 1 to Pad 2 to connect the input of the ADC to the Stage 2 output. Apply this change when disabling Stage 3.
JP19	No link	Selects the source of the power supply for Pin 3 of the AMC connector (P1).	See the Stage 3 Bypass section
JP20	No link	Selects the source of the power supply for Pin 5 of the AMC connector (P1).	See the Stage 3 Bypass section

Table 5. Solder Link Settings: External Reference Buffering

Link	Default	Function	Comment
JP1 and JP2	JP1: 1-2 and JP2: 2-3	Selection of the buffered or unbuffered path for the external voltage reference output signal, VREF. The default is the unbuffered path.	Change link JP1 to 2-3 and JP2 to 1-2 to enable the buffered path. Note that the external reference buffer is not necessary and not recommended.

Table 6. Solder Link Settings: Common-Mode Buffering

Link	Default	Function	Comment
JP8 and JP9	1-2	Selection path for the AD4080 common-mode output signal between the buffered and unbuffered. By default, the unbuffered path is selected.	Connect across 2-3 to select the buffered path

SUPPORTED CONFIGURATIONS

Table 7. Solder Link Settings: Digital Interface

Link	Default	Function	Comment
JP10, JP11, JP12, and JP13	2-3	For the SPI level translators (U4, U5, U6, and U7), select the connection of the ADC SPI data outputs from either the ADC pins or ground (default).	Do not change the connection in these solder links.

Table 8. Jumper Settings: Internal LDOs

Jumper	Default	Function	Comment
P6	Disconnected	Select whether the 2 V on-board supply rail is connected to the AD4080 internal LDO regulators supply pin or not.	Connect to supply the internal LDO regulators.
P9 and P10	Connected	Select whether the 1.1 V supply rails are supplied by the on-board LDO regulators (U34 and U35) or the internal LDO regulators s from the AD4080.	Disconnect to stop using the on-board LDO regulators and use the internal LDO regulators instead.

ANALOG FRONT END (AFE) CONSIDERATIONS

The AFE of EVAL-AD4080-FMCZ can be modified to suit the needs of specific applications. Applying changes to the AFE usually involves trade-offs, and designing the right AFE for an application requires careful consideration. The following sections discuss some of the items that must be taken into consideration when designing or modifying the AFE for this hardware evaluation platform.

INPUT SIGNAL FILTERING

Limiting the bandwidth at the input of the signal chain to the region where the signal of interest lies helps reduce excess noise. This reduction of noise can be achieved by the provided mechanisms in the form of the RC filter at the board input, the addition of the do not install (DNI) capacitors in the amplifier feedback network bandwidth adjustment in Stage 1, or the increasing of the capacitance value for the existing capacitors in the FDA feedback loop. Note that the value of filter resistors may have an impact on the overall SNR.

The internal digital filters available inside the AD4080 are a useful feature when considering the filtering in the signal chain as a whole. The user can programmatically set a low pass filter, choosing a simple sinc1 filter or a higher order sinc5 with a sharp roll-off to compliment the AFE filter or to help relax its design requirements.

POWER vs. BANDWIDTH vs. NOISE

Choosing the lowest noise, lowest distortion, highest precision, wider bandwidth amplifiers may require more power to be consumed in the AFE to reach the required target performance. Therefore, power constrained applications must carefully consider the choice of each amplifier.

GAIN

Care must be taken in the signal chain to consider where it is optimum to place gain to maximize the SNR. As an example, it may be better to add the required signal gain in a preceding low noise amplifier stage rather than in the FDA that is tasked with driving the AD4080 because the FDA noise gain may have a bigger impact on the signal chain SNR than the gain set by the preceding lower noise stage.

ADC DRIVER STAGE

See the Easy Drive Analog Inputs section in the AD4080 data sheet for details about this topic.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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