ADPL16000

60V, 400mA, Ultra-Small, High-Efficiency, Synchronous Step-Down DC-DC Converters

FEATURES

- Eliminates External Components and Reduces Total Cost
  - No Schottky—Synchronous Operation for High Efficiency and Reduced Cost
  - Internal Compensation
  - Internal Feedback Divider for Fixed 3.3V, 5V Output Voltages
  - Internal Soft-Start
  - All Ceramic Capacitors, Ultra-Compact Layout
- Flexibility to Support Multiple Rails in a System
  - Wide 4.5V to 60V Input Voltage Range
  - Fixed 3.3V and 5V Output Voltage Options
  - Adjustable 0.9V to 0.89 x V_{IN} Output Voltage Option
  - Delivers up to 400mA Load Current
  - Configurable Between PFM and Forced-PWM Modes
- Reduces Power Dissipation
  - 92% Peak Efficiency
  - PFM Feature for High Light-Load Efficiency
  - 2.2µA (typ) Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Current Limit and Auto-retry Startup
  - Built-In Output Voltage Monitoring with Open-Drain $\overline{\text{RESET}}$ Pin
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Output
  - Overtemperature Protection
  - Wide -40°C to +125°C Ambient Operating Temperature Range and -40°C to +150°C Junction Temperature Range
  - Complies with CISPR32 (EN55032) Class B Conducted and Radiated Emissions

GENERAL DESCRIPTION

The ADPL16000 family of products are high-efficiency, high-voltage, synchronous DC-DC converters with integrated MOSFETs operating over a wide input-voltage range of 4.5V to 60V.

The converters can deliver up to 400mA and generate output voltages from 0.9V to 0.89 x V_{IN}; ADPL16000A is fixed at 3.3V, ADPL16000B is fixed at 5.0V, and ADPL16000C is adjustable. The family of converters is available in a compact, 8-pin, 2mm x 2mm TDFN-CU package.

The device employs a peak-current-mode control architecture with a MODE pin that can be used to operate the device in pulse-width modulation (PWM) or pulse-frequency modulation (PFM) control schemes. PWM operation provides constant frequency operation at all loads and is useful in applications sensitive to variable switching frequency. PFM operation disables negative inductor current, and additionally skips pulses at light loads for high-efficiency. The low-resistance on-chip MOSFETs ensure high-efficiency at full load and simplify the PCB layout.

APPLICATIONS

- Industrial Sensors
- 4–20mA Current Loops
- HVAC and Building Control
- High-Voltage LDO Replacement
- General Purpose Point-of-Load

One Analog Way, Wilmington, MA 01887-2356, U.S.A. | Tel: 781.329.4700

TYPICAL APPLICATION CIRCUIT

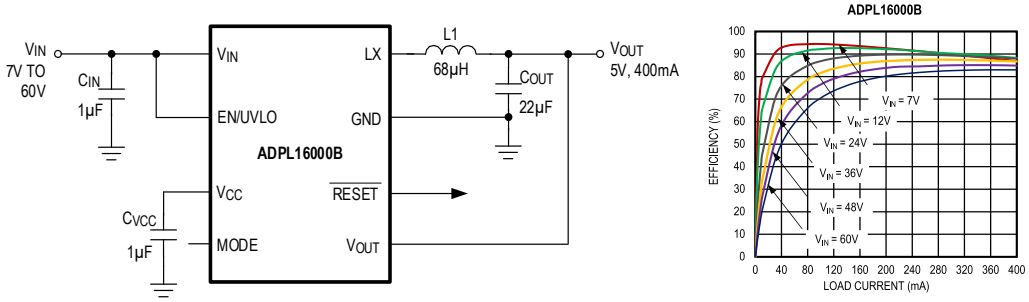


Figure 1. Simplified Application Diagram and Efficiency vs. Load Current

TABLE OF CONTENTS

Features 1
General Description 1
Applications 1
Typical Application Circuit 2
Revision history 4
Specifications 5
Absolute Maximum Ratings 8
Pin Configurations and Function Descriptions 9
Block Diagram 10
Typical Performance Characteristics 11
Detailed Description 20
DC-DC Switching Regulator 20
Mode Selection (MODE) 20
PWM Mode Operation 20
PFM Mode Operation 20
Internal 5V Linear Regulator 21
Enable Input (EN/UVLO), Soft-Start 21
Reset Output (RESET) 21
Startup into a Prebiased Output 21
Operating Input Voltage Range 21
Overcurrent Protection/Hiccup Mode 22
Thermal Overload Protection 22
Applications Information 23
Inductor Selection 23
Input Capacitor 23
Output Capacitor 24
Setting the Input Undervoltage-Lockout Level 24
Adjusting the Output Voltage 25
Power Dissipation 25
PCB Layout Guidelines 26
Typical Application Circuits 28
3.3V, 400mA Step-Down Regulator 28
5V, 400mA Step-Down Regulator 28
2.5V, 400mA Step-Down Regulator 28

12V, 400mA Step-Down Regulator 29
1.8V, 400mA Step-Down Regulator 29
15V, 400mA Step-Down Regulator 29
Outline Dimensions 30
Land Pattern 31
Ordering Guide 32

REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	03/24	Initial Release	—

SPECIFICATIONS

Table 1. Electrical Characteristics

((V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, LX = MODE = $\overline{RESET}$ = unconnected; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) [1])

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})							
Input Voltage Range	V_{IN}			4.5		60	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V, shutdown mode			2.2	4.0	µA
Input Supply Current	I_{Q-PFM}	MODE = unconnected, FB/V_{OUT} = 1.03 x FB/$V_{OUT-REG}$			95	160	µA
	I_{Q-PWM}	Normal switching mode, V_{IN} = 24V			2.5	4.0	mA
ENABLE/UVLO (EN/UVLO)							
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising		1.190	1.215	1.240	V
	V_{ENF}	$V_{EN/UVLO}$ falling		1.06	1.09	1.15	V
	$V_{EN-TRUESD}$	$V_{EN/UVLO}$ falling, true shutdown			0.75		V
EN/UVLO Input Leakage Current	$I_{EN/UVLO}$	$V_{EN/UVLO}$ = 60V, T_A = +25°C		-100		+100	nA
LDO (V_{CC})							
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 60V, 0mA < I_{VCC} < 10mA		4.75	5.00	5.25	V
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 12V		13	30	50	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 5mA			0.15	0.30	V
V_{CC} UVLO	V_{CC-UVR}	V_{CC} rising		4.05	4.18	4.30	V
	V_{CC-UVF}	V_{CC} falling		3.70	3.80	3.95	V
POWER MOSFETs							
High-Side pMOS On-Resistance	R_{DS-ONH}	I_{LX} = 0.3A (sourcing)	T_A = +25°C		1.3	1.8	Ω
			T_A = T_J = +125°C			2.7	Ω
Low-Side nMOS On-Resistance	R_{DS-ONL}	I_{LX} = 0.3A (sinking)	T_A = +25°C		0.47	0.62	Ω
			T_A = T_J = +125°C			0.9	Ω

((V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, LX = MODE = $\overline{RESET}$ = unconnected; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) (1))

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
LX Leakage Current	I_{LX-LKG}	$V_{EN/UVLO}$ = 0V, V_{IN} = 60V, T_A= +25°C, V_{LX} = (V_{GND} + 1V) to (V_{IN} - 1V)		-1		+1	µA
SOFT-START (SS)							
Soft-Start Time	t_{SS}			3.8	4.1	4.4	ms
FEEDBACK (FB)							
FB Regulation Voltage	V_{FB-REG}	MODE = GND, ADPL16000C		0.887	0.900	0.913	V
		MODE = unconnected, ADPL16000C		0.887	0.915	0.936	V
FB Leakage Current	I_{FB}	ADPL16000C, T_A = +25°C		-100	-25		nA
OUTPUT VOLTAGE (V_{OUT})							
V_{OUT} Regulation Voltage	$V_{OUT-REG}$	MODE = GND, ADPL16000A		3.25	3.30	3.35	V
		MODE = unconnected, ADPL16000A		3.25	3.35	3.42	V
		MODE = GND, ADPL16000B		4.93	5.00	5.07	V
		MODE = unconnected, ADPL16000B		4.93	5.08	5.18	V
CURRENT LIMIT							
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$			0.54	0.62	0.73	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$			0.63	0.75	0.85	A
Negative Current-Limit Threshold	$I_{SINK-LIMIT}$	MODE = GND		0.25	0.30	0.35	A
		MODE = unconnected			0.01		mA
PFM Current Level	I_{PFM}				0.15		A
TIMING							
Switching Frequency	f_{SW}			465	500	535	kHz
Events to Hiccup After Crossing Runaway Current Limit					1		cycles

((V_{IN} = 24V, V_{GND} = 0V, C_{IN} = C_{VCC} = 1µF, $V_{EN/UVLO}$ = 1.5V, LX = MODE = $\overline{RESET}$ = unconnected; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to GND, unless otherwise noted.) [1])

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS
FB/V_{OUT} Undervoltage-Trip Level to Cause Hiccup				62.5	64.5	66.5	%
Hiccup Timeout					131		ms
Minimum On-Time	t_{ON-MIN}				90	130	ns
Maximum Duty Cycle	D_{MAX}	FB/V_{OUT} = 0.98 x FB/$V_{OUT-REG}$		89.0	91.5	94.0	%
LX Dead Time					5		ns
$\overline{RESET}$							
FB/V_{OUT} Threshold for $\overline{RESET}$ Rising		FB/V_{OUT} rising		93.5	95.5	97.5	%
FB/V_{OUT} Threshold for $\overline{RESET}$ Falling		FB/V_{OUT} falling		90	92	94	%
$\overline{RESET}$ Delay After FB/V_{OUT} Reaches 95% Regulation					2		ms
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 5mA				0.2	V
$\overline{RESET}$ Output Leakage Current		$V_{\overline{RESET}}$ = 5.5V, T_A = +25°C				0.1	µA
MODE							
MODE Internal Pullup Resistor					500		kΩ
THERMAL SHUTDOWN							
Thermal-Shutdown Threshold		Temperature rising			166		°C
Thermal-Shutdown Hysteresis					10		°C

1 All limits are 100% tested at T_A = +25°C. Limits over temperature are guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
V_{IN} to GND	-0.3V to 70V
EN/UVLO to GND	-0.3V to 70V
LX to GND	-0.3V to V_{IN} + 0.3V
V_{CC}, FB/V_{OUT}, $\overline{\text{RESET}}$ to GND	-0.3V to 6V
MODE to GND	-0.3V to V_{CC} + 0.3V
LX total RMS Current	±800mA
Output Short-Circuit Duration	Continuous
Continuous Power Dissipation (T_A = +70°C) 8-Pin TDFN-CU (derate 6.2mW/°C above +70°C)	496mW
Junction Temperature ([1])	+150°C
Storage Temperature Range	-65°C to +150°C
Soldering Temperature (reflow)	+260°C
Lead Temperature (soldering, 10s)	+300°C

[1] Junction temperature greater than +125°C degrades operating lifetimes.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

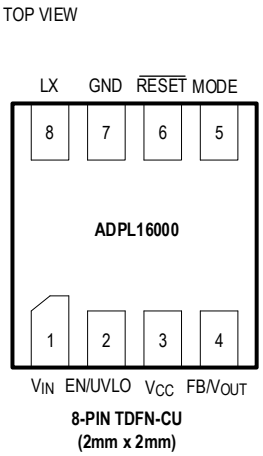


Figure 2. Pin Configuration

Table 3. Pin Descriptions

PIN CFG 1	NAME	DESCRIPTION
1	V_{IN}	Switching Regulator Power Input. Connect a X7R 1µF ceramic capacitor from V_{IN} to GND for bypassing.
2	EN/UVLO	Active-High, Enable/Undervoltage-Detection Input. Pull EN/UVLO to GND to disable the regulator output. Connect EN/UVLO to V_{IN} for always-on operation. Connect a resistor-divider between V_{IN} and EN/UVLO to GND to program the input voltage at which the device is enabled and turned on.
3	V_{CC}	Internal LDO Power Output. Bypass V_{CC} to GND with a minimum 1µF capacitor.
4	FB/V_{OUT}	Feedback Input. For fixed output voltage versions, connect FB/V_{OUT} directly to the output. For the adjustable output voltage version, connect FB/V_{OUT} to a resistor-divider between V_{OUT} and GND to adjust the output voltage from 0.9V to 0.89 x V_{IN}.
5	MODE	PFM/PWM Mode Selection Input. Connect MODE to GND to enable the fixed-frequency PWM operation. Leave unconnected for light-load PFM operation.
6	$\overline{\text{RESET}}$	Open-Drain Reset Output. Pull up $\overline{\text{RESET}}$ to an external power supply with an external resistor. $\overline{\text{RESET}}$ goes low when the output voltage drops below 92% of the set nominal regulated voltage. $\overline{\text{RESET}}$ goes high impedance 2ms after the output voltage rises above 95% of its regulation value. See the *Electrical Characteristics* table for threshold values.
7	GND	Ground. Connect GND to the power ground plane. Connect all circuit ground connections together at a single point. See the *PCB Layout Guidelines* section.
8	LX	Inductor Connection. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown.

BLOCK DIAGRAM

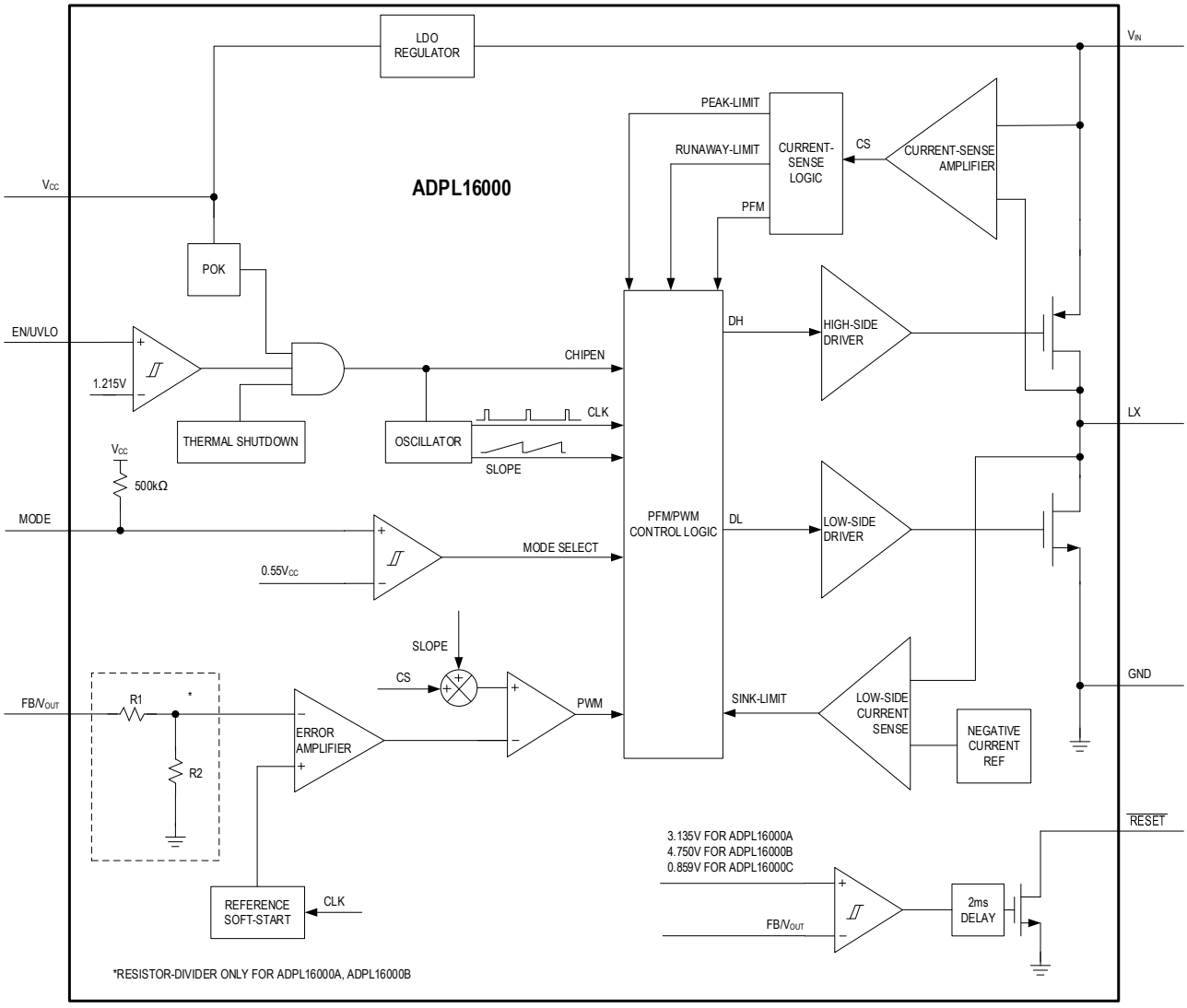


Figure 3. Block Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

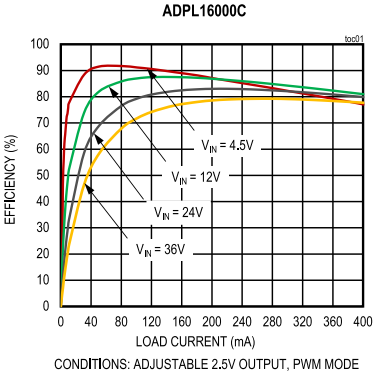


Figure 4. Efficiency vs. Load Current, Figure 64 Circuit

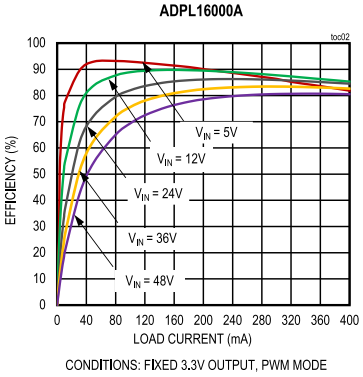


Figure 5. Efficiency vs. Load Current, Figure 62 Circuit

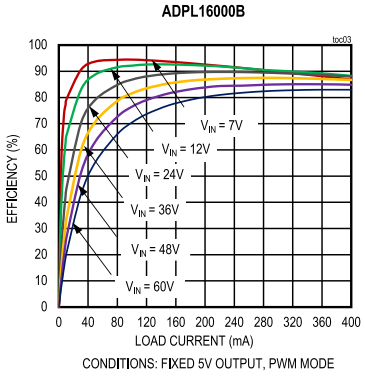


Figure 6. Efficiency vs. Load Current, Figure 63 Circuit

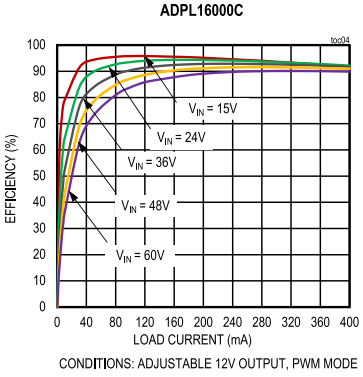


Figure 7. Efficiency vs. Load Current, Figure 65 Circuit

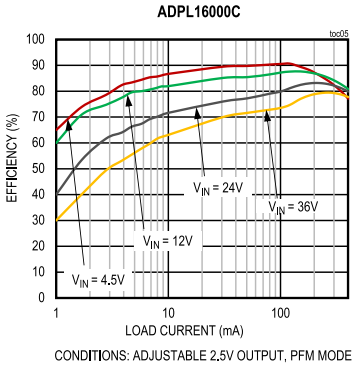


Figure 8. Efficiency vs. Load Current, Figure 64 Circuit

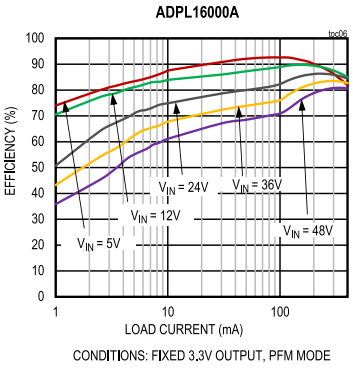


Figure 9. Efficiency vs. Load Current, Figure 62 Circuit

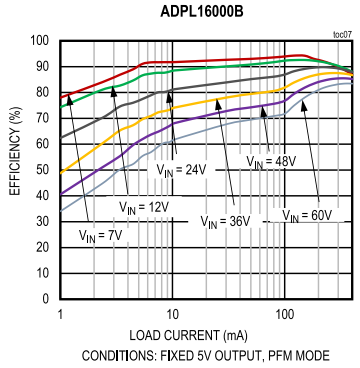


Figure 10. Efficiency vs. Load Current, Figure 63 Circuit

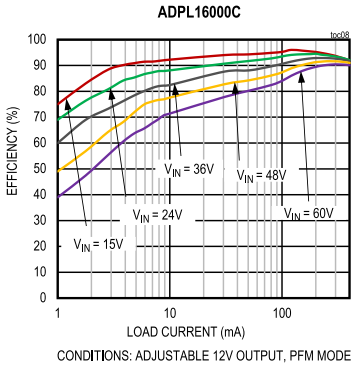


Figure 11. Efficiency vs. Load Current, Figure 65 Circuit

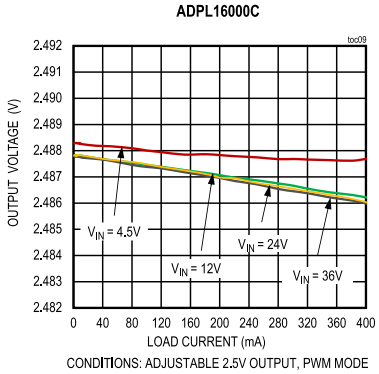


Figure 12. Output Voltage vs. Load Current, Figure 64 Circuit

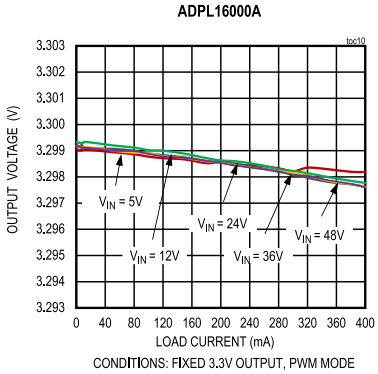


Figure 13. Output Voltage vs. Load Current, Figure 62 Circuit

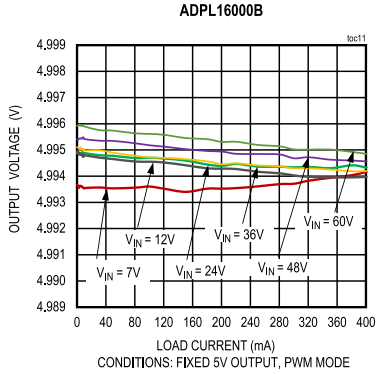


Figure 14. Output Voltage vs. Load Current, Figure 63 Circuit

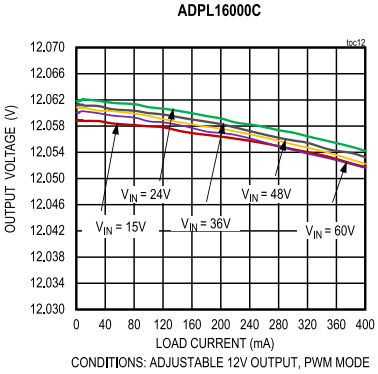


Figure 15. Output Voltage vs. Load Current, Figure 65 Circuit

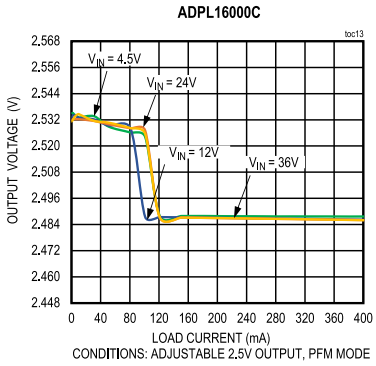


Figure 16. Output Voltage vs. Load Current, Figure 64 Circuit

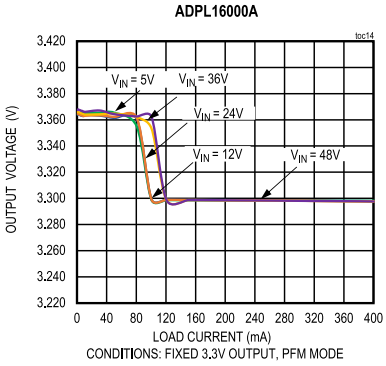


Figure 17. Output Voltage vs. Load Current, Figure 62 Circuit

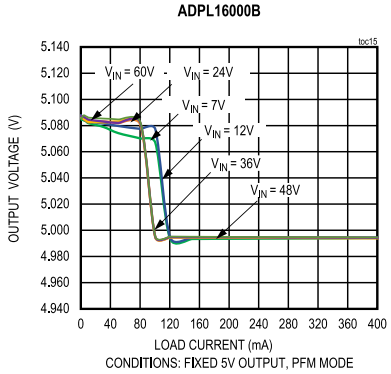


Figure 18. Output Voltage vs. Load Current, Figure 63 Circuit

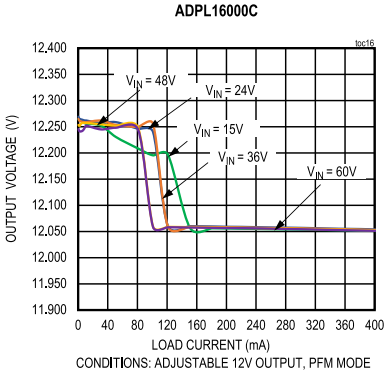


Figure 19. Output Voltage vs. Load Current, Figure 65 Circuit

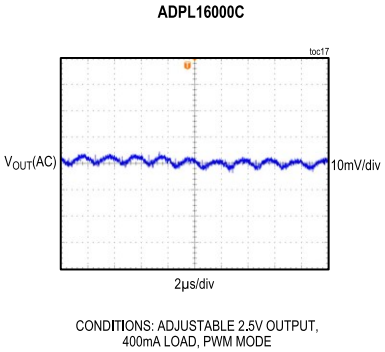


Figure 20. Output Voltage Ripple, Figure 64 Circuit

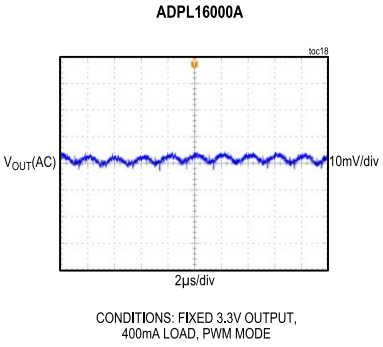
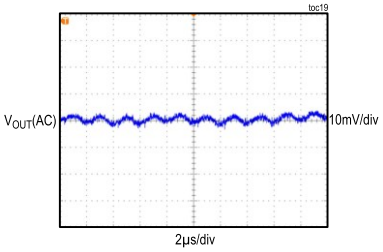


Figure 21. Output Voltage Ripple, Figure 62 Circuit

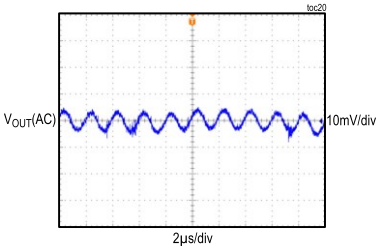
ADPL16000B



CONDITIONS: FIXED 5V OUTPUT,
400mA LOAD, PWM MODE

Figure 22. Output Voltage Ripple, Figure 63 Circuit

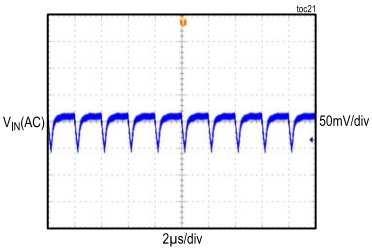
ADPL16000C



CONDITIONS: ADJUSTABLE 12V OUTPUT
400mA LOAD, PWM MODE

Figure 23. Output Voltage Ripple, Figure 65 Circuit

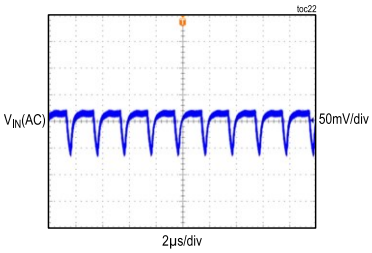
ADPL16000C



CONDITIONS: ADJUSTABLE 2.5V OUTPUT,
400mA LOAD, PWM MODE

Figure 24. Input Voltage Ripple, Figure 64 Circuit

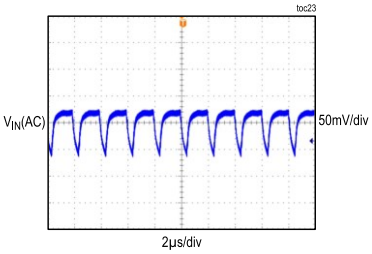
ADPL16000A



CONDITIONS: FIXED 3.3V OUTPUT,
400mA LOAD, PWM MODE

Figure 25. Input Voltage Ripple, Figure 62 Circuit

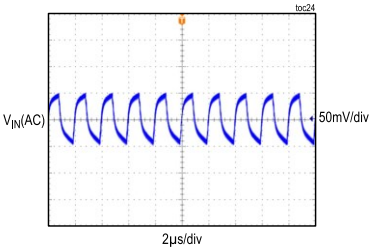
ADPL16000B



CONDITIONS: FIXED 5V OUTPUT,
400mA LOAD, PWM MODE

Figure 26. Input Voltage Ripple, Figure 63 Circuit

ADPL16000C



CONDITIONS: ADJUSTABLE 12V OUTPUT,
400mA LOAD, PWM MODE

Figure 27. Input Voltage Ripple, Figure 65 Circuit

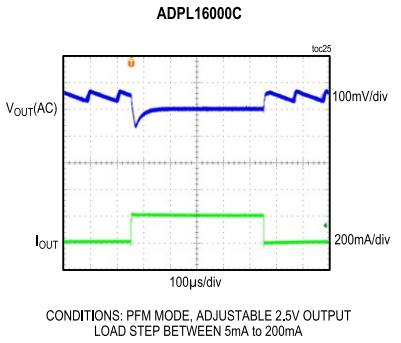


Figure 28. Load Transient Response, Figure 64 Circuit

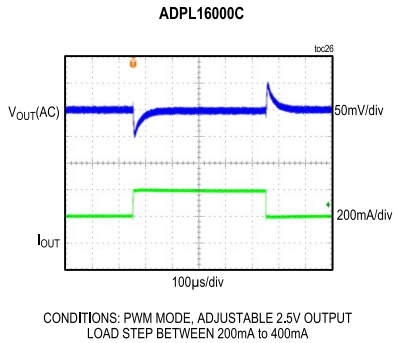


Figure 29. Load Transient Response, Figure 64 Circuit

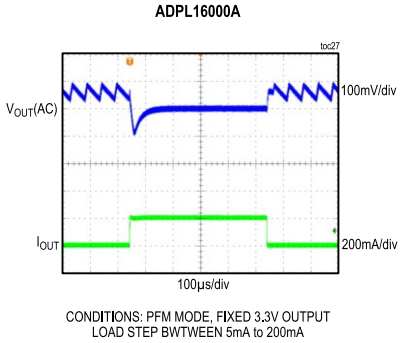


Figure 30. Load Transient Response, Figure 62 Circuit

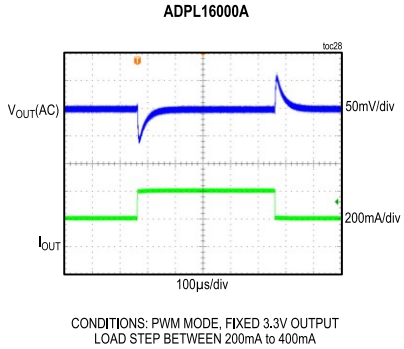


Figure 31. Load Transient Response, Figure 62 Circuit

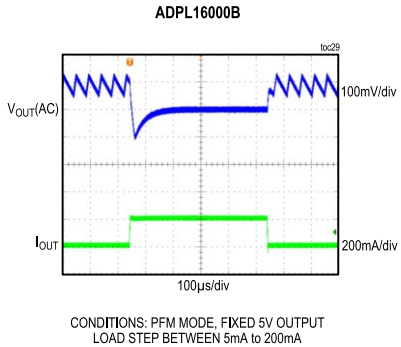


Figure 32. Load Transient Response, Figure 63 Circuit

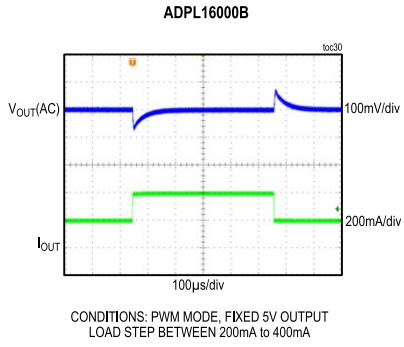


Figure 33. Load Transient Response, Figure 63 Circuit

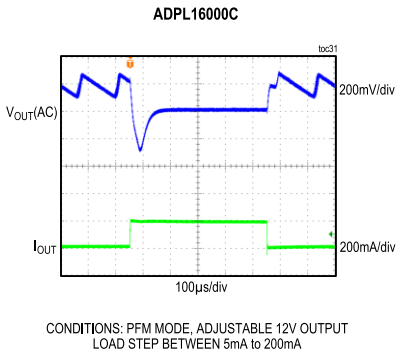


Figure 34. Load Transient Response, Figure 65 Circuit

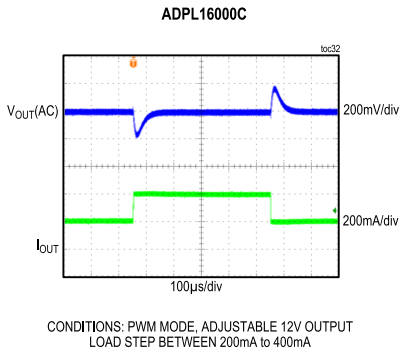


Figure 35. Load Transient Response, Figure 65 Circuit

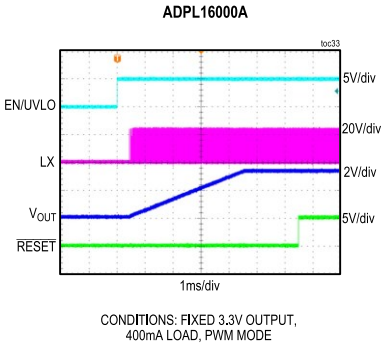


Figure 36. Startup through Enable, Figure 62 Circuit

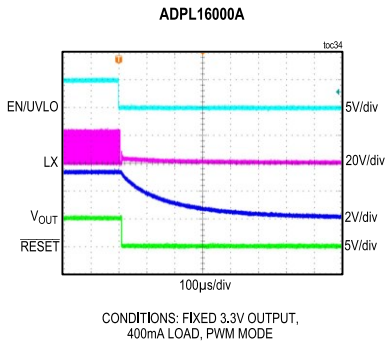


Figure 37. Shutdown through Enable, Figure 62 Circuit

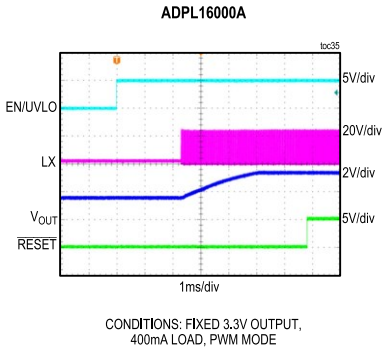


Figure 38. Startup through Enable (1.5V Prebias), Figure 62 Circuit

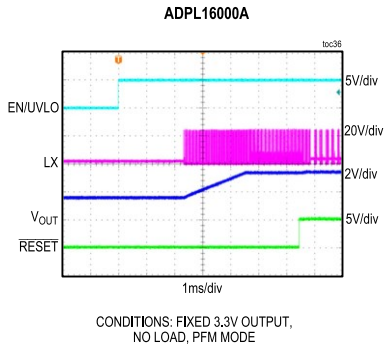


Figure 39. Startup through Enable (1.5V Prebias), Figure 62 Circuit

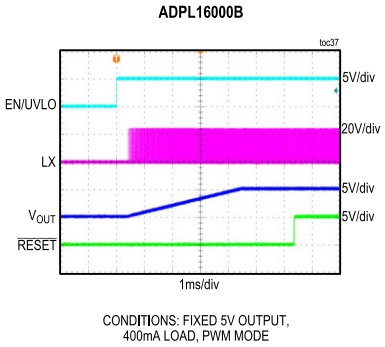


Figure 40. Startup through Enable, Figure 63 Circuit

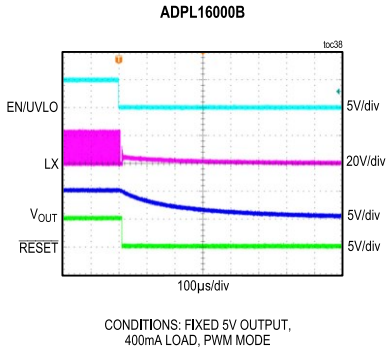


Figure 41. Shutdown through Enable, Figure 63 Circuit

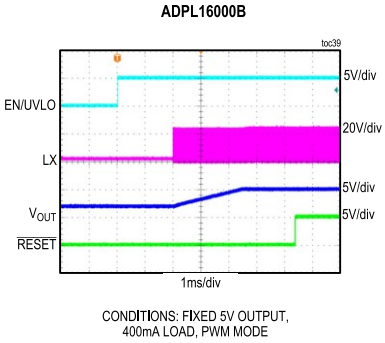


Figure 42. Startup through Enable (2V Prebias), Figure 63 Circuit

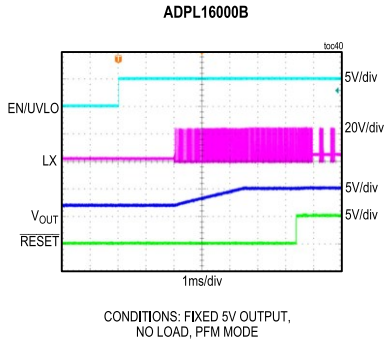


Figure 43. Startup through Enable (2V Prebias), Figure 63 Circuit

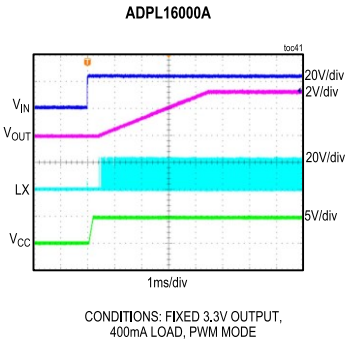


Figure 44. Startup through V_{IN}, Figure 62 Circuit

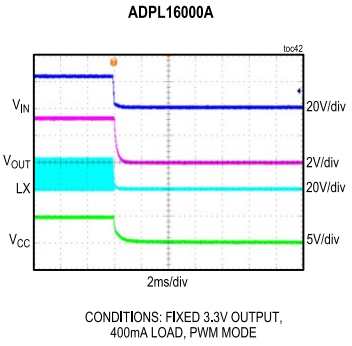


Figure 45. Shutdown through V_{IN}, Figure 62 Circuit

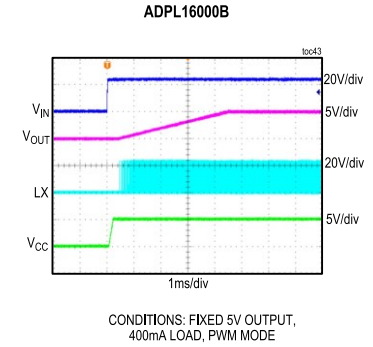


Figure 46. Startup through V_{IN}, Figure 63 Circuit

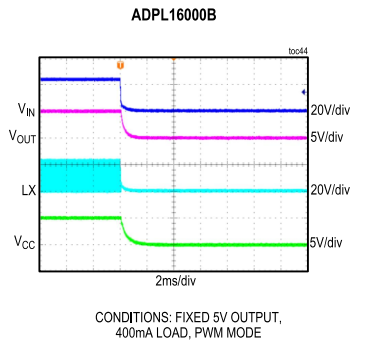


Figure 47. Shutdown through V_{IN}, Figure 63 Circuit

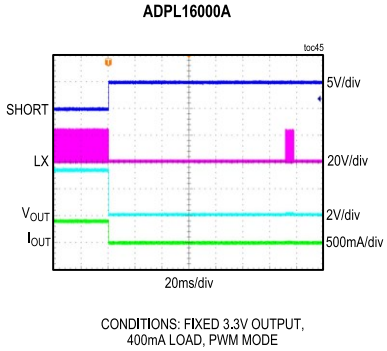


Figure 48. Output Short in Steady State, Figure 62 Circuit

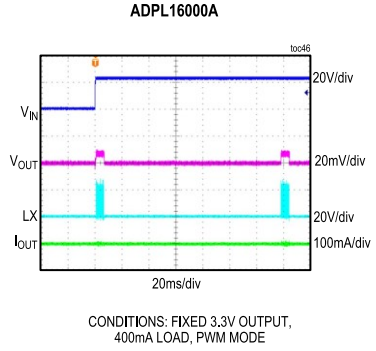


Figure 49. Output Short **uring Startup, Figure 62 Circuit

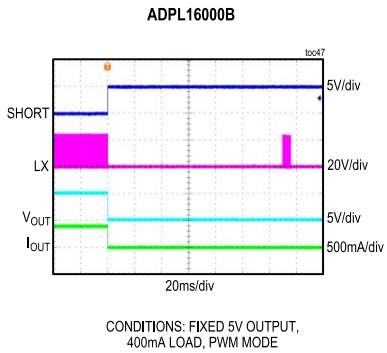


Figure 50. Output Short In Steady State, Figure 63 Circuit

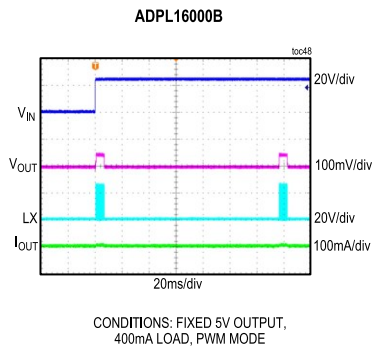


Figure 51. Output Short During Startup, Figure 63 Circuit

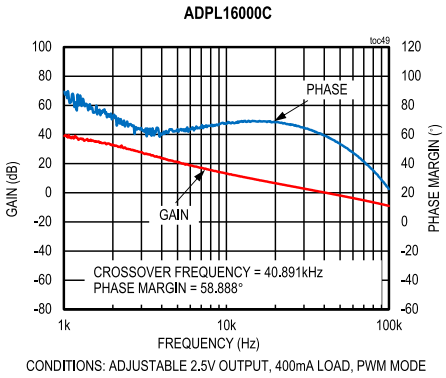


Figure 52. Bode Plot, Figure 64 Circuit

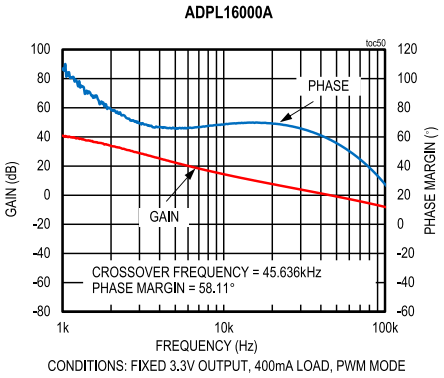


Figure 53. Bode Plot, Figure 62 Circuit

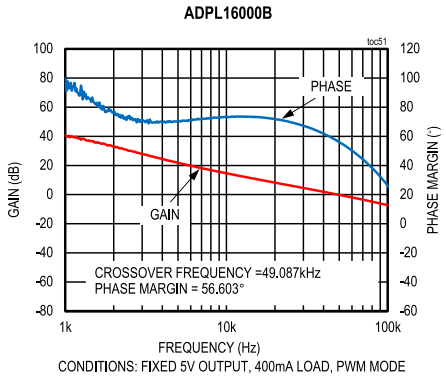


Figure 54. Bode Plot, Figure 63 Circuit

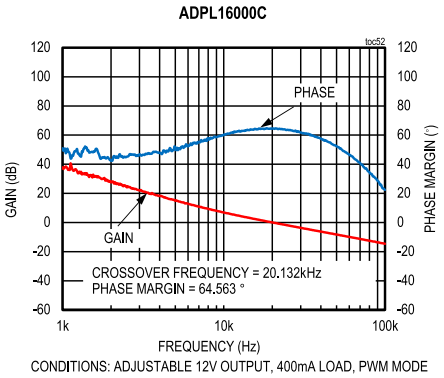


Figure 55. Bode Plot, Figure 65 Circuit

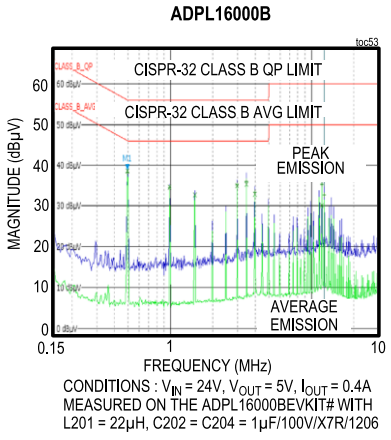


Figure 56. Conducted Emissions Plot

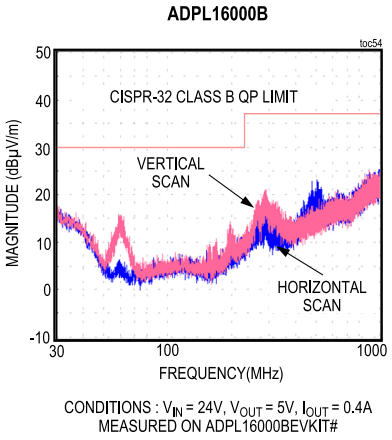


Figure 57. Radiated Emissions Plot

DETAILED DESCRIPTION

The ADPL16000 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a wide 4.5V to 60V input voltage range. The converter delivers output current up to 400mA at 3.3V (ADPL16000A), 5V (ADPL16000B), and adjustable output voltages (ADPL16000C). When EN/UVLO and V_{CC} UVLO are satisfied, an internal power-up sequence soft-starts the error-amplifier reference, resulting in a clean monotonic output voltage soft-start independent of the load current. The FB/V_{OUT} pin monitors the output voltage through a resistor-divider. $\overline{\text{RESET}}$ transitions to a high-impedance state 2ms after the output voltage reaches 95% of regulation. The device selects either PFM or forced-PWM mode depending on the state of the MODE pin at power-up. By pulling the EN/UVLO pin to low, the device enters the shutdown mode and consumes only 2.2µA (typ) of standby current.

DC-DC Switching Regulator

The device uses an internally compensated, fixed-frequency, current-mode control scheme (see *Block Diagram*). On the rising edge of an internal clock, the high-side pMOSFET turns on. An internal error amplifier compares the feedback voltage to a fixed internal reference voltage and generates an error voltage. The error voltage is compared to the sum of the current-sense voltage and a slope-compensation voltage by a PWM comparator to set the on-time. During the on-time of the pMOSFET, the inductor current ramps up. For the remainder of the switching period (off-time), the pMOSFET is kept off, and the low-side nMOSFET turns on. During the off-time, the inductor releases the stored energy as the inductor current ramps down, providing current to the output. Under overload conditions, the cycle-by-cycle current-limit feature limits the inductor peak current by turning off the high-side pMOSFET and turning on the low-side nMOSFET.

Mode Selection (MODE)

The logic state of the MODE pin is latched after V_{CC} and EN/UVLO voltages exceed respective UVLO rising thresholds, and all internal voltages are ready to allow LX switching. If the MODE pin is unconnected at power-up, the part operates in PFM mode at light loads. If the MODE pin is grounded at power-up, the part operates in constant-frequency PWM mode at all loads. State changes on the MODE pin are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation is useful in frequency-sensitive applications and provides a fixed switching frequency at all loads. However, the PWM mode of operation gives lower efficiency at light loads compared to the PFM mode of operation.

PFM Mode Operation

PFM mode operation disables negative inductor current and additionally skips pulses at light loads for high-efficiency. In PFM mode, the inductor current is forced to a fixed peak of 150mA every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both high-side and low-side FETs are turned off, and the part enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operations to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage. The device naturally exits PFM mode when the load current exceeds 90mA (typ). The advantage of the PFM mode is higher efficiency at light loads because of the lower quiescent current drawn from the supply.

Internal 5V Linear Regulator

An internal regulator provides a 5V nominal supply to power the internal functions and drive the power MOSFETs. The output of the linear regulator (V_{CC}) should be bypassed with a 1µF capacitor to GND. The V_{CC} regulator dropout voltage is typically 150mV. An undervoltage-lockout circuit disables the regulator when V_{CC} falls below 3.8V (typ). The 400mV V_{CC} UVLO hysteresis prevents chattering on power-up and power-down.

Enable Input (EN/UVLO), Soft-Start

When the EN/UVLO voltage is above 1.21V (typ), the device's internal error-amplifier reference voltage starts to ramp up. The duration of the soft-start ramp is 4.1ms, allowing a smooth increase of the output voltage. Driving EN/UVLO low disables both power MOSFETs, as well as other internal circuitry, and reduces V_{IN} quiescent current to 2.2µA (typ). EN/UVLO can be used as an input-voltage UVLO adjustment input. An external voltage-divider between V_{IN} and EN/UVLO to GND adjusts the input voltage at which the device turns on or turns off. If input UVLO programming is not desired, connect EN/UVLO to V_{IN} (see the *Electrical Characteristics* table for EN/UVLO rising and falling threshold voltages).

Reset Output ($\overline{\text{RESET}}$)

The device includes an open-drain $\overline{\text{RESET}}$ output to monitor the output voltage. $\overline{\text{RESET}}$ goes high impedance 2ms after the output rises above 95% of its nominal set value and pulls low when the output voltage falls below 92% of the set nominal regulated voltage. $\overline{\text{RESET}}$ asserts low during the hiccup timeout period.

Startup into a Prebiased Output

The device is capable of soft-start into a prebiased output without discharging the output capacitor in both the PFM and forced-PWM modes. Such a feature is useful in applications where digitally integrated circuits with multiple rails are powered.

Operating Input Voltage Range

The maximum operating input voltage is determined by the minimum controllable on-time, and the minimum operating input voltage is determined by the maximum duty cycle and circuit voltage drops. The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{INMIN} = \frac{V_{OUT} + (I_{OUT} \times (R_{DCR} + 0.6))}{D_{MAX}} + (I_{OUT} \times 1.15)$$

$$V_{INMAX} = \frac{V_{OUT}}{t_{ONMIN} \times f_{SW}}$$

where V_{OUT} is the steady-state output voltage, I_{OUT} is the maximum load current, R_{DCR} is the DC resistance of the inductor, f_{SW} is the switching frequency (max), D_{MAX} is the maximum duty cycle, and t_{ONMIN} is the worst-case minimum controllable switch on-time (130ns).

Overcurrent Protection/Hiccup Mode

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit of 0.62A (typ). A runaway current limit on the high-side switch current at 0.75A (typ) protects the device under high input voltage, and short-circuit conditions when there is insufficient output voltage available to restore the inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if, due to a fault condition, the output voltage drops to 65% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 131ms. Once the hiccup timeout period expires, a soft-start is attempted again. The hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

Care should be taken in board layout and system wiring to prevent violation of the absolute maximum rating of the FB/V_{OUT} pin under short-circuit conditions. Under such conditions, it is possible for the ceramic output capacitor to oscillate with the board or wiring inductance between the output capacitor or short-circuited load, thereby causing the absolute maximum rating of FB/V_{OUT} (-0.3V) to be exceeded. The parasitic board or wiring inductance should be minimized, and the output voltage waveform under short-circuit operation should be verified to ensure the absolute maximum rating of FB/V_{OUT} is not exceeded.

Thermal Overload Protection

Thermal overload protection limits the total power dissipation in the device. When the junction temperature exceeds +166°C, an on-chip thermal sensor shuts down the device and turns off the internal power MOSFETs, allowing the device to cool down. The thermal sensor turns the device on after the junction temperature cools by 10°C.

APPLICATIONS INFORMATION

Inductor Selection

A low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions should be selected. The saturation current (I_{SAT}) must be high enough to ensure that saturation cannot occur below the maximum current-limit value. The required inductance for a given application can be determined from the following equation:

$$L = 13 \times V_{OUT}$$

where L is inductance in µH and V_{OUT} is output voltage. Once the L value is known, the next step is to select the right core material. Ferrite and powdered iron are commonly available core materials. Ferrite cores have low core losses and are preferred for high-efficiency designs. Powdered iron cores have more core losses and are relatively cheaper than ferrite cores. See *Table 4* to select the inductors for typical applications.

Table 4. Inductor Selection

INPUT VOLTAGE RANGE V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	L (µH)	RECOMMENDED PART NUMBER
5 to 48	3.3 (Fixed)	400	47	Wurth 74404054470
7 to 60	5 (Fixed)	400	68	Wurth 74404054680
4.5 to 24	1.8	400	22	Coilcraft LPS4018-223MR
4.5 to 36	2.5	400	33	Coilcraft LPS4018-333MR
15 to 60	12	400	150	Wurth 74404054151
18.5 to 60	15	400	150	Wurth 74404054151

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT}$), so $I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = I_{OUT(MAX)} \times D \times \frac{(1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where $D = V_{OUT}/V_{IN}$ is the duty ratio of the converter, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide the necessary damping for potential oscillations caused by the inductance of the longer input power path and the input ceramic capacitor.

Output Capacitor

Small ceramic X7R-grade capacitors are sufficient and recommended for the device. The output capacitor has two functions. It filters the square wave generated by the device along with the output inductor. It stores sufficient energy to support the output voltage under load transient conditions and stabilizes the device's internal control loop. Usually, the output capacitor is sized to support a step load of 50% of the maximum output current in the application, such that the output-voltage deviation is less than 3%. The required output capacitance can be calculated from the following equation:

$$C_{OUT} = \frac{60}{V_{OUT}}$$

where C_{OUT} is the output capacitance in µF and V_{OUT} is the output voltage in V. The derating of ceramic capacitors with DC-voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors. See *Table 5* to select the output capacitor for typical applications.

Table 5. Output Capacitor Selection

INPUT VOLTAGE RANGE V_{IN} (V)	V_{OUT} (V)	I_{OUT} (mA)	C_{OUT} (µF)	RECOMMENDED PART NUMBER
5 to 48	3.3 (Fixed)	400	22µF/1206/X7R/6.3V	Murata GRM31CR70J226KE19
7 to 60	5 (Fixed)	400	22µF/1206/X7R/6.3V	Murata GRM31CR70J226KE19
4.5 to 24	1.8	400	47µF/1210/X7R/6.3V	Murata GRM32ER70J476KE20
4.5 to 36	2.5	400	22µF/1210/X7R/16V	Murata GRM32ER71C226KEA8
15 to 60	12	400	22µF/1210/X7R/16V	Murata GRM32ER71C226KEA8
18.5 to 60	15	400	10µF/1206/X7R/25V	Murata GRM31CR71E106KA12

Setting the Input Undervoltage-Lockout Level

The devices offer an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from V_{IN} to GND (see *Figure 58*). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.32MΩ max, and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the device is required to turn on.

If the EN/UVLO pin is driven from an external signal source, a series resistance of minimum 1kΩ is recommended to be placed between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

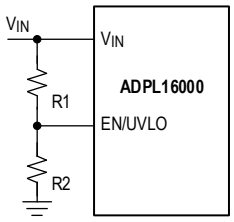


Figure 58. Adjustable EN/UVLO Network

Adjusting the Output Voltage

The ADPL16000C output voltage can be programmed from 0.9V to 0.89 x V_{IN}. Set the output voltage by connecting a resistor-divider from output to FB to GND (see *Figure 59*).

For output voltages less than 6V, choose R4 in the 50kΩ to 150kΩ range. For output voltages greater than 6V, choose R4 in the 25kΩ to 75kΩ range and calculate R3 with the following equation:

$$R3 = R4 \times \left[\frac{V_{OUT}}{0.9} - 1\right]$$

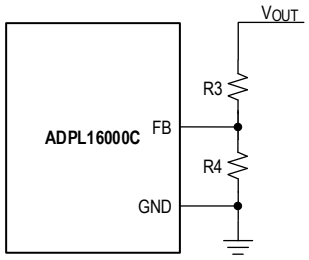


Figure 59. Setting the Output Voltage

Power Dissipation

At a particular operating condition, the power losses that lead to the temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - (I_{OUT}{}^2 \times R_{DCR})$$

$P_{OUT} = V_{OUT} \times I_{OUT}$

where P_{OUT} is the output power, η is the efficiency of power conversion, and R_{DCR} is the DC resistance of the output inductor. See the *Typical Performance Characteristics* for the power-conversion efficiency or measure the efficiency to determine the total power dissipation.

The junction temperature (T_J) of the device can be estimated at any ambient temperature (T_A) from the following equation:

$T_J = T_A + (\theta_{JA} \times P_{LOSS})$

where θ_{JA} is the junction-to-ambient thermal impedance of the package.

Junction temperatures greater than +125°C degrade operating lifetimes.

PCB Layout Guidelines

Careful PCB layout is critical to achieving clean and stable operation. The switching power stage requires particular attention. See the following guidelines for good PCB layout:

- Place the input ceramic capacitor as close as possible to the V_{IN} and GND pins.
- Connect the negative terminal of the V_{CC} bypass capacitor to the GND pin with the shortest possible trace or ground plane.
- Minimize the area formed by the LX pin and the inductor connection to reduce the radiated EMI.
- Place the V_{CC} decoupling capacitor as close as possible to the V_{CC} pin.
- Ensure that all feedback connections are short and direct.
- Route the high-speed switching node (LX) away from the FB/V_{OUT}, $\overline{\text{RESET}}$, and MODE pins.

For a sample PCB layout that ensures first-pass success, refer to the ADPL16000 evaluation kit layouts available at *www.analog.com*.

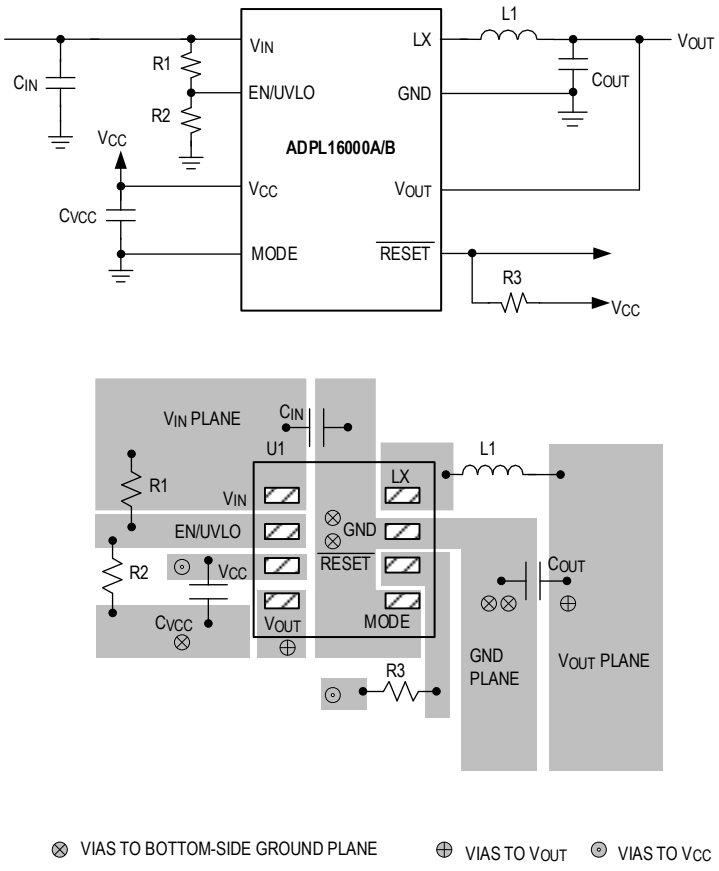


Figure 60. Layout Guidelines for ADPL16000A and ADPL16000B

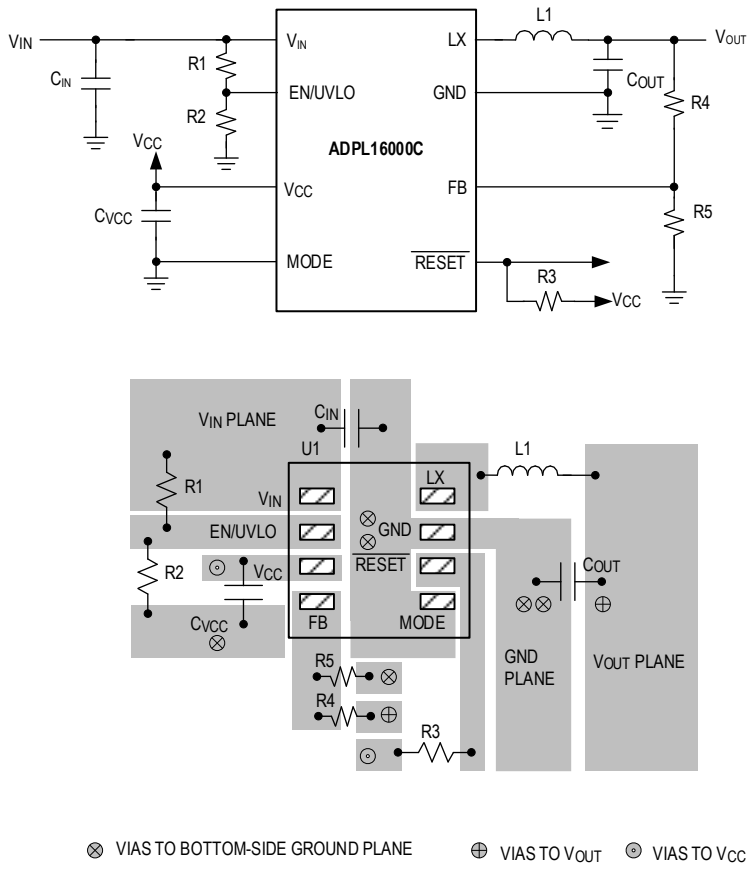


Figure 61. Layout Guidelines for ADPL16000C

TYPICAL APPLICATION CIRCUITS

3.3V, 400mA Step-Down Regulator

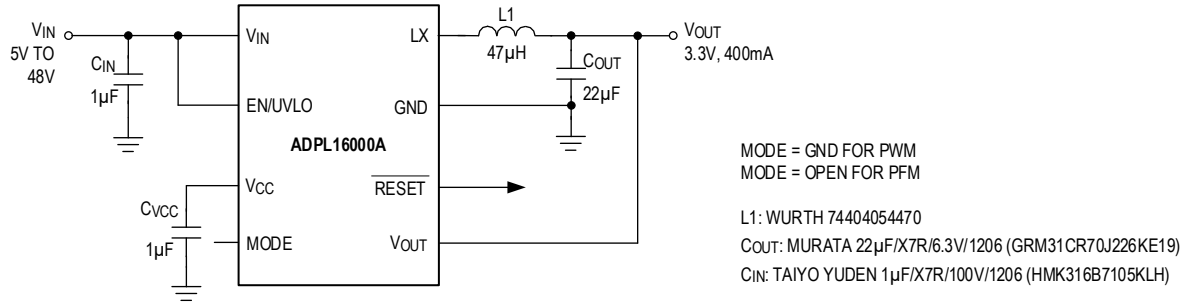


Figure 62. 3.3V, 400mA Step-Down Regulator

5V, 400mA Step-Down Regulator

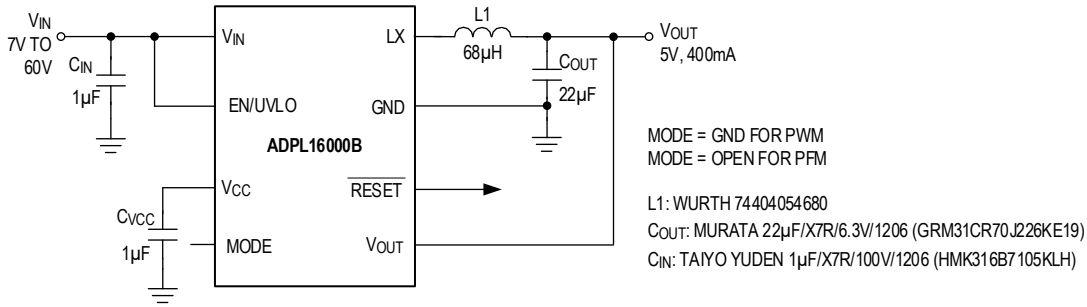


Figure 63. 5V, 400mA Step-Down Regulator

2.5V, 400mA Step-Down Regulator

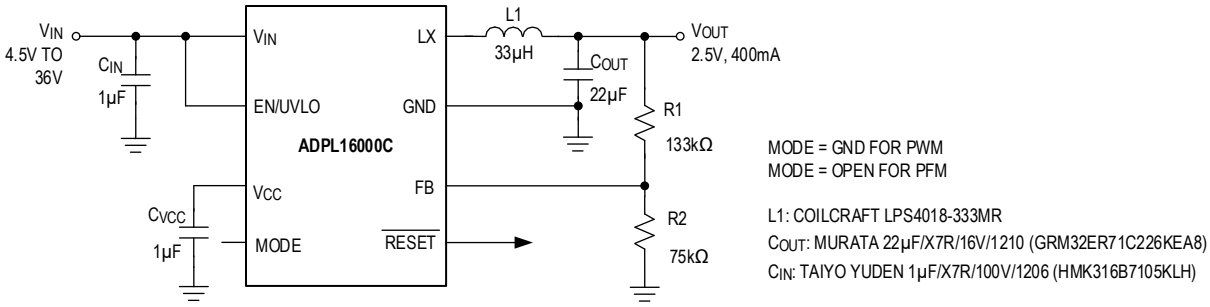


Figure 64. 2.5V, 400mA Step-Down Regulator

12V, 400mA Step-Down Regulator

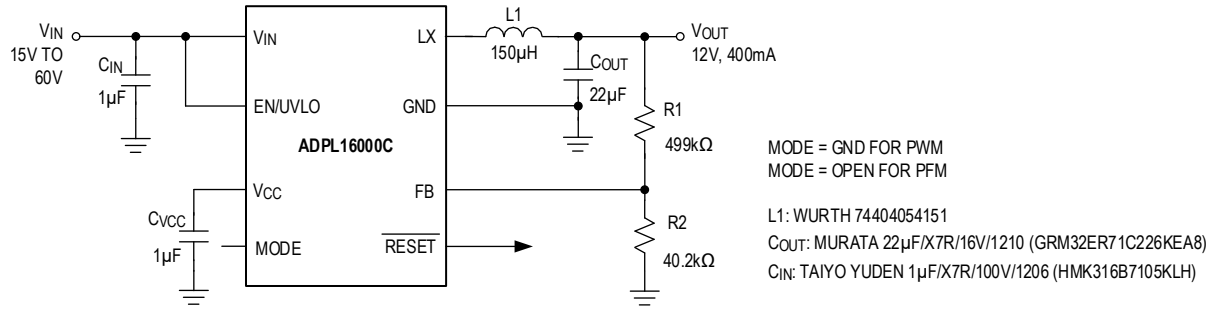


Figure 65. 12V, 400mA Step-Down Regulator

1.8V, 400mA Step-Down Regulator

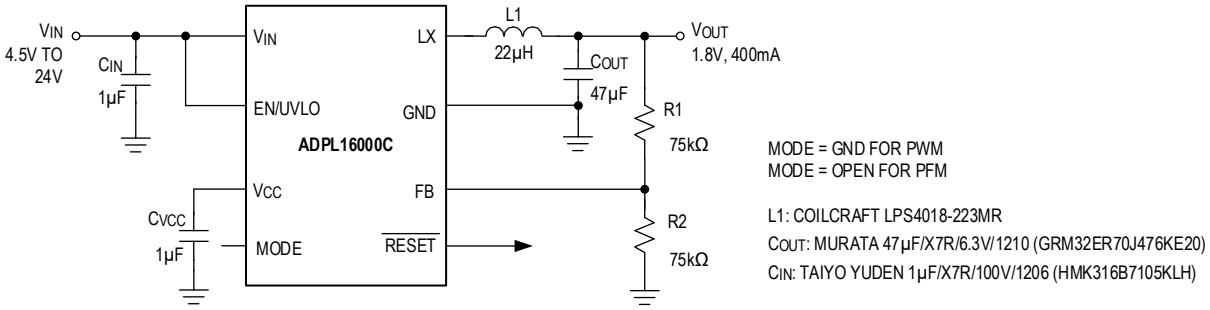


Figure 66. 1.8V, 400mA Step-Down Regulator

15V, 400mA Step-Down Regulator

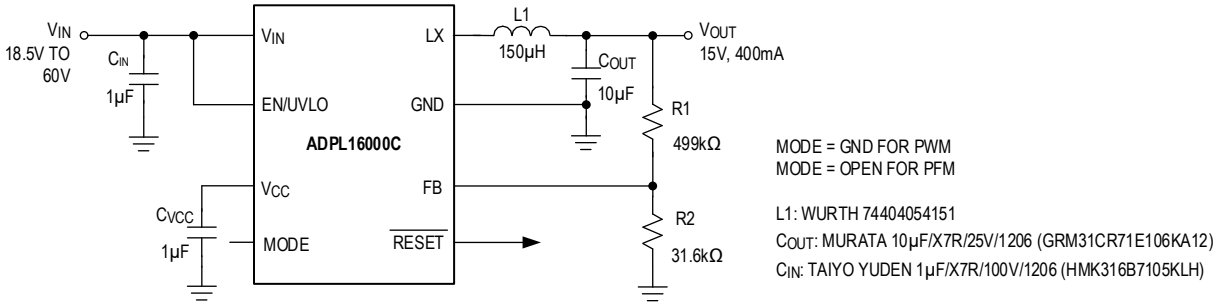
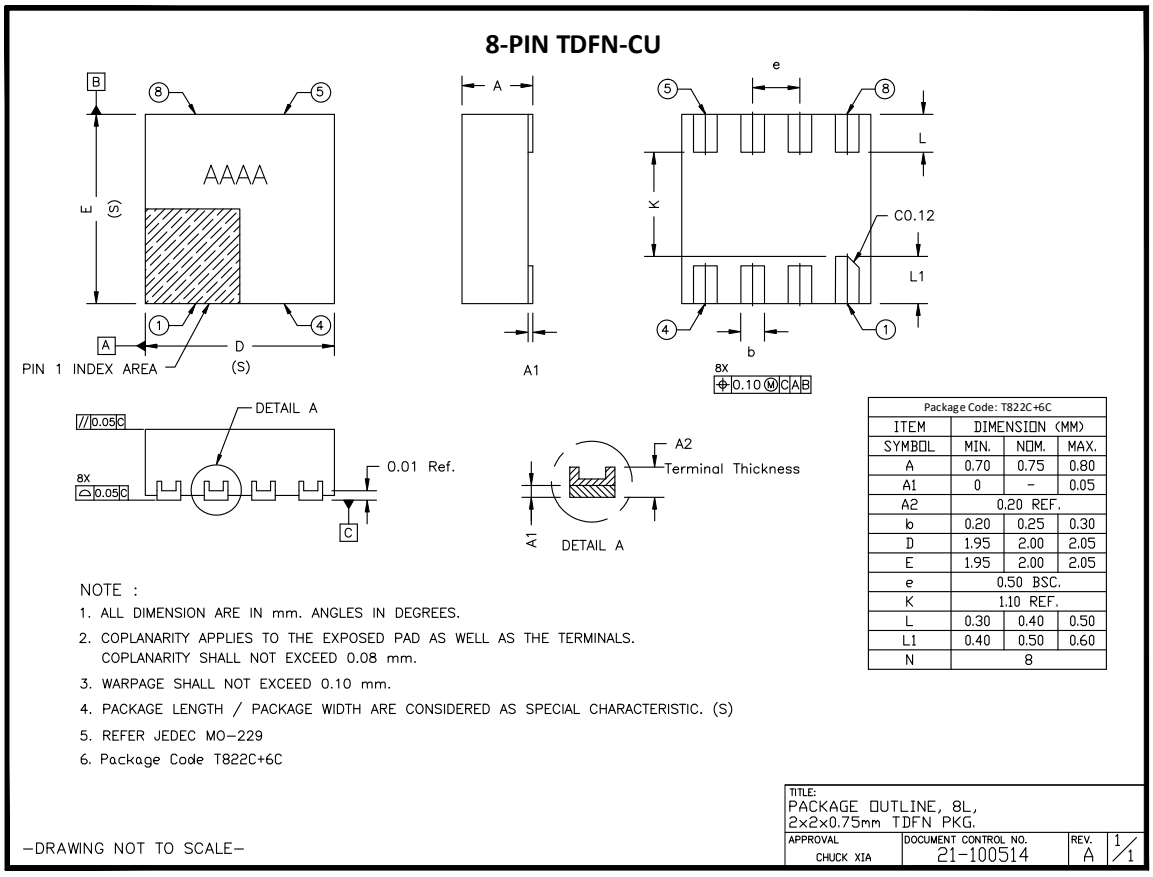


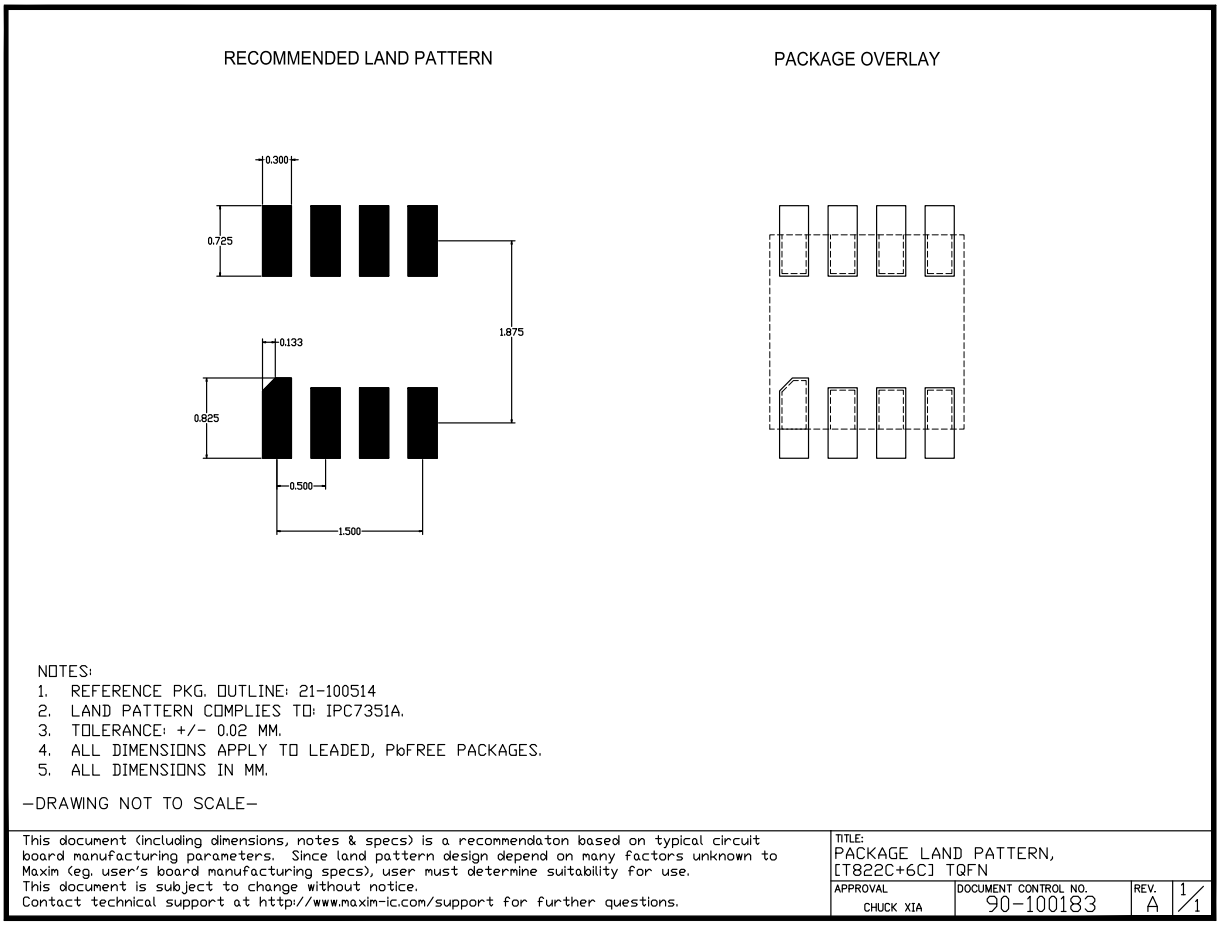
Figure 67. 15V, 400mA Step-Down Regulator

OUTLINE DIMENSIONS



Package Code: T822C+6C			
ITEM	DIMENSION (MM)		
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0	-	0.05
A2	0.20 REF.		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	0.50 BSC.		
K	1.10 REF.		
L	0.30	0.40	0.50
L1	0.40	0.50	0.60
N	8		

LAND PATTERN



Refer to **https://www.analog.com/en/design-center/packaging-quality-symbols-footprints.html** for the most recent package drawings.

Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Thermal Resistance, Four-Layer Board (*Note 2*)	
Junction-to-Ambient (θ_{JA})	162°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	20°C/W

Note 2: Package thermal resistances were obtained using the ADPL16000 Evaluation Kit with no airflow.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **https://www.analog.com/en/technical-articles/thermal-characterization-of-ic-packages.html**.

ORDERING GUIDE

PART NUMBER	TEMP RANGE	PIN-PACKAGE	V_{OUT}
ADPL16000AATA+	-40°C to +125°C	8 TDFN-CU	3.3V
ADPL16000AATA+T	-40°C to +125°C	8 TDFN-CU	3.3V
ADPL16000BATA+	-40°C to +125°C	8 TDFN-CU	5V
ADPL16000BATA+T	-40°C to +125°C	8 TDFN-CU	5V
ADPL16000CATA+	-40°C to +125°C	8 TDFN-CU	Adj
ADPL16000CATA+T	-40°C to +125°C	8 TDFN-CU	Adj

+Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADPL16000CATA+T ADPL16000BATA+T ADPL16000AATA+T