110V High Voltage, 1A High Current, Operational Amplifier

FEATURES

- Wide high voltage supply range: ±12V to ±55V
- Low quiescent current: 12mA
- High output capability
  - Output voltage range: Up to ±52V for I_{OUT} = ±100 mA
  - High output current drive: ±1A continuous
  - High slew rate: ±1300V/µs into 1nF load
- Extensive configurability
  - Unlimited capacitive loads stability with external compensation and output slew limiting
  - Stable for any gain and adjustable slew rate with external transconductance R_{SLEW}
  - Programmable supply current with shutdown mode
- Fault protection and monitoring
  - Digitally programmable current, voltage, and thermal shutdown limits
- Design-in friendly
  - Package: 80-pin, 12mm × 12mm TQFP
    - EPAD-up package for mountable heatsink
- Operating temperature range: −40°C to +85°C

APPLICATIONS

- High voltage power amplifier (PA)
- High voltage SMU/VI source
- High voltage arbitrary waveform generator (AWG)
- Piezoelectric transducer drive
- Programmable power supplies

GENERAL DESCRIPTION

The ADHV4710 is a high voltage, high power, high speed operational amplifier optimized for driving up to ±1A at ±1300V/µs into capacitive and resistive loads. Combining a high voltage amplifier with low voltage analog circuitry and an SPI programmable digital engine, the ADHV4710 is ideally suited for high voltage applications such as automated test equipment (ATE), programmable power supplies, and piezo drive.

The ADHV4710 has extensive configurability for high voltage signal chains. The amplifier achieves high slew rate and bandwidth at high gain but can alternatively be configured in low gain for high voltage input and output. External transconductance resistor R_{SLEW} enables stability under any gain and adjustable slew rate. External compensation capacitor C_{COMP} enables the amplifier output to stably drive unlimited capacitive loads.

A proprietary high voltage BCDMOS process, novel high voltage architecture, and thermally enhanced package from Analog Devices Inc. enable this high-performance amplifier. Fault protection and monitoring are programmable using SPI. Additional analog features extend functionality: junction temperature sensor voltage output and adjustable shutdown delay. The ADHV4710 operates on high voltage dual supplies up to ±55V, asymmetrical dual supplies, or a single supply of 110V.

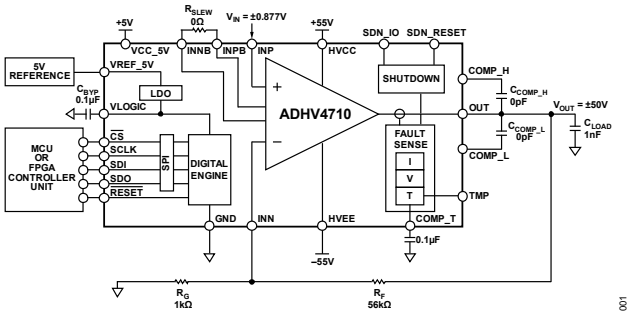

Figure 1. Simplified Functional Block Diagram

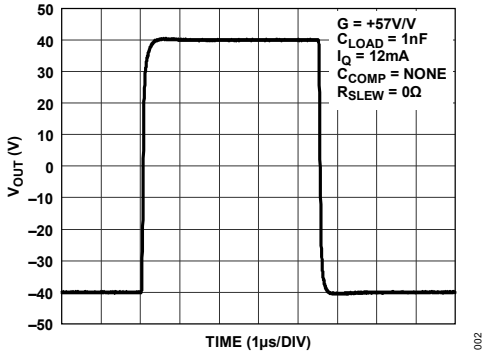

Figure 2. Large Signal Pulse Response

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FUNCTIONAL BLOCK DIAGRAM

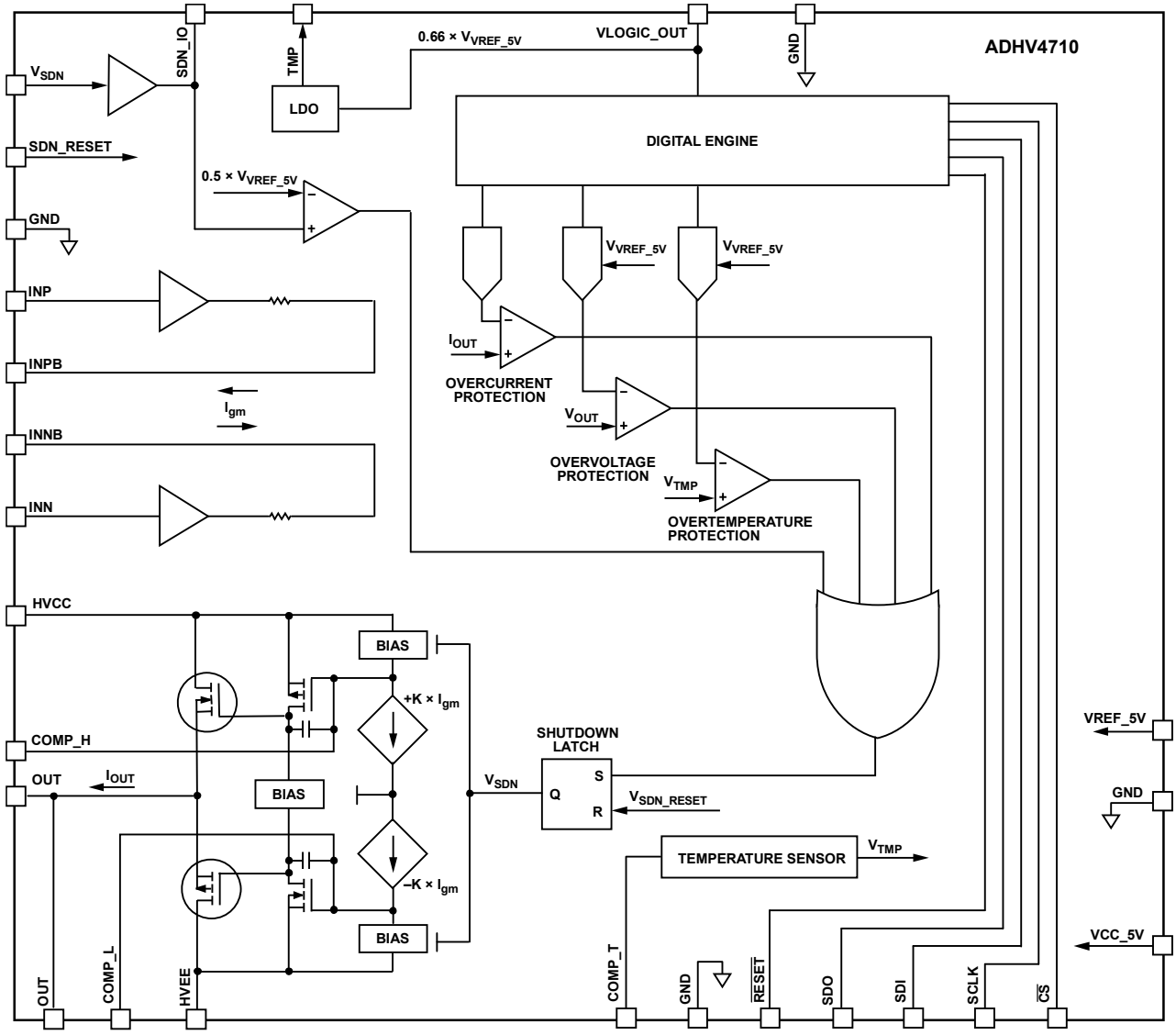

Figure 3. Functional Block Diagram

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REVISION HISTORY

03/2025 – Rev. 1

SPECIFICATIONS

Table 1. Electrical Characteristics

(HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE						
Small Signal Bandwidth	f_{-3db}	V_{OUT} = 0.1Vp-p		2.5		MHz
Large Signal Bandwidth [1]		V_{OUT} = 80Vp-p		2.3		MHz
Slew Rate, 20% to 80%	SR_{RISE}	V_{OUT} = 80Vp-p		900		V/µs
	SR_{FALL}	V_{OUT} = 80Vp-p		1000		V/µs
	SR_{RISE}	V_{OUT} = 80Vp-p, SET_IQ = 0x91 (I_{HVCC}/I_{HVEE} ≈ 22.5 mA), G = 45		1300		V/µs
	SR_{FALL}	V_{OUT} = 80Vp-p, SET_IQ = 0x91 (I_{HVCC}/I_{HVEE} ≈ 22.5 mA), G = 45		1500		V/µs
Output 1% Settling Time	t_{ST}	V_{OUT} = 80Vp-p		430		ns
Output 0.1% Settling Time	t_{ST}	V_{OUT} = 80Vp-p		1200		ns
NOISE/DISTORTION PERFORMANCE						
Voltage Noise Spectral Density, RTI	V_N	C_{LOAD} = 0nF, f = 100kHz		26		nV/√Hz
Current Noise Spectral Density, RTI	I_N	f = 40Hz, simulation		1		fA/√Hz
Total Harmonic Distortion	THD	V_{OUT} = 80Vp-p, 1kHz		-92		dB
		V_{OUT} = 80Vp-p, 10kHz		-73		dB
DC PERFORMANCE						
Offset Error, RTI	V_{OS}			13	550	µV
	V_{OS_TC}	T_J = 30°C to 85°C. See *Figure 58*.		5		µV/°C
Input Bias Current [6]					50	pA
Input Bias Current Drift		T_J = 30°C to 85°C		0.22		pA/°C
Input Offset Current [6]					100	pA
Input Offset Current Drift		T_J = 30°C to 85°C		0.44		pA/°C
Open-Loop Gain	A_{OL}	HVCC/HVEE = ±55V		127		dB

(HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
		HVCC/HVEE = ±12V		120		dB
INPUT CHARACTERISTICS						
Common-Mode Input Impedance	R_{INCM}	V_{CM} = HVEE + 6V to HVCC − 6V		13.5		TΩ
	C_{INCM}			4.4		pF
Differential Input Impedance	R_{INDM}			3.3		TΩ
	C_{INDM}			1.3		pF
Input Common-Mode Voltage Range	V_{CM}	HVCC/HVEE = ±55V		±49V		V
Common-Mode Rejection Ratio	CMRR	HVCC/HVEE = ±37.5V, V_{CM} = HVEE + 6V to HVCC − 6 V, VCC_5V = 5.5 V	114	133		dB
OUTPUT CHARACTERISTICS						
Output Voltage Range	V_{OUT}	I_{OUT} = 100mA, HVCC/HVEE = ±55V	HVEE + 2.5		HVCC − 2	V
		I_{OUT} = 1A, HVCC/HVEE = ±20V	HVEE + 9.5		HVCC − 5	V
Output Voltage Range [6]	V_{OUT}	I_{OUT} = 1A, HVCC/HVEE = ±20V, T_J = 30°C to 105°C	HVEE + 13.2		HVCC − 6	V
Continuous Output Current [2]	I_{OUT}			1		A
Peak Instantaneous Output Current Drive [3]	IOUT_PEAK			1.2		A
Closed-Loop Output Impedance	Z_{OUT}	f = 10kHz		0.13		Ω
Open-Loop Output Impedance	Z_O	f = 100kHz		12.8		Ω
Output Resistance During Shutdown	Z_{O_SDN}			110		kΩ
REFERENCE INPUT						
Input Range [4]	VREF_5V	See *Absolute Maximum Ratings* relative to VCC_5V.	4.75	5	VCC_5V + 0.1	V
Input Resistance	VREF_5V			32		kΩ

(HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
SDN_IO SPECIFICATIONS						
Output Voltage Range	SDN_IO	SDN_IO Floating	0		VCC_5V	V
Shutdown Threshold	SDN_IO_{RISING}		2.54	2.56	2.57	V
	$SDN\_IO_{FALLING}$		2.45	2.47	2.48	V
Output Current Drive Sink	SDN_IO_{SNK}	SDN_IO = 80% of VCC_5V		−180		uA
Output Current Drive Source	SDN_IO_{SRC}	SDN_IO = 20% of VCC_5V		200		uA
Turn Off Time	SDN_IO_{TOFF}	SDN_IO > SDN_IO_{RISING} to shutdown. See *Delayed Shutdown.*		400		ns
Turn On Time	SDN_IO_{TON}	I_{OUT} = 0A. SDN_IO < $SDN\_IO_{FALLING}$ to turn on. See *Delayed Shutdown.*		2		us
		I_{OUT} = 500mA. SDN_IO < $SDN\_IO_{FALLING}$ to turn on. See *Delayed Shutdown.*		11.5		us
DC OVERCURRENT PROTECTION						
Sourcing Setpoint Range Max				1		A
Sourcing Code Range			0x06		0x40	
Sinking Setpoint Range Max				−1		A
Sinking Code Range			0x40		0x06	
Setpoint Resolution				15.625		mA/lsb
Setpoint Accuracy		Code = 0x06, 93.75mA		3.6		%
Shutdown Response Time		C_{SDN_IO} = DNI, Code = 0x32		1.6		us
DC OVERVOLTAGE PROTECTION						
Positive Voltage Setpoint Range Max				105		V
Positive Code Range			0x01		0x35	
Negative Voltage Setpoint Range Max				−55		V
Negative Code Range			0x52		0x1C	

(HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
Setpoint Resolution				1.953		V/lsb
Setpoint Accuracy		Code = 0x1A, ~50V		1.2		%
Shutdown Response Time		C_{SDN_IO} = DNI, Code = 0x1A		0.9		us
DC OVERTEMPERATURE PROTECTION						
Maximum Setpoint Range [5]				150		°C
Minimum Setpoint Range				−40		°C
Code Range			0x23		0x40	
Setpoint Resolution				6.51		°C/lsb
Setpoint Accuracy		Code = 0x40, accuracy with ideal TMP pin voltage		3.6		°C
Shutdown Response Time		C_{SDN_IO} = DNI, Code = 0x40		1		us
TEMPERATURE MONITOR SPECIFICATIONS						
Initial Voltage [6]	$TMP\_V_{INITIAL}$	T_J = 30°C	1.755	1.78	1.805	V
Scaling	TMP_T_C	T_J = 30°C to 125°C		6		mV/°C
Output Impedance Sourcing	TMP_Z			40		Ω
Output Current Sinking	TMP_Z			−100		µA
DIGITAL INPUTS (SCLK, SDI, $\overline{CS}$, $\overline{RESET}$) [6, 7]						
Input High Voltage	VIH_{SPI}		2.5		VCC_5V	V
Input Low Voltage	VIL_{SPI}		0		0.8	V
Input Current	I_{L_SPI}		−1		1	µA
Input Capacitance	C_{SPI}			5		pF
$\overline{RESET}$ Minimum Duration				10		ns
SDN_RESET INPUT [6, 7]						
Input High Voltage	VIH_{SDN_RESET}		2.5		VCC_5V	V
Input Low Voltage	VIL_{SDN_RESET}		0		0.8	V
Input Current	$I_{L\_SDN\_RESET}$		−10		10	µA
Input Capacitance	C_{SDN_RESET}			5		pF

(HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (SDO) [6, 7]						
Output High Voltage	VOH_{SDO}		2.68		3	V
Output Low Voltage	VOL_{SDO}		0		0.4	V
High Impedance Input Current	I_{L_SDO}		−2		2	µA
Output Capacitance	C_{SDO}			5		pF
VLOGIC_OUT						
Output Voltage Range	VLOGIC_OUT	I_{VLOGIC_OUT} = 300µA, VREF_5V = 5V	2.95	3	3.05	V
Load Regulation		I_{VLOGIC_OUT} ≤ 50mA		2		mV/mA
Output Current Drive				50		mA
POWER SUPPLIES						
Operation Range	HVCC to HVEE		24		110	V
	HVCC to GND		12		105	V
	HVEE to GND		−55		0	V
	VCC_5V		4.7	5	5.5	V
Quiescent Current (Enabled)	I_{HVCC}	HVCC/HVEE = ±55V, VCC_5V = 5.5V, VREF_5V = 5.6V. See *Programmable Quiescent Current*.		12	14.5	mA
	I_{HVEE}	HVCC/HVEE = ±55V, VCC_5V = 5.5V, VREF_5V = 5.6V. See *Programmable Quiescent Current*.	−14.5	−12		mA
Quiescent Current (Enabled)	I_{VCC_5V}	HVCC/HVEE = ±55V, VCC_5V = 5.5V, VREF_5V = 5.6V		6	10	mA
Quiescent Current (Shutdown)	I_{HVCC}	HVCC/HVEE = ±55V, VCC_5V = 5.5V, VREF_5V = 5.6V		120	160	µA
	I_{HVEE}	HVCC/HVEE = ±55V, VCC_5V = 5.5V, VREF_5V = 5.6V	−160	−120		µA
Quiescent Current (Shutdown) [8]	I_{VCC_5V}	HVCC/HVEE = ±55V, VCC_5V = 5.5V, VREF_5V = 5.6V		5	10	mA
Power Supply Rejection Ratio	$PSRR_{HVCC}$	HVCC = 50V to 55V, HVEE = −52.5V		111		dB
	$PSRR_{HVEE}$	HVCC = 52.5 V, HVEE = −50V to −55V		115		dB

(HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
	$PSRR_{HV}$	HVCC/HVEE, ±55V to ±12V	115	123		dB
		HVCC/HVEE, ±14V to ±12V		112		dB
	$PSRR_{VCC\_5V}$	VCC_5V = 4.7V to 5.5V		98		dB

1 Large signal bandwidth may be limited by thermal design. See the *Thermal Management* section.

2 See the *Thermal Management* section for more details.

3 The ADHV4710 has been lifetime tested with a 1nF load, driven with an 80Vp-p square wave at 1kHz.

4 See the *VREF_5V* section for details on the effects of supply variations on this pin.

5 The absolute maximum junction temperature is 150°C.

6 Guaranteed by design and characterization, not production tested.

7 T_J = 30°C to 105°C

8 This specification is when the overcurrent protection is armed. When the overcurrent protection is disarmed and the ADHV4710 is in shutdown, VCC_5V may consume an additional 2mA current.

Table 2. Timing Characteristics

(VCC_5V = +5V, VREF_5V = +5V, T_J = 30°C to 105°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS	MIN	TYP	MAX	UNITS
SPI TIMING[1]						
SCLK Frequency	f_{SCLK}				19	MHz
Pulse Width High	t_{HI}		20			ns
Pulse Width Low	t_{LO}		20			ns
Setup $\overline{CS}$ to SCLK Edge	t_{S_SPI}		5			ns
Hold SCLK to $\overline{CS}$ High	t_{H_SPI}		5			ns
Setup Time SDI to SCLK High	t_{DS}		5			ns
SDI Hold Time from SCLK High	t_{DH}		5			ns
Data Valid SCLK to SDO	t_{ACCESS}				20	ns
SDO Data Release	t_Z				20	ns

1 Guaranteed by design and characterization, not production tested.

Timing Diagrams

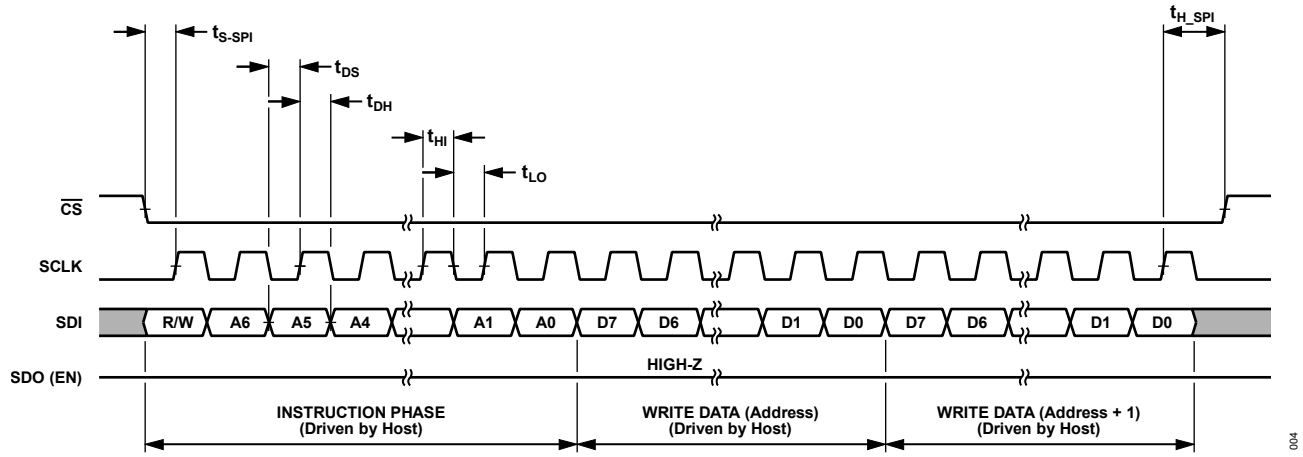

Figure 4. SPI Timing Diagram (Write Operation)

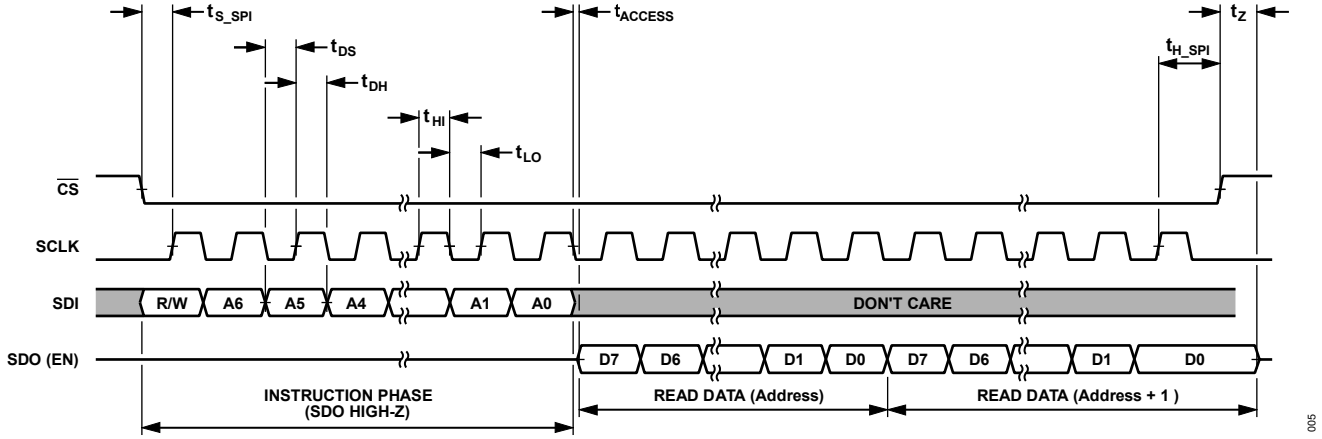

Figure 5. SPI Timing Diagram (Read Operation)

ABSOLUTE MAXIMUM RATINGS

T_A = 25 °C, unless otherwise specified.

Table 3. Absolute Maximum Ratings

PARAMETER	RATING
HVCC to HVEE	115V
HVCC to GND	107.5V
HVEE to GND	−57.5V
INP, INN	HVEE − 0.3V to HVCC + 0.3V
INPB to INP	−1.2V to +1.2V
INNB to INN	−1.2V to +1.2V
OUT	HVEE − 0.3V to HVCC + 0.3V
COMP_H	HVCC – 5V to HVCC + 0.3V
COMP_L	HVEE − 0.3V to HVEE + 5V
VCC_5V to GND	−0.3V to +6V
VREF_5V to GND	−0.3V to VCC_5V + 0.3V
VLOGIC_OUT to GND	−0.3V to VCC_5V + 0.3V
SCLK, $\overline{CS}$, SDI, SDO, $\overline{RESET}$, SDN_IO, SDN_RESET to GND	−0.3V to VCC_5V + 0.3V
TMP, COMP_T to GND	−0.3V to VCC_5V + 0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range (T_A)[1]	−40°C to +85°C
Junction Temperature (T_J)[2]	+150°C
Peak Solder Reflow Temperature[3]	IPC/JEDEC J-STD-020

1 Subject to $T_J \leq 150$ °C

2 Extended operation of T_J at or near the absolute maximum junction temperature rating accelerates device aging. Ensure proper thermal management.

3 RoHS-compliant assemblies (20 sec to 40 sec)

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required. To keep the junction temperature (T_J) below the absolute maximum rating, it is typically required to incorporate thermal management techniques. See the *Thermal Management* section for more details.

θ_{JA} is the natural convection, junction-to-ambient thermal resistance. θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}[2]	θ_{JC}[3]	θ_{JC}[2]	Unit
80-Lead TQFP (SV-80-7)	39.5	1.1	2.3	°C/W

[1] Thermal impedance simulated values based on JEDEC JESD-51. For θ_{JA} with heatsink and airflow, see the *Thermal Management* section.

[2] Includes derating across the die.

[3] Equal power dissipation across the die.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human body model (HBM) per ANSI/ESDA/JEDEC JS-001. Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

Table 5. ADHV4710 80-Lead TQFP

ESD Model	Withstand Threshold (V)	Class
HBM	± 1000	1C
FICDM	± 1000	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin Configuration and Function Descriptions

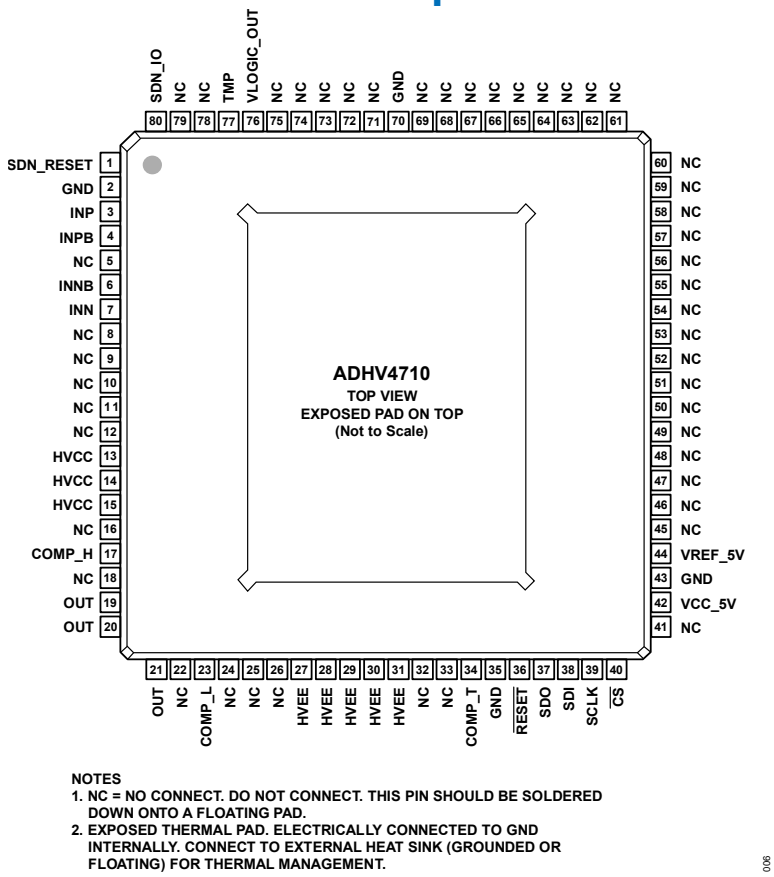

Figure 6. Top View with Pin 1 in Upper Left and Pin Numbers Ascending Anticlockwise

Table 6. Pin Function Descriptions

PIN	NAME	DESCRIPTION
1	SDN_RESET	Shutdown reset input (active high)
2	GND	Ground (analog and digital)
3	INP	Amplifier noninverting input
4	INPB	Buffered output of amplifier noninverting input. Requires external transconductance resistor R_{SLEW} from INPB to INNB.
5	NC	Do not connect. This pin should be soldered down onto a floating pad.
6	INNB	Buffered output of amplifier inverting input. Requires external transconductance resistor R_{SLEW} from INPB to INNB.
7	INN	Amplifier inverting input
8 to 12	NC	Do not connect. This pin should be soldered down onto a floating pad.
13 to 15	HVCC	High voltage positive power supply
16	NC	Do not connect. This pin should be soldered down onto a floating pad.

17	COMP_H	High-side compensation. Depending on capacitive load drive requirements, this may be left floating or connected to OUT through a capacitor. See the *Amplifier Theory* section for more details.
18	NC	Do not connect. This pin should be soldered down onto a floating pad.
19 to 21	OUT	High voltage analog output
22	NC	Do not connect. This pin should be soldered down onto a floating pad.
23	COMP_L	Low-side compensation. Depending on capacitive load drive requirements, this may be left floating or connected to OUT through a capacitor. See the *Amplifier Theory* section for more details.
24 to 26	NC	Do not connect. These pins should be soldered down onto a floating pad.
27 to 31	HVEE	High voltage negative power supply
32 to 33	NC	Do not connect. These pins should be soldered down onto a floating pad.
34	COMP_T	Thermal monitor compensation. Connect a 0.1µF capacitor to GND.
35	GND	Ground (analog and digital)
36	$\overline{\text{RESET}}$	Digital reset (active low)
37	SDO	SPI serial data output
38	SDI	SPI serial data input
39	SCLK	SPI serial clock input
40	$\overline{\text{CS}}$	SPI chip select input (active low)
41	NC	Do not connect. These pins should be soldered down onto a floating pad.
42	VCC_5V	Low voltage power supply (5V)
43	GND	Ground (analog and digital)
44	VREF_5V	Reference voltage for analog low voltage and protection threshold DACs. Connect VREF_5V to an external 5V reference or VCC_5V (reduced accuracy). See the *VREF_5V* section for more details on power sequencing.
45 to 69	NC	Do not connect. This pin should be soldered down onto a floating pad.
70	GND	Ground (analog and digital)
71 to 75	NC	Do not connect. This pin should be soldered down onto a floating pad.
76	VLOGIC_OUT	Reference voltage for logic level of SPI input. Output of internal LDO proportional to VREF_5V. 3V output for VREF_5V = 5V. Requires 0.1µF capacitor to GND.
77	TMP	Junction temperature monitor output voltage
78 to 79	NC	Do not connect. This pin should be soldered down onto a floating pad.
80	SDN_IO	Shutdown input/output (shutdown active high). Connect capacitor to GND for shutdown delay.
	EPAD	Exposed thermal pad. Electrically connected to GND internally. Connect to external heat sink (grounded or floating) for thermal management.

TYPICAL PERFORMANCE CHARACTERISTICS

HVCC/HVEE = ±50V, SET_IQ = 0x00, VCC_5V = +5V, VREF_5V = +5V, COMP_L, COMP_H = none, R_{SLEW} = 0Ω, gain (A_V) = 57, feedback resistor (R_F) = 56kΩ, noninverting configuration, C_{LOAD} = 1nF, T_C = 30°C, unless otherwise noted.

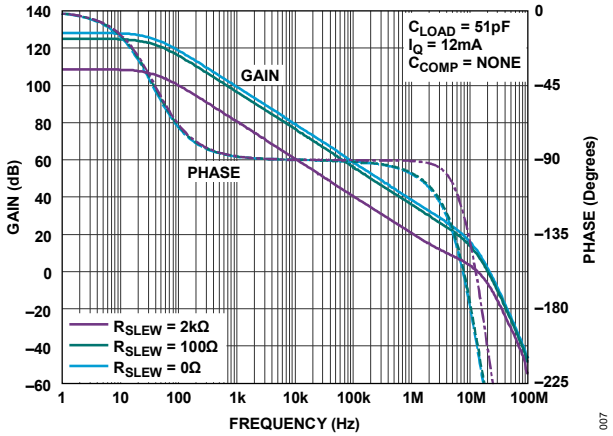

Figure 7. A_{OL} and Phase Margin vs. Frequency, Various R_{SLEW}

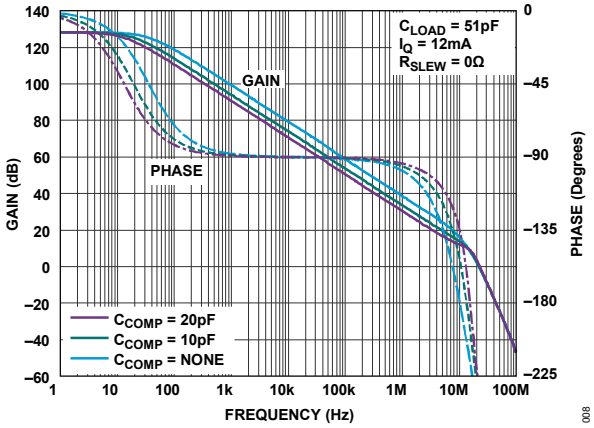

Figure 8. A_{OL} and Phase Margin vs. Frequency, Various C_{COMP}

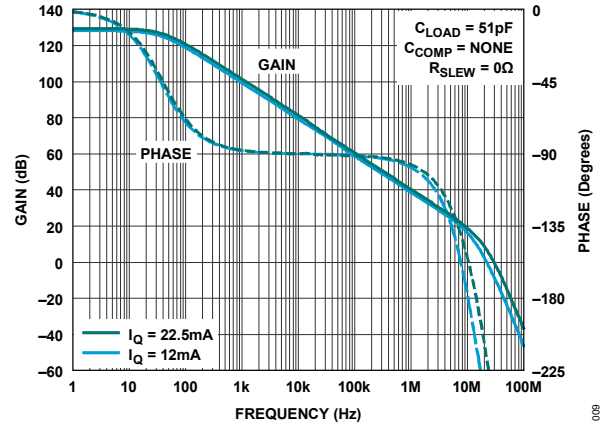

Figure 9. A_{OL} and Phase Margin vs. Frequency, Various I_Q

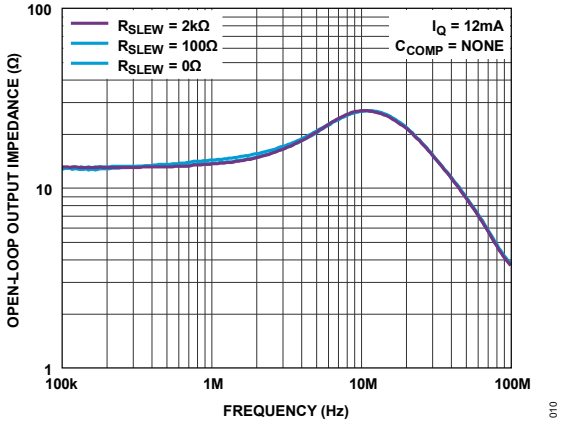

Figure 10. Open-Loop Output Impedance (Z_O) vs. Frequency, Various R_{SLEW}, Enabled

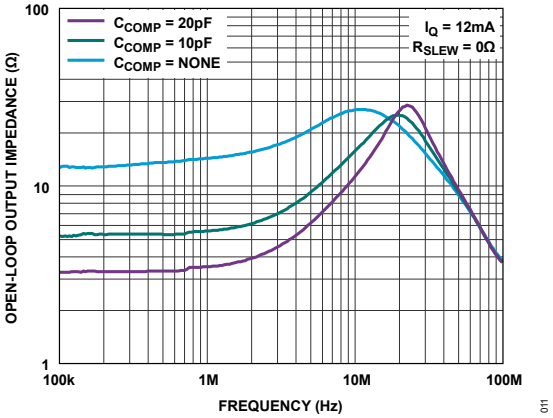

Figure 11. Open-Loop Output Impedance (Z_O) vs. Frequency, Various C_{COMP}, Enabled

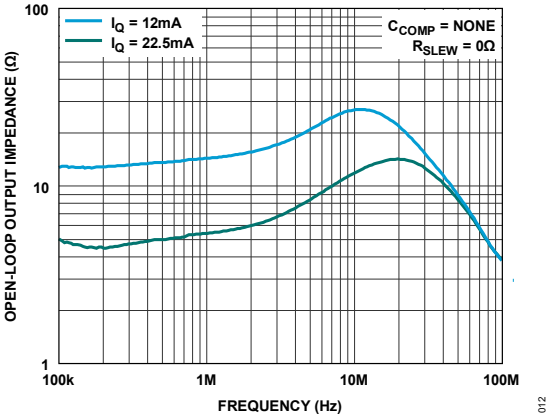

Figure 12. Open-Loop Output Impedance (Z_O) vs. Frequency, Various I_Q, Enabled

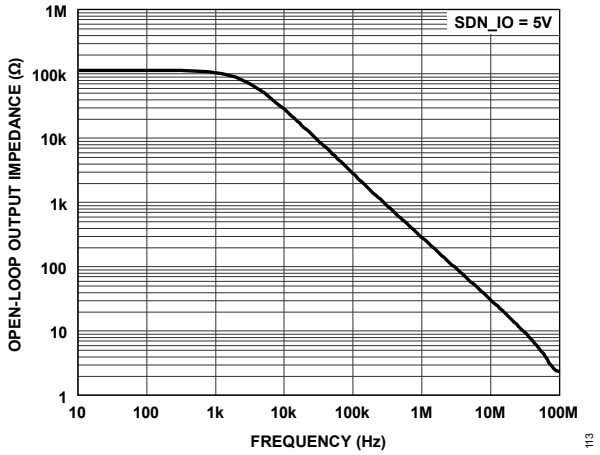

Figure 13. Open-Loop Impedance (Z_O) vs. Frequency, Shutdown

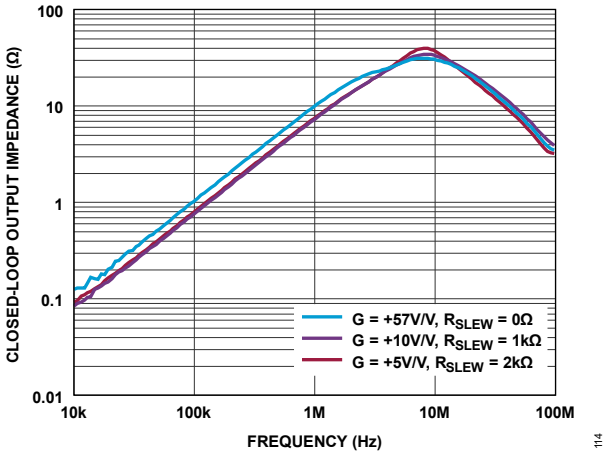

Figure 14. Closed-Loop Output Impedance (Z_{OUT}) vs. Frequency, Various Gain, Enabled

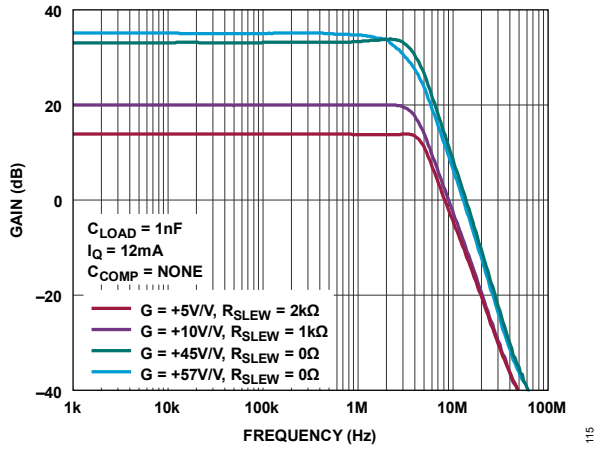

Figure 15. Small Signal Frequency Response, Various Gain

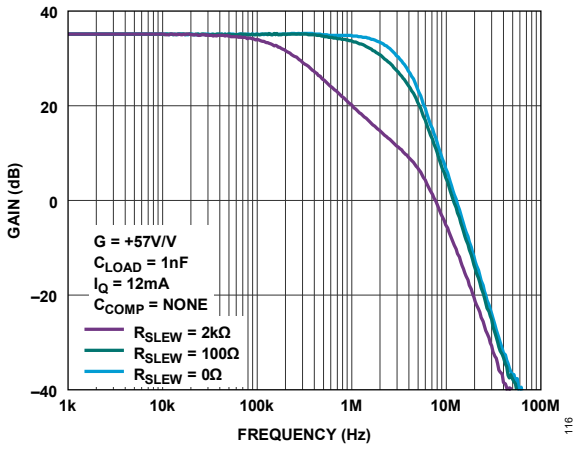

Figure 16. Small Signal Frequency Response, Various R_{SLEW}

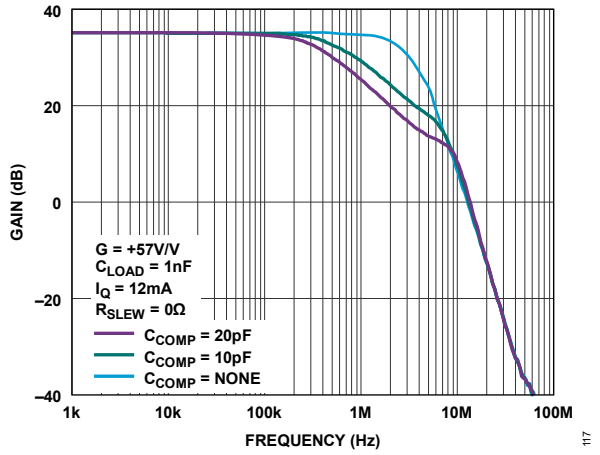

Figure 17. Small Signal Frequency Response, Various C_{COMP}

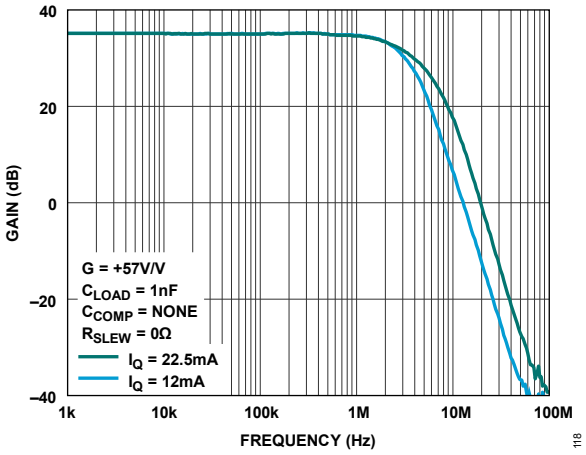

Figure 18. Small Signal Frequency Response, Various I_Q

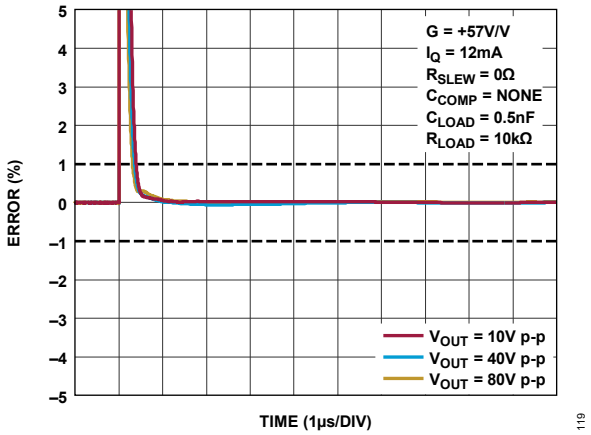

Figure 19. Settling Time 1% vs. Amplitude, Rising Edge

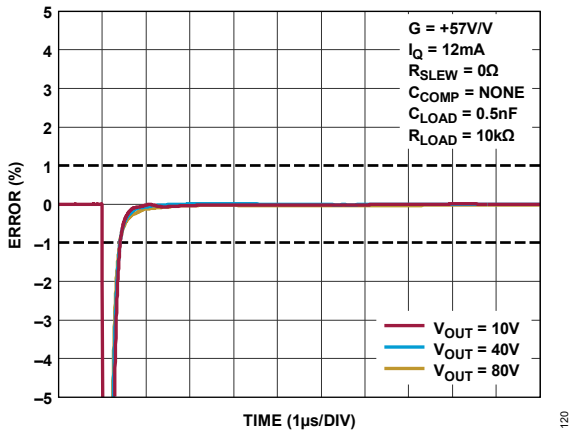

Figure 20. Settling Time 1% vs. Amplitude, Falling Edge

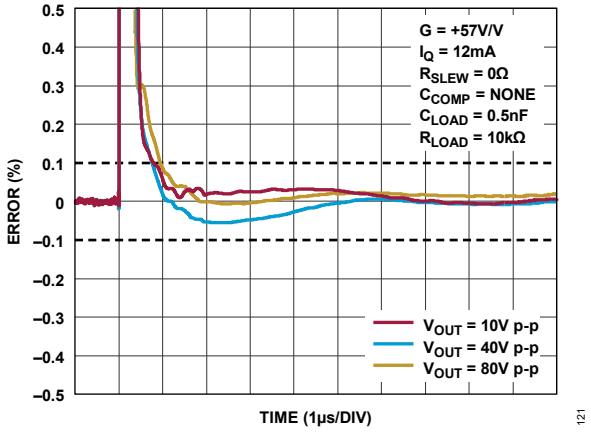

Figure 21. Settling Time 0.1% vs. Amplitude, Rising Edge

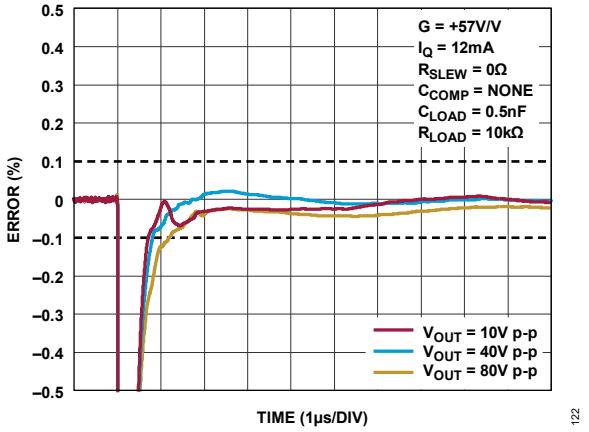

Figure 22. Settling Time 0.1% vs. Amplitude, Falling Edge

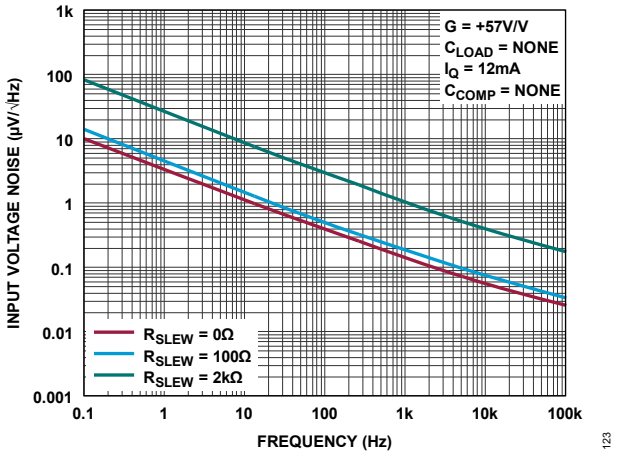

Figure 23. Input Voltage Noise vs. Frequency, Various R_{SLEW}

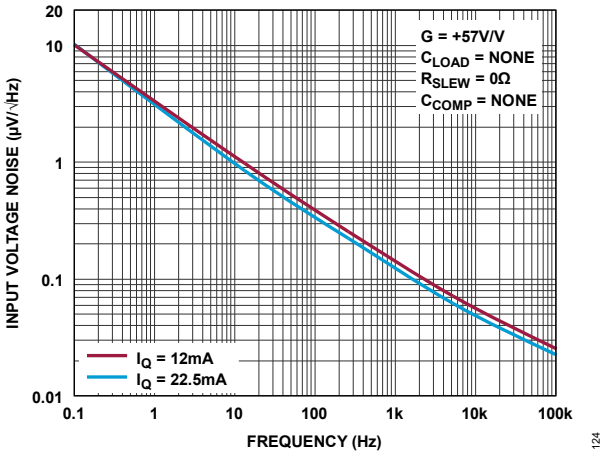

Figure 24. Input Voltage Noise vs. Frequency, Various I_Q

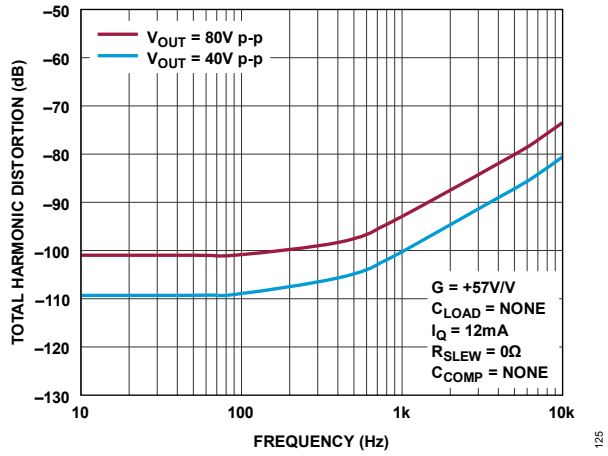

Figure 25. THD vs. Frequency

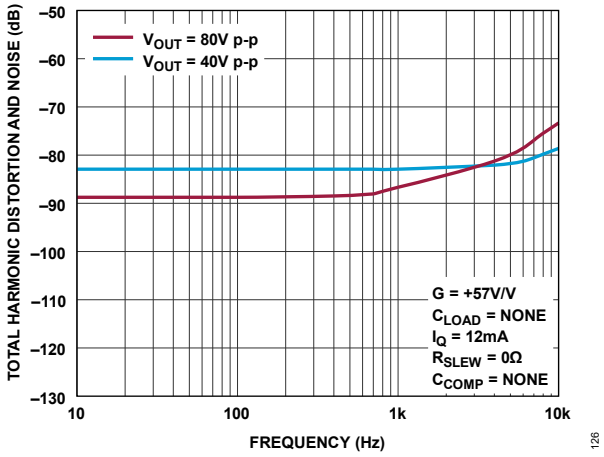

Figure 26. THD + N vs. Frequency

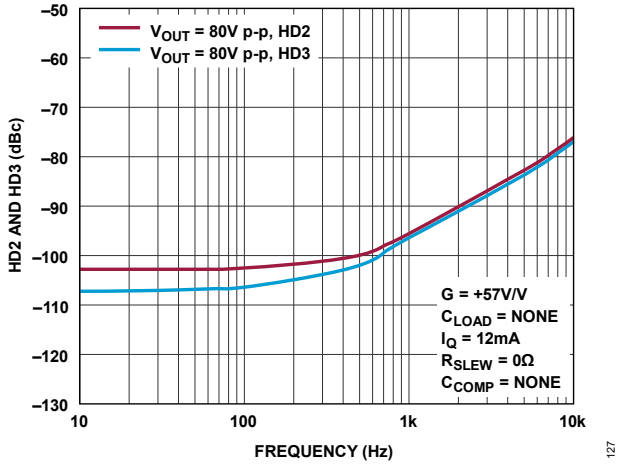

Figure 27. HD2/HD3 vs. Frequency

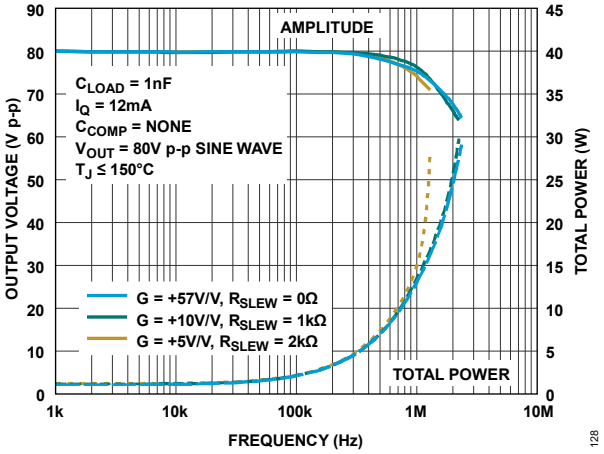

Figure 28. Large Signal Frequency Response and Total Power vs. Gain and R_{SLEW}

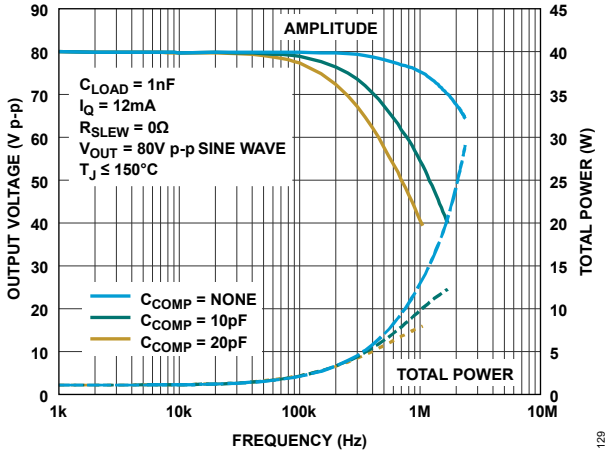

Figure 29. Large Signal Frequency Response and Total Power vs. C_{COMP}

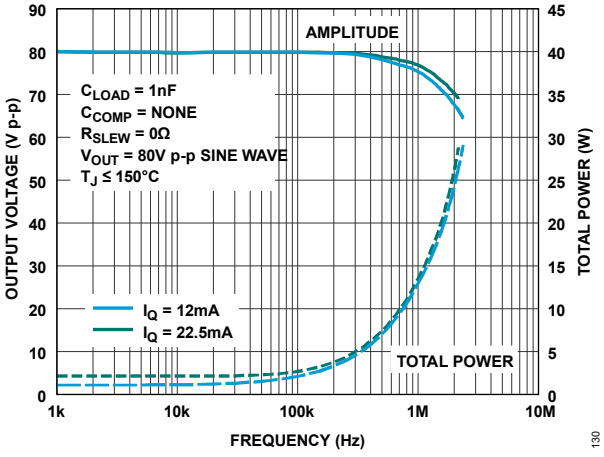

Figure 30. Large Signal Frequency Response and Total Power vs. I_Q

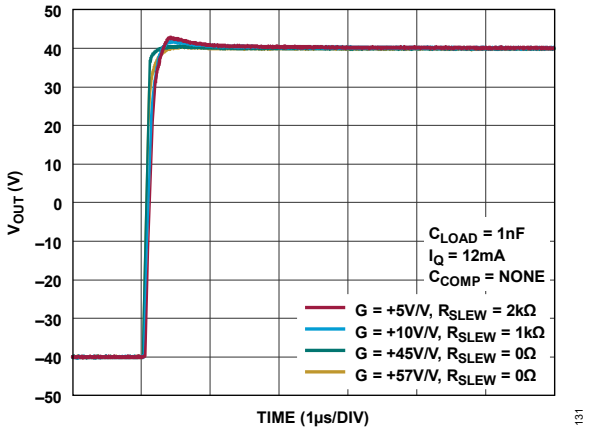

Figure 31. Large Signal Step Response, Rising Edge, Various Gain and R_{SLEW}

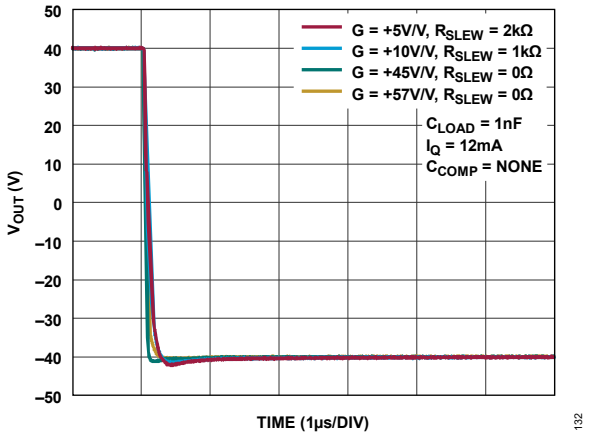

Figure 32. Large Signal Step Response, Falling Edge, Various Gain and R_{SLEW}

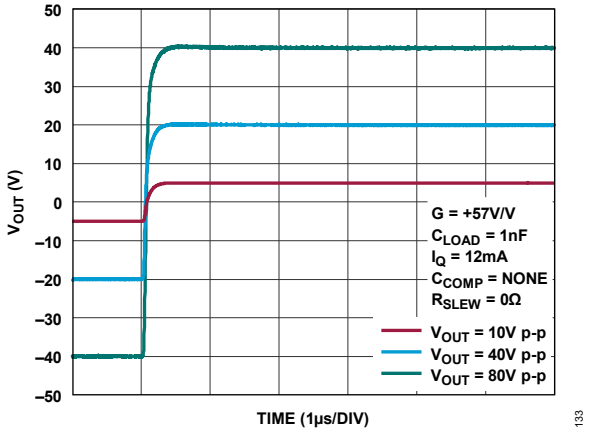

Figure 33. Large Signal Step Response, Rising Edge, Various Amplitude

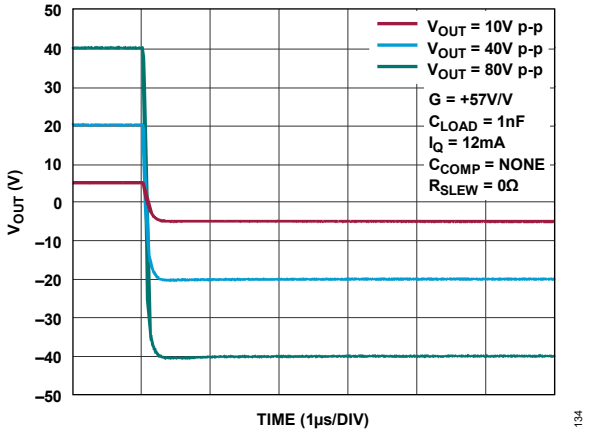

Figure 34. Large Signal Step Response, Falling Edge, Various Amplitude

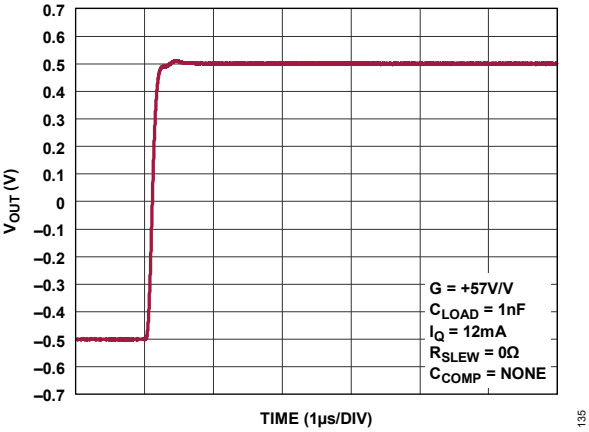

Figure 35. Small Signal Step Response, Rising Edge

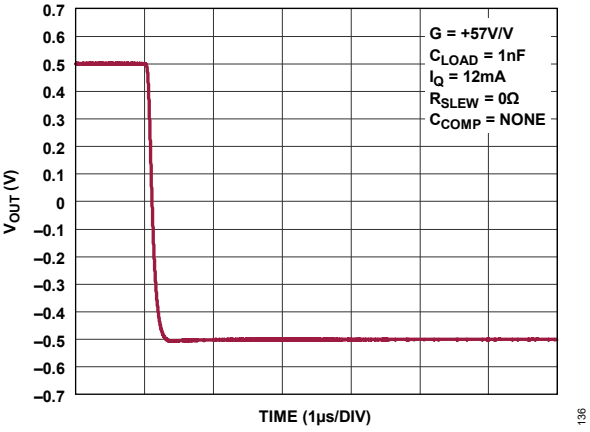

Figure 36. Small Signal Step Response, Falling Edge

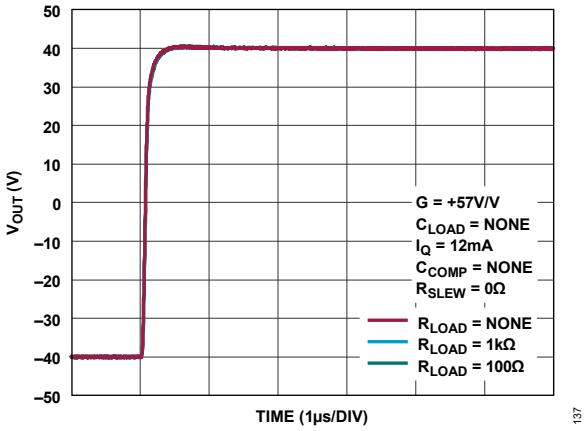

Figure 37. Large Signal Step Response, Rising Edge, Various R_{LOAD}

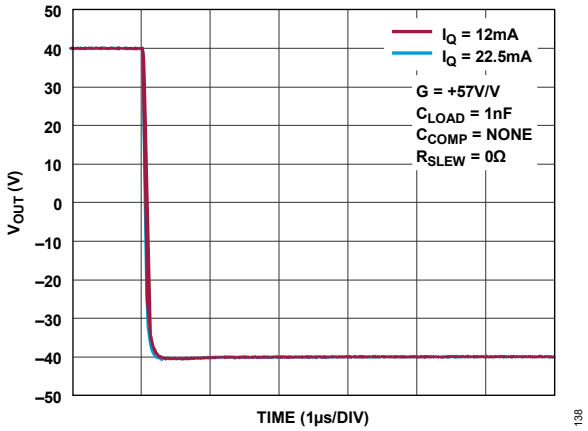

Figure 38. Large Signal Step Response, Falling Edge, Various R_{LOAD}

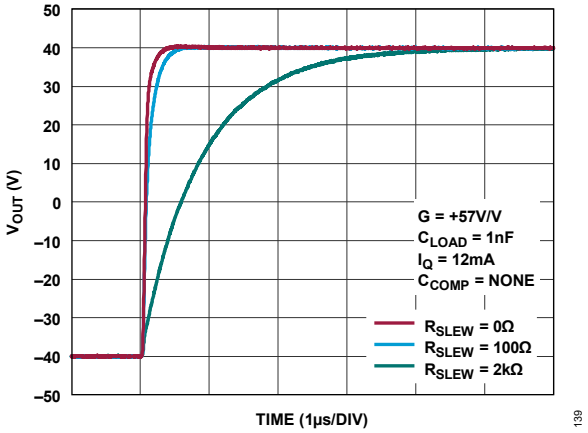

Figure 39. Large Signal Step Response, Rising Edge, Various R_{SLEW}

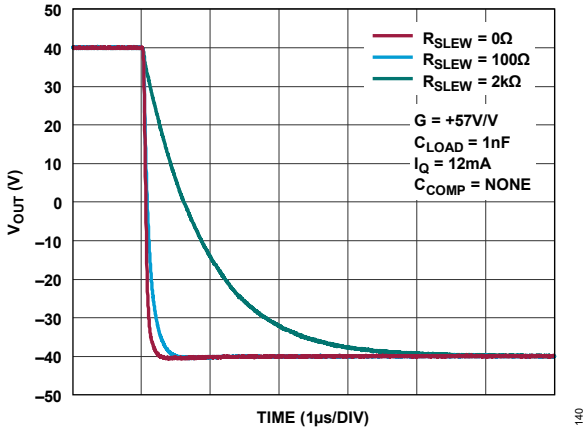

Figure 40. Large Signal Step Response, Falling Edge, Various R_{SLEW}

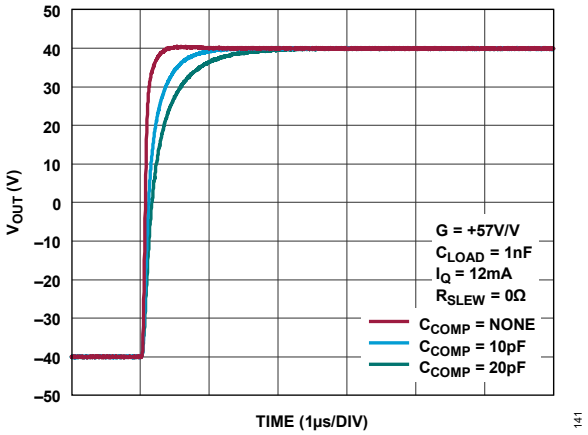

Figure 41. Large Signal Step Response, Rising Edge, Various C_{COMP}

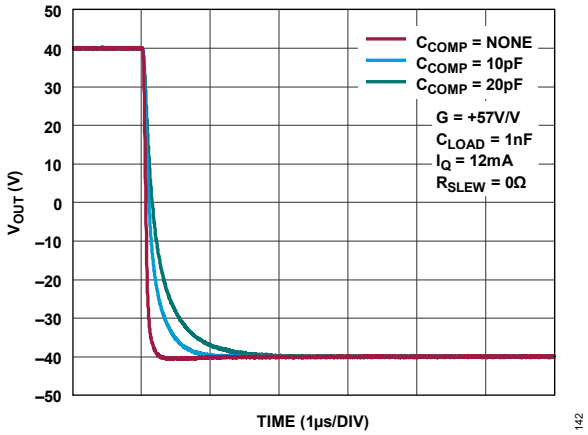

Figure 42. Large Signal Step Response, Falling Edge, Various C_{COMP}

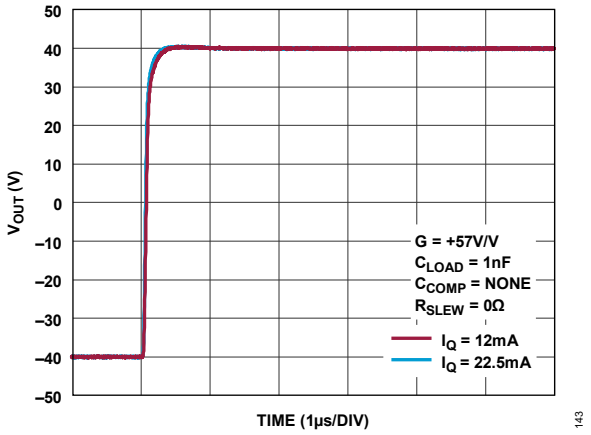

Figure 43. Large Signal Step Response, Rising Edge, Various I_Q

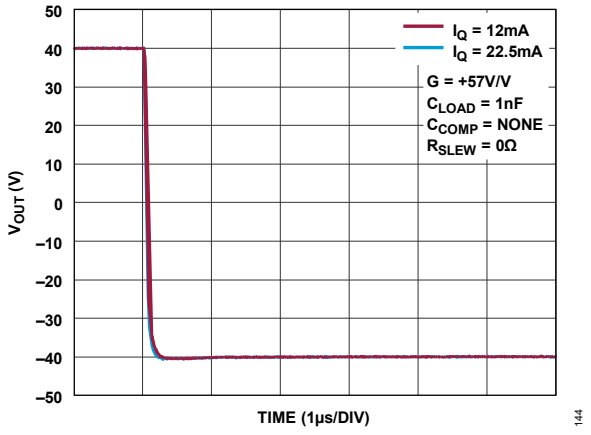

Figure 44. Large Signal Step Response, Falling Edge, Various I_Q

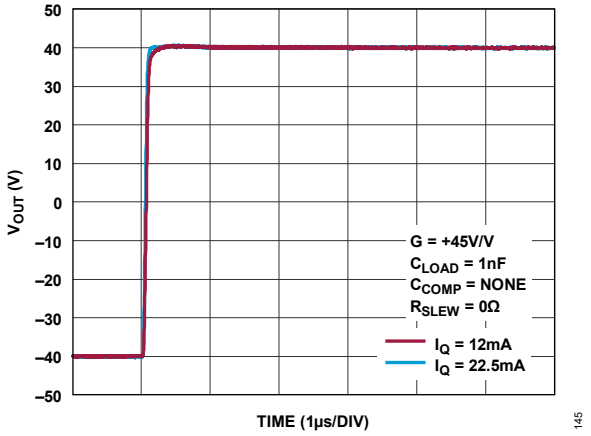

Figure 45. Large Signal Step Response, Rising Edge, Various I_Q, G = 45

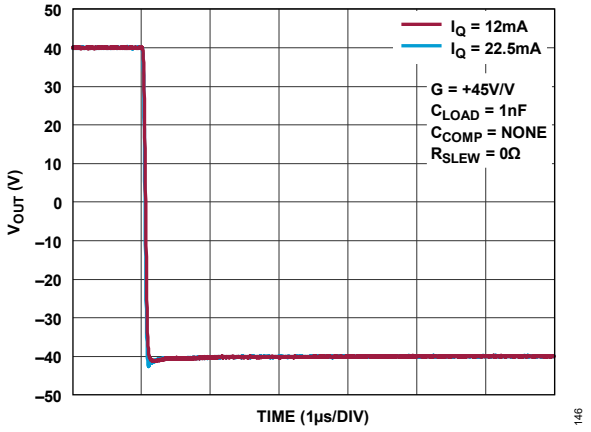

Figure 46. Large Signal Step Response, Falling Edge, Various I_Q, G = 45

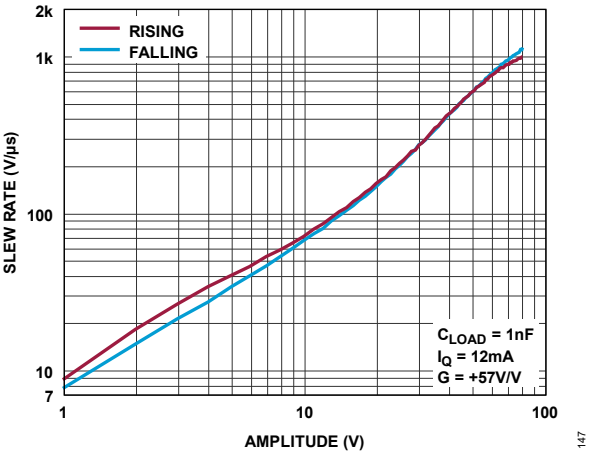

Figure 47. Slew Rate vs. Amplitude

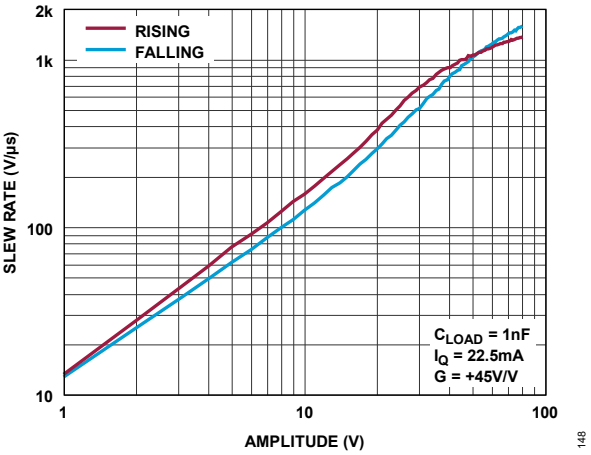

Figure 48. Slew Rate vs. Amplitude, G = 45, I_Q = 22.5mA

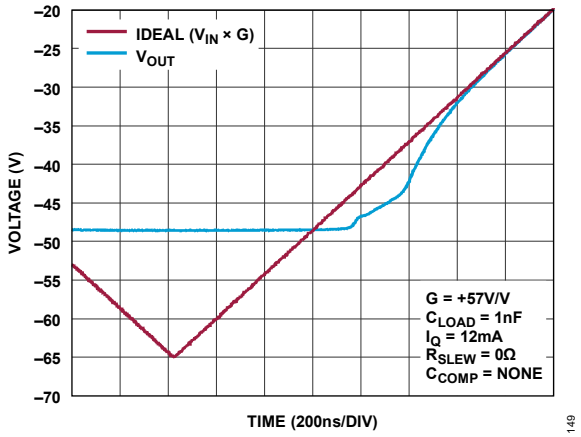

Figure 49. Output Overdrive Recovery vs. Time, Rising

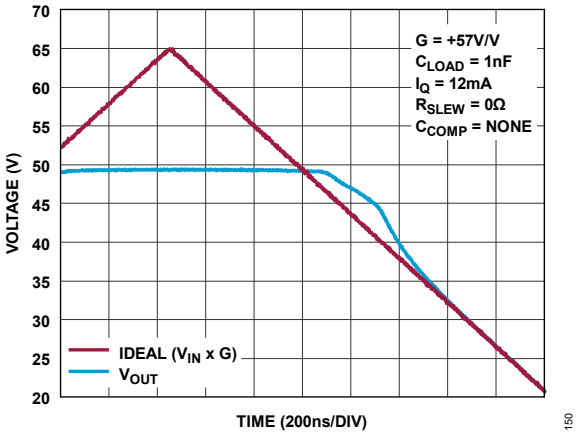

Figure 50. Output Overdrive Recovery vs. Time, Falling

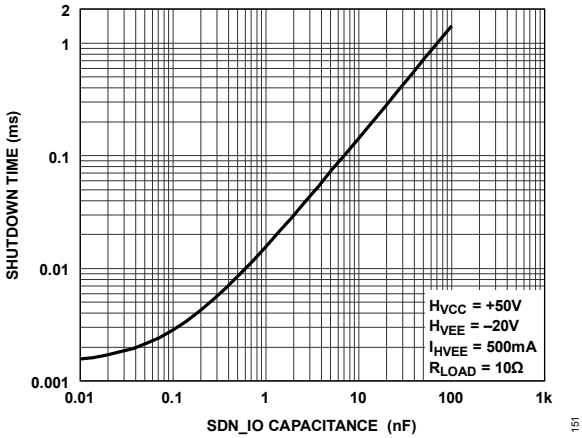

Figure 51. Shutdown Response vs. SDNIO Capacitance

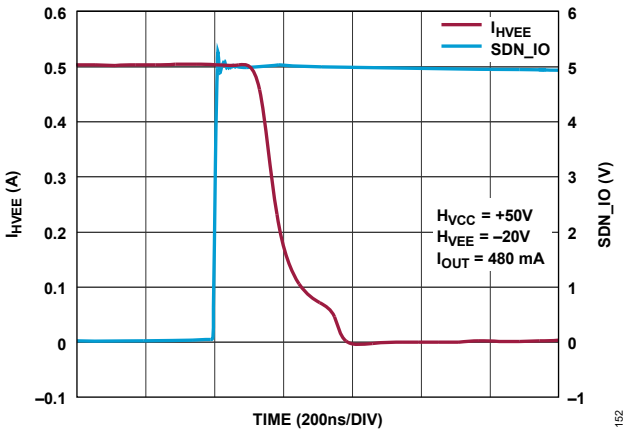

Figure 52. Shutdown Response vs. Time, SDNIO Driven

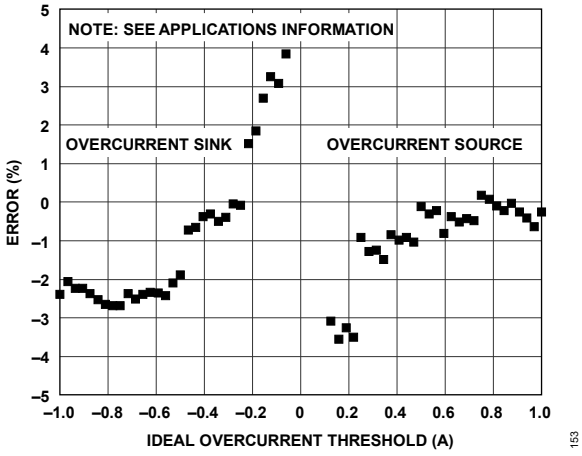

Figure 53. DC Overcurrent Setpoint Error vs. Current Setpoint

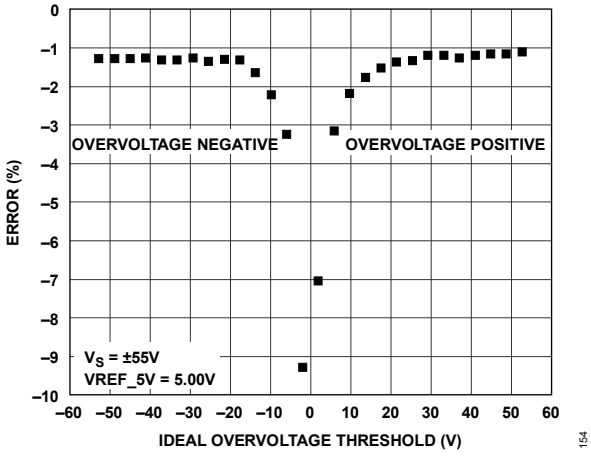

Figure 54. DC Overvoltage Setpoint Error vs. Voltage Setpoint

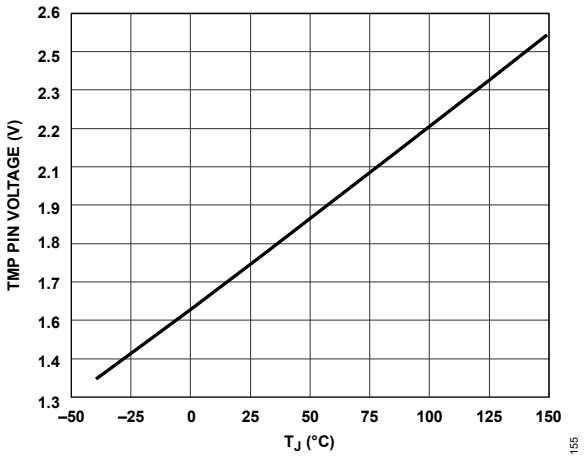

Figure 55. TMP Voltage vs. Junction Temperature

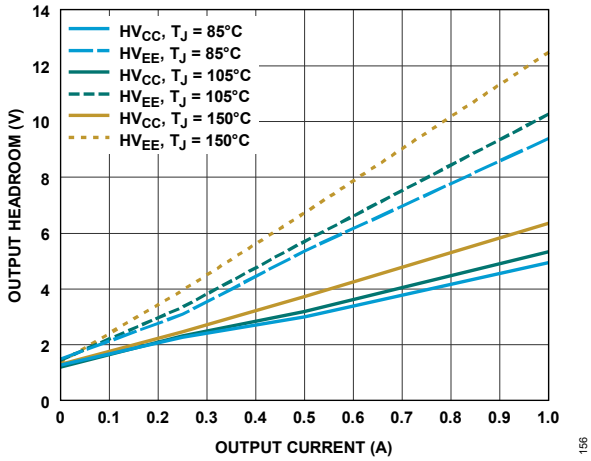

Figure 56. Output Headroom vs. Output Current and Temperature

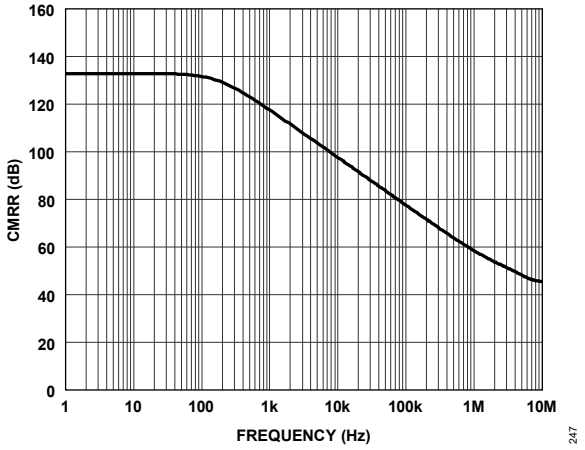

Figure 57. CMRR vs. Frequency

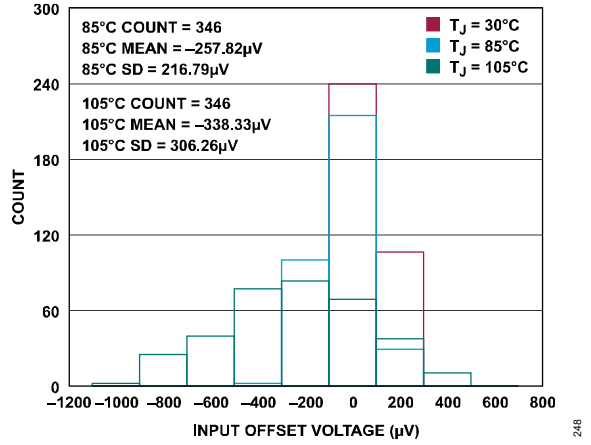

Figure 58. Input Offset Voltage Distribution vs. Temperature

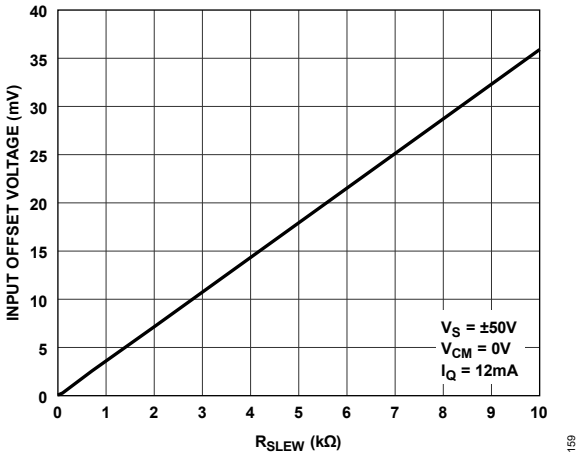

Figure 59. Input Offset Voltage vs. R_{SLEW}

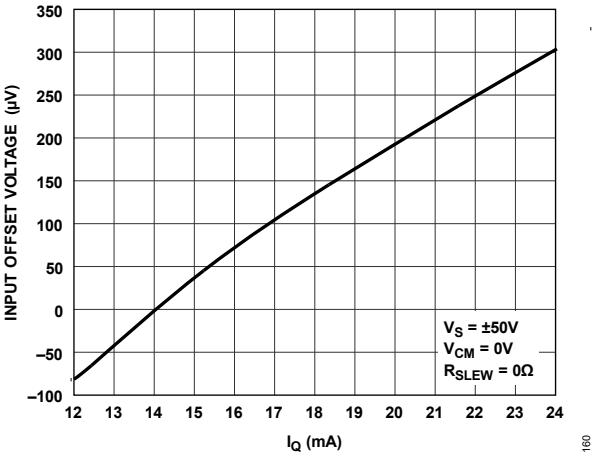

Figure 60. Input Offset Voltage vs. I_Q

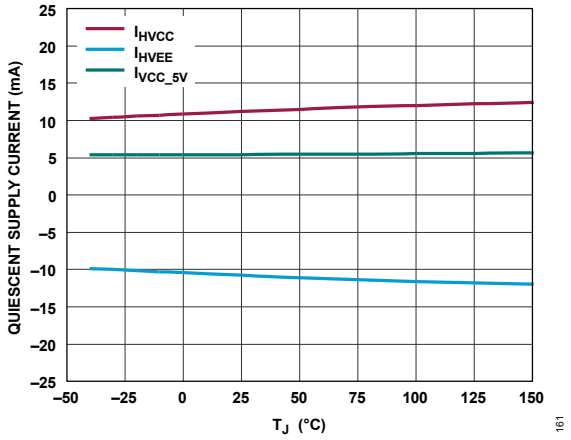

Figure 61. Quiescent Supply Current vs. Junction Temperature

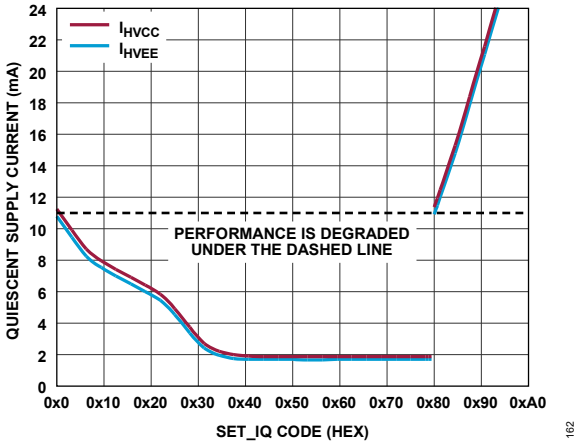

Figure 62. Quiescent Supply Current vs. SET_IQ Code

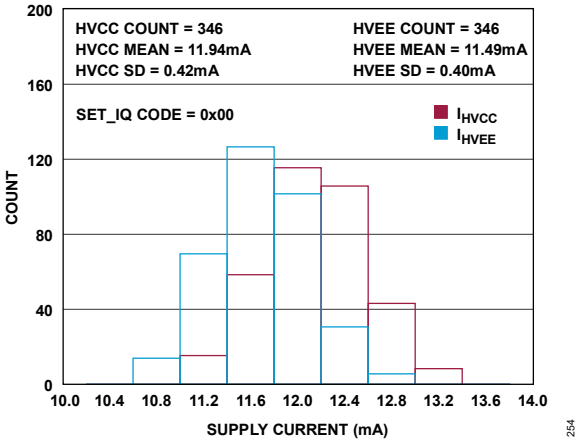

Figure 63. Quiescent Supply Current (I_Q) Distribution, I_Q = 12mA (Default)

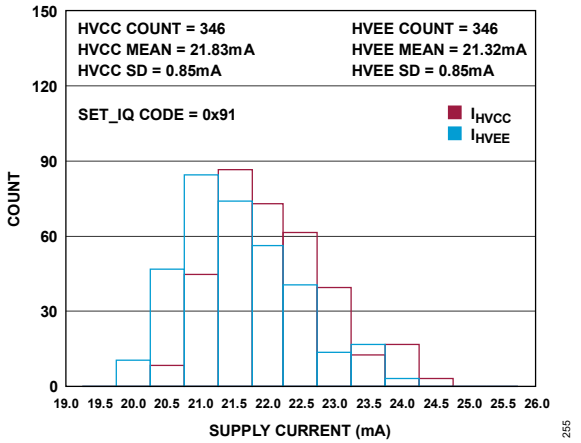

Figure 64. Quiescent Supply Current (I_Q) Distribution, I_Q = 22.5mA

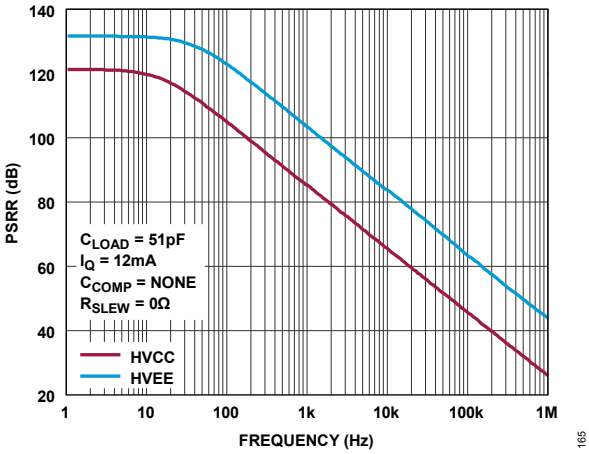

Figure 65. PSRR vs. Frequency, HVCC and HVEE

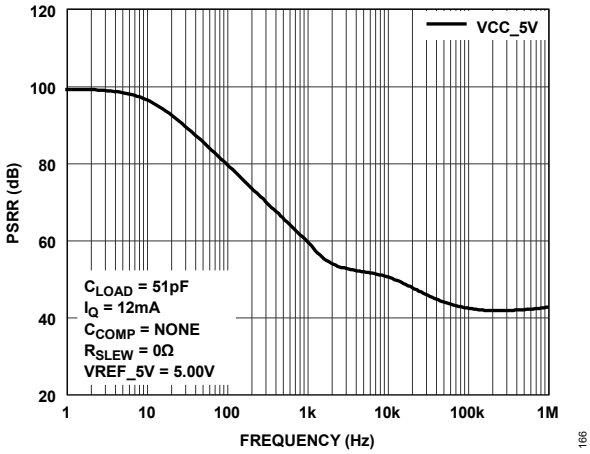

Figure 66. PSRR vs. Frequency, VCC_5V

TERMINOLOGY

Alarm

Alarm refers to the detection of any of the five fault conditions monitored by the protection system: overcurrent (sourcing or sinking), overvoltage (positive or negative), or overtemperature. The alarm flag is customizable to either self-clear upon fault clear, or latch the alarm state as evidence of fault occurrence. When any alarm is latched, it must be cleared.

Arm

To arm the protection system is to put the amplifier into a mode where it detects an alarm condition and shuts down the device.

Disarm

To disarm the amplifier is to put it into a state where it ignores an alarm condition and does not shut down the device. Use extreme caution when the amplifier is disarmed as it is unprotected from faults and possible damage.

Fault

A fault is any of the five overload conditions detectable by the protection system. Any fault triggers an alarm, though an alarm must exist for some minimum (user-adjustable) duration to force a shutdown.

Protection System

The protection system comprises limit-setting DACs, comparators, and logic gates that detect faults according to user-specified limits. See *Figure 69* for a block diagram showing basic functionality.

Reserved

Reserved refers to internal registers not for user access.

Safe Operating Area (SOA)

The safe operating area is a two-dimensional envelope bounded by parameters the user must manage to prevent damage from overheating.

Shutdown and Sleep

Both shutdown and sleep refer to a state of inactivity characterized by floating (high impedance) output and greatly reduced power consumption.

Slew Boost

Slew boost refers to a design feature of the ADHV4710 that increases supply current during fast input signal transitions, permitting faster output slew without the continuous power-dissipation penalty of conventional high-speed amplifiers.

THEORY OF OPERATION

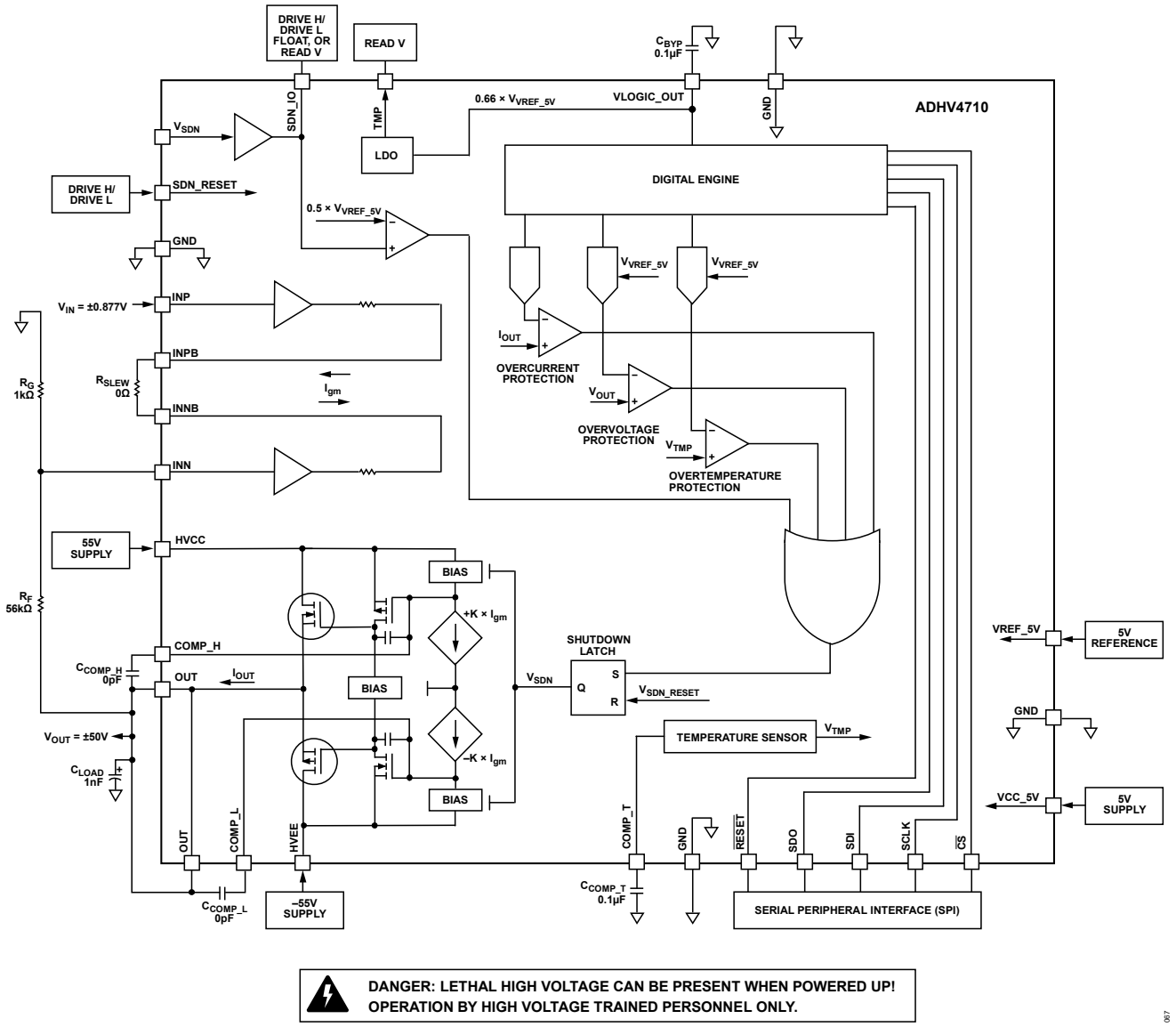

Figure 67. ADHV4710 Standard Configuration

Overview

The ADHV4710 is a high voltage, high power, high speed operational amplifier optimized for large output current (up to ±1A) and high slew rate (up to ±1300V/µs) at high voltage (up to ±52V) into capacitive and resistive loads. Combining a high voltage amplifier with low voltage analog circuitry and an SPI programmable digital engine, the ADHV4710 is ideally suited for high voltage applications such as automated test equipment (ATE), programmable power supplies, and piezo drive.

The ADHV4710 has extensive configurability for high voltage signal chains under a wide variety of conditions. The amplifier achieves high slew rate and bandwidth at high gain but can alternatively be configured in low gain for high voltage input and output. External transconductance resistor R_{SLEW} enables stability under any gain and adjustable slew rate. External compensation capacitor C_{COMP} enables the amplifier output to stably drive unlimited capacitive load.

As a high voltage operational amplifier, the ADHV4710 can be used in any operational amplifier negative feedback configuration: as a noninverting amplifier, as an inverting amplifier, or as a difference amplifier. Both input and output to the amplifier can be high voltage, within the supply range of the device.

The ADHV4710 requires dual high voltage (up to ±55V) power supplies at HVCC and HVEE, and a single low voltage (5V) power supply at VCC_5V. The part generates 3V internally from a low dropout (LDO) output at VLOGIC_OUT. See *Power Supplies and Decoupling*.

A reference of 5V is required at VREF_5V to provide the reference voltage for analog low voltage and protection threshold DACs. Connect VREF_5V to an external 5V reference or to VCC_5V (reduced accuracy). See the *VREF_5V* section.

In addition to drive capability, the ADHV4710 provides a suite of features relating to fault monitoring and load protection. The part features a junction temperature monitor providing voltage output at the TMP pin, indicating junction temperature up to 2.5V at maximum junction temperature of 150°C. The digital engine allows for programmable output current limit (source current and/or sink current), programmable output voltage limit (positive voltage and/or negative voltage), and programmable temperature limit (maximum junction temperature). See *Shutdown Protection Settings*.

Amplifier Theory

The ADHV4710 operational amplifier architecture is shown as following with emphasized connections to key external components R_{SLEW}, CCOMP_H, and CCOMP_L for extendable configurability of the amplifier.

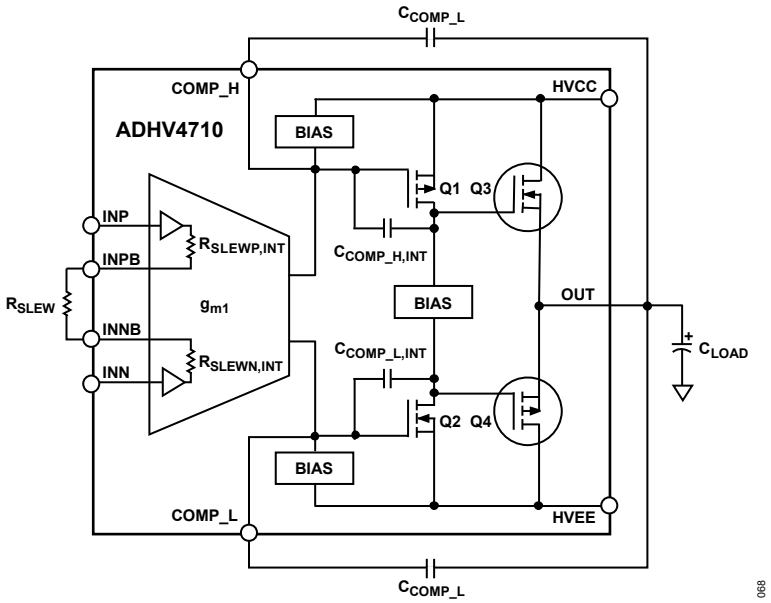

Figure 68. ADHV4710 Amplifier Architecture

The ADHV4710 amplifier architecture supports high voltage inputs (INP and INN) and high voltage output (OUT) within the full supply span (HVCC to HVEE). The inputs of the amplifier are high impedance, and the amplifier contains two gain stages, enabling high open-loop gain for precision and high speed amplifier drive.

The input stage of the amplifier has transconductance gm1, which is determined primarily by the external R_{SLEW} resistor but is also affected by small internal parasitic resistances (RSLEWP,INT and RSLEWN,INT). The open-loop gain of the amplifier is a product of the input stage transconductance gm1 and therefore changes with R_{SLEW}.

The amplifier open-loop gain varies inversely to R_{SLEW}:

$$A_{OL} \propto \frac{1}{R_{SLEW}}$$

If the amplifier is configured in a lower closed-loop gain, the phase margin of the amplifier decreases, which can lead to amplifier instability. The effect of lower closed-loop gain can be compensated for by reducing the amplifier open-loop gain to recover the phase margin of the amplifier, which increases the amplifier stability when configured in lower closed-loop gain.

The ADHV4710 is stable with R_{SLEW} = 0Ω for closed-loop gain greater than or equal to 40 with C_{LOAD} ≤ 1 nF.

By reducing the open-loop gain of the amplifier, increased R_{SLEW} is used to stabilize the amplifier for lower closed-loop gain configurations: closed-loop gain < 40.

The input stage transconductance gm1 produces an output current into pre-driver transistors (Q1, Q2), which drive the compensation capacitance of the amplifier. The compensation capacitance is determined primarily by the external CCOMP_H capacitor and CCOMP_L capacitor but is also effected by small internal parasitic capacitances (CCOMP_H,INT and CCOMP_L,INT).

The dominant pole of the amplifier open-loop frequency response varies inversely to CCOMP_H and CCOMP_L:

$$f_{p,dominant} \propto \frac{1}{C_{COMP\_H} + C_{COMP\_L}}$$

The output stage of the amplifier consists of high voltage, high power DMOS transistors (Q3, Q4) configured in a class AB buffer configuration for high voltage drive, high output current drive, and low output impedance to enable maximum load drive capability into capacitive and resistive loads.

Driving a capacitive load with the amplifier output results in a non-dominant pole, which varies inversely to C_{LOAD}:

$$f_{p,load} \propto \frac{1}{C_{LOAD}}$$

As the capacitive load value increases, the pole due to the load moves to a lower frequency. Consequently, the phase margin of the amplifier decreases, which can lead to amplifier instability. The effect of driving higher capacitive load can be compensated for by reducing the dominant pole frequency to recover the phase margin of the amplifier, which increases the amplifier stability when driving a large capacitive load.

The ADHV4710 is stable with CCOMP_H = CCOMP_L = 0pF for closed-loop gain greater than or equal to 40 with C_{LOAD} ≤ 1nF.

By reducing the dominant pole frequency, increased CCOMP_H and CCOMP_L are used to stabilize the amplifier for higher capacitive load drive configurations: C_{LOAD} > 1nF.

To select R_{SLEW}, CCOMP_H, and CCOMP_L, see *Table 7* for recommended values for select closed-loop gains and C_{LOAD} for small signal stability. See the *Limiting Dynamic Peak Current for >1nF Loads* section for large signal information.

Table 7. Recommended Compensation for Gain and C_{LOAD} for Small Signal Stability

Closed-Loop Gain	C_{LOAD}	Recommended R_{SLEW}	Recommended CCOMP_H = CCOMP_L	Closed-Loop Bandwidth	Gain Peaking
2 (RF = 10kΩ, RG = 10kΩ)	0.47nF	2kΩ	20pF	2.4MHz	0dB
	4.7nF		24pF	4.2MHz	0dB
	47nF		51pF	1.5MHz	0dB
5 (RF = 12kΩ, RG = 3kΩ)	0.47nF	2kΩ	2pF	4.3MHz	0dB
	4.7nF		6.2pF	2.9MHz	0dB
	47nF		22pF	0.9MHz	0dB
10 (RF = 9kΩ, RG = 1kΩ)	0.47nF	1kΩ	0pF	4.5MHz	0dB
	4.7nF		3.9pF	2.7MHz	0dB
	47nF		20pF	0.8MHz	0dB
40 (RF = 39kΩ, RG = 1kΩ)	0.47nF	0Ω	2pF	2.8MHz	0dB
	4.7nF		5.1pF	3.9MHz	0dB
	47nF		20pF	1.0MHz	0dB
57 (RF = 56kΩ, RG = 1kΩ)	0.47nF	0Ω	0pF	2.5MHz	0dB
	4.7nF		2.4pF	2.2MHz	0dB
	47nF		13pF	0.9MHz	0dB

Slew Boost (INPB, INNB, and R_{SLEW})

The ADHV4710 amplifier employs a slew boosting circuit to enhance high-speed signal fidelity. Slew boost is a variable-enhancement mechanism that increases quiescent current in proportion to the instantaneous differential voltage sensed at the inputs to the operational amplifier. As with any voltage-feedback operational amplifier, the inputs are kept very nearly equal through negative feedback. In cases where the output is unable to keep up with a rapidly changing input (disrupting the feedback loop), the inputs momentarily begin to move apart. This differential signal induces the slew boost circuit to increase supply current, allowing the output to slew faster, and restores the disrupted feedback signal.

Under applications driving a capacitive load, the slew rate of the amplifier must be controlled to keep the output current drive within safe operating area. For short duration slew < 100ns, the slew rate must not violate peak instantaneous output current drive (±1.2A). For longer duration, the slew rate must not violate continuous output current drive (±1A).

$$Slew\ Rate < \frac{I_{out,max}}{C_{LOAD}}$$

The slew boost current is determined by the differential voltage across the inputs imposed across the slew resistor R_{SLEW} connected from pin INPB to pin INNB. For maximum slew capability, R_{SLEW} can be a short (0Ω), and a larger value of R_{SLEW} can be used to reduce the peak slew rate and the peak dynamic current through the amplifier during slewing events. Increasing R_{SLEW} slows down and stabilizes the amplifier at the expense of a marginal degradation in offset and noise of the amplifier.

The additional current is typically needed for the duration of the slew event but increases power dissipation significantly during that time. The amount of additional self-heating that occurs as a result of this depends on the

signal dynamics. For instance, for a 100kHz square wave with a period of 10µs, the slew boost is only active for 1% of the waveform's period, resulting in a small increase in overall power dissipation.

Additionally, slew boosting of the amplifier can be limited by placing differential input antiparallel diodes from pin INP to pin INN. This limits the maximum differential voltage across the input during a slew event, which correspondingly limits the maximum slew rate of the amplifier.

The dynamic safe operating area (SOA) is shown in the *Safe Operating Area* section. The dynamic SOA shows the connection between the output swing and the maximum input/output frequency for a pulse response. If slew-boost is activated frequently, as a high-frequency square wave might require, power dissipation increases dramatically and may push the device outside its dynamic SOA. To expand the dynamic SOA curve, use additional thermal management or limit the input/output edge speed, which limits the current produced by the slew boosting circuit and reduces the internal power dissipation.

Output Current Drive

The ADHV4710's output stage is constructed with cascoded, double-diffused, metal-oxide-semiconductor (DMOS) high voltage transistors and is optimized for high currents into capacitive loads. It is designed to generate edge speeds of up to 1400V/µs and deliver ±1A continuously with proper thermal management.

Under applications driving significant output current, the output current drive must be controlled within the safe operating area. For short duration output current < 100ns, the output current drive must not violate the peak instantaneous output current drive (±1.2A). For longer duration output current, the output current drive must not violate the continuous output current drive (±1A).

In cases of high output current drive, consider the power dissipation effect of the current through the device at high voltage. This can correspond to extremely high instantaneous power dissipation.

The default heatsink for ADHV4710 is Wakefield-Vette P/N 518-95AB and active cooling is preferred for higher power dissipation applications. See *Thermal Management* for thermal related details.

The ADHV4710's protection system is highly configurable to suit a wide variety of applications. To provide maximum flexibility across applications, the ADHV4710 integrates independent monitoring of output current (sourcing and sinking), output voltage (positive and negative), and die temperature, providing protection for the amplifier and its load against five individual faults. See *Fault Monitoring and Protection* for details.

The ADHV4710 is configured with protection features disabled by default. Use SPI to enable and program the protection features. For manual overtemperature shutdown, tie the SDN_IO pin to TMP. The shutdown response time can be adjustable through a capacitor on SDN_IO pin. See *Shutdown Control (SDN_IO)* for delayed shutdown and manual thermal shutdown.

Initial Power-Up

Power Supplies and Decoupling

The ADHV4710 requires dual high voltage supplies in the range of ±12V to ±55V at HVCC and HVEE, as well as a single 5V low voltage supply at VCC_5V. Bypass all supply pins to ground using high quality, low ESR 0.1µF capacitors.

Place the bypass capacitors as close to the supply pins as possible, with a short, direct connection to the PCB's analog ground plane. Additionally, place four 1.2µF ceramic capacitors from each high voltage supply to ground to provide good low frequency bypassing, and to provide the needed current to support large, fast-slewing signals. Low-inductance planes are recommended for high voltage supply routing.

VLOGIC_OUT is the analog supply bypass point for the internal 3V LDO. VLOGIC_OUT requires a 0.1µF bypass capacitor from VLOGIC_OUT to GND.

VREF_5V

VREF_5V sets the reference voltage for internal alarm threshold DACs and must be biased. A precise 5V reference IC is recommended. Alternatively, VREF_5V can be connected to VCC_5V (reduced accuracy).

A reduced accuracy VREF_5V reference shifts the internal LDO reference voltage and causes the SDN_IO shutdown voltage, overvoltage, and overtemperature thresholds to vary from table-specified values. For example, if a 5V reference with 1% tolerance at VREF_5V is utilized, these levels may vary 1% from typical values.

The order of VCC_5V and VREF_5V power-on affects the initial state of the amplifier. See *Power Supply Sequencing*.

Power Supply Sequencing

The high voltage power supplies (HVCC and HVEE) and VCC_5V may be brought up individually, in any order.

The ADHV4710 can be powered up in shutdown or active mode.

Powering up the ADHV4710 in shutdown mode is recommended. This can be accomplished by floating the SDN_IO pin and powering on VCC_5V before VREF_5V. After initial power-up in shutdown mode, the SDN_IO pin must be pulled low to ensure the ADHV4710 is turned on. Subsequently, floating the SDN_IO pin enables the fault monitoring and protection feature while the ADHV4710 remains on. When powering down, bring VREF_5V down first, then bring down VCC_5V.

Powering up the ADHV4710 in active mode can be accomplished by floating SDN_IO, connecting VCC_5V to VREF_5V, and powering them on together. If the input of the amplifier is floating, use extreme caution when powering up with the amplifier enabled, as the output voltage can power on at high voltage. This may result in high output current if a load is present. Ensure the input of the amplifier is terminated to GND for the output of the amplifier to power on at a voltage close to GND.

Power-On-Reset (POR) and $\overline{\text{RESET}}$

The ADHV4710 executes a digital reset upon power-on. Power-on-reset (POR) resets all digital registers to default, including all alarm thresholds while powering-on the ADHV4710. The protection system is inactive upon power-on by default. Use caution in operating the device before any alarm thresholds are set and the protection system is enabled. Reset to defaults can also be commanded at any time through the SOFT_RESET register bit. See *Table 20* for more information on SOFT_RESET.

The default SOFT_RESET configuration is:

- Amplifier output enabled
- Protection system disabled
- Nominal quiescent current

Driving $\overline{\text{RESET}}$ LOW and then HIGH clears and resets all digital registers to default states.

Serial Peripheral Interface (SPI)

The ADHV4710 is controlled over a 4-wire serial interface with a clock rate up to 19MHz. As seen in *Figure 4* and *Figure 5*, data are clocked in on the rising edge of SCLK. The instruction phase always consists of 8 bits. The MSB of the instruction phase determines whether the serial interface is reading/writing, with the following 7 bits containing the desired address information. When the MSB of the instruction phase is "low", it is in write mode. When the MSB of the instruction phase is "high", it is in read mode. The two bytes after the instruction phase are

used for reading or writing data to the ADHV4710. For information about the addresses of the ADHV4710's control registers, see *Table 16*.

Shutdown and Sleep Control

Shutdown disables the amplifier. During shutdown, the HVCC and HVEE supply currents drop to ~120µA, and the output at pin OUT goes to a high impedance state (110kΩ). The impedance seen from a disabled amplifier output to GND may be dominated by the feedback resistor network in parallel with the amplifier output. When driving a capacitive load with a high impedance output, the output voltage drifts as the load capacitor discharges.

Shutdown may be initiated by the user, by pulsing SDN_IO high, or may be initiated by the protection system in response to an alarm of sufficient duration (see *Fault-Initiated Shutdown Protection Features* and *Shutdown Control (SDN_IO)* sections). To exit shutdown, use any of the following three ways:

- Pulse SDN_RESET high, then leave low.
- Pulse the HV_RESET bit high through two SPI commands (drive high, then drive low).
- Pulse SDN_IO low, then float.

Sleep refers to a non-latching state of inactivity like shutdown, but which is initiated (HV_SLEEP = 0) and terminated (HV_SLEEP = 1) through SPI commands. Sleep supersedes all commands that use the SDN_IO shutdown mechanism, both fault-initiated and user-initiated.

Fault-Initiated Shutdown Protection Features

The ADHV4710 is equipped with a power saving shutdown feature through SDN_IO. The shutdown can be either user-initiated to reduce power dissipation or fault-initiated by ADHV4710's protection system to prevent part damage. See *SHUTDOWN CONTROL (SDN_IO)* for user-initiated shutdown details. The ADHV4710 monitors five operating conditions internally and may be configured to shut down if any programmable alarm limit is exceeded:

- Sourcing overcurrent limit (to +1A)
- Sinking overcurrent limit (to −1A)
- Positive overvoltage limit (to +110V)
- Negative overvoltage limit (to −55V)
- Junction overtemperature limit (T_J = 20°C to T_J = 150°C)

See *Table 22* through *Table 28* or register addresses assigned to these limits.

Any of the five internal fault monitors latch the SDN_IO pin high if an alarm condition is detected. The latch condition persists until the fault condition is cleared and the ADHV4710 is re-enabled.

To re-enable the amplifier after shutdown, pulse the HV_RESET bit high through two SPI writes (drive high, then drive low). The ADHV4710 can also be re-enabled by pulsing SDN_RESET high, then leaving it low or pulling SDN_IO low and then floating the SDN_IO pin. This re-enables the fault monitoring and protection. The digital resource used to pulse SDN_IO low must be capable of driving ~200µA to override SDN_IO's high state. See *SHUTDOWN CONTROL (SDN_IO)* for details.

Fault Monitoring and Protection Control Logic

Fault monitoring and protection are implemented by setting thresholds and arming the protection system for each fault type individually. Thresholds are programmed through SPI for the desired protections to be implemented. Exceeding a programmed threshold triggers an alarm and shuts down the ADHV4710. *Figure 69* shows the control logic for the fault monitoring and protection.

Each of the five monitored faults has four digital registers associated with it:

1. A programmable threshold. The threshold can be programmed through register 0x08 (CTL_REG_08) through 0x0C (CTL_REG_12), bit [6:0]. See *Shutdown Protection Settings* for ranges and resolutions settings.
2. ARM. The ARM can be programmed through register 0x08 (CTL_REG_08) through 0x0C (CTL_REG_12), bit [7]. Setting the corresponding ARM to (1) directs the protection system to shut down in response to an alarm. Setting the corresponding ARM to (0) disarms the protection system, inhibiting shutdown in case of an alarm. There is no protection from faults when ARM is (0).
3. ALARM indicator flags. ALARM indicator flags can be read and cleared through register 0x0E (CTRL_ REG_14). ALARM indicator flags are set to (1) by the protection system if a fault occurs while the protection system is armed. ALARM remains at (1) for as long the fault condition persists and returns to (0) when the fault condition clears. If the ALARM forces a shutdown of the amplifier, the amplifier remains in shutdown even if the fault condition clears and the ALARM flag resets. The ALARM bits indicate the status of the fault conditions. Once the ALARM clears, it may not be possible to determine what fault(s) occurred previously. See the ALARM_LATCH function for transient faults detections. To clear an ALARM indicator flag, write a (1) to the respective ALARM register bit.
4. ALARM_LATCH is set by the user to latch any ALARM flag, preserving evidence of any transient fault that may occur. ALARM_LATCH can be programed through register 0x0D (CTRL_REG_13). When an ALARM_LATCH is enabled and when an ALARM indicator flag is triggered, the ALARM indicator flag remains even if the associated fault condition clears. This is helpful in identifying transient faults. To clear an ALARM_LATCH flag, write a (0) to the respective ALARM_LATCH register bit.

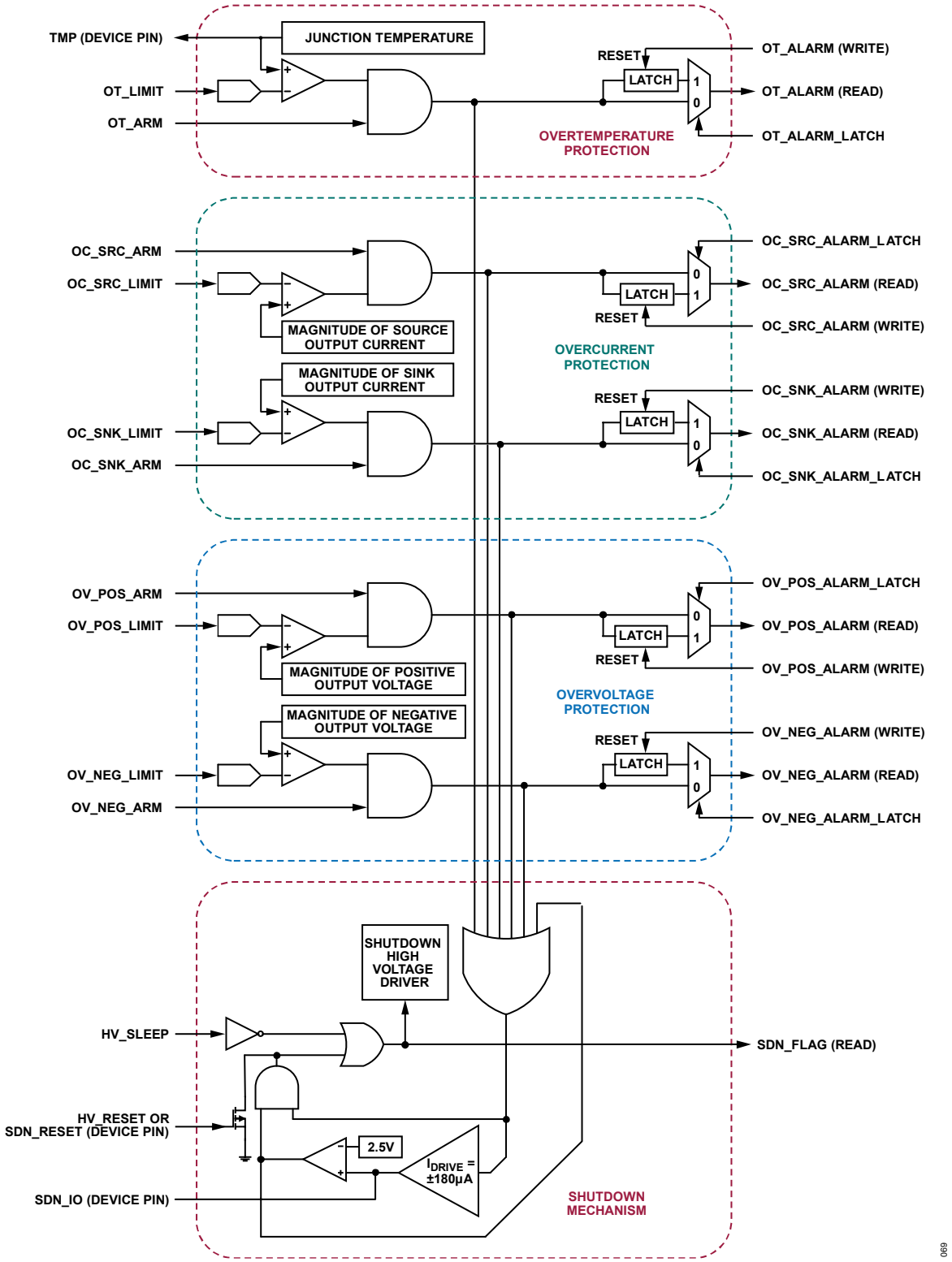

Figure 69. Fault Monitoring and Protection Control Logic

Shutdown Protection Settings

The code range for the shutdown protection features exceeds the device's operational range; the range is selected to optimize linearity and accuracy at the limitations of the part, where shutdown control is most critical. Note that the values from *Table 9* to *Table 11* are rounded and are not the exact values based on the conversion factor from the code to threshold value.

Table 8. Shutdown Protection Ranges and Resolution

Fault Type	Nominal Range	Nominal Resolution
Overcurrent	±1A	15.625mA
Overvoltage	Positive: 12V to 110V Negative: −55V to 0V	1.953V
Overtemperature	Up to T_J = 150°C	6.51°C

Programming Shutdown Threshold Settings

The register map in *Table 18* shows that the 8-bit registers, CTRL_REG_08 through CTRL_REG_12, are used to arm the five internal fault monitors and program the desired threshold value. For these internal fault monitoring registers, bit 7 is used for toggling the protection feature on or off, and bits [6:0] are used for setting the alarm threshold. It is important to note that the binary codes in *Table 9* to *Table 11* are bits [6:0] when programming the registers for fault monitoring and does not include bit 7 in the calculations.

Follow the order of the subsequent steps to properly program threshold settings into the internal fault monitoring registers and turn on each fault monitoring feature:

- Program bits [6:0] with the desired threshold code.
- Program bit [7] to a value of a (1) to enable protection and rewrite to bits [6:0] with the desired threshold code again.

Programming Overcurrent Protection

Overcurrent (source) protection is programmed in register 0x08: CTRL_REG_08. Overcurrent (sink) protection is programmed in register 0x09: CTRL_REG_09.

The threshold programming resolution (1 LSB) for overcurrent protection is nominally 15.625mA.

To convert code to current threshold:

$$Current\ Threshold\ (mA) = Code_{Decimal}(LSB) \times 15.625\left(\frac{mA}{LSB}\right)$$

To convert current to code:

$$Code_{Decimal}(LSB) = \frac{Current\ Threshold\ (mA)}{15.625\left(\frac{mA}{LSB}\right)}$$

If the user converts the desired current into a code in decimal, round the calculated value to the nearest integer. Plug the integer value back into the code-to-current-threshold equation to determine the actual temperature threshold value.

See *Table 9* for typical threshold codes tied to common operating currents.

See *Programming Shutdown Threshold Settings* on how to properly program the shutdown threshold settings. See *Overcurrent Threshold Errors with Headroom* for additional information on using this feature.

Table 9. Typical Threshold Codes for Operating Currents

Binary Code	Hexadecimal Value	Decimal Value	Current (mA)
000 0110	0x06	6	100
001 0011	0x13	19	300
010 0000	0x21	32	500
100 0000	0x40	64	1000

Programming Overvoltage Protection

Overvoltage (positive) protection is programmed in register 0x0A: CTRL_REG_10. Overvoltage (negative) protection is programmed in register 0x0B: CTRL_REG_11.

The threshold programming resolution (1 LSB) for overvoltage protection is nominally 1.953V.

To convert code to voltage threshold:

$$Voltage\ Threshold\ (V) = Code_{Decimal}(LSB) \times 1.953\left(\frac{V}{LSB}\right)$$

To convert voltage to code:

$$Code_{Decimal}(LSB) = \frac{Voltage\ Threshold\ (V)}{1.953\ \left(\frac{V}{LSB}\right)}$$

If the user converts the desired voltage into a code in decimal, round the calculated value to the nearest integer. Plug the integer value back into the code-to-voltage-threshold equation to determine the actual temperature threshold value.

See *Table 10* for typical threshold codes tied to common operating voltages.

See the *Programming Shutdown Threshold Settings* section on how to properly program the shutdown threshold settings.

Table 10. Typical Threshold Codes for Operating Voltages

Binary Code	Hexadecimal Code	Decimal Code	Voltage (V)
000 1010	0x0A	10	20
001 0100	0x14	20	40
001 1100	0x1C	28	55
010 1000 (Positive Only)	0x28	40	80
011 1000 (Positive Only)	0x38	56	110

Programming Overtemperature Protection

Overtemperature protection is programmed in register 0x0C: CTRL_REG_12.

The threshold programming resolution (1 LSB) for overtemperature protection is nominally 6.51°C.

To convert code to temperature:

$$Temperature\ Threshold\ (℃) = Code_{Decimal}(LSB) \times 6.51\left(\frac{℃}{LSB}\right) - 266.64\ (℃)$$

To convert temperature to code:

$$Code_{Decimal}(LSB) = \frac{Temperature\ Threshold\ (℃) + 266.64\ (℃)}{6.51\left(\frac{℃}{LSB}\right)}$$

If the user converts the desired temperature into a code in decimal, round the calculated value to the nearest integer. Plug the integer value back into the code-to-temperature equation to determine the actual temperature threshold value.

See *Table 11* for typical threshold codes tied to common operating temperatures.

See the *Programming Shutdown Threshold Settings* section on how to properly program the shutdown threshold settings.

Table 11. Typical Threshold Codes for Operating Temperatures

Binary Code	Hexadecimal Value	Decimal Value	Kelvin Temperature	Celsius Temperature
010 1100	0x2C	44	293	20
011 0110	0x36	54	358	85
011 1001	0x39	57	377	104
011 1011	0x3B	59	396	123
100 0000	0x40	64	423	150

Manual Thermal Shutdown

The ADHV4710 features an optional manual thermal shutdown at T_J = 150°C without the need for SPI communication and programming. This manual shutdown feature is only valid for thermal shutdown. The overcurrent and overvoltage protection still require SPI communication and programming.

To enable the manual thermal shutdown, tie TMP directly to SDN_IO, as shown in *Figure 70.* In this configuration, the ADHV4710 powers up in shutdown mode and must be enabled. If the TMP pin's analog output voltage reaches the SDN_IO's logic high threshold, which happens at approximately T_J = 150°C, shutdown mode is activated. The ADHV4710 does not self-reset when the die temperature has cooled below 150°C. The ADHV4710 remains in shutdown until resequencing the power supplies or the SDN_IO pin.

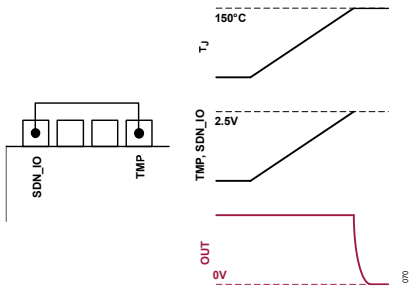

Figure 70. TMP and SDN_IO Pin Configuration for Manual Thermal Shutdown

Shutdown Control (SDN_IO)

The amplifier is disabled when SDN_IO is high. As directed in the power-up section, it is recommended to power-up with SDN_IO high so that the output amplifier is in shutdown mode and then bringing SDN_IO low once the desired ADHV4710 configuration is written over SPI. Subsequently, floating the SDN_IO pin enables the fault monitoring and protection feature while the ADHV4710 remains on. SDN_IO sinks ~180µA to override SDN_IO's high state.

When SDN_IO is floated, the driver is controlled by SPI commands. SDN_IO has both input and output functionality. The user can drive the SDN_IO pin to enable/disable the amplifier or monitor the SDN_IO. When SDN_IO is floated or connected to a high impedance digital pin such as a microcontroller GPIO, SDN_IO serves as a flag for any of the internal alarm conditions. When the ADHV4710 is enabled using SDN_RESET, the SDN_IO voltage decreases and converges towards 0V. When the ADHV4710 is disabled through fault protection, the SDN_IO voltage increases and converges towards 5V. See *Figure 69* for the logic behind SDN_IO and input/output functionality.

When SDN_IO is pulled high, the ADHV4710's HVCC and HVEE supply currents are reduced to ~120µA and the amplifier is disabled. The output goes to high impedance (110kΩ). The shutdown state is latched and the amplifier remains in shutdown even when SDN_IO is floated. To enable the ADHV4710 from shutdown, pulling SDN_IO low and following by floating the SDN_IO is required to enable the shutdown protection features.

When SDN_IO is held low or SDN_RESET high, the output is continuously enabled, and shutdown is inhibited. Use caution in this case as the device is unprotected from overstress. Holding SDN_IO low or SDN_RESET high disables the shutdown protection features.

Delayed Shutdown

The user may add delay to the ADHV4710's shutdown response time to improve noise immunity, with an external capacitor from SDN_IO to ground. The capacitor value is chosen so that the desired delay equals the time required for the voltage on SDN_IO to ramp from 0V to its threshold voltage of 2.5V under a constant current of 200µA. The capacitor value C_{SDNIO} is calculated according to the relationship:

$$C_{SDNIO} = \frac{(200\mu A \times t)}{2.5V}$$

where, t is the desired delay time.

Note: The chosen delay applies to all internally-detected alarms (current, voltage, and temperature).

For example, to add a 4.5µs delay so that short duration current or voltage spikes do not cause a shutdown, a capacitor is needed between SDN_IO and ground, with value:

$$C_{SDNIO} = \frac{(200\mu A \times 4.5\mu s)}{2.5V} = 360pF$$

Note that parasitic capacitance on the PCB impacts the shutdown response time. The values seen in *Figure 51* are the total capacitance on the SDN_IO pin, which includes the PCB's parasitic capacitance and added capacitor. In this example, any alarm condition shorter than 4.5µs in duration does not trigger a shutdown. *Figure 51* shows the ADHV4710's shutdown response time vs. various capacitance.

Alarm latching is particularly useful when delayed shutdown is implemented. In the previous example, a fault of less than 4.5µs duration does not trigger a shutdown, but the occurrence of a fault may be of interest for troubleshooting purposes. When the ALARM_LATCH is true (1), the states of the corresponding ALARM flags may be polled through SPI to see if any faults are detected, even if the event is too short to force a shutdown.

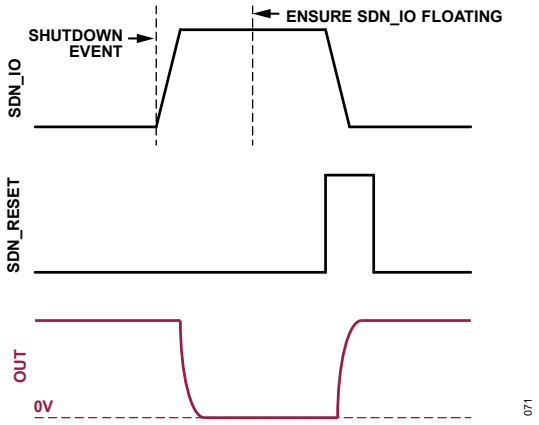

Figure 71. Shutdown Response Sequence

Thermal Monitoring (TMP)

Die temperature in the ADHV4710 is monitored by measuring its TMP pin voltage relative to GND. This pin's analog output voltage is proportional to die temperature and is converted to degrees Celsius using the formula:

$$T_J\ (^0C) = \frac{(VTMP - 1.6V)}{6\frac{mV}{^\circ C}}$$

More precise temperature readings can be achieved through a one-time room temperature calibration of the TMP pin.

The ADHV4710's thermal monitoring capability is independent of any overtemperature shutdown threshold and may be used whether or not TMP is strapped to SDN_IO. Note: If TMP is monitored while strapped to SDN_IO, a high impedance must be maintained by the user's monitoring circuit so that loading does not interfere with the shutdown function. Failure to maintain a high impedance on SDN_IO may result in damage to the ADHV4710 by inhibiting thermal shutdown.

Programmable Quiescent Current

Quiescent power dissipation may be increased for applications that require maximum dynamic performance. Programming higher supply current increases power dissipation and junction temperature at the benefit of slightly increased speed, slew rate, settling time, capacitive load drive, and noise.

This feature is controlled in CTRL_REG_04: SET_IQ and allows for adjusting the supply current up or down relative to the nominal supply current. The MSB sets the polarity of the supply current adjust: (0) is a decrease in supply current, whereas (1) is an increase in supply current. The remaining bits [6:0] are a monotonic but nonlinear control of the supply current across the span of codes (see *Figure 62*). From SET_IQ = 0x00, the part is at nominal supply current, bits [6:0] can be increased up to limit SET_IQ = 0x7F, where the part sees zero supply current, resulting in quiescent current starved shutdown. Decreasing the supply current from nominal results in degraded performance. From SET_IQ = 0x80, the part is again at nominal supply current, and bits [6:0] can be increased up to SET_IQ = 0xFF, where the part is at roughly double the nominal supply current. Exercise caution if increasing supply current, noting the thermal effects of the increased supply current, where self-heating can increase junction temperature and must be monitored appropriately.

APPLICATIONS INFORMATION

Thermal Management

PCB Thermal Design

The ADHV4710's innovative EPAD-up package greatly reduces thermal management constraints on the PCB layout. Conventional EPAD-down packages require copper-filled vias or expensive solid copper coins pressed into the PCB for thermal conduction to a heat sink on the underside of the board. EPAD-up allows the heat sink to be mounted to the top of the ADHV4710, freeing up component space on the secondary side of the PCB, and eliminating the need for through-board thermal relief. Four small mounting holes are needed to secure the recommended heat sink to the PCB, and these are located outside of the ADHV4710's immediate area. Component heights on the primary side of the PCB in the area beneath the heat sink must be smaller than the minimum height of the ADHV4710, as illustrated in *Figure 72*.

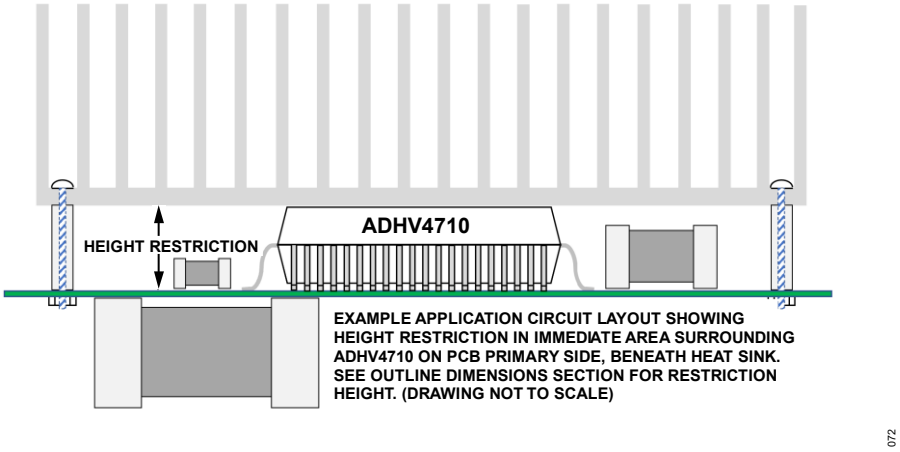

Figure 72. Component Height Restriction Beneath Heat Sink

To maximize heat transfer, attach the heat sink to the EPAD, as shown in *Figure 72*, using a high conductivity thermal interface material (TIM).

Power Dissipation

Under quiescent conditions and maximum supply voltage, with the default heat sink, the ADHV4710 dissipates ~2.67W, which produces a 17.355°C rise over ambient temperature.

Under heavier loading conditions, the increase in die temperature is greater. It is recommended that T_J be continuously monitored at the TMP pin to manage die temperature under different internal power dissipation levels. Alternatively, when operating at a constant power level, die temperature can be estimated based on the package's θ_{JA} of 25.4°C/watt when operating without a heatsink. Where the thermal setup of the ADHV4710 utilizes a heatsink, one should expect to have a junction-to-ambient thermal resistance θ_{JA_SYSTEM} (with recommended heatsink Wakefield-Vette P/N 518-95AB and TIM GC Electronics type Z9 heat sink compound) of 6.5°C/watt. The following equation is the basic formula used for calculating junction temperature for a specific power dissipation and ambient temperature.

$$T_J = \theta_{JA\_SYSTEM} \times P_{DISS} + T_A$$

For example, if dissipating 10W internally at an ambient temperature of 25°C with a heatsink and TIM in the thermal stackup for the EVAL-ADHV4710SDZ, T_J can be expected to climb to:

$$25°C + (6.5°C/W \times 10W) = 90°C$$

Note that ~ 19.2W internal power dissipation pushes T_J to its maximum rated value of 150°C when using default heatsink in an environment with natural convection.

Thermal resistance values effectively show how much a certain portion of a thermal stackup heats up for a specified power dissipation. The following equations are the basic equations for determining the junction-to-ambient thermal resistance for a thermal stackup that uses thermal paste and heatsink. The θ_{JA_SYSTEM} should be designed to meet the user's thermal requirements. Using the junction-to-case thermal resistance (θ_{JC}) and thermal resistance of the thermal interface material (θ_{TIM}), compute the thermal resistance (θ_{HS}) of the required heat sink with the following equation.

$$\theta_{HS} = \left(\frac{T_J - T_A}{P_{DISS}}\right) - \left(\theta_{JC} + \theta_{TIM}\right)$$

$$\theta_{JA\_SYSTEM} = \theta_{HS} + \theta_{JC} + \theta_{TIM}$$

High-performance applications involving maximum power delivery at high duty cycles may require active cooling to effectively reduce θ_{JA_SYSTEM} and continuously monitor T_J.

For lower power applications, or if forced air convection is used, a smaller heat sink may be sufficient.

Table 12 shows the thermal resistances for different conditions when using the evaluation board, EVAL-ADHV4710SDZ at T_A = 25 °C. The fan used is the Sunon Fans EE80251S2-1000U-999 with air flow of 37 CFM into the heatsink. The heatsink used is the Wakefield-Vette P/N 518-95AB. The TIM is the GC Electronics type Z9 heat sink compound.

Table 12. θ_{JA_SYSTEM} for Different Thermal Stackups on the EVAL-ADHV4710SDZ

Heatsink	Vertical Fin Airflow	θ_(JA_SYSTEM) (°C/W)
No	No	25.4
Yes	No	6.5
	Yes	4.5

Safe Operating Area

The safe operating area (SOA) represents the power handling capability of the device under various conditions. The power dissipation of the ADHV4710 occurs primarily from the slew boosting circuit and output stage. The SOA curves are unique to the conditions under which they are developed, such as PCB, heat sink, airflow, and ambient temperatures. In addition, all SOA curves are derated and are with respect to hotspots on the die. See the *Thermal Gradient* section for more information about hotspots. To preserve the lifespan of the silicon, it is recommended to utilize the SOA plots to estimate an optimal temperature for each specific application. Ensure that usage of the ADHV4710 remains within the published DC SOA and Dynamic SOA curves while also monitoring the junction temperature using the TMP pin voltage ($V_{TMP} \leq 2.5V$).

Long-term usage of the ADHV4710 at or near maximum junction temperature of 150°C may result in a reduction of expected lifespan of the product due to accelerated thermal stresses.

See *LTspice Support Models* for *more* information about simulation tools to aid in power dissipation analysis and thermal design.

DC SOA

Figure 73 shows that the DC safe operating area (SOA) is a curve of output current vs. output stage supply voltage differential (V_S to V_{OUT}), under which the amplifier can operate at a safe junction temperature (T_J). The area under the curves of *Figure 73* shows the operational boundaries of the ADHV4710 for using the ADHV4710 evaluation board that maintains a $T_J \leq 150°C$.

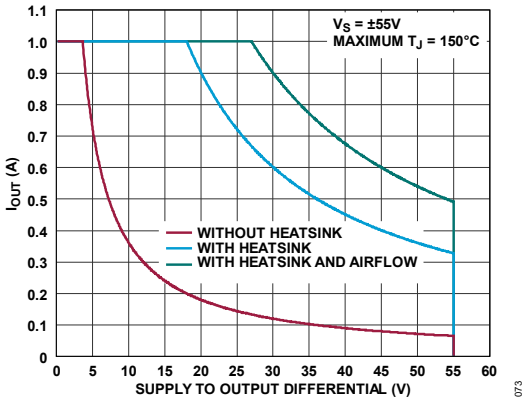

Figure 73. DC SOA Without Heatsink, with Default Heatsink, with Default Heatsink and Fan, T_A = 25°C

All testing was done in the natural convection of a lab. Forced air convection in any of the test cases effectively lowers θ_{JA_SYSTEM} and moves the corresponding curve toward the upper right, expanding the SOA. For more information on the ADHV4710 evaluation board, refer to the ADHV4710 user guide. In *Figure 73*, the horizontal line at 1A is the output current drive of the ADHV4710. The curved section maintains a fixed power dissipation that results in a junction temperature (T_J) of 150°C or less. Note that *Figure 73* shows the maximum V_S to V_{OUT} differential and output current the ADHV4710 can handle in addition to the quiescent power dissipation. Also, the x-axis is the output stage V_S to V_{OUT} differential (HVCC − V_{OUT} or V_{OUT} − HVEE) developed across the relevant output transistor and ends at a maximum V_S to V_{OUT} differential of 55V.

Dynamic SOA

Figure 74 illustrates the maximum square-wave amplitude that can be generated continuously without exceeding absolute maximum temperature, plotted versus frequency with a specified capacitive load and specified heat sink.

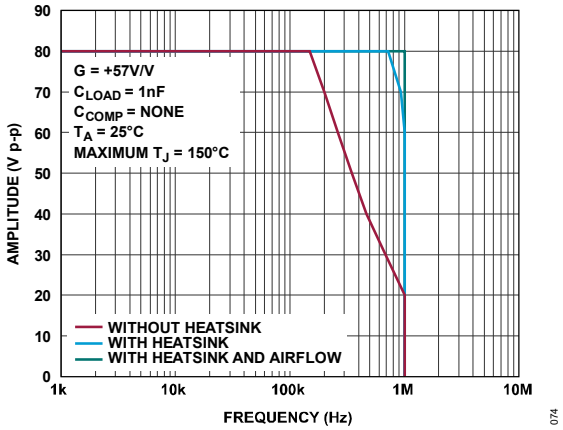

Figure 74. Dynamic SOA without Heatsink, with Default Heatsink, with Default Heatsink and Fan, C_{LOAD} = 1 nF, T_A = 25 °C

Figure 75, *Figure 76*, and *Figure 77* show how the dynamic supply current during high-slew transitions changes with amplitude and frequency. The *Slew Boost* section discusses how the ADHV4710 consumes significant dynamic supply current during high-slew transitions. Above a particular frequency (load-dependent), the electrical power consumption required to slew ±full scale exceeds the system's ability to dissipate enough power to keep T_J below the absolute maximum junction temperature. Additional thermal management can be leveraged to expand the SOA.

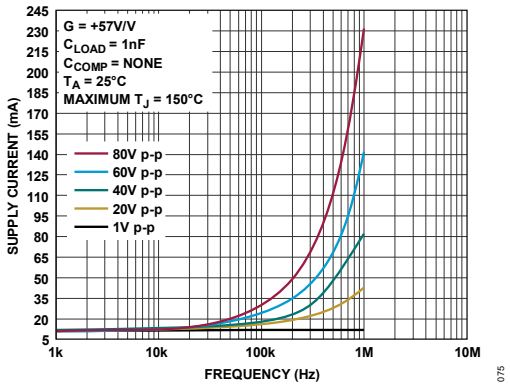

Figure 75. Supply Current and Amplitude vs. Frequency Square Wave, with Heatsink and Airflow, C_{LOAD} = 1nF, C_{COMP} = None

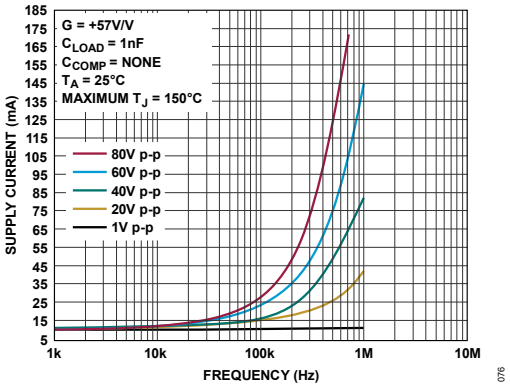

Figure 76. Supply Current and Amplitude vs. Frequency Square Wave, with Heatsink, C_{LOAD} = 1nF, C_{COMP} = None

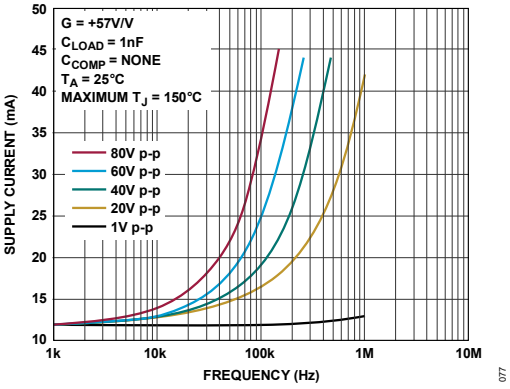

Figure 77. Supply Current and Amplitude vs. Frequency, Square Wave, No Heatsink, C_{LOAD} = 1nF, C_{COMP} = None

Thermal Gradient

Typically, it is assumed the power dissipation is uniform across the whole die of a part, but, the reality is that the power dissipation is typically concentrated in certain areas based on the application. Hotspots are locations within the die of a part that are at a higher temperature in comparison to the temperature sensor reading. In high power applications, the output stage of an amplifier is where the hotspots commonly exist, as the output stage transistors are where power is dissipated when driving a load. As seen in *Figure 78*, this behavior is seen within the ADHV4710 and should be considered for junction temperature and power dissipation calculations.

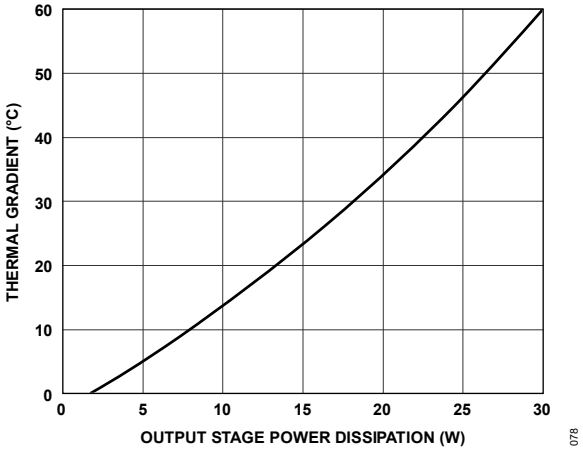

Figure 78. Thermal Gradient vs Temperature Sensor

The following equation is the basic formula used for calculating the output power stage hotspot for a specific temperature sensor reading and power dissipation:

$$T_{HOTSPOT} = T_{SENSOR} + T_{GRADIENT}$$

For example, using *Figure 78*, if dissipating an output stage power dissipation of 22.5W with a temperature sensor reading of 60°C and thermal gradient 40°C, $T_{HOTSPOT}$ can be expected to be the following:

$$60°C + 40°C = 100°C$$

Protecting the ADHV4710

Short Circuit Precaution

Extreme caution must be taken if the output of the ADHV4710 is shorted to ground or through a low impedance. To help protect against short circuit stresses, it is recommended to program overcurrent protection. The internal overcurrent protection shutdown has a finite time delay depending upon the capacitance on the SDN_IO pin. During this time, high peak currents can occur, which can cause overstress. This can exceed the rated peak instantaneous output current drive and violates the safe operating area (SOA). In many applications, this peak instantaneous current is limited by a series resistor used for measuring current into the load and with connecting lead inductance helps limit this peak current. As another precaution, it is recommended, if possible, to reduce peak instantaneous power through a current limit on the external high voltage power supplies to HVCC and HVEE. In the event of an overcurrent induced shutdown, the input differential voltage from INP to INN must be limited to maintain shutdown and prevent output current delivery (as described in the *Shutdown/Sleep Precaution* section).

Shutdown/Sleep Precaution

When the ADHV4710 is in shutdown mode or sleep mode (as described in the *Shutdown and Sleep Control* section), it is recommended to disable the input to the ADHV4710. If a large input differential voltage greater than ~1.5V is presented across inputs INP to INN while in shutdown mode or sleep mode, the output of the amplifier may leave its high impedance state, resulting in output voltage and current drive at the output. To avoid this condition, it is recommended to turn off or limit the input to the ADHV4710 when the part is placed in shutdown mode or sleep mode.

Limiting Input Differential Voltage During Shutdown/Sleep

As discussed in the *Shutdown/Sleep Precaution* section, the input differential voltage should be limited to ~1.5V or less across inputs during shutdown/sleep. One option for achieving this is to use a set of anti-parallel diodes between inputs INP and INN to limit input differential voltage and ensure proper shutdown and sleep behavior regardless of input conditions while the part is in shutdown. Placing diodes across the input limits the maximum input differential voltage for slew boost when enabled, limiting the maximum slew rate of the ADHV4710. Selecting fast-switching diodes with a singular or combined forward voltage not exceeding 1.5V is recommended to obtain the maximum limited slew rate in this configuration. *Figure 79* shows how to implement the anti-parallel diodes across the inputs. *Figure 80* and *Figure 81* show the pulse responses of the ADHV4710 with anti-parallel diode configurations. The diode array parts used for these tests is the BAV99L with forward voltage values of 715mV$_{DC}$.

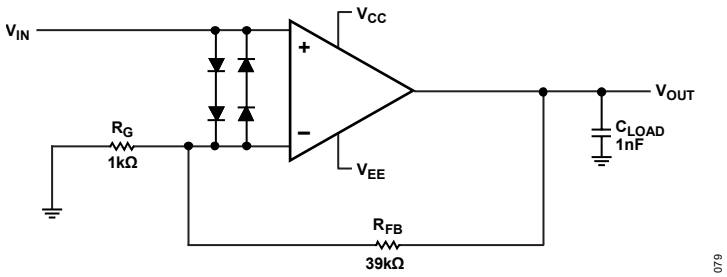

Figure 79. Schematic of an Anti-Parallel Diode Placement Between INP and INN

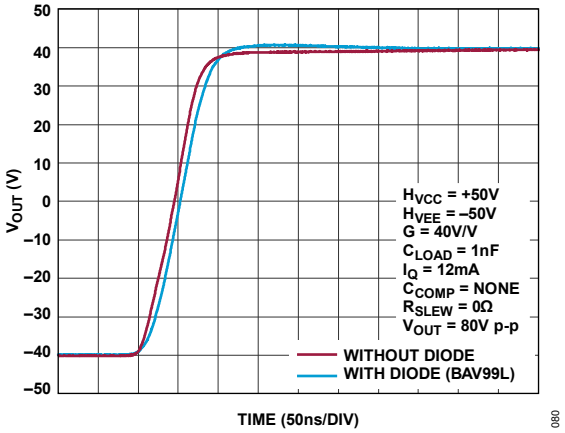

Figure 80. Large Signal Step Response vs Various Input Anti-Parallel Diode Combinations, Rising Edge

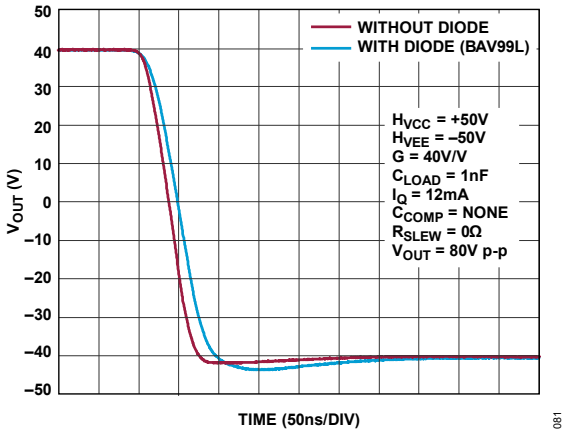

Figure 81. Large Signal Step Response vs Various Input Anti-Parallel Diode Combinations, Falling Edge

Overcurrent Threshold Errors

When utilizing the overcurrent protection features with the ADHV4710, there are cases in which the trip-point thresholds can differ from the ideal values calculated in the *Shutdown Protection Settings* section. These should be taken into consideration for applications that rely on the shutdown protection features of the ADHV4710.

Overcurrent Threshold Errors with Headroom

As seen in in the *Fault-Initiated Shutdown Protection Features* section, the ADHV4710 can be programmed to shut down with overcurrent conditions up to ±1 A. That said, additional headroom is needed to reliably trigger the overcurrent protection. *Figure 82* and *Figure 83* show how the overcurrent setpoint accuracy degrades at 500mA as headroom is reduced. Data with setpoint error higher than 7% was not taken as it continued to degrade significantly.

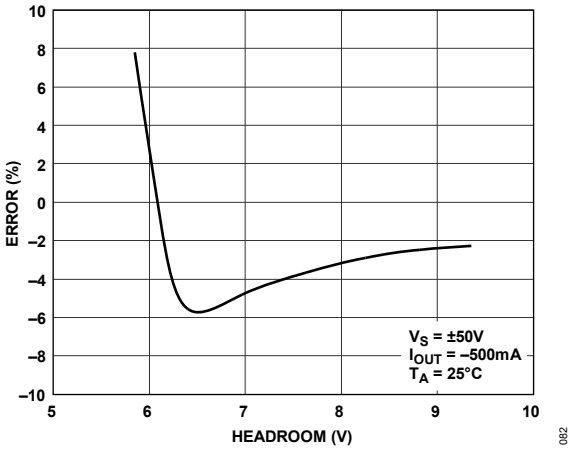

Figure 82. Source, DC Overcurrent Setpoint Error vs. Headroom, T_A = 25 °C

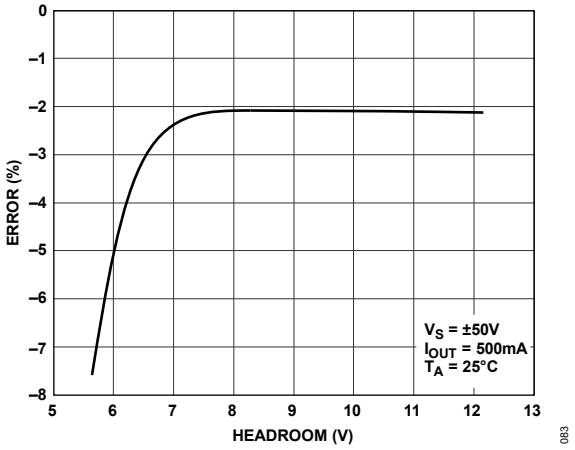

Figure 83. Sink, DC Overcurrent Setpoint Error vs. Headroom, T_A = 25 °C

Figure 56 shows that the headroom of the ADHV4710 increases with output current and temperature. Similarly, the additional headroom needed to reliably trigger the overcurrent protection also increases with output current and temperature. *Table 13* shows the recommended headroom needed to reliably activate overcurrent protection across different output currents at T_J = 150 °C.

Table 13. Recommended Headroom for Reliable Overcurrent Trip-Point Thresholds, T_J = 150 °C

Current Direction	Output Current (A)	Recommended Headroom (V)
Source	0.5	5.4
	1.0	9.0
Sink	0.5	9.5
	1.0	18.6

Limiting Dynamic Peak Current for >1nF Loads

The ADHV4710 can drive 1A continuously by design, assuming appropriate thermal management, as outlined in the *Thermal Management* section.

The ADHV4710 is also qualified to drive 80Vp-p square-wave pulses into a 1nF load at 1kHz without external compensation or slew control. This corresponds to ±1.13 A peak, with a ~100ns current pulse width at 0.5ms intervals, as specified in the electrical characteristics. If the peak power dissipations defined by the qualified device conditions are exceeded, the excessive peak power dissipations can shorten the lifespan of the ADHV4710.

If driving pulses into >1nF loads, to remain within the qualified device conditions, the peak current should be limited to the continuous output current drive of 1A. To ensure this, the user must control the input slew rate to limit the peak current when driving these loads.

The current into a capacitor can be calculated using the formula:

$$I = C\frac{dV}{dt}$$

This generates the following table of maximum slew rate that ensures a peak current of ≤ 1A.

Table 14. Maximum Slew vs. Capacitive Load

Capacitance	Maximum Slew Rate
1nF	1000V/µs
10nF	100V/µs
22nF	45V/µs
47nF	21V/µs
100nF	10V/µs

Performance Impacts of Adjusting R_{SLEW}, C_{COMP}, and SET_IQ

The ADHV4710's performance can be adjusted, through the change of R_{SLEW}, C_{COMP}, and/or SET_IQ, to allow for the best application performance based on gain and capacitive load. *Table 7* shows recommended compensation to maintain small signal stability for various C_{LOAD}. *Table 15* shows an overview of the performance changes by increasing R_{SLEW}, C_{COMP}, and/or SET_IQ from R_{SLEW} = 0Ω, C_{COMP} = 0pF, and SET_IQ = 0x00 (I_Q ≈ 12mA). See the *Typical Performance Characteristics* section for data on the performance impacts of R_{SLEW}, C_{COMP}, and/or SET_IQ.

To properly choose R_{SLEW} and C_{COMP} for small signal stability analysis, start with a desired gain. Second, choose an appropriate R_{SLEW} for the chosen gain. Then, adjust C_{COMP} as necessary to achieve the desired phase margin. Phase margin can be quickly analyzed with simulations using the LTspice model of the ADHV4710.

See the *LTspice Support Models* section for more information.

Table 15. R_{SLEW}, C_{COMP}, SET_IQ Adjustments and Performance Impacts

Specification	Increasing R_{SLEW}	Increasing SET_IQ	Increasing COMP_L, COMP_H
Slew Rate	Decreases	Increases	Decreases
Open-Loop Gain	Shifts DC A_{OL} Down, Same Low Frequency Pole	No Effect	Lowers A_{OL} Low Frequency Pole
Closed-Loop Output Impedance	Minimal Effect	Decreases	Decreases
Voltage Noise Spectral Density, RTI	Increases	Minimal Effect	No Effect
Current Noise Spectral Density, RTI	No Effect	No Effect	No Effect
Offset Voltage, RTI	Increases	Increases	No Effect
Offset Voltage Drift, RTI	Increases	Increases	No Effect
Common-Mode Rejection Ratio	Shifts DC CMRR Down, Same Low Frequency Pole	No Effect	Lowers CMRR Low Frequency Pole
Power Supply Rejection Ratio	Shifts DC PSRR Down, Same Low Frequency Pole	No Effect	Lowers PSRR Low Frequency Pole

Component Considerations for High Voltage, High Current Amplifiers

High voltage and high current power operational amplifiers require additional component considerations when compared to a typical small-signal op amp application.

Resistors used for feedback and input gain setting should be analyzed for their respective maximum voltage drop, under the highest stress condition. Based on resistor maximum voltage, one can compute worst-case power dissipation and size the resistor accordingly. In addition, voltage rating, voltage coefficient of resistance, and temperature coefficient of resistance should be checked for acceptable resistance changes in the application.

Capacitors should be checked for voltage across them, under the highest stress condition. Based on capacitor maximum voltage, the appropriate capacitor should be selected. In addition, the voltage and temperature coefficient of capacitance should be checked for acceptable capacitance change with applied maximum voltage.

Any external diodes must also be analyzed for reverse breakdown voltage, reverse leakage current, off-capacitance, forward current capability, and forward voltage drop. For all component parameters, respective temperature coefficients should be analyzed, to account for expected changes over the application's operating temperature range.

Worst-case stresses can be easily analyzed with simulations using the LTspice model of the ADHV4710. See the *LTspice Support Models* section for more information.

Layout

When designing the PCB, it is important to incorporate thermal layout techniques in addition to the standard electrical layout practices. Thermal considerations involve attention to trace thickness, thermal vias, ground and power layers, and large copper pours for power supply areas to prevent excessive power dissipation on PCBs. The high voltage power supply lines (HVCC, HVEE) should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. With high current designs, low impedance paths are important for preventing unwanted circuit voltage drops. Power supply planes should be considered for low impedance connections to all components on the PCBs. For high frequency design, short and wide traces should be used to minimize inductance to allow for low trace impedance across a wide range of frequencies.

Decouple the power supply (HVCC, HVEE, VCC_5V, and VREF_5V) PCB entry points with bulk capacitance. It is recommended to use 5µF, or greater, per peak amp of current for these capacitors.

Directly at the pins of the ADHV4710, use four 0.1µF bypass capacitors for good high frequency decoupling. Connect these capacitors using short and wide traces to provide low impedance paths and reduce the effect of glitches on the power supply lines. Lower ESR, ESL decoupling capacitors on HVCC, HVEE pins reduce voltage ripple and glitches. For supplies with multiple pins (HVCC, HVEE), it is recommended that these pins be tied together with a common copper pour and that each copper pour be decoupled only once. Place these capacitors on the same side of the board as the ADHV4710 and as close as possible to the amplifier power supply pins with the ground end of the capacitor directly to the ground plane.

High voltage PCB traces must be spaced at proper distances to meet clearance and creepage application requirements to prevent electrical breakdown and to provide increased protection against electric shock.

Because this product has analog and digital functions, it is important to separate and confine the analog and digital sections to certain areas of the PCB proximal to the ADHV4710. Allow the analog ground plane to run under the ADHV4710 to avoid noise coupling. Avoid running digital lines under the ADHV4710 because these couple noise onto the die, unless there is a ground plane acting as shield. Fast switching digital signals such as clock should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the analog traces. Traces on adjacent PCB layers should run at right angles to each other to reduce effects from coupling and feedthrough throughout the board. Avoid crossover of digital and analog signals. Use at least one

ground plane, and it can be common or split between the digital and analog section. In the latter case, join the planes underneath the ADHV4710 devices.

LTspice Support Models

There are two separate LTspice models available to support the ADHV4710, an electrical model and a thermal model.

The LTspice electrical model can be found by using the latest *LTspice* version. Be sure to perform an "update components" function and then the LTspice components library contains the ADHV4710 LTspice electrical model. A "Quick Start User Guide" for the ADHV4710 electrical model is available at *https://wiki.analog.com/resources/quick-start*, under the *ADHV4710 model* link. It is highly encouraged to review the "Quick Start User Guide" first, before using the ADHV4710 electrical model, as it details what is and is not modeled, and contains some pre-canned example circuit descriptions for definition by example use of the model. All LTspice circuits used in the guide are downloadable for use.

A second order, steady-state thermal model is available at *https://wiki.analog.com/resources/quick-start*, under the *power op-amp thermal model* link. Under the same link is a "Quick Start User Guide". It is highly encouraged to review the "Quick Start User Guide" first, before using the ADHV4710 thermal model, as it details what is and is not modeled, and contains detailed definition by example uses of the model. All LTspice circuits used in the guide are downloadable for use.

TOP LEVEL DIGITAL REGISTER ASSIGNMENT

Table 16. Digital Register Map Instance Summary

Name	Module	Address
ADHV4710_CTRL_REGMAP	ADHV4710_CTRL_REGMAP	0x00
ADHV4710_CALIBRATION_FACTORS_REGMAP	RESERVED	0x20
ADHV4710_CALIBRATION_CTRL_REGMAP	RESERVED	0x40
ADHV4710_ DATA_REGMAP	RESERVED	0x60

DEVICE CONTROL REGISTER SUMMARY AND MAP

Note: R/W means read and write; R/CLR means read and clear; R means read only. See the *Fault Monitoring and Protection* section for a description of R/CLR.

Table 17. Control Register Summary

Address	Name	Description	Reset	Access
0x00	CTRL_REG_00	General device control registers. See *Table 18.*	0x10	R/W
0x01 to 0x02	CTRL_REG_01 - CTRL_REG_02	Reserved	0x08	
0x03	CTRL_REG_03	General device control registers. See *Table 18.*	0x00	R/W
0x04	CTRL_REG_04	General device control registers. See *Table 18.*	0x00	R/W
0x05 to 0x07	CTRL_REG_05 - CTRL_REG_07	Reserved		
0x08	CTRL_REG_08	General device control registers. See *Table 18.*	0x00	R/W
0x09	CTRL_REG_09	General device control registers. See *Table 18.*	0x00	R/W
0x0A	CTRL_REG_10	General device control registers. See *Table 18.*	0x00	R/W
0x0B	CTRL_REG_11	General device control registers. See *Table 18.*	0x00	R/W
0x0C	CTRL_REG_12	General device control registers. See *Table 18.*	0x00	R/W
0x0D	CTRL_REG_13	General device control registers. See *Table 18.*	0x00	R/W
0x0E	CTRL_REG_14	General device control registers. See *Table 18.*	0x00	R/CLR
0x0F to 0x18	CTRL_REG_15 to CTRL_REG_24	Reserved		
0x19	CTRL_REG_25	General device control registers. See *Table 18.*	0x00	R
0x1A	CTRL_REG_26	General device control registers. See *Table 18.*	0x46	R

Table 18. Control Register Map

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	CTRL_REG_00	[7:0]	HV_RESET	RESERVED		HV_SLEEP	RESERVED				0x10	R/W
0x03	CTRL_REG_03	[7:0]	RESERVED							SOFT_RESET	0x00	R/W
0x04	CTRL_REG_04	[7:0]	SET_IQ								0x00	R/W

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x08	CTRL_ REG_08	[7:0]	OC_SRC_ARM	OC_SRC_LIMIT							0x00	R/W
0x09	CTRL_ REG_09	[7:0]	OC_SNK_ARM	OC_SNK_LIMIT							0x00	R/W
0x0A	CTRL_ REG_10	[7:0]	OV_POS_ARM	OV_POS_LIMIT							0x00	R/W
0x0B	CTRL_ REG_11	[7:0]	OV_NEG_ARM	OV_NEG_LIMIT							0x00	R/W
0x0C	CTRL_ REG_12	[7:0]	OT_ARM	OT_LIMIT							0x00	R/W
0x0D	CTRL_ REG_13	[7:0]	RESERVED			OC_SRC_ ALARM_ LATCH	OC_SNK_ ALARM_ LATCH	OV_POS_ ALARM_ LATCH	OV_NEG_ ALARM_ LATCH	OT_ALARM_ LATCH	0x00	R/W
0x0E	CTRL_ REG_14	[7:0]	SHUTDOWN_ FLAG	RESERVED		OC_SRC_ ALARM	OC_SNK_ ALARM	OV_POS_ ALARM	OV_NEG_ ALARM	OT_ ALARM	0x00	R/ CLR
0x19	CTRL_ REG_25	[7:0]	RESERVED				DIE_REV				0x04	R
0x1A	CTRL_ REG_26	[7:0]	CHIP_ID								0x46	R

Control Register Details

Table 19. Bit Descriptions for CTRL_REG_00

Bits	Bit Name	Description	Reset	Access
7	HV_RESET	Reset shutdown latch. (0) Default: No reset. Shutdown can occur. (1) Clear shutdown latch and re-enable amplifier from shutdown. Not self-clearing: to reset write “1” then “0”, else shutdown is suppressed while reset is enabled.	0x0	R/W
[6:5]	RESERVED	Reserved. Do not write.		
4	HV_SLEEP	Shutdown amplifier. (0) Amplifier is shutdown. HV quiescent current decreases, and output of amplifier is floating (high impedance). This overrides all other mechanisms (SDN_IO and protection features). (1) Default: Amplifier is enabled but can still be shutdown through other mechanisms (SDN_IO and protection features).	0x1	R/W
[3:0]	RESERVED	Reserved. Do not write.		

Table 20. Bit Descriptions for CTRL_REG_03

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved. Do not write.		
0	SOFT_RESET	Reset digital engine. (0) Default: Digital engine active (1) Clear all register values (including this one, self-clearing) and initiate reboot sequence of digital engine.	0x0	R/W

Table 21. Bit Descriptions for CTRL_REG_04

Bits	Bit Name	Description	Reset	Access
[7:0]	SET_IQ	Program quiescent current of amplifier. Default of 0x0 puts part at nominal supply current. Bit 7 (MSB) is polarity bit: (0) is quiescent current reduction, (1) is quiescent current increase. Bits 6:0 are monotonic but nonlinear change to supply current. See *Programmable Quiescent Current*.	0x0	R/W

Table 22. Bit Descriptions for CTRL_REG_08

Bits	Bit Name	Description	Reset	Access
7	OC_SRC_ARM	Enable overcurrent (source) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring output source current.	0x0	R/W
[6:0]	OC_SRC_LIMIT	Set level of overcurrent (source) protection. See *Programming Overcurrent Protection.*	0x0	R/W

Table 23. Bit Descriptions for CTRL_REG_09

Bits	Bit Name	Description	Reset	Access
7	OC_SNK_ARM	Enable overcurrent (sink) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring output sink current.	0x0	R/W
[6:0]	OC_SNK_LIMIT	Set level of overcurrent (sink) protection. See *Programming Overcurrent Protection.*	0x0	R/W

Table 24. Bit Descriptions for CTRL_REG_10

Bits	Bit Name	Description	Reset	Access
7	OV_POS_ARM	Enable overvoltage (positive) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring positive output voltage.	0x0	R/W
[6:0]	OV_POS_LIMIT	Set level of overvoltage (positive) protection. See *Programming Overvoltage Protection*	0x0	R/W

Table 25. Bit Descriptions for CTRL_REG_11

Bits	Bit Name	Description	Reset	Access
7	OV_NEG_ARM	Enable overvoltage (negative) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring negative output voltage.	0x0	R/W
[6:0]	OV_NEG_LIMIT	Set level of overvoltage (negative) protection. See *Programming Overvoltage Protection*	0x0	R/W

Table 26. Bit Descriptions for CTRL_REG_12

Bits	Bit Name	Description	Reset	Access
7	OT_ARM	Enable overtemperature (T_J) protection. (0) Default: Protection is disabled. (1) Protection is enabled, monitoring junction temperature.	0x0	R/W
[6:0]	OT_LIMIT	Set level of overtemperature (T_J) protection. See *Programming Overtemperature Protection.*	0x0	R/W

Table 27. Bit Descriptions for CTRL_REG_13

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved. Do not write.		
4	OC_SRC_ALARM_LATCH	Enable overcurrent (source) alarm latch. (0) Default: Latch is disabled. OC_SRC_ALARM self-clears if overcurrent (source) fault clears. (1) Enable latch of OC_SRC_ALARM flag, latched high If overcurrent (source) fault detected.	0x0	R/W
3	OC_SNK_ALARM_LATCH	Enable overcurrent (sink) alarm latch. (0) Default: Latch is disabled. OC_SNK_ALARM self-clears if overcurrent (sink) fault clears. (1) Enable latch of OC_SNK_ALARM flag, latched high If overcurrent (sink) fault detected.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
2	OV_POS_ALARM_LATCH	Enable overvoltage (positive) alarm latch. (0) Default: Latch is disabled. OV_POS_ALARM self-clears if overvoltage (positive) fault clears. (1) Enable latch of OV_POS_ALARM flag, latched high If overvoltage (positive) fault detected.	0x0	R/W
1	OV_NEG_ALARM_LATCH	Enable overvoltage (negative) alarm latch. (0) Default: Latch is disabled. OV_NEG_ALARM self-clears if overvoltage (negative) fault clears. (1) Enable latch of OV_NEG_ALARM flag, latched high If overvoltage (negative) fault detected.	0x0	R/W
0	OT_ALARM_LATCH	Enable overtemperature (T_J) alarm latch. (0) Default: Latch is disabled. OT_ALARM self-clears if overtemperature (T_J) fault clears. (1) Enable latch of OT_ALARM flag, latched high If overtemperature (T_J) fault detected.	0x0	R/W

Table 28. Bit Descriptions for CTRL_REG_14

Bits	Bit Name	Description	Reset	Access[1]
7	SHUTDOWN_FLAG	Indicates shutdown state. (0) Default: Amplifier is enabled. (1) Amplifier is shutdown.	0x0	R
[6:5]	RESERVED	Reserved. Do not write.		
4	OC_SRC_ALARM	Overcurrent (source) alarm flag. (1) Indicates overcurrent (source) fault event. If latched, write to clear.	0x0	R/CLR
3	OC_SNK_ALARM	Overcurrent (sink) alarm flag. (1) Indicates overcurrent (sink) fault event. If latched, write to clear.	0x0	R/CLR
2	OV_POS_ALARM	Overvoltage (positive) alarm flag. (1) Indicates overvoltage (positive) fault event. If latched, write to clear.	0x0	R/CLR
1	OV_NEG_ALARM	Overvoltage (negative) alarm flag. (1) Indicates overvoltage (negative) fault event. If latched, write to clear.	0x0	R/CLR
0	OT_ALARM	Overtemperature (T_J) alarm flag. (1) Indicates overtemperature (T_J) fault event. If latched, write to clear.	0x0	R/CLR

Table 29. Bit Descriptions for CTRL_REG_25

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved. Do not write.		
[3:0]	DIE_REV	Register indicating ADHV4710 silicon revision.	0x4	R

Table 30. Bit Descriptions for CTRL_REG_26

Bits	Bit Name	Description	Reset	Access
[7:0]	CHIP_ID	Register indicating chip ID of ADHV4710.	0x47	R

[1] CLR denotes that an alarm flag is cleared by writing a '1' to the corresponding register bit.

OUTLINE DIMENSIONS

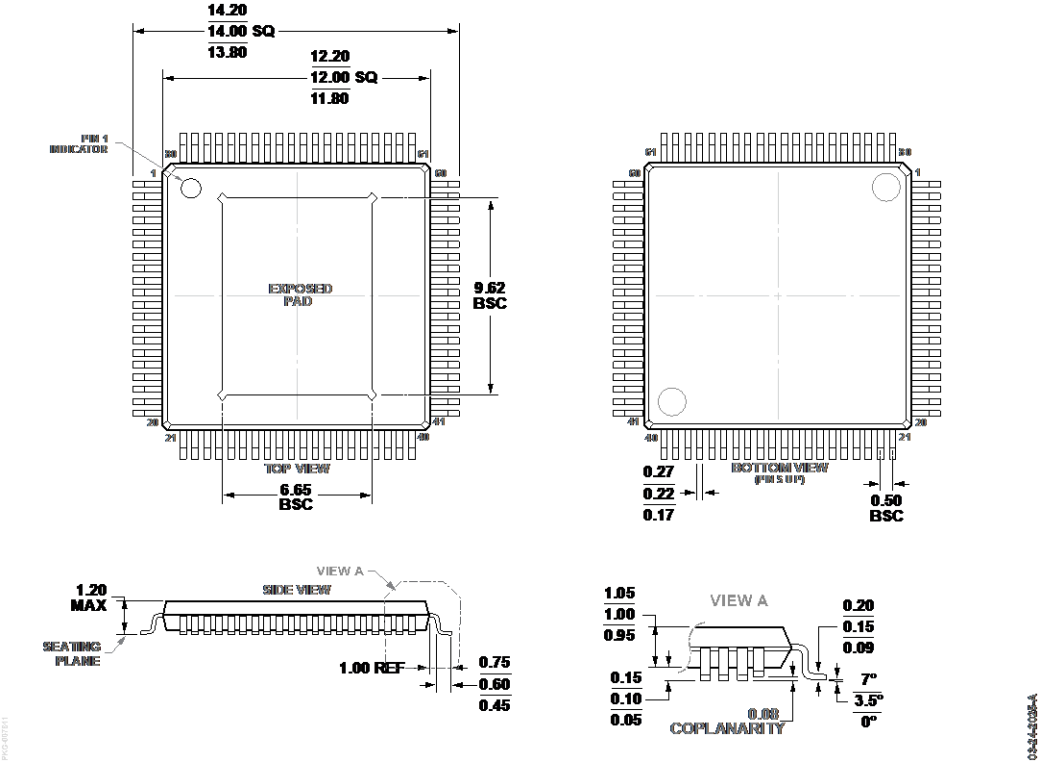

Figure 84. 80-Lead Thin Quad Flat Package, Exposed Pad TQFP, SV-80-7, Dimensions shown in milimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Packing Quantity	Package Option
ADHV4710BSVZ	-40°C to 85°C	80-Lead TQFP		SV-80-7
ADHV4710BSVZ-RL	-40°C to 85°C	80-Lead TQFP	1000	SV-80-7

EVALUATION BOARD

Model	Description
EVAL-ADHV4710SDZ	Evaluation Board for 80-Lead Thin Quad Flat Package

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADHV4710BSVZ-RL ADHV4710BSVZ EVAL-ADHV4710SDZ