Data Sheet

ADA4352-2

Compact, Dual-Channel, Precision, Programmable Gain Transimpedance Amplifier (PGTIA) with Integrated Gain Resistors

FEATURES

- Small, dual-channel, complete PGTIA and AFE solution.
- Small size package: **16-lead LFCSP, 3 mm × 3 mm.**
- Four integrated internal gain resistors (R_F) per channel:
  - Range 0, internal R_{F0} = 315 Ω
  - Range 1, internal R_{F1} = 3.5 kΩ
  - Range 2, internal R_{F2} = 40.2 kΩ
  - Range 3, internal R_{F3} = 450 kΩ
- Wide input current dynamic ranges from 100 picoamps to milliamps.
- Excellent DC precision:
  - Low offset voltage RTI: ±100 µV maximum, 25°C.
  - Low input offset voltage drift: ±1.0 µV/°C maximum, −40°C to +125°C.
  - Low switch integrated switch impedance 19 Ω maximum, −40°C to +125°C.
- Excellent dynamic performance:
  - Range 0 settling time 1 µs
  - Range 1 settling time 2 µs
  - Range 2 settling time 5 µs
  - Range 3 settling time 10 µs
- Kelvin-connected architecture eliminates gain error due to switch on-resistance over temperature.
- Single-supply operation: +2.7 V to +5.5 V (dual-supply operation: ±1.85 V to ±2.75 V).
- Wide gain bandwidth product: 8.5 MHz.
- Wide operating temperature range: −40°C to +125°C.

APPLICATIONS

- Precision current to voltage (I to V) conversion
- Programmable gain TIAs
- Photodetector interface and amplification
- Optical networking equipment
- Optical power measurement
- Instrumentation (spectroscopy and chromatography)

GENERAL DESCRIPTION

The ADA4352-2 is a compact, monolithic, dual-channel, precision, programmable gain transimpedance amplifier (PGTIA). The ADA4352-2 is a breakthrough solution to precisely measure small currents over a wide dynamic range. The precision of the ADA4352-2 over a wide temperature range of −40°C to +125°C allows one calibration of the end equipment at room temperature, thereby saving test time and cost. The ADA4352-2 integrates four current-to-voltage gain selections per channel, and the gain is programmable using two logic pins per channel to provide a flexible, fully functional compact PGTIA solution. Additionally, with its robust output stage and low noise, the ADA4352-2 can directly drive 16-bit precision analog-to-digital converters (ADCs) such as the *AD4696*, providing a complete analog front-end (AFE) to address the most challenging wide dynamic range current measurement applications.

The ADA4352-2 is offered in a **3 mm × 3 mm LFCSP**, reducing the printed circuit board (PCB) area by up to ten times relative to a discrete design using standalone operational amplifiers (op amps) and switches.

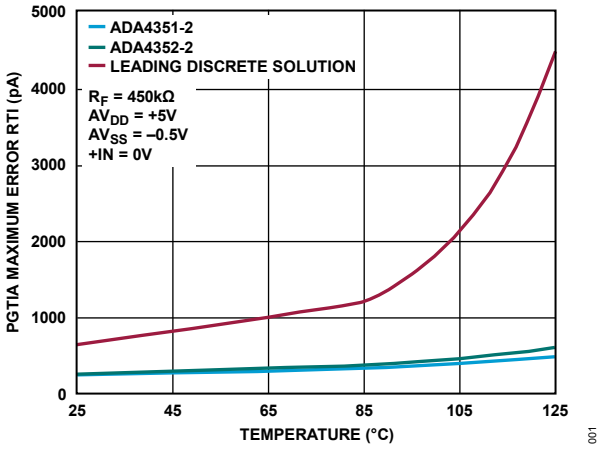

Figure 1. PGTIA Maximum Error vs. Temperature

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Compact, Dual-Channel, Precision, Programmable Gain Transimpedance Amplifier (PGTIA) with Integrated Gain Resistors

SIMPLIFIED APPLICATION DIAGRAM

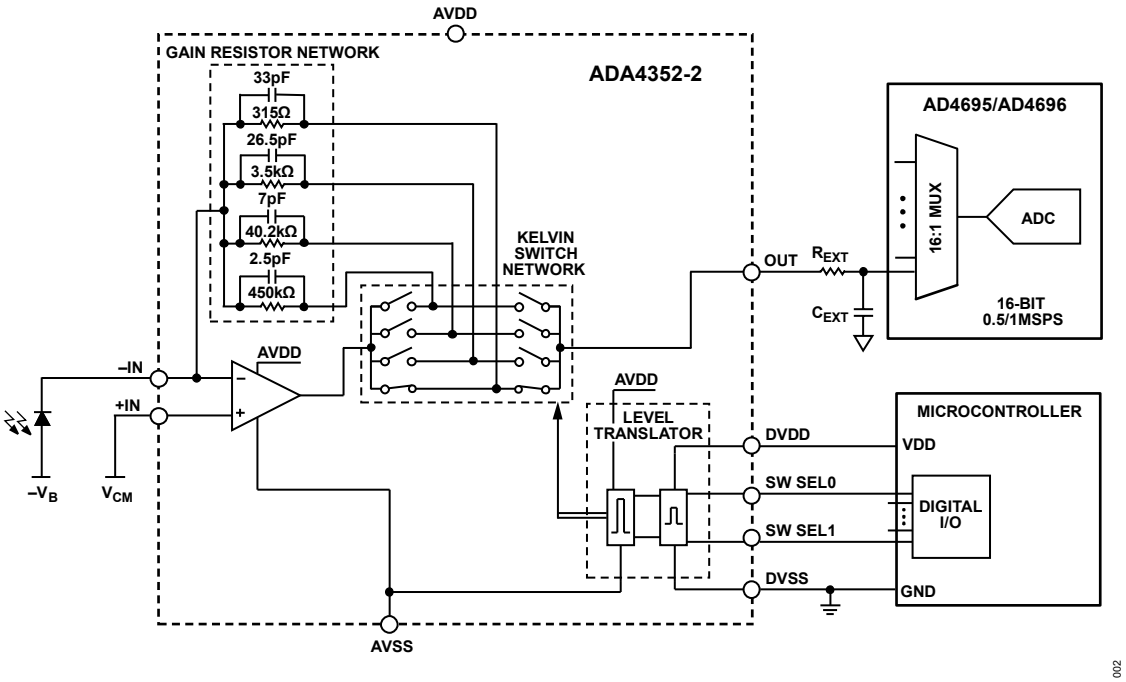

Figure 2. Compact Optical Measurement Signal Chain (One Channel Shown)

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REVISION HISTORY

Nature of Change	Page Number
10/2024 – Rev 0 Initial release	—

SPECIFICATIONS

Table 1. Electrical Characteristics 5V Specifications

(T_A = +25°C, AVDD = 2.5 V, AVSS = −2.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a single supply configuration with +IN biased to mid supplies.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
DC PARAMETERS								
Input Offset Voltage	$V_{OS,RTI}$	T_A = +25°C			±20	±100	µV	P
Input Offset Voltage Drift	$\Delta V_{OS,RTI}/\Delta T$	0°C < T_A < +85°C			±0.15	±0.8	µV	C_B
Input Offset Voltage Drift	$\Delta V_{OS,RTI}/\Delta T$	−40°C < T_A < +125°C			±0.16	±1.0	µV/°C	C_B
Output Offset Voltage	$\Delta V_{OS,OUT}$	T_A = +25°C	R_{F0} = 315 Ω		±25	±130	µV	P
			R_{F1} = 3.5 kΩ		±25	±130	µV	P
			R_{F2} = 40.2 kΩ		±25	±130	µV	P
			R_{F3} = 450 kΩ		±25	±150	µV	P
Output Offset Voltage Drift	$V_{OS,OUT}/\Delta T$	−40°C < T_A < +125°C	R_{F0} = 315 Ω		±0.1	±1.1	µV/°C	C_T
			R_{F1} = 3.5 kΩ		±0.2	±1.1	µV/°C	C_T
			R_{F2} = 40.2 kΩ		±0.3	±1.2	µV/°C	C_T
			R_{F3} = 450 kΩ		±0.4	±1.2	µV/°C	C_T
Internal Feedback Resistance	R_{FX}	T_A = +25°C	R_{F0} = 315 Ω	0.28	0.315	0.35	kΩ	P
			R_{F1} = 3.5 kΩ	3.15	3.5	3.9	kΩ	P
			R_{F2} = 40.2 kΩ	36	40.2	45	kΩ	P
			R_{F3} = 450 kΩ	400	450	500	kΩ	P
Internal Feedback Resistance Drift[2]	$\Delta R_{FX}/\Delta T$	−40°C < T_A < +125°C	R_{F0} = 315 Ω		32	47	ppm/°C	C_T
			R_{F1} = 3.5 kΩ		14	32	ppm/°C	C_T
			R_{F2} = 40.2 kΩ		14	29	ppm/°C	C_T
			R_{F3} = 450 kΩ		8	25	ppm/°C	C_T
Open-Loop Voltage Gain[2]	A_{VOL}	V_{OUT} = -2.4 V to 2.4 V, T_A = +25°C	R_{F2} = 40.2 kΩ	95	120		dB	P
		V_{OUT} = -2.4 V to 2.4 V, −40°C < T_A < +125°C	R_{F2} = 40.2 kΩ	103			dB	C_T

(T_A = +25°C, AVDD = 2.5 V, AVSS = −2.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a single supply configuration with +IN biased to mid supplies.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
Feedback Capacitance[3]	C_{FX}	T_A = +25°C	R_{F0} = 315 Ω		33		pF	C_B
			R_{F1} = 3.5 kΩ		26.5		pF	C_B
			R_{F2} = 40.2 kΩ		7		pF	C_B
			R_{F3} = 450 kΩ		2.5		pF	C_B
Ratiometric Gain Variation Between Channels		−40°C < T_A < +125°C	All Ranges		0.3	2	%	P
INPUT CHARACTERISTICS								
Input Bias Current — Non Inverting	I_{B+}	T_A = +25°C			±0.12	±1	nA	P
Input Common Mode Voltage Range	V_{CMR}	−40°C < T_A < +125°C	Guaranteed by CMRR	AVSS + 0.1		AVDD − 1.5	V	C_B
Linear Range of Current Pulled from Inverting Input	I_{INLIN-}	V_{+IN} = AVSS + 0.1 V	R_{F0} = 315 Ω		0.1 to 13		mA	C_T
			R_{F1} = 3.5 kΩ		0.01 to 1.3		mA	C_T
			R_{F2} = 40.2 kΩ		1 to 100		µA	C_T
			R_{F3} = 450 kΩ		0.1 to 10		µA	C_T
Linear Range of Current Pushed into Inverting Input	I_{INLIN+}	V_{+IN} = AVDD − 1.5 V	R_{F0} = 315 Ω		0.1 to 9		mA	C_T
			R_{F1} = 3.5 kΩ		0.01 to 0.9		mA	C_T
			R_{F2} = 40.2 kΩ		1 to 70		µA	C_T
			R_{F3} = 450 kΩ		0.1 to 7		µA	C_T
Common-Mode Rejection Ratio	CMRR	V_{CM} = -2.4 V to +1 V, T_A = −40°C to +125°C	All Ranges	78	91		dB	C_T
Common-Mode Input Impedance	Z_{CM}	(+IN)			3.75/1		GΩ/pF	C_B
		(−IN)			3.75/3.5		GΩ/pF	C_B
Differential Mode Input Capacitance	C_{INDM}	Differential mode			2		pF	C_B

(T_A = +25°C, AVDD = 2.5 V, AVSS = −2.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a single supply configuration with +IN biased to mid supplies.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
OUTPUT CHARACTERISTICS								
Output Swing High (AVDD − V_{OUT})	V_{OH}	V_{+IN} = AVSS+0.1 V, I_{-IN} = I_{INMAX-}	R_{F0} = 315 Ω			600	mV	P
			R_{F1} = 3.5 kΩ			150	mV	P
			R_{F2} = 40.2 kΩ			100	mV	P
			R_{F3} = 450 kΩ			100	mV	P
Output Swing Low (V_{OUT} − AVSS)	V_{OL}	V_{+IN} = AVDD − 1.5 V, I_{-IN} = I_{INMAX+}	R_{F0} = 315 Ω	600			mV	P
			R_{F1} = 3.5 kΩ	150			mV	P
			R_{F2} = 40.2 kΩ	100			mV	P
			R_{F3} = 450 kΩ	100			mV	P
Short-Circuit Current	I_{SC}	V_{+IN} = AVDD/2, I_{-IN} = 0 mA	V_{OUT} shorted to AVDD and AVSS		127/98		mA	C_B
DYNAMIC PERFORMANCE								
Gain Bandwidth Product	GBP				8.5		MHz	C_B
Slew Rate	SR	10% to 90%, rising and falling, I_{-IN} from 0 mA to I_{INMAX-}, no load	R_{F0} = 315 Ω		8.2		V/µs	C_B
			R_{F1} = 3.5 kΩ		6.9		V/µs	C_B
			R_{F2} = 40.2 kΩ		2		V/µs	C_B
			R_{F3} = 450 kΩ		0.4		V/µs	C_B
Total Harmonic Distortion	THD	f = 1 kHz, V_{OUT} = 1 V_{RMS}, no load	R_{F0} = 315 Ω		−123		dBc	C_B
			R_{F1} = 3.5 kΩ		−128		dBc	C_B
			R_{F2} = 40.2 kΩ		−128		dBc	C_B
			R_{F3} = 450 kΩ		−129		dBc	C_B
Settling Time to 0.1% of Output Step Voltage	t_s	C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF, V_{+IN} = AVSS + 0.1 V, I_{-IN} from 0 µA to I_{INMAX}	R_{F0} = 315 Ω		1		µs	S
			R_{F1} = 3.5 kΩ		2		µs	S
			R_{F2} = 40.2 kΩ		5		µs	S
			R_{F3} = 450 kΩ		10		µs	S
ANALOG POWER SUPPLIES								
Operating Range V_S = (AVDD − AVSS)	V_S			2.7		5.5	V	P
AVSS Range Below DVSS	VSS_R			−0.5		0	V	S

(T_A = +25°C, AVDD = 2.5 V, AVSS = −2.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a single supply configuration with +IN biased to mid supplies.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
Power Supply Rejection Ratio	PSRR	T_A = +25°C, V_S = 2.7 V to 5.5 V	All Ranges	81	90		dB	P
		T_A = −40°C to +125°C, V_S = 2.7 V to 5.5 V	All Ranges	75			dB	C_T
Analog Supply Current per Amplifier	I_{QA}	T_A = +25°C, V_S = 5.0 V	All Ranges		3.3	3.5	mA	P
		T_A = −40°C to +125°C, V_S = 5.0 V	All Ranges			4.35	mA	C_T
DIGITAL THRESHOLD VOLTAGES								
Input High Voltage	V_{IH}			DVDD − 0.7			V	S
Input Low Voltage	V_{IL}					DVSS + 0.5	V	S
Range SEL Pull-Down Resistance	R_{PD}				885		kΩ	C_B
DIGITAL POWER SUPPLIES								
Operating Range (DVDD - DVSS)	V_{SD}			1.62		5.5	V	P
Digital Quiescent Current	I_{QD}	T_A = +25°C				1	µA	P
		T_A = −40°C to +125°C				10	µA	C_T
ANALOG SWITCHES								
Switch On-Resistance	R_{ON}	T_A = +25°C			11	13	Ω	P
		T_A = −40°C to +125°C				19	Ω	C_T
Switch On-Resistance Drift	$\Delta R_{ON}/\Delta T$	T_A = −40°C to +125°C			0.3		%/°C	C_T

(T_A = +25°C, AVDD = 2.5 V, AVSS = −2.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0 V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a single supply configuration with +IN biased to mid supplies.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
Switch Off Input Capacitance	$C_{IN,OFF}$				1.8		pF	C_B
NOISE								
Input Voltage Noise Density	e_n	f = 100 kHz			7.3		nV/√Hz	C_B
Integrated Voltage Noise	$e_{n,pp}$	f = 0.1 Hz to 10 Hz			4.6		μV_{pp}	C_B

1 To simplify terminology throughout this data sheet, because the two amplifiers inside the ADA4352-2 are interchangeable, R_{F3}, R_{F2}, R_{F1}, R_{F0}, +IN, and −IN refer to Channel A or Channel B. V_{OUT} refers to OUT A or OUT B, within each channel, R_{FX} refers to R_{F3} or R_{F2}, R_{F1} or R_{F0}, and C_{FX} refers to C_{F3} or C_{F2}, C_{F1} or C_{F0}.

2 High speed production testing limits the accuracy of this specification.

3 Integrated capacitors have ±20% tolerance.

Table 2. Electrical Characteristics 3 V Specifications

(T_A = 25°C, AVDD = 1.5 V, AVSS = −1.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a symmetrical supply configuration with +IN biased to 0 V.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
DC PERFORMANCE								
Input Offset Voltage	$V_{OS,RTI}$	T_A = +25°C			±25	±150	µV	P
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	0°C < T_A < +85°C			±0.11	±0.85	µV/°C	C_B
Input Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C < T_A < +125°C			±0.22	±1.0	µV/°C	C_B
Output Offset Voltage	$V_{OS,OUT}$	T_A = +25°C	R_{F0} = 315 Ω		±40	±160	µV	P
			R_{F1} = 3.5 kΩ		±40	±160	µV	P
			R_{F2} = 40.2 kΩ		±40	±160	µV	P
			R_{F3} = 450 kΩ		±40	±165	µV	P
Output Offset Voltage Drift	$V_{OS,OUT}/\Delta T$	−40°C < T_A < +125°C	R_{F0} = 315 Ω		±0.4	±1.3	µV/°C	C_T
			R_{F1} = 3.5 kΩ		±0.4	±1.3	µV/°C	C_T
			R_{F2} = 40.2 kΩ		±0.4	±1.3	µV/°C	C_T
			R_{F3} = 450 kΩ		±0.5	±1.7	µV/°C	C_T
Internal Feedback Resistance	R_{FX}	T_A = +25°C	R_{F0} = 315 Ω	0.28	0.315	0.35	kΩ	P
			R_{F1} = 3.5 kΩ	3.15	3.5	3.9	kΩ	P
			R_{F2} = 40.2 kΩ	36	40.2	45	kΩ	P
			R_{F3} = 450 kΩ	400	450	500	kΩ	P
Internal Feedback Resistance Drift[2]	$\Delta R_{FX}/\Delta T$	−40°C < T_A < +125°C	R_{F0} = 315 Ω		32	47	ppm/°C	C_T
			R_{F1} = 3.5 kΩ		14	32	ppm/°C	C_T
			R_{F2} = 40.2 kΩ		14	29	ppm/°C	C_T
			R_{F3} = 450 kΩ		8	25	ppm/°C	C_T
Open-Loop Voltage Gain[2]	A_{VOL}	V_{OUT} = −1.4 V to 0 V, T_A = +25°C	R_{F2} = 40.2 kΩ	93	115		dB	P
		V_{OUT} = -1.4 V to 0 V, −40°C < T_A < +125°C	R_{F2} = 40.2 kΩ	98			dB	C_T
Feedback Capacitance[3]	C_{FX}	T_A = +25°C	R_{F0} = 315 Ω		33		pF	C_B
			R_{F1} = 3.5 kΩ		26.5		pF	C_B
			R_{F2} = 40.2 kΩ		7		pF	C_B
			R_{F3} = 450 kΩ		2.5		pF	C_B
Ratiometric Gain Variation Between Channels		−40°C < T_A < +125°C	All Ranges		0.3	2	%	P

(T_A = 25°C, AVDD = 1.5 V, AVSS = −1.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a symmetrical supply configuration with +IN biased to 0 V.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
INPUT CHARACTERISTICS								
Input Bias Current (Noninverting)	I_{B+}	T_A = +25°C			±0.12	±1	nA	P
Input Common-Mode Voltage Range	V_{CMR}	−40°C < T_A < +125°C	Guaranteed by CMRR	AVSS + 0.1		AVDD − 1.5	V	C_B
Linear Range of Current Pulled from Inverting Input	I_{INLIN-}	V_{+IN} = AVSS + 0.1 V	R_{F0} = 315 Ω		0.1 to 7.5		mA	C_T
			R_{F1} = 3.5 kΩ		10 to 750		µA	C_T
			R_{F2} = 40.2 kΩ		1 to 65		µA	C_T
			R_{F3} = 450 kΩ		0.1 to 6		µA	C_T
Linear Range of Current Pushed into Inverting Input	I_{INLIN+}	V_{+IN} = AVDD − 1.5 V	R_{F0} = 315 Ω		0.1 to 3.5		mA	C_T
			R_{F1} = 3.5 kΩ		10 to 350		µA	C_T
			R_{F2} = 40.2 kΩ		1 to 30		µA	C_T
			R_{F3} = 450 kΩ		0.1 to 3		µA	C_T
Common-Mode Rejection Ratio	CMRR	V_{CM} = −1.4 V to 0 V, T_A = −40°C to +125°C	All Ranges	73	87		dB	C_T
Common-Mode Input Impedance	Z_{CM}	(+IN)			3.75/2.8		GΩ/pF	C_B
		(−IN)			3.75/3.5		GΩ/pF	C_B
Differential Mode Input Capacitance	C_{INDM}	Differential mode			2		pF	C_B
OUTPUT CHARACTERISTICS								
Output Swing High (AVDD − V_{OUT})	V_{OH}	V_{+IN} = AVSS + 0.1 V, I_{-IN} = I_{INMAX-}	R_{F0} = 315 Ω			600	mV	P
			R_{F1} = 3.5 kΩ			150	mV	P
			R_{F2} = 40.2 kΩ			100	mV	P
			R_{F3}= 450k Ω			100	mV	P
Output Swing Low (V_{OUT} − AVSS)	V_{OL}	V_{+IN} = AVDD − 1.5 V, I_{-IN} = I_{INMAX+}	R_{F0} = 315 Ω	600			mV	P
			R_{F1} = 3.5 kΩ	150			mV	P
			R_{F2} = 40.2 kΩ	100			mV	P
			R_{F3} = 450 kΩ	100			mV	P

(T_A = 25°C, AVDD = 1.5 V, AVSS = −1.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a symmetrical supply configuration with +IN biased to 0 V.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
Short-Circuit Current	I_{SC}	V_{+IN} = AVDD/2, I_{-IN} = 0 mA	V_{OUT} shorted to AVDD and AVSS		57/40		mA	C_B
DYNAMIC PERFORMANCE								
Gain Bandwidth Product	GBP				8.5		MHz	C_B
Slew Rate	SR	10% to 90%, rising and falling, I_{-IN} from 0 mA to I_{INMAX-}, no load	R_{F0} = 315 Ω		8.2		V/µs	C_B
			R_{F1} = 3.5 kΩ		6.9		V/µs	C_B
			R_{F2} = 40.2 kΩ		2		V/µs	C_B
			R_{F3} = 450 kΩ		0.4		V/µs	C_B
Total Harmonic Distortion	THD	f = 1 kHz, V_{OUT} = 0.9 V_{RMS}, no load	R_{F0} = 315 Ω		−114		dBc	C_B
		f = 1 kHz, V_{OUT} = 1 V_{RMS}, no load	R_{F1} = 3.5 kΩ		−118		dBc	C_B
			R_{F2} = 40.2 kΩ		−118		dBc	C_B
			R_{F3} = 450 kΩ		−118		dBc	C_B
Settling Time to 0.1% of Output Step Voltage	t_s	C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF, V_{+IN} = AVSS + 0.1 V, I_{-IN} from 0 µA to I_{INMAX}	R_{F0} = 315 Ω		1		µs	S
			R_{F1} = 3.5 kΩ		2		µs	S
			R_{F2} = 40.2 kΩ		5		µs	S
			R_{F3} = 450 kΩ		10		µs	S
ANALOG POWER SUPPLIES								
Operating Range V_S = (AVDD − AVSS)	V_S			2.7		5.5	V	P
AVSS Range Below DVSS	VSS_R			−2.5		0	V	S
Power Supply Rejection Ratio	PSRR	T_A = +25°C, V_S = 2.7 V to 5.5 V	All Ranges	81	90		dB	P
		T_A = −40°C to +125°C, V_S = 2.7 V to 5.5 V	All Ranges	75			dB	C_T
Analog Supply Current per Amplifier	I_{QA}	T_A = +25°C, V_S = 3.0 V	All Ranges		3.0	3.25	mA	P
		T_A = −40°C to +125°C, V_S = 3.0 V	All Ranges			4.1	mA	C_T

(T_A = 25°C, AVDD = 1.5 V, AVSS = −1.5 V, DVDD = 3 V, DVSS = 0 V, load resistance (R_L) = open, +IN = 0V, unless otherwise noted. These default AVDD, AVSS, and +IN conditions are equivalent to a symmetrical supply configuration with +IN biased to 0 V.)

PARAMETER	SYMBOL	CONDITIONS	COMMENTS	MIN	TYP	MAX	UNITS	TEST LEVELS
DIGITAL THRESHOLD VOLTAGE								
Input High Voltage	V_{IH}			DVDD − 0.7			V	S
Input Low Voltage	V_{IL}					DVSS + 0.5	V	S
Range SEL Pull-Down Resistance	R_{PD}				885		kΩ	C_B
DIGITAL POWER SUPPLIES								
Operating Range (DVDD - DVSS)	V_{SD}			1.62		5.5	V	P
Digital Quiescent Current	I_{QD}	T_A = +25°C				1	µA	P
		T_A = −40°C to +125°C				10	µA	C_T
ANALOG SWITCHES								
Switch On-Resistance	R_{ON}	T_A = +25°C			21	25	Ω	P
		T_A = −40°C to +125°C				33	Ω	C_T
Switch On-Resistance Drift	$\Delta R_{ON}/\Delta T$	T_A = −40°C to +125°C			0.25		%/°C	C_T
Switch Off Input Capacitance	$C_{IN,OFF}$				1.8		pF	C_B
NOISE								
Input Voltage Noise Density	e_n	f = 100 kHz			7.3		nV/√Hz	C_B
Integrated Voltage Noise	$e_{n,pp}$	f = 0.1 Hz to 10 Hz			4.6		μV_{pp}	C_B

1 To simplify terminology throughout this data sheet, because the two amplifiers inside the ADA4352-2 are interchangeable, R_{F3}, R_{F2}, R_{F1}, R_{F0}, +IN, and −IN refer to Channel A or Channel B. V_{OUT} refers to OUT A or OUT B, within each channel, R_{FX} refers to R_{F3} or R_{F2}, R_{F1} or R_{F0}, and C_{FX} refers to C_{F3} or C_{F2}, C_{F1} or C_{F0}.

2 High speed production testing limits the accuracy of this specification.

3 Integrated capacitors have ±20% tolerance.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise specified.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only. Human body model (HBM) is per the ANSI/ESDA/JEDEC JS-001. Field-induced charged device model (FICDM) and charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

Table 3. ADA4352-2, 16-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±2500	1C
FICDM	±1250	C3

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 4. Explanation of Test Levels

Test Level	Description
D	Definition
S	Design verification simulation
P	100% production tested
P_F	Functionally checked during production test
C_T	Characterized on tester
C_B	Characterized on bench

Table 5. Absolute Maximum Ratings

PARAMETER	RATING
Voltage Between Any Two Pins	6 V
DVDD and AVDD to DVSS	−0.3 V to +6 V
DVDD, AVDD, and DVSS to AVSS	−0.3 V to +6 V
+IN and −IN Voltage	AVSS − 1 V to AVDD + 0.3 V
+IN and −IN Current	10mA
Op Amp Output Continuous Current	±20 mA
Temperature Storage Range	-65°C to +150°C
Temperature Operating Range	−40°C to +125°C

PARAMETER	RATING
Temperature Junction, T_J	150°C
Temperature Case, T_C	260°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

Thermal Resistance		
Package Type	Θ_{JA}	Unit
CP-16-32	91	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4352-2 is limited by the associated rise in T_J on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses the package exerts on the die, permanently shifting the parametric performance of the ADA4352-2. Exceeding a T_J of 175°C for an extended period can result in changes in the silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package is the sum of the quiescent power dissipation and the power dissipated in the die due to the output load drive of the amplifier.

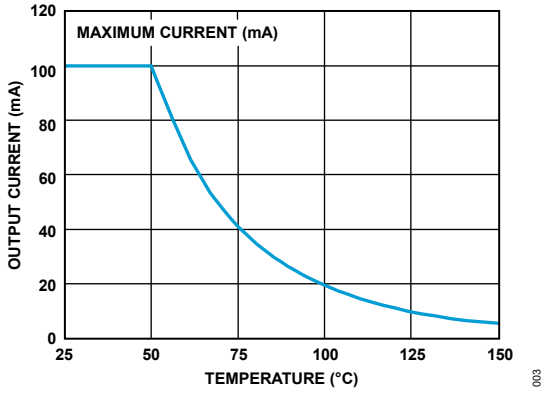


Figure 3. Output Current Derating Curve

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

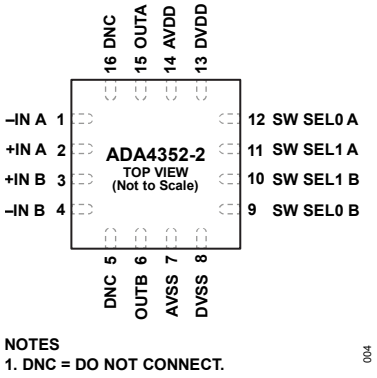


Figure 4. Pin Configuration

Table 6. Pin Descriptions

PIN	NAME	DESCRIPTION	REF SUPPLY	Type
1	−INA	Channel A TIA Inverting Input	AVDD	IN
2	+INA	Channel A TIA Noninverting Input	AVDD	IN
3	+INB	Channel B TIA Noninverting Input	AVDD	IN
4	−INB	Channel B TIA Inverting Input	AVDD	IN
5	DNC	Reserved - Do Not Connect		
6	OUT B	Channel B TIA Output	AVDD	OUT
7	AVSS	Negative Analog Supply		POWER
8	DVSS	Negative Digital Supply		POWER
9	SW SEL0 B	Channel B Range Selection Input 0	DVDD	IN
10	SW SEL1 B	Channel B Range Selection Input 1	DVDD	IN
11	SW SEL1 A	Channel A Range Selection Input 1	DVDD	IN
12	SW SEL0 A	Channel A Range Selection Input 0	DVDD	IN
13	DVDD	Positive Digital Supply		POWER
14	AVDD	Positive Analog Supply		POWER
15	OUT A	Channel A TIA Output	AVDD	OUT
16	DNC	Reserved - Do Not Connect		

TYPICAL PERFORMANCE CHARACTERISTICS

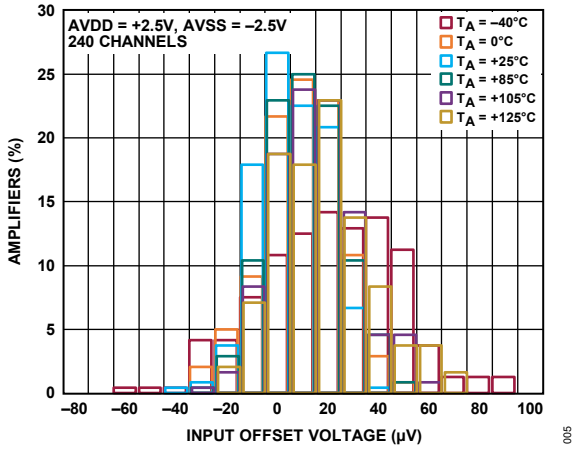


Figure 5. Input Offset Voltage Distribution, AVDD = +2.5 V, AVSS = −2.5 V

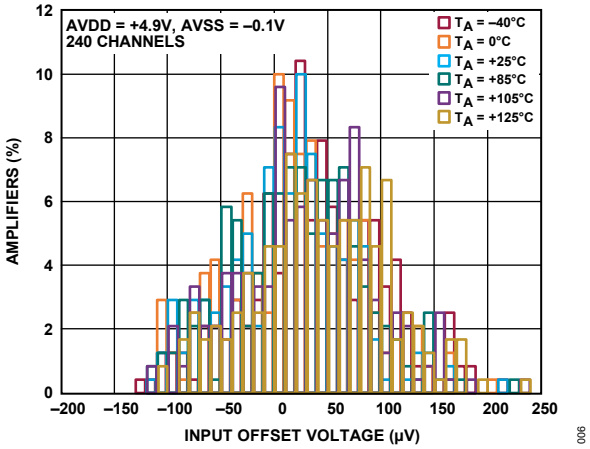


Figure 6. Input Offset Voltage Distribution, AVDD = +4.9 V, AVSS = −0.1 V

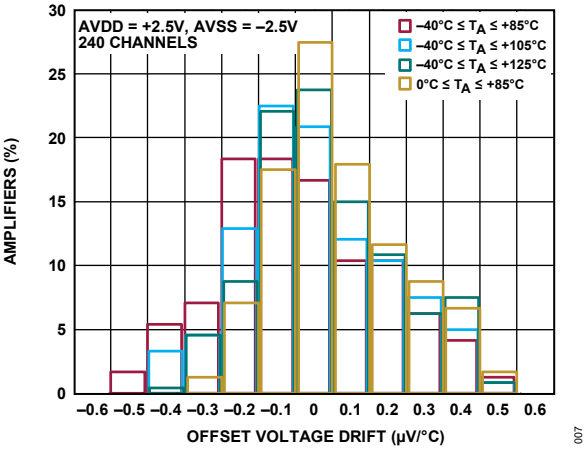


Figure 7. Input Offset Voltage Drift Distribution, AVDD = +2.5 V, AVSS = −2.5 V

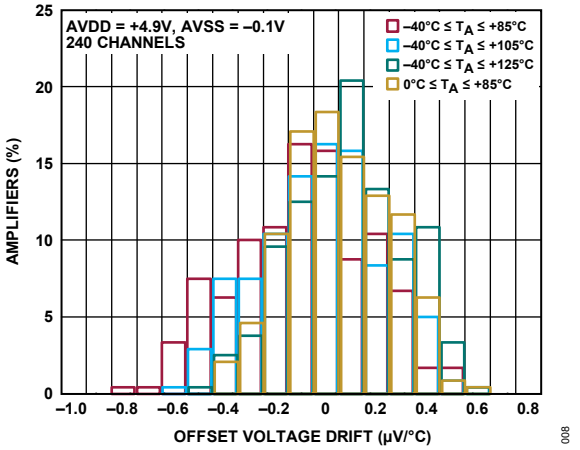


Figure 8. Input Offset Voltage Drift Distribution, AVDD = +4.9 V, AVSS = −0.1 V

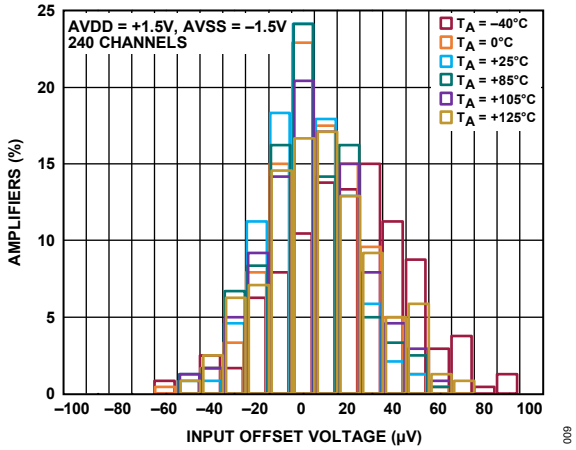


Figure 9. Input Offset Voltage Distribution, AVDD = +1.5 V, AVSS = −1.5 V

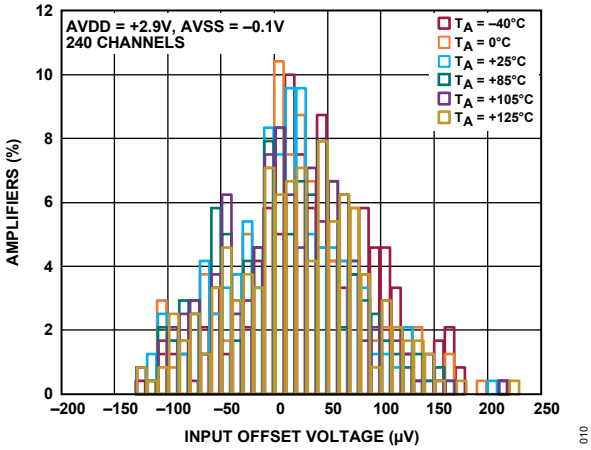


Figure 10. Input Offset Voltage Distribution, AVDD = +2.9 V, AVSS = −0.1 V

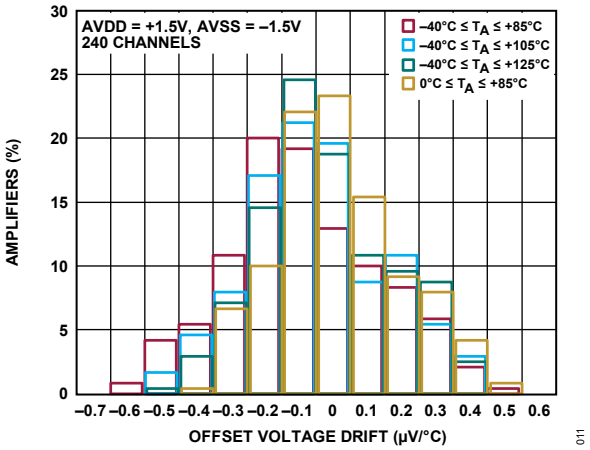


Figure 11. Input Offset Voltage Drift Distribution, AVDD = +1.5 V, AVSS = −1.5 V

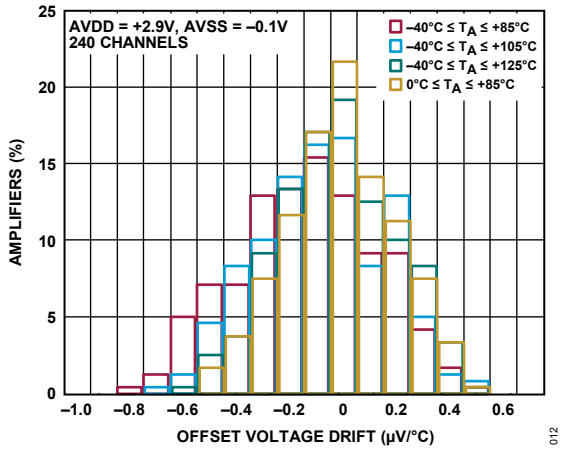


Figure 12. Input Offset Voltage Drift Distribution, AVDD = +2.9 V, AVSS = −0.1 V

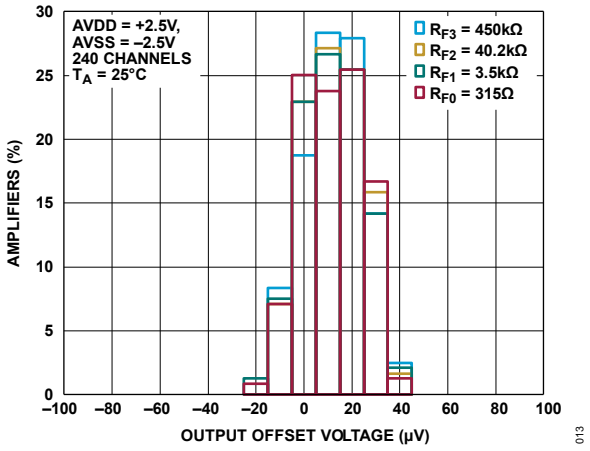


Figure 13. Output Offset Voltage Distribution, AVDD = +2.5 V, AVSS = −2.5 V

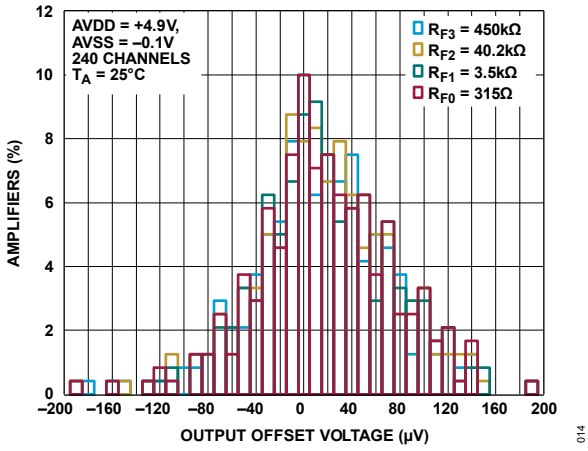


Figure 14. Output Offset Voltage Distribution, AVDD = +4.9 V, AVSS = −0.1 V

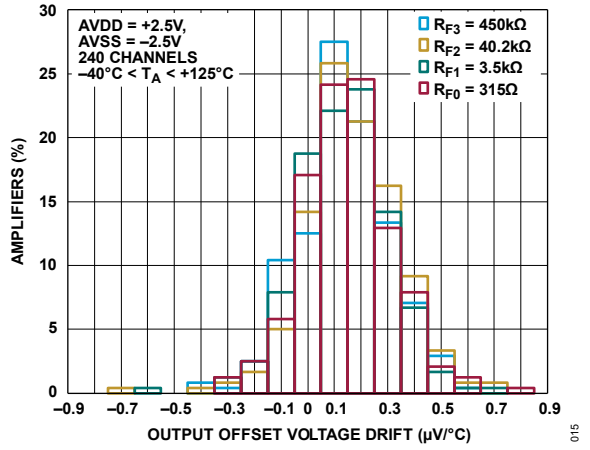


Figure 15. Output Offset Voltage Drift Distribution, AVDD = +2.5 V, AVSS = −2.5 V

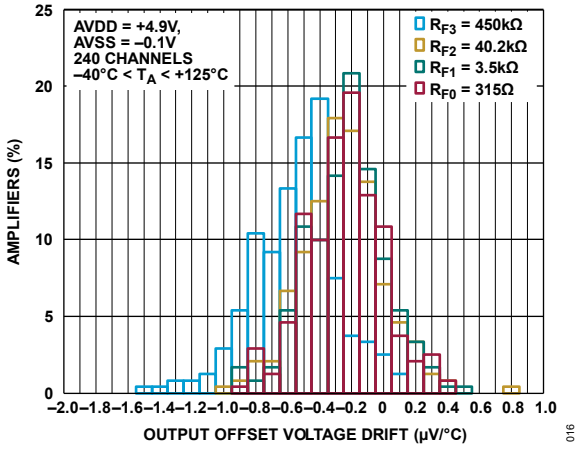


Figure 16. Output Offset Voltage Drift Distribution, AVDD = +4.9 V, AVSS = −0.1 V

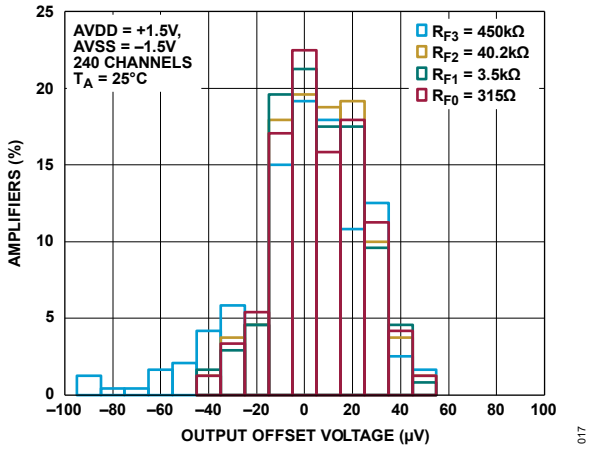


Figure 17. Output Offset Voltage Distribution, AVDD = +1.5 V, AVSS = −1.5 V

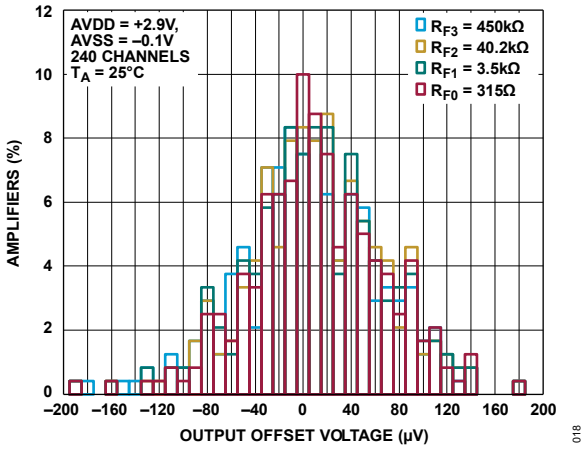


Figure 18. Output Offset Voltage Distribution, AVDD = +2.9 V, AVSS = −0.1 V

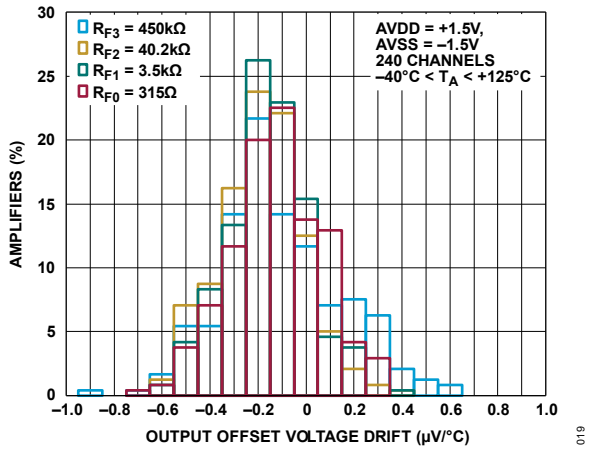


Figure 19. Output Offset Voltage Drift Distribution, AVDD = +1.5 V, AVSS = −1.5 V

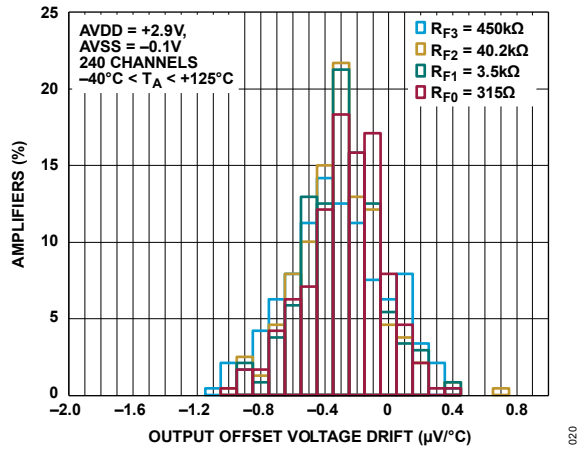


Figure 20. Output Offset Voltage Drift Distribution, AVDD = +2.9 V, AVSS = −0.1 V

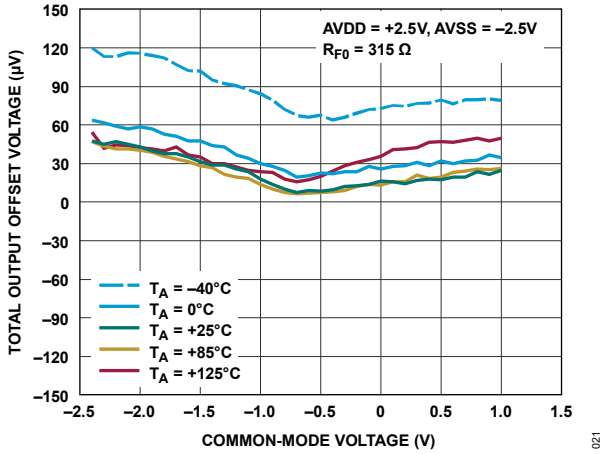


Figure 21. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F0} = 315 Ω, AVDD = +2.5 V, AVSS = −2.5 V

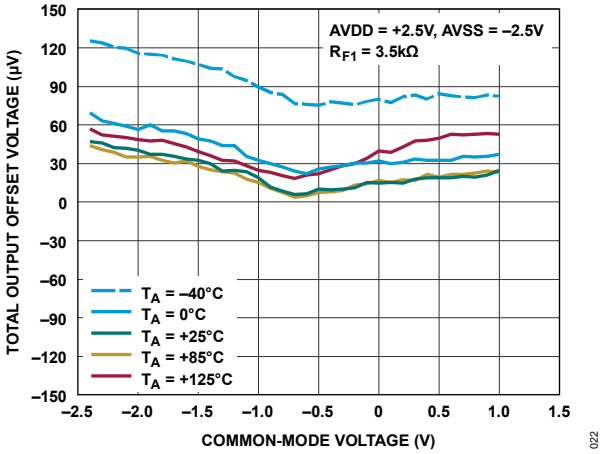


Figure 22. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F1} = 3.5 kΩ, AVDD = +2.5 V, AVSS = −2.5 V

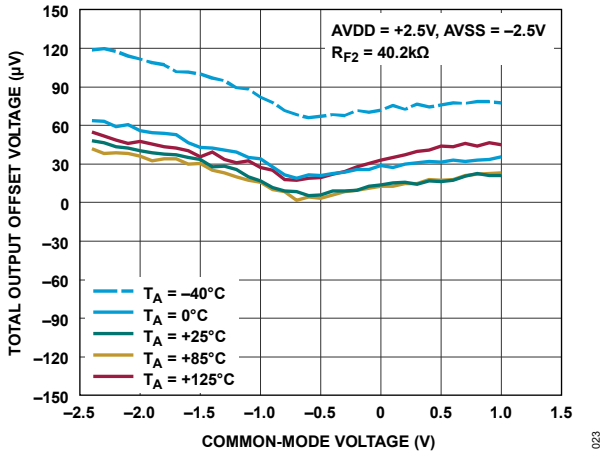


Figure 23. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F2} = 40.2 kΩ, AVDD = +2.5 V, AVSS = −2.5 V

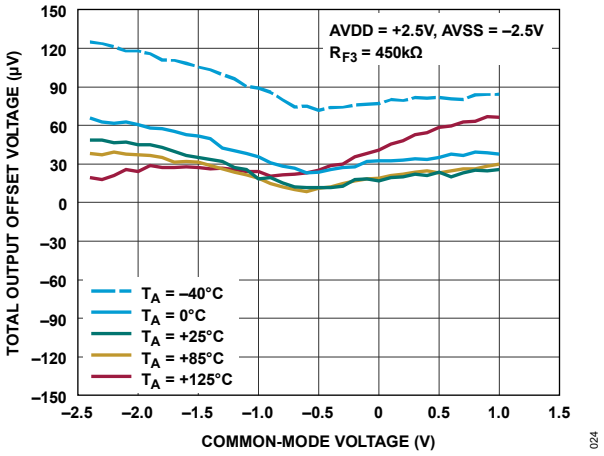


Figure 24. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F3} = 450 kΩ, AVDD = +2.5 V, AVSS = −2.5 V

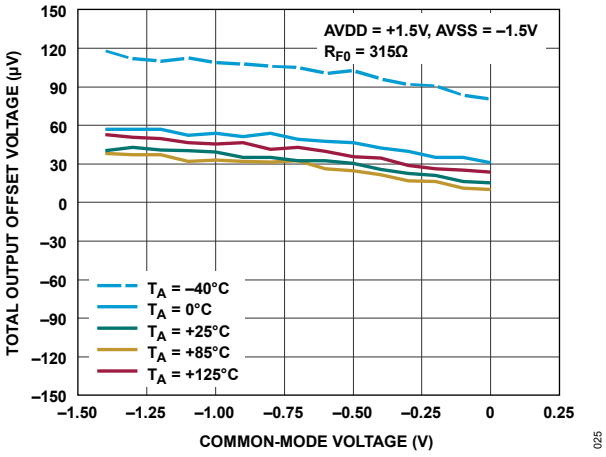


Figure 25. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F0} = 350 Ω, AVDD = +1.5 V, AVSS = −1.5 V

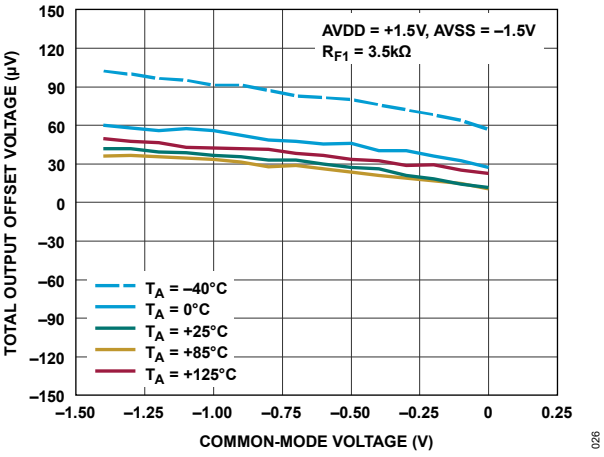


Figure 26. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F1} = 3.5 kΩ, AVDD = +1.5 V, AVSS = −1.5 V

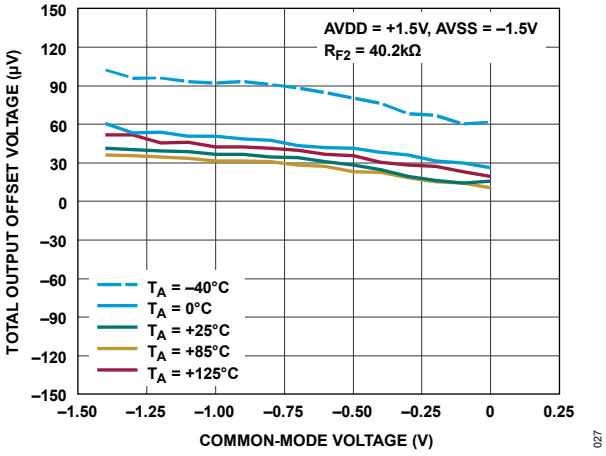


Figure 27. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F2} = 40.2 kΩ, AVDD = +1.5 V, AVSS = −1.5 V

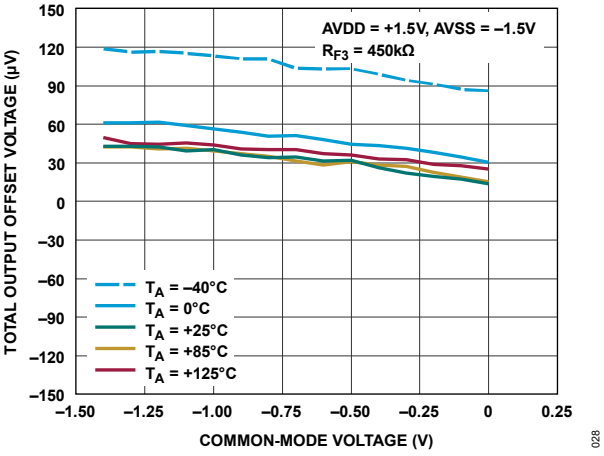


Figure 28. Total Output Offset Voltage vs. Common-Mode Voltage at Various Temperatures, R_{F3} = 450 kΩ, AVDD = +1.5 V, AVSS = −1.5 V

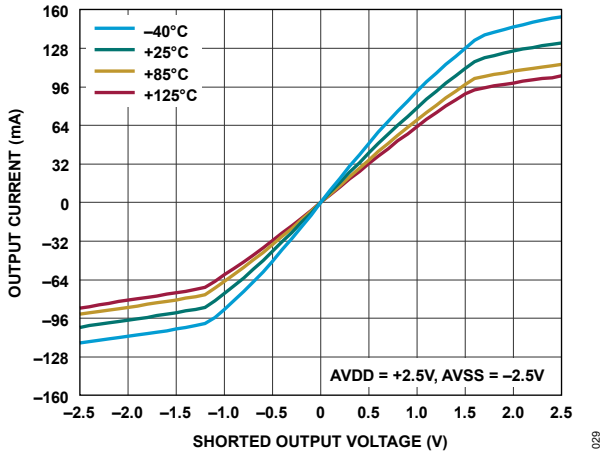


Figure 29. Short Circuit Current vs. Shorted Output Voltage, AVDD = +2.5 V, AVSS = −2.5 V

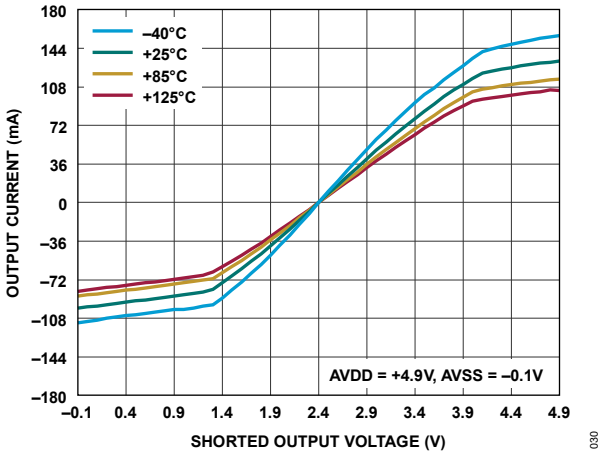


Figure 30. Short Circuit Current vs. Shorted Output Voltage, AVDD = +4.9 V, AVSS = −0.1 V

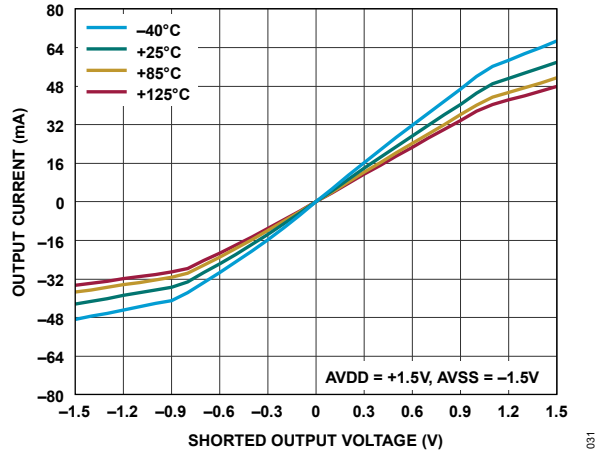


Figure 31. Short Circuit Current vs. Shorted Output Voltage, AVDD = +1.5 V, AVSS = −1.5 V

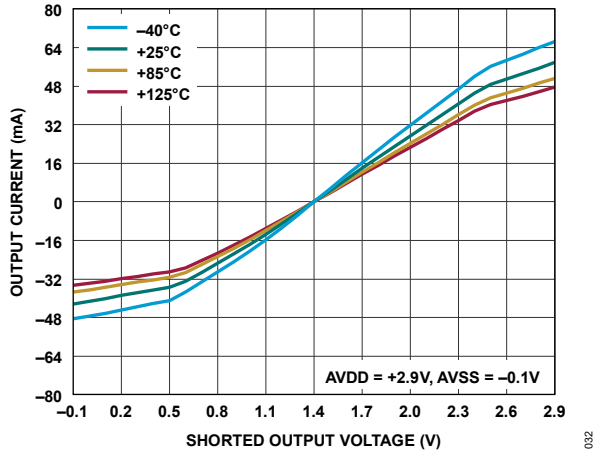


Figure 32. Short Circuit Current vs. Shorted Output Voltage, AVDD = +2.9 V, AVSS = −0.1 V

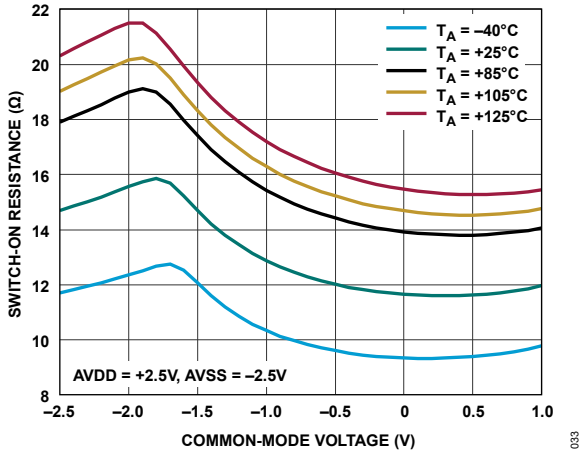


Figure 33. Switch-ON Resistance vs. Common-Mode Voltage, AVDD = +2.5 V, AVSS = −2.5 V

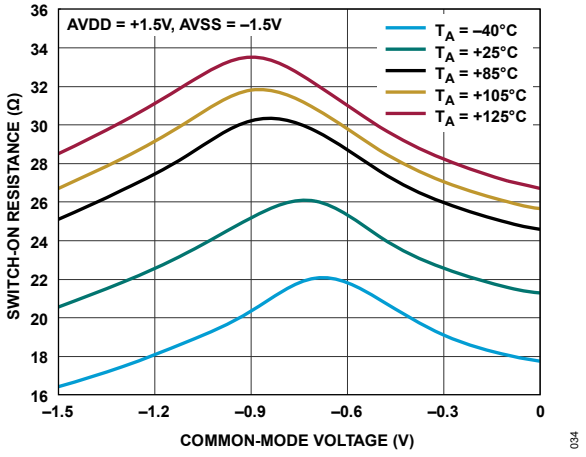


Figure 34. Switch-ON Resistance vs. Common-Mode Voltage, AVDD = +1.5 V, AVSS = −1.5 V

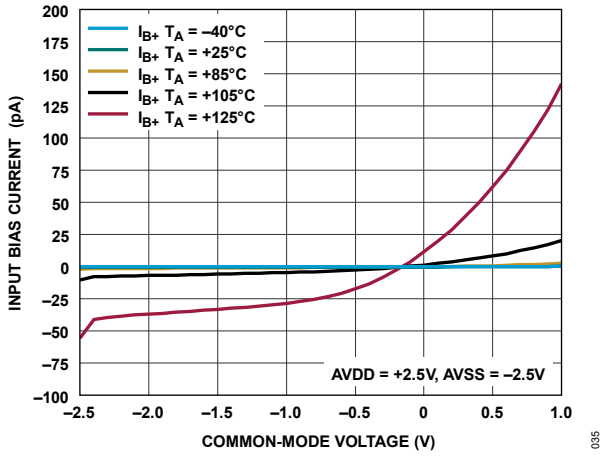


Figure 35. Noninverting Input Bias Current vs. Common-Mode Voltage, AVDD = +2.5 V, AVSS = −2.5 V

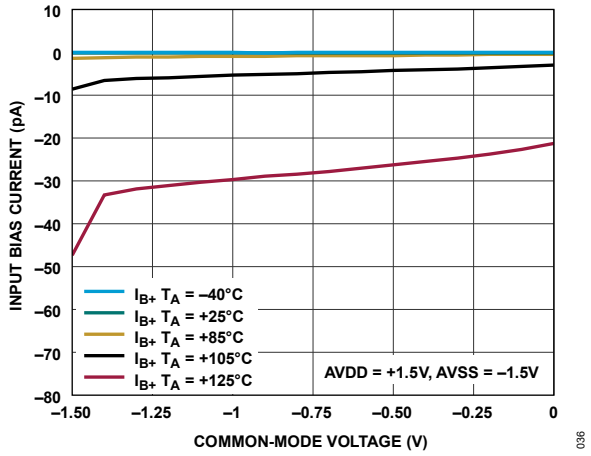


Figure 36. Noninverting Input Bias Current vs. Common-Mode Voltage, AVDD = +1.5 V, AVSS = −1.5 V

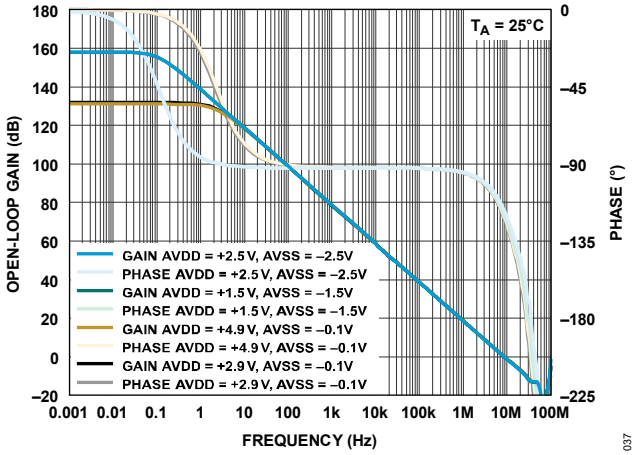


Figure 37. Open-Loop Gain and Phase vs. Frequency at Various Supplies

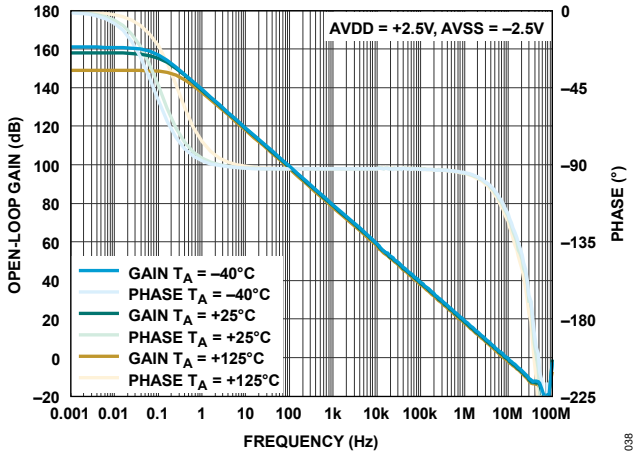


Figure 38. Open-Loop Gain and Phase vs. Frequency at Various Temperatures

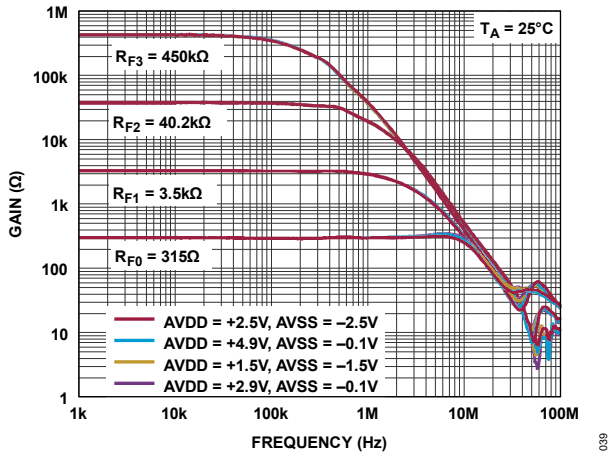


Figure 39. Closed-Loop Gain vs. Frequency at Various Supplies

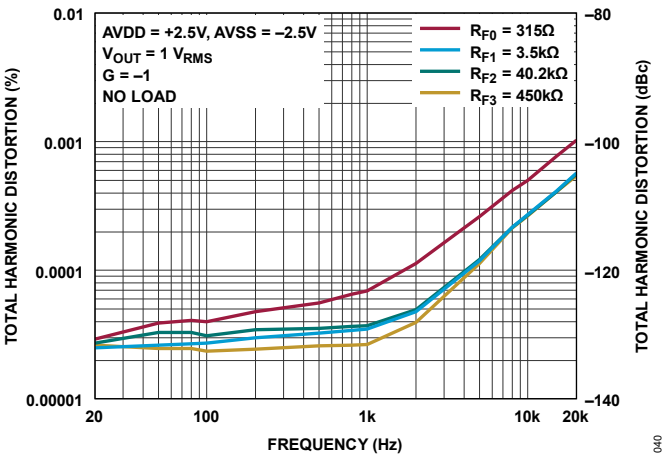


Figure 40. Total Harmonic Distortion vs. Frequency, AVDD = +2.5 V, AVSS = −2.5 V

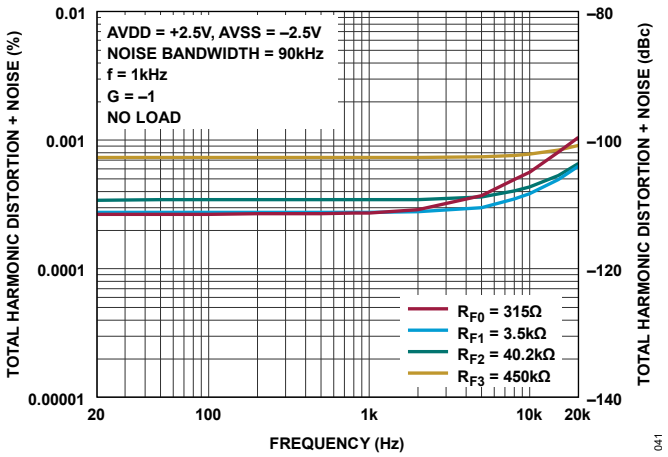


Figure 41. Total Harmonic Distortion + Noise vs. Frequency, AVDD = +2.5 V, AVSS = −2.5 V

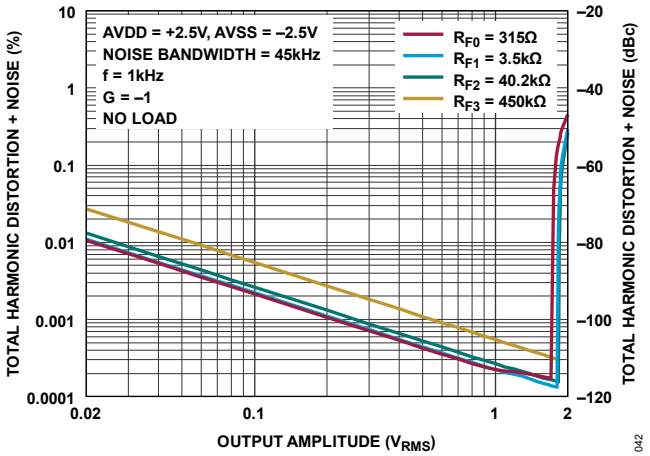


Figure 42. Total Harmonic Distortion + Noise vs. Output Amplitude, AVDD = +2.5 V, AVSS = −2.5 V

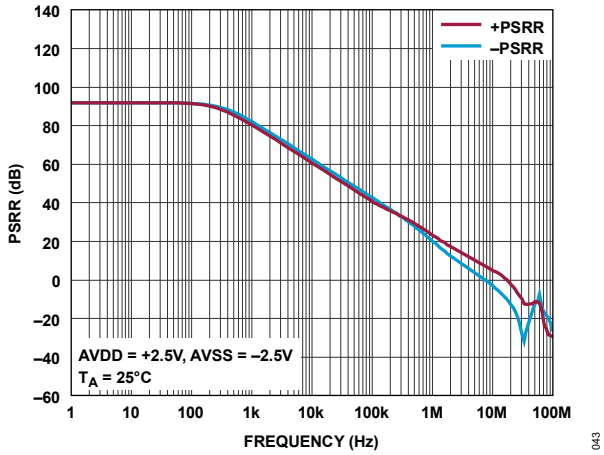


Figure 43. PSRR vs. Frequency, AVDD = +2.5 V, AVSS = −2.5 V

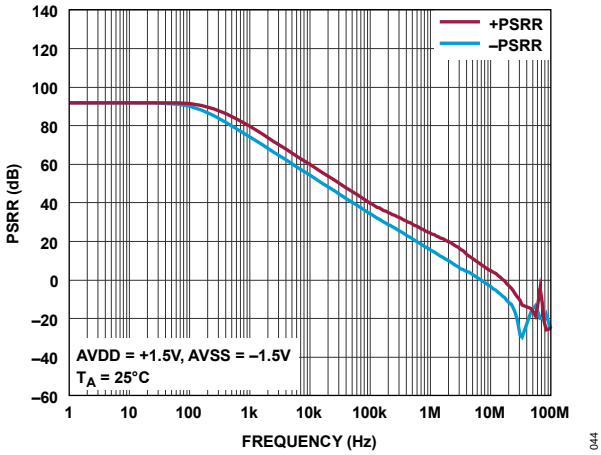


Figure 44. PSRR vs. Frequency, AVDD = +1.5 V, AVSS = −1.5 V

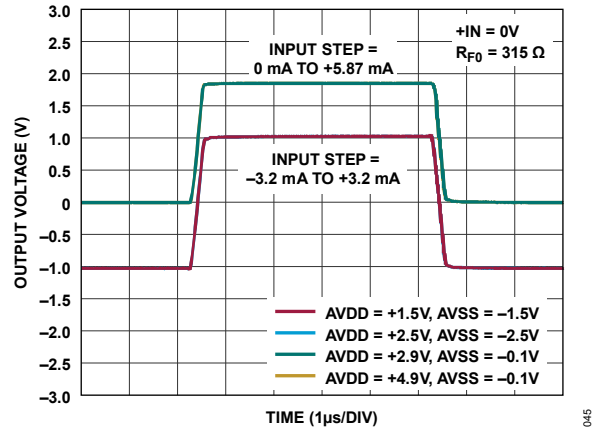


Figure 45. Large Signal Transient Response at Various Supplies, R_{F0} = 315 Ω, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

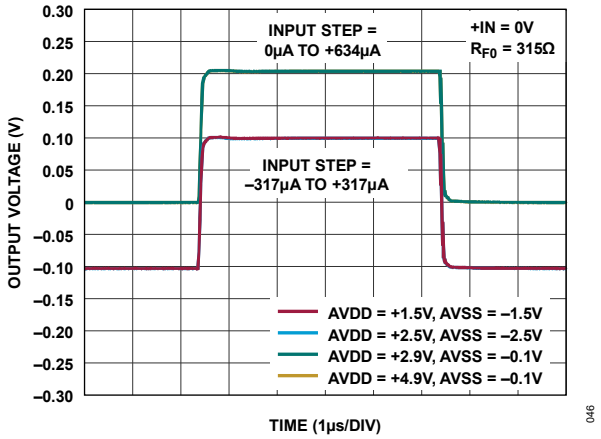


Figure 46. Small Signal Transient Response at Various Supplies, R_{F0} = 315 Ω, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

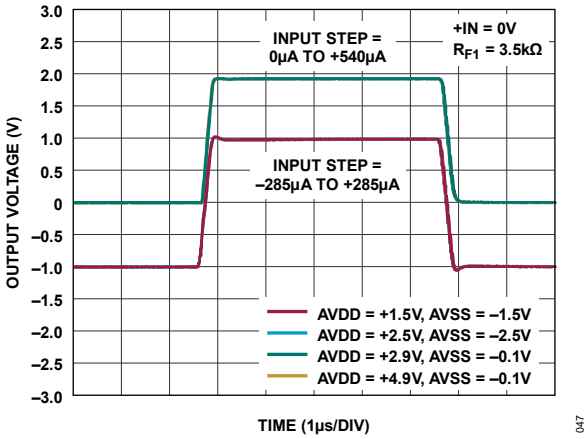


Figure 47. Large Signal Transient Response at Various Supplies, R_{F1} = 3.5 kΩ, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

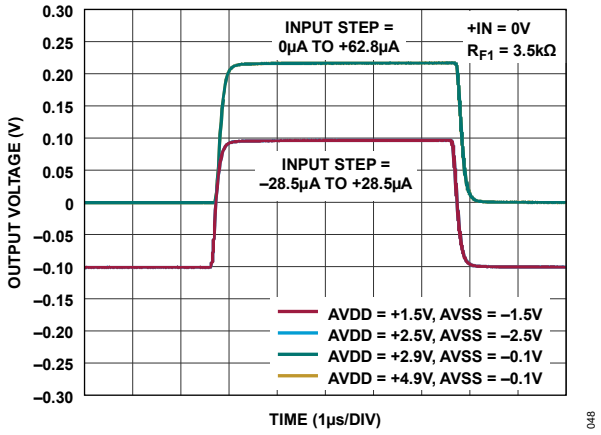


Figure 48. Small Signal Transient Response at Various Supplies, R_{F1} = 3.5 kΩ, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

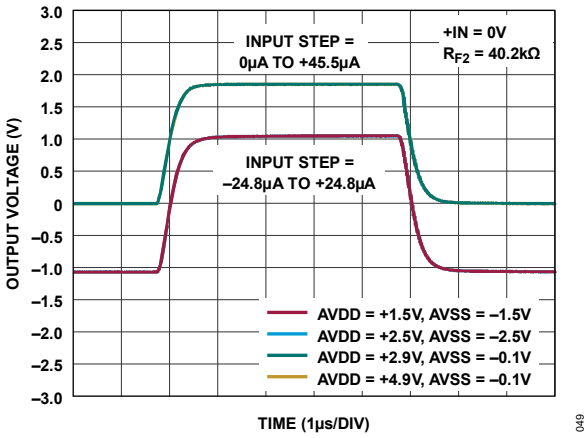


Figure 49. Large Signal Transient Response at Various Supplies, R_{F2} = 40.2 kΩ, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

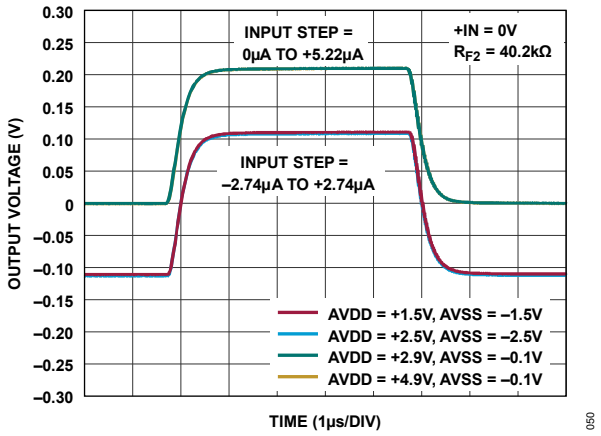


Figure 50. Small Signal Transient Response at Various Supplies, R_{F2} = 40.2 kΩ, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

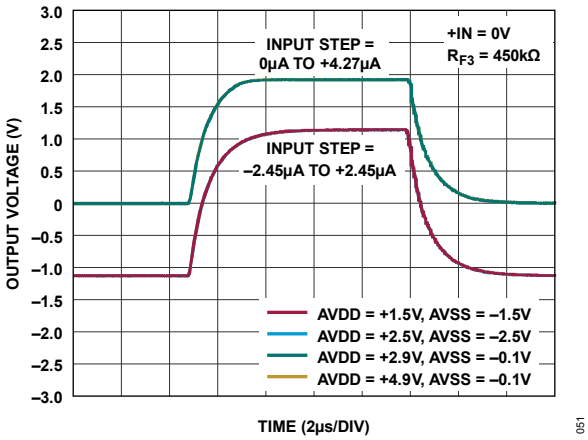


Figure 51. Large Signal Transient Response at Various Supplies, R_{F3} = 450 kΩ, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

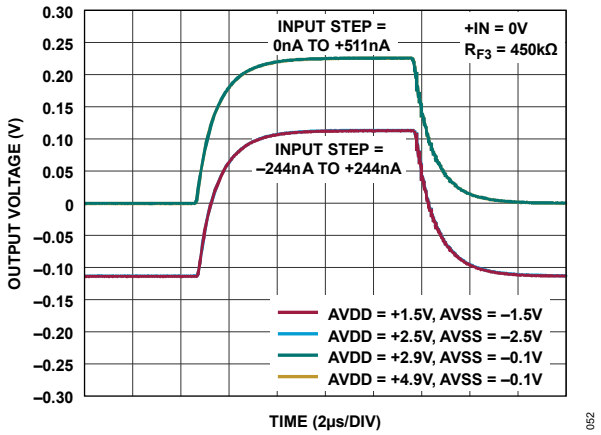


Figure 52. Small Signal Transient Response at Various Supplies, R_{F3} = 450 kΩ, C_D = 10 pF, R_{EXT} = 200 Ω, C_{EXT} = 180 pF

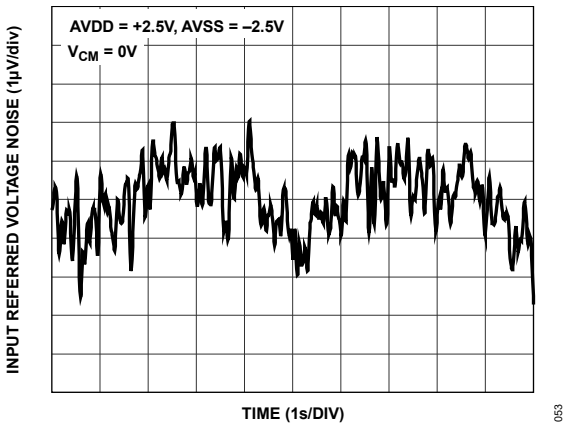


Figure 53. 0.1 Hz to 10 Hz Input Voltage Noise, AVDD = +2.5 V, AVSS = −2.5 V

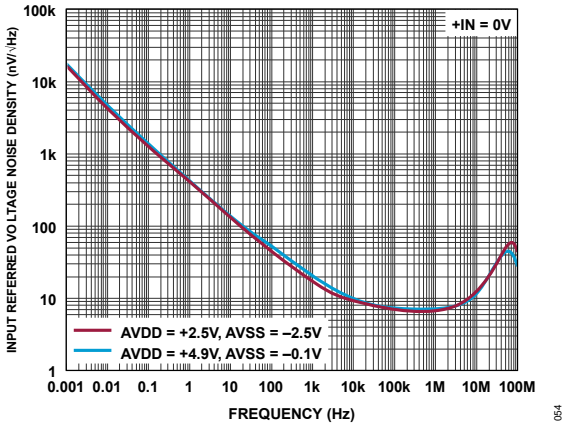


Figure 54. 0.001 Hz to 100 MHz Input Voltage Noise Density, 5 V Supply

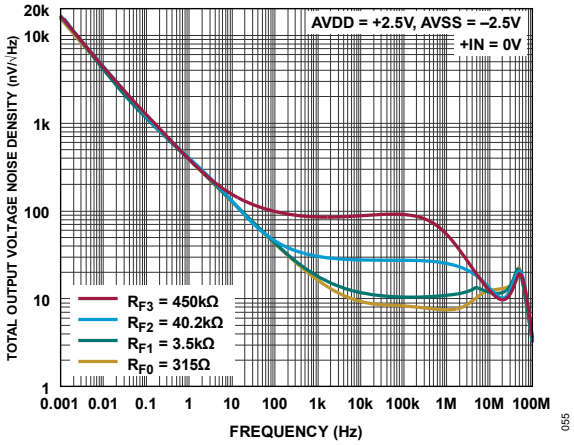


Figure 55. 0.001 Hz to 100 MHz Total Output Voltage Noise Density, AVDD = +2.5 V, AVSS = −2.5 V

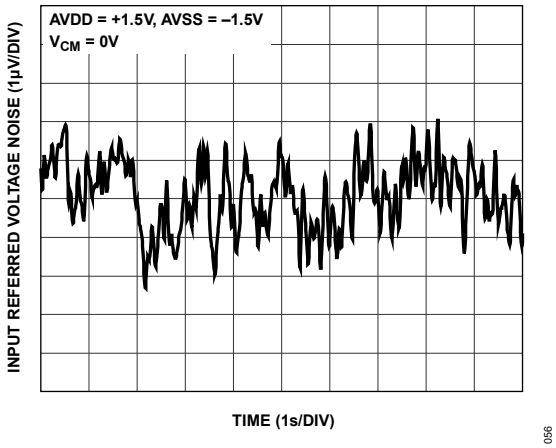


Figure 56. 0.1 Hz to 10 Hz Input Voltage Noise, AVDD = +1.5 V, AVSS = −1.5 V

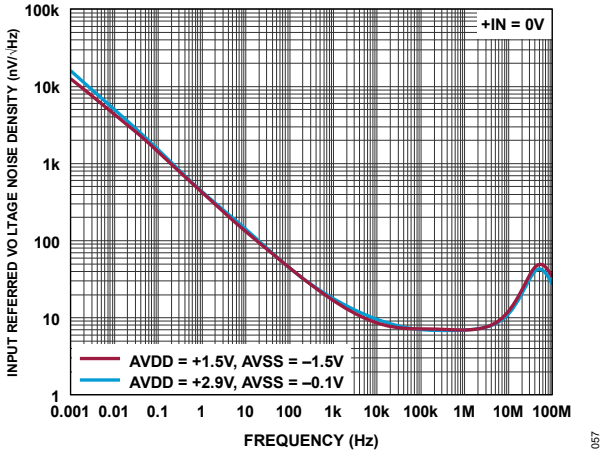


Figure 57. 0.001 Hz to 100 MHz Input Voltage Noise Density, 3 V Supply

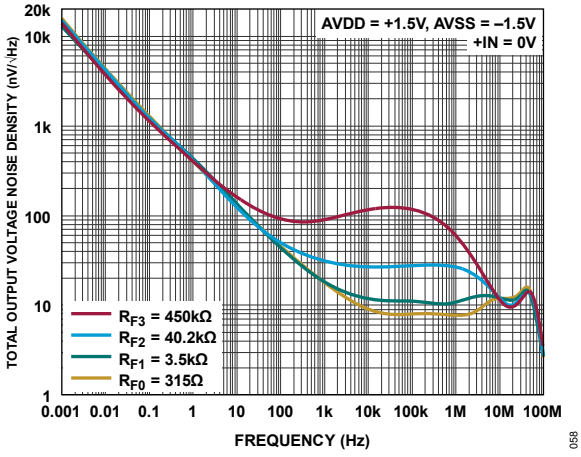


Figure 58. 0.001 Hz to 100 MHz Total Output Voltage Noise Density, AVDD = +1.5 V, AVSS = −1.5 V

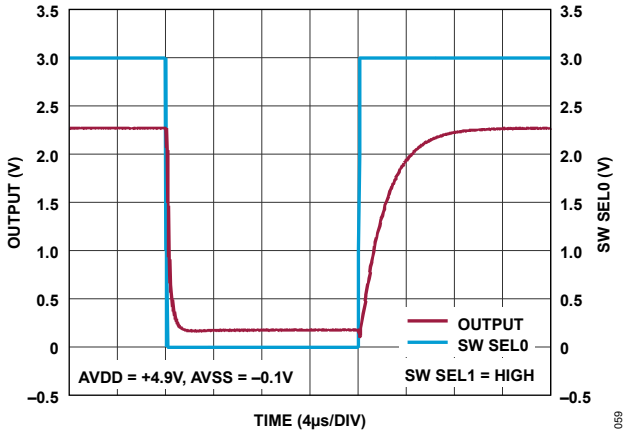


Figure 59. Switching Between R_{F3} and R_{F2}, AVDD = +4.9V, AVSS = -0.1V

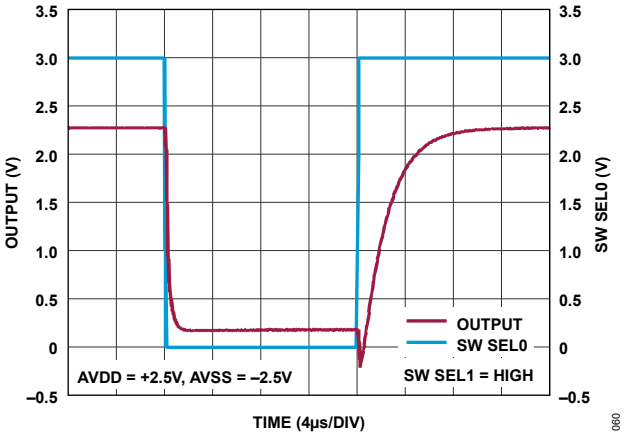


Figure 60. Switching Between R_{F3} and R_{F2}, AVDD = +2.5V, AVSS = -2.5V

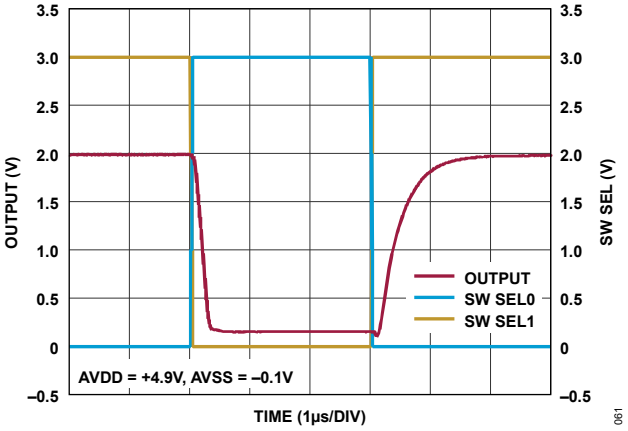


Figure 61. Switching Between R_{F2} and R_{F1}, AVDD = +4.9V, AVSS = -0.1V

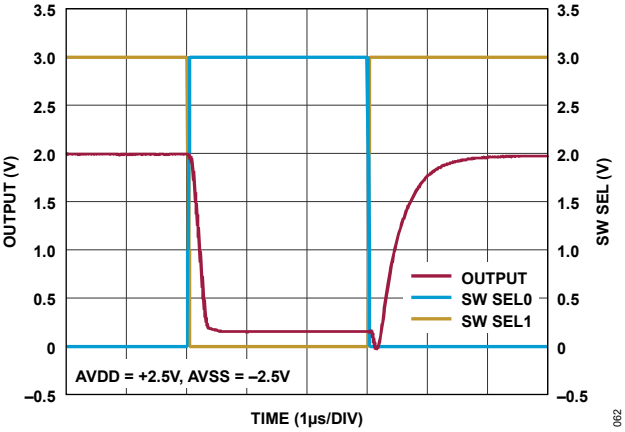


Figure 62. Switching Between R_{F2} and R_{F1}, AVDD = +2.5V, AVSS = -2.5V

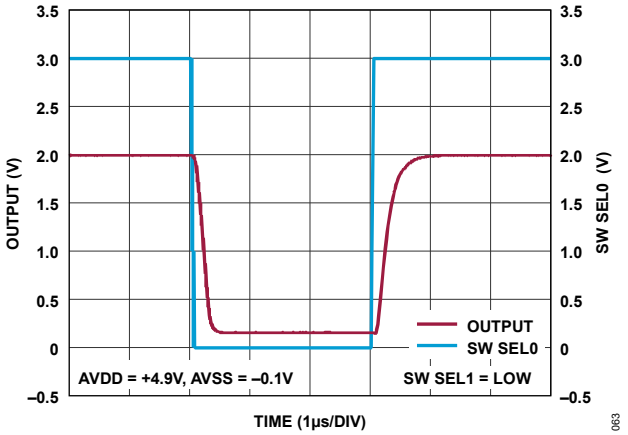


Figure 63. Switching Between R_{F1} and R_{F0}, AVDD = +4.9V, AVSS = -0.1V

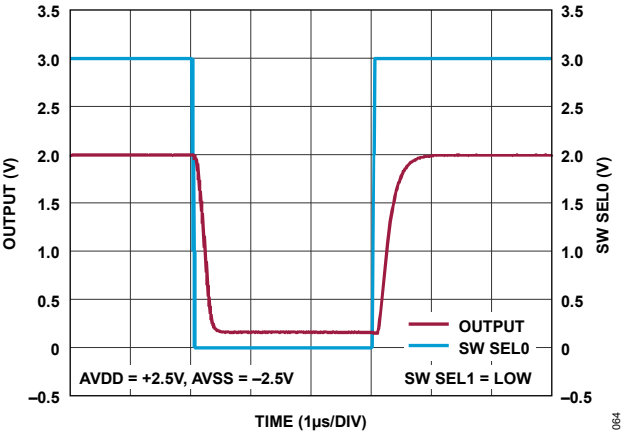


Figure 64. Switching Between R_{F1} and R_{F0}, AVDD = +2.5V, AVSS = -2.5V

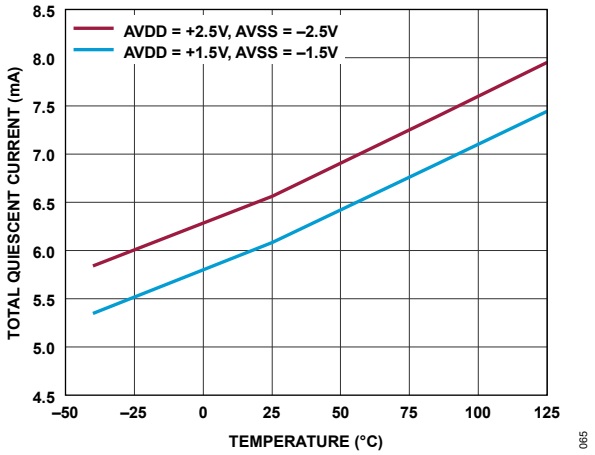


Figure 65. Analog Supply Current vs. Temperature

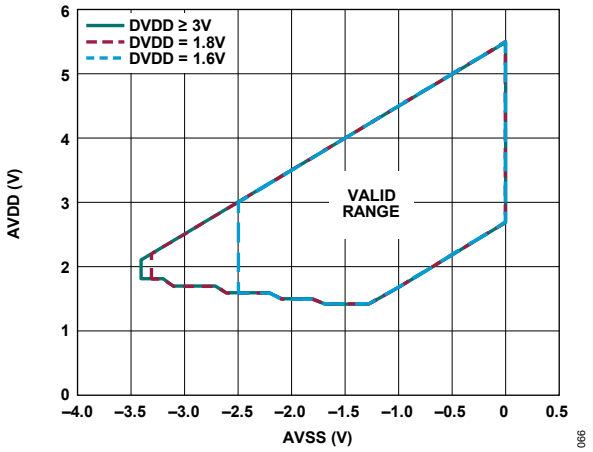


Figure 66. Valid Operating Range for AVSS Below DVSS, DVSS = 0 V

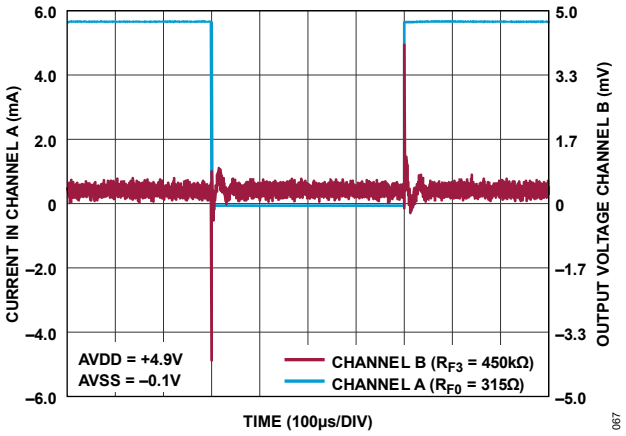


Figure 67. Channel-to-Channel Crosstalk, AVDD = +4.9V, AVSS = -0.1V

Table 7. Gain Setting Truth Table

SW SEL0	SW SEL 1	Gain setting
0	0	315 Ω
0	1	3.5 kΩ
1	0	40.2 kΩ
1	1	450 kΩ

THEORY OF OPERATION

OVERVIEW

The ADA4352-2 is a small, dual-channel programmable gain transimpedance amplifier (PGTIA) offering four selectable integrated feedback gain resistor selections for each of the two channels. The ADA4352-2 features a core amplifier with low offset and offset drift, low gain drift, low noise, and low input bias current. A simple gain calibration removes the DC error contributed by the tolerance of the integrated feedback resistors. Gain selection is done via proprietary switches that outperform typical CMOS switches of similar size and on-resistance. The switches are arranged in a Kelvin configuration that removes the added switch on-resistance and its nonlinear behavior from the signal path. Each channel's four feedback paths are internally compensated, which eliminates the need for external compensation capacitors. Additionally, the ADA4352-2 is capable of directly driving an ADC, eliminating the need for a separate ADC driver, and thus reducing the PCB footprint of the overall signal chain.

The analog circuitry can operate on either a single supply (+2.7 V to +5.5 V) or dual supplies (±1.35 V to ±2.75 V). The digital inputs (switch control) operate on supplies between 1.62 V and 5.5 V to interface directly with standard logic levels (1.8 V, 3.3 V, or 5 V) based on the voltage applied to the digital supply (DVSS and DVDD) pins. The voltage levels required for a logic low (V_{IL}) or high (V_{IH}) value are relative to the corresponding digital rail (DVSS and DVDD) (see *Table 1* and *Table 2* for more information).

The switches for channel A and channel B of the ADA4352-2 are controlled by the digital input pins, SW SEL0 A, SW SEL1 A, SW SEL0 B, and SW SEL1 B, respectively. The digital supplies included in the ADA4352-2 provide additional flexibility to control the switch logic independently from the analog supply range. The four internal switch selections are make-before-break to maintain a closed feedback loop during switching to reduce output overdrive glitches that occur otherwise. The SWSEL pins have internal pull-down resistors to DVSS, so the ADA4352-2 defaults to its lowest gain configuration (315 Ω) if the gain select pins are left floating.

To simplify terminology, because the two amplifiers inside the ADA4352-2 are interchangeable, R_{F0}, R_{F1} R_{F2}, R_{F3}, SW SEL0, SW SEL1, +IN, and −IN refer to channel A or channel B. OUT refers to OUT A or OUT B.

PGTIA ERRORS

PGTIA Measurements

The ADA4352-2 is designed for wide dynamic range transimpedance measurements with four internal gain resistors of 315 Ω, 3.5 kΩ, 40.2 kΩ, and 450 kΩ. Additionally, each gain is internally compensated with feedback capacitors of 33 pF, 26.5 pF, 7 pF, and 2.5 pF, respectively. The dominant DC error sources will vary depending on the selected PGTIA gain. When the TIA gain is set to 315 Ω, the majority of the DC error is caused by input offset voltage, while when TIA gain is set to 450 kΩ, the error is dominated by input bias currents and switch off leakage currents.

The PGTIA circuit (see *Figure 68*) models a photodiode input as a parallel current source (I_{IN}), resistor (R_{SH}), and capacitor (C_D) at the inverting input of a closed-loop op amp. Through negative feedback, a virtual reference voltage (V_{CM}) is maintained at the inverting input terminal of the PGTIA. This potential sets the bias voltage for one terminal of the photodiode and allows all the source current to flow through the feedback resistor. Ideally, only signal current from the sensor must flow through the selected gain resistor of the PGTIA. The ideal transfer function of the PGTIA is given by the following equation.

V_{OUT} = Diode current (I_{IN}) × R_{Fx} + V_{CM}

where, R_{Fx} is one of R_{F0}, R_{F1}, R_{F2}, or R_{F3}.

In some cases, large photodiode reverse bias voltage (−V_B) and/or elevated temperatures result in photodiode DC dark current (I_{DARK}), which can be considered both a DC error and current noise source in a photodiode model.

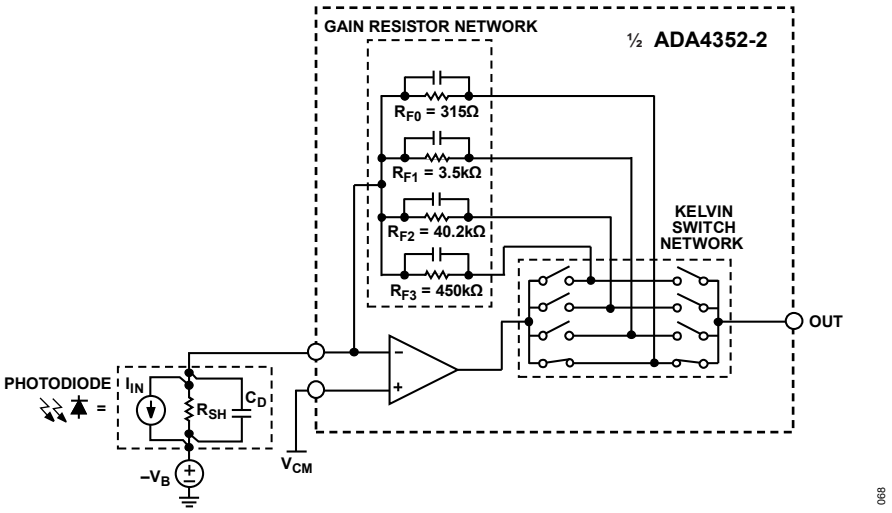


Figure 68. PGTIA Circuit

Input Offset Voltage

The input offset voltage of the amplifier in a PGTIA adds an output DC error (and drift) that is approximately the same for all gain settings. The error at the output of the PGTIA due to the input offset is gained up by the (DC) noise gain of the amplifier (see *Figure 68*).

Noise gain for a typical PGTIA is given by the following equation.

Noise gain = (1 + R_{FX}/R_{SH})

where, R_{SH} is any shunt resistance in the photodiode model.

For R_{SH} >> R_{FX}, noise gain reduces to 1.

Because the offset is a voltage error, it impacts the usable and accurate codes of the ADC for all TIA gains in a similar way. The ADA4352-2 uses proprietary in-package offset and offset-drift trim to minimize this error.

Input Bias Current

In a PGTIA, the noninverting input bias current (I_{B+}) adds to the total output DC error when the +IN source resistance (R_{IN+}) is large. For example, 1 nA of input bias current at the noninverting input adds 1 mV of offset for 1 MΩ of source resistance. Similarly, input bias current at the inverting input (I_{B-}) is only significant at the highest gain setting, as it is multiplied by the gain resistance. These input bias currents increase exponentially with junction temperature (T_J). Typically, for an amplifier with CMOS input devices, the input bias current is dominated by leakage through the electrostatic discharge (ESD) protection diodes. The ADA4352-2 is designed with proprietary architecture to reduce the reverse-biased leakage of these ESD protection diodes on the all sensitive pins.

Switch Off Leakage Current

Only one of the gain-setting integrated switches can be on at any time. Leakage currents from each of the other three open switches (I_{OFF}) and the inverting input bias current (I_{B-}) sum back into the active channel (see *Figure 69*). Both I_{OFF} and I_{B-} increase exponentially with temperature. For a CMOS switch, there is a trade-off between on-resistance (R_{ON}) and I_{OFF}. Another important aspect of CMOS switches is that I_{OFF} increases when operating the switch near the supply rail. Not only does ADA4352-2 have low I_{OFF} switches, but also the low leakage performance extends to 0.1 V from the rail, resulting in a wider usable range for the TIA circuit.

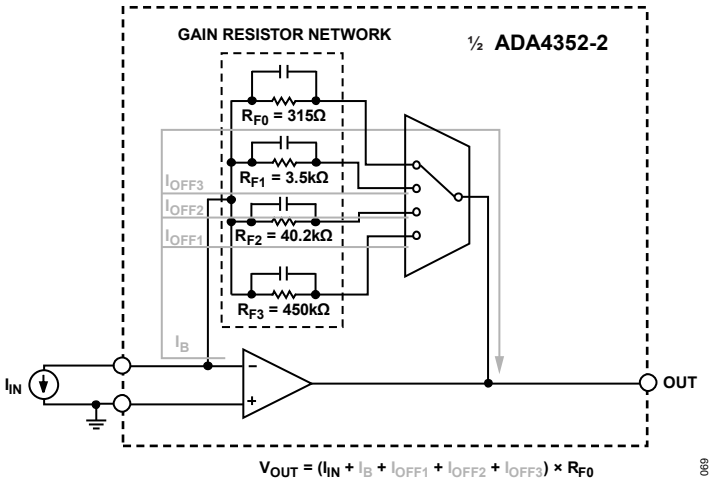


Figure 69. Leakage Current Contributions to Output Voltage Error in the ADA4352-2

Output-Referred Offset Voltage

The output-referred offset voltage is the sum of errors due to the input bias current of the inverting input (I_{B-}), switch off leakage current (I_{OFF}), and input offset voltage. The ADA4352-2 achieves a maximum of 130 µV output offset voltage at 25°C with the lowest selectable gain and 1.1 µV/°C drift from −40°C to +125°C at a 5 V supply.

For example, a 16-bit ADC with a 4.5 V reference has a 68.7 µV step size.

$$ADC\ Step\ Size\ (LSB) = \frac{V_{REF}}{2^N}$$

where, N is the ADC resolution.

For R_{F3} = 450 kΩ, the output-referred offset at 25°C is 150 µV, while the same circuit for R_{F0} = 315 Ω (lowest selectable R_{FX} value) has 130 µV of output-referred offset. In both cases, the output-referred offset is less than three ADC codes. The 1.1 µV/°C (−40°C to +125°C) maximum offset temperature drift leads to a 181 µV shift or a worst case of three additional codes.

The input bias current from the noninverting input (maximum 1 nA) has negligible impact on the TIA circuit accuracy if it adds less than 10 µV (much less than one ADC code) of output-referred offset voltage error. This occurs when the sensor output impedance (R_{SH}) is less than 10 µV/1 nA = 10 kΩ.

If the ADA4352-2 is used in applications measuring a high impedance voltage sensor, the input bias current results in a voltage error at the noninverting input. This error is equal to the sensor output impedance times the bias current (see *Figure 70*). This voltage error is gained up by (1 + R_{FX}/gain resistor (R_G)).

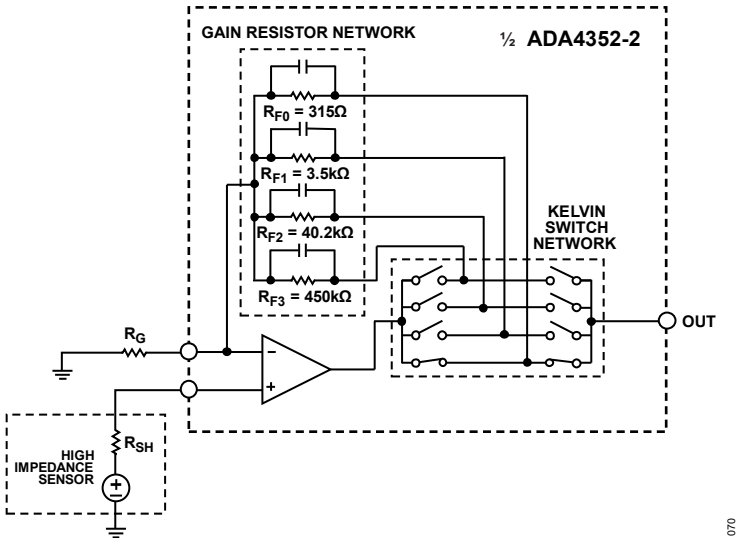


Figure 70. High Impedance Voltage Measurement Using the ADA4352-2

Kelvin Connection and TIA Accuracy

A typical PGTIA places the switches in series with the feedback resistors (see *Figure 71*). Therefore, the switch on-resistance is part of the transimpedance gain. To minimize the error, it is recommended to use gain setting switches with the lowest possible on-resistance. Unfortunately, low impedance switches have large leakage at high operating temperatures. They add leakage current to the sensitive signal path (see *Switch Off Leakage Current*). The improved Kelvin approach used in the ADA4352-2 (see *Figure 72*) places half of the switches inside the loop to provide a Kelvin connection. The on-resistance of the left side switch becomes a part of the open-loop output impedance and is corrected by the loop gain of the amplifier (shown in *Figure 72*). As most PGTIA applications do not need to drive DC current to their load, the on-resistance of the right-side switch does not create additional error. The low on-resistance switches in ADA4352-2 are also designed for low leakage to minimize the error. For traditional PGTIAs, the R_{ON} of the switches changes over temperature and causes gain error drift over temperature. This error is more obvious for the smallest gain (315 Ω range). The ADA4352-2 Kelvin connection approach greatly reduces this error.

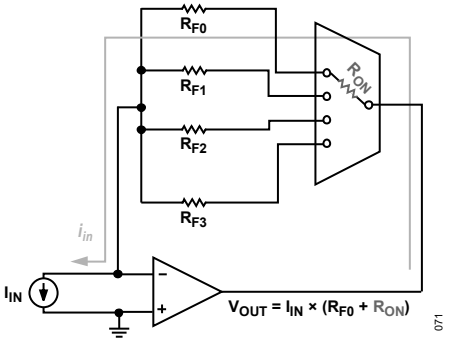


Figure 71. Typical Gain Transimpedance Amplifier with Error due to R_{ON}

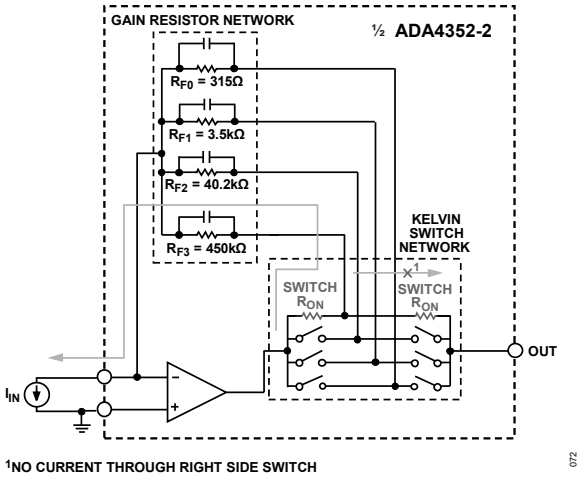


Figure 72. Switched Gain Transimpedance Amplifier with Kelvin Switching

Maximum Linear Input Current Range

Most photodiode PGTIA applications operate in a single supply configuration (see *Figure 73*). Even though ADA4352-2 input pins can swing all the way to ground, the output stage requires at least 0.1 V from either of the supplies to maintain specified linearity.

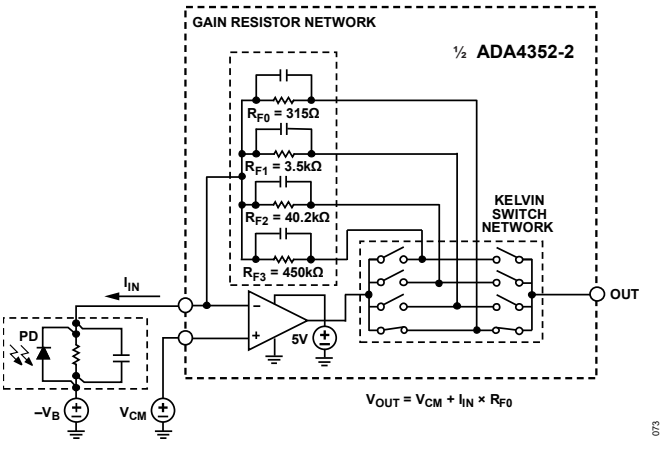


Figure 73. Maximum Linear Output Voltage

Additional voltage headroom is required due to IR drop through the switch resistance. A conservative estimate of the maximum available linear output voltage swing considering these headroom requirements is given by the following equation:

$$V_{O,MAX} = \frac{AVDD - V_{HR}}{1 + \frac{R_{ON}}{R_{FX}}}$$

where:

V_{HR} is the output stage headroom.

R_{ON} is the resistance of the switch inside the loop.

R_{FX} is the gain resistor in the selected loop.

Consequently, the PGTIA maximum linear input current can be calculated by the following equation:

$$I_{IN,MAX} = \frac{V_{O,MAX}}{R_{FX}}$$

For instance, if V_{HR} = 0.1 V, and R_{ON} = 19 Ω over process corners, the resulting maximum linear output voltage $V_{O,MAX}$ from the above equation is 4.62 V for R_{F0} = 315 Ω and 4.9 V for R_{F3} = 450 kΩ. The maximum linear input current that can be pulled from the amplifier in this case is 14.7 mA for R_{F0} = 315 Ω and 10.9 µA for R_{F3} = 450 kΩ. *Table 8* shows maximum linear currents and voltages for various gain settings and supply conditions. Note that the value of the gain resistors can vary by ±11%, which is considered in the *Table 8* values.

The previous example assumed no resistive load, and thus, no IR drop across the switch on the right side in *Figure 73*. If the PGTIA needs to drive a resistive load, there is an IR drop through the right-side switch outside the loop. Careful consideration of these effects is essential to achieve the highest signal path accuracy with maximum available output swing.

The ADA4352-2 also can be used in the applications with photodiodes pushing current into the PGTIA summing node at the inverting input (−IN). The ADA4352-2 input requires 1.5 V headroom from the positive supply to maintain specified linearity. Therefore, linear output voltage swing and linear input current are lower for this configuration (see *Table 8*).

Table 8. Maximum Linear Output Currents and Voltages

		R_{F0} = 315 Ω		R_{F1} = 3.5 kΩ		R_{F2} = 40.2 kΩ		R_{F3} = 450 kΩ	
		V_S = 5 V	V_S = 3 V	V_S = 5 V	V_S = 3 V	V_S = 5 V	V_S = 3 V	V_S = 5 V	V_S = 3 V
Sensor pulls current out	$V_{O,MAX}$ (V)	4.65	2.65	4.88	2.88	4.90	2.90	4.90	2.90
	I_{PULL} (mA)	13.41	7.64	1.27	0.75	0.11	0.065	0.01	0.006
Sensor pushes current in	$V_{O,MAX}$ (V)	3.22	1.28	3.38	1.39	3.40	1.40	3.40	1.40
	I_{PUSH} (mA)	9.30	3.69	0.88	0.36	0.077	0.031	0.07	0.003

ESD Protection

The ADA4352-2 is fabricated on a low-voltage CMOS process. To protect the device from electrostatic discharge (ESD), all pins have reverse-biased ESD protection diodes, as shown in *Figure 74*. The ADA4352-2 also has several

shunt supply clamps to protect its two supply domains, AVDD/AVSS and DVDD/DVSS. The ADA4352-2 has a pair of back-to-back diodes to protect the inputs during ESD strikes.

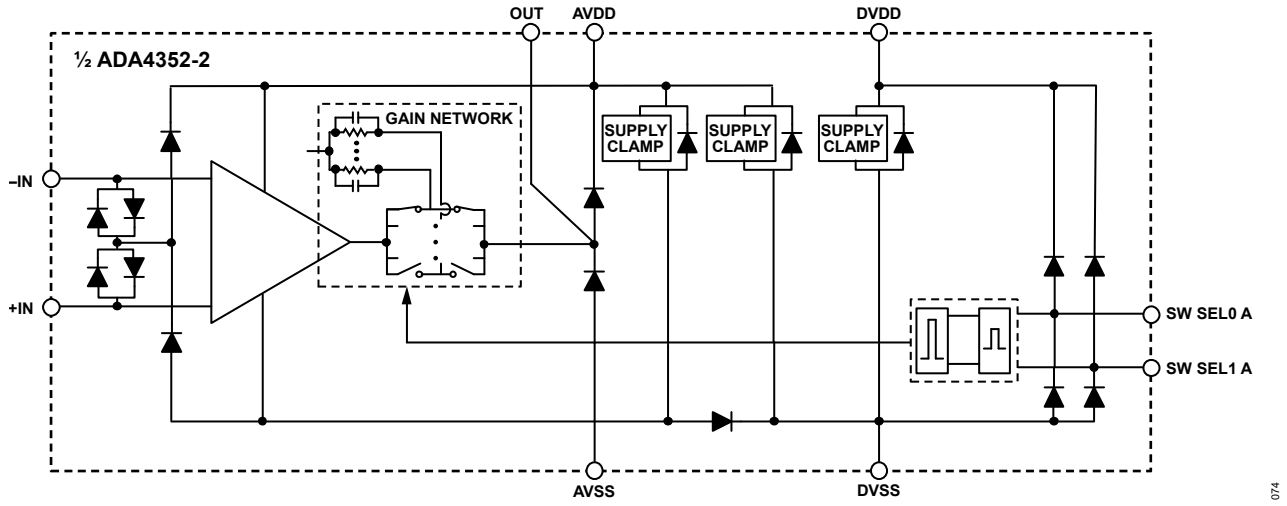


Figure 74. Simplified Internal ESD Schematic Diagram

MAIN AMPLIFIER (CMOS)

Rail-to-Rail Output Stage

The maximum detectable signal in the PGTIA is limited by the input and output operating range of the amplifier. To maintain the best accuracy, the common-mode voltage V_{CM} at the noninverting input must be biased at least 0.1 V above the negative supply.

The negative supply (AVSS) must be less than ground (0 V) for PGTIA applications that require the output to swing all the way to ground. This configuration is possible for the ADA4352-2, because the digital supplies (DVDD and DVSS) and analog supplies (AVDD and AVSS) are independent.

The ADA4352-2 is designed with a rail-to-rail output stage and can operate to within 100 mV from the power supplies with A_{VOL}> 110 dB, which provides flexibility for the system and eases design constraints.

Bottom Rail Input Stage

The V_{CM} is constrained by the input common-mode range of the main amplifier. In a single-supply configuration, V_{CM} also sets the minimum output voltage value in a TIA design. Therefore, the dynamic range is constrained between V_{CM} and the maximum ADC input voltage. The ADA4352-2 is designed with a PMOS input differential pair to allow the analog inputs to swing to AVSS, where AVSS can be set to as much as 0.5 V less than DVSS. It is less common in TIA designs for the input common-mode voltage across the inputs to approach the positive supply. The ADA4352-2 input stage requires 1.5 V headroom to the positive supply.

Low Noise Operation

In a transimpedance amplifier, having low op-amp input voltage noise is particularly crucial. At low frequency, the noise gain is near 1 V/V. However, at higher frequencies, the noise gain increases from unity due to source capacitance. Additionally, more noise is integrated (per decade) at higher frequencies, which contributes to the total output integrated noise. While there is usually a design trade-off between noise and power consumption, the ADA4352-2 contributes 7.3 nV/√Hz of wideband noise while requiring only 3.3 mA per channel.

Current Noise

When using large transimpedance gains (that is, 450 kΩ), the current noise of the main amplifier can be a major source of noise in a system. The current noise flows through the feedback resistor and appears at the output as a voltage (current noise × R_{FX}). Also, if the photodiode is reverse-biased, its dark current noise contribution can, in some cases, become the dominant current noise term.

In CMOS amplifiers, the input current noise increases over frequency and, therefore, can have a major impact on the total integrated noise. The ADA4352-2 is designed to have low current noise, but it increases with frequency. A 110 fA/√Hz flat current noise spectral density from 10 kHz to 100 kHz is used in the *Photodiode Circuit Design Wizard* to represent the worst case high frequency noise.

Using a TIA gain of 450 kΩ, the Johnson noise of the resistor itself at the output is 86 nV/√Hz (at room temperature), while the gained-up 110 fA/√Hz current noise spectral density of the amplifier at 10 kHz is a comparable 49.5 nV/√Hz. These current noise sources are usually insignificant compared to the voltage noise contribution (refer to the “Noise Contributions for Transimpedance Amplifiers” section in the *ADA4351-2 data sheet*).

APPLICATIONS INFORMATION

RC Tolerancing

The ADA4352-2's internal R_{FX} and C_{FX} values come with the typical tolerancing for IC elements. The R_{FX} values have their nominal ±11% tolerance, while their associated C_{FX} values are specified with ±20% tolerance. The R_{FX} variation is normally calibrated out to correct each of the gain slopes. The C_{FX} variation modifies the TIA frequency response and changes the pulse responses at the TIA output (V_{OUT}). *Table 9* summarizes the specified R_{FX} and C_{FX} ranges, and the resulting feedback pole (P1) range.

Table 9. Specified R_{FX} and C_{FX} Tolerancing Ranges and Feedback Pole, P1

Nom R_{FX}	Min R_{FX}	Max R_{FX}	Nom C_{FX}	Min C_{FX}	Max C_{FX}	Max P_1	Nom P_1	Min P_1
kΩ	kΩ	kΩ	pF	pF	pF	MHz	MHz	MHz
0.315	0.28	0.35	33	26.4	39.6	21.5	15.3	11.5
3.5	3.1	3.9	26.5	21.2	31.8	2.4	1.7	1.3
40.2	36	45	7	5.6	8.4	0.8	0.57	0.4
450.0	400.5	499.5	2.5	2	3	0.2	0.14	0.11

where, $P_1 = \frac{1}{2\pi \times R_{FX} \times C_{FX}}$

All these R_{FX} selections have the same range of variation that can be calibrated out. The biggest impact of this R_{FX}, C_{FX} tolerancing is for R_{F0} = 315 Ω, where the response shows peaking even with a relatively small assumed diode source capacitance (C_D) of 10 pF at the ADA4352-2's input.

Adding an external RC filter of R_{EXT} = 200 Ω and C_{EXT} = 180 pF at the TIA output, using 1% tolerance resistors and 2% tolerance capacitors, significantly reduces peaking in the frequency response when using R_{F0} = 315 Ω. The F_{-3dB} frequencies of the higher gains R_{F1} to R_{F3} are already well below the external RC filter cutoff frequency. So, they are not impacted by the external RC filter.

The Monte Carlo plot of *Figure 75* shows both the ADA4352-2's response variation due to internal tolerances of R_{F0} = 315 Ω and C_{F0} = 33 pF, and the subsequent improvement in peaking due to adding the external RC filter. Note that the ADA4352-2 LTspice model that produces the plot of *Figure 75* is configured with only the nominal internal $R_{FX}||C_{FX}$ values.

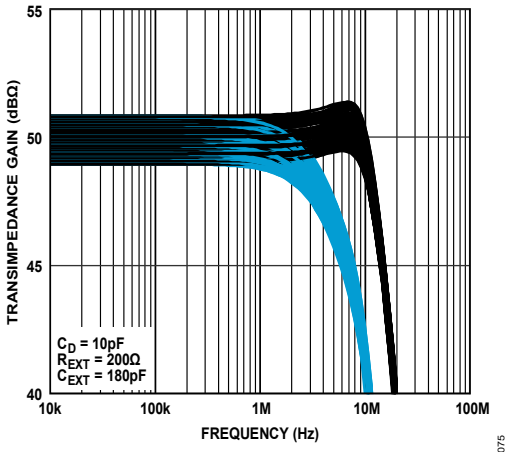


Figure 75. Monte Carlo of PGTIA Frequency Response for R_{F0} = 315Ω Nominal without (Black) and with External RC Filter (Blue) with C_D = 10 pF

RC Tolerancing and Effect of External RC Filter

This external RC filter also adds more control to the step response for the most peaked 315 Ω gain condition. The following step responses assume an R_{EXT} = 200 Ω, C_{EXT} = 180 pF, as used previously, a 0.5 V bias at +IN, C_D of 10 pF, and the part configured in the 315 Ω gain setting. The 1 V output step response in *Figure 76* shows how the external RC filter smooths the PGTIA ringing response.

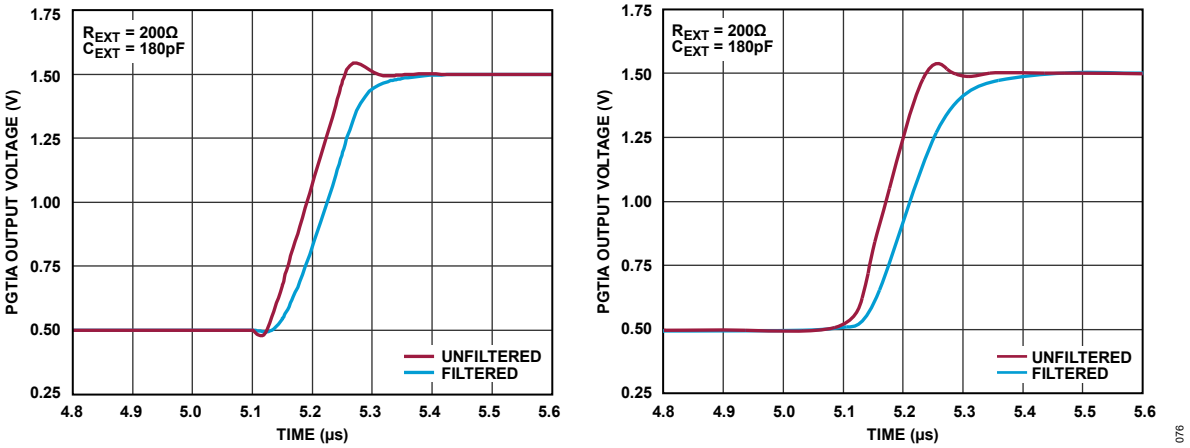


Figure 76. Simulated (Left) and Measured (Right) 1 V Output Step at the Nominal 315 Ω Gain Setting at both V_{OUT} and after the External RC Filter

The three groups of curves in *Figure 77* show the effects of extremes of component tolerance on step response. Here, the minimum R_{F0} and C_{F0} values are used together, then the nominal values, and then the maximum R_{F0} and C_{F0} values. All curves in *Figure 77* were produced with the same input current, which would result in a 1 V output step using a nominal R_{F0} = 315 Ω gain setting. The two extremes settle to a lower and higher final value, but all show the same settling behavior after the external RC filter.

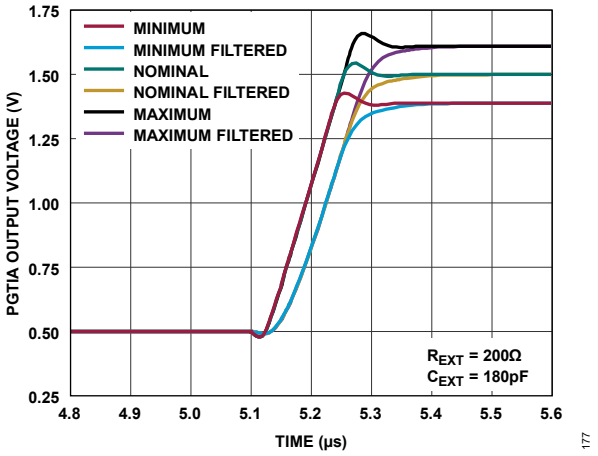


Figure 77. Simulated 1 V Output Step with Internal RC Tolerancing Extremes at the Nominal 315 Ω Gain Setting, with and without External RC Filter

Frequency Response Variation with Diode Capacitance C_D

External diode capacitance (C_D) values interact with the ADA4352-2's various internal feedback resistance and capacitance pairs ($R_{FX}||C_{FX}$) to give a range of frequency response curves. The lowest (315 Ω) R_{F0} value, which results in a F_{-3dB} bandwidth greater than 10 MHz, shows increased peaking in the frequency response as the C_D increases from 5 pF to 25 pF, and finally to 45 pF. This resulting response is normally bandlimited by the typically <5 MHz RC filter following the PGTIA into a SAR ADC (see *RC Tolerancing and Effect of External RC Filter*). In all cases, it is important to remember the ADA4352-2 adds a total of 5.5 pF parasitic input common-mode and differential capacitance (C_{CM} + C_{DIFF}) to C_D.

The family of output response curves in the left half of *Figure 78* shows the effect of changing the value of C_D to 5 pF, 25 pF, or 45 pF at the R_{F0} = 315 Ω gain setting. As the diode capacitance is increased, the frequency response exhibits more peaking and the corresponding F_{-3dB} point moves slightly lower in frequency.

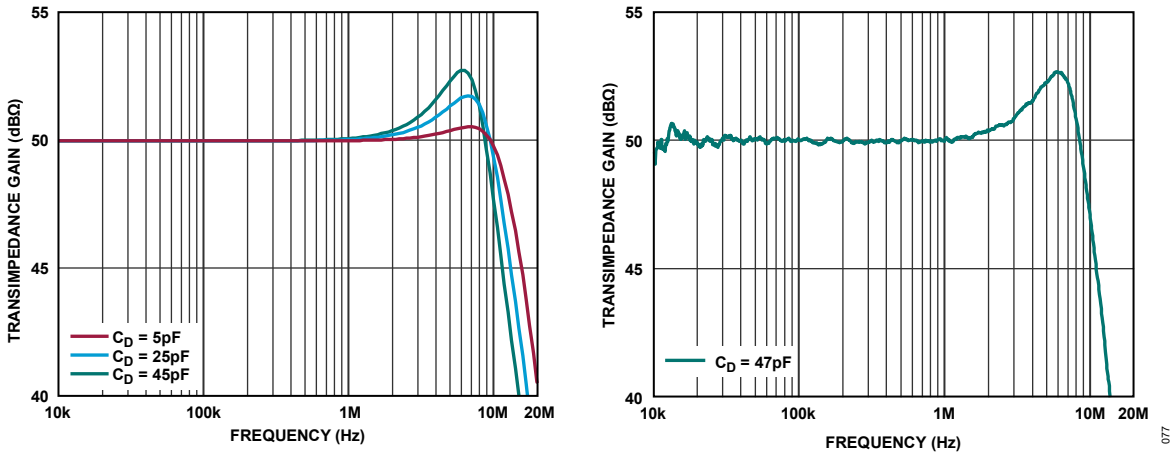


Figure 78. Simulated (Left) and Measured (Right) Frequency Response at V_{OUT} for Various C_D Values, R_{F0} = 315 Ω. Measured Curve with C_D = 47 pF Shown for Worst Case Peaking Comparison

The gains R_{F0} through R_{F3} are displayed in dBΩ in frequency response plots. *Table 10* provides the conversions from linear gains to their logarithmic equivalents to clarify the frequency response plots in this section.

Table 10. Nominal R_{FX} and Equivalent Logarithmic Gain for All Gain Settings of ADA4352-2

Nominal R_{FX} Value (Ω)	Nominal R_{FX} Value (dBΩ)	Gain Step (dBΩ)	Internal C_{FX} Value (pF)
315	50	NA	33
3.5k	71	21	26
40.2k	92	21	7.0
450k	113	21	2.5

The following curves in *Figure 79* to *Figure 82*, which show how the frequency response changes with C_D, are generated in LTspice.

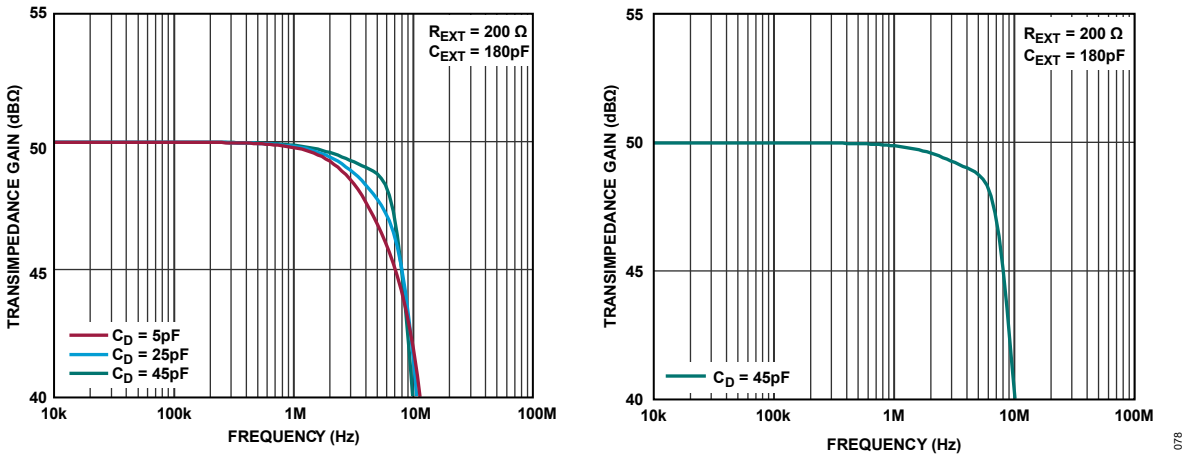


Figure 79. Simulated (Left) and Worst Case (Right) Frequency Response After External Filter for Various C_D Values, R_{F0} = 315 Ω.

Adding an RC filter at the output pin of the PGTIA with a roll off at 4.4 MHz results in the family of curves shown in *Figure 79*. As C_D increases, the increasing gain peaking of the PGTIA output nudges the gain upwards at frequencies beyond the 4.4 MHz single pole roll off, causing an apparent bandwidth extension after the external filter.

For all gain settings higher than R_{F0} = 315 Ω, varying C_D does not cause peaking in the frequency responses, as they are much more bandlimited to begin with. The external RC filter simply bandlimits the ADC input and slightly reduces integrated noise.

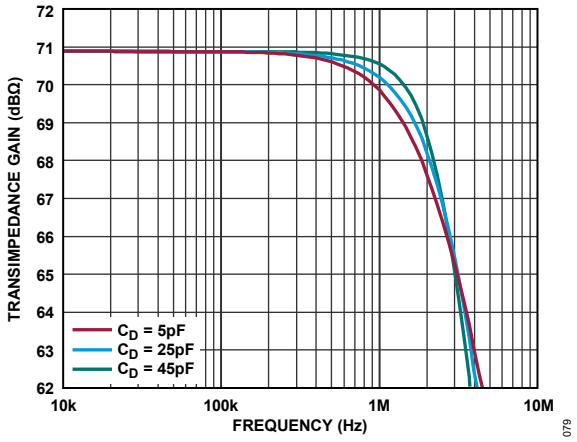


Figure 80. Simulated Frequency Response for Various C_D Values, R_{F1} = 3.5 kΩ

The next higher gain, the R_{F1} = 3.5 kΩ, C_{F1} = 26.5 pF nominal internal feedback setting, results in this family of response curves (*Figure 80*) at the PGTIA output. Here, the F_{-3dB} is increasing as the C_D is changed from 5 pF to 25 pF, and finally to 45 pF. This results from the frequency response poles moving from a simple 2-real pole response to a higher quality factor (Q) 2nd order response, while remaining clustered around 2 MHz. Refer to the "TIA Design Theory" in the *ADA4351-2* data sheet for a more in-depth discussion of the TIA 2nd order frequency response, including how Q and f_o set the frequency response shape.

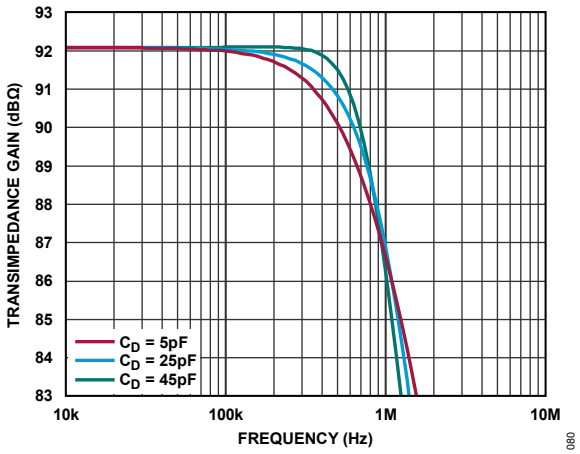


Figure 81. Simulated PGTIA Frequency Response for Various Values of C_D, R_{F2} = 40.2 kΩ

As the selected gain moves up to the next R_{F2} = 40.2 kΩ, C_{F2} = 7 pF setting, the response curves become even more bandlimited, but F_{-3dB} still increases as C_D increases. Again, the output is changing from an overcompensated 2-real pole response to a higher Q flat response, as C_D increases from 5 pF to 25 pF, and then 45 pF. These response curves are all clustered around 700 kHz F_{-3dB} for this gain setting, as shown in *Figure 81*.

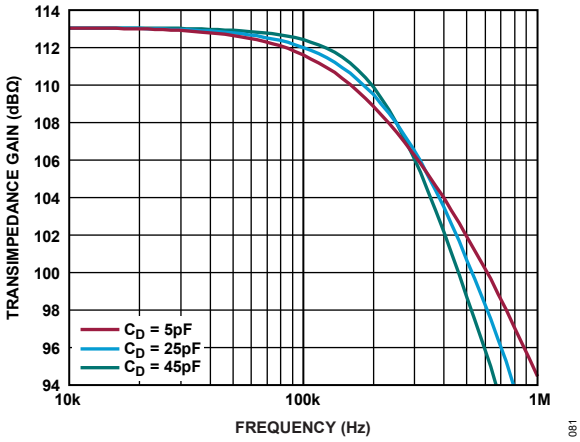


Figure 82. Simulated PGTIA Frequency Response for Various Values of C_D, R_{F3} = 450 kΩ

The highest R_{F3} = 450 kΩ, C_{F3} = 2.5 pF gain setting gives the most bandlimited response. Again, as the C_D increases from 5 pF to 25 pF and finally to 45 pF, the frequency response is moving from two real poles to a response with a higher Q and extended bandwidth. These are all clustered around a 170 kHz F_{-3dB}, as shown in *Figure 82.*

Increasing C_D beyond 45 pF continues to make the frequency response poles more complex, with possibly significant peaking. Carefully consider these effects if a higher C_D is needed using the available simulation model.

Using the ADA4352-2 LTspice Model

Figure 83 shows the available LTspice model for the ADA4352-2 used to generate many of the parametric and Monte Carlo curves shown in this applications section.

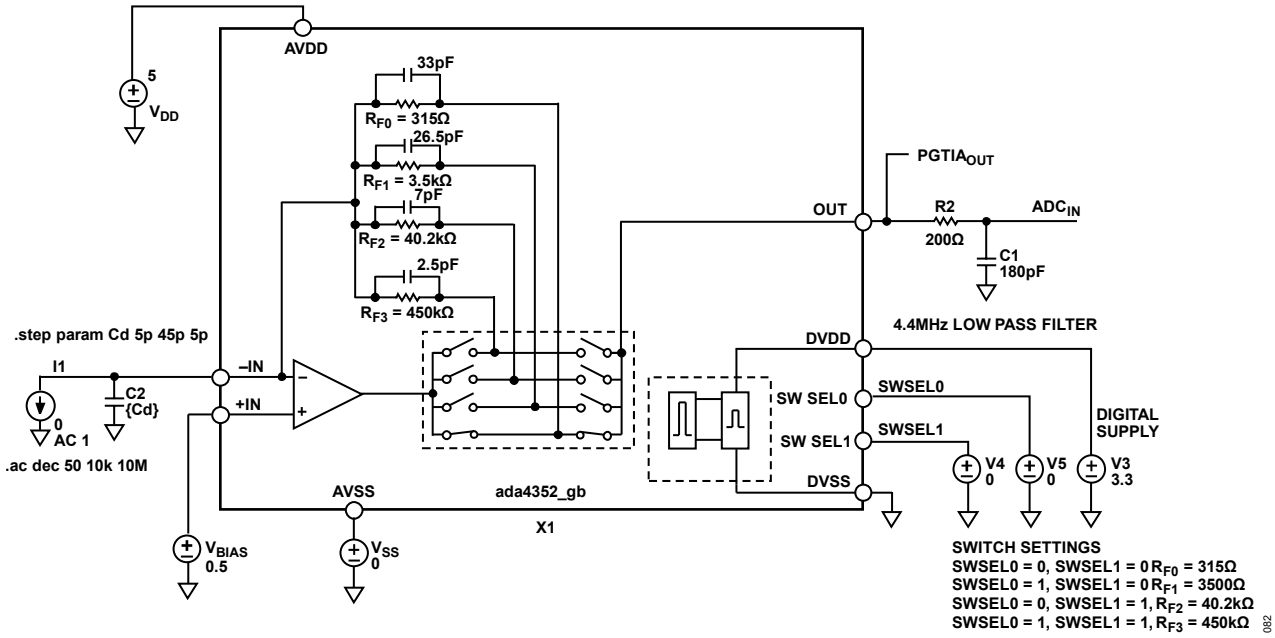


Figure 83. ADA4352-2 LTspice Model Setup for the Swept CD Curves Using the 315 Ω Gain Setting

The example simulation of *Figure 83* is set up for a stepped CD plot similar to that in *Figure 79* using the lowest gain setting of 315 Ω. Consider these configurations in any application simulation:

1. Set the PGTIA power supplies, AVDD = 5 V and AVSS = ground, here for single supply operation.
2. Set the DC bias on the +IN pin. This must be at least 0.1 V higher than AVSS and 1.5 V below AVDD for proper operation. Here, a 0.5 V bias is used. The polarity of the diode current (I1) guarantees that the output only increases from that 0.5 V level.
3. Set values for desired photodiode equivalent model parameters, such as source capacitance (C2 here) at desired reverse bias voltage, and parasitic shunt resistance (not shown in *Figure 83*) at the maximum intended operating temperature.
4. The digital switch control inputs, SW SEL0 and SW SEL1, must be set for the desired gain setting, as detailed in *Figure 83*. Usually, these control voltages are set to either 0 V at DVSS for a logic 0 or to the digital supply voltage DVDD (V3 here) for a logic 1.
5. There is usually an external RC filter after the PGTIA output to the SAR ADC. The values here come from the 16-bit 1 MSPS SAR *AD4696 data sheet*.

Error Budget

The input offset error of the ADA4352-2 is constant across all gain settings because TIA noise gain is approximately 1 for all gain ranges. This simplifies the error budget because most DC error terms due to the PGTIA are combined in Output Offset Voltage ($V_{OS,OUT}$). This term is a result of three components: the switch off leakage current (I_{OFF}), input bias current of the inverting input, and offset voltage of the core amplifier. The only other source of error is the effect of noninverting input bias current flowing through the source impedance at the noninverting input.

The following equation shows the “Total Output DC Offset Error” at room temperature.

Total output DC offset error (at 25°C) = $V_{OS,OUT}$ + (I_{B+} x R_{IN+})

where, I_{B+} is the input bias current at the noninverting input.

R_{IN+} is the source resistance at the noninverting input.

If the noninverting resistance is kept at a minimum, the I_{B+} × R_{IN+} term is insignificant.

There are other sources of DC error while using the ADA4352-2 : the gain error, and error due to CMRR and PSRR. The error contributions from CMRR and PSRR can be reduced using accurate supplies and calibration, and are typically negligible at DC for a TIA application.

There is also a gain error term because of the resistor tolerance. The equation for this error term is given by I_{IN} x ΔR_{FX}, where, I_{IN} is the photodiode current and ΔR_{FX} is the deviation from the nominal value of R_{Fx} in ohms.

Combining ADA4352-2 with a 16-Bit SAR ADC

The ADA4352-2 can be used to directly drive a successive approximation register (SAR) ADC. The slew rate of the ADA4352-2 allows for fast output settling within the acquisition time specification of the ADC. The ADA4352-2 also draws low supply current and can thus be paired with low power, high resolution ADCs for a low power precision signal chain.

Typical ADA4352-2 Optical Signal Chain Application

Figure 84 shows a typical single-supply application using the AD4696, a high accuracy, low power, 16-channel, 16-bit SAR ADC to measure an optical signal level using a photodiode. Between the output of the ADA4352-2 and the analog front-end of the ADC is an external low-pass filter formed by R_{EXT} and C_{EXT}.

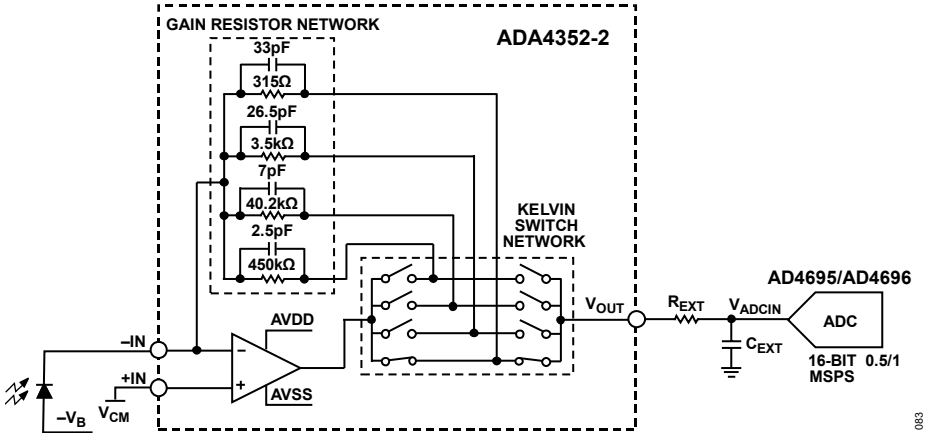


Figure 84. Optical Signal Chain with ADA4352-2 and AD4696

External RC Filter Design Considerations for SAR ADC Driving

As seen in previous sections, the RC filter at the output is used for several purposes. For ADC driving applications, this external RC filter also serves to limit both wideband noise into the ADC, and nonlinear kickback from the ADC inputs into the amplifier output.

Selecting the RC filter between the PGTIA output and ADC input is an iterative process, and the best combination depends on the intended application. For example, in lower frequency applications, opt for a higher value RC to

introduce less noise, but also make sure that this RC combination allows the signal to settle within the acquisition time specified for the desired sample rate of the ADC.

As in the section on *RC Tolerancing and Effect of External RC Filter*, assume R_{EXT} = 200 Ω and C_{EXT} = 180 pF. For the R_{F0} = 315 Ω gain setting, ADA4352-2's dominant pole lies beyond the external RC filter's bandwidth. The RC filter usually limits the system bandwidth and thus also the noise bandwidth. For the rest of the R_{FX} gain settings, the poles created by ADA4352-2's internal resistors and their respective compensation capacitors roll off at a much lower frequency than the external RC filter. For these higher R_{FX} settings, this external RC filter does not contribute to noise reduction. See *Table 9* for minimum, nominal, and maximum bandwidths for each gain setting.

Using the AD4696 Easy Drive ADC's Input Settings

The *AD4696* Easy Drive ADC provides the option of using high-Z mode at its analog inputs, which precharges the switched capacitor networks of its MUX and SAR ADC without adding noise. This mode eases driver demands on the ADA4352-2 output stage. It greatly limits the current that the ADA4352-2's output must provide when the AD4696's sampling switches close at the beginning of its acquisition period and protects it from nonlinear kickback that can significantly affect precision and linearity. Reducing this current also reduces the DC voltage error due to R_{EXT}. Enabling high-Z mode in the AD4696 helps the overall signal chain achieve better SNR, THD, and DC accuracy.

Achieving Low Input Bias Current

There are several factors to consider in a low input bias current circuit. Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of picoamp signals. At the picoamp level, leakage current can come from unexpected sources, including adjacent traces on the PCB (on the same layer or even from internal layers), contamination on the PCB (from the assembly process or the environment), or other components on the signal path. The ADA4352-2's internal feedback resistors provide an advantage here as they are protected from external leakage currents into the feedback path. Nevertheless, the system should be designed to mitigate these sources and preserve optimal performance.

An appropriate cleaning process is essential after assembly to avoid leakages from solder flux and other contaminants. Relative humidity also must be considered because PCB materials and the plastic mold compound of the package itself can absorb moisture and cause additional leakage paths.

PCB Layout Cautions and Considerations

TIAs are extremely sensitive to parasitic capacitance at their inputs, as the capacitance directly reduces their bandwidth and increases noise gain. A stray capacitance as low as 5 pF can greatly impact system performance, especially if the capacitance of the photodiode used is around the same order of magnitude as the board parasitics.

Stripping the ground plane around the input trace is crucial for minimizing parasitic capacitance at the input, and also makes it more difficult for leakage currents from the PCB to couple into the signal path and cause output errors. As the ADA4352-2's feedback resistors are internal, there is no need to strip ground plane around the feedback path, saving board space that would be required for both external resistors and the removed ground plane around them. However, the signal trace at the inverting input is still susceptible to leakage current and must be protected.

It is important to keep the high impedance signal path as short as possible on the PCB. A high impedance node is susceptible to picking up any stray signals in the system; therefore, keeping the path as short as possible reduces this effect. Additionally, the longer the signal trace into the PCB (on the inverting input), the more stray capacitance at the input of the PGTIA.

To minimize picking up stray high frequency signals on the same board, other signal traces must be routed well away from the TIA's signal path, and there must be no internal power planes under the high impedance node. The best defense from coupling signals is shielding; however, this increases capacitance in the area, which impacts the noise gain of the PGTIA. Another method to decouple signals is distance, which includes vertical layers of the PCB as well as on the surface of the PCB. The package of the ADA4352-2 simplifies board layout because there is no exposed pad (EPAD) on the back side of the package, eliminating the need for vias and allowing routing on all layers of the PCB beneath the device.

In cases where the space is limited, it is recommended to cut slots in the PCB around the high impedance input nodes to provide additional isolation and to reduce the impact of contamination on the surface of the PCB.

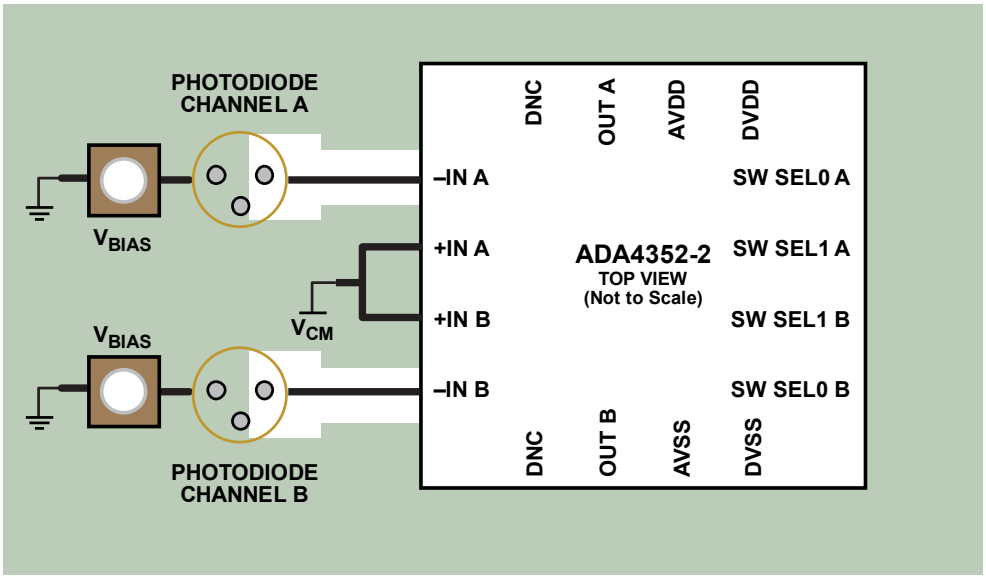


Figure 85. Example PCB Layout for Low Surface Leakage

Board Space Saving Compared to Equivalent Discrete Solution

Due to its integrated switches and resistors, ADA4352-2 uses 8.6% of the board area of a similar discrete solution with separate resistors and switches. In the layout comparison in *Figure 86,* ADA4352-2 provides 4 gain settings per channel, while the other two solutions only provide 2 per channel.

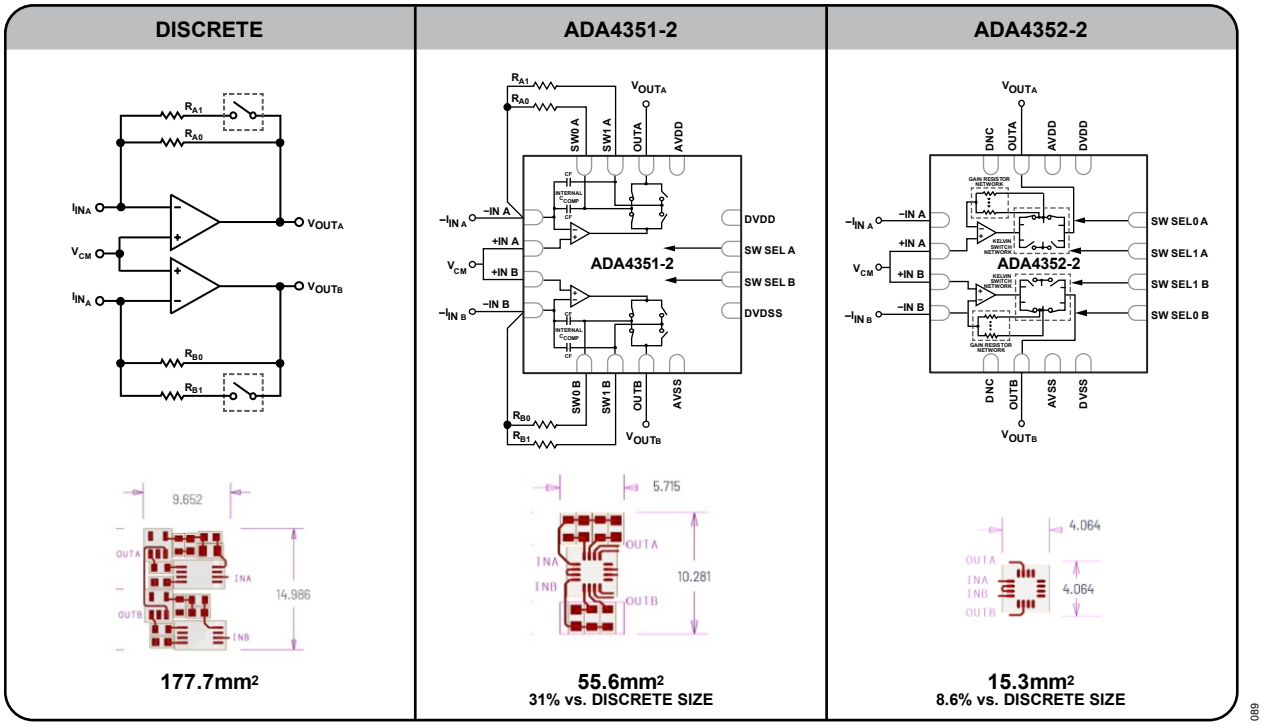
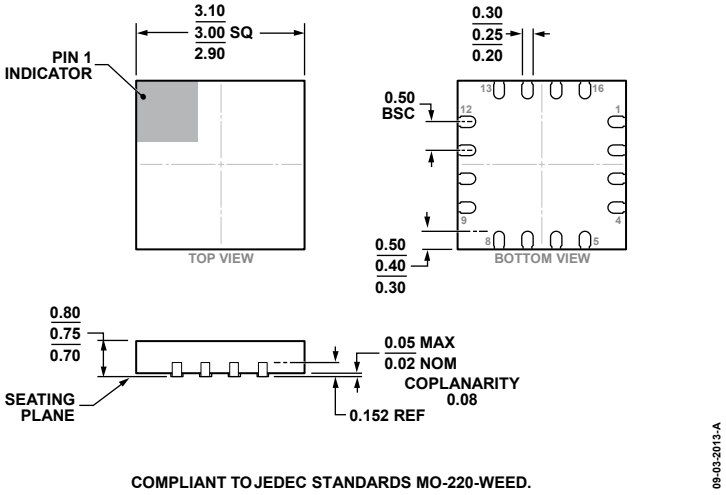


Figure 86. Comparison in Footprint Size for a Similar Discrete Solution, ADA4351-2, and ADA4352-2

OUTLINE DIMENSIONS



ORDERING GUIDE

Table 11. Ordering Guide

Model	Temperature Range	Package Description	Packaging Quantity	Package Option	Marking Code
ADA4352-2ACPZ	−40°C to +125°C	16-Lead LFCSP	Tray, 714	CP-16-32	A4Q
ADA4352-2ACPZ-R7	−40°C to +125°C	16-Lead LFCSP	Reel, 1500	CP-16-32	A4Q
ADA4352-2ACPZ-RL	−40°C to +125°C	16-Lead LFCSP	Reel, 5000	CP-16-32	A4Q

EVALUATION BOARD

Table 12. Evaluation Board

Model	Description
EVAL-ADA4352-2EBZ	Evaluation Board

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Analog Devices Inc.:

ADA4352-2ACPZ-RL ADA4352-2ACPZ ADA4352-2ACPZ-R7