EVALUATION KIT AVAILABLE

MAX77962

23V_{IN} 3.2A_{OUT} USB-C Buck-Boost Charger with Integrated FETs for 2S Li-Ion Batteries

General Description

The MAX77962 is a high-performance wide-input 3.2A buck-boost charger with a Smart Power Selector™ and operates as a reverse buck without an additional inductor, allowing the IC to power USB On-the-Go (OTG) accessories. The device integrates low-loss power switches, and provides small solution size, high efficiency, low heat, and fast battery charging. The reverse buck has true-load disconnect and is protected by an adjustable output current limit. The device is highly flexible and programmable through I^2C configuration or autonomously through resistor configuration.

The battery charger includes a Smart Power Selector to accommodate a wide range of battery sizes and system loads. The Smart Power Selector allows the system to start up gracefully when an input source is available even when the battery is deeply discharged (dead battery) or missing. For battery safety/authentication reasons, the IC can be configured to keep charging disabled, and allow the DC-DC to switch and regulate the SYS voltage. The system processor can later enable charging using the appropriate I^2C commands. Alternatively, the IC can be configured to automatically start charging.

Applications

- USB Type-C Powered Wide-Input Charging Applications
- 2-Cell Battery Powered Devices

Benefits and Features

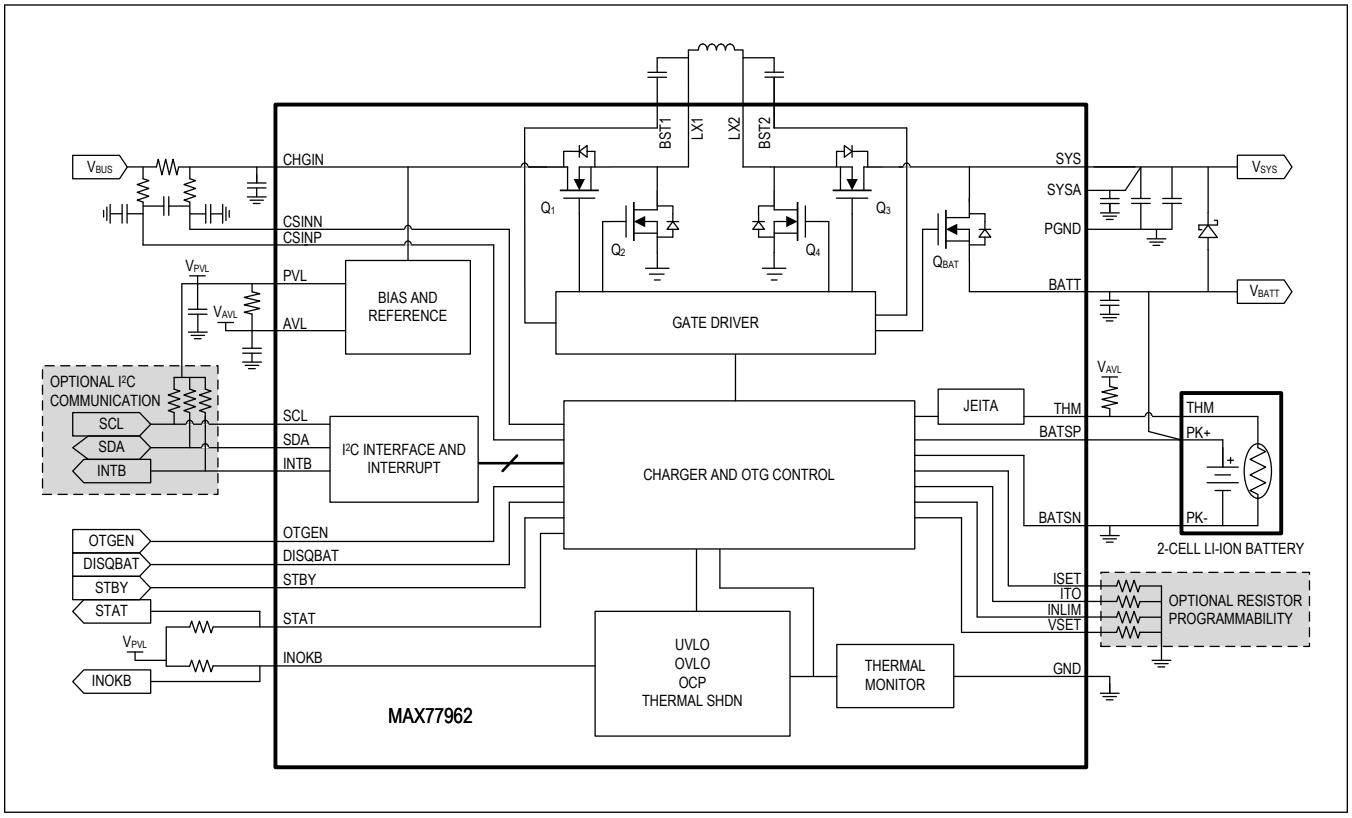
- 3.5V to 23V Input Operating Range, 30V_{DC} Withstand Voltage
- 97% Peak Efficiency at 9V_{IN}/7.4V_{OUT}/1.5A_{OUT}
- Reverse Leakage Protection
- 50mA to 3.15A Programmable Input Current Limit
- 50mA to 3.2A Programmable Constant Current Charge
- Remote Differential Voltage Sensing
- 600kHz or 1.2MHz Switching Frequency Options
- System Instant On with Smart Power Selector PowerPath
- Charge Safety Timer
- Die Temperature Regulation with Thermal Foldback Loop
- Input Power Management with Adaptive Input Current Limit (AICL) and Input Voltage Regulation
- 10mΩ BATT to SYS Switch, Up to 10A Overcurrent Threshold
- Reverse Buck Mode 5.1V/1.5A to Support USB OTG
- JEITA Compliant with NTC Thermistor Monitor
- I^2C or Resistor Programmable
- 3.458mm x 3.458mm 49-Bump WLP

Analog Devices is in the process of updating documentation to provide culturally appropriate terminology and language. This is a process with a wide scope and will be phased in as quickly as possible. Thank you for your patience.
Smart Power Selector is a trademark of Maxim Integrated Products, Inc.

Ordering Information *appears at end of data sheet.*

19-100812; Rev 2; 5/24

Simplified Block Diagram



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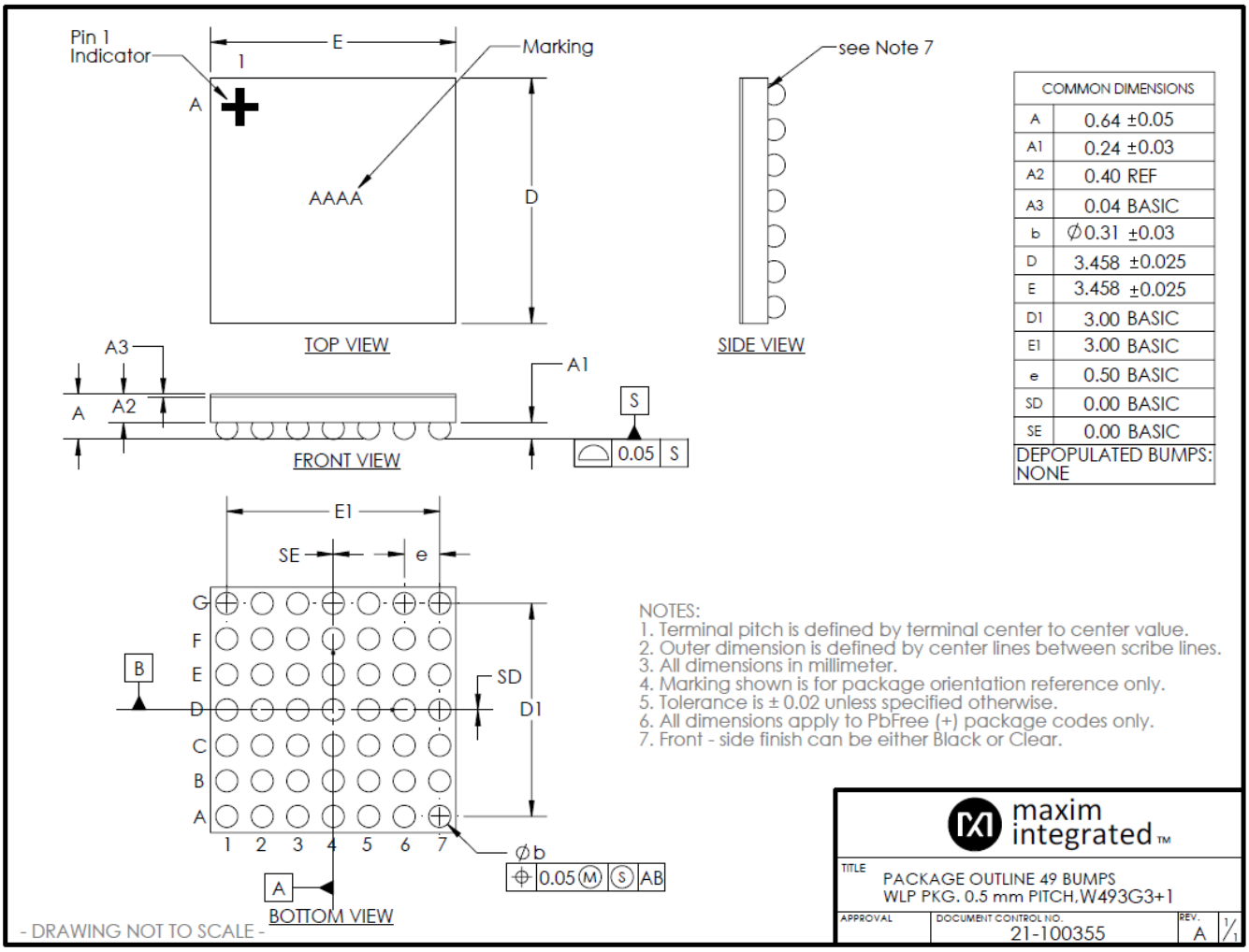
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

49-Bump WLP

Package Code	W493G3+1
Outline Number	**21-100355**
Land Pattern Number	Refer to ***Application Note 1891***
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	34.87°C/W



For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL ELECTRICAL CHARACTERISTICS						
CHGIN Voltage Range	V_{CHGIN}	Operating voltage	3.5		23.0	V
CHGIN Overvoltage Threshold	V_{CHGIN_OVLO}	V_{CHGIN} rising, 300mV hysteresis	23.0	23.7	24.3	V
CHGIN Overvoltage Delay	$t_{D\_CHGIN\_OVLO}$	V_{CHGIN} rising, 100mV overdrive		10		µs
		V_{CHGIN} falling, 100mV overdrive		7		ms
CHGIN Undervoltage Threshold	V_{CHGIN_UVLO}	V_{CHGIN} rising, 20% hysteresis	3.43	3.5	3.57	V
CHGIN Quiescent Current (I_{SYS} = 0A)	I_{CHGIN}	V_{CHGIN} = 2.4V, the input is undervoltage and R_{INSD} is the only loading		0.075		mA
		V_{CHGIN} = 9.0V, charger disabled		0.17	0.5	
		V_{CHGIN} = 9.0V, charger enabled, V_{SYS} = V_{BATT} = 8.7V, no switching		2.7	4	
	I_{CHGIN_STBY}	MODE[3:0] = 0x0 (DC-DC off), STBY = H or STBY_EN = 1, V_{CHGIN} = 5 V			1	
BATT Quiescent Current (I_{SYS} = 0A)	I_{SHDN}	FSHIP_MODE = 1 or STBY = H, V_{CHGIN} = 0V, I_{SYS} = 0A		2.3	5.0	µA
	I_{BATT}	I^2C enabled, V_{CHGIN} = 0V, I_{SYS} = 0A, V_{BATT} = 8.86V		100	200	
		V_{SYS} = 7.6V, V_{BATT} = 0V, charger disabled, T_A = +25°C		0.01	10	
		V_{SYS} = 7.6V, V_{BATT} = 0V, charger disabled, T_A = +85°C		10		
	I_{BATTDN}	V_{CHGIN} = 9V, V_{BATT} = 8.4V, Q_{BAT} is off, battery-overcurrent protection disabled, charger is enabled but in its done mode, T_A = +25°C		57	65	
		V_{CHGIN} = 9V, V_{BATT} = 8.4V, Q_{BAT} is off, battery-overcurrent protection disabled, charger is enabled but in its done mode, T_A = +85°C		57		
SYS Operating Voltage	V_{SYS}	Guaranteed by $V_{SYSUVLO}$ and $V_{SYSOVLO}$	SYSUVLO rising		SYSOVLO rising	V
SYS Undervoltage-Lockout Threshold	$V_{SYSUVLO}$	V_{SYS} falling, 530mV hysteresis	3.95	4.1	4.25	V
SYS Overvoltage-Lockout Threshold	$V_{SYSOVLO}$	V_{SYS} rising, 430mV hysteresis	10.45	10.73	11.00	V
PVL Output Voltage	V_{PVL}		1.7	1.8	1.9	V
Thermal-Shutdown Threshold	T_{SHDN}	T_J rising		165		°C
Thermal-Shutdown Hysteresis				15		°C
CHGIN Self-Discharge Resistance	R_{INSD}	V_{CHGIN} = 3V		44		kΩ

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BATT Self-Discharge Resistance	R_{BATSD}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 5V		600		Ω
SYS Self-Discharge Resistance	R_{SYSSD}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 5V		600		Ω
Self-Discharge Latch Time				300		ms
SWITCH MODE CHARGER / CHARGER						
BATT Regulation Voltage Range	$V_{BATTREG}$	Programmable from 8.10V to 8.86V; production tested at 8.4V and 8.8V only	8.10		8.86	V
BATT Regulation Voltage Accuracy		8.7V setting, T_A = +25°C	-0.9	-0.3	+0.3	%
		8.7V setting, T_A = 0°C to +85°C (Note 1)	-1	-0.3	+0.5	
BATT Overvoltage-Lockout Threshold	$V_{BATTOVLO}$	V_{BATT} rising above $V_{BATTREG}$, 2% hysteresis	75	240	375	mV/cell
BATT Undervoltage-Lockout Threshold	$V_{BATTUVLO}$	V_{BATT} rising, 100mV hysteresis	2.0	2.5	3.0	V
Fast-Charge Current Program Range	I_{FC}	50mA to 3193.75mA; production tested at 500, 1000, and 3000mA settings	50		3193.75	mA
Fast-Charge Current Accuracy		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 50mA	30	50	70	mA
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 100mA	80	100	120	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 300mA	289	300	311	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 500mA	481	500	519	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 1000mA	962	1000	1038	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 1500mA	1444	1500	1556	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3000mA	2887	3000	3113	
		T_A = +25°C, V_{BATT} > V_{SYSMIN}, programmed for 3193.75mA	3074	3194	3314	
Fast-Charge Current Accuracy (Over Temperature)		-40°C < T_A < +85°C, V_{BATT} > V_{SYSMIN}, programmed for 200mA or less (Note 1)	-20		+20	mA
		-40°C < T_A < +85°C, V_{BATT} > V_{SYSMIN}, programmed for greater than 200mA (Note 1)	-5		+5	%
CHGIN Adaptive Voltage Regulation Range	V_{CHGIN_REG}	I^2C programmable	4.025		19.05	V
CHGIN Adaptive Voltage Regulation Accuracy		4.55V setting	4.42	4.55	4.68	V

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN Current Limit Range	CHGIN_ILIM	Programmable, 500mA default; production tested at 100mA, 500mA, 1000mA, and 3000mA settings only	50		3150	mA
CHGIN Current Limit Accuracy		Charger enabled, 50mA input current setting, T_A = +25°C	44	49	54	mA
		Charger enabled, 100mA input current setting, T_A = +25°C	88	98	108	
		Charger enabled, 300mA input current setting, T_A = +25°C	285	293	300	
		Charger enabled, 500mA input current setting, T_A = +25°C	475	488	500	
		Charger enabled, 1000mA input current setting, T_A = +25°C	950	975	1000	
		Charger enabled, 1500mA input current setting, T_A = +25°C	1425	1463	1500	
		Charger enabled, 3000mA input current setting, T_A = +25°C	2850	2925	3000	
		Charger enabled, 3150mA input current setting, T_A = +25°C	2993	3071	3150	
CHGIN Current Limit Accuracy (Over Temperature)		Charger enabled and operating in a mode that is not force-buck-boost mode, 200mA or less input current setting, -40°C < T_A < +85°C (Note 1)	-22.5		+17.5	%
		Charger enabled and operating in a mode that is not force-buck-boost mode, greater than 200mA input current setting, -40°C < T_A < +85°C (Note 1)	-7.5		+2.5	
CHGIN Current Limit Error During Force-Buck-Boost Operation (Overtemperature)		Charger enabled, force-buck-boost operation, input current setting from 50mA to 1.6A, -40°C < T_A < +85°C (Note 1)		16	40	mA
Precharge Voltage Threshold	V_{PRECHG}	V_{BATT} rising, voltage threshold per cell	2.4	2.5	2.6	V/Cell
Precharge Current	I_{PRECHG}		21.875	31.25	40.625	mA
Prequalification Threshold Hysteresis	V_{PQ-H}	Applies to V_{PRECHG}		150		mV/Cell
Minimum SYS Voltage Accuracy	V_{SYSMIN}	Programmable from 5.535V to 6.970V, V_{BATT} = 5.6V; tested at 3V/cell setting	-3		+3	%
Trickle Charge Current	$I_{TRICKLE}$	Default setting = enabled; ITRICKLE[1:0] = 00	93.75	125	156.25	mA
		Default setting = enabled; ITRICKLE[1:0] = 01 (Note 1)	187.5	250	312.5	
		Default setting = enabled; ITRICKLE[1:0] = 10 (Note 1)	218.25	375	468.75	
		Default setting = enabled; ITRICKLE[1:0] = 11	375	500	625	

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Top-Off Current Program Range	I_{TO}	Programmable from 25mA to 150mA	25		150	mA
Charge Termination Deglitch Time	t_{TERM}	2mV overdrive, 100ns rise/fall time		160		ms
Charger Restart Threshold Range	V_{RSTRT}	Program options for disabled, 100mV/cell, 150mV/cell, and 200mV/cell with CHG_RSTRT[1:0]	100		200	mV/Cell
Charger Restart Deglitch Time		10mV overdrive, 100ns rise time		130		ms
Charger State Change Interrupt Deglitch Time	t_{SCIDG}	Excludes transition to timer fault state, watchdog timer state		30		ms
SWITCH MODE CHARGER / CHARGE TIMER						
Prequalification Time	t_{PQ}	Applies to both low-battery prequalification and dead-battery prequalification modes		30		min
Fast-Charge Constant Current + Fast-Charge Constant Voltage Time	t_{FC}	Adjustable from 3hrs, 4hrs, 5hrs, 6hrs, 7hrs, 8hrs, and 10hrs including a disable setting; 3hrs default		3		hrs
Top-Off Time	t_{TO}	Adjustable from 30sec to 70min in 10min steps		30		min
SWITCH MODE CHARGER / WATCHDOG TIMER						
Watchdog Timer Period	t_{WD}	(Note 2)	80			s
SWITCH MODE CHARGER / BUCK-BOOST						
CHGIN OK to Start Switching Delay	t_{START}	Delay from INOKB H → L to LX_ start switching		150		ms
Buck-Boost Current Limit	HSILIM	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V	4.3	5	5.7	A
SWITCH MODE CHARGER / BUCK-BOOST / SWITCH IMPEDANCE AND LEAKAGE CURRENT						
LX1 High-Side Resistance	R_{LX1_HS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		15.4	26	mΩ
LX1 Low-Side Resistance	R_{LX1_LS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		18.2	30	mΩ
LX2 High-Side Resistance	R_{LX2_HS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		12.3	18	mΩ
LX2 Low-Side Resistance	R_{LX2_LS}	V_{CHGIN} = 9V, V_{SYS} = V_{BATT} = 7.6V		21	33	mΩ
LX_ Leakage Current		LX1 = PGND or CHGIN, LX2 = PGND or SYS, T_A = +25°C		0.01	10	µA
		LX1 = PGND or CHGIN, LX2 = PGND or SYS, T_A = +85°C		1		
BST_ Leakage Current		BST_ = 1.8V, T_A = +25°C		0.01	10	µA
		BST_ = 1.8V, T_A = +85°C		1		

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS, SYSA Leakage Current		V_{SYS} = V_{SYSA} = 8.4V, V_{BATT} = 0V, Charger Disabled, T_A = +25°C		0.01	10	µA
		V_{SYS} = V_{SYSA} = 8.4V, V_{BATT} = 0V, Charger Disabled, T_A = +85°C		1		
CSINP, CSINN Leakage Current	I_{CSINP}, I_{CSINN}	V_{CHGIN} = 23.7V, V_{CSINP} = V_{CSINN} = 23.7V, T_A = +25°C	-1		+1	µA
SWITCH MODE CHARGER / SMART POWER SELECTOR						
BATT to SYS Dropout Resistance	$R_{BAT2SYS}$			10	17	mΩ
BATT to SYS Reverse Regulation Voltage	V_{BSREG}			90		mV
SWITCH MODE CHARGER / BATT TO SYS OVERCURRENT ALERT						
Battery Overcurrent Threshold Range	I_{BOVCR}	Programmable from 3A to 10A; option to disable	3		10	A
Battery Overcurrent Debounce Time	t_{BOVRC}	Response time for generating the overcurrent interrupt (Note 2)			3.3	ms
SWITCH MODE CHARGER / THERMAL FOLDBACK						
Junction Temperature Thermal Regulation Loop Setpoint Program Range	TREG	Junction temperature when charge current is reduced; programmable from 85°C to 130°C in 5°C steps; default value is 115°C	85		130	°C
Thermal Regulation Gain	A_{TJREG}	The charge current is decreased 5% of the fast-charge current setting for every degree that the junction temperature exceeds the thermal regulation temperature. This slope ensures that the full-scale current of 3.2A is reduced to 0A by the time the junction temperature is 20°C above the programmed loop set point. For lower programmed charge currents such as 480mA, this slope is valid for charge current reductions down to 80mA; below 100mA the slope becomes shallower but the charge current still reduced to 0A if the junction temperature is 20°C above the programmed loop set point.		-5		%/°C
SWITCH MODE CHARGER / THERMISTOR MONITOR						
THM Threshold, COLD	THM_COLD	V_{THM}/V_{AVL} rising, 1% hysteresis (thermistor temperature falling)	73.36	74.56	75.76	%
THM Threshold, COOL	THM_COOL	V_{THM}/V_{AVL} rising, 1% hysteresis (thermistor temperature falling)	58.8	60	61.2	%
THM Threshold, WARM	THM_WARM	V_{THM}/V_{AVL} falling, 1% hysteresis (thermistor temperature rising)	33.68	34.68	35.68	%
THM Threshold, HOT	THM_HOT	V_{THM}/V_{AVL} falling, 1% hysteresis (thermistor temperature rising)	21.59	22.5	23.41	%

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
THM Threshold, Disabled		V_{THM}/V_{AVL} falling, 1% hysteresis, THM function is disabled below this voltage	4.9	5.9	6.9	%
THM Threshold, Battery Removal Detection		V_{THM}/V_{AVL} rising, 1% hysteresis, battery removal	85.6	87	88.4	%
THM Input Leakage Current		V_{THM} = GND or V_{AVL}; T_A = +25°C		0.1	1	µA
		V_{THM} = GND or V_{AVL}; T_A = +85°C (Note 1)		0.1		
REVERSE BUCK						
Buck Current Limit	HSILIM_REV	F_{SW} = 600kHz	4.3	5	5.7	A
Reverse Buck Quiescent Current		Not switching: output forced 200mV above its target regulation voltage		1150		µA
Minimum BATT Voltage in OTG Mode	$V_{BATT.MIN.OTG}$	V_{BATT} = V_{SYS}, SYS UVLO falling threshold in OTG mode	5.96	6.14	6.32	V
CHGIN Voltage in OTG Mode	$V_{CHGIN.OTG}$	V_{BATT} = $V_{BATT.MIN.OTG}$, OTGEN = H	4.94	5.1	5.26	V
CHGIN Undervoltage Threshold in OTG Mode	$V_{CHGIN.OTG.UV}$	V_{CHGIN} falling, OTGEN = H		85		%
CHGIN Overvoltage Threshold in OTG Mode	$V_{CHGIN.OTG.OV}$	V_{CHGIN} rising, OTGEN = H		110		%
CHGIN Output Current Limit in OTG Mode	$I_{CHGIN.OTG.LIM}$	V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b000, OTGEN = H		500	550	mA
		V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b001, OTGEN = H		900	990	
		V_{BATT} = $V_{BATT.MIN.OTG}$, T_A = +25°C, OTG_ILIM[2:0] = 0b011, OTGEN = H		1500	1650	
CHGIN Output Voltage Ripple in OTG Mode		Continuous inductor current, OTGEN = H		±150		mV
IO CHARACTERISTICS						
R_{INLIM}, R_{ISET}, R_{VSET}, R_{TO} Resistor Range	$R_{PROG\_}$		5.49		226	kΩ
Output Low Voltage INOKB, STAT		I_{SINK} = 1mA, T_A = +25°C			0.4	V
Output High Leakage INOKB, STAT		5.5V, T_A = +25°C	-1	0	+1	µA
		5.5V, T_A = +85°C		0.1		
DISQBAT, OTGEN, STBY Logic Input Low Threshold	V_{IL}				0.4	V
DISQBAT, OTGEN, STBY Logic Input High Threshold	V_{IH}		1.4			V
DISQBAT, OTGEN, STBY Logic Input Leakage Current		5.5V (including current through pulldown resistor)		5.5	10	µA
DISQBAT, OTGEN, STBY Pulldown Resistor	$R_{DISQBAT}$			1000	1200	kΩ

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INTERFACE / I²C INTERFACE AND INTERRUPT						
SCL, SDA Input Low Level					0.3 x V_{AVL}	V
SCL, SDA Input High Level			0.7 x V_{AVL}			V
SCL, SDA Input Hysteresis				0.05 x V_{AVL}		V
SCL, SDA Logic Input Current		SDA = SCL = 5.5V	-10		+10	µA
SCL, SDA Input Capacitance				10		pF
SDA Output Low Voltage		Sinking 20mA			0.4	V
Output Low Voltage INTB		I_{SINK} = 1mA			0.4	V
Output High Leakage INTB		V_{INTB} = 5.5V, T_A = +25°C	-1	0	+1	µA
		V_{INTB} = 5.5V, T_A = +85°C		0.1		
INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Setup Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Valid Time	$t_{VD:DAT}$				0.45	µs
DATA Valid Acknowledge Time	$t_{VD:ACK}$				0.45	µs
DATA Setup time	$t_{SU;DAT}$		50			ns
Setup Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns
INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 100pF)						
Clock Frequency	f_{SCL}				3.4	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns

Electrical Characteristics (continued)

(V_{SYS} = 7.6V, V_{BATT} = 7.6V, V_{CHGIN} = 9V, T_A = -40°C to +85°C. Typical values are at T_A = +25°C. Limits are production tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

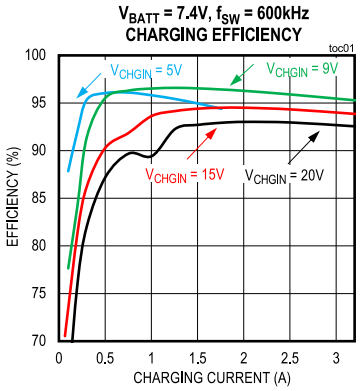
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		160			ns
CLK High Period	t_{HIGH}		60			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns
INTERFACE / I²C-COMPATIBLE INTERFACE TIMING FOR HS-MODE (C_B = 400pF)						
Clock Frequency	f_{SCL}				1.7	MHz
Setup Time Repeated START Condition	$t_{SU;STA}$		160			ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160			ns
CLK Low Period	t_{LOW}		320			ns
CLK High Period	t_{HIGH}		120			ns
DATA Setup time	$t_{SU;DAT}$		10			ns
DATA Hold Time	$t_{HD:DAT}$		0			ns
Setup Time for STOP Condition	$t_{SU;STO}$		160			ns
Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		ns

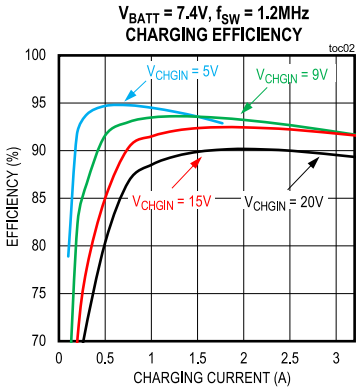
Note 1: Guaranteed by design. Not production tested.

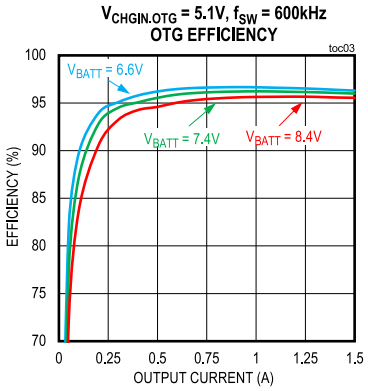
Note 2: Guaranteed by design. Production tested through scan.

Typical Operating Characteristics

(C_{CHGIN} = 10µF, C_{SYS} = 2 x 47µF, L = 3.3µH (XAL4030-332ME), T_A = +25°C unless otherwise noted.)

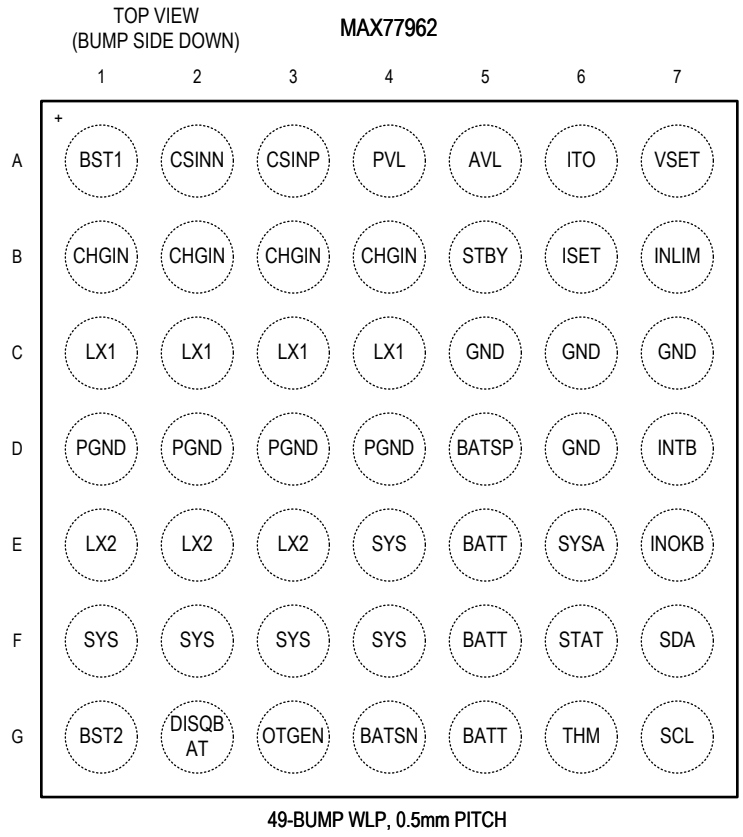






Bump Configuration

MAX77962



49-BUMP WLP, 0.5mm PITCH

Bump Descriptions

PIN	NAME	FUNCTION
A1	BST1	High-Side Input MOSFET Driver Supply. Bypass BST1 to LX1 with a 0.22µF/6.3V capacitor.
B1, B2, B3, B4	CHGIN	Buck-Boost Charger Input. CHGIN is also the buck output when the charger is operating in the reverse mode. Bypass with two 10µF/35V ceramic capacitors from CHGIN to PGND.
C1, C2, C3, C4	LX1	Inductor Connection One. Connect an inductor between LX1 and LX2.
D1, D2, D3, D4	PGND	Power Ground for Buck-Boost Low-Side MOSFETs
E1, E2, E3	LX2	Inductor Connection Two. Connect an inductor between LX1 and LX2.
E4, F1, F2, F3, F4	SYS	System Supply Output. Bypass SYS to PGND with a minimum of two 22µF/16V ceramic capacitors.
G3	OTGEN	Active-High Input. Connecting the OTGEN pin to high enables the OTG function. When the OTGEN pin is pulled low, the OTG enable function is controlled by the I^2C interface. Before enabling the OTG function, disable skip mode with DISKIP = 1. To pull the OTGEN pin low with a pulldown resistor, the resistance must be lower than 44kΩ.
G2	DISQBAT	Active-High Input. Connect high to disable the integrated Q_{BAT} FET between SYS and BATT. Charging is disabled when DISQBAT connects to high. When DISQBAT is pulled low, Q_{BAT} FET control is defined in Table 1. To pull the DISQBAT pin low with a pulldown resistor, the resistance must be lower than 44kΩ.
G1	BST2	High-Side Output MOSFET Driver Supply. Bypass BST2 to LX2 with a 0.22µF/6.3V capacitor.
G4	BATSN	Battery Voltage Differential Sense Negative Input. Connect to the negative terminal of the battery pack.
D5	BATSP	Battery Voltage Differential Sense Positive Input. Connect to the positive terminal of the battery pack.
E5, F5, G5	BATT	Battery Power Connection. Connect to the positive terminal of the battery pack. Bypass BATT to PGND with a 10µF/16V capacitor. All BATT pins must be connected together externally.
G6	THM	Thermistor Input. Connect a negative temperature coefficient (NTC) thermistor from THM to GND. Connect a resistor equal to the thermistor +25°C resistance from THM to AVL. JEITA controlled charging available with JEITA_EN = 1. Charging is suspended when the thermistor voltage is outside of the hot and cold limits. Connect THM to GND to disable the thermistor temperature sensor. Connect THM to AVL to emulate battery removal and prevent charging.
G7	SCL	Serial Interface I^2C Clock Input
F7	SDA	Serial Interface I^2C Data. Open-drain output.
F6	STAT	Charger Status Output. Active-low, open-drain output, connect to the pullup rail through a 200kΩ resistor. Pulls low when the charging is in progress. Otherwise, STAT is high impedance. STAT toggles between low and high (when connected to a pullup rail) during charge. STAT becomes low when top-off threshold is detected and charger enters done state. STAT becomes high (when connected to a pullup rail) when charge faults are detected.
E7	INOKB	Input Power-OK/OTG Power-OK Output. Active-low, open-drain output pulls low when the CHGIN voltage is valid.
D7	INTB	Active-Low, Open-Drain Interrupt Output. Connect a pullup resistor to the pullup power source.
E6	SYSA	SYS voltage sensing input for SYS UVLO and OVLO detection.
C5, C6, C7, D6	GND	Analog Ground
B7	INLIM	Charger Input Current Limit Setting Input. Connect a resistor (R_{INLIM}) from INLIM to GND programs the charger input current limit. See Table 4.
B6	ISET	Fast-Charge Current Setting Input. Connecting a resistor (R_{ISET}) from ISET to GND programs the fast-charge current. See Table 5.

Bump Descriptions (continued)

PIN	NAME	FUNCTION
A7	VSET	Charge Termination Voltage Setting Input. Connecting a resistor (R_{VSET}) from VSET to GND programs the charge termination voltage. See Table 7.
A6	ITO	Top-Off Current Setting Input. Connecting a resistor (R_{ITO}) from ITO to GND programs the top-off current. See Table 6.
A5	AVL	Analog Voltage Supply for On-Chip, Low-Noise Circuits. Bypass with a 4.7µF/6.3V ceramic capacitor to GND and connect AVL to PVL with a 4.7Ω resistor.
A4	PVL	Internal Bias Regulator High Current Output Bypass Pin. Supports internal noisy and high current gate drive loads. Bypass to PGND with a 4.7µF/6.3V ceramic capacitor, and connect AVL to PVL with a 4.7Ω resistor. Powering external loads from PVL is not recommended, other than pullup resistors.
B5	STBY	Active-High Input. Connect high to disable the DC-DC between CHGIN input and SYS output. Battery supplies the system power if the Q_{BAT} is on. See Table 1. Connect low to control the DC-DC with the power-path state machine. To pull the STBY pin low with a pulldown resistor, the resistance must be lower than 44kΩ.
A3	CSINP	Input Current Sense Positive Input
A2	CSINN	Input Current Sense Negative Input

Detailed Description

Charger Configuration

The MAX77962 is a highly-flexible, highly-integrated switch mode charger. Autonomous charging inputs configure the charger without host I^2C interface. See the *Autonomous Charging* section for more details. The IC has an I^2C interface which allows the host controller to program and monitor the charger. Charger configuration registers, interrupt, interrupt mask, and status registers are described in the *Register Map*.

CHGIN Standy Input (STBY)

The host can reduce the ICs CHGIN supply current by driving the STBY pin to high or setting the STBY_EN bit to '1'. When STBY is pulled high or STBY_EN bit is set to '1', the DC-DC turns off. When STBY is pulled low and STBY_EN bit is set to '0', the DC-DC is controlled by the power-path state machine. To pull the STBY pin low with a pulldown resistor, the resistance must be lower than 44kΩ.

Battery to SYS Q_{BAT} Disable Input (DISQBAT)

The host can disable the Q_{BAT} switch by setting the DISIBS bit to 1 or driving the DISQBAT pin to high. Charging stops when the Q_{BAT} switch is disabled.

When DISQBAT is pulled low and DISIBS bit is set to 0, Q_{BAT} FET control is defined in Table 1. To pull the DISQBAT pin low with a pulldown resistor, the resistance must be lower than 44kΩ.

Q_{BAT} and DC-DC Control—Configuration Table

The Q_{BAT} control and the DC-DC control depend on both hardware pins (OTGEN, DISQBAT and STBY) and their associated I^2C registers.

Table 1. Q_{BAT} and DC-DC Control Configuration Table

OTGEN (PIN) OR MODE [3:0] = 0xA (I^2C)	DISQBAT (PIN)	DISIBS (I^2C)	STBY (PIN)	STBY_EN (I^2C)	CHGIN	Q_{BAT}	DC-DC
0	Low	0	Low	0	x	Power-Path State Machine/Internal Logic Control	Power-Path State Machine/Internal Logic Control
				1	x	Enable (SYS is powered from battery through Q_{BAT} switch while DC-DC is disabled)	Disable
			High	x	Valid		
					Invalid	Disable **(factory ship mode)**	Disable **(factory ship mode)**
0	Low	1	Low	0	x	Disable	Power-Path State Machine/Internal Logic Control
				1	x	Disable (SYS is powered from battery through Q_{BAT} body diode while DC-DC is disabled)	Disable
			High	x	Valid		
					Invalid	Disable **(factory ship mode)**	Disable **(factory ship mode)**
	High	x	Low	0	x	Disable	Power-Path State Machine/Internal Logic Control

Table 1. Q_{BAT} and DC-DC Control Configuration Table (continued)

OTGEN (PIN) OR MODE [3:0] = 0xA (I^2C)	DISQBAT (PIN)	DISIBS (I^2C)	STBY (PIN)	STBY_EN (I^2C)	CHGIN	Q_{BAT}	DC-DC
				1	x	Disable (SYS is powered from battery through Q_{BAT} body diode while DC-DC is disabled)	Disable
			High	x	x		
1	x	x	x	x	x	Enable (if not in factory ship mode)	Power-Path State Machine/Internal Logic Control (if not in factory ship mode)

Thermistor Input (THM)

The thermistor input can be utilized to achieve functions that include charge suspension, JEITA compliant charging, and battery removal detection. The thermistor monitoring feature can be disabled by connecting the THM pin to ground.

Charge Suspension

The THM input connects to an external negative temperature coefficient (NTC) thermistor to monitor battery or system temperature. Charging stops when the thermistor temperature is out of range ($T < T_{COLD}$ or $T > T_{HOT}$). The charge timers are reset. The CHG_DTLS[3:0] and CHG_OK register bits report the charging suspension status, and the CHG_I interrupt bit is set. When the thermistor comes back into range ($T_{COLD} < T < T_{HOT}$), charging resumes and the charge timer restarts.

JEITA Compliant Charging

JEITA compliant charging is available with JEITA_EN = 1. See the *JEITA Compliance* section for more details.

Battery Removal Detection

Connecting THM to AVL emulates battery removal and prevents charging.

Disable Thermistor Monitoring

Connecting THM to GND disables the thermistor monitoring function, and JEITA controlled charging is unavailable in this configuration. The IC detects an always connected battery when THM is grounded, and charging starts automatically when a valid adapter is plugged in. In applications with removable batteries, do not connect THM to GND because the IC cannot detect battery removal when THM is grounded. Instead, connecting THM to the thermistor pin in the battery pack is recommended.

Since the thermistor monitoring circuit employs an external bias resistor from THM to AVL, the thermistor is not limited only to 10kΩ (at +25ºC). Any resistance thermistor can be used as long as the value is equivalent to the thermistors +25ºC resistance. For example, with a 10kΩ at R_{TB} resistor, the charger enters a temperature suspend state when the thermistor resistance falls below 3.97kΩ (too hot) or rises above 28.7kΩ (too cold). This corresponds to a 0ºC to +50ºC range when using a 10kΩ NTC thermistor with a beta of 3500. The general relation of thermistor resistance to temperature is defined by the following equation:

$$R_T = R_{25} x e^{\{\beta x (\frac{1}{T+273^\circ C} - \frac{1}{298^\circ C})\}}$$

where:

R_T = The resistance in Ω of the thermistor at temperature T in Celsius.

R_{25}= The resistance in Ω of the thermistor at +25ºC.

β = The material constant of the thermistor, which typically ranges from 3000k to 5000k.

T = The temperature of the thermistor in °C.

Some designs might prefer other thermistor temperature limits. Threshold adjustment can be accommodated by changing R_{TB}, connecting a resistor in series and/or in parallel with the thermistor, or using a thermistor with different β. For

example, a +45ºC hot threshold and 0°C cold threshold can be realized by using a thermistor with a β to 4250 and connecting 120kΩ in parallel. Since the thermistor resistance near 0ºC is much higher than it is near +50ºC, a large parallel resistance lowers the cold threshold, while only slightly lowering the hot threshold. Conversely, a small series resistance raises the hot threshold, while only slightly raising the cold threshold. Raising R_{TB} raises both the hot and cold threshold, while lowering R_{TB} lowers both thresholds.

Since AVL is active whenever a valid power is provided at CHGIN or BATT, thermistor bias current flows at all times, even when charging is disabled. When using a 10kΩ thermistor and a 10kΩ pullup to AVL, this results in an additional 90µA load. This load can be reduced to 9µA by instead using a 100kΩ thermistor and 100kΩ pullup resistor.

Table 2. Trip Temperatures for Different Thermistors

THERMISTOR					TRIP TEMPERATURES			
R_{25} (Ω)	β	R_{TB} (Ω)	R_{15} (Ω)	R_{45} (Ω)	T_{COLD} (˚C)	T_{COOL} (˚C)	T_{WARM} (˚C)	T_{HOT} (˚C)
10000	3380	10000	14826	4900	-0.8	14.7	42.6	61.4
10000	3940	10000	15826	4354	2.6	16.1	40.0	55.7
47000	4050	47000	75342	19993	3.2	16.4	39.6	54.8
100000	4250	100000	164083	40781	4.1	16.8	38.8	53.2

Autonomous Charging

The MAX77962 supports autonomous charging without I^2C. In applications without I^2C-serial communication, use the following pins to configure the IC charger:

INLIM, ITO, ISET, VSET, OTGEN, DISQBAT, and STBY.

INLIM, ITO, ISET, and VSET pins are used to program the charger's input current limit, top-off current, constant-charging current, and termination voltage.

Connect a valid resistor from each of these pins to ground to program the charger. See the *Pin Descriptions* of each pin for details.

Connect all four pins (INLIM, ITO, ISET, VSET) to PVL to use the default values for the associated charger registers.

For autonomous charging, it is considered an abnormal condition if some of these pins (INLIM, ITO, ISET, VSET) connect to a valid resistor but others do not (for example, open or connects to PVL or connects to a resistor that is out of range). When this happens, the MAX77962 allows the DC-DC to switch and regulate the SYS voltage, but disables charging for safety reasons. The STAT pin reports no charge.

Table 3. INLIM, ITO, ISET, and VSET Pin Connections for Autonomous Charging

INLIM PIN	ITO PIN	ISET PIN	VSET PIN	AUTONOMOUS CHARGING
Valid resistor	Valid resistor	Valid resistor	Valid resistor	Normal, charger configuration is programmed by resistors
Tied to PVL	Tied to PVL	Tied to PVL	Tied to PVL	Normal, charger configuration uses default values
All other connections				Abnormal, no charging

Charger Input Current Limit Setting Input (INLIM)

When a valid charge source is applied to CHGIN, the IC limits the current drawn from the charge source to the value programmed with INLIM pin.

The default charger input current limit is programmed with the resistance from INLIM to GND. See Table 4.

If I^2C is used in the application, the CHGIN input current limit can also be reprogrammed with CHGIN_ILIM[6:0] register bits after the device powers up. Connect the INLIM pin to PVL to use I^2C default settings.

Table 4. INLIM Program Options Lookup Table

R_{INLIM} (Ω)	CHGIN INPUT CURRENT LIMIT (mA) DEFAULT VALUE OF CHGIN_ILIM[6:0]
Tied to PVL	500
226000	100
178000	200
140000	300
110000	400
86600	500
69800	1000
54900	1500
39200	2000
22600	2500
17800	3000

Fast-Charge Current Setting Input (ISET)

When a valid input source is present, the battery charger attempts to charge the battery with a fast-charge current programmed with the ISET pin.

The default fast-charge current is programmed with the resistance from ISET to GND. See Table 5.

If I^2C is used in the application, the fast-charge current can also be reprogrammed with CHGCC_MSB and CHGCC[7:0] register bits after the device powers up. Connect the ISET pin to PVL to use I^2C default settings.

Table 5. ISET Program Options Lookup Table

R_{ISET} (Ω)	FAST-CHARGE CURRENT SELECTION (mA) DEFAULT VALUE OF CHGCC[8:0]
Tied to PVL	450
226000	100
178000	200
140000	300
110000	400
86600	500
69800	1000
54900	1500
39200	2000
22600	2500
17800	3000

Top-Off Current Setting Input (ITO)

When the battery charger is in the top-off state, the top-off charge current is programmed by ITO pin.

The default top-off charge current is programmed with the resistance from ITO to GND. See Table 6.

If I^2C is used in the application, the top-off current can also be reprogrammed with TO_ITH[2:0] register bits after the device powers up. Connect ITO pin to PVL to use I^2C default settings.

Table 6. ITO Program Options Lookup Table

R_{ITO} (Ω)	TOP-OFF CURRENT THRESHOLD (mA) DEFAULT VALUE OF TO_ITH[2:0]
Tied to PVL	25
226000	25
178000	50
140000	75
110000	100
86600	125
69800	150

Charge Termination Voltage Setting Input (VSET)

The default charge termination voltage is programmed with the resistance from VSET to GND. See Table 7.

If I^2C is used in the application, the charge termination voltage can also be reprogrammed with CHG_CV_PRM[6:0] register bits after the device powers up. Connect the VSET pin to PVL to use I^2C default settings.

Table 7. VSET Program Options Lookup Table

R_{VSET} (Ω)	CHARGE TERMINATION VOLTAGE SETTING (V) DEFAULT VALUE OF CHG_CV_PRM[6:0]
Tied to PVL	8.10
226000	8.10
178000	8.16
140000	8.22
110000	8.28
86600	8.34
69800	8.40
54900	8.46
39200	8.52
22600	8.58
17800	8.64
14000	8.70
11000	8.76
8660	8.82
6980	8.86
5490	8.86

Switch Mode Charger

The IC features a switch mode buck-boost charger for a two-cell lithium ion (Li+) or lithium polymer (Li-polymer) battery. The charger operates with a wide input range from 3.5V to 23V, which is ideal for USB-C charging applications. The charger input current limit is programmable from 50mA to 3.15A, which is flexible to operate from either an AC-to-DC wall charger or a USB-C adapter.

The IC offers a high level of integration and does not require any external MOSFETs to operate, which significantly reduces the solution size. It operates with a switching frequency of 600kHz or 1.2MHz, which is ideal for portable devices that benefit from small solution size and high-efficiency. The battery charging current is programmable from 50mA to 3.2A, which accommodates small or large capacity batteries.

When the input source is not available, the IC can be enabled in a reverse-buck mode, delivering energy from the battery to the input, CHGIN, commonly known as USB On-the-Go (OTG). In OTG mode, the regulated CHGIN voltage is 5.1V with programmable current limit up to 1.5A.

Maxim's Smart Power Selector architecture makes the best use of the limited adapter power and the battery power to power the system. Adapter power that is not used for the system charges the battery. When system load exceeds the input limit, the battery provides additional current to the system up to the BAT to SYS overcurrent threshold, programmable with B2SOVRC[3:0] I^2C register bits. All power switches for charging and switching the system load between battery and adapter power are integrated on chip—no external MOSFETs required.

Maxim's proprietary process technology allows for low-R_{DSON} devices in a small solution size. The resistance between BAT to SYS is 10mΩ (typ), allowing low power dissipation and long battery life.

A multitude of safety features ensure reliable charging. Features include charge timers, watchdog, junction thermal regulation, and over-/under- voltage protection.

Smart Power Selector (SPS)

The SPS architecture includes a network of internal switches and control loops that efficiently distributes energy between an external power source (CHGIN), the battery (BAT) and the system (SYS). This architecture allows power-path operation with system instant on with a dead battery.

The Simplified Block Diagram shows the Smart Power Selector switches and gives them the following names: Q_1, Q_2, Q_3, Q_4 and Q_{BAT}.

Power Switches and Current Sense Resistor Descriptions

- CHGIN Current Sense Resistor: As shown in the Simplified Block Diagram, the CHGIN current is monitored with the input current sensing resistor, R_{S1}, connected between CSINP and CSINN pins.
- DC-DC Switches: Q_1, Q_2, Q_3, and Q_4 are the DC-DC switches which can operate as a buck (step-down) or a boost (step-up) depends on the external power source and battery voltage conditions.
- Battery-to-System Switch: Q_{BAT} is used to control battery charging and discharging operations.

I^2C Configuration Register Bits

- MODE[3:0] configures the Smart Power Selector mode to be charging, OTG, or DC-DC mode respectively. See the MODE[3:0] register bit description in the *Register Map* for details.
- VCHGIN_REG[4:0] sets the CHGIN regulation voltage, when the IC operates in forward mode (CHGIN has a valid power source). See the *CHGIN Regulation Voltage* section for details.
- MINVSYS[2:0] sets the minimum system regulation voltage. See the *SYS Regulation Voltage* section for details.
- B2SOVRC[3:0] sets the battery to system discharge over-current alert threshold.

Energy Distribution Priority

- With a valid external power source at CHGIN:
  - The external power source is the primary source of energy.
  - The battery is the secondary source of energy.
  - Energy delivery to SYS has the highest priority.
  - Any remaining energy from the power source that is not required by the system is available to the battery charger.
- With no valid external power source at CHGIN:

- The battery is the primary source of energy.
- When OTG mode is enabled, energy delivery to SYS has the highest priority.
- Any remaining energy from the battery that is not required by the system is available to power the CHGIN.

CHGIN Regulation Voltage

- In forward mode (when CHGIN is powered from a valid external source), CHGIN voltage is regulated to VCHGIN_REG[4:0] when a high impedance or current limited source is applied. VCHGIN might experience significant voltage droop from the high impedance source when the IC extracts high power from the source. Regulating VCHGIN allows the IC to extract the most power from the power source. See the *Adaptive Input Current Limit (AICL) and Input Voltage Regulation* section for more details.
- In reverse mode (OTG), CHGIN voltage is regulated to 5.1V with programmable current limit up to 1.5A (OTG_ILIM[2:0]).

SYS Regulation Voltage

With a valid external power source at CHGIN:

- When the DC-DC is disabled (MODE[3:0] = 0x00 or STBY_EN = 0b1 or STBY pin = high), the Q_{BAT} switch is fully on and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$.
- When the DC-DC is enabled and the charger is disabled (MODE[3:0] = 0x04), V_{SYS} is regulated to $V_{BATTREG}$ (CHG_CV_PRM) and Q_{BAT} is off.
- When the DC-DC is enabled and the charger is enabled (MODE[3:0] = 0x05), but in a noncharging state such as Done, Thermistor Suspend, Watchdog Suspend, or Timer Fault, V_{SYS} is regulated to $V_{BATTREG}$ (CHG_CV_PRM) and Q_{BAT} is off.
- When the DC-DC is enabled and the charger is enabled (MODE[3:0] = 0x05) and in a valid charging state such as Precharge or Trickle Charge ($V_{BATT} < V_{SYSMIN}$ - 500mV), V_{SYS} is regulated to $V_{BATTREG}$ (CHG_CV_PRM). The charger operates as a linear regulator, and the power dissipation can be calculated with $P = (V_{BATTREG} - V_{BATT}) \times I_{BATT}$.
- When the DC-DC is enabled and the charger is enabled (MODE[3:0] = 0x05) and in a valid charging state such as Fast Charge (CC or CV) or Top-Off ($V_{BATT} > V_{SYSMIN}$ - 500mV), the Q_{BAT} switch is fully on, and $V_{SYS} = V_{BATT} + I_{BATT} \times R_{BAT2SYS}$.
- In all the modes described above, when the power demand on SYS exceeds the input source power limit, the battery automatically provides supplemental power to the system. If the Q_{BAT} switch is initially off when V_{SYS} drops to $V_{BATT} - V_{BSREG}$, the Q_{BAT} switch turns on and V_{SYS} is regulated to $V_{BATT} - V_{BSREG}$.

Without a valid external power source at CHGIN, including with OTG mode (MODE[3:0] = 0x0A):

- The Q_{BAT} switch is fully on and $V_{SYS} = V_{BATT} - I_{BATT} \times R_{BAT2SYS}$.

Power States

The IC transitions between power states as input/battery and load conditions dictate.

The IC provides four (4) power states and one (1) no power state. Under power limited conditions, the power-path feature maintains SYS and USB-OTG loads at the expense of the battery charge current. In addition, the battery supplements the input power when required. See the *Smart Power Selector (SPS)* section for more details. As shown, transitions between power states are initiated by detection/removal of valid power sources, OTG events, and under-voltage conditions.

1. NO INPUT POWER, *MODE[3:0] = undefined*: No input adapter or battery is detected. The charger and system are off. Battery is disconnected.

2. BATTERY-ONLY, *MODE[3:0] = any mode*: CHGIN is invalid or outside the input voltage operating range. Battery is connected to power the SYS load (Q_{BAT} = on).

3. NO CHARGE—DC-DC in FORWARD mode, *MODE[3:0] = 0x04*: CHGIN input is valid, DC-DC supplies power to SYS. DC-DC operates from a valid input. Battery is disconnected (Q_{BAT} = OFF) when SYS load is less than the power that DC-DC can supply.

4. CHARGE—DC-DC in FORWARD mode, *MODE[3:0] = 0x05*: CHGIN input is valid, DC-DC supplies power to SYS and charges the battery with I_{BATT}. DC-DC operates from a valid input.

5. OTG—DC-DC in REVERSE mode (OTG), *MODE[3:0] = 0x0A*: OTG is active. Battery is connected to support SYS and OTG loads (Q_{BAT} = on), and charger operates in REVERSE buck mode.

Powering Up with Charger Disabled by Default

The MAX77962's default power state is CHARGE - DC-DC in FORWARD mode, MODE[3:0] = 0x05. For battery authentication/safety purposes, the MAX77962 can be configured to keep charging disabled, while allowing the DC-DC to switch and regulate the SYS voltage, when power is applied to CHGIN. To implement this and enable the charger when appropriate:

- Connect at least one of the INLIM, ITO, ISET or VSET pins to a valid resistor while tying the others (at least one) to PVL. CHG_DTLS = 0x05 and CHG_OK = 0.
- The system processor can configure the charger using the I^2C interface.
- The system processor enables charging by setting COMM_MODE to 1 (default is 0).

See the *Wide-Input I^2C Programmable Charger with Charger Disabled* diagram for a pin connection example. INLIM is connected to a valid resistor while ITO, ISET, and VSET tie to PVL. The default input current limit is programmed by R_{INLIM}, while the default top-off current, constant charging current, and termination voltage use their default value. The system processor can re-program all four settings using the I^2C interface if needed.

Input Validation

The charger input is compared with several voltage thresholds to determine if it is valid. A charger input must meet the following characteristics to be valid:

- CHGIN must be above V_{CHGIN_UVLO} to be valid. Once CHGIN is above UVLO threshold, the information is latched and can only be reset when charger is in adaptive input current loop (AICL) and input current is lower than IULO threshold of 30mA.
- CHGIN must be below its overvoltage-lockout threshold (V_{CHGIN_OVLO}).

The device generates a CHGIN_I interrupt (maskable with CHGIN_M bit) when CHGIN status changes. Read the CHGIN input status with CHGIN_OK and CHGIN_DTLS[1:0] register bits.

Adaptive Input Current Limit (AICL) and Input Voltage Regulation (CHGIN_REG)

The IC features input power management to extract maximum input power while avoiding input source overload. The AICL and CHGIN_REG features allow the charger to extract more energy from relatively high resistance charge sources with long cables, non-compliant USB hubs, or current limited adapters. In addition, the input power management allows the IC to perform well with adapters that have poor transient load responses.

With a high resistance source, the charger input voltage drops substantially when it draws large current from the source. The charger's input voltage regulation loop automatically reduces the current drawn from the input in order to regulate the input voltage at V_{CHGIN_REG}. If the input current is reduced to $I_{CHGIN\_REG\_OFF}$ (50mA typ) and the input voltage is still below V_{CHGIN_REG}, the charger input turns off. V_{CHGIN_REG} is programmable with VCHGIN_REG[4:0] register bits.

With a current limited source, if the ICs input current limit is programmed above the current limit of the adapter, the charger input voltage starts to drop when the input current drawn exceeds the source current limit. The charger's input voltage regulation loop allows the IC to reduce its input current and operate at the current limit of the adapter.

When operating with the input voltage regulation loop active, an AICL_I interrupt is generated, AICL_OK sets to 0. The device prioritizes system energy delivery over battery charging. See the *Smart Power Selector (SPS)* section for more details.

To extract the most input power from a current limited charge source, monitor the AICL_OK status while decreasing the CHGIN_ILIM[6:0] register setting. Lowering the CHGIN_ILIM[6:0] to a value below the current limit of the adapter causes the input voltage to rise. Although the CHGIN_ILIM[6:0] is lowered, more power can be extracted from the adapter when the input voltage rises.

Input Self-Discharge

To ensure that a rapid removal and reinsertion of a charge source always results in a charger input interrupt, the charger input presents loading to the input capacitor to ensure that when the charge source is removed, the input voltage decays below the UVLO threshold in a reasonable time (t_{INSD}). The input self-discharge is implemented with a 44kΩ resistor (R_{INSD}) from CHGIN input to ground.

System Self-Discharge with No Power

To ensure a timely, complete, repeatable, and reliable reset behavior when the system has no power, the IC actively discharges the BATT and SYS nodes when the adapter is missing, the battery is removed, and V_{SYS} is less than $V_{SYSUVLO}$. The BATT and SYS discharge resistors are both 600Ω.

Charger States

The IC utilizes several charging states to safely and quickly charge batteries as shown in Figure 1 and Figure 2. Figure 1 shows an exaggerated view of a Li+/Li-Poly battery progressing through the following charge states when there is no system load and the die and battery are close to room temperature: Prequalification → Fast-charge → Top-off → Done.

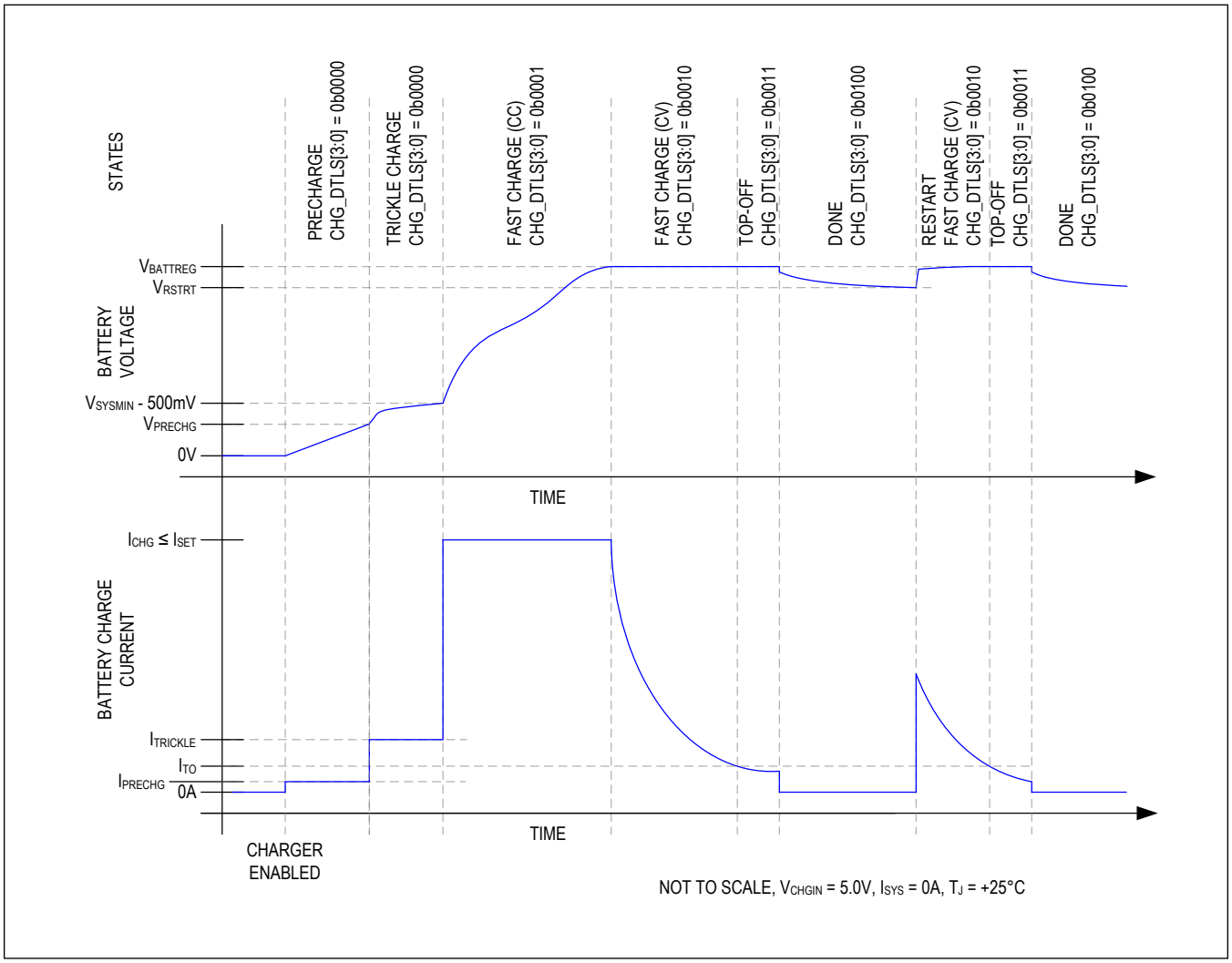


Figure 1. Li Battery Charge Profile

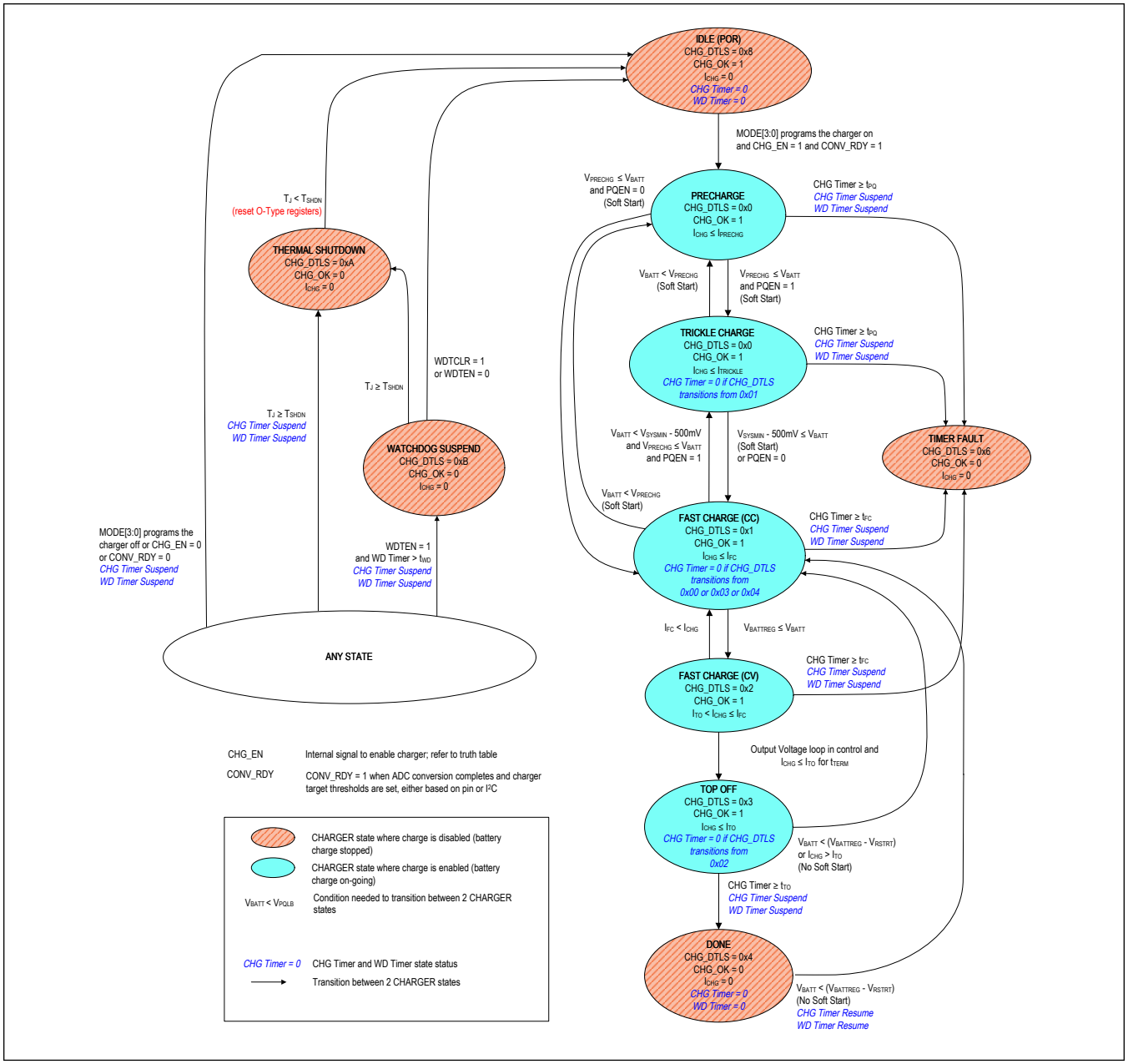


Figure 2. Charger State Diagram

No Input Power or Charger-Disabled Idle State

From any state shown in Figure 2, except thermal shutdown, the “no input power or charger disabled” state is entered whenever the charger is programmed to be off or the charger input CHGIN is invalid. After being in this state for t_{SCIDG}, CHG_DTLS is set to 0x08 and CHG_OK is set to 1. A CHG_I interrupt is generated if CHG_OK was 0 previously.

While in the “no input power or charger disabled” state, the charger current is 0mA, the watchdog and charge timers are forced to 0, and the power to the system is provided by either the battery or the adapter. When both battery and adapter power are available, the adapter provides primary power to the system and the battery contributes supplemental energy to the system if necessary.

To exit the “no input power or charger disabled” state, the charger input must be valid and the charger has to be enabled.

Precharge State

As shown in Figure 2, the charger enters the precharge state when the battery voltage is less than V_{PRECHG}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS is set to 0x00. In the precharge state, charge current into the battery is I_{PRECHG}.

The following events cause the state machine to exit this state:

- Battery voltage rises above V_{PRECHG} and the charger enters the next state in the charging cycle: “Trickle Charge”.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note that the precharge state works with battery voltages down to 0V. The 0V operation typically allows this battery charger to recover batteries that have an “open” internal pack protector. Typically a battery pack's internal protection circuit opens if the battery has seen an overcurrent, undervoltage, or overvoltage. When a battery with an “open” internal pack protector is used with this charger, the precharge mode current flows into the 0V battery—this current raises the pack’s terminal voltage to the level where the internal pack protection switch closes.

Note that a normal battery typically stays in the precharge state for several minutes or less. Therefore a battery that stays in the precharge for longer than t_{PQ} may be experiencing a problem.

Trickle Charge State

As shown in Figure 2, the charger state machine is in trickle charge state when $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$ - 500mV. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x00.

With PQEN = 1(default) and the IC is in its trickle charge state, the current in the battery is less than or equal to ITRICKLE. When PQEN = 0, the charger skips the trickle charge state and transitions directly to the fast-charge state, and the battery charging current is less than or equal to I_{FC}.

Charge current may be less than ITRICKLE/I_{FC} for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

Typical systems operate with PQEN = 1. When operating with PQEN = 0, the system’s software usually sets I_{FC} to a low value such as 200mA and then monitors the battery voltage. When the battery exceeds a relatively low voltage such as 6V, then the system’s software usually increases I_{FC}.

The following events cause the state machine to exit this state:

- When the battery voltage rises above V_{SYSMIN} - 500mV or the PQEN bit is cleared, the charger enters the next state in the charging cycle: “Fast-Charge (CC)”.
- If the battery charger remains in this state for longer than t_{PQ}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

Note that a normal battery typically stays in the trickle charge state for several minutes or less. Therefore a battery that stays in trickle charge for longer than t_{PQ} may be experiencing a problem.

Fast-Charge Constant Current (CC) State

As shown in Figure 2, the charger enters the fast-charge constant current (CC) state when V_{SYSMIN} - 500mV (typ) < V_{BATT} < $V_{BATTREG}$. After being in the fast-charge CC state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x01.

In the fast-charge CC state, the battery charging current is less than or equal to I_{FC}. Charge current may be less than I_{FC} for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charging current.

The following events cause the state machine to exit this state:

- When the battery voltage rises above $V_{BATTREG}$, the charger enters the next state in the charging cycle: “Fast-Charge (CV)”.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the “Timer Fault” state.
- If the watchdog timer is not serviced, the charger state machine transitions to the “Watchdog Suspend” state.

The battery charger dissipates the most power in the fast-charge constant current state, which causes the die temperature to rise. If the die temperature exceeds T_{REG}, the thermal foldback loop is engaged and I_{FC} is reduced. See the *Thermal Foldback* section for more information.

Fast-Charge Constant Voltage (CV) State

As shown in Figure 2, the charger enters the fast-charge constant voltage (CV) state when the battery voltage rises to $V_{BATTREG}$ from the fast-charge CC state. After being in the fast-charge CV state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x02.

In the fast-charge CV state, the battery charger maintains $V_{BATTREG}$ across the battery and the charge current is less than or equal to I_{FC}. As shown in Figure 1, charger current decreases exponentially in this state as the battery becomes fully charged.

The Smart Power Selector control circuitry may reduce the charge current for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- When the charger current is below I_{TO} for t_{TERM}, the charger enters the *Top-Off state*.
- If the battery charger remains in this state for longer than t_{FC}, the charger state machine transitions to the *Timer Fault state*.
- If the watchdog timer is not serviced, the charger state machine transitions to the *Watchdog Timer Suspend state*.

Top-Off State

As shown in Figure 2, the top-off state can only be entered from the fast-charge CV state when the charger current decreases below I_{TO} for t_{TERM}. After being in the top-off state for t_{SCIDG}, a CHG_I interrupt is generated if CHG_OK was 0 previously, CHG_OK is set to 1, and CHG_DTLS = 0x03. In the top-off state the battery charger maintains $V_{BATTREG}$ across the battery and typically the charge current is less than or equal to I_{TO}.

The Smart Power Selector control circuitry may reduce the charge current for any of the following reasons:

- The charger input is in input current limit.
- The charger input voltage is low.
- The charger is in thermal foldback.
- The system load is consuming adapter current. Note that the system load always gets priority over the battery charge current.

The following events cause the state machine to exit this state:

- After being in this state for the top-off time (t_{TO}), the charger enters the *Done state*.
- If $V_{BATT} < V_{BATTREG} - V_{RSTRT}$, the charger goes back to the *Fast-Charge (CC) state*.
- If the watchdog timer is not serviced, the charger state machine transitions to the *Watchdog Timer Suspend state*.

Done State

As shown in Figure 2, the battery charger enters its done state after the charger has been in the top-off state for t_{TO}. After being in this state for t_{SCIDG}, a CHG_I interrupt is generated only if CHG_OK was 0 previously, CHG_OK is set to 0, and CHG_DTLS = 0x04.

The following events cause the state machine to exit this state:

- If $V_{BATT} < V_{BATTREG} - V_{RSTRT}$, the charger goes back to the *Fast-Charge Constant Current state*.
- If the watchdog timer is not serviced, the charger state machine transitions to the *Watchdog Timer Suspend state*.

In the done state, the battery charging current (I_{CHG}) is 0A and the charger presents a very low load (I_{MBDN}) to the battery. If the system load presented to the battery is low (<<100µA), then a typical system can remain in the done state for many days. If left in the done state long enough, the battery voltage decays below the charging restart threshold (V_{RSTRT}) and the charger state machine transitions back into the fast-charge CC state. There is no soft-start (di/dt limiting) during the done to fast-charge state transition.

Timer Fault State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 2, the charge timer prevents the battery from charging indefinitely. The time that the charger is allowed to remain in its prequalification states is t_{PQ}. The time that the charger is allowed to remain in the fast-charge CC and CV states is t_{FC} which is programmable with FCHGTIME. Finally, the time that the charger is in the top-off state is t_{TO} which is programmable with TO_TIME. Upon entering the timer fault state, a CHG_I interrupt is generated without a delay, CHG_OK is cleared, and CHG_DTLS = 0x06.

The charger is off in the timer fault state. The charger can exit the timer fault state when the charger is programmed to be off then on again through the MODE bits or when DISQBAT pin is toggled from L-H-L. Alternatively, the charger input can be removed and re-inserted to exit the timer fault state (see the “ANY STATE” bubble in Figure 2).

Watchdog Timer Suspend State

The battery charger provides both a charge timer and a watchdog timer to ensure safe charging. As shown in Figure 2, the watchdog timer protects the battery from charging indefinitely in the event that the host hangs or otherwise cannot communicate correctly. The watchdog timer is disabled by default with WDTEN = 0. Enable the feature by setting WDTEN = 1. With watchdog timer enabled, the host controller must reset the watchdog timer within the timer period (t_{WD}) in order for the charger to operate properly. Reset the watchdog timer by programming WDTCLR = 0x01.

If the watchdog timer expires, charging stops, a CHG_I interrupt is generated if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS indicates that the charger is off because the watchdog timer expired. Once the watchdog timer expires, the charger may be restarted by programming WDTCLR = 0x01. The SYS node can be supported by the battery and/or the adapter through the DC-DC buck while the watchdog timer is expired.

Thermal Shutdown State

As shown in Figure 2, the state machine enters the thermal shutdown state when the junction temperature (T_J) exceeds the device's thermal-shutdown threshold (T_{SHDN}). When T_J is close to $T_{SHDN,}$ the charger would have already folded back the input current to 0A (see the *Thermal Foldback* section for more details), so the charger and the DC-DC are effectively off. Upon entering this state, CHG_I interrupt is generated if CHG_OK was 1 previously, CHG_OK is cleared, and CHG_DTLS = 0x0A.

In the thermal shutdown state, the charger is off. MODE register (CHG_CNFG_00[3:0]) is reset to its default value as well as all O-type registers.

Thermal Management

The IC charger uses several thermal management techniques to prevent excessive battery and die temperatures.

Thermal Foldback

Thermal foldback maximizes the battery charge current while regulating the IC junction temperature. As shown in Figure 3, when the die temperature exceeds the value programmed by REGTEMP (T_{REG}), a thermal limiting circuit reduces the battery charger's target current by 5%/°C (A_{TJREG}) with an analog control loop. When the charger transitions in and out of the thermal foldback loop, a CHG_I interrupt is generated and the host microprocessor can read the status of the thermal regulation loop with the TREG status bit. Note that an active thermal foldback loop is not an abnormal operation and the thermal foldback loop status does not affect the CHG_OK bit (only information contained within CHG_DTLS affects CHG_OK).

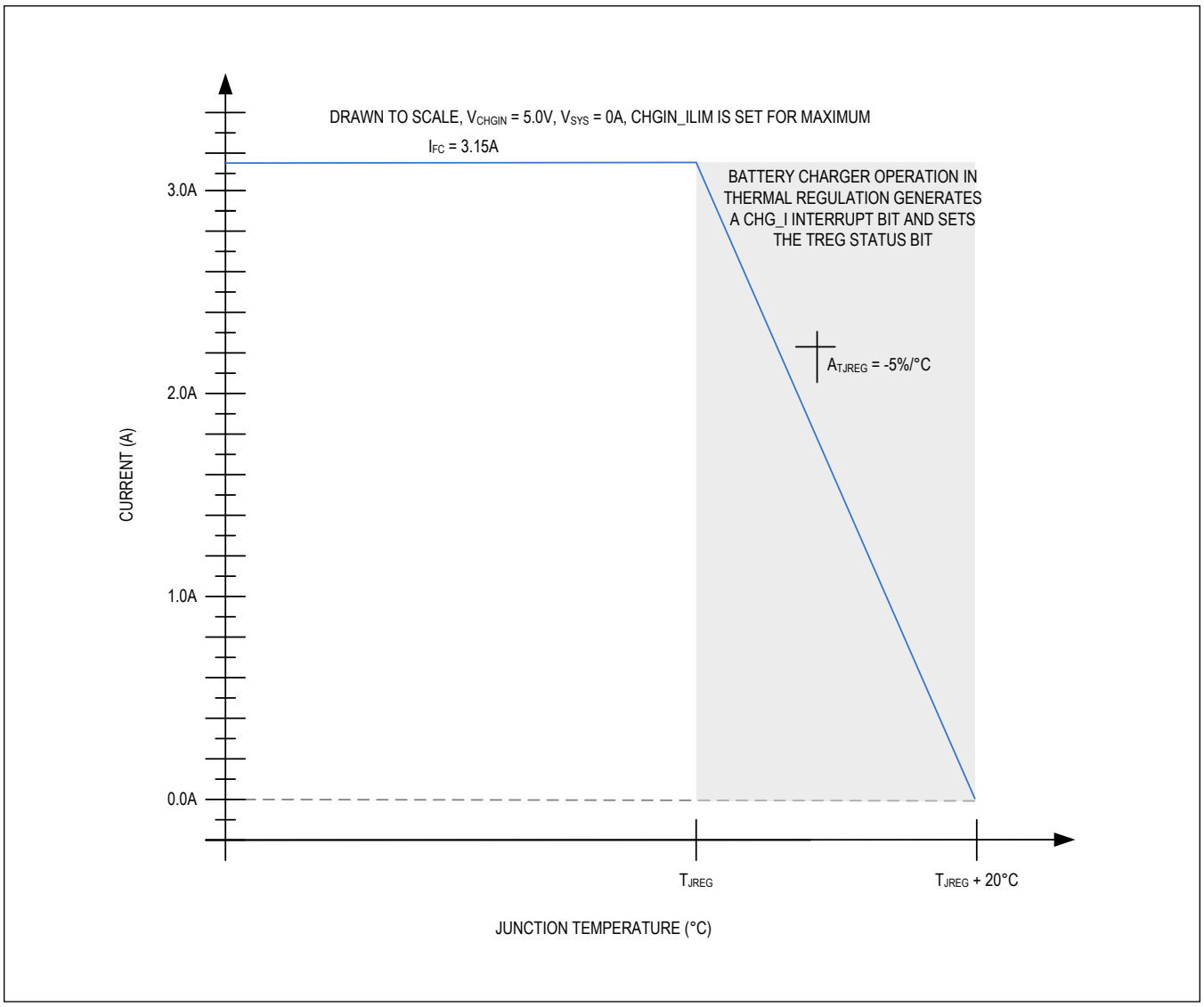


Figure 3. Charge Currents vs. Junction Temperature

JEITA Compliance

The IC safely charges Li+ batteries in accordance with JEITA specifications. The IC monitors the battery temperature with a NTC thermistor connected at the THM pin and automatically adjusts the fast-charge current and/or charge termination voltage as the battery temperature varies. JEITA controlled charging can be disabled by setting JEITA_EN to 0. CHG_DTLS and THM_DTLS registers report JEITA controlled charging status.

The JEITA controlled fast-charging current (I_{CHGCC_JEITA}) and charge termination voltage (V_{CHGCV_JEITA}) for $T_{COLD} < T < T_{COOL}$ are programmable with I^2C bits I_{CHGCC_COOL} and V_{CHGCV_COOL}.

The charge termination voltage for $T_{WARM} < T < T_{HOT}$ is reduced to (CHG_CV_PRM - 180mV/cell), as shown in Figure 4.

Charging is suspended when the battery temperature is too cold or too hot ($T < T_{COLD}$ or $T_{HOT} < T$).

Temperature thresholds T_{COLD}, T_{COOL}, T_{WARM}, and T_{HOT} depend on the thermistor selection. See the *Thermistor Input* section for more details.

When battery charge current is reduced by 50%, the charger timer is doubled.

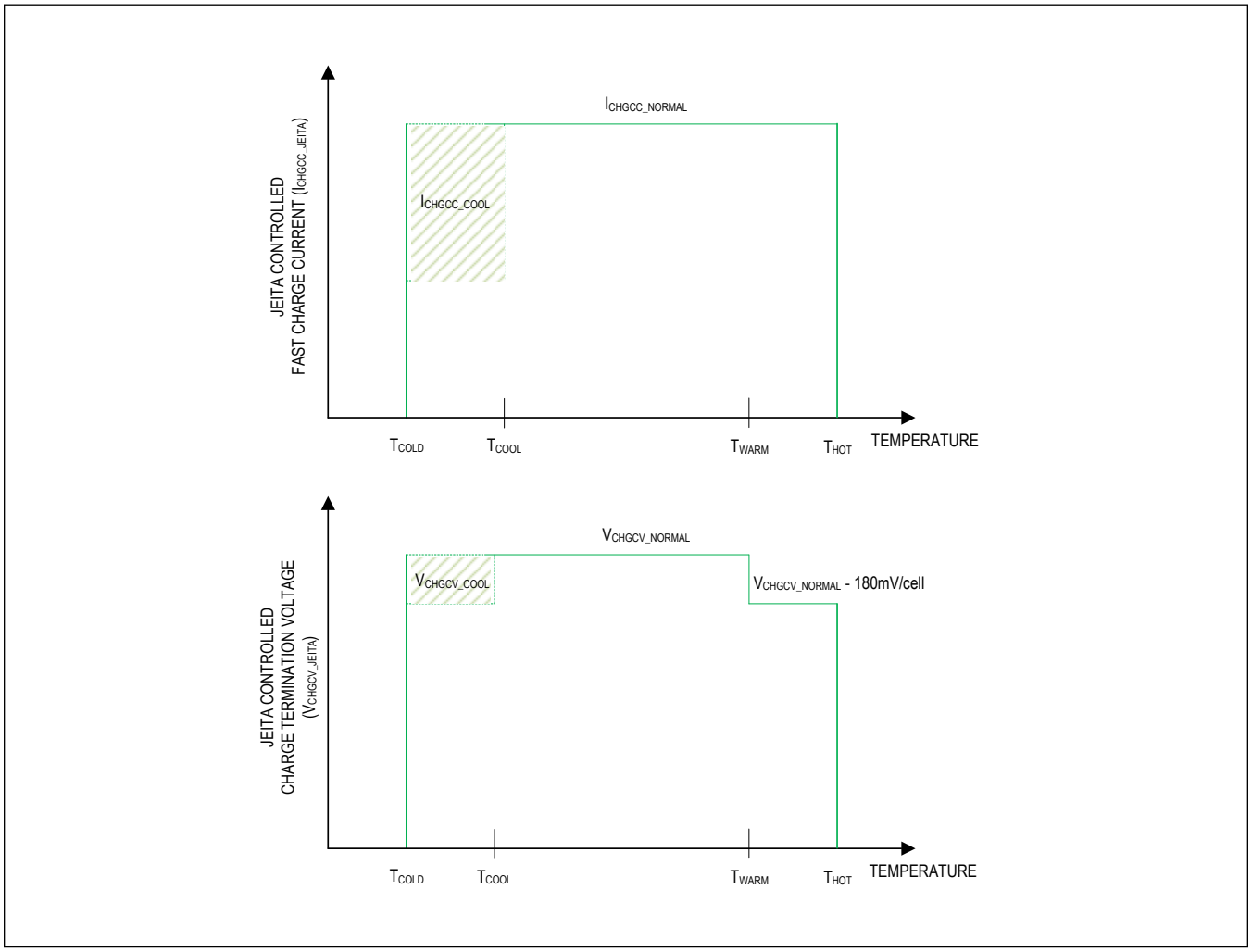


Figure 4. JEITA Compliance

Thermal Shutdown

The IC has a die temperature sensing circuit. When the die temperature exceeds the thermal-shutdown threshold, T_{SHDN}, the IC shuts down and resets O-type I^2C registers. There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown bus deasserts and the device re-enables. The battery charger has an independent thermal regulation loop, see the *Thermal Foldback* section for more details.

Automatic Charger Loop Offset

The IC has four independent analog loops, including input voltage (AICL), input current, output voltage, and output current. The IC automatically switches between different loops and only one loop is in control at any time. Due to offset between different loops, the charger might hop between two loops at the boundary condition. For example, if the IC is in the fast-charge state and V_{BATT} is close to CHG_CV_PRM, and I_{BATT} is close to CHGCC, the charger is at the boundary of fast-charge CC state (output current loop) and fast-charge CV state (output voltage loop). The charger might hop between output current loop and output voltage loop continuously.

To prevent possible loop hopping behavior, an automatic charger loop offset is implemented. Automatic offset of the output voltage loop (CHGR_CV_OFFSET[1:0]) and automatic offset of the output current loop (CHGCC_OFFSET[1:0]) provide programmable hysteresis for entering these loops. The offset is applied when the charger is not in the corresponding loop and is automatically removed if the charger transitions to the corresponding loop. For example, if CHGR_CV_OFFSET[1:0] is set to 0x1 (+24mV), the fast-charge CC to CV transition occurs at V_{BATT} equal to (CHG_CV_PRM + 24mV), and V_{BATT} regulation target in the fast-charge CV state remains at CHG_CV_PRM. This creates extra hysteresis and maintains accurate regulation of each loop.

Adding automatic offset to a loop can prevent possible hopping with all other three loops. It is recommended that the user set:

- CHGCC_OFFSET[1:0] to 0x01 for +62.5mA
- CHGR_CV_OFFSET[1:0] to 0x01 for +24mV

Offsets for the input current loop and input voltage (AICL) loop are set in OTP. The input current loop offset OTP_INLIM_OFFSET[1:0] is 0x0 (0mA/disabled), and the input voltage (AICL) loop offset OTP_BYPV_OFFSET[1:0] is set to 0x1 (-1 LSB). (The LSB is 175mV at VCHGIN_REG = 4.025V—4.900V, 525mV at VCHGIN_REG = 5.425V—10.950V, or 600mV at VCHGIN_REG = 11.550V—19.050V).

Setting the automatic offset to 0x0 effectively disables this feature.

Factory Ship Mode

The IC supports factory ship mode with low battery quiescent current, I_{SHDN}.

When the input source is not valid, and the device is powered by battery, the device enters factory ship mode if STBY pin is pulled high or FSHIP_MODE bit is set to 1. I^2C communication is unavailable in the factory ship mode. When a valid input source is applied to the device's CHGIN pin or DISQBAT pin is pulled high, the device exits factory ship mode. I^2C communication is enabled.

Minimum System Voltage

The system voltage is regulated to the minimum SYS voltage (V_{SYSMIN}) when the battery is low ($V_{BATT} < V_{SYSMIN}$ - 500mV).

- The charging current is I_{PRECHG} when $V_{BATT} < V_{PRECHG}$.
- The charging current is $I_{TRICKLE}$ when $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$ - 500mV.
- The charging current is I_{FC} when V_{SYSMIN} - 500mV < V_{BATT}.

Battery Differential Voltage Sense (BATSP, BATSN)

BATSP and BATSN are differential remote voltage sense lines for the battery. The MAX77962's remote sensing feature improves voltage sense accuracy, maximizes charging time in Fast-Charge CC State and thus minimizes total charging time. The thermistor voltage is interpreted with respect to BATSN. For best results, connect BATSP and BATSN as close as possible to the battery connector.

Battery Overcurrent Alert

Excessive battery discharge current can occur for several reasons such as exposure to moisture, a software problem, an IC failure, a component failure, or a mechanical failure that causes a short circuit. The battery overcurrent alert feature is enabled with B2SOVRC[3:0]; disabling this feature reduces the battery current consumption by I_{BOVRC}.

When the battery (BATT) to system (SYS) discharge current (I_{BATT}) exceeds the programmed overcurrent threshold for at least t_{BOVRC}, the Q_{BAT} switch closes to reduce the power loss in the IC. A B2SOVRC_I and a BAT_I interrupt are generated, BAT_OK is cleared, and BAT_DTLS reports an overcurrent condition. Typically, when the host processor detects this overcurrent interrupt it executes a housekeeping routine that tries to mitigate the overcurrent situation. If the processor cannot correct the overcurrent within t_{OCP}, then the IC turns off the DC-DC.

t_{OCP} time duration can be set through the B2SOVRC_DTC register bit (battery to SYS overcurrent debounce time control): 0x0 (dflt): t_{OCP} = 6ms, 0x1: t_{OCP} = 100ms.

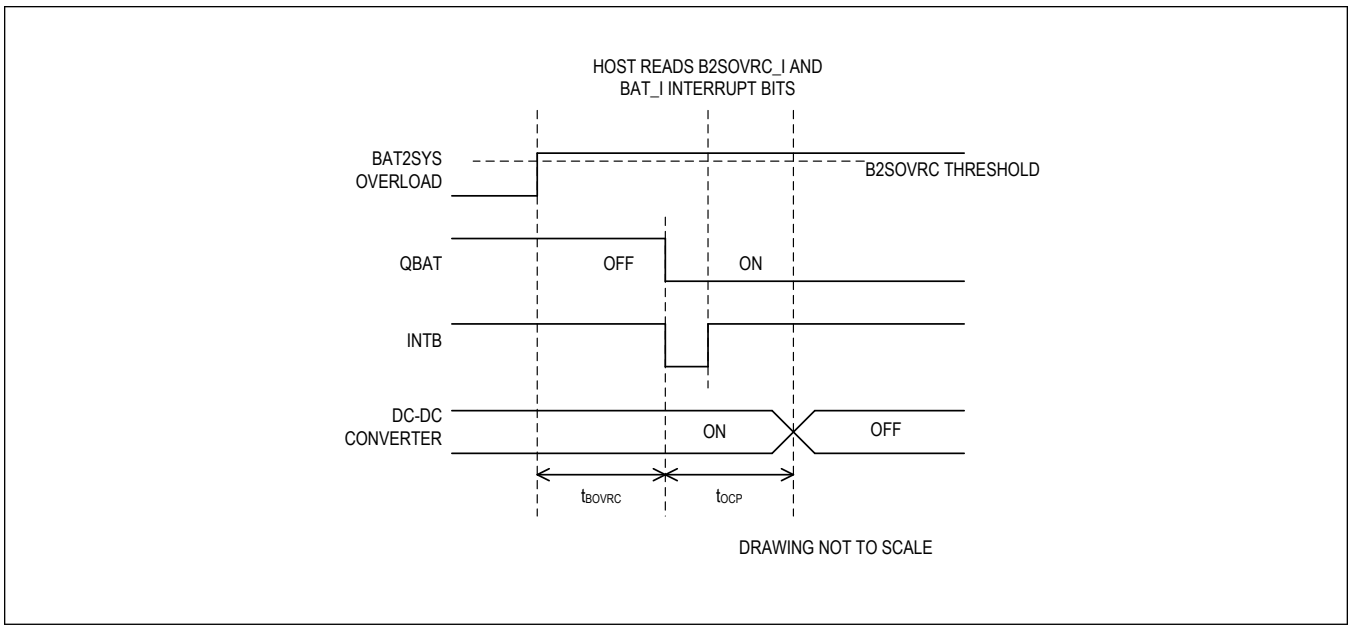


Figure 5. B2SOVRC

Charger Interrupt Debounce Time

Debounce times of charger interrupts are listed in Table 8.

Table 8. List of Charger Interrupt Debounce Times

INTERRUPT	DEBOUNCE TIME			
	RISING		FALLING	
	MIN	MAX	MIN	MAX
AICL_I	30ms	—	30ms	—
CHGIN _I	7ms	—	None	—
B2SOVRC_I	—	3.3ms	None	—
BAT_I (OV)	30ms	—	None	—
OTG_PLIM_I (OTG Fault)	37.5ms	—	None	—
OTG_PLIM_I (Buck-Boost Positive Current Limit)	450us	—	None	—

Input Power-OK/OTG Power-OK Output (INOKB)

INOKB is an open-drain and active-low output that indicates CHGIN power-ok status.

When OTG mode is disabled, (OTGEN = L and MODE[3:0] ≠ 0x0A), INOKB pulls low when a valid input source is inserted at CHGIN, $V_{CHGIN\_UVLO} < V_{CHGIN} < V_{CHGIN\_OVLO}$.

When OTG mode is enabled, (OTGEN = H or MODE[3:0] = 0x0A), INOKB pulls low to indicate the OTG output power-OK when $V_{CHGIN.OTG.UV} < V_{CHGIN} < V_{CHGIN.OTG.OV}$.

INOKB can be used as a logic output by adding a 200kΩ pullup resistor to a system IO voltage.

Charge Status Output (STAT)

STAT is an open-drain and active-low output that indicates charge status. STAT can be used as a logic input to the host processor by adding a 200kΩ pullup resistor to a system IO rail and a rectifier (a diode and a capacitor).

Table 9. Charge Status Indicator by STAT

CHARGE STATUS	STAT	LOGIC STATE
No input	High impedance	High
No DC-DC/no charge: Valid adapter with STBY_EN = 1 or MODE = 0x0/1/2/3/4	High impedance	High
Trickle, Precharge, Fast-Charge	Repeat low and high impedance with 1Hz, 50% duty cycle	High, rectified with an external diode and a capacitor
Top-Off and Done	Low	Low
Faults	High impedance	High

Reverse Buck Mode (OTG)

The DC-DC converter topology of the MAX77962 allows it to operate as a forward buck-boost converter or as a reverse buck converter. The modes of the DC-DC converter are controlled with MODE[3:0] register bits. When MODE[3:0] = 0x0A or OTGEN = H, the DC-DC converter operates in reverse buck mode, allowing it to source current to CHGIN, commonly referred to as USB On-the-Go (OTG) mode.

Note that reverse buck mode of the MAX77962 conflicts with skip mode operation. Before enabling OTG function, disable skip mode with DISKIP = 1. Once OTG function is disabled, skip mode is allowed to be enabled with DISKIP = 0.

In OTG mode, the DC-DC converter operates in reverse buck mode and regulates V_{CHGIN} to $V_{CHGIN.OTG}$ (5.1V, typ). The current through the CHGIN current sensing resistor (CSINN, CSINP) is limited to the value programmed by OTG_ILIM[2:0]. There are four OTG_ILIM options to program CHGIN current limit from 500mA to 1.5A. When the OTG mode is enabled, the unipolar CHGIN transfer function measures current going out of CHGIN. When OTG mode is disabled, the unipolar CHGIN transfer function measures current going into CHGIN.

OTG_I, OTG_M, and OTG_OK are the interrupt bit, interrupt mask bit, and interrupt status bit associated with OTG function. OTG_DTLS[1:0] reports the status of the OTG operation. OTG_DTLS[1:0] is latched until the host reads the register.

If the external OTG load at CHGIN exceeds $I_{CHGIN.OTG.ILIM}$ current limit for a minimum of 37.5ms, an OTG_I interrupt is generated, OTG_OK = 0, and OTG_DTLS[1:0] = 01. The reverse buck operates as a current limited voltage source when overloaded. The DC-DC converter stops switching when the OTG_ILIM condition lasts for 60ms and automatically resumes switching after 300ms OFF time. If the OTG_ILIM fault condition at CHGIN persists, the DC-DC toggles ON and OFF with ~60ms ON and ~300ms OFF.

When CHGIN voltage drops below $V_{CHGIN.OTG.UVLO}$, the DC-DC stops switching and an OTG_I interrupt is generated. OTG_OK = 0 and OTG_DTLS[1:0] = 00.

When CHGIN voltage exceeds $V_{CHGIN.OTG.OV}$, the DC-DC stops switching and an OTG_I interrupt is generated. OTG_OK = 0 and OTG_DTLS[1:0] = 10.

If the DC-DC stops switching due to a OTG_UV or OTG_OV fault condition, it automatically retries after 300ms OFF time.

INOKB is the hardware indication of the OTG power-OK. See the *Input Power-OK/OTG Power-OK Output (INOKB)* section for details.

OTG mode is not supported for configuration of 1.2MHz switching frequency.

OTG Enable (OTGEN)

The OTGEN is an active-high input. When the OTGEN pin is pulled high, the OTG function is enabled. When the OTGEN pin is pulled low, the OTG function can be enabled through the I^2C interface by setting MODE[3:0] = 0x0A. Before enabling the OTG function, disable skip mode with DISKIP = 1. To pull the OTGEN pin low with a pulldown resistor, the resistance must be lower than 44kΩ.

The device enables reverse buck operation only when the voltage on the CHGIN bypass cap, V_{CHGIN}, falls below V_{CHGIN_UVLO}.

In case V_{CHGIN} is above the V_{CHGIN_UVLO} threshold at OTG enable, the device ensures the V_{CHGIN} node discharges through an 8kΩ pulldown resistor before enabling OTG function and reverse buck switching.

The pulldown is released once V_{CHGIN_UVLO} is reached.

Analog Low-Noise Power Input (AVL)

AVL is the power input for the ICs analog circuitry. Do not power external devices from this pin. Bypass with a 4.7Ω resistor between AVL and PVL and a 4.7µF capacitor from AVL to GND.

Low-Side Gate Driver Power Supply (PVL)

PVL is an internal 1.8V LDO output, which powers the ICs low-side gate driver circuitry. Do not power external devices other than pullup resistors from this pin. Bypass with a 4.7µF capacitor to GND.

System Faults

V_{SYS} Fault

The IC monitors the V_{SYS} node for undervoltage and overvoltage events. The following describes the device's behavior if any of these events is to occur.

V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)

When the voltage from SYS to GND (V_{SYS}) is less than the undervoltage-lockout threshold ($V_{SYSUVLO}$), the IC generates a SYSUVLO_I interrupt immediately. If V_{SYS} is undervoltage for greater than 8ms, the device shuts down and resets O-type I^2C registers.

V_{SYS} Overvoltage Lockout ($V_{SYSOVLO}$)

When the V_{SYS} exceeds $V_{SYSOVLO}$, the IC generates a SYSOVLO_I interrupt immediately and the device shuts down and resets O-type I^2C registers.

Thermal Fault

The IC has a die temperature sensing circuit. When the die temperature exceeds the thermal-shutdown threshold, 165°C (T_{SHDN}), the IC shuts down and resets O-type I^2C registers. There is a 15°C thermal hysteresis. After thermal shutdown, if the die temperature reduces by 15°C, the thermal shutdown bus deasserts and the IC re-enables. The battery charger has an independent thermal regulation loop. See the *Thermal Foldback* section for more details.

Register Types and Reset Conditions

The IC has different levels of reset as defined below:

- S-type: registers are reset each time when: V_{AVL} < 1.8V. S-type registers include TOP registers from 0x00 to 0x05; CHARGER_FUNC registers 0x10, 0x12, 0x13, 0x14, 0x15.
- O-type: registers are reset each time when: V_{AVL} < 1.8V or V_{SYS} < $V_{SYSUVLO}$ or V_{SYS} > $V_{SYSOVLO}$ or die temperature > T_{SHDN} or software reset (SW_RST). O-type registers include CHARGER_FUNC registers 0x11, and all registers from 0x16 to 0x20.

Charger Register Write Protection

CHG_CNFG register 1, 2, 3, 4, 5, 7, 8, 9 (CHARGER_FUNC register address 0x17, 0x18, 0x19, 0x1A, 0x1B, 0x1D, 0x1E, 0x1F) are protected by CHG_CNFG_06.CHGPROT bitfield. By default, these configurations are not writable, and need unlocking by writing bitfield CHGPROT = 0x3 first.

Interrupt Output (INTB)

The INTB is an active-low, open-drain output. Connect a pullup resistor to the pullup power source.

The ICs INTB can be connected to the host's interrupt input and signals to the host when unmasked interrupt events occur within the IC.

I²C Serial Interface

The I²C serial bus consists of a bidirectional serial-data line (SDA) and a serial clock (SCL). I²C is an open-drain bus. SDA and SCL require pullup resistors (500Ω or greater). Optional 24Ω resistors in series with SDA and SCL help to protect the device inputs from high voltage spikes on the bus lines. Series resistors also minimize crosstalk and undershoot on bus lines.

System Configuration

The I²C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 6 shows an example of a typical I²C system. A device on I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. When the MAX77962 I²C-compatible interface is operating, it is a slave on I²C bus and it can be both a transmitter and a receiver.

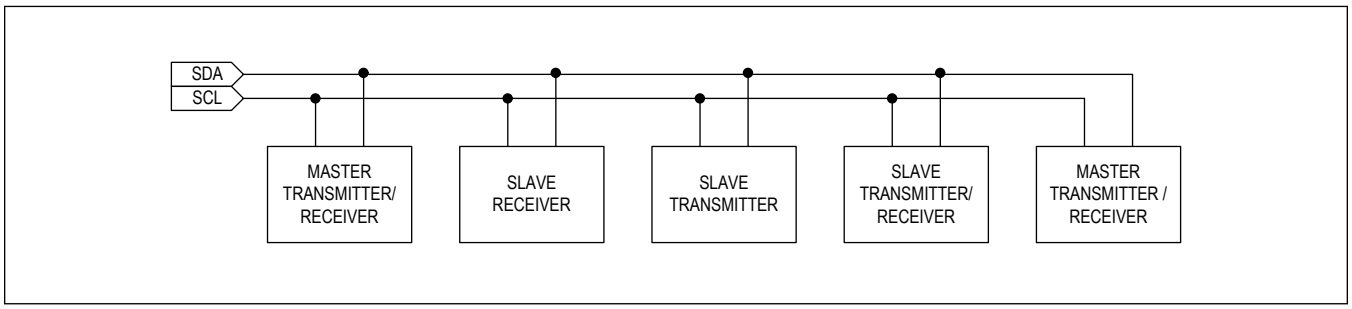


Figure 6. Functional Logic Diagram for Communications Controller

Bit Transfer

One data bit is transferred for each SCL clock cycle. The data on SDA must remain stable during the high portion of SCL clock pulse. Changes in SDA while SCL is high are control signals (START and STOP conditions).

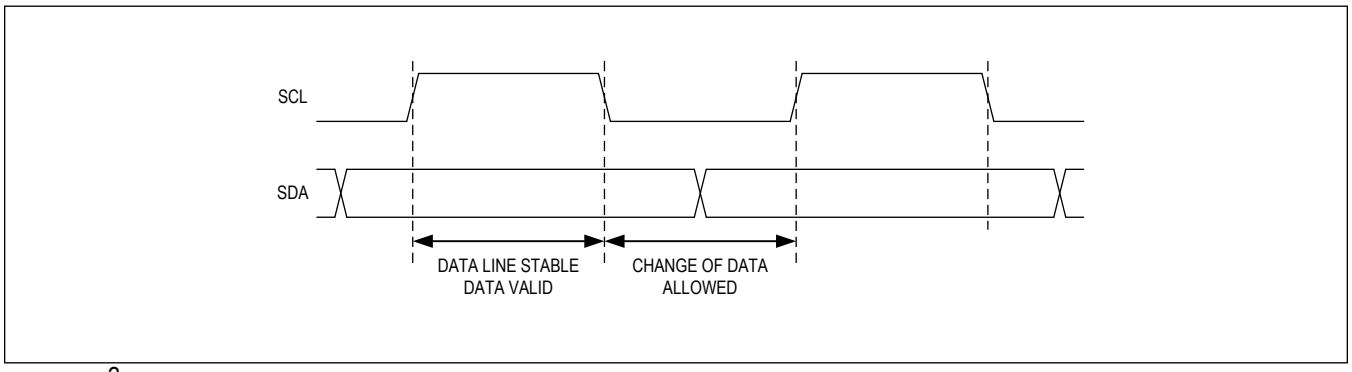


Figure 7. I²C Bit Transfer

START and STOP Conditions

When I^2C serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high.

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a NOT ACKNOWLEDGE followed by a STOP condition.

STOP condition frees the bus. To issue a series of commands to the slave, the master can issue REPEATED START (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a REPEATED START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from I^2C serial interface until the next START condition, minimizing digital noise and feed-through.

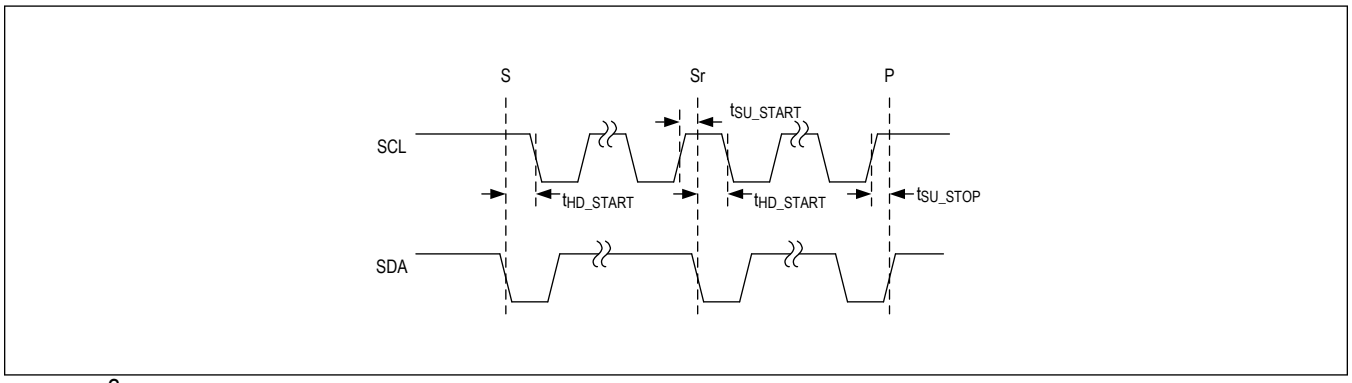


Figure 8. I^2C Start Stop

Acknowledge

Both the I^2C bus master and the IC (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine bit data packet. To generate an ACKNOWLEDGE (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. To generate a NOT-ACKNOWLEDGE (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

Slave Address

The IC acts as a slave transmitter/receiver. The slave address of the IC is 0xD2h/0xD3h. The least significant bit is the read/write indicator (1 for read, 0 for write).

Clock Stretching

In general, the clock signal generation for I^2C bus is the responsibility of the master device. I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

General Call Address

The IC does not implement an I^2C specification general call address. If the IC sees general call address (00000000b), it does not issue an ACKNOWLEDGE (A).

Communication Speed

The IC provides I^2C 3.0-compatible (1MHz) serial interface.

- I^2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast-Mode Plus)
- Does not utilize I^2C Clock Stretching

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *"Pullup Resistor Sizing"* section of the I^2C revision 3.0 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitance of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about a 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that the pullup resistor dissipates power when the open-drain bus is low. The lower the value of the pullup resistor, the higher the power dissipation (V^2/R).

Operating in high-speed mode requires some special considerations. For the full list of considerations, refer to the I^2C 3.0 specification. The major considerations with respect to the IC are:

- I^2C bus master uses current source pullups to shorten the signal rise times.
- I^2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each STOP condition, the IC input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Communication Protocols* section.

Communication Protocols

The IC supports both writing and reading from its registers.

Writing to a Single Register

Figure 9 shows the protocol for the I^2C master device to write one byte of data to the IC. This protocol is the same as SMBus specification's "Write Byte" protocol.

The "Write Byte" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit ($R/\overline{W} = 0$).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

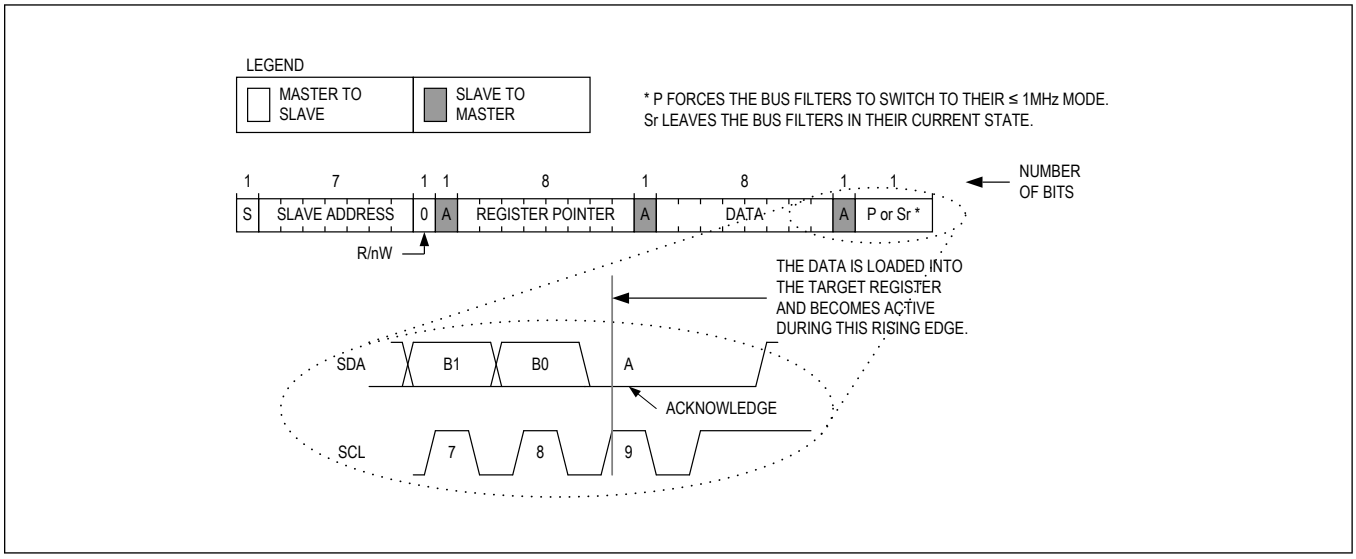


Figure 9. Writing to a Single Register

Writing to Sequential Registers

Figure 10 shows the protocol for writing to sequential registers. This protocol is similar to the “Write Byte” protocol, except the master continues to write after it receives the first byte of data. When the master is done writing, it issues a STOP or REPEATED START.

The “Writing to Sequential Registers” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge related clock pulse, the slave issues an ACKNOWLEDGE (A).
10. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

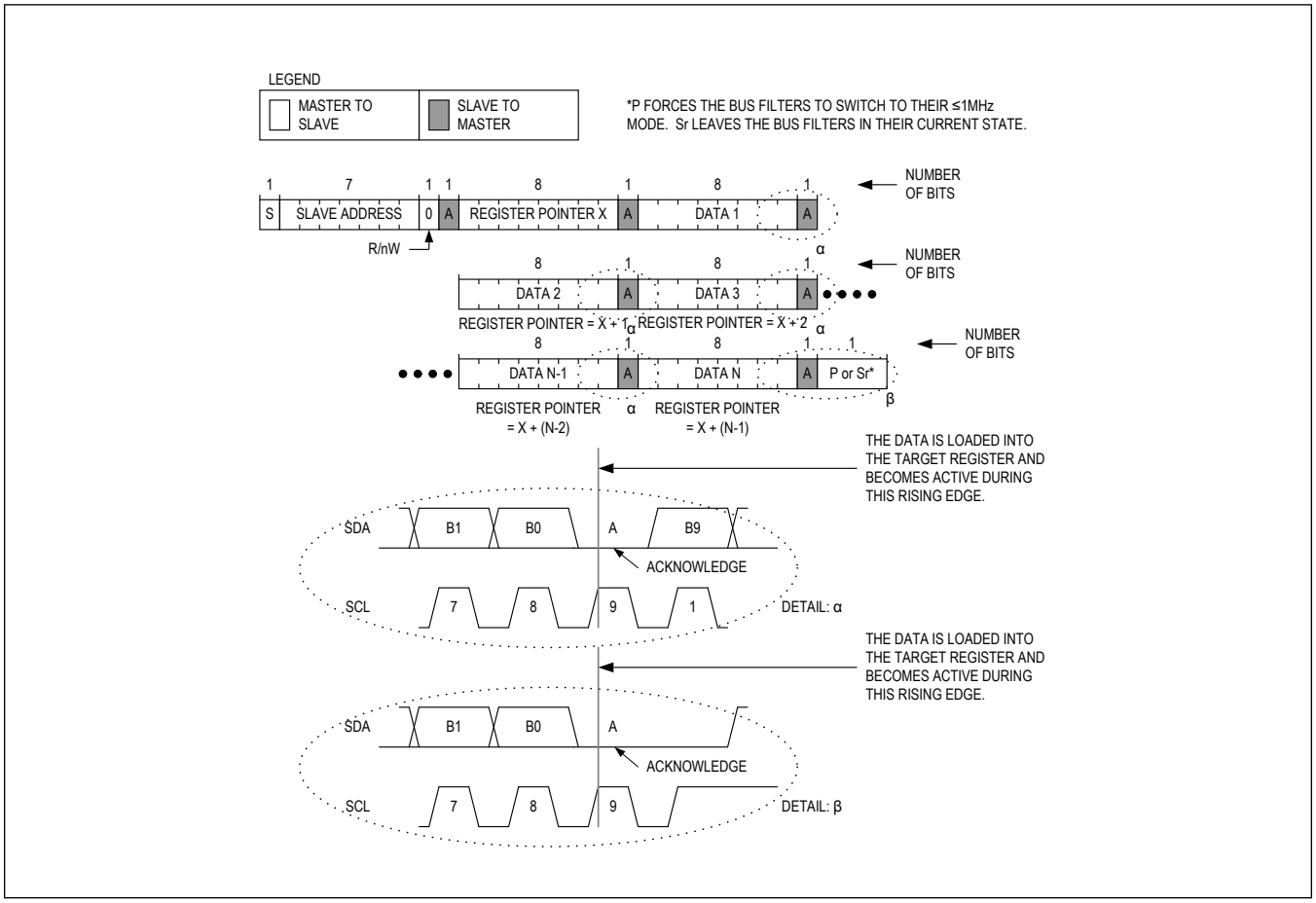


Figure 10. Writing to Sequential Registers

Writing Multiple Bytes using Register-Data Pairs

Figure 11 shows the protocol for the I^2C master device to write multiple bytes to the IC using register-data pairs. This protocol allows the I^2C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a STOP condition.

The “Multiple Byte Register-Data Pair” protocol is as follows:

1. The master sends a START command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. At the rising edge of SCL, the data byte is loaded into its target register and the data becomes active.
8. Steps 4 to 7 are repeated as many times as the master requires.
9. The master sends a STOP condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

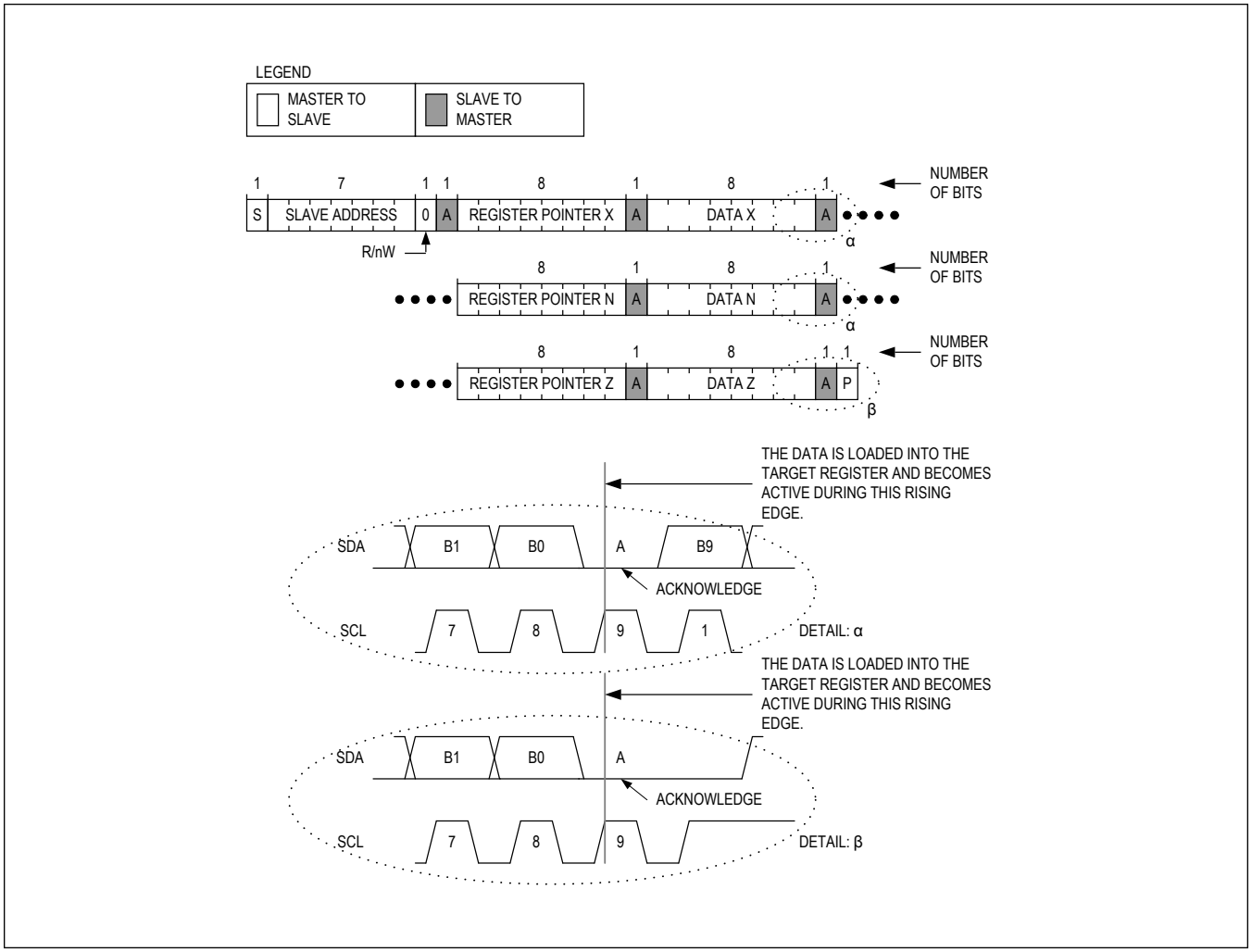


Figure 11. Writing to Multiple Registers with “Multiple Byte Register-Data Pairs” Protocol

Reading from a Single Register

The I^2C master device reads one byte of data to the IC. This protocol is the same as SMBus specification's "Read Byte" protocol.

The "Read Byte" protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues a NOT-ACKNOWLEDGE (nA).
11. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

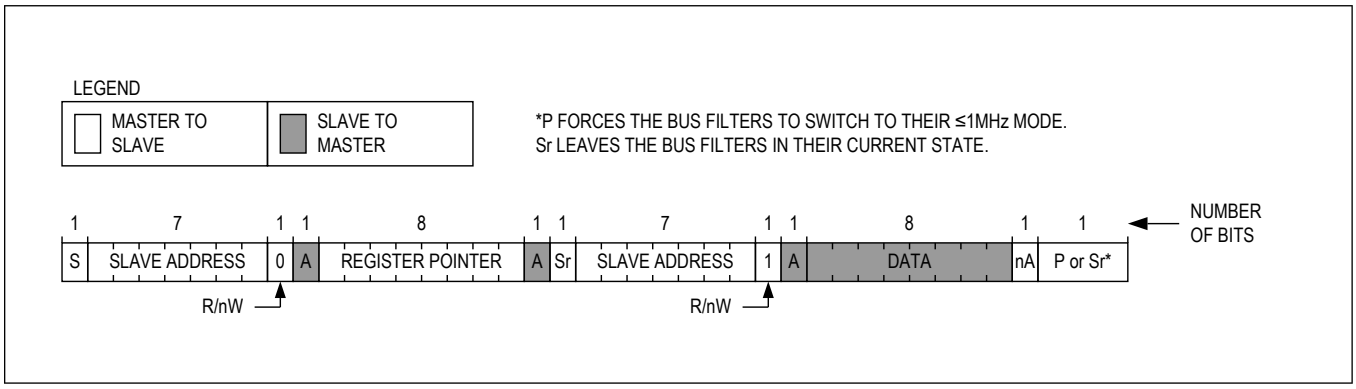


Figure 12. Reading from a Single Register

Reading from Sequential Registers

Figure 13 shows the protocol for reading from sequential registers. This protocol is similar to the “Read Byte” protocol except the master issues an ACKNOWLEDGE (A) to signal the slave that it wants more data—when the master has all the data it requires, it issues a not-acknowledge (nA) and a STOP (P) to end the transmission.

The “Continuous Read from Sequential Registers” protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a REPEATED START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ =1).
8. The addressed slave asserts an ACKNOWLEDGE (A) by pulling SDA low.
9. The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10. The master issues an ACKNOWLEDGE (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a NOT-ACKNOWLEDGE (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a REPEATED START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing a REPEATED START (Sr) leaves the bus input filters in their current state.

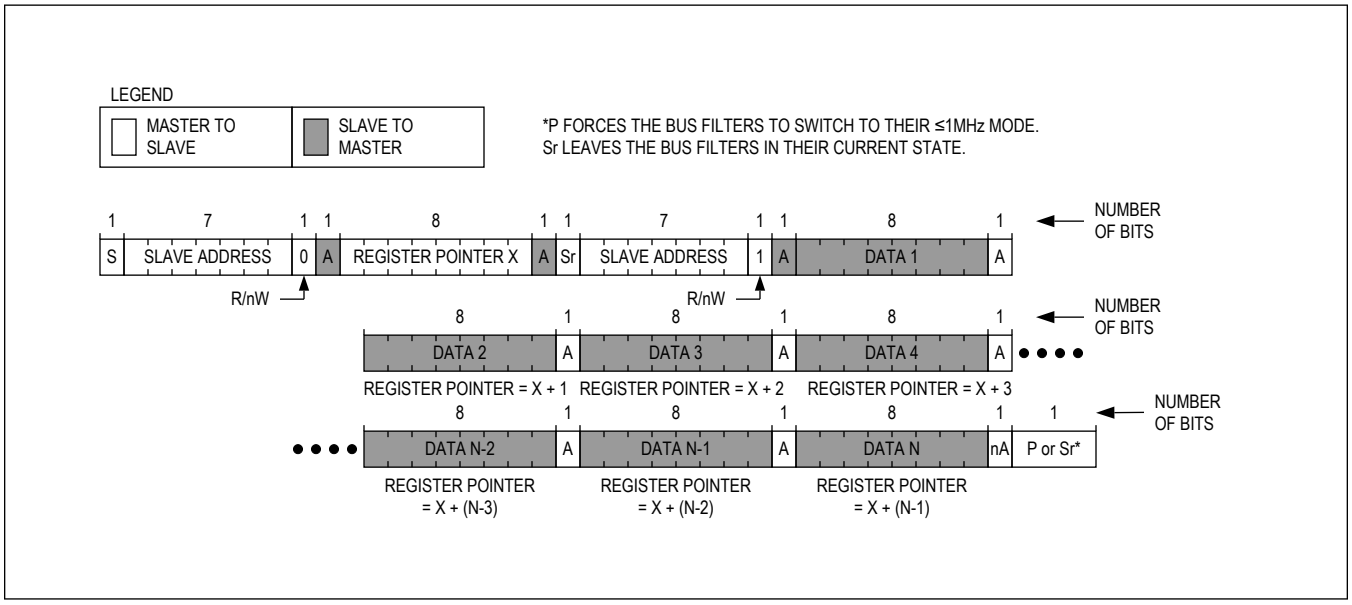


Figure 13. Reading from Sequential Registers

Register Map

FUNC

ADDRESS	NAME	MSB							LSB
TOP									
0x00	CID[7:0]	CID[7:0]							
0x01	CHIP_REV[7:0]	REVISION[2:0]			VERSION[4:0]				
0x02	SWRST[7:0]	SW_RST[7:0]							
0x03	TOP_INT[7:0]	SPR[4:0]					TSHDN_I	SYSOVLO_I	SYSUVLO_I
0x04	TOP_INT_MASK[7:0]	SPR[4:0]					TSHDN_M	SYSOVLO_M	SYSUVLO_M
0x05	TOP_INT_OK[7:0]	SPR[4:0]					TSHDN_OK	SYSOVLO_OK	SYSUVLO_OK
CHARGER_FUNC									
0x10	CHG_INT[7:0]	AICL_I	CHGIN_I	B2SOVRC_I	CHG_I	BAT_I	CHGINILIM_I	DISQBAT_I	OTG_PLIM_I
0x11	CHG_INT_MASK[7:0]	AICL_M	CHGIN_M	B2SOVRC_M	CHG_M	BAT_M	CHGINILIM_M	DISQBAT_M	OTG_PLIM_M
0x12	CHG_INT_OK[7:0]	AICL_OK	CHGIN_OK	B2SOVRC_OK	CHG_OK	BAT_OK	CHGINILIM_OK	DISQBAT_OK	OTG_PLIM_OK
0x13	CHG_DETAILS_00[7:0]	SPR7	CHGIN_DTLS[1:0]		OTG_DTLS[1:0]		SPR2_1[1:0]		QB_DTLS
0x14	CHG_DETAILS_01[7:0]	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
0x15	CHG_DETAILS_02[7:0]	SPR	THM_DTLS[2:0]			APP_MODE_DTLS	FSW_DTLS[1:0]		NUM_CELL_DTLS
0x16	CHG_CNFG_00[7:0]	COMM_MODE	DISIBS	STBY_EN	WDTEN	MODE[3:0]			
0x17	CHG_CNFG_01[7:0]	PQEN	LPM	CHG_RSTRT[1:0]		STAT_EN	FCHGTIME[2:0]		
0x18	CHG_CNFG_02[7:0]	CHGCC[7:0]							
0x19	CHG_CNFG_03[7:0]	SYS_TRACK_DIS	B2SOVRC_DTC	TO_TIME[2:0]			TO_ITH[2:0]		
0x1A	CHG_CNFG_04[7:0]	CHGCC_MSB	CHG_CV_PRM[6:0]						
0x1B	CHG_CNFG_05[7:0]	CHGR_CV_OFFSET[1:0]		ITRICKLE[1:0]		B2SOVRC[3:0]			
0x1C	CHG_CNFG_06[7:0]	CHGCC_WR_EN	RESERVED[1:0]		SPR	CHGPROT[1:0]		WDTCLR[1:0]	
0x1D	CHG_CNFG_07[7:0]	JEITA_EN	REGTEMP[3:0]				VCHGCV_COOL	ICHGCC_COOL	FSHIP_MODE
0x1E	CHG_CNFG_08[7:0]	RESERVED	CHGIN_ILIM[6:0]						
0x1F	CHG_CNFG_09[7:0]	INLIM_CLK[1:0]		OTG_ILIM[2:0]			MINVSYS[2:0]		
0x20	CHG_CNFG_10[7:0]	CHGCC_OFFSET[1:0]		VCHGIN_REG[4:0]					DISKIP

Register Details

CID (0x0)

BIT	7	6	5	4	3	2	1	0
Field	CID[7:0]							
Reset	0x84							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
CID	7:0	Chip ID

CHIP_REV (0x1)

BIT	7	6	5	4	3	2	1	0
Field	REVISION[2:0]			VERSION[4:0]				
Reset	0x1			0x0				
Access Type	Read Only			Read Only				

BITFIELD	BITS	DESCRIPTION	DECODE
REVISION	7:5	Silicon Revision	0x1: Pass1
VERSION	4:0		

SWRST (0x2)

BIT	7	6	5	4	3	2	1	0
Field	SW_RST[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
SW_RST	7:0	Software Reset	0xA5: O-type registers are reset. SW_RST register is auto-clear as under O-type reset control. All others: No reset

TOP_INT (0x3)

BIT	7	6	5	4	3	2	1	0
Field	SPR[4:0]					TSHDN_I	SYSOVLO_I	SYSUVLO_I
Reset	0x0					0x0	0x0	0x0
Access Type	Read Clears All					Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:3	Spare Bit	
TSHDN_I	2	Thermal Shutdown Interrupt	0b0: No interrupt detected 0b1: Interrupt detected

BITFIELD	BITS	DESCRIPTION	DECODE
SYSOVLO_I	1	SYSOVLO Interrupt	0b0: No interrupt detected 0b1: Interrupt detected
SYSUVLO_I	0	SYSUVLO Interrupt	0b0: No interrupt detected 0b1: Interrupt detected

TOP_INT_MASK (0x4)

BIT	7	6	5	4	3	2	1	0
Field	SPR[4:0]					TSHDN_M	SYSOVLO_M	SYSUVLO_M
Reset	0x1F					0x1	0x1	0x1
Access Type	Write, Read					Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:3	Spare Bit	
TSHDN_M	2	Thermal Shutdown Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSOVLO_M	1	SYSOVLO Interrupt Mask	0b0: Unmasked 0b1: Masked
SYSUVLO_M	0	SYSUVLO Interrupt Mask	0b0: Unmasked 0b1: Masked

TOP_INT_OK (0x5)

BIT	7	6	5	4	3	2	1	0
Field	SPR[4:0]					TSHDN_OK	SYSOVLO_OK	SYSUVLO_OK
Reset	0x0					0x1	0x1	0x1
Access Type	Read Only					Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7:3	Spare Bit	
TSHDN_OK	2	Thermal Shutdown Status Indicator	0b0: Device is in thermal shutdown 0b1: Device is not in thermal shutdown
SYSOVLO_OK	1	SYSOVLO Status Indicator	0b0: SYS voltage is above SYSOVLO threshold 0b1: SYS voltage is below SYSOVLO threshold
SYSUVLO_OK	0	SYSUVLO Status Indicator	0b0: SYS voltage is below SYSUVLO threshold 0b1: SYS voltage is above SYSUVLO threshold

CHG_INT (0x10)

Interrupt status register for the charger block.

BIT	7	6	5	4	3	2	1	0
Field	AICL_I	CHGIN_I	B2SOVRC_I	CHG_I	BAT_I	CHGINILIM_I	DISQBAT_I	OTG_PLIM_I
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_I	7	AICL Interrupt	0b0: The AICL_OK bit has not changed since the last time this bit was read. 0b1: The AICL_OK bit has changed since the last time this bit was read.
CHGIN_I	6	CHGIN Interrupt	0b0: The CHGIN_OK bit has not changed since the last time this bit was read. 0b1: The CHGIN_OK bit has changed since the last time this bit was read.
B2SOVRC_I	5	B2SOVRC Interrupt	0b0: The B2SOVRC_OK bit has not changed since the last time this bit was read. 0b1: The B2SOVRC_OK bit has changed since the last time this bit was read.
CHG_I	4	Charger Interrupt	0b0: The CHG_OK bit has not changed since the last time this bit was read. 0b1: The CHG_OK bit has changed since the last time this bit was read.
BAT_I	3	Battery Interrupt	0b0: The BAT_OK bit has not changed since the last time this bit was read. 0b1: The BAT_OK bit has changed since the last time this bit was read.
CHGINILIM_I	2	CHGINILIM Interrupt	0b0: The CHGINILIM_OK bit has not changed since the last time this bit was read. 0b1: The CHGINILIM_OK bit has changed since the last time this bit was read.
DISQBAT_I	1	DISQBAT Interrupt	0b0: The DISQBAT_OK bit has not changed since the last time this bit was read. 0b1: The DISQBAT_OK bit has changed since the last time this bit was read.
OTG_PLIM_I	0	OTG Interrupt/PLIM Interrupt	0b0: Mode = 0xA: The OTG_OK bit has not changed since the last time this bit was read. Mode ≠ 0xA: PLIM_OK bit has not changed since the last time this bit was read. 0b1: Mode = 0xA: The OTG_OK bit has changed since the last time this bit was read. Mode ≠ 0xA: The PLIM_OK bit has changed since the last time this bit was read.

CHG_INT_MASK (0x11)

Mask register to mask the corresponding charger interrupts.

BIT	7	6	5	4	3	2	1	0
Field	AICL_M	CHGIN_M	B2SOVRC_M	CHG_M	BAT_M	CHGINILIM_M	DISQBAT_M	OTG_PLIM_M
Reset	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_M	7	AICL Interrupt Mask	0b0: Unmasked 0b1: Masked
CHGIN_M	6	CHGIN Interrupt Mask	0b0: Unmasked 0b1: Masked

BITFIELD	BITS	DESCRIPTION	DECODE
B2SOVRC_M	5	B2SOVRC Interrupt Mask	0b0: Unmasked 0b1: Masked
CHG_M	4	Charger Interrupt Mask	0b0: Unmasked 0b1: Masked
BAT_M	3	Battery Interrupt Mask	0b0: Unmasked 0b1: Masked
CHGINILIM_M	2	CHGINILIM Interrupt Mask	0b0: Unmasked 0b1: Masked
DISQBAT_M	1	DISQBAT Interrupt Mask	0b0: Unmasked 0b1: Masked
OTG_PLIM_M	0	OTG/PLIM Interrupt Mask	0b0: Unmasked 0b1: Masked

CHG_INT_OK (0x12)

BIT	7	6	5	4	3	2	1	0
Field	AICL_OK	CHGIN_OK	B2SOVRC_OK	CHG_OK	BAT_OK	CHGINILIM_OK	DISQBAT_OK	OTG_PLIM_OK
Reset	0x1	0x0	0x1	0x1	0x1	0x1	0x1	0x1
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
AICL_OK	7	AICL_OK Status	0b0: AICL mode 0b1: Not in AICL mode
CHGIN_OK	6	CHGIN Input Status Indicator. See CHGIN_DTLS for more information.	0b0: The CHGIN input is invalid. CHGIN_DTLS ≠ 0x03 0b1: The CHGIN input is valid. CHGIN_DTLS = 0x03
B2SOVRC_OK	5	B2SOVRC Status	0b0: BATT to SYS exceeds current limit. 0b1: BATT to SYS does not exceed current limit.
CHG_OK	4	Charger Status Indicator. See CHG_DTLS for more information.	0b0: The charger has reduced charge current or charge termination voltage based on JEITA control, or suspended charging, or TREG = 1. 0b1: The charger is okay or the charger is off.
BAT_OK	3	Battery Status Indicator. See BAT_DTLS for more information.	0b0: The battery has an issue or the charger has been suspended. BAT_DTLS ≠ 0x03 and ≠ 0x07 0b1: The battery is okay. BAT_DTLS = 0x03 or 0x07
CHGINILIM_OK	2	CHGINILIM status	0b0: The CHGIN input has reached the current limit. 0b1: The CHGIN input has not reached the current limit.
DISQBAT_OK	1	DISQBAT Status	0b0: DISQBAT pin is high or DISIBS bit is set to '1' and Q_{BAT} is disabled. 0b1: DISQBAT is low and DISIBS bit is '0' and Q_{BAT} is not disabled.

BITFIELD	BITS	DESCRIPTION	DECODE
OTG_PLIM_OK	0	Mode = 0xA: OTG Status Indicator. See OTG_DTLS for more information. Mode ≠ 0xA: PLIM Status Indicator. (Buck-boost limit reached.)	0b0: Mode = 0xA: There is a fault in OTG mode. OTG_DTLS ≠ 0x11 Mode ≠ 0xA: Buck-boost reaches positive current limit. 0b1: Mode = 0xA: The OTG operation is okay. OTG_DTLS = 0x11 Mode ≠ 0xA: Buck-boost does not reach positive current limit.

CHG_DETAILS_00 (0x13)

BIT	7	6	5	4	3	2	1	0
Field	SPR7	CHGIN_DTLS[1:0]		OTG_DTLS[1:0]		SPR2_1[1:0]		QB_DTLS
Reset	0x0	0x0		0x0		0x0		0x0
Access Type	Read Only	Read Only		Read Only		Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPR7	7	Spare Bit	
CHGIN_DTLS	6:5	CHGIN Details	0b00: V_{BUS} is invalid. $V_{CHGIN} < V_{CHGIN\_UVLO}$ 0b01: RSVD 0b10: V_{BUS} is invalid. $V_{CHGIN} > V_{CHGIN\_OVLO}$ 0b11: V_{BUS} is valid. $V_{CHGIN} > V_{CHGIN\_UVLO}$ and $V_{CHGIN} < V_{CHGIN\_OVLO}$
OTG_DTLS	4:3	OTG Details	0b00: OTG output (V_{CHGIN}) is in undervoltage condition. $V_{CHGIN} < V_{OTG\_UVLO}$ 0b01: OTG output (V_{CHGIN}) is in current limit (OTG_ILIM) within the last 37.5ms. 0b10: OTG output (V_{CHGIN}) is in overvoltage condition. $V_{CHGIN} > V_{OTG\_OVLO}$ 0b11: OTG is disabled (OTGEN = L and MODE ≠ 0xA) or OTG output (V_{CHGIN}) is valid. $V_{CHGIN} > V_{OTG\_UVLO}$ and $V_{CHGIN} < V_{OTG\_OVLO}$ and it is not in current limit.
SPR2_1	2:1		
QB_DTLS	0	Q_{BAT} status Read back value of QB_DTLS reflects the actual Q_{BAT} state.	0b0: Q_{BAT} is OFF 0b1: Q_{BAT} is ON

CHG_DETAILS_01 (0x14)

BIT	7	6	5	4	3	2	1	0
Field	TREG	BAT_DTLS[2:0]			CHG_DTLS[3:0]			
Reset	0x0	0x7			0x8			
Access Type	Read Only	Read Only			Read Only			

BITFIELD	BITS	DESCRIPTION	DECODE
TREG	7	Temperature Regulation Status	0b0: The junction temperature is less than the threshold set by REGTEMP and the full charge current limit is available. 0b1: The junction temperature is greater than the threshold set by REGTEMP and the charge current limit may be folding back to reduce power dissipation.
BAT_DTLS	6:4	Battery Details **Note**: Only B2SOVRC is reported in battery-only mode. As a consequence, BAT_OK = 1 is also reported in BAT_DTLS = 0x07. In the event that multiple faults occur within the battery details category, overcurrent has priority followed by no-battery, then over-voltage, then timer fault, and then below prequal.	0b000: Battery removal is detected on THM pin. 0b001: $V_{BATT} < V_{PRECHG}$. This condition is also reported in the CHG_DTLS as 0x00. 0b010: The battery is taking longer than expected to charge. This could be due to high system currents, an old battery, a damaged battery, or something else. Charging has suspended and the charger is in its timer-fault mode. This condition is also reported in the CHG_DTLS as 0x06. 0b011: The battery is okay and its voltage is greater than the minimum system voltage (V_{SYSMIN} - 500mV < V_{BATT}), Q_{BAT} is on and V_{SYS} is approximately equal to V_{BATT}. 0b100: The battery is okay but its voltage is low: $V_{PRECHG} < V_{BATT} < V_{SYSMIN}$ - 500mV. This condition is also reported in the CHG_DTLS as 0x00. 0b101: The battery voltage has been greater than the battery-overvoltage threshold (CHG_CV_PRM + 240mV/cell) for the last 30ms. This flag is only generated when there is a valid input. 0b110: The battery has been overcurrent for at least 3ms since the last time this register has been read. 0b111: Battery level not available. In battery only mode, all battery comparators are off except for B2SOVRC.

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_DTLS	3:0	Charger Details	0x00: Charger is in precharge or trickle-charge mode. CHG_OK = 1 and $V_{BATT} < V_{SYSMIN}$ - 500mV and $T_J < T_{SHDN}$ 0x01: Charger is in fast-charge constant current mode. CHG_OK = 1 and $V_{BATT} < V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x02: Charger is in fast-charge constant voltage mode. CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x03: Charger is in top-off mode. CHG_OK = 1 and $V_{BATT} = V_{BATTREG}$ and $T_J < T_{SHDN}$ 0x04: Charger is in done mode. CHG_OK = 0 and $V_{BATT} > V_{BATTREG} - V_{RSTRT}$ and $T_J < T_{SHDN}$ 0x05: Charger is off because at least one pin (INLIM, ITO, ISET, VSET) has valid resistance while others do not (invalid resistance, open, or tied to PVL). Configure charger with the I^2C interface, then set COMM_MODE to '1' to enable charging. CHG_OK = 0 0x06: Charger is in timer-fault mode. CHG_OK = 0 and if BAT_DTLS = 0b001 then $V_{BATT} < V_{SYSMIN}$ - 500mV or $V_{BATT} < V_{PRECHG}$ and $T_J < T_{SHDN}$ 0x07: Charger is suspended because Q_{BAT} is disabled (DISQBAT = H or DISIBS = 1). CHG_OK = 0 0x08: Charger is off, charger input invalid and/or charger is disabled. CHG_OK = 1 0x09: Reserved 0x0A: Charger is off and the junction temperature is > T_{SHDN}. CHG_OK = 0 0x0B: Charger is off because the watchdog timer expired. CHG_OK = 0 0x0C: Charger is suspended, or charge current, or voltage is reduced based on JEITA control. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0D: Charger is suspended because battery removal is detected on THM pin. This condition is also reported in THM_DTLS. CHG_OK = 0 0x0E: Reserved 0x0F: Reserved

CHG_DETAILS_02 (0x15)

BIT	7	6	5	4	3	2	1	0
Field	SPR	THM_DTLS[2:0]			APP_MODE_DTLS	FSW_DTLS[1:0]		NUM_CELL_DTLS
Reset	0x0	0x2			0x0	0x0		0x0
Access Type	Read Only	Read Only			Read Only	Read Only		Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
SPR	7	Spare Bit	
THM_DTLS	6:4	Thermistor Status This is also reported in the CHG_DTLS as 0x0C.	0b000: Low temperature and charging suspended (COLD). 0b001: Low temperature charging (COOL). 0b010: Normal temperature charging (NORMAL). 0b011: High temperature charging (WARM). 0b100: High temperature and charging suspended (HOT). 0b101: Battery removal detected on THM pin. 0b110: Thermistor monitoring is disabled. 0b111: Reserved
APP_MODE_DTLS	3	Application Mode Status	0b0: Device is configured to operate as a standalone DC-DC converter. 0b1: Device is configured to operate as a charger.
FSW_DTLS	2:1	Programmed Switching Frequency Details	0b00: 600kHz 0b01: 1.2MHz 0b10: Reserved 0b11: Reserved
NUM_CELL_DTLS	0	Number of Serially Connected Battery Cells Details	0b0: Device is configured to support a 2-cell battery. 0b1: Device is configured to support a 3-cell battery.

CHG_CNFG_00 (0x16)

Charger configuration 0

BIT	7	6	5	4	3	2	1	0
Field	COMM_MODE	DISIBS	STBY_EN	WDTEN	MODE[3:0]			
Reset	0x0	0x0	0x0	0x0	0x5			
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
COMM_MODE	7	I^2C Mode Enable	0b0: Autonomous mode CHGIN_ILIM, CHGCC, CHG_CV_PRM, and TO_ITH registers are programmed by external resistors on INLIM, ISET, VSET, and ITO pins Writing 0 to COMM_MODE is ignored. 0b1: I^2C mode enabled. CHGIN_ILIM, CHGCC, CHG_CV_PRM, and TO_ITH registers are programmed by I^2C. Writing 1 to COMM_MODE is allowed. Writting COMM_MODE = 1 clears any charger suspension due to invalid resistance detected on INLIM, ISET, VSET, and ITO pins. Charger starts with I^2C programmed settings in CHGIN_ILIM, CHGCC, CHG_CV_PRM, and TO_ITH registers.
DISIBS	6	BATT to SYS FET Disable Control. Read back value of DISIBS register bit reflects the actual DISIBS command or DISQBAT pin state.	0b0: BATT to SYS FET is controlled by the power-path state machine. 0b1: BATT to SYS FET is forced off.
STBY_EN	5	CHGIN Standby Enable. Read back value of the STBY_EN register bit reflects the actual CHGIN standby setting.	0b0: DC-DC is controlled by the power-path state machine. 0b1: Force DC-DC off. Device goes to CHGIN low quiescent current standby.
WDTEN	4	Watchdog Timer Enable While enabled, the system controller must reset the watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the watchdog timer by programming WDTCLR = 0x01.	0b0: Watchdog timer disabled 0b1: Watchdog timer enabled

BITFIELD	BITS	DESCRIPTION	DECODE
MODE	3:0	Smart Power Selector Configuration. Read back value of the MODE register reflects the actual Smart Power Selector configuration.	0x0: Charger = off, OTG = off, DC-DC = off. When the Q_{BAT} switch is on (DISQBAT = L and DISIBS = 0), the battery powers the system. 0x1: Same as 0b0000 0x2: Same as 0b0000 0x3: Same as 0b0000 0x4: Charger = off, OTG = off, DC-DC = on. When there is a valid input, the DC-DC converter regulates the system voltage to be the maximum of (V_{SYSMIN} and V_{BATT} + 4%). 0x5: Charger = on,OTG = off, DC-DC = on. When there is a valid input, the battery is charging. V_{SYS} is the larger of V_{SYSMIN} and ~V_{BATT} + I_{BATT} x $R_{BAT2SYS}$. 0x6: Same as 0b0101 0x7: Same as 0b0101 0x8: Reserved 0x9: Reserved 0xA: Charger = off, OTG = on, DC-DC = off. The Q_{BAT} switch is on to allow the battery to support the system, and the charger's DC-DC operates in reverse mode as a buck converter. The OTG output, CHGIN, can source current up to $I_{CHGIN.OTG.LIM}$. The CHGIN target voltage is $V_{CHGIN.OTG}$. 0xB: Reserved 0xC: Reserved 0xD: Reserved 0xE: Reserved 0xF: Reserved

CHG_CNFG_01 (0x17)

Charger configuration 1

BIT	7	6	5	4	3	2	1	0
Field	PQEN	LPM	CHG_RSTRT[1:0]		STAT_EN	FCHGTIME[2:0]		
Reset	0x1	0x0	0x1		0x1	0x1		
Access Type	Write, Read	Write, Read	Write, Read		Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
PQEN	7	Low-Battery Prequalification Mode Enable	0b0: Low-battery prequalification mode is disabled. 0b1: Low-battery prequalification mode is enabled.
LPM	6	Low-Power Mode Control	0b0: Q_{BAT} charge pump runs in normal mode. 0b1: Q_{BAT} charge pump is in low-power mode.
CHG_RSTRT	5:4	Charger Restart Threshold	0b00: 100mV/cell below the value programmed by CHG_CV_PRM 0b01: 150mV/cell below the value programmed by CHG_CV_PRM 10: 200mV/cell below the value programmed by CHG_CV_PRM 11: Disabled
STAT_EN	3	Charge Indicator Output Enable	0b0: Disable STAT output 0b1: Enable STAT output

BITFIELD	BITS	DESCRIPTION	DECODE
FCHGTIME	2:0	Fast-Charge Timer Setting (t_{FC}, hrs)	0b000: Disabled 0b001: 3 0b010: 4 0b011: 5 0b100: 6 0b101: 7 0b110: 8 0b111: 10

CHG_CNFG_02 (0x18)

Charger configuration 2

BIT	7	6	5	4	3	2	1	0
Field	CHGCC[7:0]							
Reset	0x40							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
CHGCC	7:0	Fast-Charge Current Selection (mA). When the charger is enabled, the charge current limit is set by these bits. Read back value of the CHGCC register reflects the actual fast-charge current programmed in the charger. The thermal foldback loop can reduce the battery charger's target current by A_{TJREG}.	0x000: 50 0x001: 56.25 0x002: 62.5 0x003: 68.75 0x004: 75 0x005: 81.25 0x006: 87.5 0x007: 93.75 0x008: 100 0x009: 106.25 0x00A: 112.5 0x00B: 118.75 0x00C: 125 0x00D: 131.25 0x00E: 137.5 0x00F: 143.75 0x010: 150 0x011: 156.25 0x012: 162.5 0x013: 168.75 0x014: 175 0x015: 181.25 0x016: 187.5 0x017: 193.75 0x018: 200 0x019: 206.25 0x01A: 212.5 0x01B: 218.75 0x01C: 225 0x01D: 231.25 0x01E: 237.5 0x01F: 243.75 0x020: 250 0x021: 256.25 0x022: 262.5 0x023: 268.75 0x024: 275 0x025: 281.25 0x026: 287.5 0x027: 293.75 0x028: 300 0x029: 306.25 0x02A: 312.5 0x02B: 318.75 0x02C: 325 0x02D: 331.25 0x02E: 337.5 0x02F: 343.75 0x030: 350 0x031: 356.25 0x032: 362.5 0x033: 368.75 0x034: 375 0x035: 381.25 0x036: 387.5 0x037: 393.75 0x038: 400 0x039: 406.25 0x03A: 412.5

BITFIELD	BITS	DESCRIPTION	DECODE
			0x03B: 418.75 0x03C: 425 0x03D: 431.25 0x03E: 437.5 0x03F: 443.75 0x040: 450 0x041: 456.25 0x042: 462.5 0x043: 468.75 0x044: 475 0x045: 481.25 0x046: 487.5 0x047: 493.75 0x048: 500 0x049: 506.25 0x04A: 512.5 0x04B: 518.75 0x04C: 525 0x04D: 531.25 0x04E: 537.5 0x04F: 543.75 0x050: 550 0x051: 556.25 0x052: 562.5 0x053: 568.75 0x054: 575 0x055: 581.25 0x056: 587.5 0x057: 593.75 0x058: 600 0x059: 606.25 0x05A: 612.5 0x05B: 618.75 0x05C: 625 0x05D: 631.25 0x05E: 637.5 0x05F: 643.75 0x060: 650 0x061: 656.25 0x062: 662.5 0x063: 668.75 0x064: 675 0x065: 681.25 0x066: 687.5 0x067: 693.75 0x068: 700 0x069: 706.25 0x06A: 712.5 0x06B: 718.75 0x06C: 725 0x06D: 731.25 0x06E: 737.5 0x06F: 743.75 0x070: 750 0x071: 756.25 0x072: 762.5 0x073: 768.75 0x074: 775 0x075: 781.25

BITFIELD	BITS	DESCRIPTION	DECODE
			0x076: 787.5 0x077: 793.75 0x078: 800 0x079: 806.25 0x07A: 812.5 0x07B: 818.75 0x07C: 825 0x07D: 831.25 0x07E: 837.5 0x07F: 843.75 0x080: 850 0x081: 856.25 0x082: 862.5 0x083: 868.75 0x084: 875 0x085: 881.25 0x086: 887.5 0x087: 893.75 0x088: 900 0x089: 906.25 0x08A: 912.5 0x08B: 918.75 0x08C: 925 0x08D: 931.25 0x08E: 937.5 0x08F: 943.75 0x090: 950 0x091: 956.25 0x092: 962.5 0x093: 968.75 0x094: 975 0x095: 981.25 0x096: 987.5 0x097: 993.75 0x098: 1000 0x099: 1006.25 0x09A: 1012.5 0x09B: 1018.75 0x09C: 1025 0x09D: 1031.25 0x09E: 1037.5 0x09F: 1043.75 0x0A0: 1050 0x0A1: 1056.25 0x0A2: 1062.5 0x0A3: 1068.75 0x0A4: 1075 0x0A5: 1081.25 0x0A6: 1087.5 0x0A7: 1093.75 0x0A8: 1100 0x0A9: 1106.25 0x0AA: 1112.5 0x0AB: 1118.75 0x0AC: 1125 0x0AD: 1131.25 0x0AE: 1137.5 0x0AF: 1143.75 0x0B0: 1150

BITFIELD	BITS	DESCRIPTION	DECODE
			0x0B1: 1156.25 0x0B2: 1162.5 0x0B3: 1168.75 0x0B4: 1175 0x0B5: 1181.25 0x0B6: 1187.5 0x0B7: 1193.75 0x0B8: 1200 0x0B9: 1206.25 0x0BA: 1212.5 0x0BB: 1218.75 0x0BC: 1225 0x0BD: 1231.25 0x0BE: 1237.5 0x0BF: 1243.75 0x0C0: 1250 0x0C1: 1256.25 0x0C2: 1262.5 0x0C3: 1268.75 0x0C4: 1275 0x0C5: 1281.25 0x0C6: 1287.5 0x0C7: 1293.75 0x0C8: 1300 0x0C9: 1306.25 0x0CA: 1312.5 0x0CB: 1318.75 0x0CC: 1325 0x0CD: 1331.25 0x0CE: 1337.5 0x0CF: 1343.75 0x0D0: 1350 0x0D1: 1356.25 0x0D2: 1362.5 0x0D3: 1368.75 0x0D4: 1375 0x0D5: 1381.25 0x0D6: 1387.5 0x0D7: 1393.75 0x0D8: 1400 0x0D9: 1406.25 0x0DA: 1412.5 0x0DB: 1418.75 0x0DC: 1425 0x0DD: 1431.25 0x0DE: 1437.5 0x0DF: 1443.75 0x0E0: 1450 0x0E1: 1456.25 0x0E2: 1462.5 0x0E3: 1468.75 0x0E4: 1475 0x0E5: 1481.25 0x0E6: 1487.5 0x0E7: 1493.75 0x0E8: 1500 0x0E9: 1506.25 0x0EA: 1512.5 0x0EB: 1518.75

BITFIELD	BITS	DESCRIPTION	DECODE
			0x0EC: 1525 0x0ED: 1531.25 0x0EE: 1537.5 0x0EF: 1543.75 0x0F0: 1550 0x0F1: 1556.25 0x0F2: 1562.5 0x0F3: 1568.75 0x0F4: 1575 0x0F5: 1581.25 0x0F6: 1587.5 0x0F7: 1593.75 0x0F8: 1600 0x0F9: 1606.25 0x0FA: 1612.5 0x0FB: 1618.75 0x0FC: 1625 0x0FD: 1631.25 0x0FE: 1637.5 0x0FF: 1643.75 0x100: 1650 0x101: 1656.25 0x102: 1662.5 0x103: 1668.75 0x104: 1675 0x105: 1681.25 0x106: 1687.5 0x107: 1693.75 0x108: 1700 0x109: 1706.25 0x10A: 1712.5 0x10B: 1718.75 0x10C: 1725 0x10D: 1731.25 0x10E: 1737.5 0x10F: 1743.75 0x110: 1750 0x111: 1756.25 0x112: 1762.5 0x113: 1768.75 0x114: 1775 0x115: 1781.25 0x116: 1787.5 0x117: 1793.75 0x118: 1800 0x119: 1806.25 0x11A: 1812.5 0x11B: 1818.75 0x11C: 1825 0x11D: 1831.25 0x11E: 1837.5 0x11F: 1843.75 0x120: 1850 0x121: 1856.25 0x122: 1862.5 0x123: 1868.75 0x124: 1875 0x125: 1881.25 0x126: 1887.5

BITFIELD	BITS	DESCRIPTION	DECODE
			0x127: 1893.75 0x128: 1900 0x129: 1906.25 0x12A: 1912.5 0x12B: 1918.75 0x12C: 1925 0x12D: 1931.25 0x12E: 1937.5 0x12F: 1943.75 0x130: 1950 0x131: 1956.25 0x132: 1962.5 0x133: 1968.75 0x134: 1975 0x135: 1981.25 0x136: 1987.5 0x137: 1993.75 0x138: 2000 0x139: 2006.25 0x13A: 2012.5 0x13B: 2018.75 0x13C: 2025 0x13D: 2031.25 0x13E: 2037.5 0x13F: 2043.75 0x140: 2050 0x141: 2056.25 0x142: 2062.5 0x143: 2068.75 0x144: 2075 0x145: 2081.25 0x146: 2087.5 0x147: 2093.75 0x148: 2100 0x149: 2106.25 0x14A: 2112.5 0x14B: 2118.75 0x14C: 2125 0x14D: 2131.25 0x14E: 2137.5 0x14F: 2143.75 0x150: 2150 0x151: 2156.25 0x152: 2162.5 0x153: 2168.75 0x154: 2175 0x155: 2181.25 0x156: 2187.5 0x157: 2193.75 0x158: 2200 0x159: 2206.25 0x15A: 2212.5 0x15B: 2218.75 0x15C: 2225 0x15D: 2231.25 0x15E: 2237.5 0x15F: 2243.75 0x160: 2250 0x161: 2256.25

BITFIELD	BITS	DESCRIPTION	DECODE
			0x162: 2262.5 0x163: 2268.75 0x164: 2275 0x165: 2281.25 0x166: 2287.5 0x167: 2293.75 0x168: 2300 0x169: 2306.25 0x16A: 2312.5 0x16B: 2318.75 0x16C: 2325 0x16D: 2331.25 0x16E: 2337.5 0x16F: 2343.75 0x170: 2350 0x171: 2356.25 0x172: 2362.5 0x173: 2368.75 0x174: 2375 0x175: 2381.25 0x176: 2387.5 0x177: 2393.75 0x178: 2400 0x179: 2406.25 0x17A: 2412.5 0x17B: 2418.75 0x17C: 2425 0x17D: 2431.25 0x17E: 2437.5 0x17F: 2443.75 0x180: 2450 0x181: 2456.25 0x182: 2462.5 0x183: 2468.75 0x184: 2475 0x185: 2481.25 0x186: 2487.5 0x187: 2493.75 0x188: 2500 0x189: 2506.25 0x18A: 2512.5 0x18B: 2518.75 0x18C: 2525 0x18D: 2531.25 0x18E: 2537.5 0x18F: 2543.75 0x190: 2550 0x191: 2556.25 0x192: 2562.5 0x193: 2568.75 0x194: 2575 0x195: 2581.25 0x196: 2587.5 0x197: 2593.75 0x198: 2600 0x199: 2606.25 0x19A: 2612.5 0x19B: 2618.75 0x19C: 2625

BITFIELD	BITS	DESCRIPTION	DECODE
			0x19D: 2631.25 0x19E: 2637.5 0x19F: 2643.75 0x1A0: 2650 0x1A1: 2656.25 0x1A2: 2662.5 0x1A3: 2668.75 0x1A4: 2675 0x1A5: 2681.25 0x1A6: 2687.5 0x1A7: 2693.75 0x1A8: 2700 0x1A9: 2706.25 0x1AA: 2712.5 0x1AB: 2718.75 0x1AC: 2725 0x1AD: 2731.25 0x1AE: 2737.5 0x1AF: 2743.75 0x1B0: 2750 0x1B1: 2756.25 0x1B2: 2762.5 0x1B3: 2768.75 0x1B4: 2775 0x1B5: 2781.25 0x1B6: 2787.5 0x1B7: 2793.75 0x1B8: 2800 0x1B9: 2806.25 0x1BA: 2812.5 0x1BB: 2818.75 0x1BC: 2825 0x1BD: 2831.25 0x1BE: 2837.5 0x1BF: 2843.75 0x1C0: 2850 0x1C1: 2856.25 0x1C2: 2862.5 0x1C3: 2868.75 0x1C4: 2875 0x1C5: 2881.25 0x1C6: 2887.5 0x1C7: 2893.75 0x1C8: 2900 0x1C9: 2906.25 0x1CA: 2912.5 0x1CB: 2918.75 0x1CC: 2925 0x1CD: 2931.25 0x1CE: 2937.5 0x1CF: 2943.75 0x1D0: 2950 0x1D1: 2956.25 0x1D2: 2962.5 0x1D3: 2968.75 0x1D4: 2975 0x1D5: 2981.25 0x1D6: 2987.5 0x1D7: 2993.75

BITFIELD	BITS	DESCRIPTION	DECODE
			0x1D8: 3000 0x1D9: 3006.25 0x1DA: 3012.5 0x1DB: 3018.75 0x1DC: 3025 0x1DD: 3031.25 0x1DE: 3037.5 0x1DF: 3043.75 0x1E0: 3050 0x1E1: 3056.25 0x1E2: 3062.5 0x1E3: 3068.75 0x1E4: 3075 0x1E5: 3081.25 0x1E6: 3087.5 0x1E7: 3093.75 0x1E8: 3100 0x1E9: 3106.25 0x1EA: 3112.5 0x1EB: 3118.75 0x1EC: 3125 0x1ED: 3131.25 0x1EE: 3137.5 0x1EF: 3143.75 0x1F0: 3150 0x1F1: 3156.25 0x1F2: 3162.5 0x1F3: 3168.75 0x1F4: 3175 0x1F5: 3181.25 0x1F6: 3187.5 0x1F7: 3193.75 0x1F8: 3193.75 0x1F9: 3193.75 0x1FA: 3193.75 0x1FB: 3193.75 0x1FC: 3193.75 0x1FD: 3193.75 0x1FE: 3193.75 0x1FF: 3193.75

CHG_CNFG_03 (0x19)

Charger configuration 3

BIT	7	6	5	4	3	2	1	0
Field	SYS_TRACK_DIS	B2SOVRC_DTC	TO_TIME[2:0]			TO_ITH[2:0]		
Reset	0x1	0x0	0x3			0x0		
Access Type	Write, Read	Write, Read	Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
SYS_TRACK_DIS	7	SYS Tracking Disable Control	0x0: SYS tracking is enabled. SYS is regulated to MAX of (V_{BATT} + 4%, V_{SYSMIN}). This is also valid in charge done state. 0x1: SYS tracking is disabled. SYS is regulated to $V_{CHG\_CV\_PRM}$.

BITFIELD	BITS	DESCRIPTION	DECODE
B2SOVRC_DTC	6	Battery to SYS Overcurrent Debounce Time Control While under OVRC condition, after t_{OCP} switcher (and therfore charge) is disabled.	0x0: t_{OCP} = 6ms 0x1: t_{OCP} = 100ms
TO_TIME	5:3	Top-Off Timer Setting (min)	0b000: 30sec 0b001: 10 0b010: 20 0b011: 30 0b100: 40 0b101: 50 0b110: 60 0b111: 70
TO_ITH	2:0	Top-Off Current Threshold (mA). The charger transitions from its fast-charge constant voltage mode to its top-off mode when the charger current decays to the value programmed by this register. This transition generates a CHG_I interrupt and causes the CHG_DTLS register to report top-off mode. This transition also starts the top-off time as programmed by TO_TIME. Read back value of the TO_ITH register reflects the actual top-off current programmed in the charger.	0b000: 25 0b001: 50 0b010: 75 0b011: 100 0b100: 125 0b101: 150 0b110: 150 0b111: 150

CHG_CNFG_04 (0x1A)

Charger configuration 4

BIT	7	6	5	4	3	2	1	0
Field	CHGCC_MSB	CHG_CV_PRM[6:0]						
Reset	0x0	0x00						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
CHGCC_MSB	7	Fast-Charge Current Selection (mA) Most Significant Bit	

BITFIELD	BITS	DESCRIPTION	DECODE
CHG_CV_PRM	6:0	Charge Termination Voltage Setting (V) Read back value of the CHG_CV_PRM register reflects the actual charge termination voltage programmed in the charger when JEITA_EN = 0. When JEITA_EN = 1, charge termination voltage is controlled by V_{CHGCV_COOL} and V_{CHGCV_WARM} register settings.	0x00: 8.100 0x01: 8.106 0x02: 8.112 0x03: 8.118 0x04: 8.124 0x05: 8.130 0x06: 8.136 0x07: 8.142 0x08: 8.148 0x09: 8.154 0x0A: 8.160 0x0B: 8.166 0x0C: 8.172 0x0D: 8.178 0x0E: 8.184 0x0F: 8.190 0x10: 8.196 0x11: 8.202 0x12: 8.208 0x13: 8.214 0x14: 8.220 0x15: 8.226 0x16: 8.232 0x17: 8.238 0x18: 8.244 0x19: 8.250 0x1A: 8.256 0x1B: 8.262 0x1C: 8.268 0x1D: 8.274 0x1E: 8.280 0x1F: 8.286 0x20: 8.292 0x21: 8.298 0x22: 8.304 0x23: 8.310 0x24: 8.316 0x25: 8.322 0x26: 8.328 0x27: 8.334 0x28: 8.340 0x29: 8.346 0x2A: 8.352 0x2B: 8.358 0x2C: 8.364 0x2D: 8.370 0x2E: 8.376 0x2F: 8.382 0x30: 8.388 0x31: 8.394 0x32: 8.400 0x33: 8.406 0x34: 8.412 0x35: 8.418 0x36: 8.424 0x37: 8.430 0x38: 8.436 0x39: 8.442 0x3A: 8.448

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: 8.454 0x3C: 8.460 0x3D: 8.466 0x3E: 8.472 0x3F: 8.478 0x40: 8.484 0x41: 8.490 0x42: 8.496 0x43: 8.502 0x44: 8.508 0x45: 8.514 0x46: 8.520 0x47: 8.526 0x48: 8.532 0x49: 8.538 0x4A: 8.544 0x4B: 8.550 0x4C: 8.556 0x4D: 8.562 0x4E: 8.568 0x4F: 8.574 0x50: 8.580 0x51: 8.586 0x52: 8.592 0x53: 8.598 0x54: 8.604 0x55: 8.610 0x56: 8.616 0x57: 8.622 0x58: 8.628 0x59: 8.634 0x5A: 8.640 0x5B: 8.646 0x5C: 8.652 0x5D: 8.658 0x5E: 8.664 0x5F: 8.670 0x60: 8.676 0x61: 8.682 0x62: 8.688 0x63: 8.694 0x64: 8.700 0x65: 8.706 0x66: 8.712 0x67: 8.718 0x68: 8.724 0x69: 8.730 0x6A: 8.736 0x6B: 8.742 0x6C: 8.748 0x6D: 8.754 0x6E: 8.760 0x6F: 8.766 0x70: 8.772 0x71: 8.778 0x72: 8.784 0x73: 8.790 0x74: 8.796 0x75: 8.802

BITFIELD	BITS	DESCRIPTION	DECODE
			0x76: 8.808 0x77: 8.814 0x78: 8.820 0x79: 8.826 0x7A: 8.832 0x7B: 8.838 0x7C: 8.844 0x7D: 8.850 0x7E: 8.856 0x7F: 8.862

CHG_CNFG_05 (0x1B)

Charger configuration 5

BIT	7	6	5	4	3	2	1	0
Field	CHGR_CV_OFFSET[1:0]		ITRICKLE[1:0]		B2SOVRC[3:0]			
Reset	0x0		0x0		0x4			
Access Type	Write, Read		Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CHGR_CV_OFFSET	7:6	CHG_CV_PRM Offset Control (Positive)	0x0: No offset 0x1: +24mV 0x2: +36mV 0x3: +42mV
ITRICKLE	5:4	Trickle Charge Current Selection (mA)	0b00: 125 0b01: 250 0b10: 375 0b11: 500
B2SOVRC	3:0	BATT to SYS Overcurrent Threshold (A)	0x00: Disable 0x01: 3.000 0x02: 3.500 0x03: 4.000 0x04: 4.500 0x05: 5.000 0x06: 5.500 0x07: 6.000 0x08: 6.500 0x09: 7.000 0x0A: 7.500 0x0B: 8.000 0x0C: 8.500 0x0D: 9.000 0x0E: 9.500 0x0F: 10.000

CHG_CNFG_06 (0x1C)

Charger configuration 6

BIT	7	6	5	4	3	2	1	0
Field	CHGCC_WR_EN	RESERVED[1:0]		SPR	CHGPROT[1:0]		WDTCLR[1:0]	
Reset	0x0	0x0		0x0	0x0		0x0	
Access Type	Write 1 to Toggle, Read	Write, Read		Write, Read	Write, Read		Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
CHGCC_WR_EN	7	Fast-Charge Current Write Command. When set to "1" CHGCC_MSB/CHGCC[7:0] registers are loaded into design. Auto clear bit.	
RESERVED	6:5	Reserved	Default value is 0x0. Do not change.
SPR	4	Spare Bit	
CHGPROT	3:2	Charger Settings Protection Bit. Writing "11" to these bits unlocks the write capability for the registers which are "Protected with CHGPROT". Writing any value besides "11" locks the protected registers.	0b00: Write capability locked. 0b01: Write capability locked. 0b10: Write capability locked. 0b11: Write capability unlocked.
WDTCLR	1:0	Watchdog Timer Clear Bit. Writing "01" to these bits clears the watchdog timer when the watchdog timer is enabled.	0b00: The watchdog timer is not cleared. 0b01: The watchdog timer is cleared. 0b10: The watchdog timer is not cleared. 0b11: The watchdog timer is not cleared.

CHG_CNFG_07 (0x1D)

Charger configuration 7

BIT	7	6	5	4	3	2	1	0
Field	JEITA_EN	REGTEMP[3:0]				VCHGCV_COOL	ICHGCC_COOL	FSHIP_MODE
Reset	0x0	0x6				0x0	0x1	0x0
Access Type	Write, Read	Write, Read				Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
JEITA_EN	7	JEITA Enable	0b0: JEITA disabled. Fast-charge current and charge termination voltage do not change based on thermistor temperature. 0b1: JEITA enabled. Fast-charge current and charge termination voltage change based on thermistor temperature.
REGTEMP	6:3	Junction Temperature Thermal Regulation (ºC). The charger's target current limit starts to foldback and the TREG bit is set if the junction temperature is greater than the REGTEMP setpoint.	0x0: 85 0x1: 90 0x2: 95 0x3: 100 0x4: 105 0x5: 110 0x6: 115 0x7: 120 0x8: 125 0x9: 130

BITFIELD	BITS	DESCRIPTION	DECODE
VCHGCV_COOL	2	JEITA controlled battery termination voltage when thermistor temperature is between T_{COLD} and T_{COOL}.	0b0: Battery termination voltage is set by CHG_CV_PRM. 0b1: Battery termination voltage is set by (CHG_CV_PRM - 180mV/cell).
ICHGCC_COOL	1	JEITA controlled battery fast-charge current when thermistor temperature is between T_{COLD} and T_{COOL}.	0b0: Battery fast-charge current is set by CHGCC. 0b1: Battery fast-charge current is reduced to 50% of CHGCC.
FSHIP_MODE	0	Factory Ship Mode Enable	0b0: Disable factory ship mode. 0b1: Enable factory ship mode.

CHG_CNFG_08 (0x1E)

Charger configuration 8

BIT	7	6	5	4	3	2	1	0
Field	RESERVED	CHGIN_ILIM[6:0]						
Reset	0x1	0x15						
Access Type	Write, Read	Write, Read						

BITFIELD	BITS	DESCRIPTION	DECODE
RESERVED	7	Reserved	Default value is 0x1. Do not change.

BITFIELD	BITS	DESCRIPTION	DECODE
CHGIN_ILIM	6:0	CHGIN Input Current Limit (mA). Read back value of the CHGIN_ILIM register reflects the actual input current limit programmed in the charger.	0x00: 50 0x01: 50 0x02: 50 0x03: 50 0x04: 75 0x05: 100 0x06: 125 0x07: 150 0x08: 175 0x09: 200 0x0A: 225 0x0B: 250 0x0C: 275 0x0D: 300 0x0E: 325 0x0F: 350 0x10: 375 0x11: 400 0x12: 425 0x13: 450 0x14: 475 0x15: 500 0x16: 525 0x17: 550 0x18: 575 0x19: 600 0x1A: 625 0x1B: 650 0x1C: 675 0x1D: 700 0x1E: 725 0x1F: 750 0x20: 775 0x21: 800 0x22: 825 0x23: 850 0x24: 875 0x25: 900 0x26: 925 0x27: 950 0x28: 975 0x29: 1000 0x2A: 1025 0x2B: 1050 0x2C: 1075 0x2D: 1100 0x2E: 1125 0x2F: 1150 0x30: 1175 0x31: 1200 0x32: 1225 0x33: 1250 0x34: 1275 0x35: 1300 0x36: 1325 0x37: 1350 0x38: 1375 0x39: 1400 0x3A: 1425

BITFIELD	BITS	DESCRIPTION	DECODE
			0x3B: 1450 0x3C: 1475 0x3D: 1500 0x3E: 1525 0x3F: 1550 0x40: 1575 0x41: 1600 0x42: 1625 0x43: 1650 0x44: 1675 0x45: 1700 0x46: 1725 0x47: 1750 0x48: 1775 0x49: 1800 0x4A: 1825 0x4B: 1850 0x4C: 1875 0x4D: 1900 0x4E: 1925 0x4F: 1950 0x50: 1975 0x51: 2000 0x52: 2025 0x53: 2050 0x54: 2075 0x55: 2100 0x56: 2125 0x57: 2150 0x58: 2175 0x59: 2200 0x5A: 2225 0x5B: 2250 0x5C: 2275 0x5D: 2300 0x5E: 2325 0x5F: 2350 0x60: 2375 0x61: 2400 0x62: 2425 0x63: 2450 0x64: 2475 0x65: 2500 0x66: 2525 0x67: 2550 0x68: 2575 0x69: 2600 0x6A: 2625 0x6B: 2650 0x6C: 2675 0x6D: 2700 0x6E: 2725 0x6F: 2750 0x70: 2775 0x71: 2800 0x72: 2825 0x73: 2850 0x74: 2875 0x75: 2900

BITFIELD	BITS	DESCRIPTION	DECODE
			0x76: 2925 0x77: 2950 0x78: 2975 0x79: 3000 0x7A: 3025 0x7B: 3050 0x7C: 3075 0x7D: 3100 0x7E: 3125 0x7F: 3150

CHG_CNFG_09 (0x1F)

Charger configuration 9

BIT	7	6	5	4	3	2	1	0
Field	INLIM_CLK[1:0]		OTG_ILIM[2:0]			MINVSYS[2:0]		
Reset	0x2		0x3			0x3		
Access Type	Write, Read		Write, Read			Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
INLIM_CLK	7:6	Input current limit soft-start period (µsec) between consecutive increments of 25mA.	0b00: 8 0b01: 256 0b10: 1024 0b11: 4096
OTG_ILIM	5:3	OTG Mode Current Limit Setting (mA)	0x0: 500 0x1: 900 0x2: 1200 0x3: 1500 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved
MINVSYS	2:0	Minimum System Regulation Voltage (V)	0b000: 5.535 0b001: 5.740 0b010: 5.945 0b011: 6.150 0b100: 6.355 0b101: 6.560 0b110: 6.765 0b111: 6.970

CHG_CNFG_10 (0x20)

Charger configuration 10

BIT	7	6	5	4	3	2	1	0
Field	CHGCC_OFFSET[1:0]		VCHGIN_REG[4:0]					DISKIP
Reset	0x0		0x00					0x0
Access Type	Write, Read		Write, Read					Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
CHGCC_OFFSET	7:6	CHGCC Offset Control (Positive)	0x0: No offset 0x1: +62.5mA 0x2: +125mA 0x3: +250mA
VCHGIN_REG	5:1	CHGIN Voltage Regulation Threshold (V)	0x00: 4.025 0x01: 4.200 0x02: 4.375 0x03: 4.550 0x04: 4.725 0x05: 4.900 0x06: 5.425 0x07: 5.950 0x08: 6.475 0x09: 7.000 0x0A: 7.525 0x0B: 8.050 0x0C: 8.575 0x0D: 9.100 0x0E: 9.625 0x0F: 10.150 0x10: 10.675 0x11: 10.950 0x12: 11.550 0x13: 12.150 0x14: 12.750 0x15: 13.350 0x16: 13.950 0x17: 14.550 0x18: 15.150 0x19: 15.750 0x1A: 16.350 0x1B: 16.950 0x1C: 17.550 0x1D: 18.150 0x1E: 18.750 0x1F: 19.050
DISKIP	0	Charger Skip Mode Disable	0b0: Auto skip mode 0b1: Disable skip mode

Applications Information

Inductor Selection

Buck-boost allows a range of inductance for different combinations of switching frequency and maximum nominal CHGIN voltage. See Table 10 for recommendations. The lower the inductor DCR is, the higher the buck-boost efficiency is. The user needs to weigh the trade-offs between inductor size and DCR value and choose a suitable inductor for the buck-boost. See Table 11 for inductor recommendations.

Table 10. Recommended Inductance for Combinations of Switching Frequency and Maximum Nominal CHGIN Voltage

SWITCHING FREQUENCY (kHz)	MAXIMUM NOMINAL CHGIN VOLTAGE (V)	RECOMMENDED NOMINAL INDUCTANCE (µH)
600	15 or lower	2.2, 3.3
	Higher than 15	3.3
1200	15 or lower	1.0, 1.5, 2.2, 3.3
	Higher than 15	1.5, 2.2, 3.3

Table 11. Suggested Inductors

MFGR.	SERIES	NOMINAL INDUCTANCE (µH)	TYPICAL DC RESISTANCE (mΩ)	CURRENT RATING (A) -30% (ΔL/L)	CURRENT RATING (A) ΔT = +40°C RISE	DIMENSIONS L x W x H (mm)
TDK	VLS3012HBX-1R0M	1.0	39.0	6.11	5.13	3.0 x 3.0 x 1.2
Coilcraft	XAL4020-152ME	1.5	21.5	7.1	7.5	4.0 x 4.0 x 2.1
Coilcraft	XAL4020-222ME	2.2	35.2	5.6	5.5	4.0 x 4.0 x 2.1
Coilcraft	XAL4030-332ME	3.3	26.0	5.5	6.6	4.0 x 4.0 x 3.1

CHGIN Capacitor Selection

The CHGIN capacitor, C_{CHGIN}, reduces the current peaks drawn from the input power source and reduces switching noise in the device. In OTG mode, it also reduces the output voltage ripple and ensures regulation loop stability. The impedance of C_{CHGIN} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R dielectrics are highly recommended due to their small size, low ESR, and small temperature coefficients. For most applications, 1 x 10µF (1210) or 1 x 10µF (1206) or 2 x 10µF (0805) capacitors are sufficient. See Table 12 for CHGIN capacitor recommendations.

Table 12. Suggested CHGIN Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Murata	GRM32ER7YA106KA12	10	35	X7R	1210	3.2 x 2.5 x 2.5
Murata	GRT31CR6YA106KE01	10	35	X5R	1206	3.2 x 1.6 x 1.6
Murata	GRM21BR6YA106ME43	10	35	X5R	0805	2.0 x 1.25 x 1.25

SYS Capacitor Selection

The SYS capacitor, C_{SYS}, is required to keep the output voltage ripple small and to ensure regulation loop stability. The C_{SYS} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R dielectric are highly recommended due to their small size, low ESR, and small temperature coefficients. For stable operation, buck-boost requires 22µF of minimum effective output capacitance. Considering the DC bias characteristic of ceramic capacitors,

1 x 47µF (1210) or 2 x 47µF (1206) or 4 x 22µF (0805) capacitors are recommended. See Table 13 for SYS capacitor recommendations.

Table 13. Suggested SYS Capacitors

MFGR.	SERIES	NOMINAL CAPACITANCE (µF)	RATED VOLTAGE (V)	TEMPERATURE CHARACTERISTICS	CASE SIZE (in)	DIMENSIONS L x W x H (mm)
Taiyo Yuden	EMK325ABJ476MM8P	47	16	X5R	1210	3.2 x 2.5 x 2.5
Murata	GRM31CR61C476ME44	47	16	X5R	1206	3.2 x 1.6 x 1.6
Murata	GRM21BR61C226ME44	22	16	X5R	0805	2.0 x 1.25 x 1.25

Battery Insertion Protection

When the battery hot inserts into the MAX77962, it creates high inrush current flowing through the body diode of Q_{BAT} FET. The inrush current peaks at tens of amperes and lasts for less than a few hundreds of microseconds. Such current can possibly damage the Q_{BAT} FET. For IC protection, the following battery insertion protection is required on the board:

- Include an external 3A Schottky diode from BATT to SYS. The Schottky diode has low forward voltage drop when conducting high current in the forward direction. It diverts the inrush current from BATT to SYS at battery insertion. The inrush current flowing through the Q_{BAT} FET is greatly reduced and therefore the IC is protected. See Figure 14.

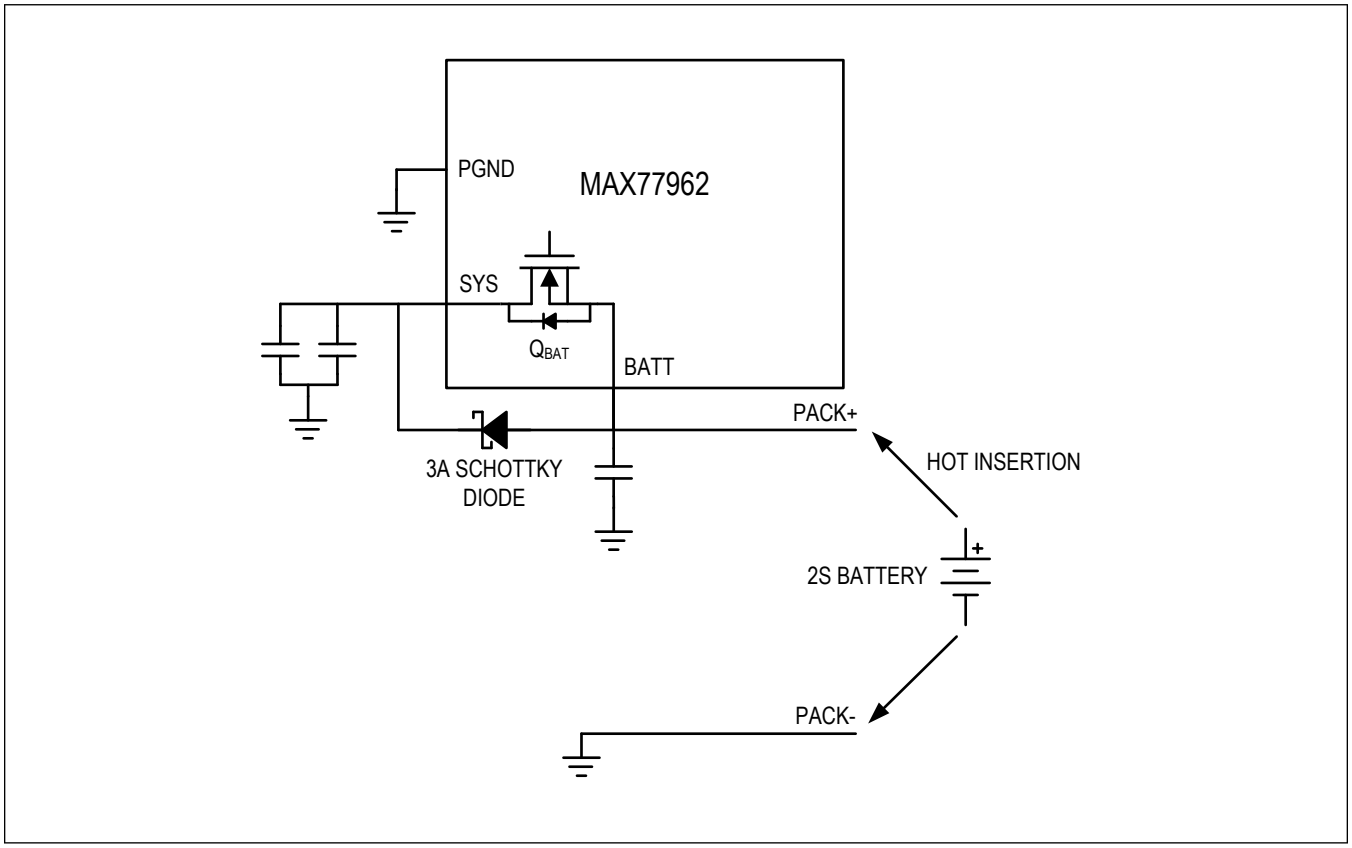


Figure 14. Battery Insertion Protection

PCB Layout Guidelines

Careful circuit board layout is critical to achieve low switching power losses and clean, stable operation. Figure 15 shows a PCB layout example.

When designing the PCB, follow these guidelines:

1. Place the CHGIN capacitor (C_{CHGIN}) and SYS capacitors (C_{SYS}) immediately next to the CHGIN pin and SYS pin of the IC, respectively. Since the IC operates at a high switching frequency, this placement is critical for minimizing parasitic inductance within the input and output current loops which can cause high voltage spikes and can damage the internal switching MOSFETs.
2. Place the inductor next to the LX pins and make the traces between the LX pins and the inductor short and wide to minimize PCB trace impedance. Excessive PCB impedance reduces converter efficiency. When routing LX traces on a separate layer, make sure to include enough vias to minimize trace impedance. Routing LX traces on multiple layers is recommended to further reduce trace impedance. Furthermore, do not make LX traces take up an excessive amount of area. The voltage on this node switches very quickly and additional area creates more radiated emissions.
3. Route LX nodes to their corresponding bootstrap capacitors (C_{BST}) as short as possible. Prioritize C_{BST} placement to reduce trace length to the IC.
4. Route CSINP and CSINN traces as symmetrical as possible. Having the same trace parasitics improves accuracy of the differential CHGIN current sensing.
5. Place the PVL capacitor (C_{PVL}) immediately next to the PVL pin. Proximity to the IC provides a stable supply for the internal circuitry.
6. Place the BATT capacitor (C_{BATT}) and SYSA capacitor (C_{SYSA}) immediately next to the BATT pin and SYSA pin of the IC, respectively.
7. Connect BATSP and BATSN as close as possible to the battery connector. This optimizes remote sense of the battery voltage.
8. Keep the power traces and load connections short and wide. This is essential for high converter efficiency.
9. Do not neglect ceramic capacitor DC voltage derating. Choose capacitor values and case sizes carefully. See the SYS Capacitor Selection section and refer to *Tutorial 5527* for more information.

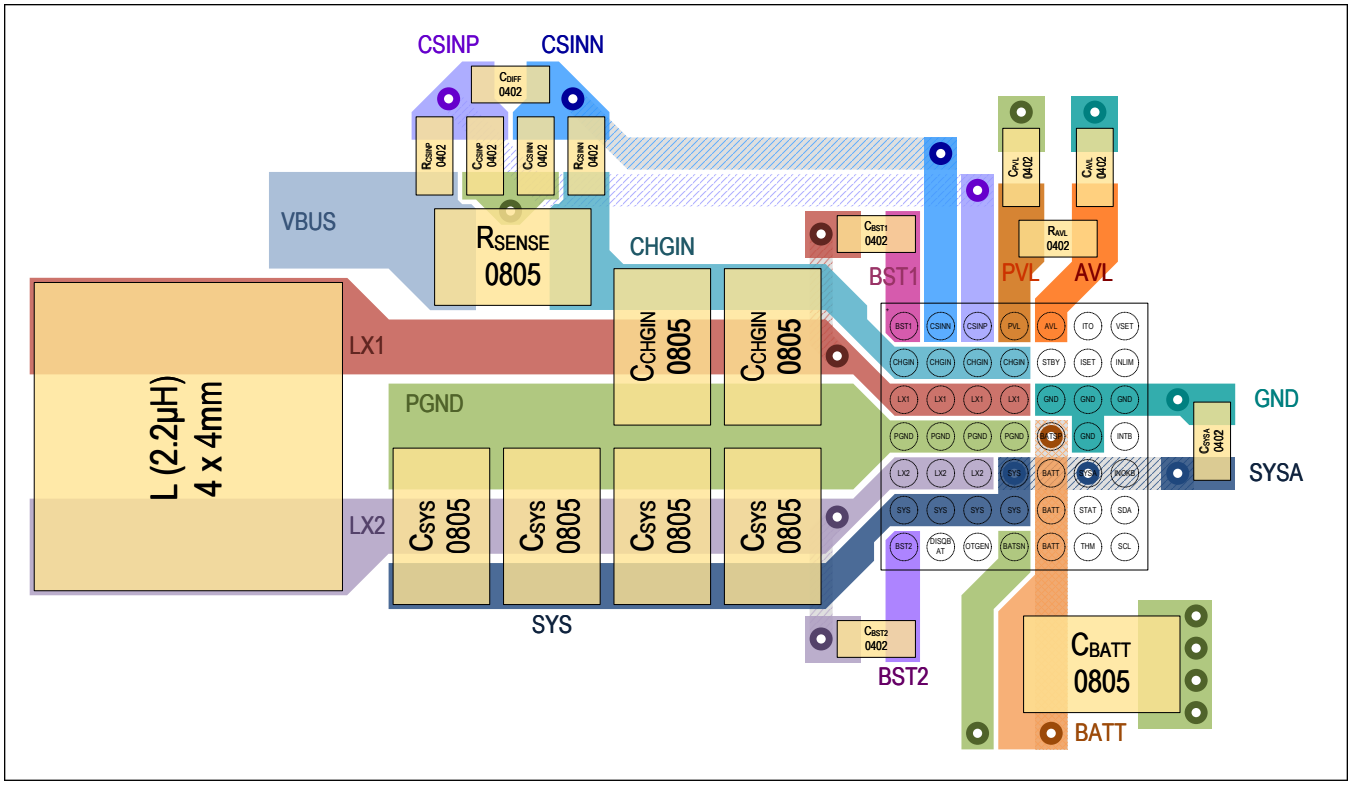
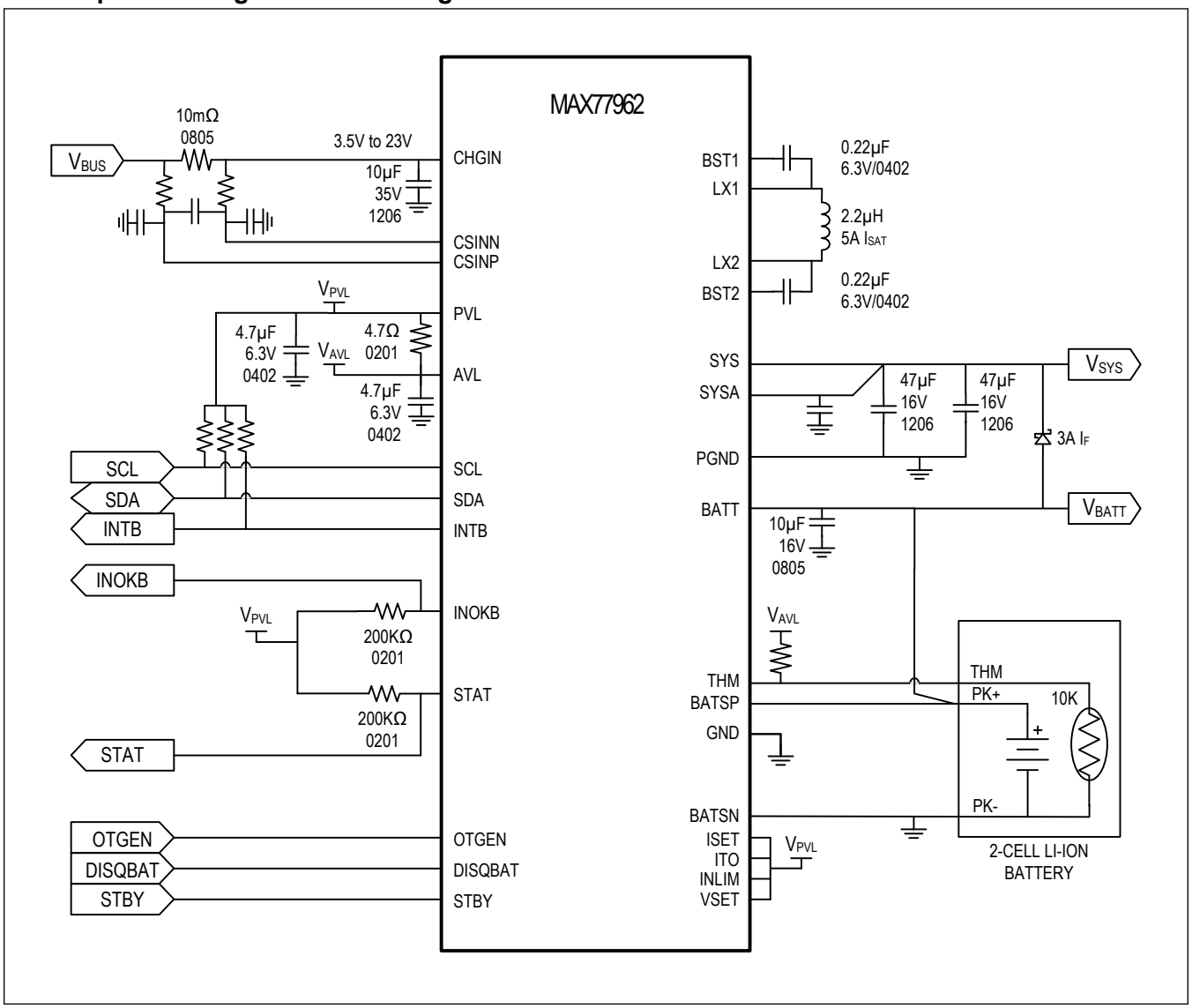


Figure 15. PCB Layout Example

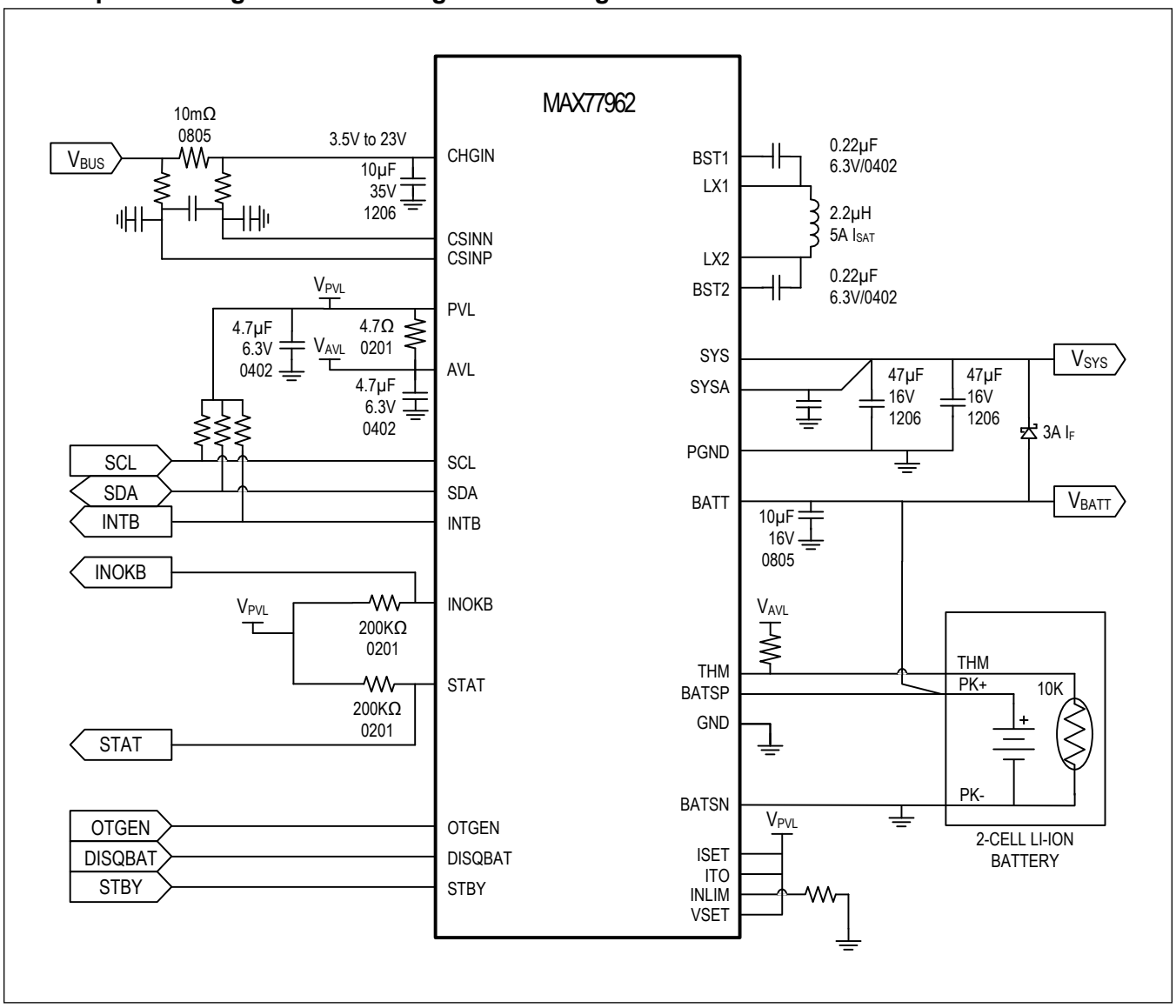
Typical Application Circuits

Wide-Input I²C Programmable Charger



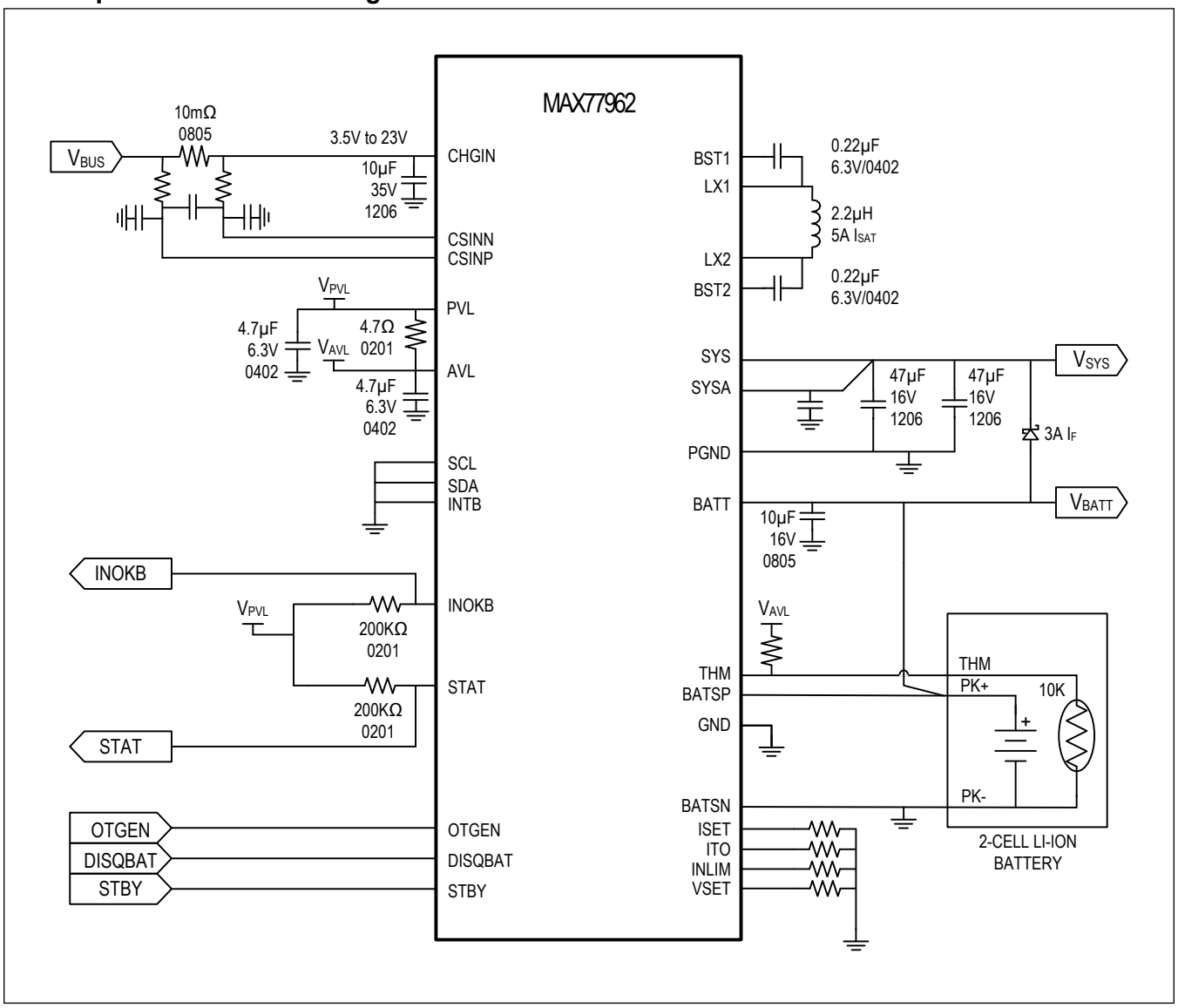
Typical Application Circuits (continued)

Wide-Input I²C Programmable Charger with Charger Disabled



Typical Application Circuits (continued)

Wide-Input Autonomous Charger



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	SWITCHING FREQUENCY	OTG MODE
MAX77962EWJ06+	-40°C to +85°C	3.458mm x 3.458mm 49-Bump WLP	600kHz	Supported
MAX77962EWJ06+T	-40°C to +85°C	3.458mm x 3.458mm 49-Bump WLP	600kHz	Supported
MAX77962EWJ12+	-40°C to +85°C	3.458mm x 3.458mm 49-Bump WLP	1.2MHz	Not Supported
MAX77962EWJ12+T	-40°C to +85°C	3.458mm x 3.458mm 49-Bump WLP	1.2MHz	Not Supported

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/20	Initial release	—
1	7/21	Updated *Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics table, Bump Descriptions, Thermistor Input (THM), Disable Thermistor Monitoring, Fast-Charge Current Setting Input (ISET), SYS Regulation Voltage, Battery Differential Voltage Sense (BATSP, BATSN)*, and *Register Details* tables, added *Applications Information* section, updated *Typical Application Circuits* section	1, 8–19, 22–24, 27, 37, 50, 73, 78, 80–84
2	5/24	Updated *Typical OpeAddedrating Characteristics*, *Disable Thermistor Monitoring*, *Figure 2*, *Thermal Shutdown State*, *Thermal Shutdown*, *Battery Differential Voltage Sense (BATSP, BATSN)*, *Reverse Buck Mode (OTG)*, *V_{SYS} Undervoltage Lockout ($V_{SYSUVLO}$)*, CHGIN Capacitor Selection, Typical Application Circuits, Ordering Information, and Register tables: *SWRST (0x2)*, *CHG_CNFG_06 (0x1C)*, *CHG_CNFG_08 (0x1E)*. Added *Register Types and Reset Conditions*, *Charger Register Write Protection*, PCB Layout Guidelines Sections.	18, 23, 31, 35, 37, 38, 40, 41, 52, 76, 77, 82, 84, 86-89.

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