MAX77863

Complete System PMIC, Featuring 13 Regulators, 8 GPIOs, RTC, and Flexible Power Sequencing for Multicore Applications

General Description

The MAX77863 is a complete power management IC (PMIC) for mobile devices using multicore application processors.

It is available in a wafter-level package (WLP) to be used in space-constrained applications.

The IC offers a total of 13 regulators. Two regulators have differential remote sensing and are rated for both continuous and peak output current.

Numerous factory-programmable options allow the IC to be tailored for many applications. Contact the factory for more information about programmable options; minimum order quantities may apply.

Applications

- Netbooks
- Tablet PCs
- Personal Internet Viewer
- Digital Photo Frames
- Set-Top Boxes
- Smartphones
- GPS
- Automotive Aftermarket Accessories

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Operates from a 2.6V to 5.5V Source
- Allows for Low-Cost PCB Technology
- Includes 4 DC-to-DC Step-Down Regulators
- Includes 9 Low-Dropout Linear Regulators
- No External MOSFETs Required
- Consumes just 12μA in its Lowest-Power State
- Low-Power Modes on all Regulators Reduces Power Consumption
- LDOs are Stable with only the Point-of-Load Capacitor
- I^2C 3.0 Compatible Interface
- nIRQ Interrupt Output
- Eight GPIOs
- Real-Time Clock (RTC)
  - Backup Battery Charger
  - Timing Clock Output
- System Watchdog Timer
- I^2C Watchdog Timer
- Bidirectional Reset I/O
- Flexible Power Sequencer (FPS)
- Thermal Shutdown

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Absolute Maximum Ratings

LDO and Step-Down Output
Short-Circuit Duration ....Continuous
Continuous Power Dissipation at T_A = +70°C)
(Derate 28.6mW/°C above +70°C, Multilayer PCB)... 2.353W
Operating Ambient Temperature Range............ -40°C to +85°C
Operating Junction Temperature Range .... -40°C to +150°C
Storage Temperature Range .... -65°C to +150°C
Soldering Temperature (reflow).....................................+260°C
IN_LDO0-1, IN_LDO2, IN_LDO3-5, IN_LDO4-6, IN_LDO7-8, MBATT, MON, BBAT, INI2C, SCL, EN0, EN1, SHDN, ACOK, LID, GPIO_INA to GND..-0.3V to +6.0V
GPIO_INB to GND .... -0.3V to (V_{MBATT} + 0.3V)
OUT_LDO0, OUT_LDO1 to GND.................-0.3V to (IN_LDO0-1 + 0.3V). Output short-circuit duration is continuous.
OUT_LDO2 to GND ....-0.3V to (IN_LDO2 + 0.3V). Output short-circuit duration is continuous.
OUT_LDO3, OUT_LDO5 to GND.................-0.3V to (IN_LDO3-5 + 0.3V). Output short-circuit duration is continuous.
OUT_LDO4, OUT_LDO6 to GND.................-0.3V to (IN_LDO4-6 + 0.3V). Output short-circuit duration is continuous.
OUT_LDO7, OUT_LDO8 to GND.................-0.3V to (IN_LDO7-8 + 0.3V). Output short-circuit duration is continuous.
AVSD to GND................-0.3V to +6.0V. AVSD and all INy_SDx must be within ±0.3V from each other.
XOUT to XGND.......-0.3V to lower of (V_{RTC} + 0.3V) and +6.0V
XIN to XGND....... -0.3V to lower of (V_{BBATT} + 0.3V) and +6.0V
D_SD3 to GND....-0.3V to lower of (V_{MBATT} + 0.3V) and +6.0V
32K_OUT0 to GND ....-0.3V to lower of (V_{GPIO_INB} + 0.3V) and +6.0V
Maximum DC current for 1 year is 20mA
Maximum AC current is 20mA/duty where the peak must be less than 200mA (Note 1)
SDA to GND ....-0.3V to +6.0V
Maximum DC current for 1 year is 25mA
Maximum AC current is 25mA/duty where the peak must be less than 200mA (Note 1)
nIRQ to GND ....Lower of (V_{INI2C} + 0.3V) and +6.0V
Maximum DC current for 1 year is 20mA
Maximum AC current is 20mA/duty where the peak must be less than 200mA (Note 1)
nRST_IO to GND ....-0.3V to +6.0V
Maximum DC current for 1 year is 20mA
Maximum AC current is 20mA/duty where the peak must be less than 200mA (Note 1)
GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7 to GND ....-0.3V to +6.0V (when open-drain GPO with internal pullup disabled) -0.3V to lower of (V_{GPIO_INx} +0.3V) and +6.0V (when otherwise)
Maximum 1-year DC source current is 12mA for each GPO
Maximum 1-year total GPO source current is 100mA for GPO0-3 and 100mA for GPIO4-7
Maximum AC source current for each GPO is 12mA/duty where the peak must be less than 200mA (Note 1)
Maximum 1-year DC sink current is 20mA for each GPO
Maximum 1-year total GPO sink current is 100mA for all GPO combined
Maximum AC sink current for each GPO is 20mA/duty where the peak must be less than 200mA (Note 1)
INA_SD0 to PGA_SD0, INB_SD0 to PGB_SD0, IN_SD1 to PG_SD1, IN_SD2 to PG_SD2, IN_SD3 to PG_SD3.......................................-0.3V to +6.0V. Within ±0.3V from AVSD
RMS current must not exceed 3.0A per bump at 110°C for 10k hours out of 100k hours of operating life
PGA_SD0, PGB_SD0, PG_SD1, PG_SD2, PG_SD3 to (PGy_SDx, GND, and XGND)............................Within ±0.3V
RMS current must not exceed 3.0A per bump at 110°C for 10k hours out of 100k hours
FB_SD0, FB_SD1, FB_SD2, FB_SD3 to GND..................-0.3V to lower of (V_{AVSD} + 0.3V) and +4.5V
SNSP_SD0, SNSP_SD1, F4, SNSN_SD0, SNSN_SD1, F3 to GND..................-0.3V to lower of (V_{AVSD} + 0.3V) and +6.0V
LXA_SD0, LXB_SD0, LX_SD1, LX_SD2, LX_SD3 ...... RMS current must not exceed 3.0A per bump at 110°C for 10k hours out of 100k hours (Note 2)
GND............... Within ±0.3V from PG_SDx grounds and XGND
XGND ....Within ±0.3V from PG_SDx grounds and GND

Note 1: Maximum AC current capability is rated as some current divided by a duty cycle with a maximum peak value. For example, given an AC current capability of "20mA/duty where the peak must be less than 200mA", a pin can withstand 100mA pulses at a 20% duty cycle (20mA/20% = 100mA).

Note 2: LXx has internal clamp diodes to PG_SDx and PVx. Applications that forward bias these diodes must take care not to exceed the current limit and package power dissipation.

Package Thermal Characteristics

WLP

PACKAGE CODE	W703A4+1
Outline Number	21-100187
Land Pattern Number	Refer to Application Note 1891
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	37.43°C/W
Junction to Case (θ_{JC})	NA

Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{MBATT} = 3.6V, I_{BBATT} = 0μA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN-BATTERY POWER INPUT (MBATT)						
MBATT/AVSD Operating Voltage Range	V_{MBATT} V_{IN_SDx} V_{AVSD}	AVSD and SDx must be connected together	2.6		5.5	V
MBATT Undervoltage-Lockout Threshold	$V_{MBATTUVLO}$	V_{MBATT} falling, 200mV hysteresis		2.5		V
AVSD Undervoltage-Lockout Threshold	$V_{AVSDUVLO}$	V_{AVSD} falling, 25mV hysteresis		2.5		V
AVSD Low Threshold	V_{AVSD_LOW}	V_{AVSD} falling, 200mV hysteresis		3		V
MBATT/AVSD Overvoltage-Lockout Threshold	$V_{MBATTOVLO}$	V_{MBATT} rising, 200mV hysteresis	5.70	5.85	6.00	V
Quiescent Supply Current	I_{Q_MBATT} + I_{Q_AVSD}	All regulators off, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b00), V_{MBATT} = 3.6V, I_{BBATT} = 0μA		12	25	μA
		All regulators off, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b00), internal reference and bias circuitry active (L_B_EN = 1), V_{MBATT} = 3.6V, I_{BBATT} = 0μA		42		
AVSD Low Threshold Comparator Quiescent Supply Current		AVSD low is enabled whenever SD1 or SD2 is enabled		6.5		μA

Electrical Characteristics (continued)

(V_{MBATT} = 3.6V, I_{BBATT} = 0μA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load LDO Supply Current		Current into M_{BATT} and all LDO power inputs, V_{MBATT} = 3.6V. All LDO power inputs are 3.6V, I_{BBATT} = 0μA, LDOs set to minimum output voltage, all step-down regulators disabled, 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b00), $V_{GPIOA-IN}$ = V_{GPIOB_IN} = 0V; this does not include any current into nRST_IO or nIRQ	Normal mode, all LDOs enabled		265		μA
			Low-power mode, LDO2-LDO6 enabled (PMOS)		58		
No-Load Step-Down Supply Current		Current into M_{BATT}, AVSD, and all step-down power inputs, V_{MBATT} = 3.6V, all regulator inputs are 3.6V, I_{BBATT} = 0μA, all step-downs enabled with their minimum output voltages, all remote feedback disabled, all LDOs disabled, 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b00), V_{GPIOA_IN} = V_{GPIOB_IN} = 0V. This does not include any current into nRST_IO or nIRQ	Normal mode, all step-downs enabled		145		μA
			Low-power mode, all step-downs enabled		82.5		

Electrical Characteristics (continued)

(V_{MBATT} = 3.6V, I_{BBATT} = 0μA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
No-Load LDO and Step-Down Supply Current		Current into M_{BATT}, AVSD all step-down power inputs, and all LDO power inputs, V_{MBATT} = 3.6V, all regulator inputs are 3.6V, I_{BBATT} = 0μA, regulators set to minimum output voltage, all remote feedback disabled, 32kHz clock buffer disabled, 32kHz oscillator in low-power mode (PWR_MD_32k = 0b00), $V_{GPIOA\text{-}IN}$ = VG_{PIOB_IN} = 0V; this does not include any current into nRST_IO or nIRQ	Normal mode, all regulators enabled		375	520	μA
			Low-power mode, all regulators except LDO0/1/7/8 (NMOS)		110	165	
BACKUP-BATTERY POWER INPUT							
BBATT Current	I_{BBATT}	V_{MBATT} = 0V, PWR_MD_32k = 0b00	V_{BBATT} = 2.45V		2.0		μA
			V_{BBATT} = 3.00V		2.2	4.2	
THERMAL ALARMS AND SHUTDOWN							
Thermal Alarm 1	T_{J120}	T_J rising, 5°C hysteresis			120		°C
Thermal Alarm 2	T_{J140}	T_J rising, 5°C hysteresis			140		°C
Thermal Shutdown Temperature	T_{JSHDN}	T_J rising, 15°C hysteresis			165		°C
VOLTAGE MONITOR (MON)							
Low-Battery Hysteresis	V_{HYSL}	LBHYST[1:0] = 0b00			100		mV
		LBHYST[1:0] = 0b01			200		
		LBHYST[1:0] = 0b10			300		
		LBHYST[1:0] = 0b11			400		

Electrical Characteristics (continued)

(V_{MBATT} = 3.6V, I_{BBATT} = 0μA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Low-Battery Threshold	V_{MONL}	V_{MON} falling	LBDAC[2:0] = 0b000		2.7		V
			LBDAC[2:0] = 0b001		2.8		
			LBDAC[2:0] = 0b010		2.9		
			LBDAC[2:0] = 0b011	2.95	3.00	3.05	
			LBDAC[2:0] = 0b100		3.1		
			LBDAC[2:0] = 0b101		3.2		
			LBDAC[2:0] = 0b110		3.3		
			LBDAC[2:0] = 0b111		3.4		
MON Input Bias Current	I_{MON}	V_{MON} = 3.0V	T_A = +25°C	-125	0	+125	nA
			T_A = +85°C		0.5		
Response Time		100mV threshold overdrive			10		μs
INTERRUPT TIMING							
Interrupt Event to nIRQ-Low Time					10		ns
Interrupt Register Read to nIRQ-Deassert Time					10		ns
Thermal Shutdown Temperature	T_{JSHDN}	T_J rising, 15°C hysteresis			165		°C
BIDIRECTIONAL RESET INPUT/OUTPUT (nRST_IO)							
Reset Output Deassert Delay Time	t_{RST-O}	OTP_TRSTO[1:0] = 0b00		1.02	1.28	1.54	ms
		OTP_TRSTO[1:0] = 0b01			10.24		
		OTP_TRSTO[1:0] = 0b10			40.96		
		OTP_TRSTO[1:0] = 0b11			81.92		
Reset Input Debounce Timer	t_{DBNC}			24	30	36	ms
Minimum V_{MBATT} for nRST_IO Assertion					1		V
Output Voltage Low	V_{OL}	I_{SINK} = 4mA, RSO = 1				0.4	V
Output High Leakage Current	I_{OZH}	V_{MBATT} = 5.5V, V_{nRST_IO} = 0V and 5.5V, RSO = 0	T_A = +25°C		0.001	1	μA
			T_A = +85°C		0.01		
Input Voltage Low	V_{IL}	RSO = 0				0.4	V
Input Voltage High	V_{IH}	RSO = 0		1.4			V
Input Hysteresis	V_{HYS}	RSO = 0			0.05		V
Input Leakage Current	I_i	V_{MBATT} = 5.5V, V_{nRST_IO} = 0V and 5.5V, RSO = 0	T_A = +25°C		0.001	1	μA
			T_A = +85°C		0.01		

Electrical Characteristics (continued)

(V_{MBATT} = 3.6V, I_{BBATT} = 0µA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC							
DEDICATED ACTIVE-LOW OPEN-DRAIN OUTPUTS—nIRQ							
Output Voltage Low	V_{OL}	I_{SINK} = 4mA				0.4	V
Output High Leakage Current	I_{OZH}	V_{MBATT} = 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
DEDICATED INPUT—EN0, EN1, EN2, SHDN, ACOK, LID							
Input Voltage Low	V_{IL}					0.4	V
Input Voltage High	V_{IH}			1.4			V
Input Hysteresis	V_{HYS}				0.05		V
Internal Pullup Resistance	R_{PUEN0}	EN0, OTP_EN0AL = 1, Figure 22			10		kΩ
	R_{PUACOK}	ACOK, OTP_ACOKAL = 1, Figure 25			100		
	R_{PULID}	LID, OTP_LIDAL = 1, Figure 26			100		
	R_{PUSHDN}	SHDN, OTP_SHDNAL = 1, Figure 27			100		
Internal Pulldown Resistance	R_{PDEN0}	EN0, OTP_EN0AL = 0, Figure 22			10		kΩ
	R_{PDACOK}	ACOK, OTP_ACOKAL = 0, Figure 25			100		
	R_{PDLID}	LID, OTP_LIDAL = 0, Figure 26			100		
	R_{PDSHDN}	SHDN, OTP_SHDNAL = 0, Figure 27			100		
TIMING CLOCK OUTPUT—32K_OUT0							
Output Voltage Low	V_{OL}	I_{SINK} = 4mA, V_{GPIO_INB} = 1.7V				0.4	V
Output Voltage High	V_{OH}	I_{SOURCE} = 2mA, OTP_32K = 0, V_{GPIO_INB} = 1.7V		0.7 x $V_{GPIO-INB}$			V
Output High Leakage Current	I_{OZH}	T_A = +25°C, OTP_32K = 1, V_{GPIO_INB} = 1.7V			0.001	1	µA
GPIO INPUT—GPIO0-GPIO7							
Input Voltage Low	V_{IL}	GPIO0-3				0.5	V
		GPIO4-7				0.5	
Input Voltage High	V_{IH}	GPIO0-3		0.7 x V_{GPIO_INA}			V
		GPIO4-7		0.7 x V_{GPIO_INB}			
Input Hysteresis	V_{HYS}				0.25		V
Input Leakage Current	I_i	V_{GPIO_INA} = 5.5V, V_{GPIO_INB} = 5.5V, V_{IN} = 0V and 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		

Electrical Characteristics (continued)

(V_{MBATT} = 3.6V, I_{BBATT} = 0μA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GPIO PUSH-PULL OUTPUT—GPIO0-GPIO7						
Output Voltage Low	V_{OL}	I_{SINK} = 4mA			0.08	V
		I_{SINK} = 12mA			0.25	
Output Voltage High	V_{OH}	GPIO0-3, I_{SOURCE} = 4mA	0.7 x V_{GPIO_INA}			V
		GPIO4-7, I_{SOURCE} = 4mA	0.7 x V_{GPIO_INB}			
GPIO OPEN-DRAIN OUTPUT—GPIO0-GPIO7						
Output Voltage Low	V_{OL}	I_{SINK} = 4mA			0.08	V
		I_{SINK} = 12mA			0.25	
Output High Leakage Current	I_{OH}	V_{GPIO_INx} = 5.5V, T_A = +25°C internal pullup/pulldown disabled		0.01	1.0	μA
		V_{GPIO_INx} = 5.5V, T_A = +85°C internal pullup/pulldown disabled		0.1		
GPIO PULL RESISTANCES—GPIO0-GPIO7						
Pullup Resistance	R_{PU}	Note 5	50	100	160	kΩ
Pulldown Resistance	R_{PD}	Note 5	50	100	160	kΩ
SDA AND SCL I/O STAGES—SDA, SCL						
SCL, SDA Input High Voltage	V_{IH}		0.7 x V_{INI2C}			V
SCL, SDA Input Low Voltage	V_{IL}				0.3 x V_{INI2C}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{INI2C}		V
SCL, SDA Input Current	I_i	V_{I2CIN} = 3.6V or 0V	-10		+10	μA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V

Note 4: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 5: The min/max variation that is shown is based on process statistics. These parameters are not production tested.

Electrical Characteristics—SD0

($V_{IN\_}$ = 3.6V, V_{SD0} = 1.0V, C_{SD0} = 2 x 22µF, L0A = L0B = 1.0µH, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN REGULATOR							
Input Voltage Range	V_{AVSD} V_{INA_SD0} V_{INB_SD0}	AVSD, INA_SD0, and INB_SD0 must be connected together		2.6		5.5	V
Output Voltage Accuracy	V_{SD0}	V_{SD0} = 1.2V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-1.5	0	+1.5	%
			T_A = -40°C to +85°C	-2.5	0	+2.5	
		V_{SD0} from 0.8V to 1.4V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-2.0	0	+2.0	
			T_A = -40°C to +85°C	-3.0	0	+3.0	
		V_{SD0} from 1.0V to 1.4V, accuracy includes transient variations in line, load, and temperature during dynamic load transients from 0mA to 1.4A with a transient rate of 3.2A/µs, PWM mode or skip mode, normal-power mode	T_A = -40°C to +85°C		±5		
		Low-power mode, I_{SD0} = 0mA to 5mA, any output voltage	T_A = -5°C to +85°C	-4.0	0	+4.0	
			T_A = -40°C to +85°C	-5.0	0	+5.0	
Load Regulation	$LDREG_{SD0}$				-0.25		%/A
Line Regulation		V_{MBATT} = 2.6V to 5V			0.08		%/V
Shutdown Supply Current	I_{SHDN}				0.1		µA
Supply Quiescent Current	I_{Q_SD0}	No switching, remote output voltage sensing off			32		µA
	I_{Q_SD0}	Switching, no load, skip mode			40		
	$I_{Q\_LPM\_SD0}$	Low-power mode			10		
	$I_{Q\_SNS\_EN0}$	Additional current consumed by SD0 remote output voltage sense circuitry total in normal mode is $I_Q = I_{Q\_SD0} + I_{Q\_SNS\_EN0}$	ROVS_EN_SD0 = 1		10		
			ROVS_EN_SD0 = 0		0.1		
	$I_{Q\_PWM\_SD0}$	Switching, no load, forced PWM mode			20		mA

Electrical Characteristics—SD0 (continued)

($V_{IN\_}$ = 3.6V, V_{SD0} = 1.0V, C_{SD0} = 2 x 22µF, L0A = L0B = 1.0µH, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Range		12.5mV steps		0.6000		1.4000	V
Maximum Output Current (Note 9)	I_{MAX_SD0}	V_{AVSD_LOW} < V_{AVSD} < 5.5V			8000		mA
		2.6V < V_{IN} < V_{AVSD_LOW}			6000		
		Low-power mode			5		
Switching Frequency	f_{SW}	Normal operation		3.96	4.4	4.84	MHz
Peak Current Limit	I_{LIMPP_HIGH0}	Per phase, FPWM mode, V_{AVSD} > V_{AVSD_LOW}			4400		mA
	I_{LIMPP_LOW0}	Per phase, FPWM mode, V_{AVSD} < V_{AVSD_LOW}			3600		
Valley Current Limit	I_{LIMNV_HIGH0}	Per phase, FPWM mode, V_{AVSD} > V_{AVSD_LOW}			3600		mA
	I_{LIMNV_LOW0}	Per phase, FPWM mode, V_{AVSD} < V_{AVSD_LOW}			3600		
Negative Current Limit	I_{LIMNN0}	FPWM mode			1500		mA
PMOS On-Resistance	R_{ON_PCH0}	IN_ = 3.6V, each phase			60		mΩ
NMOS On-Resistance	R_{ON_NCH0}	IN_ = 3.6V, each phase			50		mΩ
NMOS Zero-Crossing Threshold		Skip mode			20		mA
V_{SD0} Ripple in Skip Mode (Note 8)		Skip mode, no load, C_{SD0} = 2 x 22µF			40		mV_{P-P}
		Skip mode, no load, C_{SD0} = 4 x 22µF			20		
V_{SD0} Ripple in PWM Mode		FPWM mode, ESR = 1.5mΩ, ESL = 0.2nH, C_{SD0} = 2 x 22µF			2		mV_{P-P}
LX0 Leakage Current		LX_ = PG_ or IN_	T_A = +25°C		0.1	±1	µA
			T_A = +85°C		1		
FB_SD0 Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from FB_SD0 to PG_SD0, active discharge disabled (nADE_SD0 = 1)			0.1		µA
FB_SD0 Active Discharge Resistance		Output disabled, resistance from FB_SD0 to PGx_SD0, active discharge enabled (nADE_SD0 = 0)			50		Ω
Minimum Output Capacitance for Stable Operation	C_{OSD0}	0µA < I_{OUT0} < 6000mA, MAX ESR = 20mΩ	Nominal capacitor value		44		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		30		
Output Inductor	L	MAX DCR = 100mΩ			1.0		µH

Electrical Characteristics—SD0 (continued)

($V_{IN\_}$ = 3.6V, V_{SD0} = 1.0V, C_{SD0} = 2 x 22μF, L0A = L0B = 1.0μH, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time	t_{ONSD0}	Time from the enable signal to the output starting to increase	All other regulators are off and L_B_EN = 0 (i.e., central bias off and buck bias is off)		185		μs
			At least one LDO is on or L_B_EN = 1 and all step-down are off (i.e., central bias is on and buck bias is off)		135		
			At least one other step-down regulator is on (i.e., central bias is on and buck bias is on)		22		
Turn-Off Time	t_{OFFSD0}	After the regulator is disabled; the output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active-discharge resistor			0.1		μs
Dynamic Voltage Change Ramp Rate		Note 10	SR_SD0 [1:0] = 0b01		27.5		mV/μs
			SR_SD0 [1:0] = 0b00		13.75		
			SR_SD0 [1:0] = 0b10		55		
			SR_SD0 [1:0] = 0b11 (Note 11)		100		
Soft-Start Slew Rate	dV/dt_SS_SD0	OTP_SD_SS = 1			25		mV/μs
		OTP_SD_SS = 0			14		
Maximum Remote Sense Compensation Range	V_{RSR}	Voltage drop through power and ground plane, $V_{RSR} = V_{FB\_SD0} - (V_{SNSP\_SD0} - V_{SNSN\_SD0})$			430		mV
Output POK Threshold	V_{POK_SD0}	V_{SD0} falling, 3% hysteresis, T_A = +25°C		70	75	80	%V_{SD0}
Power-OK Noise Pulse Immunity	$t_{POKNFSD0}$	V_{SD0} pulsed from 100% to 80% of regulation			8		μs

Electrical Characteristics—SD1

($V_{IN\_}$ = 3.6V, V_{SD1} = 1.0V, C_{SD1} = 22µF, L1 = 1.0µH, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN REGULATOR							
Input Voltage Range	V_{AVSD} V_{IN_SD1}	AVSD and IN_SD1 must be connected together		2.6		5.5	V
Output Voltage Accuracy	V_{SD1}	V_{SD1} = 1.2V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-1.5	0	+1.5	%
			T_A = -40°C to +85°C	-2.5	0	+2.5	
		V_{SD1} from 0.8V to 1.5V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-2.0	0	+2.0	
			T_A = -40°C to +85°C	-3.0	0	+3.0	
		V_{SD1} from 1.0V to 1.5V, accuracy includes transient variations in line, load, and temperature during dynamic load transients from 0mA to 1.4A with a transient rate of 3.2A/µs, PWM mode or skip mode, normal-power mode	T_A = -40°C to +85°C		±5		
		Low-power mode I_{SD1} = 0mA to 5mA, any output voltage	T_A = -5°C to +85°C	-4.0	0	+4.0	
			T_A = -40°C to +85°C	-5.0	0	+5.0	
Load Regulation	$LDREG_{SD1}$				-0.25		%/A
Line Regulation		V_{MBATT} = 2.6V to 5V			0.08		%/V
Shutdown Supply Current	I_{SHDN}				0.1		µA
Supply Quiescent Current	I_{Q_SD1}	No switching, remote output voltage sensing off			16		µA
	I_{Q_SD1}	Switching, no load, skip mode			20		
	$I_{Q\_LPM\_SD1}$	Low-power mode			5		
	$I_{Q\_SNS\_EN1}$	Additional current consumed by SD0 remote output voltage sense circuitry total in normal mode is $I_Q = I_{Q\_SD0} + I_{Q\_SNS\_EN0}$	ROVS_EN_ SD1 = 1		10		
			ROVS_EN_ SD1 = 0		0.1		
	$I_{Q\_PWM\_SD1}$	Switching, no load, forced PWM mode			10		mA
Output Voltage Range		12.5mV steps		0.60		1.55	V

Electrical Characteristics—SD1 (continued)

($V_{IN\_}$ = 3.6V, V_{SD1} = 1.0V, C_{SD1} = 22µF, L1 = 1.0µH, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Output Current (Note 9)	I_{MAX_SD1}	$V_{AVSD\_LOW} < V_{AVSD} < 5.5V$			3000		mA
		$2.6V < V_{IN} < V_{AVSD\_LOW}$			2500		
		Low-power mode			5		
Switching Frequency	f_{SW}	Normal operation		3.96	4.4	4.84	MHz
Peak Current Limit	I_{LIMPP_HIGH1}	FPWM mode, $V_{AVSD} > V_{AVSD\_LOW}$			3750		mA
	I_{LIMPP_LOW1}	FPWM mode, $V_{AVSD} < V_{AVSD\_LOW}$			3050		
Valley Current Limit	I_{LIMNV_HIGH1}	FPWM mode, $V_{AVSD} > V_{AVSD\_LOW}$			3150		mA
	I_{LIMNV_LOW1}	FPWM mode, $V_{AVSD} < V_{AVSD\_LOW}$			3050		
Negative Current Limit	I_{LIMNN1}	FPWM mode			775		mA
PMOS On-Resistance	R_{ON_PCH1}	IN_ = 3.6V			80		mΩ
NMOS On-Resistance	R_{ON_NCH1}	IN_ = 3.6V			60		mΩ
NMOS Zero-Crossing Threshold		Skip mode			20		mA
V_{SD1} Ripple in Skip Mode (Note 8)		Skip mode, no load, C_{SD1} = 22µF			40		mV_{P-P}
		Skip mode, no load, C_{SD1} = 44µF			20		
V_{SD1} Ripple in PWM Mode		FPWM mode, ESR = 3.0mΩ, ESL = 0.4nH, C_{SD1} = 22µF			4		
LX_SD1 Leakage Current		LX_SD1 = PG_SD1 or IN_SD1	T_A = +25°C		0.1	±1	µA
			T_A = +85°C		1		
FB_SD1 Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from FB_SD1 to PG_SD1, active discharge disabled (nADE_SD1 = 1)			0.1		µA
FB_SD1 Active Discharge Resistance		Output disabled, resistance from FB_SD1 to PGA_ SD1, active discharge enabled (nADE_SD1 = 0)			100		Ω
Minimum Output Capacitance for Stable Operation	C_{OSD1}	0µA < I_{OUT1} < 3000mA, MAX ESR = 20mΩ	Nominal capacitor value		22		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		15		
Output Inductor	L	MAX DCR = 100mΩ			1.0		µH

Electrical Characteristics—SD1 (continued)

($V_{IN\_}$ = 3.6V, V_{SD1} = 1.0V, C_{SD1} = 22µF, L1 = 1.0µH, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time	t_{ONSD1}	Time from the enable signal to the output starting to increase	All other regulators are off and L_B_EN = 0 (i.e., central bias off and buck bias is off)		185		µs
			At least one LDO is on or L_B_EN = 1 and all step-down are off (i.e., central bias is on and buck bias is off)		135		
			At least one other step-down regulator is on (i.e., central bias is on and buck bias is on)		22		
Turn-Off Time	t_{OFFSD1}	After the regulator is disabled, the output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active-discharge resistor			0.1		µs
Dynamic Voltage Change Ramp Rate		Note 10	SR_SD1 [1:0] = 0b01		27.5		mV/µs
			SR_SD1 [1:0] = 0b00		13.75		
			SR_SD1 [1:0] = 0b10		55		
			SR_SD1 [1:0] = 0b11 (Note 11)		100		
Soft-Start Slew Rate	dV/dt_SS_SD1	OTP_SD_SS = 1			25		mV/µs
		OTP_SD_SS = 0			14		
Maximum Remote Sense Compensation Range	V_{RSR}	Voltage drop through power and ground plane, $V_{RSR} = V_{FB\_SD1} - (V_{SNSP\_SD1} - V_{SNSN\_SD1})$			430		mV
Output POK Threshold	V_{POK_SD1}	V_{SD1} falling, 3% hysteresis, T_A = +25°C		71	75	79	%V_{SD1}
Power-OK Noise Pulse Immunity	$t_{POKNFSD1}$	V_{SD1} pulsed from 100% to 80% of regulation			8		µs

Electrical Characteristics—SD2

($V_{IN\_}$ = 3.6V, V_{SD2} = 1.8V, C_{SD2} = 22µF, L2 = 1.0µH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN REGULATOR							
Input Voltage Range	V_{AVSD} V_{IN_SD2}	AVSD and IN_SD2 must be connected together		2.6		5.5	V
Output Voltage Accuracy	V_{SD2}	V_{SD2} = 1.8V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-1.5	0	+1.5	%
			T_A = -40°C to +85°C	-2.5	0	+2.5	
		V_{SD2} from 1.2V to 2.8V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-2.0	0	+2.0	
			T_A = -40°C to +85°C	-3.0	0	+3.0	
		V_{SD2} from 1.2V to 2.8V, accuracy includes transient variations in line, load, and temperature during dynamic load transients from 0mA to 1.4A with a transient rate of 3.2A/µs, PWM mode or skip mode, normal-power mode	T_A = -40°C to +85°C		±5		
		Low-power mode I_{SD2} = 0mA to 5mA, any output voltage	T_A = -5°C to +85°C	-4.0	0	+4.0	
			T_A = -40°C to +85°C	-5.0	0	+5.0	
Load Regulation	$LDREG_{SD2}$				-0.25		%/A
Line Regulation		V_{MBATT} = 2.6V to 5V			0.04		%/V
Shutdown Supply Current	I_{SHDN}				0.1		µA
Supply Quiescent Current	I_{Q_SD2}	No switching, remote output voltage sensing off			16		µA
	I_{Q_SD2}	Switching, no load, skip mode			20		
	$I_{Q\_LPM\_SD2}$	Low-power mode, V_{OUT} = 1.8V			5		
	$I_{Q\_PWM\_SD2}$	Switching, no load, forced PWM mode			10		mA
Output Voltage Range		12.5mV steps		0.6000		3.3875	V
Maximum Output Current	I_{MAX_SD2}	Normal operation			2000		mA
		Low-power mode			5		
Switching Frequency	f_{SW}	Normal operation		3.96	4.4	4.84	MHz

Electrical Characteristics—SD2 (continued)

($V_{IN\_}$ = 3.6V, V_{SD2} = 1.8V, C_{SD2} = 22μF, L2 = 1.0μH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Peak Current Limit	I_{LIMPP2}	FPWM mode, T_A = +25°C		2500	3000	3600	mA
Valley Current Limit	I_{LIMNV2}	FPWM mode, T_A = +25°C		2000	2500	3000	mA
Negative Current Limit	I_{LIMNN2}	FPWM mode			620		mA
PMOS On-Resistance	R_{ON_PCH2}	IN_ = 3.6V			100		mΩ
NMOS On-Resistance	R_{ON_NCH2}	IN_ = 3.6V			75		mΩ
NMOS Zero-Crossing Threshold		Skip mode			20		mA
V_{SD2} Ripple in SKIP Mode (Note 8)		No load, C_{SD2} = 10μF			40		mV_{P-P}
		No load, C_{SD2} = 20μF			20		
V_{SD2} Ripple in PWM Mode		No load, ESR = 3.0 mΩ, ESL = 0.4 nH			2		mV_{P-P}
LX_SD2 Leakage Current		LX_SD2 = PG_ SD2 or IN_SD2	T_A = +25°C		0.1	±1	μA
			T_A = +85°C		1		
FB_SD2 Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from FB_SD2 to PG_SD2, active discharge disabled (nADE_SD2 = 1)			0.1		μA
FB_SD2 Active Discharge Resistance		Output disabled, resistance from FB_SD2 to PG_SD2, active discharge enabled (nADE_SD2 = 0)			100		Ω
Minimum Output Capacitance for Stable Operation	C_{OSD1}	0μA < I_{OUT1} < 2000mA, MAX ESR = 20mΩ	Nominal capacitor value		22		μF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		14		
Output Inductor	L	MAX DCR = 100mΩ			1.0		μH

Electrical Characteristics—SD2 (continued)

($V_{IN\_}$ = 3.6V, V_{SD2} = 1.8V, C_{SD2} = 22µF, L2 = 1.0µH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time	t_{ONSD2}	Time from the enable signal to the output starting to increase	All other regulators are off and L_B_EN = 0 (i.e., central bias off and buck bias is off)		185		µs
			At least one LDO is on or L_B_EN = 1 and all step-down are off (i.e., central bias is on and buck bias is off)		135		
			At least one other step-down regulator is on (i.e., central bias is on and buck bias is on)		22		
Turn-Off Time	t_{OFFSD0}	After the regulator is disabled, the output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active-discharge resistor			0.1		µs
Dynamic Voltage Change Ramp Rate		Note 10	SR_SD2 [1:0] = 0b01		27.5		mV/µs
			SR_SD2 [1:0] = 0b00		13.75		
			SR_SD2 [1:0] = 0b10		55		
			SR_SD2 [1:0] = 0b11 (Note 11)		100		
Soft-Start Slew Rate	dV/dt_SS_SD2	OTP_SD_SS = 1			25		mV/µs
		OTP_SD_SS = 0			14		
Output POK Threshold	V_{POK_SD2}	V_{SD2} falling, 3% hysteresis, T_A = +25°C		86	90	94	%V_{SD2}
Power-OK Noise Pulse Immunity	$t_{POKNFSD}$	V_{SD2} pulsed from 100% to 80% of regulation			8		µs

Electrical Characteristics—SD3

(V_{IN_SD3} = 3.6V, V_{SD3} = 1.5V, C_{SD3} = 22µF, L3 = 1.0µH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
STEP-DOWN REGULATOR							
Input Voltage Range	V_{AVSD} V_{IN_SD3}	AVSD and IN_SD3 must be connected together		2.6		5.5	V
Output Voltage Accuracy	V_{SD3}	V_{SD3} = 1.8V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-1.5	0	+1.5	%
			T_A = -40°C to +85°C	-2.5	0	+2.5	
		V_{SD3} from 1.2V to 2.8V, accuracy includes static variations in line and temperature, no load, PWM mode, normal-power mode	T_A = +25°C	-2.0	0	+2.0	
			T_A = -40°C to +85°C	-3.0	0	+3.0	
		V_{SD3} from 1.2V to 2.8V, accuracy includes transient variations in line, load, and temperature during dynamic load transients from 0mA to 1.4A with a transient rate of 3.2A/µs, PWM mode or skip mode, normal-power mode	T_A = -40°C to +85°C		±5		
		Low-power mode I_{SD3} = 0mA to 5mA, any output voltage	T_A = -5°C to +85°C	-4.0	0	+4.0	
			T_A = -40°C to +85°C	-5.0	0	+5.0	
Load Regulation	$LDREG_{SD3}$				-0.25		%/A
Line Regulation		V_{MBATT} = 2.6V to 5V			0.04		%/V
Shutdown Supply Current	I_{SHDN}				0.1		µA
Supply Quiescent Current	I_{Q_SD3}	No switching, remote output voltage sensing off			16		µA
	I_{Q_SD3}	Switching, no load, skip mode			20		
	$I_{Q\_LPM\_SD3}$	Low-power mode, V_{OUT} = 1.8V			5		
	$I_{Q\_PWM\_SD3}$	Switching, no load, forced PWM mode			10		mA
Output Voltage Range		12.5mV steps		0.6000		3.3875	V
Default Output Voltage		D_SD3 = GND			1.2		V
		D_SD3 = unconnected; this value is set by OTP; see the *Register Map* for more information			OTP		
		D_SD3 = MBATT			1.35		

Electrical Characteristics—SD3 (continued)

(V_{IN_SD3} = 3.6V, V_{SD3} = 1.5V, C_{SD3} = 22µF, L3 = 1.0µH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Output Current	I_{MAX_SD3}	Normal operation			2000		mA
		Low-power mode			5		
Switching Frequency	f_{SW}	Normal operation		3.96	4.4	4.84	MHz
Peak Current Limit	I_{LIMPP3}	FPWM mode, T_A = +25°C		2500	3000	3600	mA
Valley Current Limit	I_{LIMNV3}	FPWM mode, T_A = +25°C		2000	2500	3000	mA
Negative Current Limit	I_{LIMNN3}	FPWM mode			620		mA
PMOS On-Resistance	R_{ON_PCH3}	V_{IN_SD3} = 3.6V			100		mΩ
NMOS On-Resistance	R_{ON_NCH3}	V_{IN_SD3} = 3.6V			75		mΩ
NMOS Zero-Crossing Threshold		Skip mode			20		mA
V_{SD3} Ripple in SKIP Mode (Note 8)		No load, C_{SD3} = 10µF			40		mV_{P-P}
		No load, C_{SD3} = 20µF			20		
V_{SD3} Ripple in PWM Mode		No load, ESR = 3.0mΩ, ESL = 0.4nH			2		mV_{P-P}
LX_SD3 Leakage Current		LX_SD3 = PG_SD3 or IN_SD3	T_A = +25°C		0.1	±1	µA
			T_A = +85°C		1		
FB_SD3 Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from FB_SD3 to PG_SD3, active discharge disabled (nADE_SD3 = 1)			0.1		µA
FB_SD3 Active Discharge Resistance		Output disabled, resistance from FB_SD3 to PG_SD3, active discharge enabled (nADE_SD3 = 0)			100		Ω
Minimum Output Capacitance for Stable Operation	C_{OSD3}	0µA < I_{OUT3} < 2000mA, MAX ESR = 20mΩ	Nominal capacitor value		22		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		14		
Output Inductor	L	MAX DCR = 100 mΩ			1.0		µH

Electrical Characteristics—SD3 (continued)

(V_{IN_SD3} = 3.6V, V_{SD3} = 1.5V, C_{SD3} = 22µF, L3 = 1.0µH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-On Time	t_{ONSD3}	Time from the enable signal to the output starting to increase	All other regulators are off and L_B_EN = 0 (i.e., central bias off and buck bias is off)		185		µs
			At least one LDO is on or L_B_EN = 1 and all step-down are off (i.e., central bias is on and buck bias is off)		135		
			At least one other step-down regulator is on (i.e., central bias is on and buck bias is on)		22		
Turn-Off Time	t_{OFFSD0}	After the regulator is disabled, the output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active-discharge resistor			0.1		µs
Dynamic Voltage Change Ramp Rate		Note 10	SR_SD3 [1:0] = 0b01		27.5		mV/µs
			SR_SD3 [1:0] = 0b00		13.75		
			SR_SD3 [1:0] = 0b10		55		
			SR_SD3 [1:0] = 0b11 (Note 11)		100		
Soft-Start Slew Rate	dV/dt_SS_ SD3	OTP_SD_SS = 1			25		mV/µs
		OTP_SD_SS = 0			14		
Output POK Threshold	V_{POK_SD3}	V_{SD3} falling, 3% hysteresis, T_A = +25°C		86	90	94	%V_{SD3}
Power-OK Noise Pulse Immunity	$t_{POKNFSD3}$	V_{SD3} pulsed from 100% to 80% of regulation			8		µs
D_SD3 TRI-LEVEL LOGIC INPUT							
Maximum D_SD3 to Ground Resistance to Achieve the “LOW” Logic Level		The impedance from D_SD3 to ground must be less than 2kΩ to set the “LOW” state; Maxim recommends that D_SD3 be connected directly to ground to achieve the “LOW” state			2		kΩ
Maximum D_SD3 to Ground Resistance to Achieve the “UNCONNECTED” Logic Level		The impedance at D_SD3 must be larger than 200kΩ to set the “UNCONNECTED” state; Maxim recommends that D_SD3 be left unconnected (floating) to achieve the “UNCONNECTED” state			200		kΩ

Electrical Characteristics—SD3 (continued)

(V_{IN_SD3} = 3.6V, V_{SD3} = 1.5V, C_{SD3} = 22µF, L3 = 1.0µH, T_A = -40°C to 85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum D_SD3 to Ground Resistance to Achieve the "HIGH" Logic Level		The impedance from D_SD3 to MBATT must be less than 2kΩ to set the "HIGH" state; Maxim recommends that D_SD3 be connected directly to ground to achieve the "HIGH" state		2		kΩ
D_SD3 Force Time	$t_{DSD3LTCH}$	From MBATT okay until the D_SD3 detects its state; after state detection, D_SD3 becomes high-impedance		22		µs
D_SD3 Input Leakage Current		T_A = +25°C, after the force time has expired		0.01		µA

Note 6: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 7: SD0 and SD1 have remote output voltage sensing. When enabled, the remote output voltage sensing compensates for voltage drops (up to VRSR) in a PCBs power path due to parasitic resistance. As a result of this compensation, the output voltage directly at the output of SD0 and SD1 may vary up to VRSR, but the voltage at the remote sense point complies with the load regulation specifications. When the remote sensing feature is disabled, the output voltage is sensed at FB_SDx.

Note 8: Skip mode output voltage ripple decreases as the output capacitance increases. Typically a system's point-of-load capacitance contributes to the step-down regulators local output capacitance to decrease the overall skip-mode output voltage ripple.

Note 9: Maximum output current refers to the maximum current that the step-down regulator is electrically capable of delivering. Thermal and reliability limits can reduce the maximum sustainable output current and/or the operation time at maximum output current.

Note 10: During a DVS transition, the regulators output current increases by COUT x dV/dt. In the event that the load current plus the additional current imposed by the DVS transition reaches the regulator's current limit, the current limit is enforced. When the current limit is enforced, the advertised DVS transition rate (dV/dt) does not occur.

Note 11: For the 0b00, 0b01, and 0b10 settings, the device actively controls the slew rate. For the 0b11 setting, the device drives the output voltage as fast as possible and the slew rate is limited by the current limit and the output capacitance.

Electrical Characteristics—150mA PMOS

(V_{MBATT} = V_{IN} = 3.7V, C_{OUT} = 1.0μF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPERATIONAL SPECIFICATIONS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		1.7		5.5	V
Undervoltage Lockout	V_{UVLOxx}	Rising, 100mV hysteresis			1.6	1.7	V
Battery Voltage Range	V_{MBATT}	Guaranteed by main bias testing		2.45		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7V or V_{OUT} +0.3V	50mV/Step (6-bit), LDO2, LDO5, LDO6	0.8		3.95	V
			12.5mV Step (6-bit), LDO4	0.8		1.5875	
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	150			mA
			Low-power mode	5			
Minimum Output Capacitance for Stable Operation (Note 13, Note 14)	C_{OUTxx}	Normal mode	Nominal capacitor value		1.0		μF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0.7		
		Low-power mode	Nominal capacitor value		1.0		
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0.7		
BIAS							
Bias Enable Time	t_{LBIAS}	Time to enable LDO bias only; central bias is already enabled			90		μs
Bias Enable Currents	I_{QBIAS}	LDO bias enabled; L_B_EN = 1			10		μA
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM} + 0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM} + 0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage	-5		+5	
Load Regulation (Note 14)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM} + 0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM} + 0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		

Electrical Characteristics—150mA PMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, C_{OUT} = 1.0µF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

<table>
<tr><th>PARAMETER</th><th>SYMBOL</th><th colspan="3">CONDITIONS</th><th>MIN</th><th>TYP</th><th>MAX</th><th>UNITS</th></tr>
<tr><td rowspan="2">Line Regulation (Note 14)</td><td rowspan="2"></td><td>Normal mode</td><td colspan="2">V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum; I_{OUT} = 0.1mA, V_{NOM} set to any voltage</td><td></td><td>0.01</td><td></td><td rowspan="2">%/V</td></tr>
<tr><td>Low-power mode</td><td colspan="2">V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum; I_{OUT} = 0.1mA, V_{NOM} set to any voltage</td><td></td><td>0.01</td><td></td></tr>
<tr><td rowspan="3">Dropout Voltage</td><td rowspan="3">V_{DOxx}</td><td rowspan="2">Normal mode</td><td rowspan="2">I_{OUT} = I_{MAX}</td><td>V_{IN} = 3.7V</td><td></td><td>50</td><td>100</td><td rowspan="3">mV</td></tr>
<tr><td>V_{IN} = 1.7V</td><td></td><td>150</td><td>300</td></tr>
<tr><td>Low-power mode</td><td colspan="2">I_{OUT} = 5mA, V_{IN} = 3.7V</td><td></td><td>150</td><td>300</td></tr>
<tr><td>Output Current Limit</td><td>I_{LIMxx}</td><td colspan="3">V_{OUT} = 0V, percentage of I_{MAX}</td><td>110</td><td>180</td><td>250</td><td>%</td></tr>
<tr><td rowspan="5">Output Load Transient (OVCLMP_EN_Lxx = 1) (Note 14)</td><td rowspan="5"></td><td rowspan="4">Normal mode, V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 1% to 100% to 1% of I_{MAX}, V_{NOM} set to any voltage, t_R = t_F = 1µs, C_{OUT} = 1.0µF</td><td colspan="2">COMP_Lx = 0b00, C_{ESR} = 50mΩ, C_{ESL} = 5nH</td><td></td><td>55</td><td></td><td rowspan="5">mV</td></tr>
<tr><td colspan="2">COMP_Lx = 0b01, C_{ESR} = 150mΩ, C_{ESL} = 10nH</td><td></td><td>66</td><td></td></tr>
<tr><td colspan="2">COMP_Lx = 0b10, C_{ESR} = 500mΩ, C_{ESL} = 35nH</td><td></td><td>99</td><td></td></tr>
<tr><td colspan="2">COMP_Lx = 0b11, C_{ESR} = 1000mΩ, C_{ESL} = 50nH</td><td></td><td>125</td><td></td></tr>
<tr><td colspan="3">Low-power mode, V_{IN} = V_{NOM} + 0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage; t_R = t_F = 1µs, C_{OUT} = 1.0µF</td><td></td><td>25</td><td></td></tr>
<tr><td rowspan="2">Output Line Transient (Note 14)</td><td rowspan="2"></td><td colspan="3">Normal mode, V_{IN} = V_{NOM} + 0.3V to V_{NOM} + 0.8V to V_{NOM} + 0.3V with 1.7V absolute minimum; t_R = t_F = 1µs, I_{OUT} = I_{MAX}, V_{NOM} set to any voltage</td><td></td><td>5</td><td></td><td rowspan="2">mV</td></tr>
<tr><td colspan="3">Low-power mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V with 1.7V absolute minimum. t_R = t_F = 1µs, I_{OUT} = 5mA, V_{NOM} set to any voltage</td><td></td><td>5</td><td></td></tr>
</table>

Electrical Characteristics—150mA PMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, C_{OUT} = 1.0µF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Rejection	PSRRxx	Rejection from V_{IN} to V_{OUT} I_{OUT} = 10% of I_{MAX}	V_{INDC} = V_{NOM} +1V V_{INAC} = 50mV	f = 1kHz		79		dB
				f = 10kHz		68		
				f = 100kHz		50		
				f = 1000kHz		39		
				f = 4450kHz		35		
			V_{INDC} = V_{NOM} +0.5V V_{INAC} = 50mV	f = 1kHz		81		
				f = 10kHz		71		
				f = 100kHz		52		
				f = 1000kHz		45		
				f = 4450kHz		39		
			V_{INDC} = V_{NOM} +0.1V V_{INAC} = 10mV	f = 1kHz		52		
				f = 10kHz		43		
				f = 100kHz		38		
				f = 1000kHz		33		
				f = 4450kHz		28		
		Low-power mode, I_{OUT} = 1mA, f = 1kHz, rejection from V_{IN} to V_{OUT}				50		
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 0.8V			45		µV_{RMS}
			V_{OUT} = 1.8V			45		
			V_{OUT} = 3.7V			60		
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, Note 17	Lxx_SS = 0			100		mV/µs
			Lxx_SS = 1			5		
Output Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from OUT_LDOx to GND, active discharge disabled (Lxx_ADE = 0)				0.1		µA
Active-Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (Lxx_ADE = 1)				65		Ω
OVERVOLTAGE CLAMP								
Clamp Active Regulation Voltage		Clamp active (OVCLMP_EN_Lxx = 1), LDO output sinking 0.1mA				V_{NOM}		V
Clamp Disabled Overvoltage Sink Current		V_{OUTxx} = V_{NOM} × 110%				2.2		µA

Electrical Characteristics—150mA PMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, C_{OUT} = 1.0µF, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING							
Turn-On Time	t_{LON}	Time from LDO enable command received to the output starting to slew, LDO bias enabled	Lxx_SS = 0		10		µs
			Lxx_SS = 1		60		
Turn-Off Time		After LDO is disabled, the LDO output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active discharge resistor.			0.1		µs
Transition Time from Low-Power Mode to Normal Mode					50		µs
THERMAL SHUTDOWN							
Thermal Shutdown		Output Disabled or Enabled	T_J Rising		165		°C
			T_J Falling		150		
POWER-OK							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} Rising		92	95	%
			V_{OUT} Falling	84	87		
Power-OK Noise Pulse Immunity	$t_{POKNFLDO}$	V_{OUT} pulsed from 100% to 80% of regulation			25		µs

Electrical Characteristics—300mA PMOS

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPERATIONAL SPECIFICATIONS							
Input Voltage Range	V_{IN_LDOx}	Guaranteed by output accuracy		1.7		5.5	V
Undervoltage Lockout	V_{UVLOxx}	Rising, 100mV hysteresis			1.6	1.7	V
Battery Voltage Range	V_{MBATT}	Guaranteed by main bias testing		2.45		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7V or V_{OUT} +0.3V.	50mV/Step (6-bit), LDO3	0.8		3.95	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	300			mA
			Low-power mode	5			
Minimum Output Capacitance for Stable Operation (Note 13, Note 14)	C_{OUTxx}	Normal mode	Nominal capacitor value		2.2		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		1.5		
		Low-power mode	Nominal capacitor value		2.2		
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		1.5		
BIAS							
Bias Enable Time	t_{LBIAS}	Time to enable LDO bias only; central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS}	LDO bias enabled; L_B_EN = 1			10		µA
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage	-5		+5	
Load Regulation (Note 14)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM} +0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM} +0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		

Electrical Characteristics—300mA PMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Line Regulation (Note 14)		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum; I_{OUT} = 0.1mA, V_{NOM} set to any voltage			0.01		%/V
		Low-power mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum; I_{OUT} = 0.1mA, V_{NOM} set to any voltage			0.01		
Dropout Voltage	V_{DOxx}	Normal mode	I_{OUT} = I_{MAX}	V_{IN} = 3.7V		50	100	mV
				V_{IN} = 1.7V		150	450	
		Low-power mode	I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	OUT = 0V			110	180	250	%
Output Load Transient (OVCLMP_EN_Lxx = 1) (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 1% to 100% to 1% of I_{MAX}, V_{NOM} set to any voltage, t_R = t_F = 1µs, C_{OUT} = 2.2µF	COMP_Lx = 0b00, C_{ESR} = 50mΩ, C_{ESL} = 5nH			55		mV
			COMP_Lx = 0b01, C_{ESR} = 150mΩ, C_{ESL} = 10nH			66		
			COMP_Lx = 0b10, C_{ESR} = 500mΩ, C_{ESL} = 35nH			99		
			COMP_Lx = 0b11, C_{ESR} = 1000mΩ, C_{ESL} = 50nH			125		
		Low-power mode, V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V absolute minimum. I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage; t_R = t_F = 1µs, C_{OUT} = 2.2µF				25		
Output Line Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V with 1.7V absolute minimum; t_R = t_F = 1µs, I_{OUT} = I_{MAX}, V_{NOM} set to any voltage				5		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V with 1.7V absolute minimum; t_R = t_F = 1µs, I_{OUT} = 5mA, V_{NOM} set to any voltage				5		

Electrical Characteristics—300mA PMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Rejection	PSRRxx	Rejection from V_{IN} to V_{OUT} I_{OUT} = 10% of I_{MAX}	V_{INDC} = V_{NOM}+1V V_{INAC} = 50mV	f = 1kHz		79		dB
				f = 10kHz		68		
				f = 100kHz		50		
				f = 1000kHz		39		
				f = 4450kHz		35		
			V_{INDC} = V_{NOM} +0.5V V_{INAC} = 50mV	f = 1kHz		81		
				f = 10kHz		71		
				f = 100kHz		52		
				f = 1000kHz		45		
				f = 4450kHz		39		
			V_{INDC} = V_{NOM} +0.1V V_{INAC} = 10mV	f = 1kHz		52		
				f = 10kHz		43		
				f = 100kHz		38		
				f = 1000kHz		33		
				f = 4450kHz		28		
		Low-power mode, I_{OUT} = 1mA, f = 1kHz, rejection from V_{IN} to V_{OUT}				50		
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 0.8V			45		μV_{RMS}
			V_{OUT} = 1.8V			45		
			V_{OUT} = 3.7V			60		
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, Note 17	Lxx_SS = 0			100		mV/µs
			Lxx_SS = 1			5		
Output Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from OUT_LDOx to GND, active discharge disabled (Lxx_ADE = 0)				0.1		µA
Active-Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (Lxx_ADE = 1)				65		Ω
OVERVOLTAGE CLAMP								
Clamp Active Regulation Voltage		Clamp active (OVCLMP_EN_Lxx = 1), LDO output sinking 0.1mA				V_{NOM}		V
Clamp Disabled Overvoltage Sink Current		V_{OUTxx} = V_{NOM} x 110%				2.2		µA

Electrical Characteristics—300mA PMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING							
Turn ON Time	t_{LON}	Time from LDO enable command received to the output starting to slew, LDO bias enabled	Lxx_SS = 0		10		µs
			Lxx_SS = 1		60		µs
Turn OFF Time		After LDO is disabled, the LDO output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active-discharge resistor			0.1		µs
Transition time from Low Power mode to Normal Mode					50		µs
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} rising		92	95	%
			V_{OUT} falling	84	87		
Power-OK Noise Pulse Immunity	$t_{POKNFLDO}$	V_{OUT} pulsed from 100% to 80% of regulation			25		µs

Electrical Characteristics—150mA NMOS

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPERATIONAL SPECIFICATIONS							
Input Voltage Range	V_{INxx}	Note 15		V_{OUT}		5.5	V
Battery Voltage Range	V_{MBATT}	Guaranteed by main bias testing (Note 16)		2.45		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7V or V_{OUT} +0.3V	25mV/step (6-bit)	0.8		2.375	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	150			mA
			Low-power mode		5		
Minimum Output Capacitance for Stable Operation (Note 13, Note 14)	C_{OUTxx}	Normal mode (1.0µF is recommended for “nice” transient performance)	Nominal capacitor value		0		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0		
		Low-power mode	Nominal capacitor value		1		
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0.7		
BIAS							
Bias Enable Time	t_{LBIAS}	Time to enable LDO bias only; central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS}	LDO bias enabled. L_B_EN = 1			10		µA
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage, V_{MBATT} = V_{NOM} +1.5V with 2.45V minimum	-3		+3	%
		Low-power mode	V_{MBATT} = V_{NOM} +0.3V to 5.5V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage, V_{IN} = V_{NOM} +0.3V	-5		+5	
Load Regulation (Note 14)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM} +0.3V V_{MBATT} = V_{NOM} +1.5V with 2.45V minimum		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM} +0.3V, V_{MBATT} = V_{NOM} +0.3V with 2.45V minimum		0.05		

Electrical Characteristics—150mA NMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Line Regulation (Note 14)		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V, I_{OUT} = 0.1mA			0.01		%/V
		Low-power mode	V_{MBATT} = V_{NOM} +0.3V to 5.5V with 2.45V minimum, V_{IN} = V_{NOM} +0.3V I_{OUT} = 0.1mA			0.01		
Dropout Voltage	V_{DOxx}	Normal mode	I_{OUT} = I_{MAX}	V_{MBATT} - V_{OUT} = 2.5V		50	100	mV
				V_{MBATT} - V_{OUT} = 1.5V		150	300	
		Low-power mode	I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	V_{OUT} = 0V, percentage of I_{MAX}			103	180	250	%
Output Load Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to 5.5V; I_{OUT} = 1% to 100% to 1% of I_{MAX}, V_{NOM} set to any voltage, t_R = t_F = 1µs, C_{OUT} = 1µF				60		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to 5.5V; I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. t_R = t_F = 1µs, C_{OUT} = 1µF				25		
Output Line Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V; t_R = t_F = 1µs, I_{OUT} = I_{MAX}, V_{NOM} set to any voltage				5		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V; t_R = t_F = 1µs, I_{OUT} = 5mA, V_{NOM} set to any voltage, C_{OUT} = 1µF				5		
Power Supply Rejection	PSRRxx	Rejection from V_{IN} to V_{OUT} I_{OUT} = 10% of I_{MAX} C_{OUT} = 1µF	V_{INDC} = V_{NOM}+1V V_{INAC} = 50mV	f = 1kHz		88		dB
				f = 10kHz		65		
				f = 100kHz		51		
				f = 1000kHz		22		
				f = 4450kHz		15		
			V_{INDC} = V_{NOM} +0.5V V_{INAC} = 50mV	f = 1kHz		85		
				f = 10kHz		63		
				f = 100kHz		49		
				f = 1000kHz		21		
				f = 4450kHz		14		
			V_{INDC} = V_{NOM}+0.1V V_{INAC} = 10mV	f = 1kHz		45		
				f = 10kHz		45		
				f = 100kHz		30		
				f = 1000kHz		18		
				f = 4450kHz		10		
		Low-power mode, I_{OUT} = 1mA, f = 1kHz, rejection from V_{MBATT} to V_{OUT}				50		

Electrical Characteristics—150mA NMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}
			V_{OUT} = 1.8V		65		
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, Note 17	Lxx_SS = 0		100		mV/µs
			Lxx_SS = 1		5		
Output Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from OUT_LDOx to GND, active discharge disabled (Lxx_ADE = 0)			0.1		µA
Active-Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (Lxx_ADE = 1)			65		Ω
OVERVOLTAGE CLAMP							
Clamp Active Regulation Voltage		Clamp active (OVCLMP_EN_Lxx = 1), LDO output sinking 0.1mA			V_{NOM}		V
Clamp Disabled Overvoltage Sink Current		V_{OUTxx} = V_{NOM} x 110%			2.5		µA
TIMING							
Enable Delay	t_{LON}	Time from LDO enable command received to the output starting to slew, LDO bias enabled	Lxx_SS = 0		15		µs
			Lxx_SS = 1		140		µs
Disable Delay	t_{LDD}	After LDO is disabled, the LDO output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active discharge resistor			0.1		µs
Transition Time from Low-Power Mode to Normal Mode					50		µs
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J Rising		165		°C
			T_J Falling		150		
POWER-OK							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} Rising		92	95	%
			V_{OUT} Falling	84	87		
Power-OK Noise Pulse Immunity	$t_{POKNFLDO}$	V_{OUT} pulsed from 100% to 80% of regulation			25		µs

Electrical Characteristics—300mA NMOS

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPERATIONAL SPECIFICATIONS							
Input Voltage Range	V_{IN_LDO}	Note 15		V_{OUT}		5.5	V
Battery Voltage Range	V_{MBATT}	Guaranteed by main bias testing		2.45		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7V or V_{OUT} +0.3V.	50mV/Step (6-bit)	0.8		3.95	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	300			mA
			Low-power mode		5		
Minimum Output Capacitance for Stable Operation (Note 13, Note 14)	C_{OUTxx}	Normal mode (2.2µF is recommended for “nice” transient performance)	Nominal capacitor value		0		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0		
		Low-power mode	Nominal capacitor value		1		
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0.7		
BIAS							
Bias Enable Time	t_{LBIAS}	Time to enable LDO bias only; central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS}	LDO bias enabled; L_B_EN = 1			10		µA
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-3		+3	%
		Low-power mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage	-5		+5	
Load Regulation (Note 14)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM} +0.3V, V_{NOM} set to any voltage		0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM} +0.3V with 1.7V minimum, V_{NOM} set to any voltage		0.05		

Electrical Characteristics—300mA NMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Line Regulation (Note 14)		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V, I_{OUT} = 0.1mA, V_{NOM} set to any voltage			0.01		%/V
		Low-power mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA, V_{NOM} set to any voltage			0.01		
Dropout Voltage	V_{DOxx}	Normal mode	I_{OUT} = I_{MAX}	V_{MBATT} - V_{OUT} = 2.5V		50	100	mV
				V_{MBATT} - V_{OUT} = 1.5V		150	450	
		Low-power mode	I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	OUT = 0V			110	180	250	%
Output Load Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to 5.5V; I_{OUT} = 1% to 100% to 1% of I_{MAX}, V_{NOM} set to any voltage, t_R = t_F = 1µs, C_{OUT} = 2.2uF				60		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to 5.5V; I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. t_R = t_F = 1µs, C_{OUT} = 2.2µF				25		
Output Line Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V; t_R = t_F = 1µs, I_{OUT} = I_{MAX}, V_{NOM} set to any voltage				5		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V. t_R = t_F = 1µs, I_{OUT} = 5mA, V_{NOM} set to any voltage				5		
Power Supply Rejection	PSRRxx	Rejection from V_{IN} to V_{OUT} I_{OUT} = 10% of I_{MAX}	V_{INDC} = V_{NOM} +1V V_{INAC} = 50mV	f = 1kHz		88		dB
				f = 10kHz		65		
				f = 100kHz		51		
				f = 1000kHz		22		
				f = 4450kHz		15		
			V_{INDC} = V_{NOM} +0.5V V_{INAC} = 50mV	f = 1kHz		85		
				f = 10kHz		63		
				f = 100kHz		49		
				f = 1000kHz		21		
				f = 4450kHz		14		
			V_{INDC} = V_{NOM} +0.1V V_{INAC} = 10mV	f = 1kHz		45		
				f = 10kHz		45		
				f = 100kHz		30		
				f = 1000kHz		18		
				f = 4450kHz		10		
		Low-power mode, I_{OUT} = 1mA, f = 1kHz, rejection from V_{BATT} to V_{OUT}				50		

Electrical Characteristics—300mA NMOS (continued)

($V_{MBATT} = V_{IN}$ = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 0.8V		55		μV_{RMS}
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 1.8V		65		μV_{RMS}
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, Note 17	Lxx_SS = 0		100		mV/µs
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, Note 17	Lxx_SS = 1		5		mV/µs
Output Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from OUT_LDOx to GND, active discharge disabled (Lxx_ADE = 0)			0.1		µA
Active-Discharge Resistance		Output disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active discharge enabled (Lxx_ADE = 1)			65		Ω
OVERVOLTAGE CLAMP							
Clamp Active Regulation Voltage		Clamp active (OVCLMP_EN_Lxx = 1), LDO output sinking 0.1mA			V_{NOM}		V
Clamp Disabled Overvoltage Sink Current		$V_{OUTxx} = V_{NOM}$ x 110%			2.2		µA
TIMING							
Turn-On Time	t_{LON}	Time from LDO enable command received to the output starting to slew, LDO bias enabled	Lxx_SS = 0		15		µs
Turn-On Time	t_{LON}	Time from LDO enable command received to the output starting to slew, LDO bias enabled	Lxx_SS = 1		140		µs
Turn-Off Time		After LDO is disabled, the LDO output voltage discharges based on load and C_{OUT}. To ensure fast discharge times, enable the active-discharge resistor			0.1		µs
Transition Time from Low-Power Mode to Normal Mode					50		µs
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
Thermal Shutdown		Output disabled or enabled	T_J falling		150		°C
POWER-OK							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} rising		92	95	%
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} falling	84	87		%
Power-OK Noise Pulse Immunity	$t_{POKNFLDO}$	V_{OUT} pulsed from 100% to 80% of regulation			25		µs

Electrical Characteristics—450mA NMOS

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OPERATIONAL SPECIFICATIONS							
Input Voltage Range	V_{INxx}	Note 15		V_{OUT}		5.5	V
Battery Voltage Range	V_{MBATT}	Guaranteed by main bias testing		2.45		5.5	V
Output Voltage Range	V_{OUTxx}	V_{INxx} is the maximum of 3.7V or V_{OUT} +0.3V.	50mV/step (6-bit)	0.8		3.95	V
Maximum Output Current	I_{MAXxx}	Guaranteed by output accuracy	Normal mode	450			mA
			Low-power mode		5		
Minimum Output Capacitance for Stable Operation (Note 13, Note 14)	C_{OUTxx}	Normal mode (4.7µF is recommended for “nice” transient performance)	Nominal capacitor value		0		µF
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0		
		Low-power mode	Nominal capacitor value		1		
			Minimum capacitor value after deration for initial accuracy, temperature coefficient, DC bias voltage, and aging		0.7		
BIAS							
Bias Enable Time	t_{LBIAS}	Time to enable LDO bias only, central bias is already enabled			90		µs
Bias Enable Currents	I_{QBIAS}	LDO bias enabled; L_B_EN = 1			10		µA
CORE PERFORMANCE SPECIFICATIONS							
Output Voltage Accuracy		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V, I_{OUT} = 0.1mA to I_{MAX}, V_{NOM} set to any voltage	-3		+3	%
		Low-power mode	V_{MBATT} = V_{NOM} +1.5V to 5.5V with 2.45V minimum, I_{OUT} = 0.1mA to 5mA, V_{NOM} set to any voltage; V_{IN} = V_{NOM} +0.3V	-5		+5	

Electrical Characteristics—450mA NMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Load Regulation (Note 14)		Normal mode	I_{OUT} = 0.1mA to I_{MAX}, V_{IN} = V_{NOM} +0.3V			0.05		%
		Low-power mode	I_{OUT} = 0.1mA to 5mA, V_{IN} = V_{NOM} +0.3V with 1.7V minimum			0.05		
Line Regulation (Note 14)		Normal mode	V_{IN} = V_{NOM} +0.3V to 5.5V, I_{OUT} = 0.1mA			0.01		%/V
		Low-power mode	V_{IN} = V_{NOM} +0.3V to 5.5V with 1.7V minimum, I_{OUT} = 0.1mA			0.01		
Dropout Voltage	V_{DOxx}	Normal mode	I_{OUT} = I_{MAX}	V_{MBATT} - V_{OUT} = 2.5V		50	100	mV
				V_{MBATT} - V_{OUT} = 1.5V		150	450	
		Low-power mode	I_{OUT} = 5mA, V_{IN} = 3.7V			150	300	
Output Current Limit	I_{LIMxx}	OUT = 0V			105	180	250	%
Output Load Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to 5.5V; I_{OUT} = 1% to 100% to 1% of I_{MAX}, V_{NOM} set to any voltage, t_R = t_F = 1µs, C_{OUT} = 4.7µF				60		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to 5.5V; I_{OUT} = 0.05mA to 5mA to 0.05mA, V_{NOM} set to any voltage. t_R = t_F = 1µs, C_{OUT} = 4.7µF				25		
Output Line Transient (Note 14)		Normal mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V; t_R = t_F = 1µs, I_{OUT} = I_{MAX}, V_{NOM} set to any voltage				5		mV
		Low-power mode, V_{IN} = V_{NOM} +0.3V to V_{NOM} +0.8V to V_{NOM} +0.3V; t_R = t_F = 1µs, I_{OUT} = 5mA, V_{NOM} set to any voltage				5		

Electrical Characteristics—450mA NMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
Power Supply Rejection	PSRRxx	Rejection from V_{IN} to V_{OUT} I_{OUT} = 10% of I_{MAX}	V_{INDC} = V_{NOM} +1V V_{INAC} = 50mV	f = 1kHz		88		dB
				f = 10kHz		65		
				f = 100kHz		51		
				f = 1000kHz		22		
				f = 4450kHz		15		
			V_{INDC} = V_{NOM} +0.5V V_{INAC} = 50mV	f = 1kHz		85		
				f = 10kHz		63		
				f = 100kHz		49		
				f = 1000kHz		21		
				f = 4450kHz		14		
			V_{INDC} = V_{NOM} +0.1V V_{INAC} = 10mV	f = 1kHz		45		
				f = 10kHz		45		
				f = 100kHz		30		
				f = 1000kHz		18		
				f = 4450kHz		10		
		Low-power mode, I_{OUT} = 1mA, f = 1kHz, rejection from V_{MBATT} to V_{OUT}				50		
Output Noise		f = 10Hz to 100kHz, I_{OUT} = 10% of I_{MAX}	V_{OUT} = 0.8V			55		μV_{RMS}
			V_{OUT} = 1.8V			65		
Soft-Start and Dynamic Voltage Change Ramp Rate	t_{SSxx}	After enabling, Note 17	Lxx_SS = 0			100		mV/µs
			Lxx_SS = 1			5		
Output Disabled Leakage Current		Output disabled, V_{OUT} = 1V, current from OUT_LDOx to GND, active-discharge disabled (Lxx_ ADE = 0)				0.1		µA
Active-Discharge Resistance		Output Disabled, V_{OUT} = 1V, resistance from OUT_LDOx to GND, active-discharge enabled (Lxx_ADE = 1)				65		Ω
OVERVOLTAGE CLAMP								
Clamp Active Regulation Voltage		Clamp active (OVCLMP_EN_Lxx = 1), LDO output sinking 0.1mA				V_{NOM}		V
Clamp Disabled Overvoltage Sink Current		V_{OUTxx} = V_{NOM} x 110%				2.2		µA

Electrical Characteristics—450mA NMOS (continued)

(V_{MBATT} = V_{IN} = 3.7V, T_A = -40°C to +85°C, unless otherwise noted.) (Note 12)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIMING							
Turn-On Time	t_{LON}	Time from LDO enable command received to the output starting to slew, LDO bias enabled	Lxx_SS = 0		15		µs
			Lxx_SS = 1		140		µs
Turn-Off Time		After LDO is disabled, the LDO output voltage discharges based on Load and C_{OUT}. To ensure fast discharge times enable the active-discharge resistor			0.1		µs
Transition Time from Low-Power Mode to Normal Mode					50		µs
THERMAL SHUTDOWN							
Thermal Shutdown		Output disabled or enabled	T_J rising		165		°C
			T_J falling		150		
POWER-OK							
Power-OK Threshold	V_{POKTHL}	V_{OUT} when V_{POK} switches	V_{OUT} rising		92	95	%
			V_{OUT} falling	84	87		
Power-OK Noise Pulse Immunity	$t_{POKNFLDO}$	V_{OUT} pulsed from 100% to 80% of regulation			25		µs

Note 12: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control (SQC) methods.

Note 13: For stability requirements, refer to the *Remote Capacitor Design with the Register Adjustable Compensation* section.

Note 14: Does not include ESR of the capacitance or trace resistance of the PCB.

Note 15: Input voltage range is guaranteed from V_{OUT} +0.3V to 5.5V by output accuracy specifications. Inputs between V_{OUT} and V_{OUT} +0.3V are guaranteed by design and subject to drop-out resistance limitations [V_{IN} (min) = V_{OUT} + I_{OUT} x R_{DO}] and may have reduced PRSS and transient performance. For example, with V_{OUT} = 0.8V and V_{MBATT} = 2.7V, R_{DO} = 0.5Ω therefore with I_{OUT} = 0.2A, the input voltage must be at least 0.9V (V_{IN} ≥ V_{OUT} +I_{OUT} x R_{DO} = 0.8V + 0.2A x 0.5Ω = 0.9V).

Note 16: Battery Voltage Range is guaranteed from V_{OUT} +1.5V to 5.5V by the Dropout Voltage specification. Inputs between V_{OUT} +1.0V and V_{OUT} +1.5V are guaranteed by design and subject to drop-out resistance limitations (see *Typical Operating Characteristics*). Absolute minimum battery voltage range for LDOs is 2.45V.

Note 17: During a soft-start event or a DVS transition, the regulators output current increases by C_{OUT} x dV/dt. In the event that the load current plus the additional current imposed by the soft-start or DVS transition reach the regulator's current limit, the current limit is enforced. When the current limit is enforced, the advertised transition rate (dV/dt) does not occur.

Electrical Characteristics—GPIOs

(V_{MBATT} = V_{GPIO_INA} = V_{GPIO_INB} = 3.6V, I_{BBATT} = 0µA, circuit of *Simplified Functional Diagram*, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 18)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY							
Supply Voltage	V_{GPIO_INx}			1.7		5.5	V
Supply Current	I_{GPIO_INx}					1	µA
GPIO INPUT							
Input Voltage Low	V_{IL}	GPIO0-3, V_{GPIO_INA} = 1.7V to 5.5V				0.5	V
		GPIO4-7, V_{GPIO_INB} = 1.7V to 5.5V				0.5	
Input Voltage High	V_{IH}	GPIO0-3, V_{GPIO_INA} = 1.7V to 5.5V		0.7 x V_{GPIO_INA}			V
		GPIO4-7, V_{GPIO_INB} = 1.7V to 5.5V		0.7 x V_{GPIO_INB}			
Input Hysteresis	V_{hys}				0.25		V
Input Leakage Current	I_i	V_{GPIO_INA} = 5.5V V_{GPIO_INB} = 5.5V V_{IN} = 0V and 5.5V	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
GPIO PUSH-PULL OUTPUT—GPIO0-GPIO7							
Output Voltage Low	V_{OL}	I_{SINK} = 4mA				0.08	V
		I_{SINK} = 12mA				0.25	
Output Voltage High	V_{OH}	GPIO0-3, I_{SOURCE} = 4mA		0.7 x V_{GPIO_INA}			V
		GPIO4-7, I_{SOURCE} = 4mA		0.7 x V_{GPIO_INB}			
GPIO OPEN-DRAIN OUTPUT—GPIO0-GPIO7							
Output Voltage Low	V_{OL}	I_{SINK} = 4mA				0.08	V
		I_{SINK} = 12mA				0.25	
Output High Leakage Current	I_{OH}	V_{GPIO_INx} = 5.5V, T_A = +25°C, internal pullup/pulldown disabled			0.01	1.0	µA
		V_{GPIO_INx} = 5.5V, T_A = +85°C, internal pullup/pulldown disabled			0.1		
GPIO PULL RESISTANCES—GPIO0-GPIO7							
Pullup Resistance	R_{PU}	Note 19		50	100	160	kΩ
Pulldown Resistance	R_{PD}	Note 19		50	100	160	kΩ

Electrical Characteristics—GPIOs (continued)

(V_{MBATT} = V_{GPIO_INA} = V_{GPIO_INB} = 3.6V, I_{BBATT} = 0μA, circuit of *Simplified Functional Diagram*, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 18)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE OUTPUT—GPIO7						
Output Voltage	V_{REF}	0μA < I_{REFOUT} < 160μA	1.225	1.250	1.272	V
Line Regulation		V_{MBATT} = 5.5V, 2.6V < V_{GPIO_INB} < 5.5V, I_{REFOUT} = 0μA		2		mV
Load Regulation		0μA < I_{REFOUT} < 160μA		2		mV
Ripple Rejection		f = 1kHz		70		dB
Output Current		V_{MBATT} = 5.5V, 2.6V < V_{GPIO_INB} < 5.5V, I_{REFOUT} = 0μA	160			μA
Output Noise Voltage		10Hz to 100kHz, C_{REFOUT} = 20pF		55		$μV_{RMS}$

Note 18: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 19: The min/max variation shows it is based on process statistics. This parameter is not production tested.

Electrical Characteristics—RTC

(V_{MBATT} = 3.6V, V_{BBATT} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 20)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{RTC}	Note 21		1.65		5.5	V
B_{BATT} Current	I_{BBATT}	V_{MBATT} = 0V, PWR_MD_32k = 0b00	V_{BBATT} = 2.45V		2.0		μA
			V_{BBATT} = 3.00V		2.2	4.2	
Time Accuracy		Per day (Note 21)			2		s
32KCLK Input Frequency		f_{32KCLK}			32768		Hz
32KCLK Voltage		V_{32KCLK}			V_{RTC}		V

Note 20: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 21: Design guidance only, not tested during final test.

Electrical Characteristics—32kHz Crystal Oscillator

(V_{MBATT} = 3.6V, V_{RTC} = 2.5V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 20)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR							
Minimum Oscillator Supply Voltage	$V_{RTCUVLO}$				1.5		V
Oscillator Supply Current	I_{BBATT}	V_{MBATT} = 3.6V, V_{BBATT} = 2.55V, backup battery charger target voltage = 2.5V (BBCRS[1:0] = 0b00)	Low-jitter mode (PWR_MD_32K[1:0] = 0b11)		23		µA
			Low-power mode (PWR_MD_32K[1:0] = 0b00)		2.0		
Oscillator Voltage Temperature Coefficient	V_{OLTCO}	V_{OSC} = 1.5V to 3.4V			20		ppm/V
Maximum Crystal ESR					90		kΩ
Parasitic XIN/XOUT Pin Capacitance	C_{PAR}	From XIN to XGND and from XOUT to XGND			3		pF
Crystal Loading		32KLOAD = 0x03			6.5		pF
		32KLOAD = 0x00			7.5		
		32KLOAD = 0x01			12.5		
Maximum Oscillator Start-Up Time	t_{OSU}				1000		ms
32K OUTPUT BUFFERS							
Output Frequency	f_{32K_OUTx}				32768		Hz
32k Output Buffer Supply Voltage		Buffer is internally supplied by GPIO_INB		1.7	1.8		V
Supply Current	I_{32K_OUTx}	C_{32K_OUTx} = 25pF, f_{32K_OUTx} = 32768Hz, (Note 22)			3.7		µA
Maximum 32K_OUTx Enable Time		Clock input = 32768Hz			64		µs
32K_OUT0 Duty Cycle		Low-power mode (PWR_MD_32K[1:0] = 0b00)		40		60	%
		Low-jitter mode (PWR_MD_32K[1:0] = 0b11) push-pull output (OTP_32K = 0)		45		55	
32K_OUT0 Rise/Fall Time		C_{32K_OUTx} = 25pF			20		ns
32K_OUT0 Output Voltage High	V_{OH}	V_{GPIO_INB} = 1.7V, I_{SOURCE} = 4mA, push-pull output (OTP_32K = 0)		0.7 x V_{GPIO_INB}			V
Output High Leakage Current (Note 22)	I_{OZH}	T_A = +25°C, open-drain output (OTP_32K = 1)			0.001	1	µA
32K_OUT0 Output Voltage Low	V_{OL}	V_{GPIO_INB} = 1.7V, I_{SINK} = 4mA				0.4	V

Note 22: The MAX77863 internal clock buffer consumes 1uA. To drive a 25pF capacitor at 32kHz consumes 2.7µA (C x V x F losses). Therefore, enabling a single 32kHz clock buffer consumes approximately 3.7µA.

Electrical Characteristics—Backup Battery Charger

(Operating conditions (unless otherwise specified) V_{MBATT} = 3.7V, V_{BBATT} = 3.0V, T_A = -40°C to +85°C.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Programmable Output Voltage Range	I_{LOAD} = 1µA		BBCVS[1:0] = 0x00	2.420	2.500	2.580	V
			BBCVS[1:0] = 0x01	2.910	3.000	3.090	
			BBCVS[1:0] = 0x02	3.200	3.300	3.400	
			BBCVS[1:0] = 0x03	3.395	3.500	3.605	
Constant Current Limit	V_{BBATT} short to GND	BBCLOWIEN = 0	BBCCS[1:0] = 0x00, 0x01, 0x02		50		µA
			BBCCS[1:0] = 0x01		100		
		BBCLOWIEN = 1	BBCCS[1:0] = 0x00		200		
			BBCCS[1:0] = 0x01		600		
			BBCCS[1:0] = 0x02		800		
			BBCCS[1:0] = 0x03		400		
Output Resistance	BBCRS[1:0] = 0x00				0.1		kΩ
	BBCRS[1:0] = 0x01				1		
	BBCRS[1:0] = 0x02				3		
	BBCRS[1:0] = 0x03				6		
Reverse Leakage Current from BBATT to V_{MBATT}	Input = 0V, V_{BBATT} = 3.0V		T_A = +25°C		0.01	10	µA
			T_A = +85°C		0.1		
Charger Ground Current	I_{LOAD} = 1µA (Note 1)				5		µA

Electrical Characteristics—On-Off Controller

(V_{MBATT} = 3.6V, I_{BBATT} = 0μA, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 23)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN0						
Input Voltage Low	V_{IL}				0.4	V
Input Voltage High	V_{IH}		1.4			V
Input Hysteresis	V_{HVS}			0.05		V
Debounce Time	t_{DBEN0}		24	30	36	ms
EN0_1SEC Time	$t_{1SECEN0}$			1		s
Manual Reset Time	t_{HRDRST}	MRT[2:0] = 0b000		2		s
		MRT[2:0] = 0b001		3		
		MRT[2:0] = 0b010		4		
		MRT[2:0] = 0b011		5		
		MRT[2:0] = 0b100		6		
		MRT[2:0] = 0b101		8		
		MRT[2:0] = 0b110		10		
		MRT[2:0] = 0b111		12		
Manual Reset Warning Time (MRWRN)	t_{MRWRN}	MRT[2:0] = 0b000		2		s
		MRT[2:0] = 0b001		2		
		MRT[2:0] = 0b010		3		
		MRT[2:0] = 0b011		4		
		MRT[2:0] = 0b100		5		
		MRT[2:0] = 0b101		6		
		MRT[2:0] = 0b110		8		
		MRT[2:0] = 0b111		10		
Internal Pullup Resistance	R_{PUEN0}	Only available with OTP_EN0AL = 1, Figure 20		10		kΩ
Internal Pulldown Resistance	R_{PDEN0}	Only available with OTP_EN0AL = 0, Figure 20		10		kΩ

Note 23: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Electrical Characteristics—FPS

(V_{MBATT} = 3.6V, I_{BBATT} = 0µA, circuit of *Simplified Functional Diagram*, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 24)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Flexible Power Sequencer Enable Delay	t_{FSDON}	The MAX77863 reference is already powered up prior to the enable command (Note 25)			0.01		µs
		The MAX77863 reference is powered down prior to the enable command			30		
Flexible Power Sequencer Disable Delay	$t_{FPSDOFF}$				0.01		µs
Flexible Power Sequencer Event Period	t_{FST}	Figure 28	TFPSx[2:0] = 0b000		40		µs
			TFPSx[2:0] = 0b001		80		
			TFPSx[2:0] = 0b010		160		
			TFPSx[2:0] = 0b011		320		
			TFPSx[2:0] = 0b100		640		
			TFPSx[2:0] = 0b101		1280		
			TFPSx[2:0] = 0b110		2560		
			TFPSx[2:0] = 0b111		5120		
Flexible Power Sequencer Event Period Timer Accuracy		Accuracy of the flexible power sequencer clock		-15		+15	%

Note 24: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

Note 25: The MAX77863 reference is powered up if any of the step-down regulators or any of the low dropout linear regulators are enabled.

Electrical Characteristics—I2C

(V_{MBATT} = 3.6V, V_{INI2C} = 1.8V, circuit of *Simplified Functional Diagram*, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 26)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
INI2C Voltage	V_{INI2C}		1.7		3.6	V
SDA AND SCL I/O STAGES						
SCL, SDA Input High Voltage	V_{IH}	V_{INI2C} = 1.7V to 3.6V	0.7 x V_{INI2C}			V
SCL, SDA Input Low Voltage	V_{IL}	V_{INI2C} = 1.7V to 3.6V			0.3 x V_{INI2C}	V
SCL, SDA Input Hysteresis	V_{HYS}			0.05 x V_{INI2C}		V
SCL, SDA Input Current	II	V_{I2CIN} = 3.6V or 0V	-10		+10	µA
SDA Output Low Voltage	V_{OL}	Sinking 20mA			0.4	V
SCL, SDA Pin Capacitance	Ci			10		pF
Output Fall Time from VIH to VIL	t_{OF}	Note 27			120	ns

Electrical Characteristics—I2C (continued)

(V_{MBATT} = 3.6V, V_{INI2C} = 1.8V, circuit of *Simplified Functional Diagram*, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 27)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I2C-COMPATIBLE INTERFACE TIMING FOR STANDARD, FAST, AND FAST-MODE PLUS						
Clock Frequency	f_{SCL}				1000	kHz
Hold Time (Repeated) START Condition	$t_{HD;STA}$		0.26			µs
CLK Low Period	t_{LOW}		0.5			µs
CLK High Period	t_{HIGH}		0.26			µs
Set-Up Time Repeated START Condition	$t_{SU;STA}$		0.26			µs
DATA Hold Time	$t_{HD:DAT}$		0			µs
DATA Set-Up time	$t_{SU;DAT}$		50			ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		0.26			µs
Bus-Free Time Between STOP and START	t_{BUF}		0.5			µs
Capacitive Load for Each Bus Line	C_B				550	pF
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter				50		ns

Electrical Characteristics—I2C (continued)

(V_{MBATT} = 3.6V, V_{INI2C} = 1.8V, circuit of *Simplified Functional Diagram*, T_A = -40°C to +85°C, unless otherwise specified, typical values are at T_A = +25°C.) (Note 27)

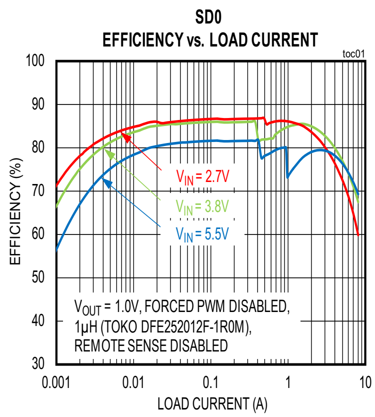
PARAMETER	SYMBOL	CONDITIONS	C_B = 100pF		C_B = 400pF		UNITS
			MIN	MAX	MIN	MAX	
I2C-COMPATIBLE INTERFACE TIMING FOR HS-MODE							
Clock Frequency	f_{SCL}			3.4		1.7	MHz
Set-Up Time Repeated START Condition	$t_{SU;STA}$		160		160		ns
Hold Time (Repeated) START Condition	$t_{HD;STA}$		160		160		ns
CLK Low Period	t_{LOW}		160		320		ns
CLK High Period	t_{HIGH}		60		120		ns
DATA Set-Up time	$t_{SU;DAT}$		10		10		ns
DATA Hold Time	$t_{HD:DAT}$		0	70	0	150	ns
SCL Rise Time	t_{RCL}		10	40	20	80	ns
Rise Time of SCL Signal After a Repeated START Condition and after an Acknowledge Bit	t_{rCL1}		10	80	20	80	ns
SCL Fall Time	t_{fCL}		10	40	20	80	ns
SDA Rise Time	t_{rDA}		10	80	20	160	ns
SDA Fall Time	t_{fDA}		10	80	20	160	ns
Set-Up Time for STOP Condition	$t_{SU;STO}$		160		160		ns
Capacitive Load for Each Bus Line	C_B			100		400	pF
Maximum Pulse Width of Spikes that Must be Suppressed by the Input Filter				10		10	ns

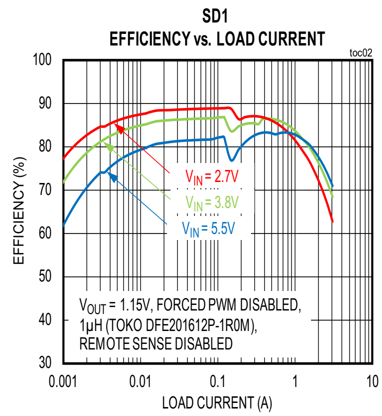
Note 26: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed through correlation using statistical quality control methods.

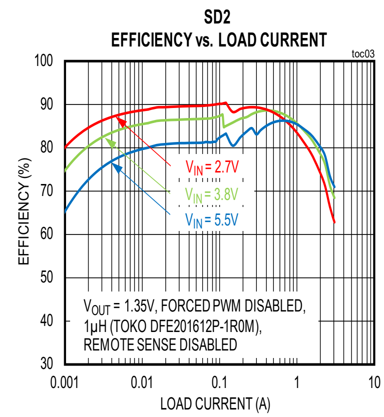
Note 27: System design guidance only. Not production tested.

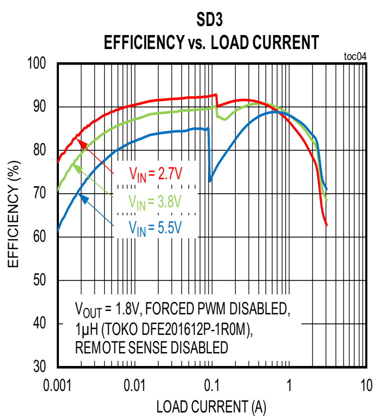
Typical Operating Characteristics

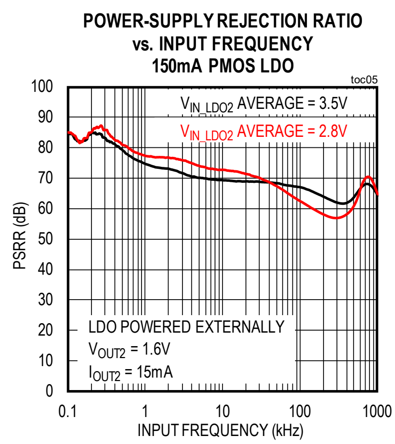
(IN_SDx = MBATT, FPWM Mode, L = 1μH (TOKO 2520 case size) ,remote sense disabled, T_A = +25°C unless otherwise noted.)

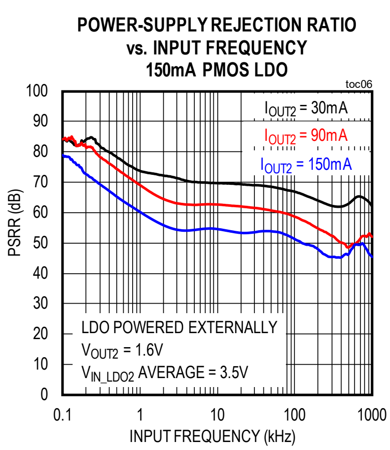


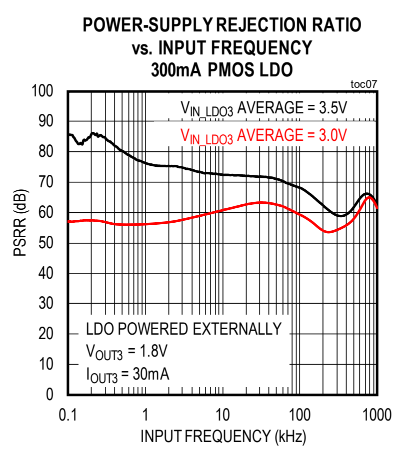








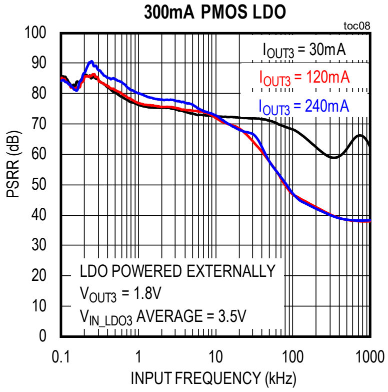




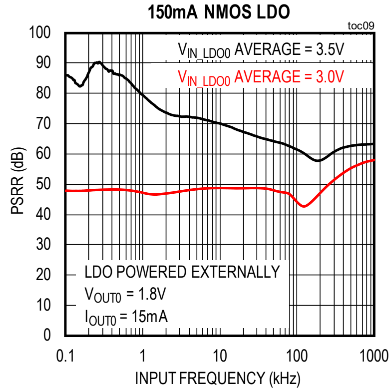
Typical Operating Characteristics (continued)

(IN_SDx = MBATT, FPWM Mode, L = 1μH (TOKO 2520 case size) ,remote sense disabled, T_A = +25°C unless otherwise noted.)

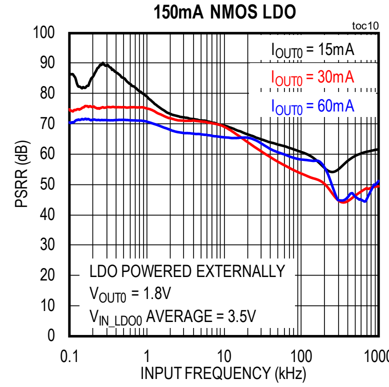
POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 300mA PMOS LDO



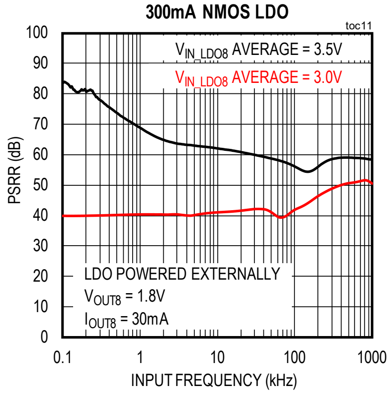
POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 150mA NMOS LDO



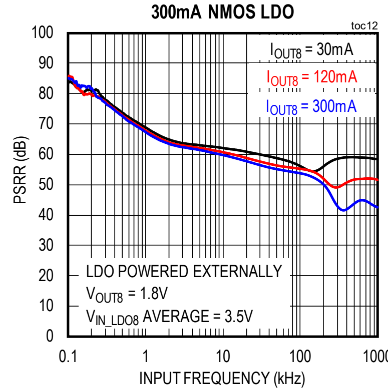
POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 150mA NMOS LDO



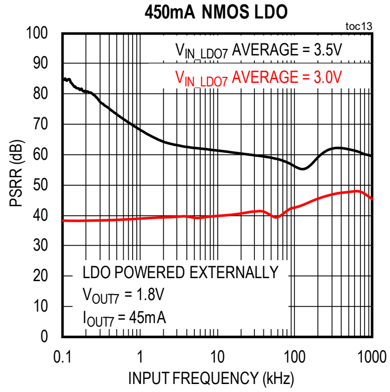
POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 300mA NMOS LDO



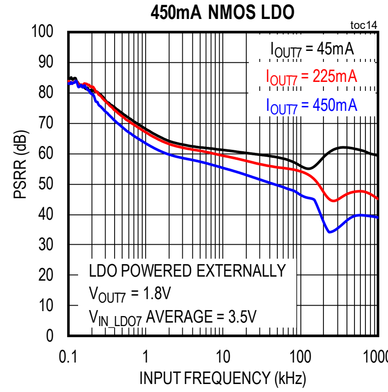
POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 300mA NMOS LDO



POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 450mA NMOS LDO



POWER-SUPPLY REJECTION RATIO vs. INPUT FREQUENCY 450mA NMOS LDO



Bump Configuration

TOP VIEW
(BUMP SIDE DOWN)

MAX77863

	1	2	3	4	5	6	7	8	9	10
A	NIC0	MON	OUT_LDO3	IN_LDO3-5	OUT_LDO5	IN_LDO2	OUT_LDO7	IN_LDO7-8	OUT_LDO8	NIC1
B	IN_SD3	AVSD	OUT_LDO4	IN_LDO4-6	OUT_LDO6	OUT_LDO2	OUT_LDO0	IN_LDO0-1	OUT_LDO1	XIN
C	LX_SD3	LX_SD3	MBATT	FB_SD3	EN1	EN2	EN0	ACOK	XGND	XOUT
D	PG_SD3	nIRQ	FB_SD2	D_SD3	GND	GND	GND	FB_SD1	32K_OUT0	BBATT
E	PG_SD2	SCL	INI2C	GND	LID	GND	GND	SNSN_SD1	SNSP_SD1	SHDN
F	PG_SD2	SDA	GND	GND	FB_SD0	FB_SD0	SNSP_SD0	SNSN_SD0	nRST_IO	PG_SD1
G	LX_SD2	LX_SD2	GPIO4	GPIO6	GPIO_INB	GPIO_INA	GPIO0	GPIO2	LX_SD1	LX_SD1
H	IN_SD2	INB_SD0	GPIO5	GPIO7	PGB_SD0	PGA_SD0	GPIO1	GPIO3	INA_SD0	IN_SD1
J	NIC2	INB_SD0	LXB_SD0	LXB_SD0	PGB_SD0	PGA_SD0	LXA_SD0	LXA_SD0	INA_SD0	NIC3

WLP
(4.1mm x 3.8mm X 0.7mm)

Bump Description

PIN	NAME	DESCRIPTION
LINEAR REGULATORS		
B8	IN_LDO0-1	Linear regulator 0 and 1 power input. Bypass IN_LDO0 to GND with a 1.0μF ceramic capacitor.
A6	IN_LDO2	Linear regulator 2 power input. Bypass IN_LDO2 to GND with a 1.0μF ceramic capacitor.
A4	IN_LDO3-5	Linear regulator 3 and 5 power input. Bypass IN_LDO3-5 to GND with a 1.0μF ceramic capacitor. A single IN_LDO3-5 and IN_LDO4-6 input bypass capacitor can be shared between LDOs 3, 4, 5, and 6 if they are powered from the same input supply.
B4	IN_LDO4-6	Linear regulator 4 and 6 power input. Bypass IN_LDO4-6 to GND with a 1.0μF ceramic capacitor. A single IN_LDO3-5 and IN_LDO4-6 input bypass capacitor can be shared between LDOs 3, 4, 5, and 6 if they are powered from the same input supply.
A8	IN_LDO7-8	Linear regulator 7 and 8 power input. Bypass IN_LDO7-8 to GND with a 1.0μF ceramic capacitor.
B7	OUT_LDO0	LDO0 power output. LDO0 is an N-channel linear regulator.
B9	OUT_LDO1	LDO1 power output. LDO1 is an N-channel linear regulator.
B6	OUT_LDO2	LDO2 power output. LDO2 is a P-channel linear regulator.
A3	OUT_LDO3	LDO3 power output. LDO3 is a P-channel linear regulator.
B3	OUT_LDO4	LDO4 power output. LDO4 is a P-channel linear regulator.
A5	OUT_LDO5	LDO5 power output. LDO5 is a P-channel linear regulator.
B5	OUT_LDO6	LDO6 power output. LDO6 is a P-channel linear regulator.
A7	OUT_LDO7	LDO7 power output. LDO7 is a N-channel linear regulator.
A9	OUT_LDO8	LDO8 power output. LDO8 is a N-channel linear regulator.
GLOBAL RESOURCES		
C3	MBATT	Low-noise PMIC power input. Bypass MBATT with a 0.1μF ceramic capacitor to ground.
A2	MON	Low-battery monitor analog input.
D5, D6, D7, E4, E6, E7	GND	Ground. All GND pins must be connected together.
D10	BBATT	Backup battery connection. Bypass BBATT with a 0.1μF ceramic capacitor to ground.
C10	XOUT	32.768kHz crystal oscillator output. XOUT has on-chip programmable load capacitors for the crystal oscillator.
B10	XIN	32.768kHz crystal oscillator input. XIN has on-chip programmable load capacitors for the crystal oscillator.
C9	XGND	Crystal oscillator ground. All XGND pins must be connected together.
A10	NIC1	Not internally connected #1. However, for best PCB routing, connect NIC1 to XGND.
D9	32K_OUT0	32.768kHz crystal oscillator output. 32K_OUT0 is a 50% duty cycle square wave buffered version of TXIN.

Bump Description (continued)

PIN	NAME	DESCRIPTION
I2C SERIAL INTERFACE		
E3	INI2C	Internal logci supply for SDA and SCl.
F2	SDA	Serial interface data bidirectional open-drain.
E2	SCL	Serial interface clock input. Open-drain output.
D2	nIRQ	Active-low interrupt output. nIRQ is an open-drain output.
ON/OFF CONTROLLER AND FLEXIBLE POWER SEQUENCER		
C7	EN0	Enable input 0 to the flexible power sequencer. EN0 is typically connected to the system's ONKEY. See the *EN0* section for more information.
C5	EN1	Enable input 1 to the flexible power sequencer. EN1 is typically connected to the system's AP. See the *EN1* section for more information.
C6	EN2	Enable input 2 to the flexible power sequencer. EN2 is typically connected to the system's AP. See the *EN2* section for more information.
E10	SHDN	Shutdown digital input.
C8	ACOK	ACOK is a digital input to the ON/OFF controller that typically comes from the system's battery charger .
E5	LID	LID is a digital input to the ON/OFF controller that typically comes from the system's battery charger.
STEP-DOWN REGULATORS		
B2	AVSD	Step-down regulator analog power input. AVSD powers the analog portions of all step-down regulators. INy_SDx, and AVSD are typically connected to MBATT in the typical applications circuit for a 1s battery configuration as shown in Figure 40. For applications with 2s (or higher) battery configuration AVSD can be connected to an external step-down regulator as shown in Figure 41 and all INy_SDx must be connected together.
D4	D_SD3	D_SD3 default output voltage select input. D_SD3 is a tri-level logic input. Connect D_SD3 as described in Table D_SD3 Logic. The logic level of D_SD3 is latched each time the MBATT voltage rises above the main-battery under voltage lockout threshold ($V_{MBATT} > V_{MBATTUVLO}$). Changes to D_SD3 after the logic level has been latched have no effect.
H9, J9	INA_SD0	Power input for phase "A" of the step-down regulator 0. Connect AVSD and all INA_SD0 together. Bypass INA_SD0 to GND with a 4.7μF ceramic capacitor.
H2, J2	INB_SD0	MAX77863 power input for phase "B" of the step-down regulator 0. Connect AVSD and all INB_SD0 together. Bypass INB_SD0 to GND with a 4.7μF ceramic capacitor.
H10	IN_SD1	Power input for step-down regulator 1. Connect AVSD and all IN_SD1 together. All IN_SD1 pins must be connected together. Bypass IN_SD1 to GND with a 2.2μF ceramic capacitor.
J10	NIC3	Not internally connected #3. J10 is not internally connected. However, for best PCB routing, connect NIC3 to IN_SD1.
H1	IN_SD2	Power input for step-down regulator 2. Connect AVSD and all IN_SD2 together. All IN_SD2 pins must be connected together. Bypass IN_SD2 to GND with a 2.2μF ceramic capacitor.
J1	NIC2	Not internally connected #2. J1 is not internally connected. However, for best PCB routing, connect NIC2 to IN_SD2.

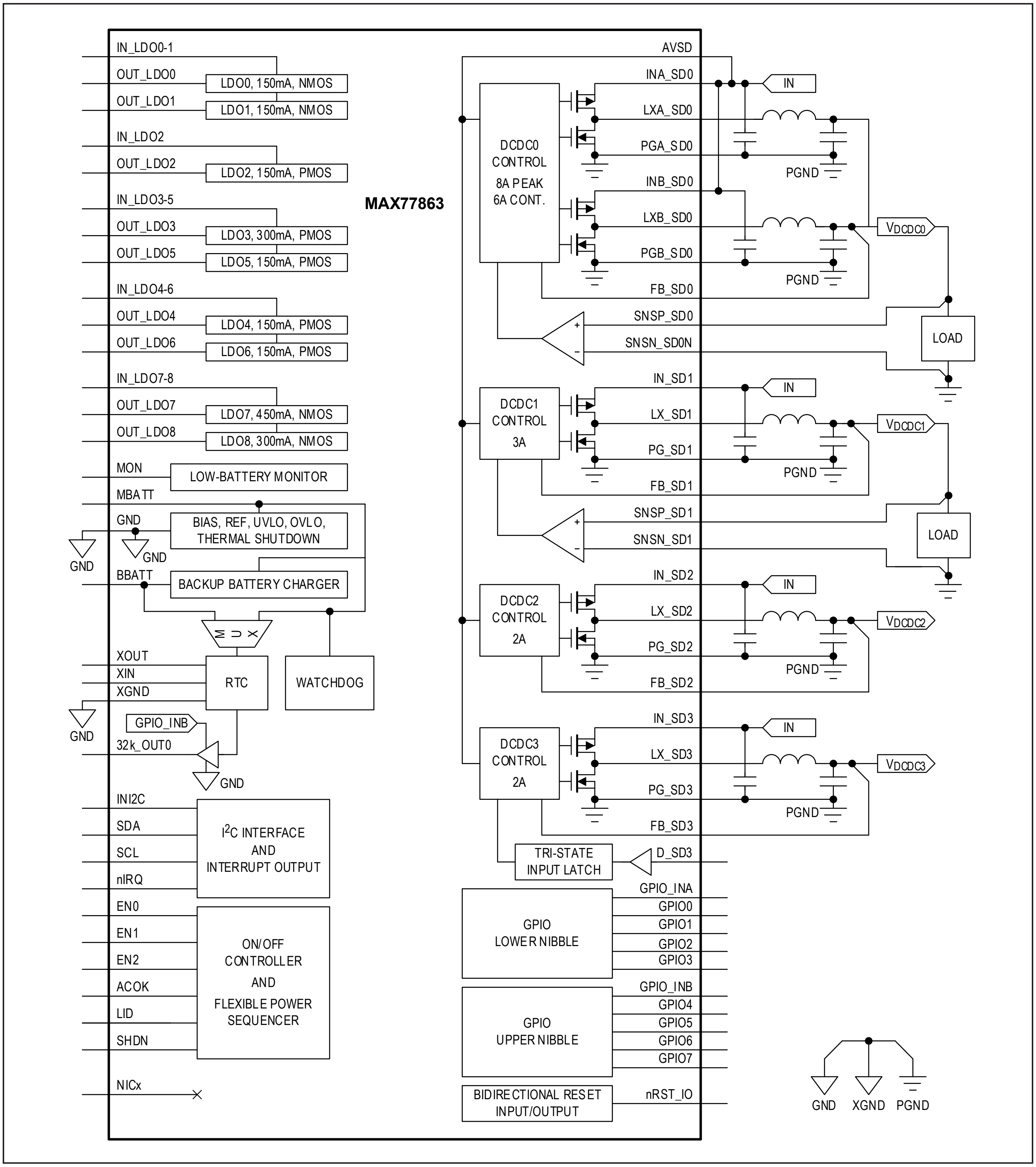
Bump Description (continued)

PIN	NAME	DESCRIPTION
B1	IN_SD3	Power input for step-down regulator 3. Connect AVSD and all IN_SD3 together. All IN_SD3 pins must be connected together. By pass IN_SD3 to GND with a 2.2μF ceramic capacitor.
A1	NIC0	Not internally connected #0. A1 is not internally connected. However, for best PCB routing, connect NIC0 to IN_SD3.
J7, J8	LXA_SD0	Inductor switching node for phase “A” of step-down regulator 0. When the regulator is enabled, the inductor switching node drives between INA_SD0 and PGA_SD0 to maintain FB_SD0 at its regulation threshold. All LXA_SD0 pins must be connected together.
J3, J4	LXB_SD0	Inductor switching node for phase “B” of step-down regulator 0. When the regulator is enabled, the inductor switching node drives between INB_SD0 and PGB_SD0 to maintain FB_SD0 at its regulation threshold. All LXB_SD0 pins must be connected together.
G9, G10	LX_SD1	Inductor switching node for step-down regulator 1. When the regulator is enabled, the inductor switching node drives between IN_SD1 and PG_SD1 to maintain FB_SD1 at its regulation threshold. All LX_SD1 pins must be connected together.
G1, G2	LX_SD2	Inductor switching node for step-down regulator 2. When the regulator is enabled, the inductor switching node drives between IN_SD2 and PG_SD2 to maintain FB_SD2 at its regulation threshold. All LX_SD2 pins must be connected together.
C1, C2	LX_SD3	Inductor switching node for step-down regulator 3. When the regulator is enabled, the inductor switching node drives between IN_SD3 and PG_SD3 to maintain FB_SD3 at its regulation threshold. All LX_SD3 pins must be connected together.
H6, J6	PGA_SD0	Power ground for phase “A” of step-down regulator 0. All PGA_SD0 pins must be connected together.
H5, J5	PGB_SD0	Power ground for phase “B” of step-down regulator 0. All PGB_SD0 pins must be connected together.
F10	PG_SD1	Power ground for step-down regulator 1. All PG_SD1 pins must be connected together.
E1, F1	PG_SD2	Power ground for step-down regulator 2. All PG_SD2 pins must be connected together.
D1	PG_SD3	Power ground for Step-down regulator 3.
F6	FB_SD0	Step-down regulator 0 output voltage feedback node. Connect FB_SD0 directly to the step-down regulator output capacitor.
D8	FB_SD1	Step-down regulator 1 output voltage feedback node. Connect FB_SD1 directly to the step-down regulator output capacitor.
D3	FB_SD2	Step-down regulator 2 output voltage feedback node. Connect FB_SD2 directly to the step-down regulator output capacitor.
C4	FB_SD3	Step-down regulator 3 output voltage feedback node. Connect FB_SD3 directly to the step-down regulator output capacitor.
F5	FB_SD0	Step-down regulator 0 output voltage feedback node. Connect FB_SD0 directly to the step-down regulator output capacitor.
F7	SNSP_SD0	Output voltage remote sense positive input for step-down regulator 0. Connect SNSP_SD0 directly to the point-of-load positive terminal.
E9	SNSP_SD1	Output voltage remote sense positive input for step-down regulator 1. Connect SNSP_SD1 directly to the point-of-load positive terminal.

Bump Description (continued)

PIN	NAME	DESCRIPTION
F4	GND	Unused pin that is internally connected. Connect to ground for the lowest thermal impedance.
F8	SNSN_SD0	Output voltage remote sense negative input for step-down regulator 0. Connect SNSN_SD0 directly to the point-of-load ground terminal.
E8	SNSN_SD1	Output voltage remote sense negative input for step-down regulator 1. Connect SNSN_SD1 directly to the point-of-load ground terminal.
F3	GND	Unused pin that is internally connected. Connect to ground for the lowest thermal impedance.
GPIO		
G6	GPIO_INA	GPIO power input for the lower nibble. Bypass GPIO_INA to GND with a 0.1μF ceramic capacitor. However, for the MAX77863, if GPIO_INA is supplied by one of the on-chip regulators, the regulators output capacitor is sufficient bypass capacitance for GPIO_INA.
G5	GPIO_INB	GPIO power input for the upper nibble. Bypass GPIO_INB to GND with a 0.1μF ceramic capacitor. However, for the MAX77863, if GPIO_INB is supplied by one of the on-chip regulators, the regulators output capacitor is sufficient bypass capacitance for GPIO_INB.
G7	GPIO0	General purpose input/output.
H7	GPIO1	
G8	GPIO2	
H8	GPIO3	
G3	GPIO4	
H3	GPIO5	
G4	GPIO6	
H4	GPIO7	
RESET I/O		
F9	nRST_IO	Bidirectional active-low open-drain reset input/output.

Simplified Functional Diagram



Detailed Description

The MAX77863 is a complete power management IC (PMIC) for mobile devices that use multicore application processors. The IC works well with many different series/parallel (s/p) configurations of a Li+/Li-Poly battery pack. Figure 40 shows the MAX77863 in its *Typical Application Circuit* for systems with 1s configuration batteries.

Figure 41 shows the IC in its typical applications circuit for a system with a 2s1p (two series one parallel) battery configuration. This applications circuit for systems with series battery configurations adds three components that are not shown in Figure 40: battery charger, low-I_Q LDO, and step-down regulator. A battery charger charges the series configured battery pack and generates a system voltage (V_{MBATT}) that is derived from the adapter and/or the battery pack. V_{MBATT} is regulated down to an always on voltage (AON5V0) by a low-I_Q linear regulator such as the MAX1725 or the MAX8881. AON5V0 powers the global resources of the IC through MBATT and GPIO band "A". With AON5V0 applied to MBATT, the on/off controller monitors its inputs for a wakeup event. When a wakeup event occurs, the IC begins its wakeup sequence by enabling the external step-down regulator such as the MAX15066 with GPIO2. The MAX15066 generates SD5V0 which powers all of the step-down regulators and a few of its LDOs which are required to complete the wakeup sequence. The concepts used in Figure 41 can be utilized to create solutions for 3s and 4s configurations. Other devices such as the MAX17085B, MAX17005/6, MAX17015, and MAX17020 are also good candidates for support devices in this series battery configuration.

Simplified Functional Diagram: where appropriate, further details of each functional block are shown within the dedicated chapter for that function.

Table 1 provides a regulator summary for the IC.

Table 1. Regulator Summary

	REGULATOR TOPOLOGY	MAXIMUM I_{OUT}	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	V_{OUT} RESOLUTION (mV)	OUTPUT CAPACITOR (C_{OUTX})	OUTPUT NOISE	SPECIAL FEATURES
SD0	Step-Down Regulator	8.0A Peak 6.0A Continuous	3.0 to 5.5	0.6 to 1.4	12.5	2x22µF	N/A	Differential remote output voltage sensing
		6.0A	2.6 to 3.0					
SD1	Step-Down Regulator	3.0A	3.0 to 5.5	0.6 to 1.55	12.5	22µF	N/A	Differential remote output voltage sensing
		2.5A	2.6 to 3.0					
SD2	Step-Down Regulator	2.0A	2.6 to 5.5	0.6 to 3.3875	12.5	22µF	N/A	Capable of 100% duty-cycle
SD3	Step-Down Regulator	2.0A	2.6 to 5.5	0.6 to 3.3875	12.5	22µF	N/A	• Capable of 100% duty-cycle • Three default output voltage options via pin strap (D_SD3)
LDO0	N-Channel LDO (NDRV1)	150mA	0.8 to 5.5	0.8 to 2.35	25	1.0µF	65µV$_{RMS}$	N/A
LDO1	N-Channel LDO (NDRV1)	150mA	0.8 to 5.5	0.8 to 2.35	25	1.0µF	65µV$_{RMS}$	N/A
LDO2	P-Channel LDO (PDRV1)	150mA	1.7 to 5.5	0.8 to 3.95	50	1.0µF	45µV$_{RMS}$	N/A

Table 1. Regulator Summary (continued)

	REGULATOR TOPOLOGY	MAXIMUM I_{OUT}	V_{IN} RANGE (V)	V_{OUT} RANGE (V)	V_{OUT} RESOLUTION (mV)	OUTPUT CAPACITOR (C_{OUTX})	OUTPUT NOISE	SPECIAL FEATURES
LDO3	P-Channel LDO (PDRV2)	300mA	1.7 to 5.5	0.8 to 3.95	50	2.2µF	$45\mu V_{RMS}$	N/A
LDO4	P-Channel LDO (PDRV1)	150mA	1.7 to 5.5	0.8 to 1.5875	12.5	1.0µF	$45\mu V_{RMS}$	N/A
LDO5	P-Channel LDO (PDRV1)	150mA	1.7 to 5.5	0.8 to 3.95	50	1.0µF	$45\mu V_{RMS}$	N/A
LDO6	P-Channel LDO (PDRV1)	150mA	1.7 to 5.5	0.8 to 3.95	50	1.0µF	$45\mu V_{RMS}$	N/A
LDO7	N-Channel LDO (NDRV3)	450mA	0.8 to 5.5	0.8 to 3.95	50	4.7µF	$65\mu V_{RMS}$	N/A
LDO8	N-Channel LDO (NDRV2)	300mA	0.8 to 5.5	0.8 to 3.95	50	2.2µF	$65\mu V_{RMS}$	N/A

**Output noise is proportional to output voltage. The specified noise values are for V_{OUT_LDOx} = 0.8V.*

***Quiescent supply current is the sum of the main battery current (I_{MBATT}), the step-down regulator analog input supply current (I_{AVSD}), and the regulator's power input current.*

Global Resources

The global resources encompasses a set of circuits that serve the entire device and ensures safe, consistent, and reliable operation. These resources include voltage reference, bias currents, timing references, voltage monitors, and thermal monitors. See Figure 1 for more information.

Voltage References, Bias Currents, and Timing References

Centralized voltage references, bias current, and timing references support all the functional blocks within the IC. These resources are automatically enabled when any of the peripherals functions within the device require them. The supply current associated with the minimum set of these resources make up the quiescent current (I_{Q_MBATT}).

Voltage Monitors

The MBATT undervoltage lockout (UVLO) and MBATT overvoltage lockout (OVLO) comparators force the entire device off when the supply voltage (V_{MBATT}) is not within the acceptable window of operation (2.6V to 5.5V). Similarly, the AVSD undervoltage lockout (UVLO) and AVSD overvoltage lockout (OVLO) comparators force the IC step-down regulators off when the supply voltage (V_{AVSD}) is not within the acceptable window of operation (2.6V to 5.5V). Disabling the IC when the supply is outside of its acceptable range ensures reliable consistent behavior when the supply voltage is removed/applied and it prevents overvoltage stress to the device.

In addition to the fixed threshold, UVLO and OVLO comparators and adjustable threshold low-battery monitor monitors the battery voltage through the MON input and provides the system with a signal that the main-battery is low through a MBATTLOW status bit and MBATTLOW_R interrupt bit. When $V_{MON} < V_{MONL}$, MBATTLOW is 1. The main-battery low signal is also available through the nRST_IO signal when LBRSTEN = 1. With all peripheral blocks of the IC disabled, the quiescent current of the device is 12µA (I_{Q_MBATT}). The “low-battery” comparator's threshold and hysteresis are register programmable.

For a single-cell (i.e., 1s) battery configuration (Figure 40), MON is intended to connect directly to the MBATT pin externally. For multi-cell (i.e., 2s, 3s, 4s) configurations (Figure 41), MON is intended to connect to the main system power source (i.e., battery or system node) through a resistive divider. Although V_{MON} can independently swing from -0.3V to +6.0V, systems should be designed such that V_{MON} is less than or equal to MBATT.

Example 1: Setting the low-battery cutoff threshold to 5.6V and the battery valid threshold to 6.0V for a 2s battery configuration

- A system with two series batteries has a maximum charge voltage of 8.4V and a low battery cutoff voltage of 5.6V (i.e., 2.8V per cell). A 400mV hysteresis is desired before the system recognizes the battery as valid.
- The LBDAC[2:0] = 0b001 setting is chosen (2.8V) to get a falling cutoff voltage of 5.6V for the two series cell battery configuration.
- The LBHSYT[1:0] = 0b01 setting is chosen (200mV) to get 400mV of hysteresis (i.e., 200mV per cell) and a battery valid threshold of 6.0V.
- A divide-by-two resistive divider using two 402kΩ resistors is used from the system voltage (either battery or adapter) to ground with the center tap connected at MON. The low MON bias current (I_{MON}) allows for the use of a large resistor to minimize the drain on the system. Limiting the top of the resistive divider to < 402kΩ limits the total error due to bias current to 50mV. When using high-impedance resistive dividers, make sure to isolate them from noise sources in the PCB layout.

Example 2: Optimizing the low-battery threshold and hysteresis

The default low-battery threshold is 3.0V falling with 200mV hysteresis. A system with a low battery cannot start until its battery has charged above 3.2V.

The following bullet points give some examples of situations where the low-battery falling threshold (V_{MONL}) can be optimized:

- Some systems may need to choose the low-battery threshold based on step-down regulator dropout: Consider the case where an 800mAh battery supports a system where the highest step-down regulator output voltage is 2.8V, the step-down regulator output can be prevented from going into dropout by setting the low-battery threshold to **3.0V falling**. This assumes that 200mV (3.2V-3.0V) is sufficient for the step-down regulator to stay out of dropout.
- Some systems may need to choose the low-battery threshold based on the battery capacity: Consider the case where a 2000mAh battery supports a system where the highest step-down regulator output voltage is 2.5V, then the step-down regulator dropout is not an issue because the valid battery operating range is from 2.6V to 5.5V. However, it could be possible that the battery capacity is not enough to support the system when the voltage is lower than 2.9V. In this situation, the low-battery threshold would be set for **2.9V falling**.
- Some systems may need to choose the low-battery threshold based on backup time: Consider the case where a 2000mAh battery supports a system where the highest step-down regulator output voltage is 2.5V (no dropout issues), the battery can support the system when the voltage is down to 2.7V (no capacity issues), but the system must have a backup time of one year. In this case, the low-battery threshold must be set sufficiently high so that the main battery has enough capacity to support the system in its backup mode for one year. In a situation like this, the low-battery threshold may be set to **3.3V falling**.

The V_{MONL} hysteresis (V_{LBHYST}) is configurable using LHYST[1:0]. Choose V_{LBHYST} based on your system peak currents and battery impedance. Set V_{LBHYST} sufficiently high to avoid oscillation in and out of the low-battery state due to system peak currents.

- For example, consider a system that has maximum peak currents of 1A with an internal battery impedance of 100mΩ, a connector impedance of 50mΩ, and a fuse impedance of 50mΩ. The total impedance of 200mΩ combined with the 1A peak currents results in the battery voltage varying by 200mV. In this case, V_{LBHYST} needs to be set to 300mV (>200mV).

Example 3: Charging a dead battery with a 3.0V falling threshold and 200mV of hysteresis.

- A device with a 2.5V battery is off and does not start when the user presses the “on key” because the battery is too low. The user plugs the device into the charger and presses the “on key” to find out that it still does not start because the battery voltage is too low. Three minutes later, the battery voltage rises above 3.2V and the device starts up with no user intervention.

Thermal Monitors

Several on-chip thermal sensors force the IC to shut down if the junction temperature exceeds 165°C (T_{JSHDN}). In addition to the 165°C shutdown threshold, these thermal sensors also provide interrupts when the temperature exceeds 120°C (thermal alarm 1) and 140°C (thermal alarm 2).

Bidirectional Reset Input/Output

The MAX77863 has a bidirectional, active-low, open-drain, reset input/output (nRST_IO) as shown in Figure 1. The RSO signal within the bidirectional reset IO logic in Figure 1 is asserted by the IC when it needs to drive nRST_IO low. If the IC is not driving nRST_IO low (i.e., RSO is low), and an external device such as a reset button (Figure 1) pulls nRST_IO low, then the RSI signal within the bidirectional reset IO logic is asserted. If RSI is asserted for longer than t_{DBNC}, then a global shutdown event is triggered (GLBALSHDN). A global shutdown due to RSI is recorded in the NVERC register such that when the system's microprocessor recovers from the reset it can recognize that the cause of the power down was due to RSI. If a global shutdown event is triggered by RSI, then the IC automatically generates a wakeup event after the global shutdown event has completed. See the *Global Shutdown* section for more information.

The reset output is a programmable slave to the flexible power sequencer. Allowing the RSO to respond to the flexible power sequencer gives it the capability to drive the nRST_IO line low as the first action in the power down sequence (Figure 26). The FPS_RSO register configures how nRST_IO behaves with respect to the flexible power sequencer.

Once all conditions for allowing the reset output to go high-impedance have been met, a reset delay timer is initiated before RSO is deasserted (t_{RST_O}).

The following bulleted list summarizes all the conditions required for the MAX77863 to set RSO low and allow nRST_IO to go high-impedance.

- The IC must not be in a global shutdown state. See the *Global Shutdown* section for more information.
- The low-battery monitor must be satisfied (V_{MON} > V_{MONL}) if LBRSTEN is set. See the *Voltage Monitors* section for more information.
- The 32kHz oscillator must be stable (32K_OK). See the *32kHz Crystal Oscillator and Buffered Outputs* section for more information.
- The flexible power sequencer (FPS_RSO) must be satisfied.
- Reset timer has expired (t_{RST_O}).

An example configuration that allows nRST_IO to go high-impedance is:

- No global shutdown events.
- The main-battery voltage is within the valid region.
- The 32kHz clock is stable.
- FPS0 (flexible power sequencer 0) has gotten past power up cycle 5 (FSO_RSO).
- t_{RST_O} expired.
- No external device such as a reset button (Figure 40) are pulling nRST_IO low.

Global Shutdown

This document uses the term "global shutdown" to refer to any event that causes a shutdown of all regulators and a reset for most of the registers within the IC. The NVERC register records the source of a "global shutdown" event. Figure 4 shows the global shutdown state machine. Figure 5 is the simplified logic diagram for the global shutdown. Figure 6 and Figure 7 shows the simplified timing diagram for the global shutdown events. In addition to the state machine, the various conditions that causes a global shutdown are also shown in the bulleted list below:

- Reset input (i.e., RSI event)
  - nRST_IO externally pulled low for t_{DBNC} after RSO is deasserted.
- Software Reset (i.e., SFT_RST event)
  - SFT_RST bit is set.
- Main-Battery Undervoltage ($V_{MBATT} < V_{MBATTUVLO}$)
- Main-Battery Low when MBLPD is set ($V_{MON} < V_{MONL}$)
- Overvoltage ($V_{MBATT} > V_{MBATTOVLO}$ or $V_{AVSD} > V_{MBATTOVLO}$)
- Thermal Overload ($T_J > T_{JSHDN}$)
- Manual Reset
  - EN0 low for more than the time programmed by MRT[2:0] and MREN is set.
- System Watchdog Timeout
- SHDN Pin
- PWR_OFF Bit

After a global shutdown occurs, the device may be powered up normally as long as the main-battery voltage and the die temperature are within their valid ranges. Although all regulators are forced off in response to a global shutdown, the RTC remains powered and continues to record the calendar.

From any state there are three ways of implementing a "global shutdown". The source of the global shutdown event determines how the global shutdown is implemented and is described as follows.

Global Shutdown Events with Sequenced Shutdown and Automatic Wakeup

As shown in Figure 4, three events initiate "sequenced global shutdown and automatic wakeup." The events in this category are associated with faulty system states where the software may not be working properly but the system could potentially recover by powering down the microprocessor, resetting all the "global shutdown" registers, and then powering up the microprocessor again.

Global Shutdown Events with Sequenced Shutdown to the Off State

As shown in Figure 4, five events initiate "sequenced global shutdown to the off state." With the exception of PWR_OFF which is a normal system function, the events in this category are associated with undesirable system states that may occur in a "normally" functioning product. Powering down the microprocessor and resetting all the "global shutdown" registers helps the system resolve these undesirable events. In general, a wakeup event such as an on-key press is required to power up the microprocessor again.

In the case of a software reset input (SFT_RST) with SFT_RST_WK = 0, the global shutdown state machine results in the "default state" with the device off and waiting for a wakeup event. It is possible for the system software to program a wakeup event based on an RTC alarm. For example, once the state machine lands in the "default state" it waits there until the RTC alarm generates the wakeup event.

Global Shutdown Events with Immediate Shutdown

As shown in Figure 4, five events initiate an "immediate shutdown." The events in this category are associated with potentially hazardous system events. Powering down the microprocessor and resetting all the IC registers helps mitigate any issues that can occur due to these potentially hazardous system events.

Global Low-Power Mode

All step-down regulators, linear regulators, and the 32kHz oscillator have low-power modes. Each block containing low-power mode allows for the power mode to be controlled individually or for the power mode to be controlled globally with the global low-power mode bit (GLBL_LPM), or GPIO0 when it is set in its alternative mode, or the EN1 hardware input. See Figure 8 for the simplified logic.

For the step-down regulators, the power modes are configured with PWR_MD_SDx[1:0]. For the linear regulators, the power modes are configured with PWR_MD_Lx[1:0]. The 32kHz oscillator power mode is configured with PWR_MD_32K[1:0]. When any of these power mode bits are programmed to 0b01 (PWR_MD_xx[1:0] = 0b01), the given peripheral are in low-power mode.

The logic shown in Figure 8 allows EN1 to control the low-power mode bus (LPM_BUS). With LPM_BUS = 1, any peripheral (32kHz oscillator (OSC), linear regulator (LDO), or step-down regulator (SD)) with its power mode bits programmed to 0b01 (PWR_MD_xx[1:0] = 0b01) are in low-power mode when LPM_BUS = 1.

When the IC is asserting its reset output (RSO = 1), the EN1 signal cannot control the active-low sleep mode signal (i.e., EN1_LPM is forced low). However, if the IC is not asserting RSO and the low-power mode during sleep mask bit (nSLP_LPM_MSK) is clear, the EN1 signal can affect EN1_LPM and LPM_BUS.

Logic

The IC includes an I2C interface as well as several other logic signals. All logic level specifications for the IC are consolidated within the "Logic" section of the *Electrical Characteristics* table.

Status and Interrupts

The IC contains several status, interrupt, and interrupt mask registers. Table 2 shows the various register types within the IC along with a brief description. Figure 2 shows the simplified interrupt, status, and mask logic for the entire device; see each section for more information. Status, interrupt, and interrupt mask functions are typically provided in a block of three registers and register blocks are typically associated with a single device function.

An elegant interrupt structure design minimizes processor time. This structure allows the applications processor to quickly find the interrupt of interest. It achieves this through a top-level interrupt register that sub-divides the interrupt sources into eight different categories.

Figure 3 provides a guideline for processing the interrupt information. The following bulleted list reviews the basic details of this diagram:

- The starting point is that the processor is powered but it could be in normal operating mode or sleep mode and its global interrupt is unmasked.
- Upon the interrupt hardware line going low (nIRQ = 0), the software is switched to the priority decoder which decides in what order all interrupts to the processor are serviced and therefore, transfers control to the PMIC interrupt service routine appropriately.

- The first task for the processor is to mask the PMIC interrupt by setting GLBLM (not to be confused with IRQ_GLBLM).
  - This forces nIRQ to go high-impedance in which case it is pulled high by the external pullup resistor.
  - Forcing nIRQ to go high-impedance ensures that any interrupts that occur within the PMIC while the PMIC interrupt service routine is being executed causes a subsequent falling edge on the processor interrupt line.
- The next task is to read the IRQTOP register and maintain a local copy. Note that IRQTOP is cleared when read.
- Based on the value of the IRQTOP register, the service routing branches to individual functions that service interrupts from each of the PMIC sub-blocks.
  - Note that at this point, subsequent interrupts that occur on the PMIC are masked from reaching the processor. They are however, not lost since they are stored on the local interrupt registers and global interrupt register on the PMIC.
- Once all interrupts have been checked and serviced, the interrupt service routine unmasks the hardware interrupt line by clearing GLBLM (not to be confused with IRQ_GLBLM).
  - If any interrupts occurred on the PMIC during the process of servicing the PMIC interrupts, and these interrupts are unmasked, the nIRQ line now gets pulled low causing an interrupt on the processor. The process now repeats.

The above bulleted list reviews the basic details of Figure 3. The following bulleted list is of second-level interrupt service routine concerns:

- If an additional PMIC sub-block interrupt occurs after the top level interrupt register (IRQTOP) has been read but prior to the sub-block being serviced, it is serviced in the routine although it did not cause the original interrupt.
  - For example, if GPIO0 rising edge caused the original interrupt but GPIO1 had a rising edge before the GPIO sub-block's interrupts were serviced, both GPIO0 and GPIO1 interrupts would get serviced.
- If an additional PMIC sub-block interrupt occurs after the top level interrupt register (IRQTOP) has been read and after the sub-block being serviced, it is serviced the next time the interrupt service routine is called.
  - Using the same example, if GPIO1 has a rising edge subsequent to the GPIO sub-block being serviced, it gets stored in the GPIO block interrupt flag and in the global interrupt register (IRQTOP) which then causes an interrupt once GLBLM is unmasked.
- If a PMIC sub-block that did not cause an interrupt has an interrupt while the interrupt service routine is being executed (due to another sub-block), it gets stored and serviced the next time the routine is called.
  - For example, if the service routine was called due to the GPIO sub-block but the RTC sub-block has an interrupt while the service routine is being executed, it gets stored in its local interrupt flag (RTCINT) and the bit in the top level interrupt register (IRQTOP) also gets set. This subsequently causes an interrupt when GLBLM is unmasked after the present interrupt service routine has completed.

Table 2. Register Type Description

REGISTER TYPES	DESCRIPTION
Interrupt	Interrupt registers are read only and provide indications that a particular event has occurred. When an interrupt event has occurred, the corresponding bit is set in the interrupt register. Each interrupt event has a corresponding interrupt mask that determines whether an interrupt event affects the hardware interrupt output. Interrupt registers are cleared when read.
Interrupt Mask	Interrupt mask registers allow for preventing (masking) an interrupt event from affecting the hardware interrupt output. Note that the interrupt mask settings have no effect on the interrupt registers. If an interrupt mask is set, then when an interrupt event happens it does not get reported on the hardware interrupt output, however, that interrupt is still reported in the interrupt register.
Status	Status registers are read only and reflect the actual condition of a particular event or input.
Data	Data registers provide information. One example is the RTCs minutes register (RTCMIN).
Configuration	Configuration registers allow for the adjustment of device parameters.

System Watchdog Timer

The IC contains a system watchdog timer to ensure safe and reliable operation. The system watchdog timer prevents the device from powering a system in the event that the system controller hangs or otherwise isn't communicating correctly. The default state of the system watchdog timer enable bit (WDTEN) can be factory programmed with an OTP bit (OTP_WDTED). To use the watchdog timer feature, enable the feature by setting WDTEN. While enabled, the system controller must reset the system watchdog timer within the timer period (t_{WD}) for the charger to operate normally. Reset the system watchdog timer by programming WDTC[1:0] = 0b01. t_{WD} is programmable from 2s to 128s with TWD[1:0].

With WDTEN set, an internal counter is incremented with the internal oscillator. When the internal counter matches a value programmed by TWD[1:0], the IC asserts nRST_IO, powers down all of its regulators with a global shutdown condition, and sets the WDT bit in the nonvolatile event recorder.

To prevent the system watchdog timer from initiating a global shutdown event and disabling the IC, a properly operating processor clears the system watchdog timer within the timer period programmed by TWD[1:0]. The system watchdog timer is cleared by setting WDTC[1:0] = 0b01. See the *Global Shutdown* section for more information.

The system watchdog timer can be set to automatically clear when the AP enters its sleep or off states. The device interprets the AP sleep state as FPS1 is being disabled. The device interprets the off state as FPS1 and FPS2 being disabled.

Note that the IC contains both a system watchdog timer and an I^2C watchdog timer. See the *I^2C Watchdog Timer* section for more information.

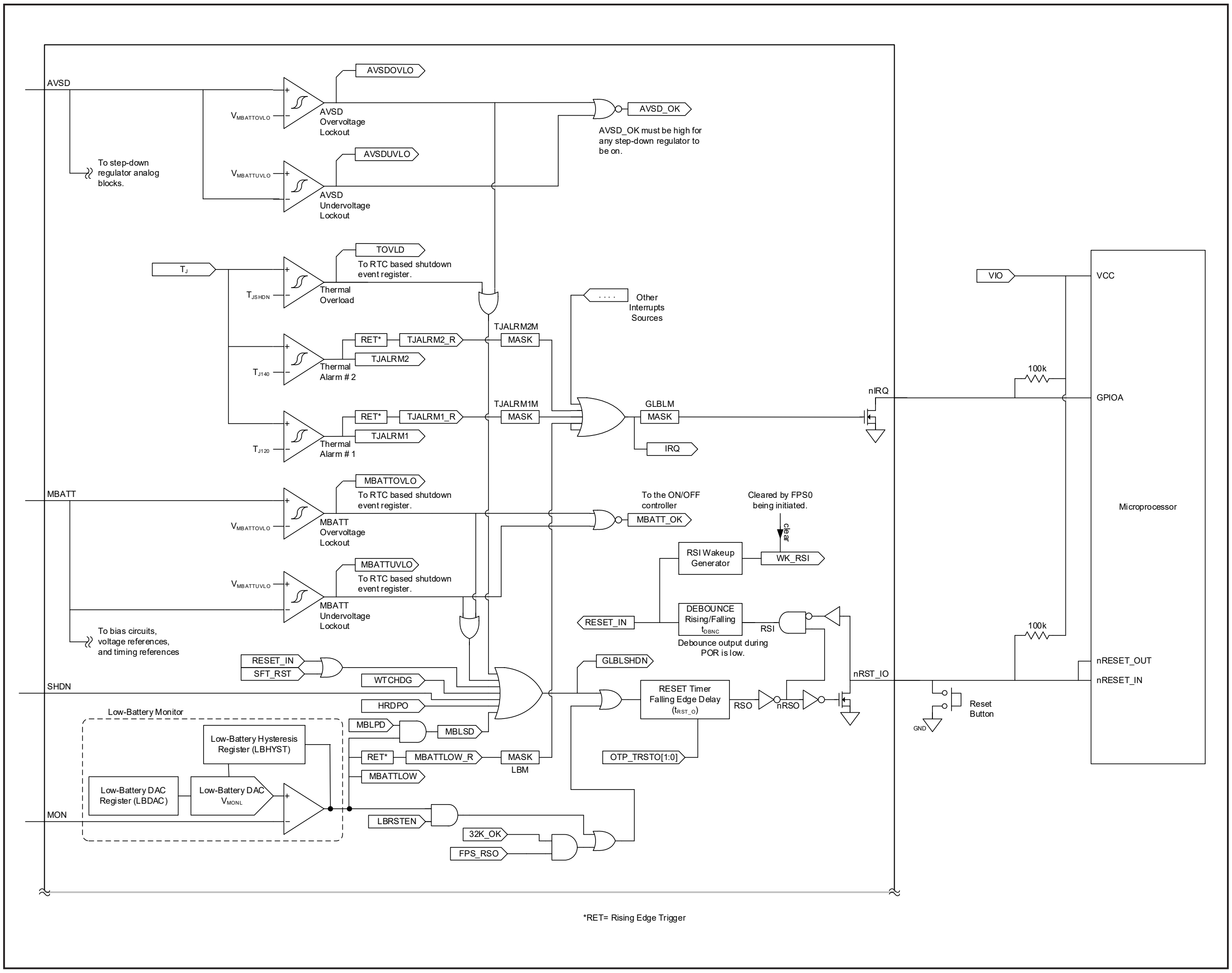


Figure 1. Global Resource Logic

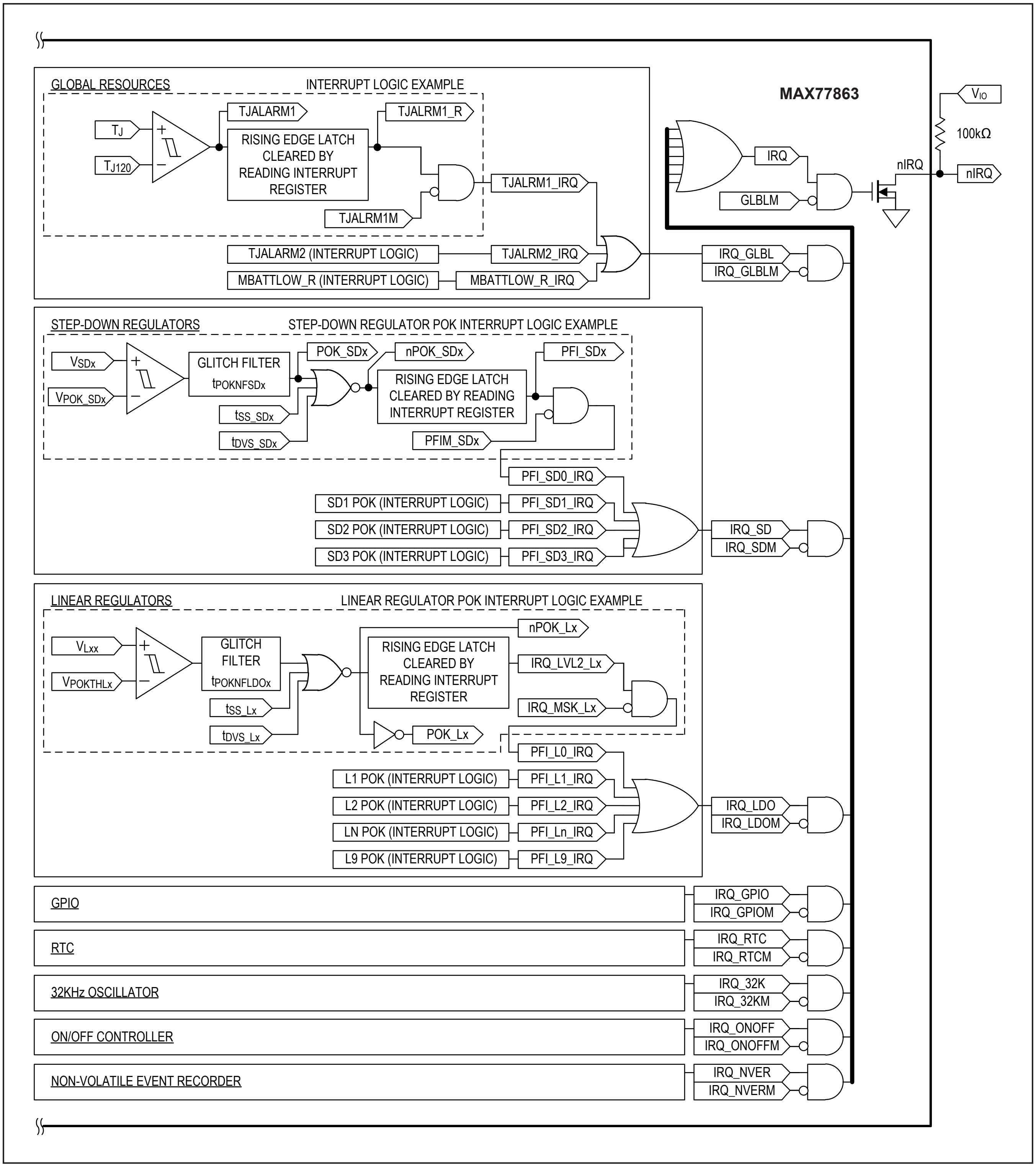


Figure 2. Simplified Interrupt, Status, and Mask Logic

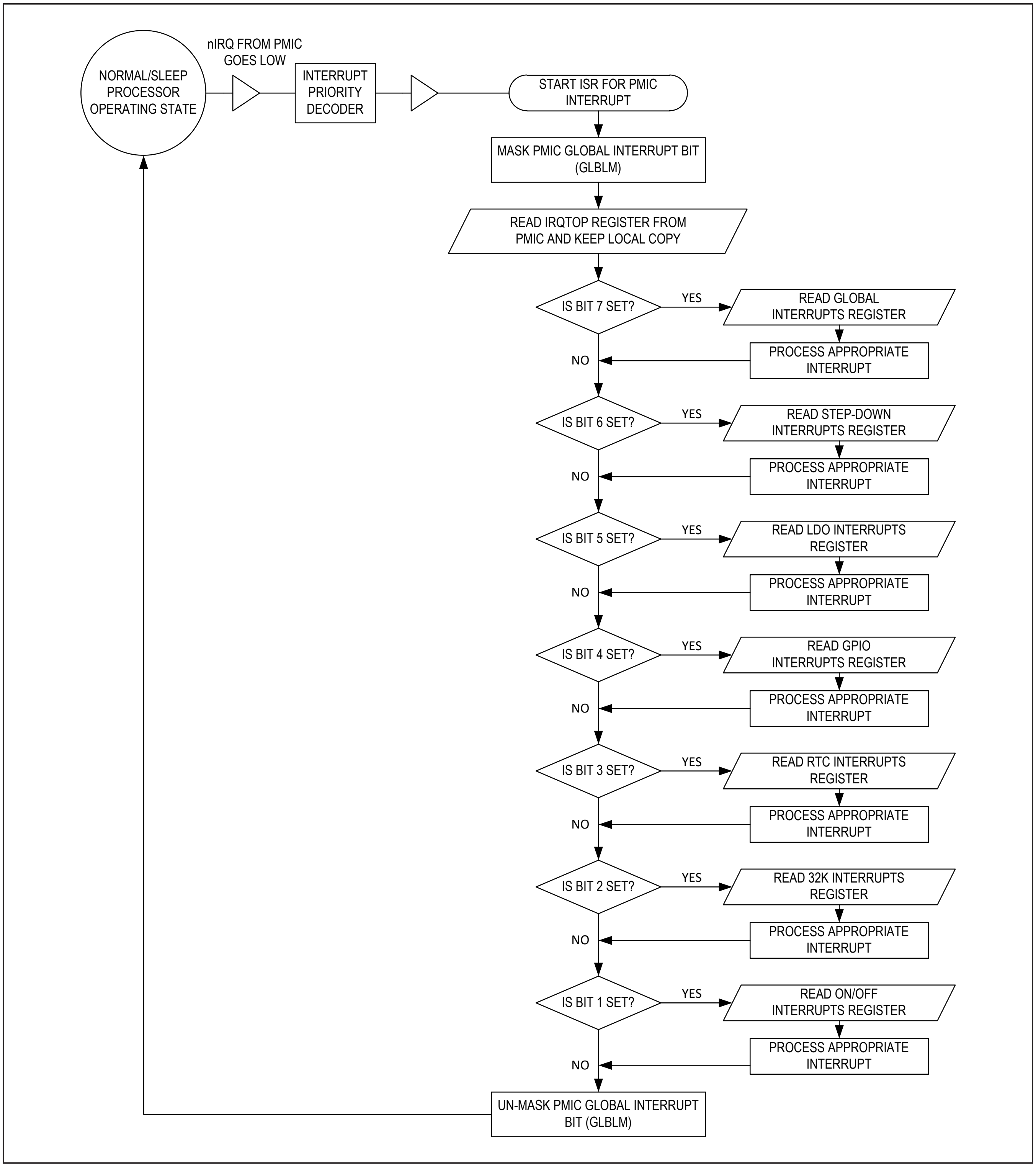


Figure 3. Interrupt Service Routine Example

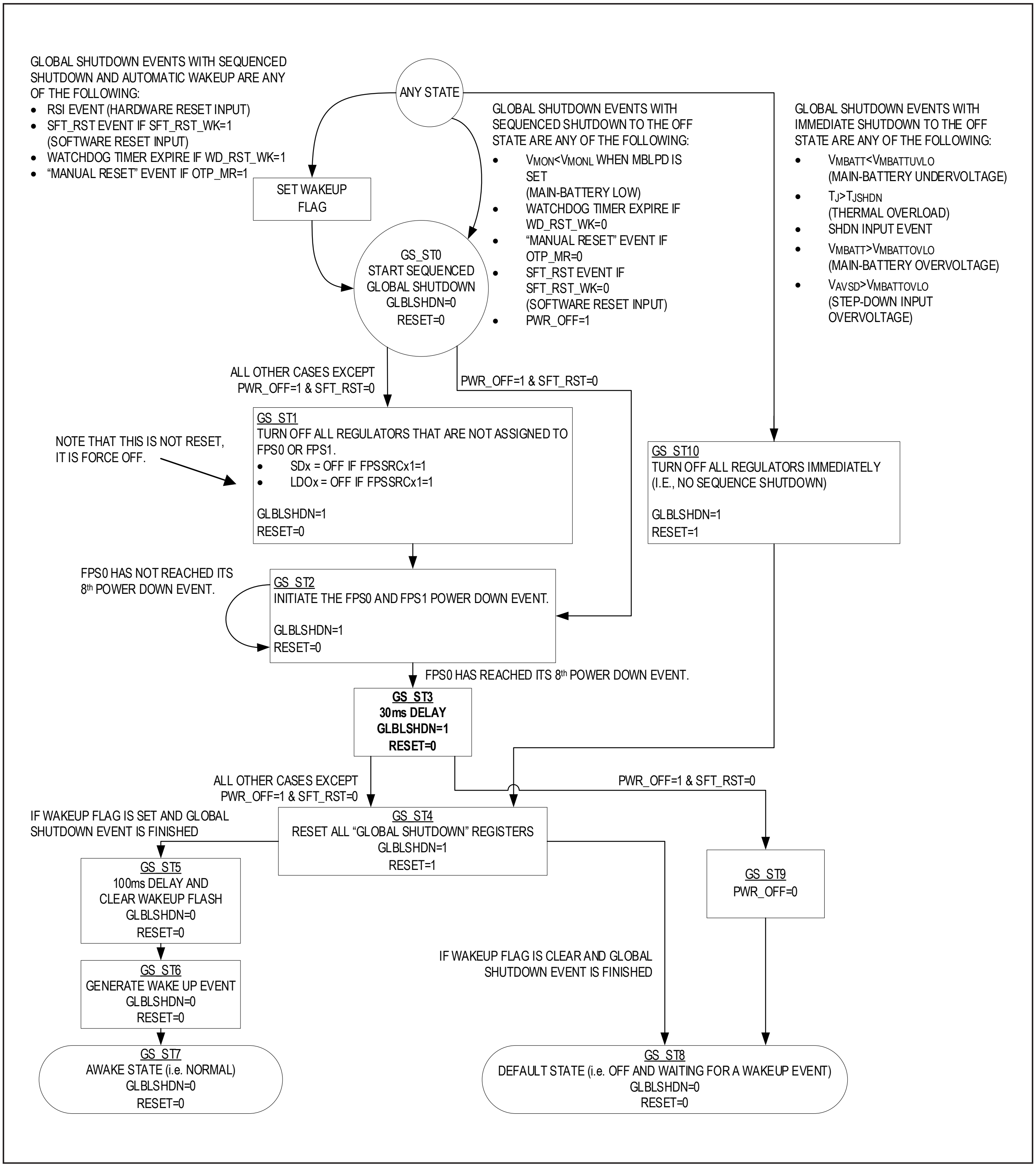


Figure 4. Global Shutdown State Diagram

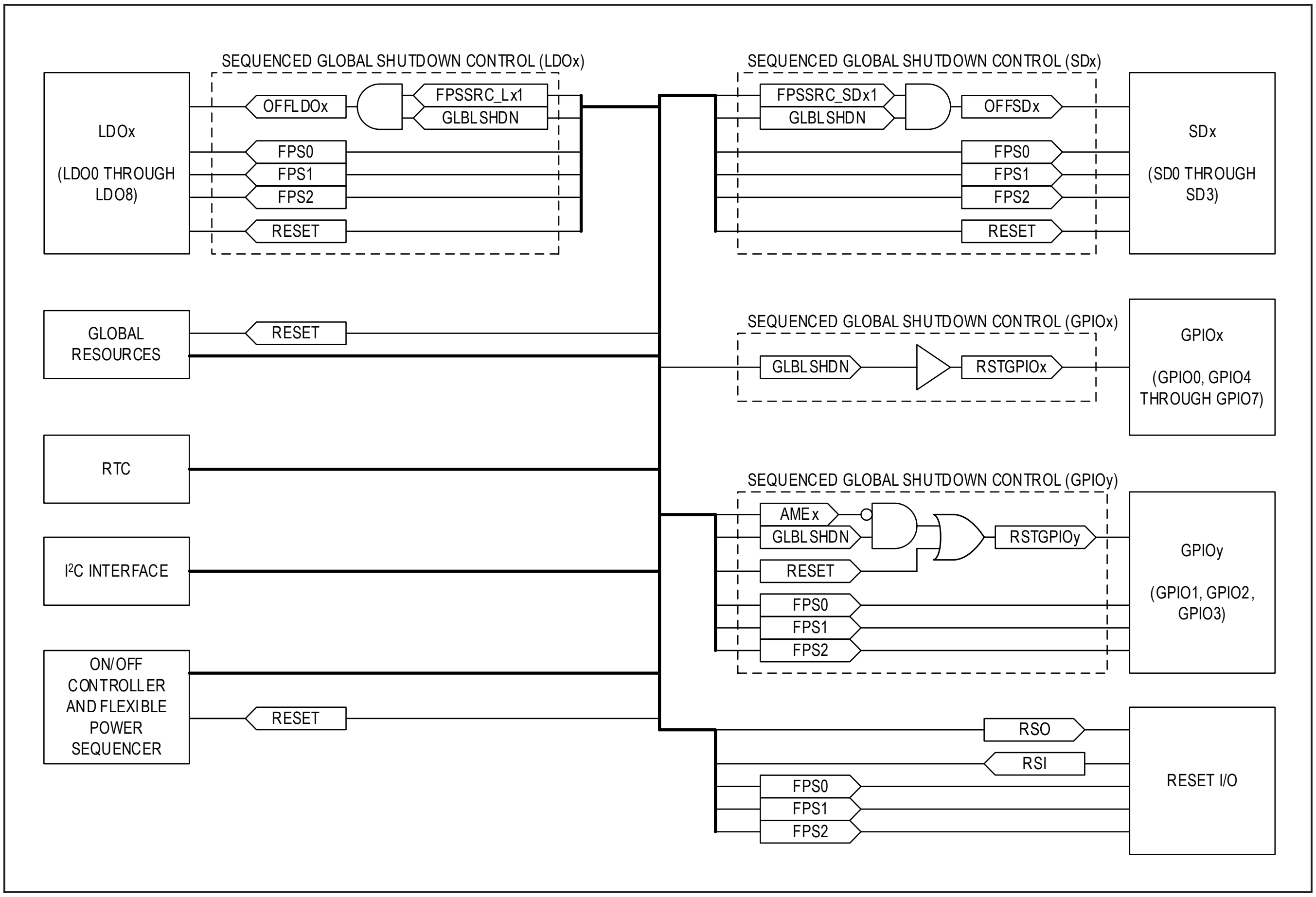


Figure 5. Simplified Logic for Global Shutdown

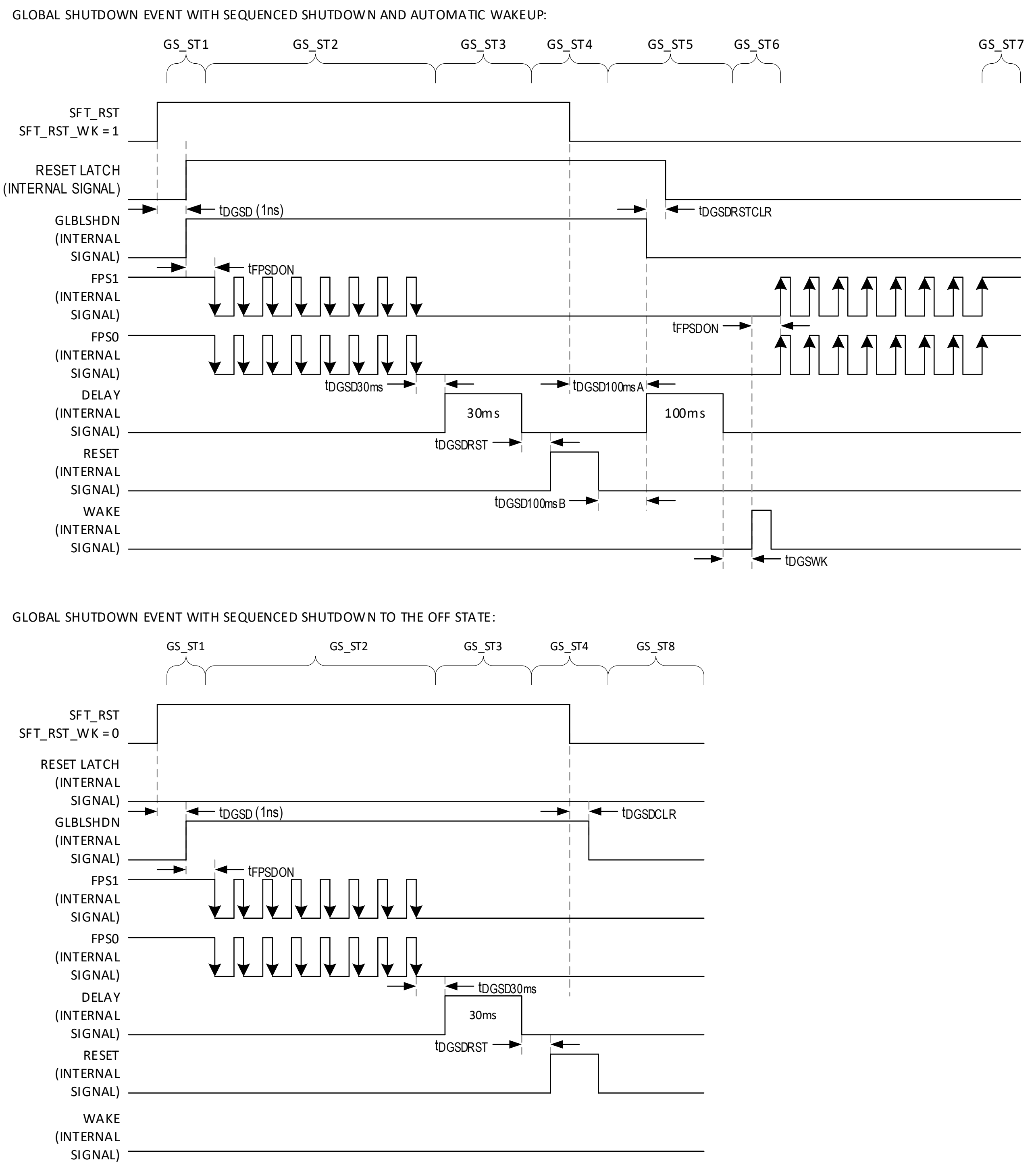


Figure 6. Simplified Timing Diagram for Global Shutdown

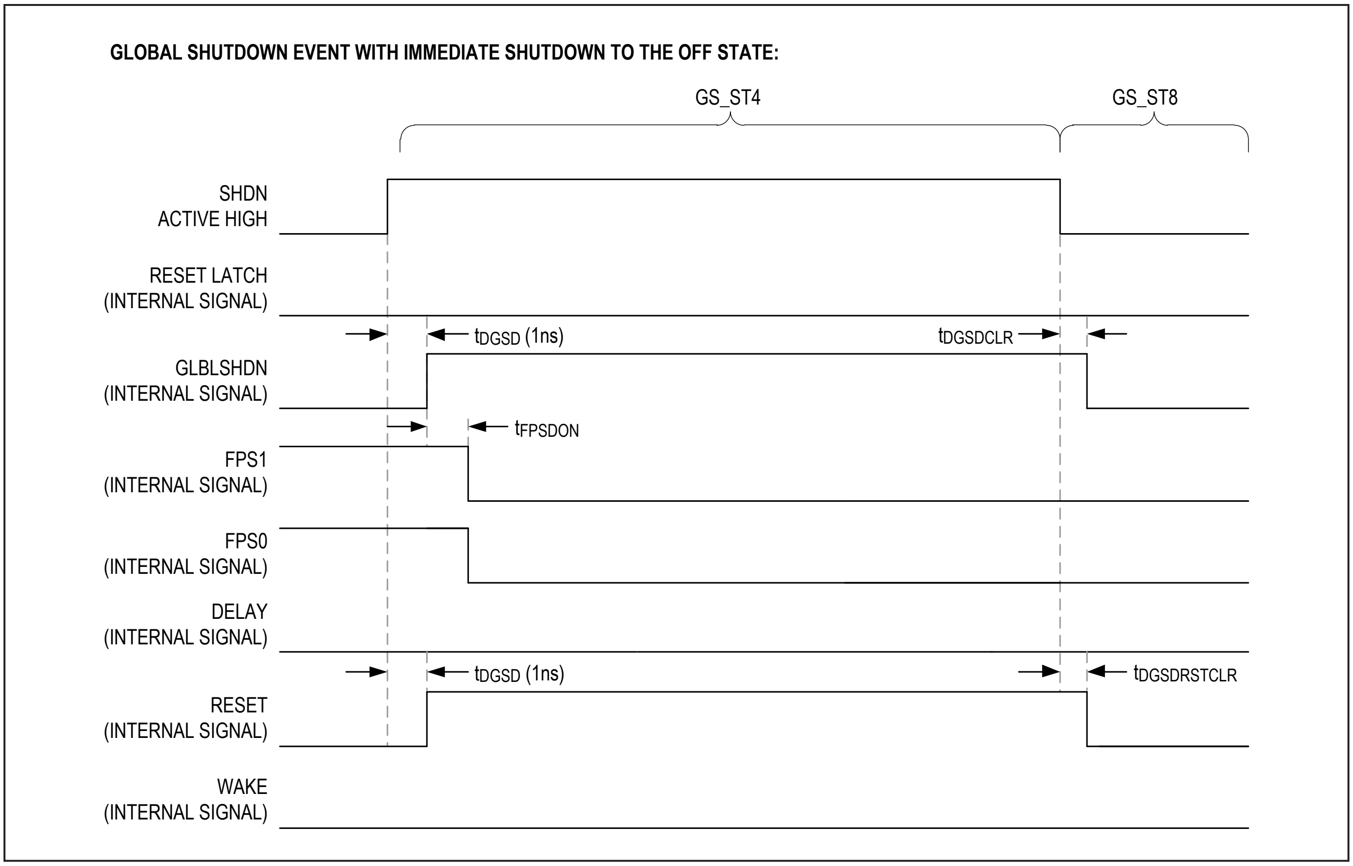


Figure 7. Simplified Timing Diagram for Global Shutdown

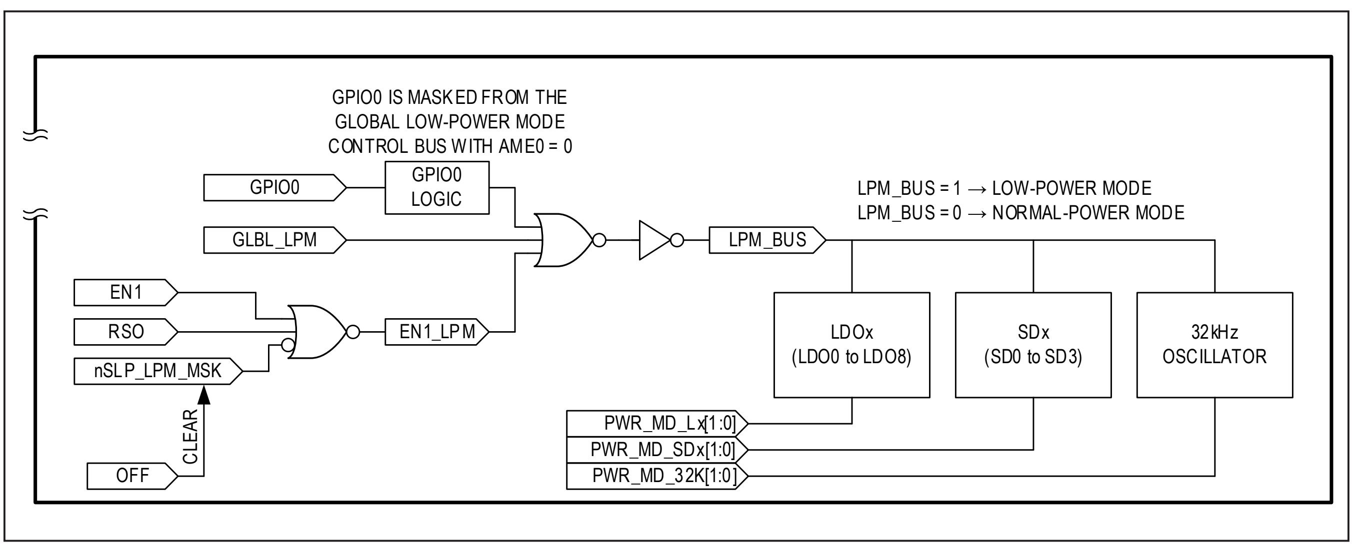


Figure 8. Simplified Logic for Global Low-Power Mode

Step-Down Regulators

The IC features four ultra-low I_Q step-down regulators (SD0, SD1, SD2, SD3). Table 1 summarizes the basic characteristics of the step-down regulators in addition to the other regulators on the device. Figure 40 shows the external component values for the step-down regulators. Figure 2 shows a *Simplified Functional Diagram* of the step-down regulators.

In normal operation, these step-down regulators consume only 16μA of quiescent current except for SD0 which consumes 32μA. In standby mode, the quiescent current is reduced to 5μA per step-down regulator, with reduced load capability (10μA for SD0). Each step-down regulator can be independently put into standby mode by writing a bit in a control register.

Each step-down regulator features internal feedback, minimizing external component count by allowing all step-down regulator output voltages to be programmed through the serial interface. A 4.4MHz switching frequency minimizes the external component size. All step-down regulators feature dynamic voltage scaling (DVS) through the I^2C serial interface. Additionally, all step-down regulators automatically transition from PFM to PWM operation (FPWM_SDx = 0). Forced PWM operation can be independently enabled for each step-down regulator by setting FPWM_SDx.

SD1 and SD3 switching is interleaved to minimize the input capacitance requirement. Each phase of SD0 are also interleaved. SD2 switching is independent of the other step-down regulators

Features

- 16μA quiescent current in normal mode (SD1, SD2, SD3)
- 25μA quiescent current in normal mode (SD0)
- 5μA quiescent current in low-power mode (SD1, SD2, SD3)
- 10μA quiescent current in low-power mode (SD0)
- Four step-down regulators
  - SD0: 6.0A continuous, 8.0A peak
  - SD1: 3.0A
  - SD2: 2.0A
  - SD3: 2.0A
- 100% duty-cycle operation for SD2 and SD3
- No external MOSFETs, synchronous rectifiers, or current sense resistors are required
- Dynamically programmable output voltage
- Programmable output voltage slew rate during dynamic voltage changes.
- Low-power mode Increases light-load efficiency
- Forced PWM operation selectable through serial interface
- Remote output voltage sensing (SD0, SD1)
- ±1% steady-state accuracy and ±5% transient accuracy (SD0, SD1)
- Power-OK interrupt
- Soft-start into prebiased output

Efficiency

The typical efficiencies for the IC step-down regulators are shown in the *Typical Operating Characteristics* section. Note that the inductors used to get the efficiency shown are physically small and therefore the ESR is high. Physically larger inductors achieve efficiencies that are 1 to 3% higher than what is shown.

Step-Down Regulator Input Voltage Range

All step-down regulators share a single analog power input (AVSD). Additionally, each step-down regulator has a dedicated power input that is connected to the source of its high-side p-channel MOSFET (INy_SDx) as shown in the *Simplified Functional Diagram*. All INy_SDx pins and AVSD must be connected together. For applications with 1s battery configurations, typically AVSD, INY_SDx, MBATT, and MON are connected together (Figure 40). For applications with 2s (or higher) battery configurations, INy_SDx and AVSD can be connected to an external step-down regulator as shown in Figure 41.

The valid operating input voltage range for AVSD and INy_SDx is 2.6V to 5.5V. AVSD undervoltage lockout (UVLO) and AVSD overvoltage lockout (OVLO) comparators force the MAX77863 step-down regulators off when the supply voltage (VAVSD) is not within the acceptable window of operation (2.6V to 5.5V). See Figure 1 and the *Voltage Monitors* section for more information.

SD0 is capable of operating across the full AVSD and INy_SDx range of 2.6V to 5.5V. The peak output current of 8.0A is guaranteed only for AVSD and INy_SDx greater than 3.0V. From 2.6V to 3.0V, the rated output current derates to 6.0A.

Buck Regulator Control Scheme

The step-down converter uses a PWM peak current-mode control scheme with a high-gain architecture. Peak current mode control provides precise control of the inductor current on a cycle-by-cycle basis and inherent compensation for supply voltage variation. On-times (MOSFET Q1 on) are started by a fixed-frequency clock and terminated by a PWM comparator. See Figure 9. When an on-time ends (starting an off-time) current conducts through the low-side MOSFET (Q2 on). Shoot-through current from IN_SDx to PG_SDx is avoided by introducing a brief period of dead time between switching events when neither MOSFET is on. Inductor current conducts through Q2's intrinsic body diode during dead time. The PWM comparator regulates VOUT by controlling duty cycle. The negative input of the PWM comparator is a voltage proportional to the actual output voltage error. The positive input is the sum of the current-sense signal through MOSFET Q1 and a slope-compensation ramp. The PWM comparator ends an on-time when the error voltage becomes less than the slope-compensated current-sense signal. On-times begin again due to a fixed-frequency clock pulse. The controller's compensation components and current-sense circuits are integrated. This reduces the risk of routing sensitive control signals on the PCB. A high-gain architecture is present in the controller design. The feedback uses an integrator to eliminate steady-state output voltage error while the converter is conducting heavy loads.

Step-Down Regulator Power Modes

Step-down regulators and linear regulators have very similar power mode controls. Each step-down regulator is independently controlled with PWR_MD_SDx[1:0] and each linear regulator is independently controlled with PWR_MD_Lx[1:0] (see the *Linear Regulator* section for more information). In addition, to enable and disable control, each step-down regulator has a special low-power mode that reduced the quiescent current to 5μA for SD1-SD2 and 10μA for SD0. In low-power mode, each regulator supports a load of up to 5mA (IMAX_SDx). Remote output voltage sensing (ROVS) is disabled in low-power mode and the load regulation performance degrades proportionally with the reduced load current.

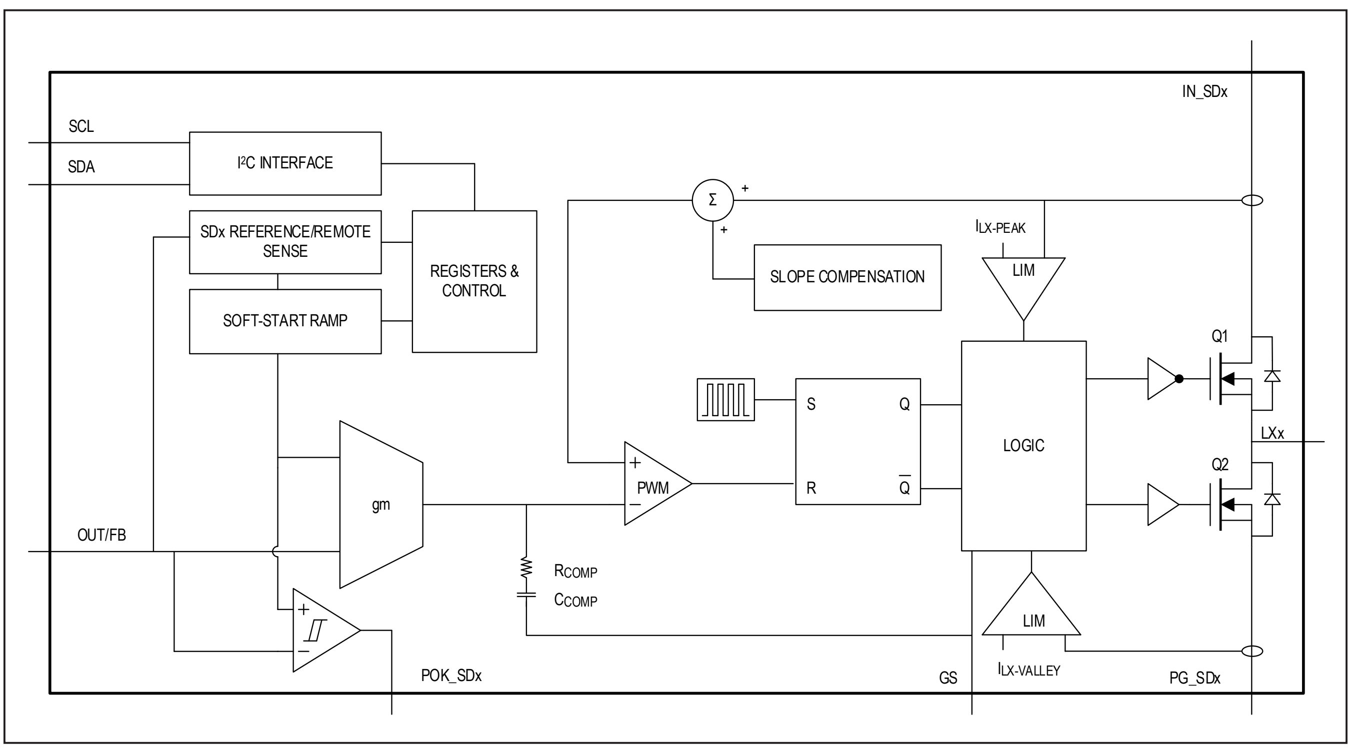


Figure 9. Buck Control Scheme Diagram

Several usage options are available for low-power mode. To force individual regulators to low-power mode, set PWR_MD_SDx to 0b10. To force a group of regulators to enter and exit low-power mode in unison, set their individual PWR_MD_SDx_ bits to 0b10. When set for this "group and/or dynamic" low-power mode, the low-power mode is enabled when the global low-power mode signal is high. The global low-power mode signal is driven by the GLBL_LPM bit or though GPIO0 (see the *Global Low-Power Mode* section for more information).

When a step-down regulator is configured to be part of a flexible power sequence (FPSSRC_SDx), the power mode bits (PWR_MD_SDx) are still used to configure low-power mode and normal-power mode, but the flexible power sequencer itself controls weather the regulator is enabled or disabled. See the Step-Down Regulator Configuration—Register 1 table for complete information on PWR_MD_SDx[1:0] bit descriptions.

SD0 is unique in that it has a hardware enable pin called EN2. When EN2 is high, SD0 is enabled. See the Step-Down Regulator Configuration—Register 1 table for PWR_MD_SDx[1:0] bit descriptions and Table 9 for the full details.

Output Voltage Settings

SD2 and SD3 are independently programmable from 0.6V to 3.3875V in 12.5mV increments. SD0 is programmable from 0.6V to 1.4V in 12.5mV increments. SD1 is programmable from 0.6V to 1.55V in 12.5mV increments. The main target voltage registers are programmed with VSDx[7:0]. The DVS registers for SD0 and SD1 are programmed with VDVSSDx[7:0].

Output Current

The output current rating of each step-down regulator are slightly conservative numbers based on the typical application for the devices:

- SD0: 6.0A continous, 8.0A peak
- SD1: 3.0A
- SD2: 2.0A
- SD3: 2.0A

These output current ratings vary with output voltage setting, inductor, switching frequency, and device current limits.

Soft-Start

The step-down regulators have an OTP programmable (OTP_SD_SS) soft-start rate of either 25mV/µs or 12.5mV/µs. The controlled soft-start rate and the step-down regulator current limit (I_{LIMP}) limit the input inrush current to the output capacitor (I_{INRUSH}). I_{INRUSH} = min (I_{LIMP} & C_{OUT} x dV/dt). Note that the input current on the step-down converter is lower than the inrush current to the output capacitor by the ratio of output to input voltage.

The step-down regulators support starting into a pre-biased output. For example, if the output capacitor has an initial voltage of 0.4V when the regulator is enabled, the regulator gracefully increases the capacitor voltage to the required target voltage such as 1.2V. This is unlike other regulators without the start into prebias feature where they may force the output capacitor voltage to 0V before the soft-start ramp begins.

During the soft-start period, the POK comparator is masked to prevent false POK interrupts.

Example 4: What is the inrush current when starting SD0 with an output capacitance (C_{OUT}) of 100µF?

- I_{INRUSH} = min(I_{LIMP} and C_{OUT} x dV/dt)
- SD0 is a two-phase regulator with a high PMOS current limit (I_{LIMPP_HIGH0}) of 4.4A per phase. For I_{LIMP} in the above equation we use 2 x 4.4A = 8.8A.
- SD0 has a typical soft-start rate (dV/dt_SS_SD0) of 25mV/µs when OTP_SD_SS = 1. For dV/dt in the above equation we use 25mV/µs.
- I_{INRUSH} = min (8.8A & 100µF x 25mV/µs)
- I_{INRUSH} = min (8.8A and 2.5A)
- I_{INRUSH} = 2.5A

Example 5: What is the inrush current when starting SD1 with an output capacitance (C_{OUT}) of 20µF?

- I_{INRUSH} = min (I_{LIMP} and C_{OUT} x dV/dt)
- SD1 is a single-phase regulator with a high PMOS current limit (I_{LIMPP_HIGH1}) of 3.75A per phase. For I_{LIMP} in the above equation we use 3.75A.
- SD1 has a typical soft-start rate (dV/dt_SS_SD1) of 25mV/µs when OTP_SD_SS = 1. For dV/dt in the above equation we use 25mV/µs.
- I_{INRUSH} = min (3.75A and 20µF x 25mV/µs)
- I_{INRUSH} = min (3.75A and 0.5A)
- I_{INRUSH} = 0.5A

Example 6: What is the inrush current when starting SD3 with an output capacitance (C_{OUT}) of 200µF?

- I_{INRUSH} = min (I_{LIMP} and C_{OUT} x dV/dt)
- SD3 is a single-phase regulator with a typical PMOS current limit (I_{LIMPP3}) of 1.8A per phase. For I_{LIMP} in the above equation we use 1.8A.
- SD3 has a typical soft-start rate (dV/dt_SS_SD3) of 25mV/µs with OTP_SD_SS = 1. For dV/dt in the above equation we use 25mV/µs.
- I_{INRUSH} = min (3.0A and 200µF x 25mV/µs)
- I_{INRUSH} = min (3.0A and 5.0A)
- I_{INRUSH} = 3.0A

Dynamic Voltage Scaling

All step-down regulators feature dynamic voltage scaling (DVS). DVS allows the system controller to issue a new output voltage request to a regulator without managing the output voltage slew rate of that regulator. In other words, the system controller may change a regulator output voltage from 0.8V to 1.1V by writing the target voltage register to 1.1V. The DVS function then ramps the output voltage in a controlled manner to the new target voltage.

DVS for all step-down regulators is achieved through the I^2C interface. Additionally, GPIO5 can control DVS for SD0. Similarly, GPIO6 can control DVS for SD1. To control DVS for SD0 or SD1 through GPIO5 or GPIO6, the GPIO must be set in its alternative mode (AME5 = 1 or AME6 = 1). When in their alternative mode, DIRx determines whether the GPIO input is active high or active low. With the GPIO input active, the step-down regulator's target voltage is set by VDVSSDx. With the GPIO input inactive, the step-down regulator's target voltage is set by VSDx.

The rising and falling slew-rate during DVS is adjustable with SR_SDx[1:0] and nFSRAD_SDx. The typical use case for SR_SDx[1:0] and nFSRAD_SDx bits is to set them to the desired value during system initialization and then leave them that way during the normal operation of the system. These bits should not be changed while their associated step-down regulators are in the middle of an output voltage slew-rate event. When determining the ideal settings for these bits, consider the required transition time, the output capacitance on the regulator, the regulator output current needed to slew that output capacitance at the designated rate, and required input current. In general, larger output capacitances should use slower transition rates.

During a DVS transition, the regulators output current increases by C_{OUT} x dV/dt. In the event that the load current plus the additional current imposed by the DVS transition reach the regulator's current limit, the current limit is enforced. When the current limit is enforced, the advertised DVS transition rate (dV/dt) does not occur.

The POK comparator is masked to prevent false POK interrupts during the DVS period.

Remote Output Voltage Sensing (ROVS)

SD0 and SD1 feature remote output voltage sensing (ROVS) for improved output voltage accuracy. The SNSN and SNSP inputs connect directly across the load, with the SNSN pin connected to a quiet analog ground near the load, and SNSP connected directly to the load's power input. The ROVS can be independently disabled through software order to reduce quiescent current consumption (ROVS_EN_SDx). When SD0 or SD1 is placed in low-power mode, the ROVS is automatically disabled. Although the ROVS is automatically disabled, the ROVS_EN_SDx bits are not automatically cleared. If ROVS_EN_SDx is set when SDx enters normal-power mode, the ROVS feature is automatically re-enabled.

Out-of-Phase Switching

The IC has five step-down converter power stages. Enabling the high-side switches of each power stages on alternate clock edges (i.e., out-of-phase) minimizes input current ripple, thus reducing the input capacitance required. Table 3 shows how the IC step-down converter power stages are assigned to alternate phases of the step-down converter's master clock.

SKIP/FPWM Operation

In the normal IC operating state, all step-down regulators automatically transition between skip mode and fixed-frequency operation as load current varies (i.e., skip mode with low load current and fixed-frequency with high load current). For operating modes where lowest output ripple is required at low load currents, forced PWM switching behavior can be independently enabled by setting FPWM_SDx. Note that forcing PWM behavior at light loads decreases the regulator efficiency.

Table 3. Out-of-Phase Switching Details

HIGH-SIDE SWITCH ENABLE SIGNAL	
RISING EDGE	**FALLING EDGE**
SD0A, SD1	SD2, SD3, SD0B

Power-OK Comparators for Step-Down Regulators

Each step-down regulator includes a power-OK (POK) comparator. The POK comparator signals (nPOK_SDx) indicate when each output has lost regulation (i.e., the output voltage is below V_{POK_SDx}). The POK signal has a noise immunity filter ($t_{POKNFSD}$). The POK comparator is also masked during the soft-start time and during the DVS time to prevent false POK interrupts.

When any of the POK signals (nPOK_Lx) go high, a maskable interrupt is generated. POK is the only interrupt available for the IC step-down regulators. The block level step-down interrupt register is IRQSD and the top level LDO interrupt is IRQ_SD. See the *Status and Interrupts* section for more information.

Inductor Selection

Choose the step-down regulator inductance to be 1.0µH for all step-down regulators as shown in Figure 40 and Figure 41. The IC works well with physically small inductors, however, care must be taken when choosing the proper inductor saturation current and equivalent series resistance (ESR).

The minimum recommended saturation current requirement is 600mA, however, typical applications require-larger saturation current to support their loads. The peak-to-peak inductor ripple current (I_{P-P}) during PWM operation is calculated as shown in Equation 1. The inductor's peak ripple current (I_{L-PEAK}) due to the load (I_{LOAD}) is shown in Equation 2. A well-designed system need only have an inductor saturation current of I_{L-PEAK}. Note that is some cases, the maximum expected system current can occur based on the step-down regulator startup, dynamic voltage slew-rate, or output short circuit.

Equation 1. Inductor Peak-to-Peak Ripple Current

$$I_{P-P} = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

Equation 2. Inductor Peak Ripple Current

$$I_{L-PEAK} = I_{LOAD} + \frac{I_{P-P}}{2}$$

Reduce the inductor's series resistance for maximum efficiency. For designs that require a small solution size, the step-down regulators tolerate relatively high series resistance (~100mΩ). Using an inductor with high series resistance reduces the overall efficiency of the buck and causes additional thermal dissipation.

Input Capacitor Selection

The input capacitor in a step-down converter reduces current peaks drawn from the power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency must be less than that of the source impedance of the supply so that high-frequency switching currents do not pass through the input source.

The step-down regulator power inputs are critical discontinuous current paths that require careful bypassing. In the PCB layout, place the step-down regulator input bypass capacitors as close as possible to each pair of switching regulator power input pins (IN_SDx to PG_SDx) on the same side of the PCB as the IC (i.e., don't make input capacitor connections through vias).

The input capacitor must meet the input ripple current requirement imposed by the step-down converter. Ceramic capacitors are preferred due to their low ESR and resilience to power-up surge currents. Choose the input capacitor so that its temperature rise due to input ripple current does not exceed about +10°C. For a step-down DC-DC converter, the maximum input ripple current is half of the output current. This maximum input ripple current occurs when the step-down converter operates at 50% duty factor (V_{IN} = 2 x V_{OUT}).

Bypass each step-down regulator input with a 4.7µF or 2.2µF ceramic capacitor from IN_SDx to PG_SDx as shown in Figure 40 and Figure 41. Use capacitors that maintain their capacitance over temperature and DC bias. Ceramic capacitors with an X7R or X5R temperature characteristic generally perform well. The capacitor voltage rating should be 6.3V or greater.

Output Capacitor Selection

The step-down regulator output capacitance keeps output ripple small and ensures control loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors are recommended due to their low equivalent series resistance (ESR) and good frequency response impedance. The required output capacitance for each of the IC step-down regulators are shown in their respective *Electrical Characteristics* tables (COSDx). The typical value shown corresponds to the capacitors nominal output capacitance. The minimum value shown corresponds to the output capacitance that is required for stability.

As the case sizes of ceramic surface-mount capacitors decrease, their capacitance vs. DC bias voltage characteristic becomes poor. Due to this characteristic, it is possible for 0805 capacitors to perform well while 0603 capacitors of the same value might not. The nominal output capacitor requirement for the IC is shown in the “typical” value of the *Electrical Characteristics* table; however, after their DC bias voltage derating, the output capacitance must have at least the “minimum” value shown in the *Electrical Characteristics* table.

In applications where the parasitic impedance between the step-down regulator’s local output capacitance and its point-of-load (POL) input capacitor is small (i.e., <10mΩ), the POL’s input capacitor contributes to the step-down regulator’s stability. This means that with respect to SD2’s output capacitor, it is possible to use one local 10μF output capacitor and one 10μF POL input capacitor to satisfy the typical 20μF requirement for SD2 output capacitance.

Active-Discharge Resistors

Each step-down regulator has an active-discharge resistor feature that can be enabled/disabled with nADE_SDx_. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled such that whenever V_{MBATT} is below $V_{MBATTUVLO}$ all regulators are disabled with their active-discharge resistors turned on. When V_{MBATT} is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

SD3 Default Voltage (D_SD3)

The default output voltage of SD3 is pin programmable with the D_SD3 tri-level logic input. As shown in Table 4, it programs either 1.2V, 1.35V, or a factory OTP setting. The logic level of D_SD3 is latched each time the MBATT voltage rises above the main-battery undervoltage-lockout threshold (V_{MBATT} > $V_{MBATTUVLO}$). The time required for the D_SD3 to latch in the correct logic state is $t_{DSD3LTCH}$. Changes to D_SD3 after the logic level is latched have no effect.

Table 4. D_SD3 Logic

D_SD3 LOGIC LEVEL	SD3 DEFAULT VOLTAGE
MBATT (logic high)	1.35V
Unconnected	Factory OTP setting such as 1.5V
GND (logic low)	1.2V

Linear Regulator

The IC has nine linear regulators (LDOs). Table 1 summarizes the basic characteristics of the linear regulators in addition to the other regulators on the device. Figure 40 shows the external component values for the linear regulators. Figure 2 shows a *Simplified Functional Diagram* of the entire device including the linear regulators. Figure 10 shows a more detailed functional diagram of just linear regulators. The nine LDOs of the MAX77863 are derived of five basic topologies as shown in Table 5.

The four NMOS regulators are capless designs that are stable with or without an output decoupling capacitor. Additionally, the PMOS regulators have adjustable compensation that allows for the use of remote output capacitors.

All regulators can be operated in low-power mode, where the no load quiescent current drops to 1.5μA. In low-power mode, each output supports a maximum load of 5mA.

All regulators have an output voltage power-OK interrupt signal that is integrated into the IC interrupt architecture.

Features

- Nine Linear Regulators
- General Performance
  - ±3% Output Accuracy Over Load/Line/Temperature
  - 50mV Drop-Out at Full Load
  - 70dB PSRR at 10kHz
  - 1.5μA Low-Power Mode
  - Short-Circuit and Thermal-Overload Protection
  - Dynamically Programmable Output Voltage
  - Power-OK Interrupt
  - Programmable Soft-Start Rate: 100mV/μs or 5mV/μs
    - Soft-Start into Pre-Biased Output
- Four N-Channel Regulators (LDO0/1/7/8)
  - 0.8V to 5.5V Input Range
  - 29μA Quiescent Supply Current
  - No Output Capacitor Required in Normal Operating Mode (Cap Required for Low-Power Mode)
- Five Standard P-Channel Regulators (LDO2/3/4/5/6)
  - 1.7V to 5.5V Input Range
  - 20μA Quiescent Supply Current
  - Remote Capacitor Design with Register Adjustable Compensation to Optimize Transient Performance

Basic LDO Topologies

The nine LDOs of the IC are derived of five basic topologies as shown in Table 5.

The PMOS regulators (PDRVx) operate and draw power from their power inputs (IN_LDOxx), which have a minimum operating supply voltage of 1.7V (V_{IN_LDOx}). The control registers and some input circuitry operate from the main system supply (MBATT) and hold their contents when the regulator input voltage (V_{IN_LDOx}) drops to 0V.

The NMOS regulators (NDRVx) gate drive operates from the main system supply (MBATT), while the load current is provided by the regulator input (IN_LDOxx). The input voltage (V_{IN_LDOx}) for the NMOS regulators extends down to 0.8V. To provide adequate gate drive for the NMOS output device, the NMOS output voltage should be more than 1.5V lower than the main system supply voltage (V_{MBATT}). The control registers are also powered from MBATT.

NMOS regulators work into dropout with the V_{IN_LDOx} to V_{OUT_LDOx} voltage determined by I_{LOAD} x R_{DO} where R_{DO} is the dropout resistance (typically 200mΩ). As dropout voltage decreases (by reducing load) below 0.3V, the PSRR and load regulation degrades.

All PMOS regulators are compensated at their output and require a remote output capacitance large enough to prevent oscillation, as specified in the *Electrical Characteristics* table (C_{OUTx}). The NMOS regulators are internally compensated, but an additional output capacitor can be added to improve immunity to high-frequency noise and allow stable low-power mode operation.

Table 5. Basic LDO Topologies

NAME	DESCRIPTION	LDO
PDRV1	Power device: PMOS Output current: 150mA	LDO2, LDO4, LDO5, LDO6
PDRV2	Power device: PMOS Output current: 300mA	LDO3
NDRV1	Power device: NMOS Output current: 150mA	LDO0, LDO1
NDRV2	Power device: NMOS Output current: 300mA	LDO8
NDRV3	Power device: NMOS Output current: 450mA	LDO7

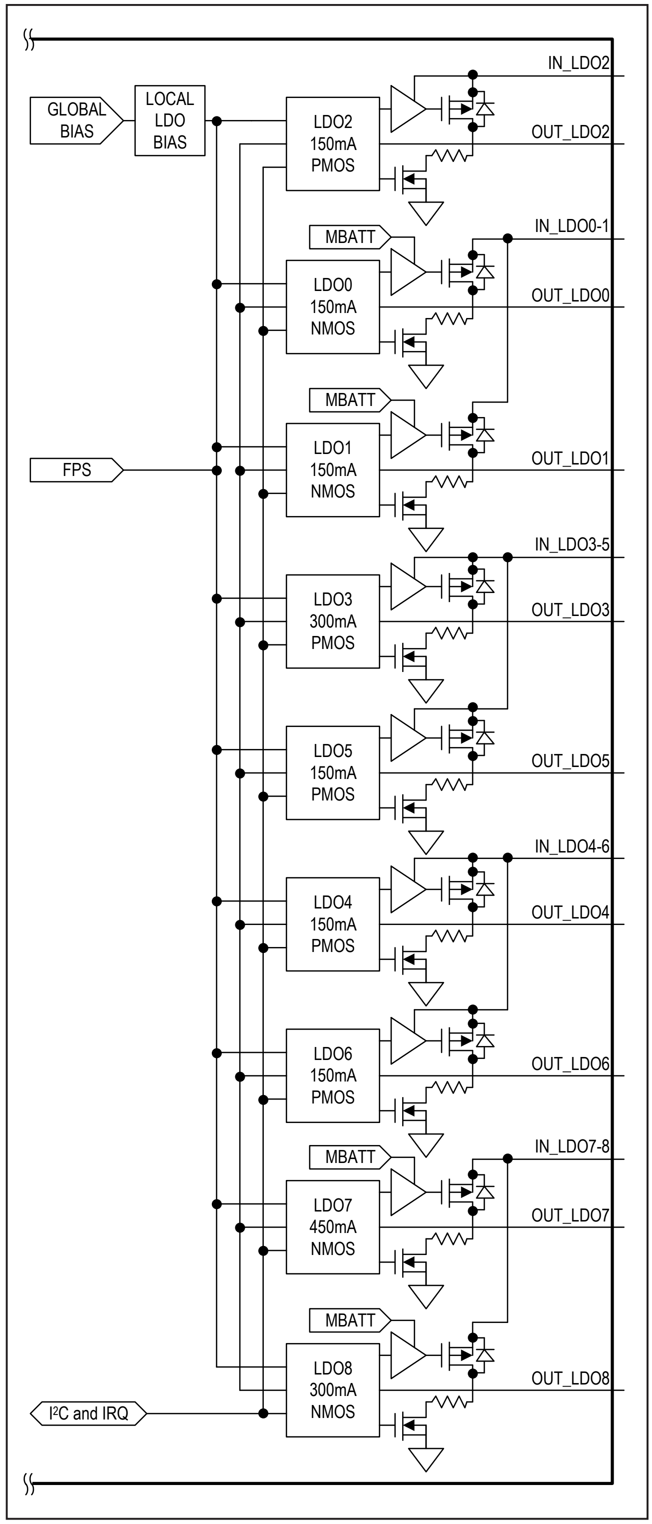


Figure 10. Linear Regulator Functional Diagram

LDO Power Modes

Linear regulators and step-down regulators have very similar power mode controls. Each linear regulator is independently controlled with PWR_MD_Lx[1:0] and each step-down regulator is independently controlled with PWR_MD_SDx[1:0] (see the *Dynamic Voltage Scaling* section for more information about step-down regulators). In addition, to enable and disable control each linear regulator has a special low-power mode that reduced the quiescent current to 1.5µA. In low-power mode, each regulator supports a load of up to 5mA (I_{MAXxx}). The load regulation performance degrades proportionally with the reduced load current.

Several usage options are available for low-power mode. To force individual regulators to low-power mode, set PWR_MD_Lx to 0b10. To force a group of regulators to enter and exit low-power mode in unison, set their individual PWR_MD_Lx_ bits to 0b10. When set for this "group and/or dynamic" low-power mode, the low-power mode is enabled when the global low-power mode signal is high. The global low-power mode signal is driven by the GLBL_LPM bit or through a GPIO0 (see the *Global Low-Power Mode* section for more information).

When a linear regulator is configured to be part of a flexible power sequence (FPSSRC_Lx), the power mode bits (PWR_MD_Lx) are still used to configure low-power mode and normal-power mode, but the flexible power sequencer itself controls weather the regulator is enabled or disabled. See the PWR_MD_Lx[1:0] bit descriptions for complete information.

Soft-Start and Dynamic Voltage Scaling

The linear regulators have a programmable soft-start rate. When a linear regulator is enabled, the output voltage ramps to its final voltage at a slew rate of either 5mV/µs or 100mV/µs, depending on the state of the SS_Lx bit. The 5mV/µs ramp rate limits the input inrush current to around 10mA on a 300mA regulator with a 2.2µF output capacitor and no load. The 100mV/µs ramp rate results in a 200mA inrush current on a 300mA regulator with a 2.2µF output capacitor and no load, but achieves regulation within 50µs. The soft-start ramp rate is also the rate of change at the output when changing dynamically between two output voltages while enabled (dynamic voltage scaling: DVS).

The LDO soft-start circuitry supports starting into a prebiased output. For example, if the output capacitor has an initial voltage of 0.4V when the regulator is enabled, the regulator gracefully increases the capacitor voltage to the required target voltage such as 1.2V. This is unlike other regulators without the start into prebias feature where they can force the output capacitor voltage to 0V before the soft-start ramp begins.

During a soft-start event or a DVS transition, the regulators output current increases by C_{OUT} x dV/dt. In the event that the load current, plus the additional current imposed by the soft-start or DVS transition, reach the regulator's current limit, the current limit is enforced. When the current limit is enforced, the advertised transition rate (dV/dt) does not occur.

Power-OK Comparators for Linear Regulators

Each linear regulator includes a power-OK (POK) comparator. The POK comparator signals (POK_Lx) indicate when each output has lost regulation (i.e., the output voltage is below V_{POKTHL}). The POK signal has a 25µs noise immunity filter ($t_{POKNFLDO}$).

When any of the POK signals (POK_Lx) go low, a maskable interrupt is generated. POK is the only interrupt available for the MAX77863 LDOs. The block level LDO interrupt register is IRQ_LVL2_Lx and the top level LDO interrupt is IRQ_LDO. See the *Status and Interrupts* section for more information.

Active-Discharge Resistors

Each linear regulator has an active-discharge resistor feature that can be enabled/disabled with ADE_Lx_. Enabling the active discharge feature helps ensure a complete and timely power down of all system peripherals. The default condition of the active-discharge resistor feature is enabled such that whenever V_{MBATT} is below $V_{MBATTUVLO}$ all regulators are disabled with their active-discharge resistors turned on. When V_{MBATT} is less than 1.0V, the NMOS transistors that control the active-discharge resistors lose their gate drive and become open.

Overvoltage Clamp

Each LDO has an overvoltage clamp that allows it to sink current when the output voltage is above its target voltage. This overvoltage clamp for a given LDO is disabled when that LDO is in low-power mode. If an LDO is in normal-power mode, then the overvoltage clamp is enabled/disabled with OVCLMP_EN_Lx (default enabled). The following bulleted list briefly describes three typical application scenarios that pertain to the overvoltage clamp.

Typical application scenarios for the overvoltage clamp:

- LDOs Load Leaking Current into the LDOs Output: Some LDO loads leak current into an LDO output during certain operating modes. This is typically seen with microprocessor loads. For example, a microprocessor with 3.3V, 2.5V, 1.8V, and 1.0V supply rails is running in standby mode. In this mode, the higher voltage rails can leak currents of several milliamps into the lower voltage rails. If the 1.0V rail is supplied by an LDO, the LDO output voltage rises based on the amount of leakage current. With the LDO overvoltage clamp enabled, when the output voltage rises above its target regulation voltage, the overvoltage clamp sinks current from the output capacitor, which brings the output voltage back within regulation.
- Negative Load Transient to 0A: When the LDO load current quickly ramps to 0A (i.e., 300mA to 0A load transient with 1μs transition time), the output voltage can overshoot (i.e., sore). Since the LDO cannot turn off its pass device with an intently fast load transition, the LDO output voltage overshoots. In this instance, when the output voltage sores above target regulation voltage, the overvoltage clamp sinks current from the output capacitor, which brings the output voltage back within regulation.
- Negative Dynamic Voltage Transition: When the LDO output target voltage is decreased (i.e., 1.2V to 0.8V) when the system loading is light, the energy in the output capacitor tends to hold the output voltage up. When the output voltage is above its target regulation voltage, the overvoltage clamp sinks current from the output capacitor, which brings the output voltage back within regulation.

Output Capacitor Selection

The output capacitor selection differs slightly between a P-channel and an N-channel LDO.

P-Channel Linear Regulator Output Capacitor

P-channel LDOs (PDRx as shown in Table 5) require an output capacitor to maintain stable output voltage regulation. Adjustable compensation allows for flexibility when designing the PCB and placing the output capacitor. The default compensation is factory programmable; additionally, the compensation is register adjustable when the LDO is off. For each LDOs output capacitor recommendation (C_{OUTx}) see Table 1.

In many LDO designs, there is little-to-no flexibility in the physical placement of the output capacitor on the PCB. However, the LDO implementation within the IC provides adjustable compensation for the P-channel LDOs. This adjustable compensation allows flexibility in the placement of the output capacitor on the PCB, however, as the output capacitor is placed farther from the device, slower compensation values are required to maintain stability; these slower compensation values decrease performances.

For optimum p-channel LDO performance, place the output capacitor as close to the LDO output as possible and program COMP_Lx = 0b00. In situations where the full LDO performance is not required, the output capacitor can be place farther away from the LDO output with slower compensation values. This option becomes especially useful when the LDO output capacitor can be eliminated and the load's local input capacitor becomes the only capacitance on the LDO output node. See the COMP_Lx bit descriptions for more information.

Warning: The COMP_Lx bits should only be changed when the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes.

N-Channel Linear Regulator Output Capacitor

N-channel LDOs (NDRVx as shown in Table 5) technically do not require any output capacitor to maintain stable output voltage regulation if they are in normal mode (i.e., they can be capless). However, an n-channel LDO does require an output capacitor to maintain stable output voltage regulation in low-power mode. In either mode (normal or low-power) the LDO performs best with an output capacitor (C_{OUTx}) as recommended in Table 1.

Note that the COMP_Lx[1:0] bits for n-channel LDOs must be set to 0b00.

BIAS

A small section of bias circuitry is required to be on when any of the LDOs are enabled. Figure 11 shows that any LDO enable signal OR the L_B_EN enables the LDO bias circuits. In addition, whenever the LDO bias is enabled, the global bias for the IC is also enabled. The LDO bias circuitry takes t_{LBIAS} to turn on. If the LDO bias circuit is off and an LDO is enabled, the total time before the output starts slewing up is $t_{LBIAS} + t_{LON}$. If the LDO bias is on and an LDO is enabled, the total time before the output starts slewing is t_{LON}.

If the sequencing of a group of regulators is particularly important, it may be desirable to force the LDO bias to be on with the L_B_EN bit to ensure that LDOs enable in a consistent manner with the shortest latency. Note that whenever L_B_EN is set, the global bias circuits and LDO bias circuits are enabled. The combined bias circuitry current is I_{QBIAS}. To ensure that the system always operates with the lowest quiescent current possible, it is a good idea to clear L_B_EN when it is not needed.

General Purpose Input/Output (GPIO)

The IC has eight GPIO channels. The *Simplified Functional Diagram* shows a simplified functional diagram of the GPIO functional block. Figure 12 shows a detailed functional diagram of the GPIOs. Table 7 is the GPIO programming matrix. Each GPIO is programmable to operate in a special alternative mode as shown in Table 6.

Features

- Eight GPIO
- Two Input Power Sources
  - 4 GPIOs per input
  - Input Voltage Range from 1.7V to 5.5V
- GPI
  - GPI to Global Low-Power Mode Control
  - GPI to SD0 DVS Signal
  - GPI to SD1 DVS Signal
  - GPI to Interrupt
  - GPI to Flexible Power Sequencer
  - Flexible Edge Trigger Support
  - Selectable Debounce Time
  - Optional Pullup/Pulldown
- GPO
  - Push-Pull
  - Open-Drain
  - Buffered Reference Output
  - GPO to 32kHz Output Option
  - 12mA Sink Current Allows for LED Drive

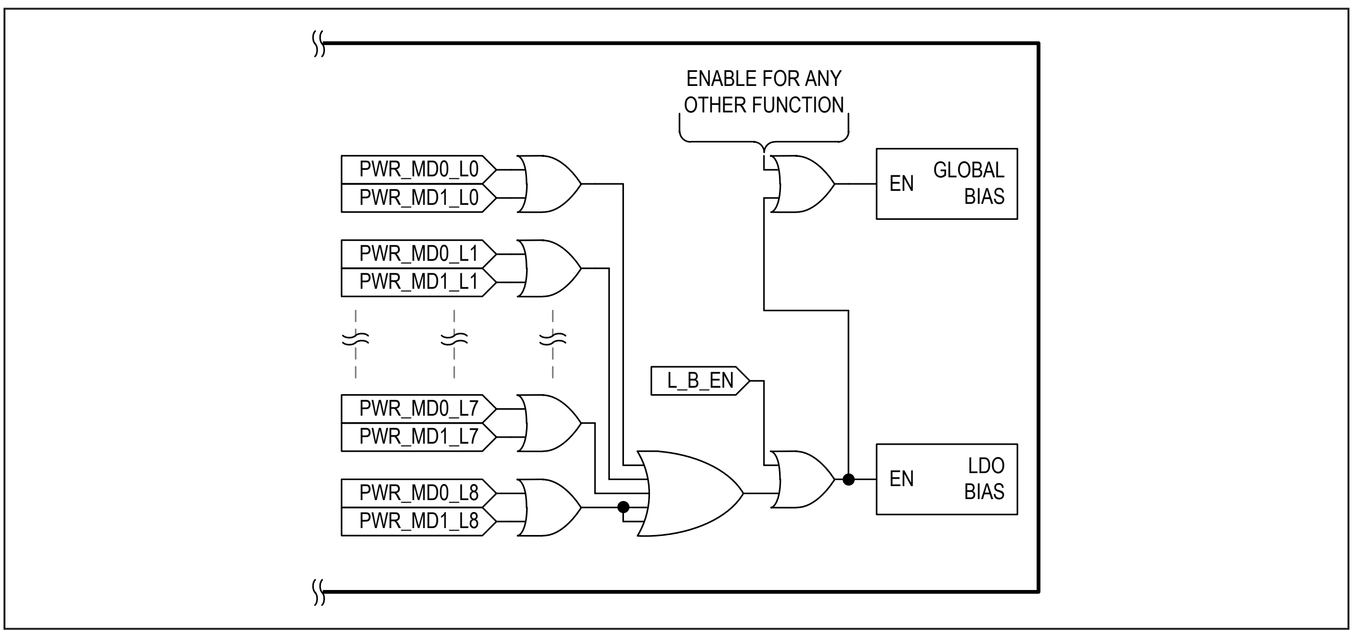


Figure 11. LDO Bias Enable Circuitry

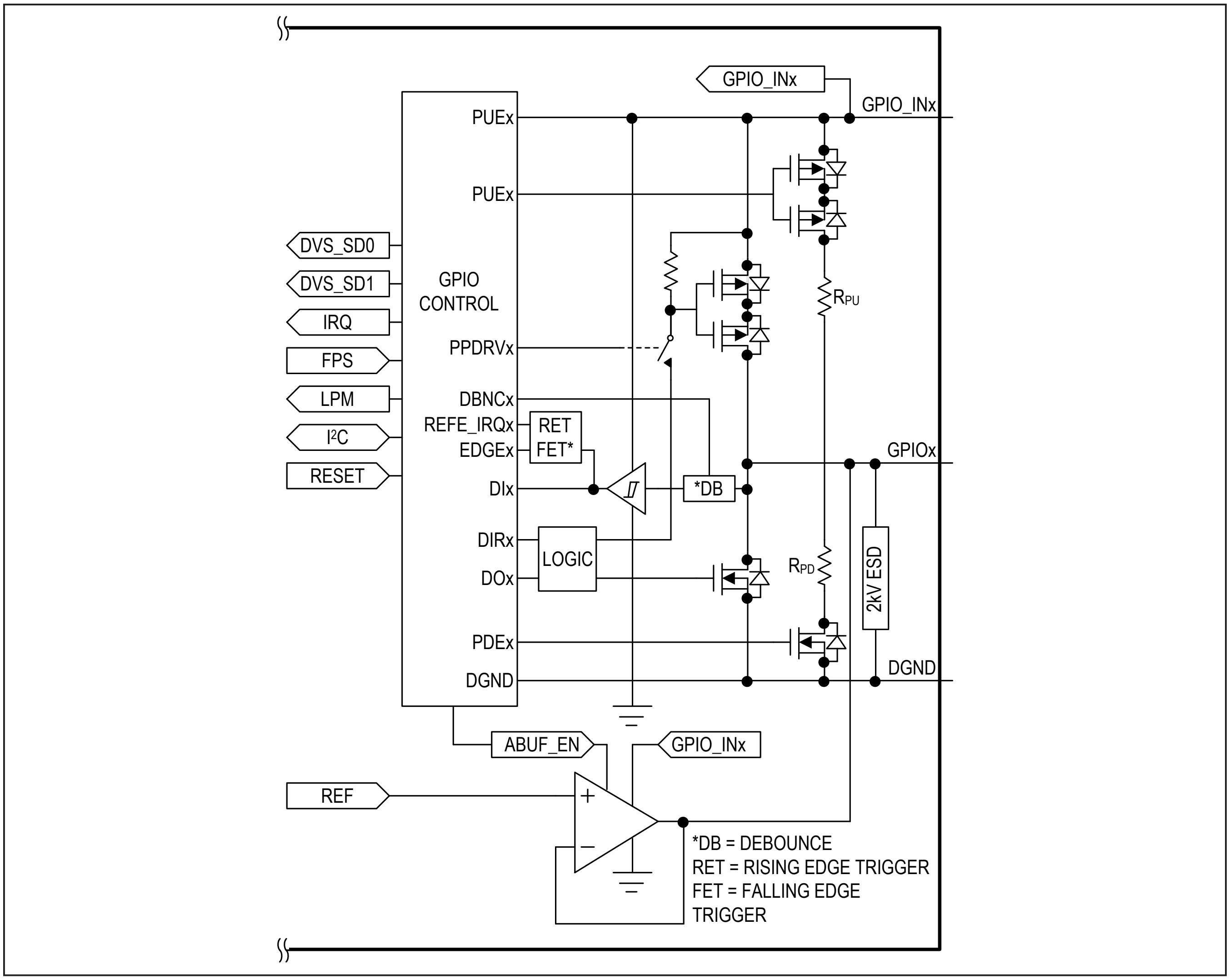


Figure 12. GPIO Simplified Block Diagram

GPO

When configured as a general-purpose output (GPO), the GPO is programmable to be push-pull or open-drain. See the “GPIOx GPO” section of Table 7 for the full details of how to program a GPO.

GPI

When configured as a general-purpose input (GPI), the GPI is programmable to have either a high-impedance, 100kΩ pulldown, or 100kΩ pullup. Additionally, interrupt inputs with programmable debounce timers are available. See the “GPIOx GPI” section of Table 7 for the full details of how to program a GPI.

GPI Interrupts

The GPI edge(s) that triggers interrupts are selectable with REFE_IRQx. When a GPI interrupt is enabled and the selected edge(s) are detected, EDGEx is set in the IRQ_LVL2_GPIO register and IRQ_GPIO is set in the top-level interrupt register. If the top-level interrupt mask is cleared (IRQ_GPIOM), the external interrupt signal nIRQ is asserted.

Alternate Mode

In addition to the GPO and GPI configurations, each GPIO has an alternate mode as shown in Table 7 and *AME_GPIO: Alternate Mode Enable GPIO Configuration Register* register description.

When a GPIO is in an alternate mode the device may internally force the direction (i.e., output or input) and or logic level of the GPIO. However other options such as debounce times and rising/falling edge triggered interrupt settings are still valid in alternate mode. See the register descriptions and “alternative mode” sections of the Table 7 for the full details of how to program an alternative mode.

When GPIO7 is an alternative mode it is a 1.25V reference output. As a reference output, the GPIO7 output drivers are high-z, the input buffer is disabled to prevent leakage, and the interrupt feature is disabled. It is recommended that user disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode. Note that when using GPIO7 as a reference output, minimize the capacitance at this node. The maximum acceptable capacitance is 0.1µF.

Table 6. Alternate Modes for GPIOs

GPIOx	ALTERNATE MODES
GPIO0	Low-power mode control input
GPIO1	Active-high, open-drain, flexible power sequencer output
GPIO2	Active-high, open-drain, flexible power sequencer output
GPIO3	Active-high, open-drain, flexible power sequencer output
GPIO4	32kHz output (32K_OUT1)
GPIO5	SD0 dynamic voltage scaling input
GPIO6	SD1 dynamic voltage scaling input
GPIO7	Reference output 1.25V buffered reference output

Table 7. GPIO Programming Matrix

GPIOx GPI									
Comment	DBNCx[1:0]	REFE_IRQx[1:0]	DOx	DIx	DIRx	PPDRVx	PUEx	PDEx	AMEx
GPI	Debounce times	Interrupt options	0	Input logic level	1 = GP1	0	0	0	0
GPI with Internal Pullup	Debounce times	Interrupt options	0	Input logic level	1 = GP1	0	1	0	0
GPI with Internal Pulldown	Debounce times	Interrupt options	1	Input logic level	1 = GP1	0	0	1	0
GPIOx GPO									
GPO Push-Pull	0	0	Output logic level	0	0 = GPO	1-push-pull	0	0	0
GPO Open-Drain	0	0	Output logic level	0	0 = GPO	0-open-drain	0	0	0
GPIO0 ALTERNATIVE MODE LOW-POWER MODE CONTROL INPUT									
Comment	DENC0[1:0]	REFE_IRQ0[1:0]	DO0	DI0	DIR0	PPDRV0	PUE0	PDE0	AME0
GPI1 Low-Power Mode Input, Low-Power Mode	Debounce times	Interrupt options	0	0	0 = active-low	0	0	0	1
GPI1 Low-Power Mode Input, Low-Power Mode, Internal Pullup	Debounce times	Interrupt options	0	0	0 = active-low	0	1	0	1

Table 7. GPIO Programming Matrix (continued)

GPIO0 ALTERNATIVE MODE LOW-POWER MODE CONTROL INPUT (continued)									
GPI1 Low-Power Mode Input, Normal-Power Mode	Debounce times	Interrupt options	0	1	0 = active-low	0	0	0	1
GPI1 Low-Power Mode Input, Normal-Power Mode, Internal Pullup	Debounce times	Interrupt options	0	1	0 = active-low	0	1	0	1
GPI1 Low-Power Mode Input, Normal-Power Mode	Debounce times	Interrupt options	0	0	1 = active-high	0	0	0	1
GPI1 Low-Power Mode Input, Normal-Power Mode, Internal Pullup	Debounce times	Interrupt options	0	0	1 = active-high	0	1	0	1
GPI1 Low-Power Mode Input, Low-Power Mode	Debounce times	Interrupt options	0	1	1 = active-high	0	0	0	1
GPI1 Low-Power Mode Input, Low-Power Mode, Internal Pullup	Debounce times	Interrupt options	0	1	1 = active-high	0	1	0	1
GPIO1/2/3 ALTERNATIVE MODE ACTIVE-HIGH FLEXIBLE POWER SEQUENCER OUTPUT									
Comment	DENCx[1:0]	REFE_IRQx[1:0]	DOx	DIx	DIRx	PPDRVx	PUEx	PDEx	AMEx
GPO Flexible Power Sequencer Output, Push-Pull	0	0	Set by FPS	0	0	1 = push-pull	0	0	1
GPO Flexible Power Sequencer Output, Open-Drain	0	0	Set by FPS	0	0	0 = open-drain	0	0	1
GPIO4 ALTERNATIVE MODE 32kHz OUTPUT (32K_OUT1)									
Comment	DBNC4[1:0]	REFE_IRQ4[1:0]	DO4	DI4	DIR4	PPDRV4	PUE4	PDE4	AME4
GPO 32kHz Output, Push-Pull	0	0	Set by XIN	0	0	1 = push-pull	0	0	1
GPO 32kHz Output, Open-Drain	0	0	Set by XIN	0	0	0 = open-drain	0	0	1

Table 7. GPIO Programming Matrix (continued)

GPIO5 ALTERNATIVE MODE SD0 DYNAMIC VOLTAGE SCALING INPUT									
Comment	DBNC5[1:0]	REFE_IRQ5[1:0]	DO5	DI5	DIR5	PPDRV5	PUE5	PDE5	AME5
GPI SD0 DVS Input, VSD0 = VDVSSD0	Debounce times	Interrupt options	0	0	0 = active-low	0	0	0	1
GPI SD0 DVS Input, VSD0 = VDVSSD0, Internal Pullup	Debounce times	Interrupt options	0	0	0 = active-low	0	1	0	1
GPI SD0 DVS Input, VSD0 = VSD0	Debounce times	Interrupt options	0	1	0 = active-low	0	0	0	1
GPI SD0 DVS Input, VSD0 = VSD0, Internal Pullup	Debounce times	Interrupt options	0	1	0 = active-low	0	1	0	1
GPI SD0 DVS Input, VSD0 = VSD0	Debounce times	Interrupt options	0	0	1 = active-high	0	0	0	1
GPI SD0 DVS Input, VSD0 = VSD0, Internal Pullup	Debounce times	Interrupt options	0	0	1 = active-high	0	1	0	1
GPI SD0 DVS Input, VSD0 = VDVSSD0	Debounce times	Interrupt options	0	1	1 = active-high	0	0	0	1
GPI SD0 DVS Input, VSD0 = VDVSSD0, Internal Pullup	Debounce times	Interrupt options	0	1	1 = active-high	0	1	0	1
GPIO6 ALTERNATIVE MODE SD1 DYNAMIC VOLTAGE SCALING INPUT									
Comment	DBNC6[1:0]	REFE_IRQ6[1:0]	DO6	DI6	DIR6	PPDRV6	PUE6	PDE6	AME6
GPI SD1 DVS Input, VSD1 = VDVSSD1	Debounce times	Interrupt options	0	0	0 = active-low	0	0	0	1
GPI SD1 DVS Input, VSD1 = VDVSSD1, Internal Pullup	Debounce times	Interrupt options	0	0	0 = active-low	0	1	0	1
GPI SD1 DVS Input, VSD1 = VSD1	Debounce times	Interrupt options	0	1	0 = active-low	0	0	0	1

Table 7. GPIO Programming Matrix (continued)

GPIO6 ALTERNATIVE MODE SD1 DYNAMIC VOLTAGE SCALING INPUT (continued)									
GPI SD1 DVS Input, VSD1 = VSD1, Internal Pullup	Debounce times	Interrupt options	0	1	0 = active-low	0	1	0	1
GPI SD1 DVS Input, VSD1 = VSD1	Debounce times	Interrupt options	0	0	1 = active-high	0	0	0	1
GPI SD1 DVS Input, VSD1 = VSD1, Internal Pullup	Debounce times	Interrupt options	0	0	1 = active-high	0	1	0	1
GPI SD1 DVS Input, VSD1 = VDVSSD1	Debounce times	Interrupt options	0	1	1 = active-high	0	0	0	1
GPI SD1 DVS Input, VSD1 = VDVSSD1, Internal Pullup	Debounce times	Interrupt options	0	1	1 = active-high	0	1	0	1
GPIO7 ALTERNATIVE MODE REFERENCE OUTPUT 1.25V BUFFERED REFERENCE OUTPUT									
Comment	DBNC7[1:0]	REFE_IRQ7[1:0]	DO7	DI7	DIR7	PPDRV7	PUE7	PDE7	AME7
GPIO7 = 1.25V Output	0	0	0	0	0	0	0	0	1

Real-Time Clock (RTC)

The real-time clock (RTC) is responsible for keeping track of the time. It records seconds, minutes, hours, days, months, and years with a calendar structure that accounts for leap years. The RTC is further equipped with two alarms and has a host of maskable interrupt capabilities.

Through a set of configuration registers, various modes of operation are possible. RTC supports both "Binary" and "Binary Coded Decimal", and supports features such as AM/PM and 24/12 modes of operation. Additional sudden momentary power loss (SMPL) is available.

Features

- Gregorian calendar with leap year correction
- Two alarms
- Maskable interrupts
  - 1s and 60s
  - Alarm 1 and 2
  - SMPL
- Binary and BCD Modes
- 12/24 hour modes
- Sudden momentary power loss (SMPL)
- Double buffered read/write registers allow asynchronous register access
- Operates down to 1.65V

Read/Write Operations

The RTC has double buffered read/write registers that allow the register access to be asynchronous to the RTC (Figure 13).

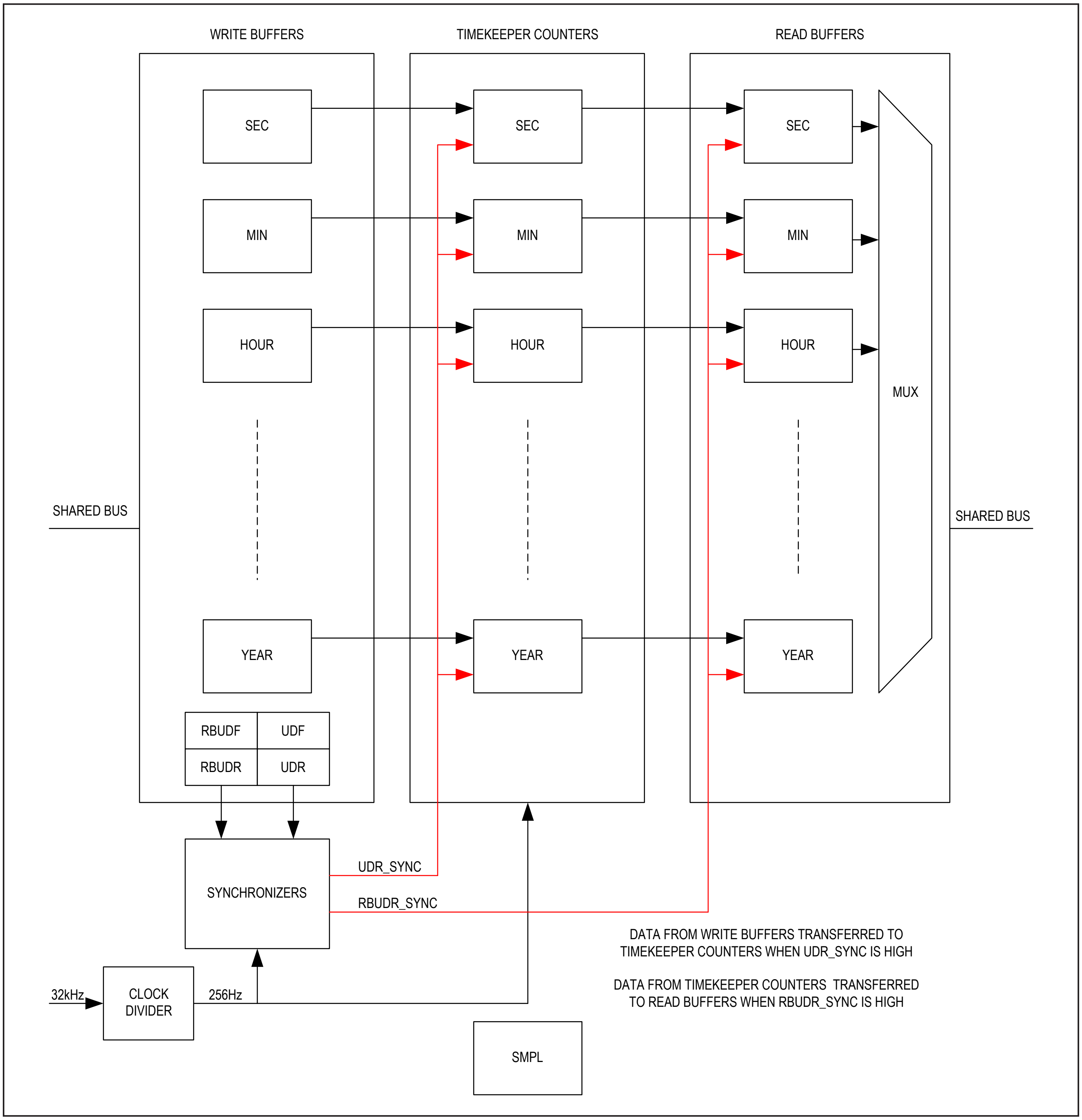


Figure 13. RTC Simplified Functional Diagram

In order to safely write to various registers on-board the RTC, all RTC registers (except RTCINT register, bit 0 of UPDATE0 the register, and bit 4 of UPDATE0 the register) have a corresponding "Write Buffer". When the user writes to the RTC, the user is actually performing a write to these "Write Buffers". Therefore, in writing to RTC there are two steps needed to update a particular register or set of registers:

1) User writes desired value(s) to the register(s) located between 0x07 and 0x1B. Behind the scenes, only the "Write Buffers" are updated with these new values.
2) The user then writes a 1 to UDR bit 0 of the "UPDATE0 register" at address 0x04 to transfer the modified "Write Buffers" to the corresponding time registers.

The logic subsequently would perform a transfer of data from the "Write Buffers" to the actual registers and then clears the "UDR" bit automatically as well as clearing the "Write Buffers" (marking them as not modified).

Under the hood, the logic first does a double synchronization of the UDR bit to the 32.768kHz clock before using it as an enable bit (UDR_sync in Figure 13) to transfer from "Write buffers" to the actual registers thus allowing a safe update of these two unsynchronized clock events.

Example 7. Pseudo code for setting clock to Saturday, Jan 01, 2011, 1:00:00 PM

```
Set RTCCNTL to 0x01              //12hr mode, BCD mode
Set RTCUPDATE0 to 0x01           // transfer RTCCNTL modification to RTC
Set RTCSEC to 0x00               // 0 second
Set RTCMIN to 0x00               // 0 minute
Set RTCHOUR to 0x41              // 1 PM
Set RTCDOW to 0x40               // Saturday
Set RTCMONTH to 0x01             // January
Set RTCYEAR to 0x11              // 11
Set RTCDOM to 0x01               // First
Set RTCUPDATE0 to 0x01           // transfer write buffers to counters
Wait 16ms for write to complete

Set RTCSEC to 0x…                //new write
```

Example 8. Pseudo code for setting ALARM1 to every Wednesday at 7:30:00 AM

```
Set RTCCNTL to 0x01              //12hr mode, BCD mode
Set RTCUPDATE0 to 0x01           // transfer RTCCNTL modification to RTC
Set RTCSECA1 to 0x80             //0 sec, enabled
Set RTCMINA1 to 0xB0             //30 minute, enabled
Set RTCHOURA1 to 0x87            //7 AM, enabled
Set RTCDOWA1 to 0x08             //Wednesday, enabled
Set RTCMONTHA1 to 0x00           //Disabled
Set RTCYEARA1 to 0x00            //Disabled
Set RTCDOMA1 to 0x00             //Disabled
Set RTCUPDATE0 to 0x01           // transfer write buffers to counters
Wait 16ms for write to complete

Set RTCSEC to 0x…                //new write
```

Reading from RTC

Corresponding to most timing registers there are a series of “Read Buffers”.

In order to safely read from various registers on-board the RTC, all RTC registers (except RTCINT register and bit 0 and 4 of UPDATE0 register) have a corresponding “Read Buffer”. When the user reads from the RTC, the user is actually performing a read from these “Read Buffers”. Therefore, there are two steps needed to read a particular register or set of registers:

1. The user writes a 1 to RBUDR bit 4 of the “UPDATE0 Register” at address 0x04 to transfer most timing registers to the “Read Buffers”. Behind the scenes, the “Read Buffers” are updated.
2. The user then reads from the desired register location.

After step 1, the logic subsequently performs a transfer of data from the actual registers to the “Read Buffers” and then clears the “RBUDR” bit.

Under the hood, the logic first does a double synchronization of the RBUDR bit to the 32.768kHz clock before using it as a clock (RBUDR_sync in Figure 13) to transfer from the actual registers to the “Read Buffers” thus allowing a safe update of these two unsynchronized clock events.

Example 9. Pseudo code for reading the time

```
Set RTCUPDATE0 to 0x10          // transfer timekeeper counters to read buffers
Wait 16ms for read to complete
Read RTCSEC                     // second
Read RTCMIN                     // minute
Read RTCHOUR                    // hour
Read RTCDOW                     // Day of Week
Read RTCMONTH                   // Month
Read RTCYEAR                    // Year
Read RTCDOM                     // Day of Month
```

Example 10. Pseudo code for reading ALARM1 setting

```
Set RTCUPDATE0 to 0x10          // transfer timekeeper counters to read buffers
Wait 16ms for read to complete
Read RTCSECA1                   // sec
Read RTCMINA1                   // minute
Read RTCHOURA1                  // hour
Read RTCDOWA1                   // Day of Week
Read RTCMONTHA1                 // Month
Read RTCYEARA1                  // Year
Read RTCDOMA1                   // Day of Month
```

SMPL (Sudden Momentary Power Loss)

The SMPL function allows the system to recover if power is briefly lost due to a poor battery connection. If V_{MBATT} falls below and returns above the UVLO threshold within the SMPL timer threshold (SMPLT[1:0]) and SMPL is enabled (SMPL_EN = 1), SMPL initiates a power-up sequence and the SMPL interrupt bit is set. If the SMPL timer expires before V_{MBATT} returns, the SMPL enable bit is automatically cleared in order to prevent power-up on subsequent SMPL events.

To ensure proper operation of the SMPL state machine, initialization software should clear and set SMPL_EN after each power-on event.

32kHz Crystal Oscillator and Buffered Outputs

The IC contains a crystal oscillator driver with internal load capacitance selectable by 32KLOAD[1:0] (Figure 14). PWR_MD_32K controls whether the crystal driver is in low-power mode or low-jitter mode. In low-power mode, the oscillator quiescent current is 1.5μA and in low-jitter mode the cycle-by-cycle jitter is 15ns. The crystal driver is supplied from the internal V_{RTC} node which is equal to V_{MBATT} if $V_{MBATT} > V_{MBATTUVLO}$.

The crystal driver generates two 32kHz buffered outputs. One 32kHz output has a dedicated pin (32K_OUT0). The other output (32K_OUT1) is available through GPIO4 and is useful for peripherals such as BT/WLAN chipsets (see AME4). The configuration of the output stage for 32K_OUT0 is factory programmable with OTP. The primary OTP option (OTP_32K_OUT = 0) configures the output stage for a push-pull output between ground and GPIO_INB. OTP_32K_OUT = 1 sets 32K_OUT0 for an open-drain output. The output stage for 32K_OUT1 is determined by their respective GPIO blocks.

There are three options for the internal load capacitance from XIN to XGND and XOUT to XGND: 10pF, 12pF, and 22pF. XIN and XOUT each have approximately 3pF of parasitic capacitance. The total load capacitance on the crystal is shown in Table 1.

The crystal driver also generates a status bit (32K_OK), when the 32kHz clock is OK (typically 1 second after initial start up).

Features

- Low-jitter mode provides 15ns cycle-by-cycle jitter
- On-chip crystal oscillator load capacitors
- 32kHz digital outputs
- Oscillator OK status
- Operates down to 1.5V

Backup Battery Charger

The backup battery charger is a constant voltage (CV) and constant current (CC) style charger with a series output resistance as shown in Figure 14. The backup battery charger is enabled and disabled with BBCEN. The charge current, charger voltage, output current, and output resistance are adjustable with the BBCCTRL register. The backup-battery charger is suitable for the following types of backup cells:

- Super capacitor (a.k.a., gold cap, double-layer electrolytic)
- Standard capacitors (tantalum … etc.)
- Rechargeable lithium manganese cells

Features

- 800μA maximum CC-CV backup battery charger
- 2.5V—3.5V adjustable backup battery setting with ± 3% tolerance
- Seamless transition of RTC supply from V_{MBATT} to V_{BBATT} when V_{MBATT} drops below V_{MBATT_UVLO} threshold

Table 8. 32kHz Crystal Oscillator Load Capacitance

32kLOAD	PARASITIC CAPACITANCE FROM XIN TO XGND AND XOUT TO XGND (pF)	INTERNAL LOAD CAPACITANCE FROM XIN TO XGND AND XOUT TO XGND (pF)	EXTERNAL LOAD CAPACITANCE FROM XIN TO XGND AND XOUT TO XGND (pF)	TOTAL LOAD CAPACITANCE ON THE CRYSTAL (pF)
0x00	3	12	None	7.5
0x01	3	22	None	12.5
0x02	3	None	10	6.5
0x02	3	None	12	7.5
0x02	3	None	22	12.5
0x03	3	None	22	12.5
0x03	3	10	None	6.5

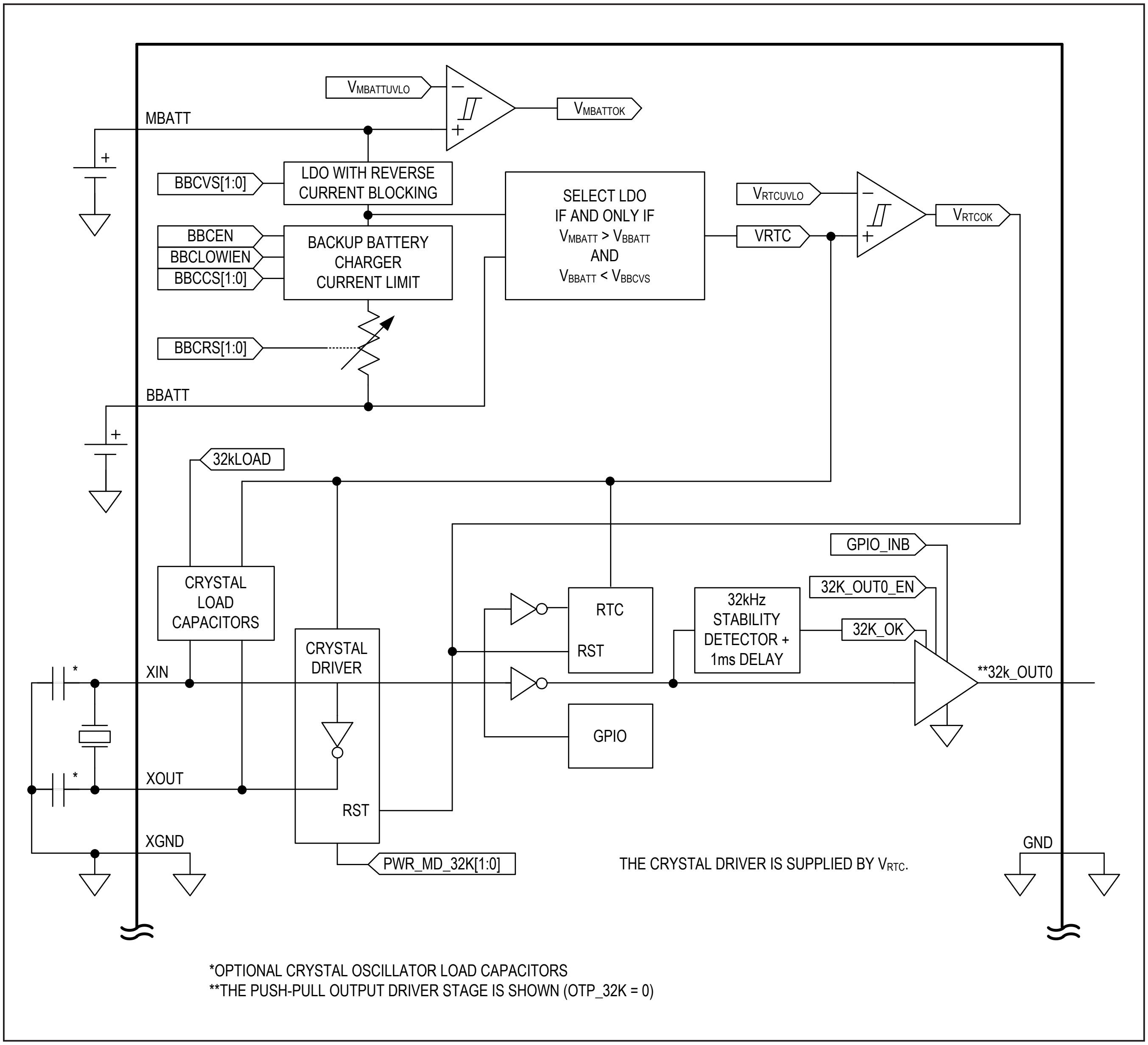


Figure 14. Backup Battery Charger, 32kHz Crystal Oscillator and RTC

ON/OFF Controller

The ON/OFF controller monitors multiple wakeup sources to intelligently enable all resources that are necessary for the AP to boot (i.e., FPS0 and FPS1). As shown in Figure 18, the on/off controller monitors wakeup events on the EN0, EN1, EN2, ACOK, nRST_IO, and LID hardware inputs. Additionally, internal wakeup events are also monitored: SMPL, ALARM1, and ALARM2 internal signals. Wakeup events go through logic to affect flexible power sequencers 0 and 1 (FPS0, FPS1). Many wakeup signals can be masked (WK_ACOK, WL_LID, WK_ALARM1, WL_ALARM2, WK_EN0).

Many signals within the on/off controller generate interrupts and are recorded in status registers.

EN0

EN0 is a digital input to the ON/OFF controller that (Figure 18) typically comes from the system's on key. The EN0 polarity is factory programmable with OTP (OTP_EN0AL) to be active-high or active-low (Figure 20).

EN0 is internally debounced (t_{DBEN0}). Programming EN0DLY allows an additional delay in the EN0 signal path ($t_{1SECEN0}$).

Manual Reset with EN0

An extended EN0 event forces MRO high which activates a global shutdown (see the *Global Resources* section for more information on global shutdown). Note that an OTP bit OTP_MR sets what the device does after the shutdown. With OTP_MR = 1, the device automatically wakes up after a manual reset event.

The extended EN0 event duration on EN0 is programmable from 2s to 12s with MRT[2:0]. A warning interrupt (MRWRN) is generated one timer interval before the manual reset time (i.e., MRT[2:0]-1).

Example 11: 12s EN0 assertion with an 8s manual reset time.

Comments:

- A 12s EN0 assertion with an 8s manual reset time causes the part to turn off once and restart.

Settings:

- Manual reset is enabled (MREN = 1) and manual reset time is set for 8s (MRT[2:0] = 0b101).

Stimulus:

- EN0 is asserted for 12s and then deasserted.

Result:

- At 0s, EN0 is asserted.
- After the debounce time (30ms), an EN0 assertion interrupt is generated.
- After the 1s, the EN0 1s interrupt is generated.
- After 6s, the MRWRN is generated.
- After 8s, the manual reset event is initiated and all the regulators shutdown.
- After 8.03s, the registers are reset.
- After 8.13s, a wakeup event is generated and the non-volatile event recorder's (NVERC) HDRST is set.
- After 12s, the EN0 is deasserted.
- After the debounce time (30ms) an EN0 deassertion interrupt is generated.

Example 12: 20s EN0 assertion with an 8s manual reset time.

Comments:

- A 20s EN0 assertion with an 8s manual reset time causes the part to turn off ONCE and restart.

Settings:

- Manual reset is enabled (MREN = 1) and manual reset time is set for 8s (MRT[2:0] = 0b101).

Stimulus:

- EN0 is asserted for 20s and then deasserted.

Result:

- At 0s, EN0 is asserted.
- After the debounce time (30ms), an EN0 assertion interrupt is generated.
- After the 1s, the EN0 1s interrupt is generated.
- After 6s, the MRWRN is generated.
- After 8s, the manual reset event is initiated and all the regulators shutdown.
- After 8.03s, the registers are reset.
- After 8.13s, a wakeup event is generated and the non-volatile event recorder's (NVERC) HDRST is set.
- After 20s, the EN0 is deasserted.
- After the debounce time (30ms), an EN0 deassertion interrupt is generated.

Example 13: 20s EN0 assertion with an 8s manual reset time followed by a 20s EN0 assertion.

Comments:

- The initial 20s EN0 assertion causes the part to turn off and restart once.
- The second EN0 assertion causes the part to turn off and restart again.

Settings:

- Manual reset is enabled (MREN = 1) and manual reset time is set for 8s (MRT[2:0] = 0b101).

Stimulus:

- EN0 is asserted for 20s and then deasserted for 100ms.
- EN0 is asserted again for 20s and then deasserted.

Result:

- At 0s, EN0 is asserted.
- After the debounce time (30ms), an EN0 assertion interrupt is generated.
- After the 1s, the EN0 1s interrupt is generated.
- After 6s, the MRWRN is generated.
- After 8s, the manual reset event is initiated and all the regulators shutdown.
- After 8.03s, the registers are reset.
- After 8.13s, a wakeup event is generated and the non-volatile event recorder's (NVERC) HDRST is set.
- After 20s, the EN0 is deasserted.
- After the debounce time (20.03s) an EN0 deassertion interrupt is generated.
- After 20.1, EN0 is asserted again.
- This causes the process to repeat from step #1.

EN1

EN1 is a digital input to the ON/OFF controller (Figure 18) that typically comes from the system's AP. EN1 is used to control sleep modes as shown in Figure 27. The EN1 polarity is factory programmable with OTP (OTP_EN1AL) to be active-high or active-low (Figure 21).

EN2

EN2 is an active-high digital input to the ON/OFF controller (Figure 18, Figure 22) that typically comes from the system's AP. Generally, EN2 can directly control the enable for SD0 when configured correctly. To configure EN2 to control the enable of SD0, set FPSSCR_SD0[1:0] = 0b00, PWR_MD_SD0[1:0] = 0b00, and then drive EN2 logic-low or logic-high to move between case 2 vs. case 5 as shown in Table 9. If EN2 is not needed to control SD0, then connect it to ground and use the other flexible power sequencer and/or registers to control SD0 as shown in Table 9.

Table 9. SD0 Power Mode Logic

CASE	OFF STATE	EN2	FPSx	PWR_MD_SD0[1:0]	FPSSRC_SD0[1:0]	SD0 POWER MODE
0	1	X	X	X	X	Disabled
1	0	0	X	0b00	= 0b11	Disabled
2	0	X	X	0b01	= 0b11	Group and/or dynamic low power mode
3	0	X	X	0b10	= 0b11	Low-power mode
4	0	X	X	0b11	= 0b11	Normal operating mode
5	0	1	X	0b00	X	Normal operating mode
6	0	1	X	0b01	X	Group and/or dynamic low-power mode
7	0	1	X	0b10	X	Low-power mode
8	0	1	X	0b11	X	Normal operating mode
9	0	0	0	X	≠0b11	Disabled
10	0	X	1	0b00	≠0b11	Normal operating mode
11	0	X	1	0b01	≠0b11	Group and/or dynamic low-power mode
12	0	X	1	0b10	≠0b11	Low-power mode
13	0	X	1	0b11	≠0b11	Normal operating mode

FPSx = 0 means that the specific FPS is disabled through software.

ACOK

ACOK is a digital input to the ON/OFF controller (Figure 15) that typically comes from the system's battery charger. ACOK indicates the presence/absence of the external charge adapter. The ACOK polarity is factory programmable with OTP (OTP_ACOKAL) to be active-high or active-low with the appropriate internal pullup/down (Figure 23).

LID

LID is a digital input to the ON/OFF controller (Figure 18) that typically comes from the system's battery door. LID indicates whether the battery door is open or closed. The LID polarity is factory programmable with OTP (OTP_LIDAL) to be active-high or active-low with the appropriate internal pullup/down (Figure 24).

SMPL, ALARM1, and ALARM2

SMPL, ALARM1, and ALARM2 are signal generated from the RTC and used by the ON/OFF controller as shown in (Figure 18). See the *Real-Time Clock (RTC)* section for more information on these signals.

SHDN

The shutdown input (SHDN) is a digital input to the ON/OFF controller that causes the IC to reset through a global shutdown event (Figure 1). The signal for SHDN typically comes from a temperature sensor that measures the internal die temperature of the AP. The SHDN polarity is factory programmable with OTP (OTP_SHDNAL) to be active-high or active-low with the appropriate internal pullup/down (Figure 25). A system shutdown based on SHDN is recorded in the non-volatile power-off event recorder (NVREC).

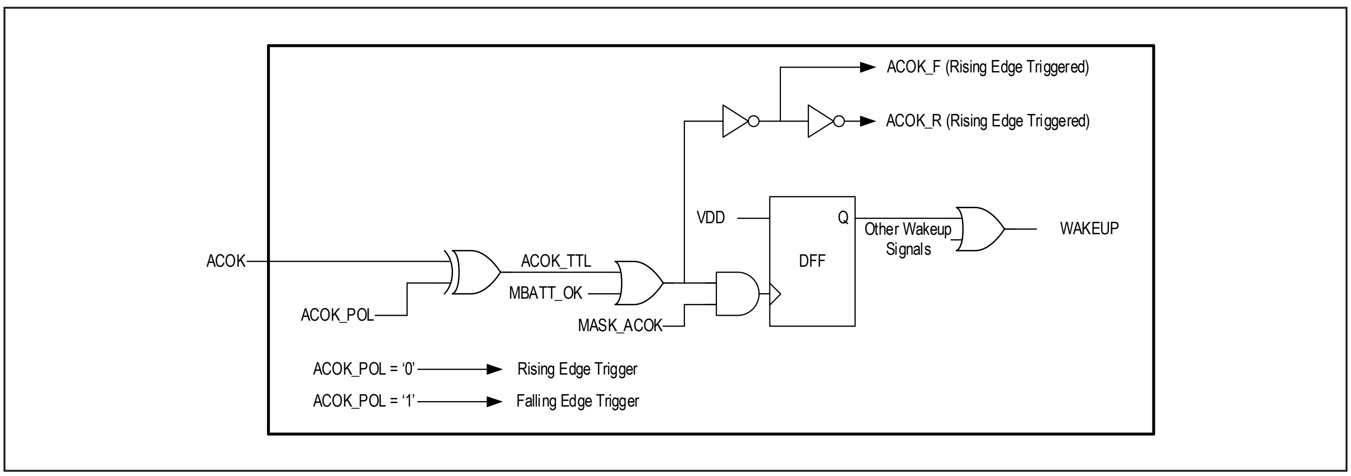


Figure 15. Functional Block Diagram for ACOK

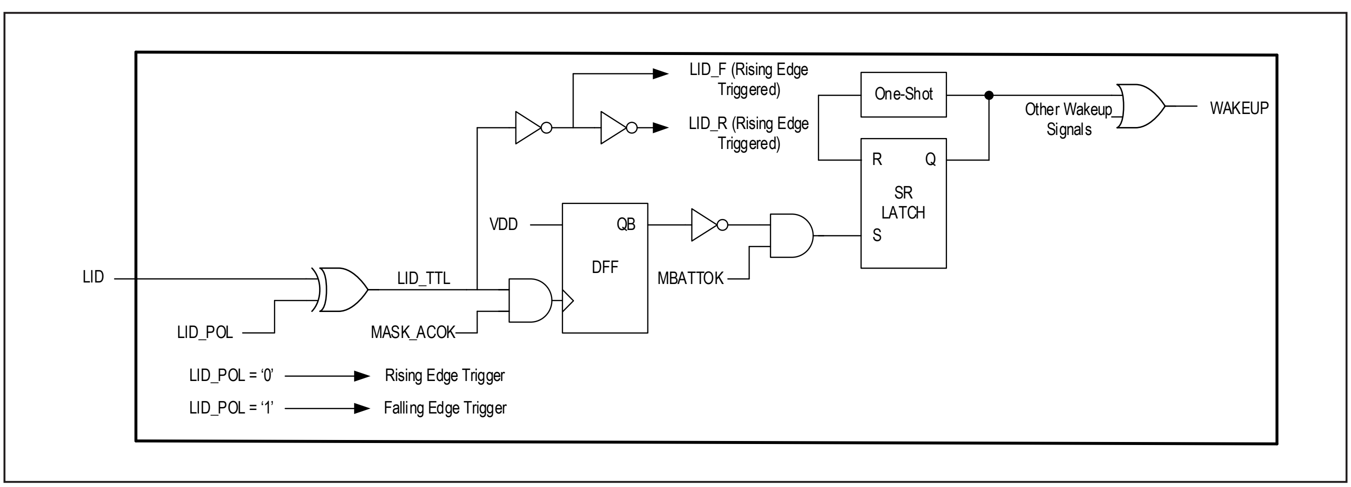


Figure 16. Functional Block Diagram for LID

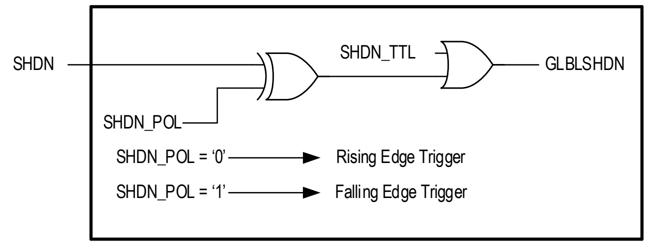


Figure 17. Functional Block Diagram for SHDN

MBATT_OK and MBATTLOW

MBATT_OK and MBATTLOW are digital signals that come from the systems' main-battery monitor (Figure 1). MBATT_OK gates several wakeup sources such that they cannot enable FPS0, FPS1, and SD0 until the battery is above the system undervoltage-lockout threshold ($V_{MBATTUVLO}$). MBATTLOW prevents FPS0, FPS1, and SD0 from being enabled when the main-battery is below a programmed minimum voltage.

FPS0

Flexible Power Sequencer 0 is the enable signal for the resources that need to be enabled when the AP is in its normal operating mode and its sleep mode. When the AP is in normal operating mode, both FPS0 and FPS1 are enabled and FPS2 is cycled on/off as needed. Figure 18, Figure 19 and Table 10 describe the behavior of FPS0 in addition to the following text description:

- FPS0 and FPS1 are enabled on EN0 rising edge if MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on EN0 rising edge if MBLPD is low and the device is not in global shutdown.
- FPS0 and FPS1 are enabled on ALARM1_R if WK_ALRM0R is high, MBATT_OK is high, MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on ALARM1_R if WK_ALRM0R is high, MBATT_OK is high, MBLPD is low and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on ALARM2_R if WK_ALRM1R is high, MBATT_OK is high, MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on ALARM2_R if WK_ALRM1R is high, MBATT_OK is high, MBLPD is low and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on SMPL_EVENT if SMPL_EN is high, MBATT_OK is high, MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on SMPL_EVENT if SMPL_EN is high, MBATT_OK is high, MBLPD is low and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on LID if WK_LID is high, MBATT_OK is high, MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on LID if WK_LID is high, MBATT_OK is high, MBLPD is low and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on ACOK if WK_ACOK is high, MBATT_OK is high, MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS0 and FPS1 are enabled on ACOK if WK_ACOK is high, MBATT_OK is high, MBLPD is low and the IC is not in global shutdown.
- FPS0 is disabled on global shutdown.
- FPS0 is disabled when PWR_OFF is set.
- FPS0 is disable if MBLPD is high and MBATTLOW is high.

FPS1

Flexible Power Sequencer 1 is the enable signal for the resources that need to be enabled when the AP is in its normal operating mode and disabled when the AP is in sleep mode. When the AP is in normal operating mode, both FPS0 and FPS1 are enabled and FPS2 is cycled on/off as needed.

Figure 18, Figure 19, and Table 10 describe the behavior of FPS1 in addition to the following text description:

- See all FPS1 enable conditions listed in the *FPS0* section. Note that if only FPS0 is on but a wakeup event occurs, then FPS1 is enabled.
- FPS1 is enabled on EN1 rising edge if, MBATTLOW is low, MBLPD is high, and the IC is not in global shutdown.
- FPS1 is enabled on EN1 rising edge if MBLPD is low, and the IC is not in global shutdown.
- FPS1 is disabled on global shutdown.
- FPS1 is disabled on EN1 falling edge if SLPEN is high.
- FPS1 is disabled when PWR_OFF is set.
- FPS1 is disabled if MBLPD is high and MBATTLOW is high.

Table 10. ON/OFF Controller State Diagram Transitions

TRANSITION	CONDITION
1	The fundamental system voltages and resources are available. Move to the OFF state. • The battery voltage is not undervoltage ($V_{MBATT} > V_{MBATTUVLO}$)
2	A wakeup signal has been received. Move the “OK?” state to check to see if the system is okay to wakeup. • A debounced EN0 press (i.e., edge) has been detected OR • ALARM1_R event occurs and WK_ALRM0R is set OR • ALARM2_R event occurs and WK_ALRM1R is set OR • SMPL_EVENT occurs and SMPL_EN is set OR • LID event (i.e., edge) occurs and WK_LID is set OR • ACOK event (i.e., edge) occurs and WK_ACOK is set OR • WAKEUP flag is set by the previous sequenced shutdown
2A	The basic system resources are okay. • All ‘2B’ transition conditions are not true AND all ‘2C’ transition conditions are not true AND MBATTLOW = 0
2B	Failed attempt to power up because the battery voltage is too low. The battery voltage is low (MBATTLOW = 1) AND the ‘2’ transition was not ACOK. OR The battery voltage monitor is set for main-battery low power down (MBLPD = 1) AND the battery voltage is low (MBATTLOW = 1) AND the ‘2’ transition is ACOK. OR The battery voltage monitor is AND not set for main-battery low power down (MPLPD = 0) AND the battery voltage is low (MBATTLOW = 1) AND the ‘2’ transition was ACOK, then the machine remains in the “OK?” state waiting for MBATTLOW = 0. Once MBATTLOW = 0, then a transition along path ‘2A’ occurs. This ‘2B’ transition condition cancels the wakeup requests that occurred in transition ‘2’.
2C	Failed attempt to power up because a basic system resource was not okay. • The battery voltage is undervoltage ($V_{MBATT} < V_{MBATTUVLO}$) OR • The battery voltage is overvoltage ($V_{MBATT} > V_{MBATTOVLO}$) OR • AVSD input is overvoltage ($V_{AVSD} > V_{MBATTOVLO}$) OR • The junction temperature is too high ($T_J > T_{JSHDN}$) OR • SHDN pin is asserted (SHDN = 1)

Table 10. ON/OFF Controller State Diagram Transitions (continued)

TRANSITION	CONDITION
3	Enter sleep mode. • Sleep mode is enabled (SLPEN = 1) and EN1 transitions from high to low.
4	Exit sleep mode. • Sleep mode is enabled (SLPEN = 1) and EN1 transitions from low to high. • A debounced EN0 press has been detected OR • ALARM1_R event occurs and WK_ALRM0R is set OR • ALARM2_R event occurs and WK_ALRM1R is set OR • LID event occurs and WK_LID is set OR • ACOK event occurs and WK_ACOK is set
5	Enter the power-down sequence with register reset (see Figure 4). • The low battery power-down is enabled (MBLPD = 1) AND the battery voltage is low (MBATTLOW = 1) OR • Hardware reset input (RSI) event detected OR • Manual reset event detected OR • Watchdog timer expires OR • SFT_RST = 1 OR • PWR_OFF = 1
6	Immediate shutdown (see Figure 4). • The battery voltage is undervoltage ($V_{MBATT} < V_{MBATTUVLO}$) OR • The battery voltage is overvoltage ($V_{MBATT} > V_{MBATTOVLO}$) OR • AVSD input is overvoltage ($V_{AVSD} > V_{MBATTOVLO}$) OR • The junction temperature is too high ($T_J > T_{JSHDN}$) OR • SHDN pin is asserted (SHDN = 1)

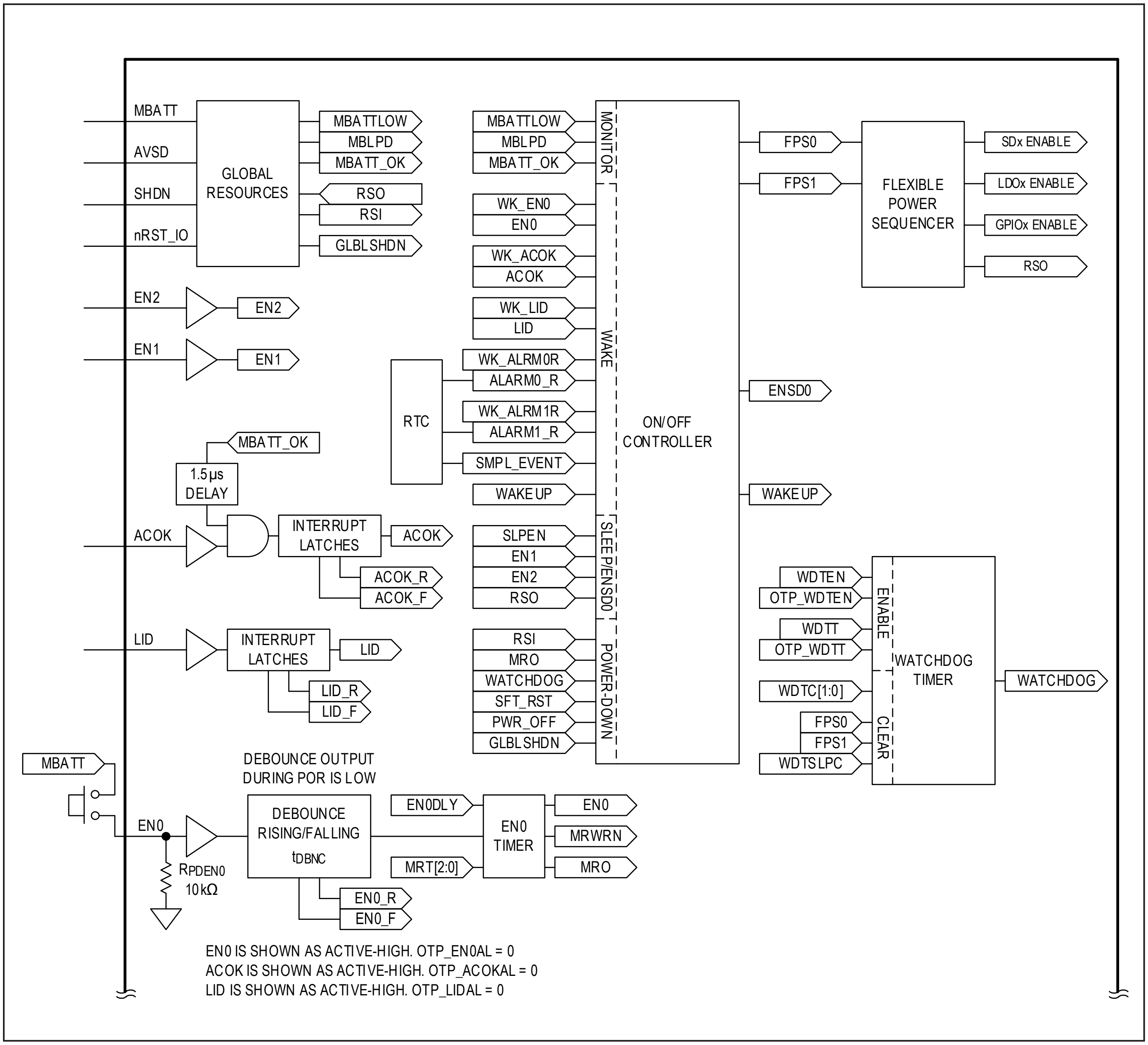


Figure 18. Simplified Block Diagram: ON/OFF Controller

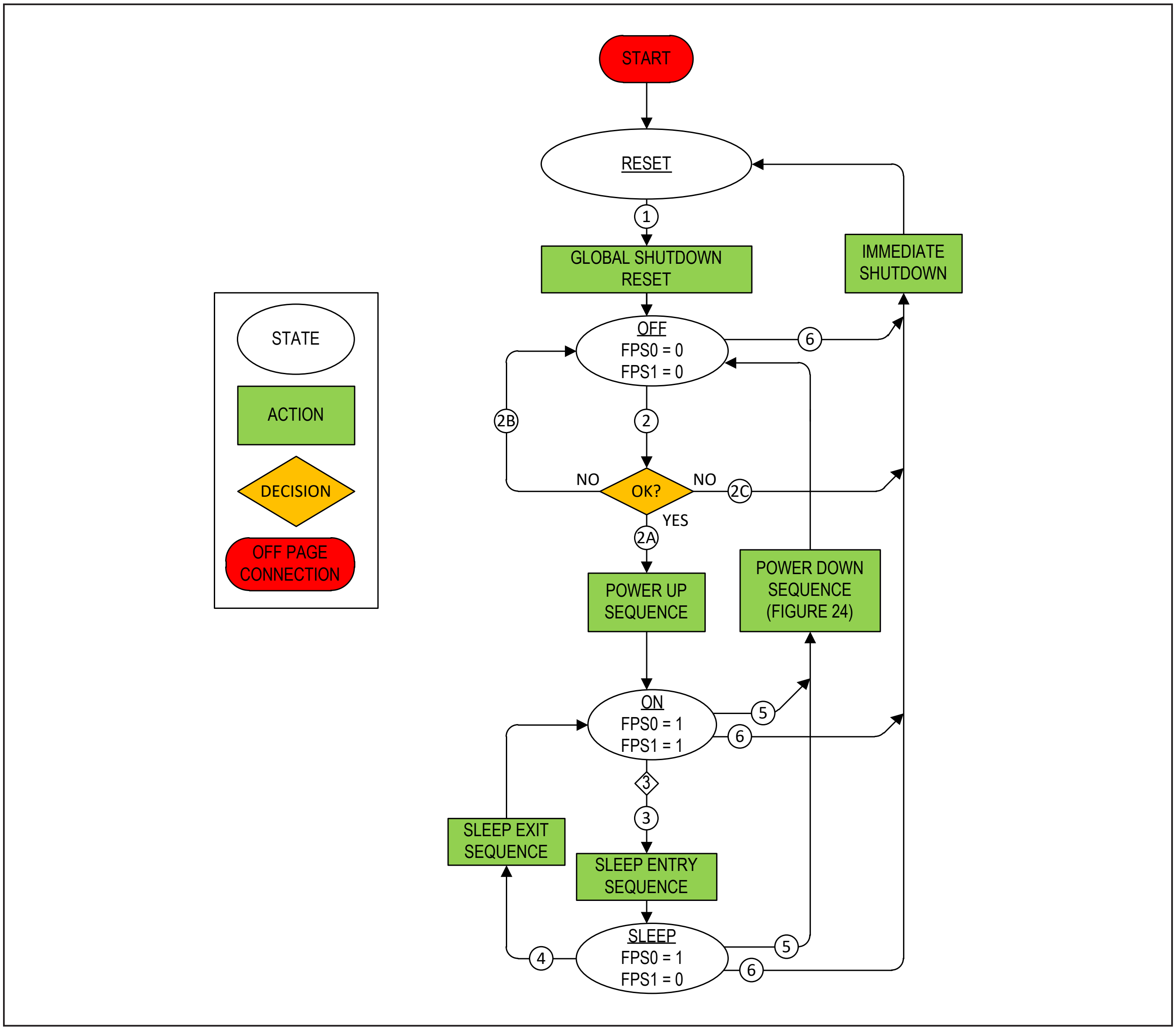


Figure 19. State Diagram: ON/OFF Controller

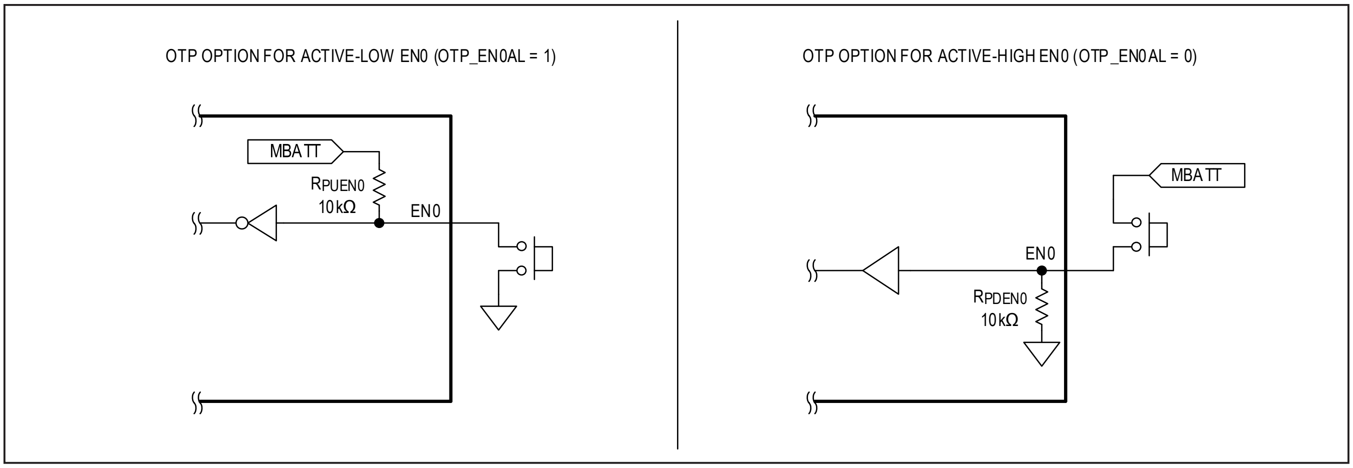


Figure 20. EN0 Simplified Input Stage: Active-High or Low

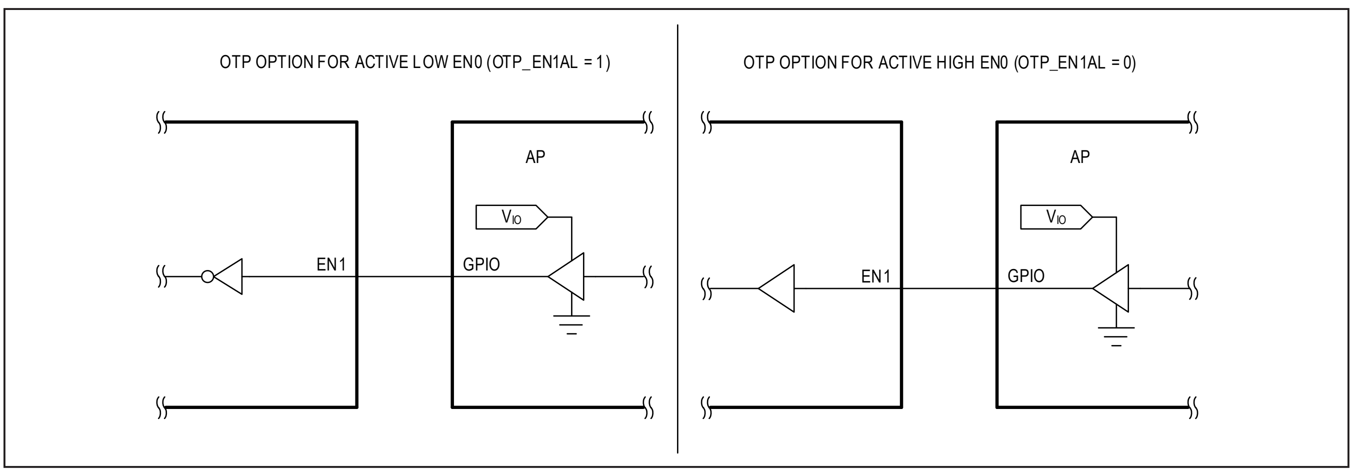


Figure 21. EN1 Simplified Input Stage: Active-High or Low

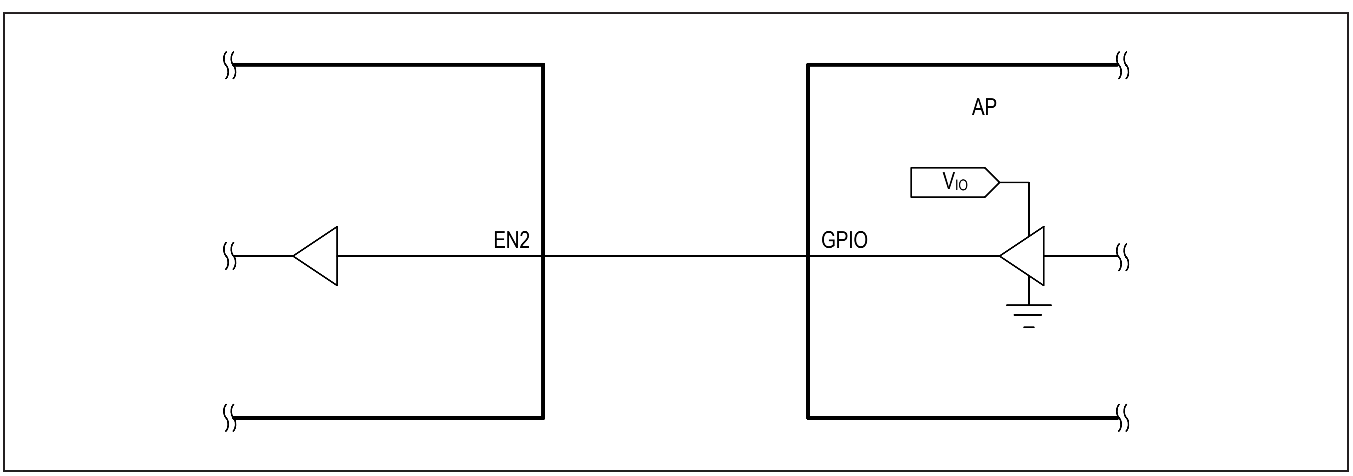


Figure 22. EN2 Simplified Input Stage: Active-High or Low

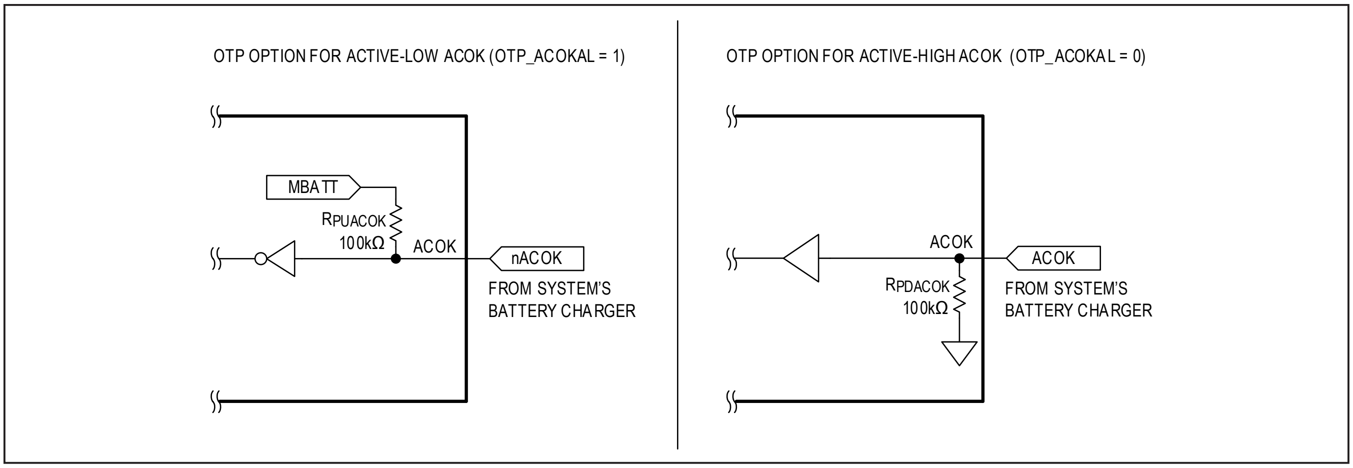


Figure 23. ACOK Simplified Input Stage: Active-High or Low

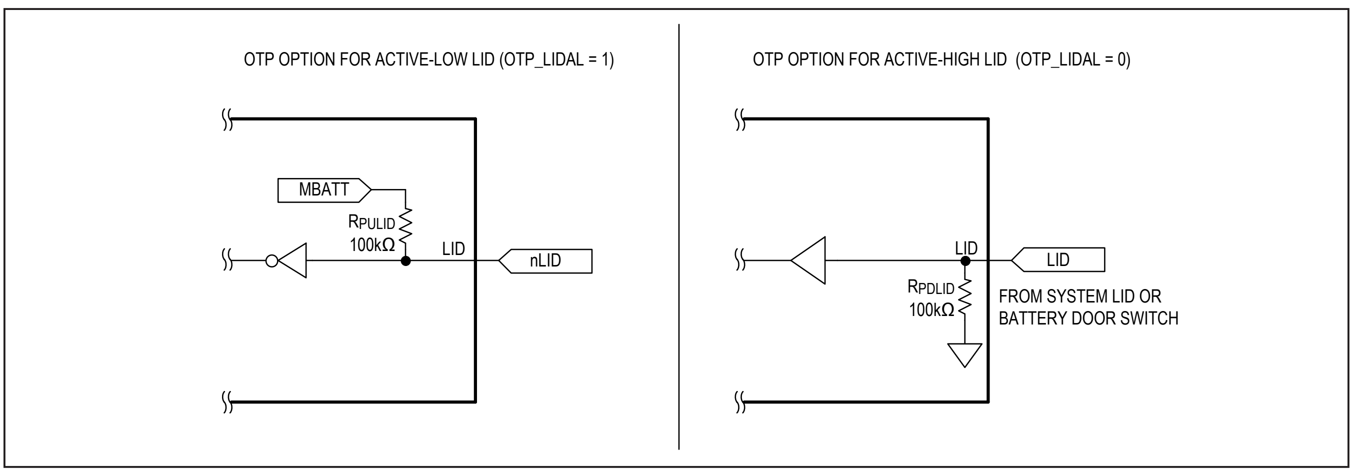


Figure 24. LID Simplied Input Stage: Active-High or Low

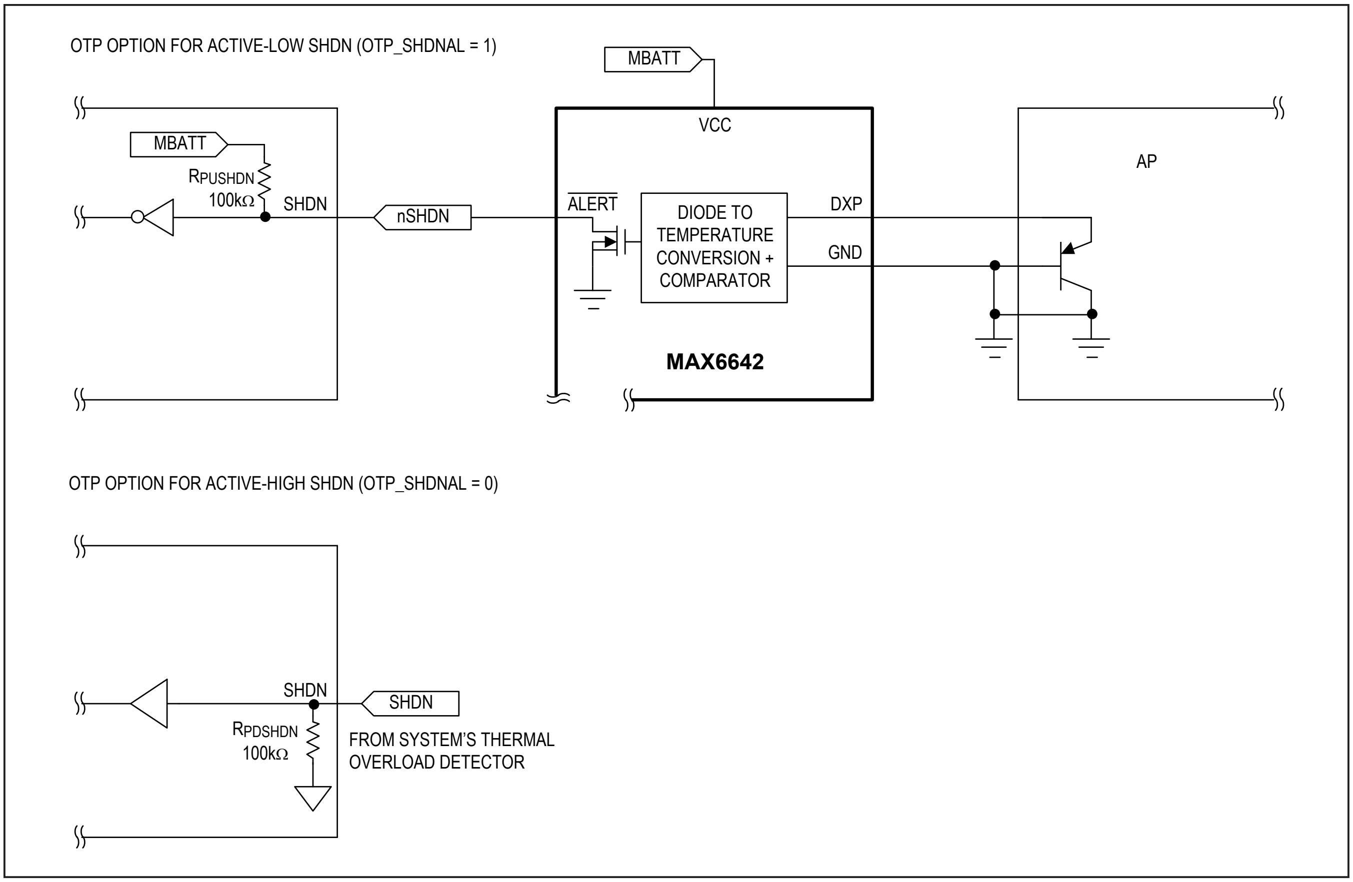
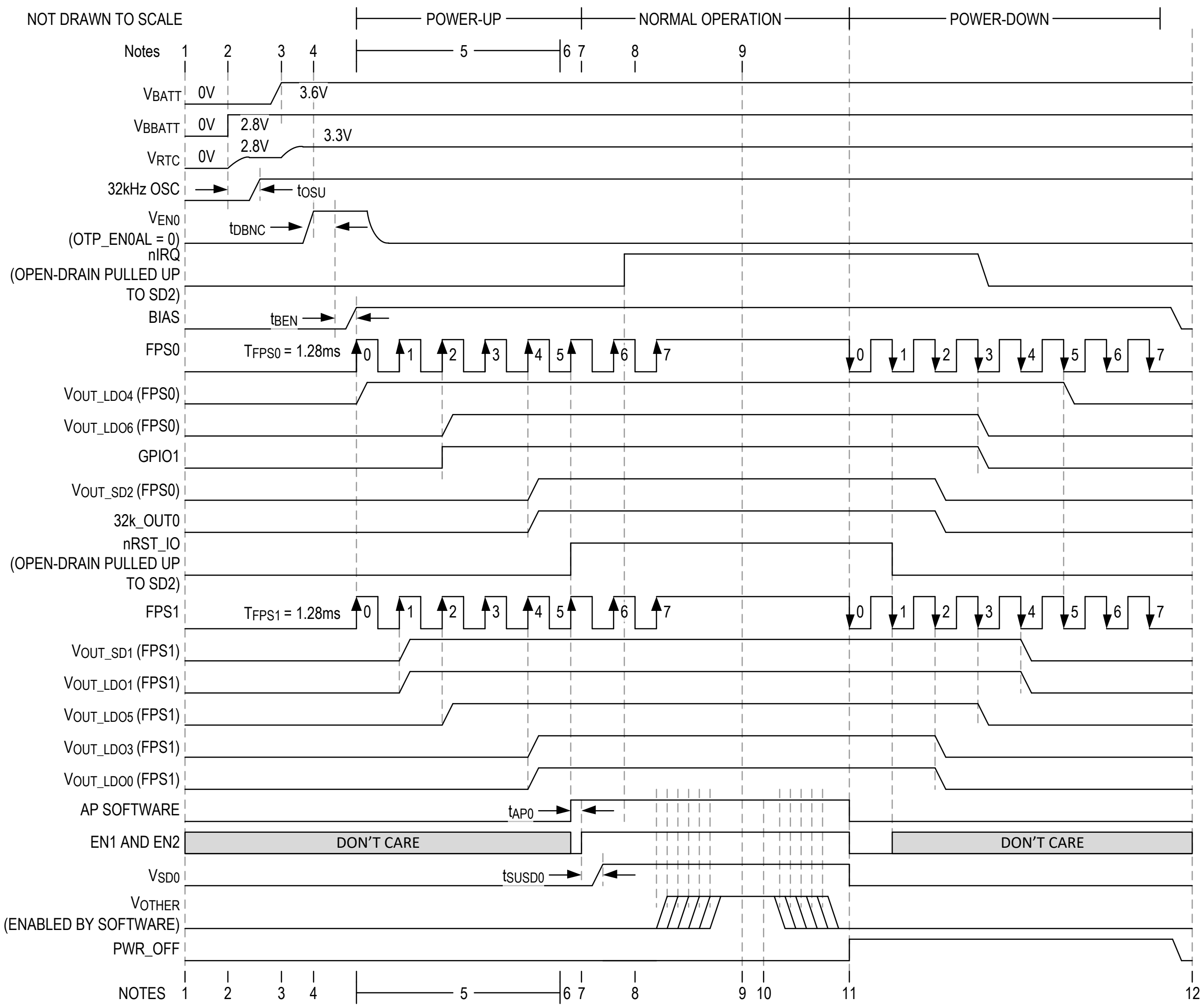
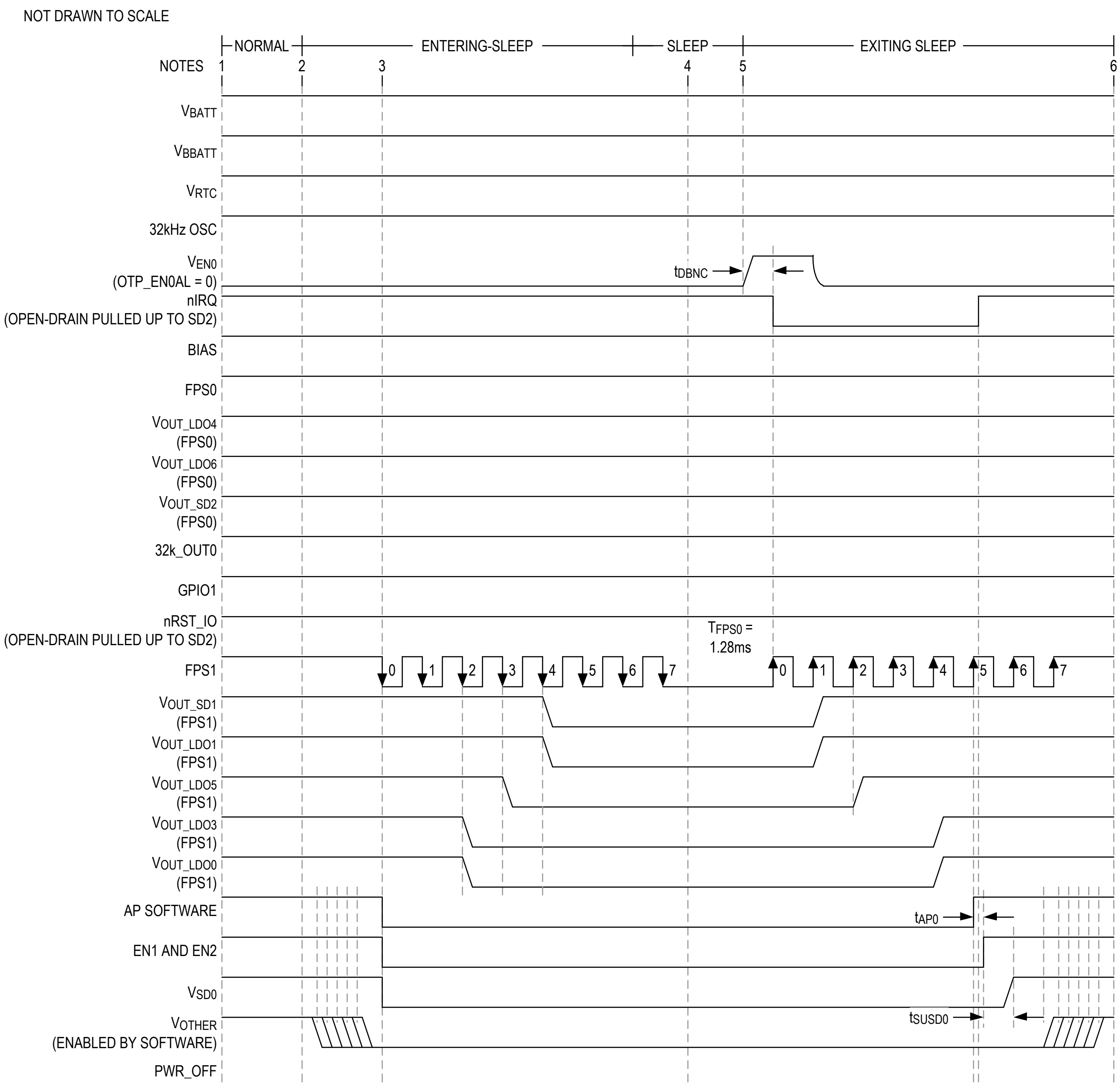


Figure 25. SHDN Simplified Input Stage: Active-High or Low



1) THE AP AND ENTIRE SYSTEM IS OFF WITH NO BACKUP BATTERY AND NO MAIN BATTERY INSTALLED.
2) A HALF-CHARGED LITHIUM MANGANESE CELL IS INSTALLED FROM BBATT TO GND. V_{RTC} RISES TO ~V_{BBATT}. THE RTC RELATED PORTION OF THE I^2C REGISTER MAP POWERS UP TO ITS DEFAULT VALUE. THE OSCILLATOR STARTS TO FUNCTION AND THE RTC BLOCK BEGINS TO FUNCTION.
3) THE MAIN BATTERY IS CONNECTED. V_{RTC} RISES UP TO ITS 3.3V REGULATION LEVEL. THE BACKUP-BATTERY CHARGER DEFAULTS TO "ON" WITH A 2.5V REGULATION THRESHOLD. THE NON-RTC RELATED I^2C REGISTERS GO TO THEIR DEFAULT VALUES.
4) AN EXTERNAL EVENT PULLS EN0 HIGH. THE DEVICE DEBOUNCES EN0 AND STARTS THE BIAS FOLLOWED BY FPS0 AND FPS1.
5) FPS0 STARTS THE FUNDAMENTAL REGULATORS AT THE SAME TIME AS FPS1 STARTS THE SECONDARY REGULATORS.
6) FPS0 DEASSERTS nRST_IO ON ITS RISING EDGE #5. WITH nRST_IO HIGH, THE AP STARTS RUNNING SOFTWARE.
7) AP ASSERTS EN1 AND EN2. EN1 KEEPS THE FPS1 REGULATORS ENABLED. EN2 STARTS SD0.
8) WITH SD0 ENABLED, THE AP CONTINUES TO RUN SOFTWARE. IT CHECKS THE nIRQ INTERRUPT CAUSING nIRQ TO GO HIGH. IT POWERS UP THE "OTHER" RESOURCES OF THE DEVICE AS REQUIRED.
9) THE AP AND ENTIRE SYSTEM ARE ON IN NORMAL OPERATING MODE.
10) THE AP DECIDES IT WANTS TO POWER DOWN AND IT POWERS DOWN THE OPTIONAL RESOURCES OF THE SYSTEM AND PMIC.
11) WITH ALL THE OPTIONAL RESOURCES POWERED DOWN, THE AP SETS TO "OFF" BIT AND PULLS EN1 AND EN2 LOW. EN2 LOW TURNS DISABLES SD0. THE OFF BIT STARTS THE POWER DOWN SEQUENCE OF FPS0 AND EN1 LOW STARTS THE POWER DOWN SEQUENCE OF FPS1.
12) AFTER THE FPS0 AND FPS1 POWER DOWN SEQUENCES ARE FINISHED, THE BIAS TURNS OFF AND THE AP IS OFF.

Figure 26. Application Processor Power-Up and Power-Down Timing



1) THE AP AND ENTIRE SYSTEM ARE ON AND IN NORMAL OPERATING MODE.
2) THE AP DECIDES IT WANTS TO POWER DOWN AND IT POWERS DOWN THE OPTIONAL RESOURCES OF THE SYSTEM AND PMIC.
3) WITH ALL THE OPTIONAL RESOURCES POWERED DOWN, THE AP AND PULLS EN1 AND EN2 LOW. EN2 LOW TURNS DISABLES SD0. EN1 LOW STARTS THE POWER DOWN SEQUENCE OF FPS1.
4) AFTER THE FPS1 POWER DOWN SEQUENCES ARE FINISHED, THE AP IS IN SLEEP.
5) AN EN0 BUTTON PRESS GENERATES A WAKEUP EVENT THAT TURNS FPS1 ON.
6) WITH THE FPS1 POWER UP SEQUENCE FINISHED, THE AP IS IN ITS NORMAL OPERATING MODE.

Figure 27. Application Processor Entering and Exiting Sleep Timing

Nonvolatile Power-OFF Event Recorder

Several events within an IC based system can autonomously cause a power off (i.e., global shutdown). The source of the power down event is recorded in a non-volatile register such that when the system's microprocessor powers on again it can determine the source of the previous power-off condition. Maxim recommends that as part of the software's initialization code, it check the NVERC register. This power-off event recorder register is non-volatile as long as the RTCs coin cell (BBATT) remains within its valid voltage range. Unlike most interrupt registers, the NVERC register does not have a corresponding interrupt mask and status register. Additionally, it does not affect the nIRQ pin. No status register is provided since all NVERC events result in a global shutdown which would subsequently reset any related status.

Flexible Power Sequencer (FPS)

The FPS allows each regulator to power up under hardware or software control. Additionally, each regulator can power on independently or among a group of other regulators with an adjustable power-up and power-down delays (sequencing). GPIO1, GPIO2, and GPIO3 can be programmed to be part of a sequence allowing external regulators to be sequenced along with internal regulators. nRST_IO can be programmed to be part of a sequence.

Figure 26 shows LDO0, LDO1, LDO2, and LDO3 powering up under the control of flexible power sequencer 2.

The flexible sequencing structure consists of two hardware enable inputs (EN0, EN1), and three master sequencing timers. Each master sequencing timer is programmable through its configuration register to have a hardware enable source or a software enable source (CNFGFPSx). When enabled/disabled the master sequencing timer generates eight sequencing events. The time period between each event is programmable within the configuration register. An internal 800kHz silicon oscillator is used to generate the eight combinations of the FPS timing period TFPSx[2:0]. This oscillator is turned on once a valid wakeup signal is received.

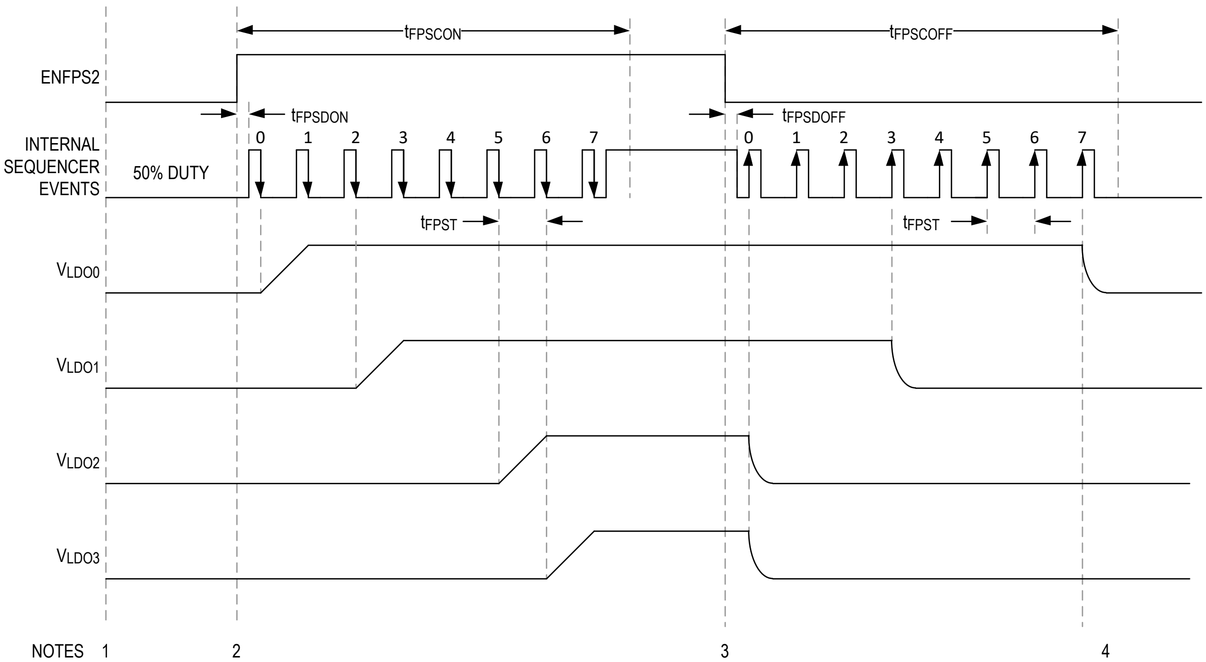
Each regulator, GPIO1, GPIO2, GPIO3, and nRST_IO has a flexible power sequence slave register (FPS_x) which allows its enable source to be specified as a flexible power sequencer timer or a software bit. When a FPSSRCx specifies the enable source to be a flexible power sequencer, the power up and power down delays are configured by FPSPUx[2:0] and FPSPDx[2:0]. can be specified in that regulators flexible power sequencer configuration register.

If any of the FPS hardware inputs (EN0, EN1) are not needed, connect them to ground. Grounding these inputs when they are not needed ensures that they do not accidentally turn on any voltage regulators—furthermore, it improves the thermal impedance of the IC package.

Table 11 shows one possible configuration of the flexible power sequencer. Figure 26 and Figure 27 show the timing diagrams for the default flexible power sequencer settings.

Features

- Three Sequencers
- Power-Up and Power-Down Sequencing Control
- Eight Power-Up Sequence Time Slots
- Eight Power-Down Sequence Time Slots
- Adjustable Time Period Between Time Slots from 40μs to 5,120μs in Eight Binary Weighted Steps
- Sequence Enable/Disable can be Controlled by Hardware and Software
- <10μs Sequencer Delay
- Capable of Controlling:
  - All Regulators
  - GPIO1, GPIO2, and GPIO3
  - nRST_IO



1) LDO0, LDO1, LDO2, AND LDO3 ARE OFF. EACH LDO'S ENABLE REGISTER SELECTS ACTIVE DISCHARGE ENABLED AND FPS2 AS THE ENABLE SOURCE. EACH LDO'S FLEXIBLE SEQUENCER CONFIGURATION REGISTER IS PROGRAMMED WITH THE POWER-UP AND POWER-DOWN TIMING DELAYS AS SHOWN IN THE FIGURE. THE CNFGFPS2 REGISTER SELECTS THE ENFPS2 BIT AS THE ENABLE SOURCE.
2) THE ENFPS2 BIT IS SET HIGH WHICH CAUSES EIGHT INTERNAL SEQUENCING EVENTS. EACH REGULATOR IS ENABLED AT THE SEQUENCING EVENT THAT CORRESPONDS TO ITS FLEXIBLE SEQUENCER CONFIGURATION REGISTER.
3) THE ENFPS2 BIT IS CLEARED TO LOW WHICH CAUSES AND EIGHT INTERNAL SEQUENCING EVENTS. EACH REGULATOR IS DISABLED AT THE SEQUENCING EVENT THAT CORRESPONDS TO ITS FLEXIBLE SEQUENCER CONFIGURATION REGISTER.
4) LDO0, LDO1, LDO2, AND LDO3 ARE OFF.

Figure 28. Example Timing Diagram: Flexible Power Sequencer

Table 11. Example Configuration of the Flexible Power Sequencer

FPS MASTER CONFIGURATION	TIMER PERIOD (MS)	ENABLE SOURCE	FPS SLAVE CONFIGURATION	ENABLE SOURCE	POWER UP DELAYS	POWER DOWN DELAYS
FPS0	1.28	EN0	SD0	Bit or EN2	N/A	N/A
FPS1	1.28	EN1	SD1	FPS1	3	4
FPS2	N/A	N/A	SD2	FPS1	6	2
			SD3	BIT	N/A	N/A
			LDO0	FPS1	6	2
			LDO1	FPS1	3	4
			LDO2	BIT	N/A	N/A
			LDO3	FPS1	6	2
			LDO4	FPS0	2	5
			LDO5	FPS1	3	3
			LDO6	FPS0	4	3
			LDO7	BIT	N/A	N/A
			LDO8	BIT	N/A	N/A
			GPIO1	FPS0	4	3
			GPIO2	FPS0	0	7
			GPIO3	AME3 = 0	N/A	N/A
			nRESET_OUT	FPS0	7	1

Commitment Time

If the FPS begins a power-up sequence, it is committed to completing that sequence (see t_{FPSCON} in Figure 28). In other words, if the FPS begins a power-up sequence, and then a power-down event (such as RSI) is initiated before the power-up is complete, that power-down event waits in a queue and executes after the FPS power-up sequence is complete. Similarly, if the FPS begins a power-down sequence, it is committed to completing that sequence (see $t_{FPSCOFF}$ in Figure 28). In other words, if the FPS begins a power-down sequence, and then a power-up event (such as ACOK) is initiated before the power-down is complete, that power-up event waits in a queue and executes after the FPS power-up sequence is complete. Note that the above comments are applicable to all resources that can be assigned to the FPS (GPIO, BUCK, LDO).

Changing Regulator Enable Source

The FPS allows the regulator enable sources to be changed at any time. Table 12 illustrates what happens when changing enable sources.

Example 14: Powering up ten regulators on sequencer 1 and then reassigning three of them to sequencer 2.

Table 12. Changing Enable Sources Behavior

EXISTING ENABLE SOURCE: STATE	NEW ENABLE SOURCE: STATE	REGULATOR BEHAVIOR
FPS or software: enabled	FPS or software: disabled	Turns off within 6.6μs
FPS or software: disabled	FPS or software: enabled	Turns on within 6.6μs
FPS: enabled	FPS or software: enabled	Remains on
Software: enabled	FPS: enabled	Remains on
FPS or software: disabled	FPS or software: disabled	Remains off

Note an FPS enabled source is any of the seven flexible power sequencers, a software enabled source is the dedicated enable bit that is in location B0 of each regulator's enabled register.

Ten regulators are assigned to FPS#1 and enabled in a given sequence. No regulators are assigned to FPS#2 but FPS#2 is enabled. Then, three of the regulator enable sources are changed from FPS#1 to FPS#2. Since both FPS#1 and FPS#2 are enabled during the change, the regulators remain on. Finally, the three regulators on FPS#2 can then be enabled/disabled independently.

I2C Interface and Interrupt Output

The IC features a revision 3 I2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). The IC acts as a slave-only device where it relies on the master to generate a clock signal. SCL clock rates from 0Hz to 3.4MHz are supported.

I2C is an open-drain bus and therefore SDA and SCL require pullup resistors. Optional resistors (24Ω) in series with SDA and SCL protect the device inputs from high-voltage spikes on the bus lines. Series resistors also minimize cross-talk and undershoot on bus signals.

Figure 29 shows the functional diagram for the I2C based communications controller. For additional information on I2C, refer to the I2C-bus specification and user manual that is available from NXP (document title: **UM10204**).

Features

- I2C Revision 3 Compatible Serial Communications Channel
  - 0Hz to 100kHz (Standard Mode)
  - 0Hz to 400kHz (Fast Mode)
  - 0Hz to 1MHz (Fast-Mode Plus)
  - 0Hz to 3.4MHz (High-Speed Mode)
- Does not Utilize I2C Clock Stretching
- I2C Watchdog Timer

I2C System Configuration

The I2C bus is a multi-master bus. The maximum number of devices that can attach to the bus is only limited by bus capacitance.

Figure 30 shows an example of a typical I2C system. A device on the I2C bus that sends data to the bus in called a ”transmitter”. A device that receives data from the bus is called a “receiver”. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a “master.” Any device that is being addressed by the master is considered a “slave.” The IC is a slave on the I2C bus and it can be both a transmitter and a receiver.

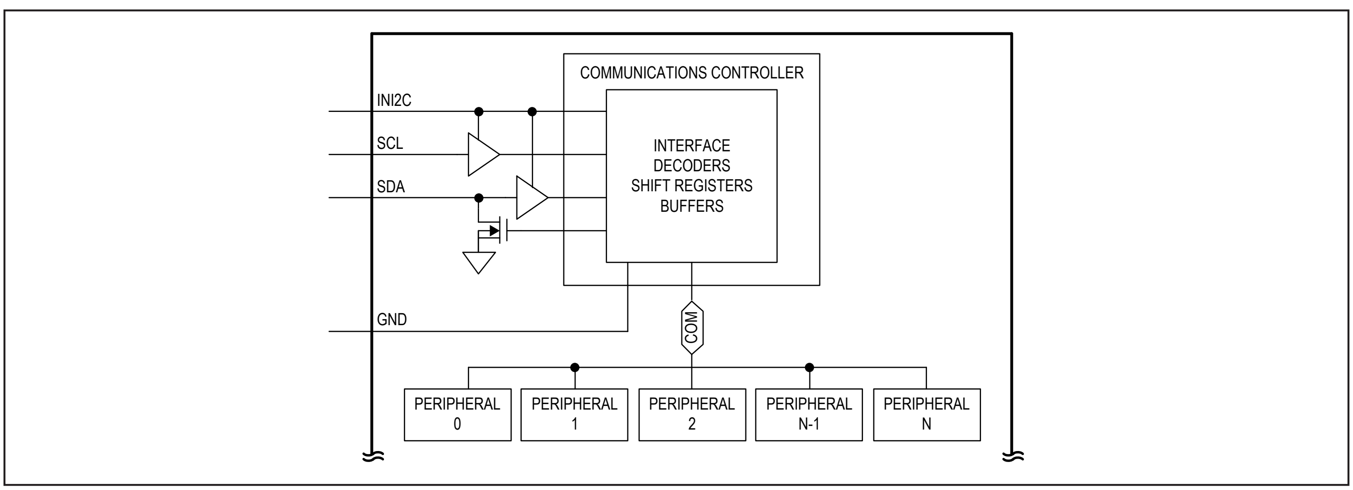


Figure 29. Functional Logic Diagram: Communications Controller

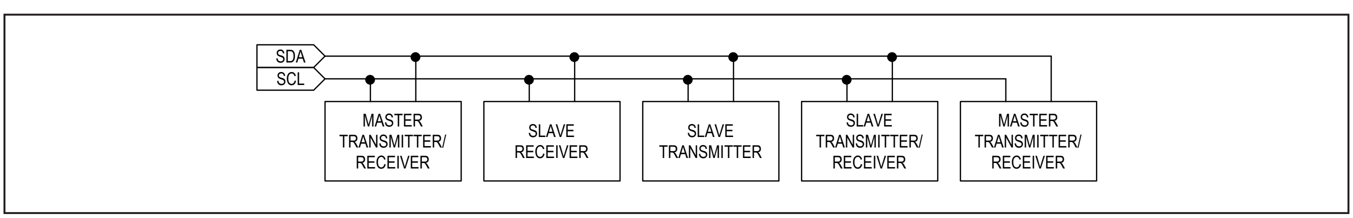


Figure 30. Functional Logic Diagram: Communications Controller

I2C Interface Power

The I2C interface derives its power from INI2C. Typically, a power input such as INI2C would require a local 0.1μF ceramic bypass capacitor to ground. However, in highly integrated power distribution systems, a dedicated capacitor may not be necessary. If the impedance between INI2C and the next closest capacitor (≥ 0.1μF) is less than 100mΩ in series with 10nH, then a local capacitor is not needed. Otherwise, place a local 0.1μF ceramic bypass capacitor from INI2C to ground.

INI2C accepts voltages from 1.7V to 3.6V (V_{INI2C}). Cycling V_{INI2C} does not reset the I2C registers.

I2C Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals (see the *I2C Interface and Interrupt Output* section).

Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is nine bits long: eight bits of data followed by the acknowledge bit. Data is transferred with the MSB first.

I2C Start and Stop Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA, while SCL is high (Figure 32).

A START condition from the master signals the beginning of a transmission to the IC. The master terminates transmission by issuing a not-acknowledge followed by a STOP condition (see the *I2C Acknowledge Bit* section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated start (Sr) commands instead of a STOP command in order to maintain control of the bus. In general, a repeated start command is functionally equivalent to a regular start command.

When a STOP condition or incorrect address is detected, the IC internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feed-through.

I2C Acknowledge Bit

Both the I2C bus master and the IC (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each nine-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse (Figure 33). To generate a not-acknowledge (nA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

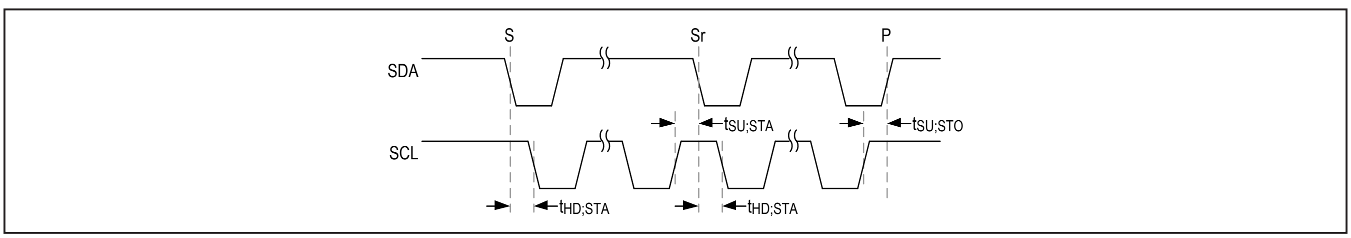


Figure 31. START and STOP Conditions

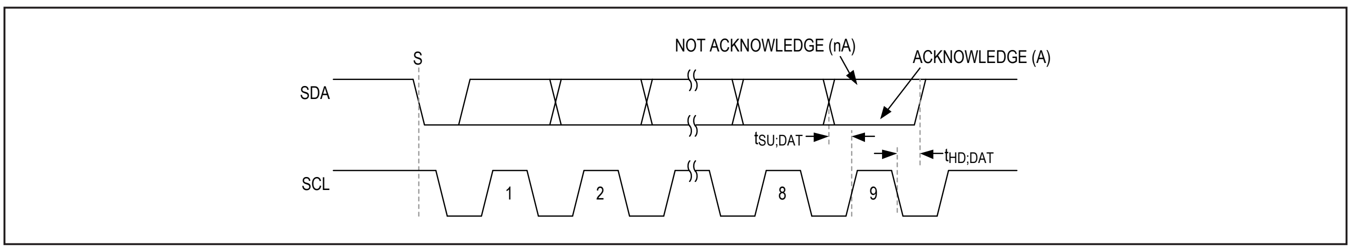


Figure 32. Acknowledge Bits

I^2C Slave Address

The IC implements 7-bit slave addressing. An I^2C bus master initiates communication with a slave device (MAX77863) by issuing a START condition followed by the slave address. As shown in Table 13, the IC slave addresses are factory programmable with OTP_I2CADDR[1:0]. With any one programming option of OTP_I2CADDR[1:0], the IC responds to only four slave addresses; all other slave addresses are ignored.

Figure 33 is an example of the slave address byte format using the RTCs slave address. As shown, the slave address byte consists of seven address bits and a read/write bit (R/nW). After receiving any of the slave addresses shown in Table 13, the IC issues an acknowledge by pulling SDA low during the ninth clock cycle.

I^2C Clock Stretching

In general, the clock signal generation for the I^2C bus is the responsibility of the master device. The I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The IC does not use any form of clock stretching to hold down the clock line.

I^2C General Call Address

The IC does not implement the I^2C specifications "general call address." If the IC sees the general call address (0b0000_0000), it does not issue an acknowledge.

I^2C Watchdog Timer

The IC contains an I^2C watchdog timer to ensure reliable operation of the I^2C bus. This I^2C watchdog timer helps the system recover from I^2C bus hang-ups that can occur when devices on an I^2C bus operate out of sync from each other due to noise or poor system design.

In many cases, I^2C bus hang-ups can be cleared by the master. The master can clear the I^2C bus by issuing nine consecutive stop commands. In all known cases, the device's I^2C state machine is cleared whenever the master issues nine consecutive stop commands. However, to account for unforeseen system issues, the I^2C watchdog timer serves as a backup protection method for I^2C bus hang-ups.

The I^2C watchdog timer is disabled by default. With the I^2C watchdog timer disabled, the device meets the 0Hz SCL frequency requirements in the I^2C specification (**UM10204**). In many cases, this 0Hz capability is not needed. Activating the I^2C watchdog timer defeats the 0Hz specification of I^2C.

Table 13. MAX77863 I^2C Slave Addresses

OTP_ I2C ADDR[1:0]	RTC SLAVE ADDRESS WRITE	RTC SLAVE ADDRESS READ	PMIC/GPIO SLAVE ADDRESS WRITE	PMIC/GPIO SLAVE ADDRESS READ
0b00	0x90, 0b1001_0000	0x91, 0b1001_0001	0x38, 0b0011_1000	0x39, 0b0011_1001
0b01	0x94, 0b1001_0100	0x95, 0b1001_0101	0x3C, 0b0011_1100	0x3D, 0b0011_1101
0b10	0xD0, 0b1101_0000	0xD1, 0b1101_0001	0x78, 0b0111_1000	0x79, 0b0111_1001
0b11	0xD4, 0b1101_0100	0xD5, 0b1101_0101	0x7C, 0b0111_1100	0x7D, 0b0111_1101

Slave Address is constructed with M, O, M, M, M, O, M, R/nW
where:

M = bit fixed in metal
O = factory programmable OTP bit
R/nW = user controlled Read/Write bit

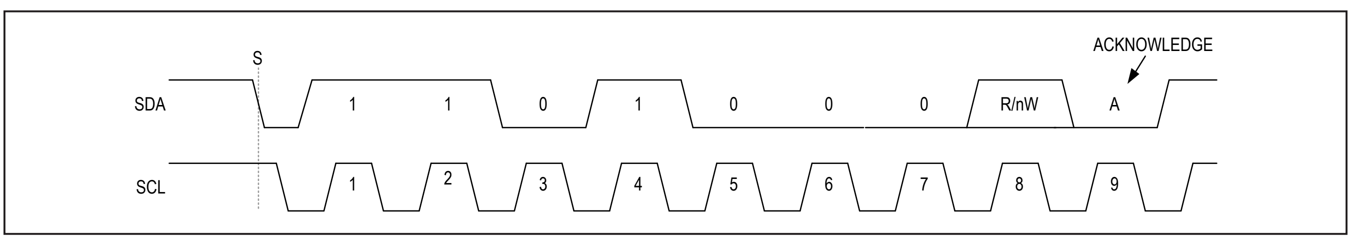


Figure 33. Slave Address Byte Example Using the Power Management Slave Address

Enable the I^2C watchdog timer with the I2CTWD[1:0] bits. With the I^2C watchdog timer enabled, the device monitors the time between a START and STOP condition. If this time ever exceeds the programmed I^2C watchdog timer period, the MAX77863 I^2C state machine is reset.

Note that the IC contains both a system watchdog timer and an I^2C watchdog timer. See the *System Watchdog Timer* section for more information.

I^2C Communication Speed

The IC is compatible with all four communication speed ranges as defined by the revision 3 I^2C specification:

- 0Hz to 100kHz (standard mode)
- 0Hz to 400kHz (fast mode)
- 0Hz to 1MHz (fast-mode plus)
- 0Hz to 3.4MHz (high-speed mode)

Operating in standard mode, fast mode, and fast-mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C x R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the "*Pullup Resistor Sizing*" section of the I^2C Revision 3 specification for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs about 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, see the I^2C specification. The major considerations with respect to the MAX77863 are:

- The I^2C bus master uses current source pullups to shorten the signal rise times.
- The I^2C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols need to utilize the high-speed master code.

At power-up and after each stop condition, the device input filters are set for standard mode, fast mode, or fast-mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *I^2C Communication Protocols* section.

I^2C Communication Protocols

The IC supports both writing and reading from its registers. Table 13 shows the I^2C communication protocols for each functional block. The power management and GPIO functions use the same communications protocols. The *Real-Time Clock (RTC)* section does not support the "writing multiple bytes using register-data pairs" protocol—instead, the *Real-Time Clock (RTC)* section supports the "writing to sequential registers" protocol.

Table 14. I^2C Communication Protocols Supported by Different Functional Blocks

POWER MANAGEMENT AND GPIO	RTC
Writing to a single register	Writing to a single register
Writing multiple bytes using register-data pairs	Writing to sequential registers
Reading from a single register	Reading from a single register
Reading from sequential registers	Reading from sequential registers

Writing to a Single Register

Figure 34 shows the protocol for the I2C master device to write one byte of data to the IC. This protocol is the same as the SMBus specification's "write byte" protocol.

The "write byte" protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges or not acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Writing to Sequential Registers

Figure 35 shows the protocol for writing to sequential registers. This protocol is similar to the "write byte" protocol (Figure 34) except the master continues to write after it receives the first byte of data. When the master is done writing it issues a stop or repeated start. This protocol is recommended when writing the RTC timekeeping registers (RTC_SEC, RTC_MIN, RTC_HOURS, RTC_WEEKDAY, RTC_DATE, RTC_MONTH, RTC_YEAR1, RTC_YEAR2).

The "writing to sequential registers" protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8) Steps 6 to 7 are repeated as many times as the master requires.
9) During the last acknowledge related clock pulse, the master can issue an acknowledge or a not-acknowledge.
10) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

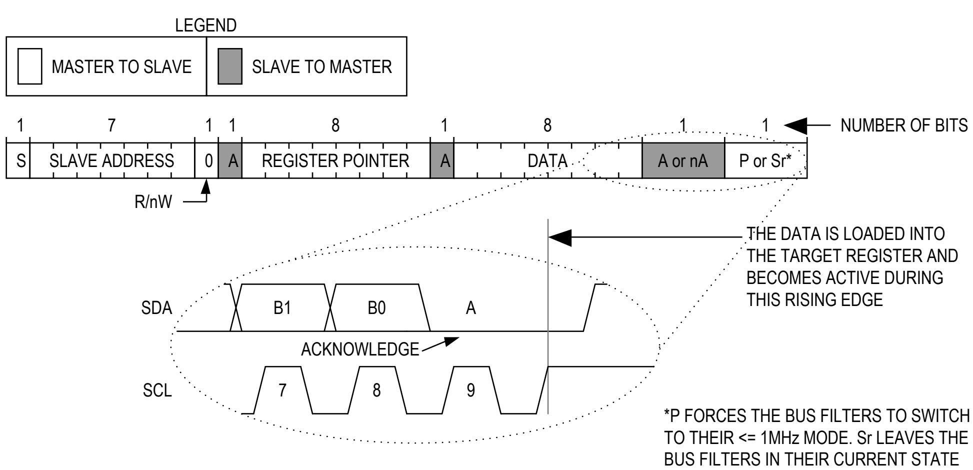


Figure 34. Writing to a Single Register with the "Write Byte" Protocol

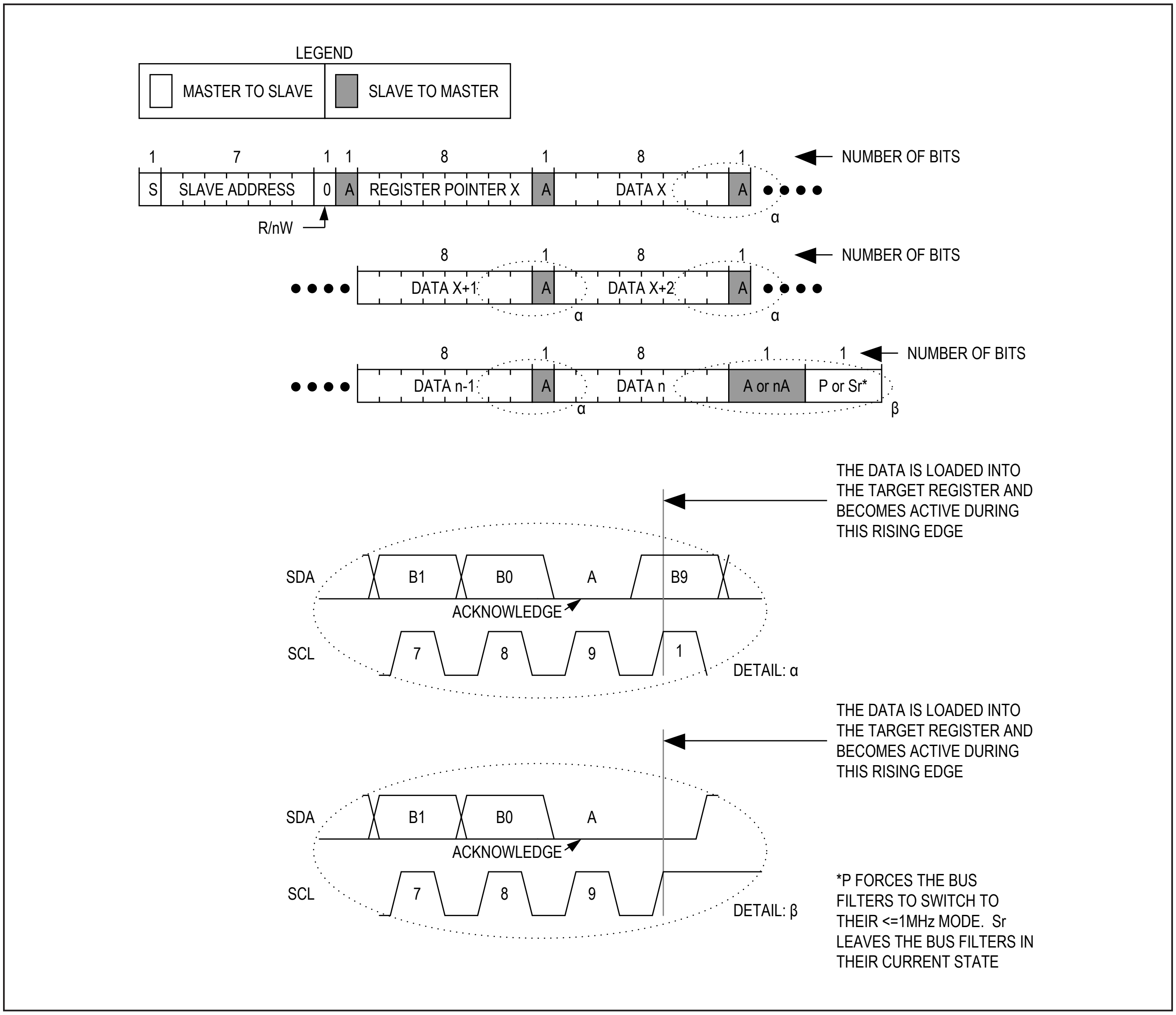


Figure 35. Writing to Sequential Register "x" to "n"

Writing Multiple Bytes Using Register-Data Pairs

Figure 36 shows the protocol for the I2C master device to write multiple bytes to the IC using register-data pairs. This protocol allows the I2C master device to address the slave only once and then send data to multiple registers in a random order. Registers can be written continuously until the master issues a stop condition.

The "Writing Multiple Bytes using Register-Data Pairs" protocol is not supported by the RTC functional block.

The "multiple byte register-data pair" protocol is as follows:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit.
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
8) Steps 4 to 7 are repeated as many times as the master requires.
9) The master sends a stop condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

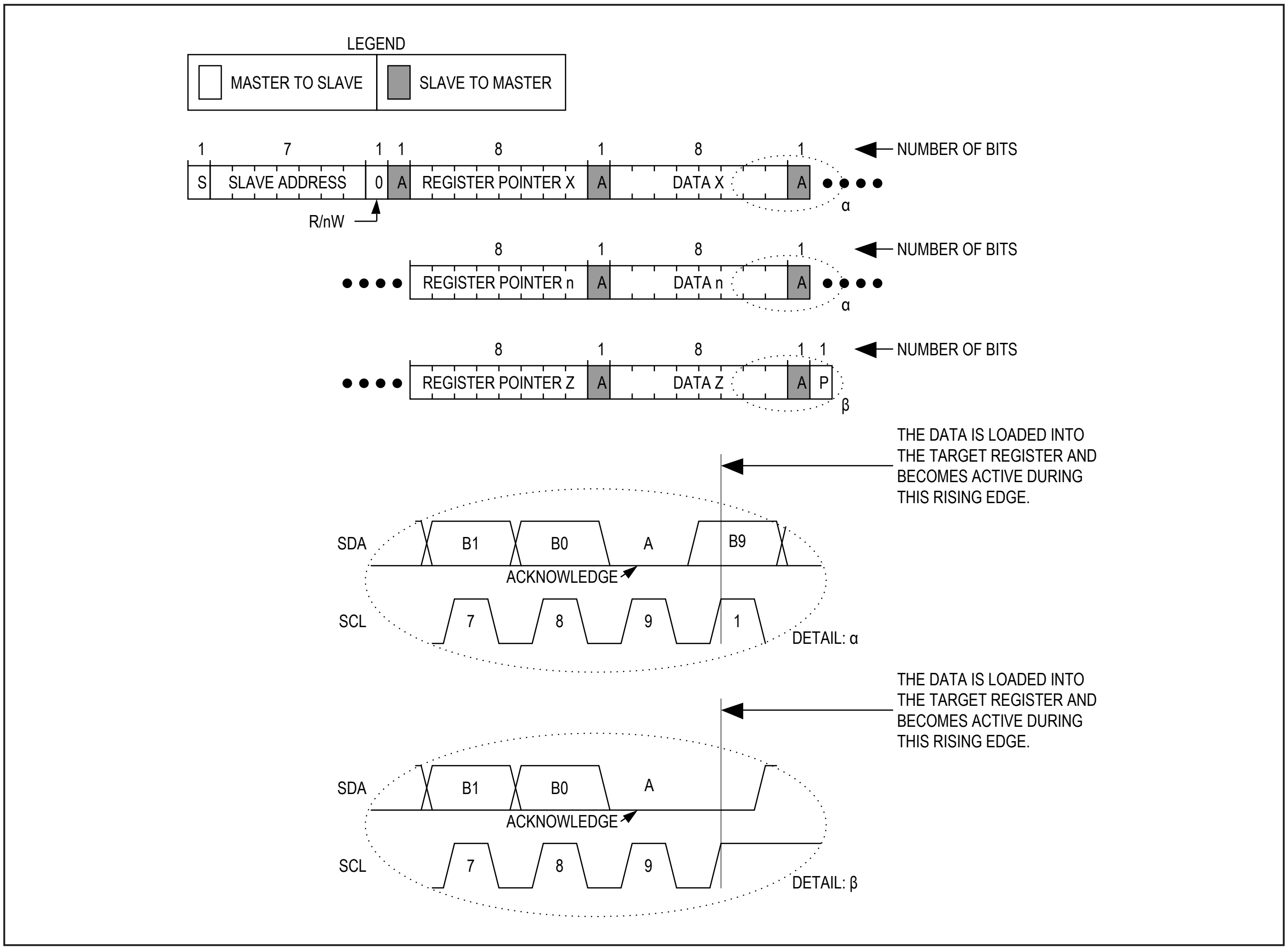


Figure 36. Writing to Multiple Registers with the "Multiple Byte Register-Data Pair" Protocol

Reading from a Single Register

Figure 37 shows the protocol for the I²C master device to read one byte of data to the MAX77863. This protocol is the same as the SMBus specification's "Read Byte" protocol.

The "read byte" protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated start command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1).
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues a not-acknowledge (nA).
11) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the IC receives a stop it does not modify its register pointer.

Reading from Sequential Registers

Figure 35 shows the protocol for reading from sequential registers. This protocol is similar to the "read byte" protocol except the master issues an acknowledge to signal the slave that it wants more data—when the master has all the data it requires it issues a not-acknowledge (nA) and a stop (P) to end the transmission. This continuous read protocol is recommended when reading from the RTC timekeeping registers (RTC_SEC, RTC_MIN, RTC_HOURS, RTC_WEEKDAY, RTC_DATE, RTC_MONTH, RTC_YEAR1, RTC_YEAR2). When reading the RTC timekeeping registers, secondary buffers are used to prevent errors when the internal registers update. The secondary buffers are loaded with the timekeeping register data during an address read byte to the RTC (0xD1) and when the register pointer rolls over to zero. The time information is read from these secondary registers, while the clock continues to run. This eliminates the need to reread the registers in case the main registers update during a read.

The "Continuous Read from Sequential Registers" protocol is as follows:

1) The master sends a start command (S).
2) The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3) The addressed slave asserts an acknowledge (A) by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a repeated start command (Sr).
7) The master sends the 7-bit slave address followed by a read bit (R/nW = 1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
8) The addressed slave asserts an acknowledge by pulling SDA low.
9) The addressed slave places 8-bits of data on the bus from the location specified by the register pointer.
10) The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.

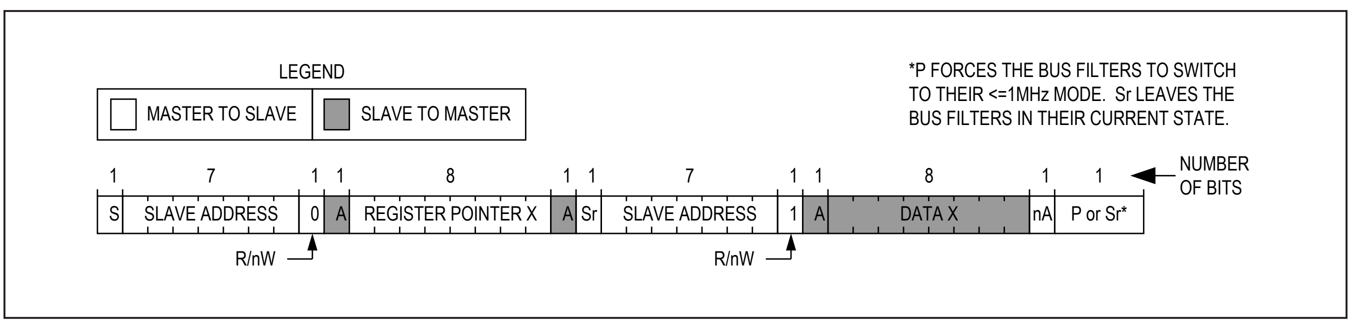


Figure 37. Reading from a Single Register with the "Read Byte" Protocol

11) Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not acknowledge (nA) to signal that it wishes to stop receiving data.
12) The master sends a stop condition (P) or a repeated start condition (Sr). Issuing a stop (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the IC receives a stop it does not modify its register pointer.

Engaging HS-Mode for Operation up to 3.4MHz

Figure 39 shows the protocol for engaging HS-mode operation. HS-mode operation allows for a bus operating speed up to 3.4MHz.

The “Engaging HS-Mode” protocol is as follows:

1) Begin the protocol while operating at a bus speed of 1MHz or lower.
2) The master sends a start command (S).
3) The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don’t care bits.
4) The addressed slave issues a not acknowledge (nA).
5) The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.
6) The master can continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high-speed mode, use repeated start (Sr) commands instead of stop (P) comments. Issuing a stop (P) sets the bus for 1MHz or slower operation.

Factory OTP

To optimize system flexibility, the IC offers many one-time programmable (OTP) options. These OTP options can only be programmed by Maxim during the end-of-line production test. Many OTP options set the reset value of registers; in this case, the default value is listed by an “x” in the register table. Additional OTP options that are not part of the basic register set are summarized in Table 15. If non-standard OTP settings are desired, contact Maxim; minimum order quantities may apply.

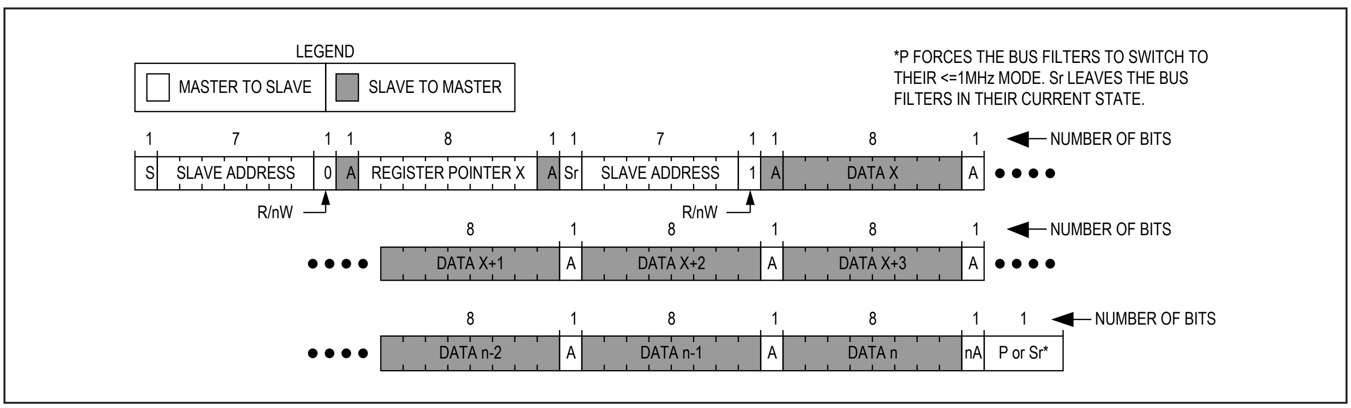


Figure 38. Reading Continuously from Sequential Registers “x” to “n”

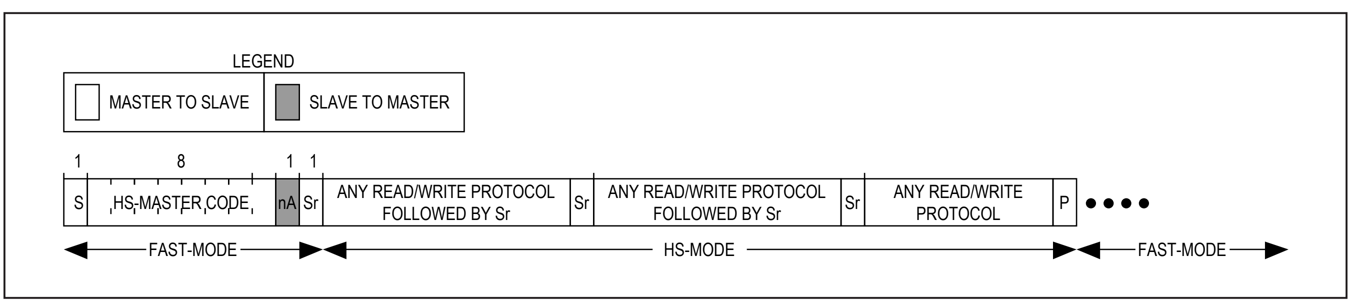


Figure 39. Engaging HS-Mode

Table 15. OTP Bit Descriptions

FUNCTIONAL BLOCK	BIT NAME	DESCRIPTION
32kHz Buffered Output	OTP_32K	32K_OUT0 Output Driver Stage Configuration 0 = The 32K_OUT0 output driver is a push-pull stage between ground and GPIO_INB. 1 = The 32K_OUT0 output driver is an open-drain stage.
Step-Down Regulators	OTP_SD_SS	Step-Down Regulator Soft-Start Rate 0 = 12.5mV/μs 1 = 25mV/μs
On/Off Controller	OTP_EN0AL	Enable 0 Active Low (Figure 20) 0 = EN0 is active-high 1 = EN0 is active-low
On/Off Controller	OTP_EN1AL	Enable 1 Active-Low (Figure 20) 0 = EN1 is active-high 1 = EN1 is active-low
On/Off Controller	OTP_ACOKAL	AC Okay Active-Low (Figure 23) 0 = ACOK is active-high 1 = ACOK is active-low
On/Off Controller	OTP_LIDAL	LID Active-Low (Figure 24) 0 = LID is active-high 1 = LID is active-low
On/Off Controller	OTP_SHDNAL	SHDN Active-Low (Figure 25) 0 = SHDN is active-high 1 = SHDN is active-low
System Watchdog Timer	OTP_WDTEN	If OTP_WDTEN = 0, then WDTEN can be changed at any time. If OTP_WDTEN = 1, then once WDTEN is set the watchdog timer cannot be disabled by clearing WDTEN. Once enabled, the system watchdog timer runs until a global shutdown occurs or the power off (PWR_OFF) functions is initiated.
System Watchdog Timer	OTP_WDTT	If OTP_WDTT = 0, then TWD[1:0] can be changed at any time. If OTP_WDTT = 1, then TWD[1:0] can only be changed when WDTEN = 0.
nRST_IO	OTP_TRSTO[1:0]	Reset Output Deassert Delay Time 0b00 = 1.28ms 0b01 = 10.24ms 0b10 = 40.96ms 0b11 = 81.92ms
I2C	OTP_I2CADDR[1:0]	I2C Address Selection Bits. See Table 13.
Global Resources	OTP_MR	Manual Reset Global Shutdown Control. See the *Global Resources* section for more information on global shutdown. 0 = The device shuts down due to a manual-reset event and stays off until a wakeup event is generated. 1 = The device shuts down due to a manual-reset event and automatically generates its own wakeup.

Register Descriptions

REGISTER NAME	CID0
I²C Slave Address	0x3C
Register Address	0x58
Access Type	Read
Reset Condition	Fixed

BIT	NAME	DESCRIPTION
B[7:0]	SR[7:0]	Serial number least-significant byte SR[23:16] + SR[15:8] + SR[7:0] form a 24-bit serial number

Global Configuration Register 1

REGISTER NAME	CNFGGLBL1
I²C Slave Address	0x3C
Register Address	0x00
Reset Value	0b xx01 xx1x (“x” is an OTP bit)
Access Type	Read/write
Reset Condition	$V_{RTC} < V_{VRTC\_UVLO}$

BIT	NAME	DESCRIPTION		
B7	RSVD	Reserved - Write to 0b1		
B6	MBLPD	Main-Battery Low-Power Down 0 = MBATTLOW does not cause a global shutdown. 1 = MBATTLOW rising forces a global shutdown.		
B[5:4]	LBHYST	Low-Battery Comparator Hysteresis	0x00 = 100mV 0x01 = 200mV	0x02 = 300mV 0x03 = 400mV
B[3:1]	LBDAC[2:0]	Low-Battery DAC Falling Threshold (V_{MONL})	0b000 = 2.7V 0b001 = 2.8V 0b010 = 2.9V 0b011 = 3.0V	0b100 = 3.1V 0b101 = 3.2V 0b110 = 3.3V 0b111 = 3.4V
B0	LBRSTEN	Low-Battery Monitor to nRST_IO Enable (Figure 1) 0 = The low-battery monitor only generates the MBATTLOW status bit and the MBATTLOW_R interrupt bit. 1 = In addition to the bits mentioned above, the low-battery monitor also pulls nRST_IO low when V_{MON} is less than V_{MONL}.		

CNFGGLBL2: Global Configuration Register 2

REGISTER NAME	CNFGGLBL2
I^2C Slave Address	0x3C
Register Address	0x01
Reset Value	0b 0000 0x11 ("x" is an OTP bit)
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION
B[7:6]	I2CTWD[1:0]	I^2C Watchdog Timer Period 0b00 = I^2C watchdog timer is disabled. 0b01 = 1.33ms 0b10 = 35.7ms 0b11 = 41.7ms
B5	GLBL_LPM	Global Low-Power Mode 0 = The global low-power mode signal is logic low. Devices that have been programmed to follow the global low-power mode signal operates in their normal-power modes. 1 = The global low-power mode signal is logic high. Devices that have been programmed to follow the global low-power mode signal operates in their low-power modes. Note that this bit is logically ORed with the alternative mode operation of GPIO0.
B4		Reserved. Write to 1. Read is don't care.
B3	WDTSLPC	System Watchdog Timer Automatic Clear in the SLEEP Mode 0 = The system watchdog timer does not automatically clear in the sleep state. 1 = The system watchdog timer automatically clears in the sleep state.
B2	WDTEN	System Watchdog Timer Enable 0 = System watchdog timer disabled. 1 = System watchdog timer enabled. If OTP_WDTEN = 0, then WDTEN can be changed at any time. If OTP_WDTEN = 1, then once WDTEN is set the watchdog timer cannot be disabled by clearing WDTEN. Once enabled, the system watchdog timer runs until a global shutdown occurs.
B[1:0]	TWD[1:0]	System Watchdog Timer Period 0b00 = 2s 0b01 = 16s 0b10 = 64s 0b11 = 128s If OTP_WDTT = 0, then TWD can be changed at any time. If the value of TWD needs to be changed, clear the system watchdog timer first (WDTC[1:0] = 0b01), then change the value of TWD. If OTP_WDTT = 1, then TWD can only be changed when WDTEN = 0.

CNFGGLBL3: Global Configuration Register 3

REGISTER NAME	GLBLCNFG3
I²C Slave Address	0x3C
Register Address	0x02
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7		Reserved	0
B6		Reserved	0
B5		Reserved	0
B4		Reserved	0
B3		Reserved	0
B2		Reserved	0
B[1:0]	WDTC[1:0]	System Watchdog Timer Clear. Writing 0b01 to these bits clears the watchdog timer. These bits automatically reset to 0b00 after they are written to 0b01. 0b00 = The system watchdog timer is not cleared. 0b01 = The system watchdog timer is cleared. 0b10 = The system watchdog timer is not cleared. 0b11 = The system watchdog timer is not cleared.	0b00

IRQTOP: Top Level Interrupt Register

REGISTER NAME	IRQTOP
I^2C Slave Address	0x3C
Register Address	0x05
Reset Value	0x00
Access Type	Read
Special Features	IRQTOP is cleared when read.
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	IRQ_GLBL	Top-Level Global Interrupt 0 = No unmasked interrupts pending in the INTLBT register 1 = There are unmasked interrupts pending in the INTLBT register	0
B6	IRQ_SD	Top-Level Step-Down Interrupt 0 = No unmasked interrupts pending in the IRQSD register 1 = There are unmasked interrupts pending in the IRQSD register	0
B5	IRQ_LDO	Top-Level LDO Interrupt 0 = No unmasked interrupts pending in the IRQ_LVL2_L0-7 or IRQ_LVL2_L8 registers. 1 = There are unmasked interrupts pending in the IRQ_LVL2_L0-7 or IRQ_LVL2_L8 registers.	0
B4	IRQ_GPIO	Top-Level GPIO Interrupt 0 = No unmasked interrupts pending in the IRQ_LVL2_GPI register. 1 = There are unmasked interrupts pending in the IRQ_LVL2_GPI register.	0
B3	IRQ_RTC	Top-Level RTC Interrupt 0 = No unmasked interrupts pending in the RTCINT register. 1 = There are unmasked interrupts pending in the RTCINT register.	0
B2	IRQ_32K	Top-Level 32kHz Oscillator Interrupt 0 = The 32kHz crystal oscillator has not failed since the last time this bit was read. 1 = The 32kHz crystal oscillator has failed since the last time this bit was read. See the 32K_OK bit for the oscillator status.	0
B1	IRQ_ONOFF	Top-Level On/Off Controller Interrupt 0 = No unmasked interrupts pending in the ONOFFIRQ register. 1 = There are unmasked interrupts pending in the ONOFFIRQ register.	0
B0		Reserved	0

IRQTOPM: Top Level Interrupt Mask Register

IRQTOPM masks interrupts generated by the top level IRQ register IRQTOP. See Figure 2 for a logic diagram showing the IRQTOP and IRQTOPM bits.

REGISTER NAME	IRQTOPM
I^2C Slave Address	0x3C
Register Address	0x0D
Reset Value	0x75
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	IRQ_GLBLM	Top-Level Global Interrupt Mask. IRQ_GLBLM blocks the interrupts from the global resources (INTLBT register) from affecting the nIRQ pin as shown in Figure 2. Be careful not to confuse IRQ_GLBLM with GLBLM. GLBLM blocks all interrupts from affecting the nIRQ pin as shown in Figure 2. 0 = Unmasked 1 = Masked	0
B6	IRQ_SDM	Top-Level Step-Down Interrupt Mask 0 = Unmasked 1 = Masked	1
B5	IRQ_LDOM	Top-Level LDO Interrupt Mask 0 = Unmasked 1 = Masked	1
B4	IRQ_GPIOM	Top-Level GPIO Interrupt Mask 0 = Unmasked 1 = Masked	1
B3	IRQ_RTCM	Top-Level RTC Interrupt Mask 0 = Unmasked 1 = Masked	0
B2	IRQ_32KM	Top-Level 32kHz Oscillator Interrupt Mask 0 = Unmasked 1 = Masked	1
B1	IRQ_ONOFFM	Top-Level On/Off Controller Interrupt Mask 0 = Unmasked 1 = Masked	0
B0		Reserved	1

INTENLBT

INTENLBT enables/disables interrupts generated by the low-battery monitor and the 120°C and 140°C thermal monitor comparators.

REGISTER NAME	INTENLBT
I^2C Slave Address	0x3C
Register Address	0x0E
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B[7:4]		Reserved	0b0000
B3	LBM	Low-Battery Interrupt Mask 0 = Unmasked 1 = Masked	0
B2	$T_{JALRM1M}$	120°C Thermal Alarm 1 Interrupt Mask 0 = Unmasked 1 = Masked	0
B1	$T_{JALRM2M}$	140°C Thermal Alarm 2 Interrupt Mask 0 = Unmasked 1 = Masked	0
B0	GLBLM	Global Interrupt Mask. IRQ_GLBLM blocks the interrupts from the global resources (INTLBT register) from affecting the nIRQ pin as shown in Figure 2. Be careful not to confuse IRQ_GLBLM with GLBLM. GLBLM blocks all interrupts from affecting the nIRQ pin as shown in Figure 2. 0 = Unmasked 1 = Masked	0

STATLBT: Low-Battery and Thermal Monitor Status

STATLBT shows the status of the low-battery monitor and thermal monitors.

REGISTER NAME	STATLBT
I^2C Slave Address	0x3C
Register Address	0x13
Reset Value	0x10
Access Type	Read
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B[7:4]		Reserved. These bits can be written to any value. They always read 0b0001.	0b0001
B3	MBATTLOW	Main-Battery Low Voltage. See Figure 1 for a simplified drawing. 0 = $V_{MON} > V_{MONL}$ 1 = $V_{MON} < V_{MONL}$	0
B2	T_{JALRM1}	120°C Thermal Alarm Status Bit 0 = $T_J < T_{J120}$ 1 = $T_J > T_{J120}$	0
B1	T_{JALRM2}	140°C Thermal Alarm Status Bit 0 = $T_J < T_{J140}$ 1 = $T_J > T_{J140}$	0
B0	IRQ	Software Version Of The Unmasked nIRQ MOSFET Gate Drive (Figure 1) 0 = Unmasked gate drive is logic-low. 1 = Unmasked gate drive is logic-high.	0

INTLBT: Low-Battery and Thermal Monitors Interrupt Register

INTLBT shows the interrupts for the status of the low-battery monitor and thermal monitors.

REGISTER NAME	INTLBT
I^2C Slave Address	0x3C
Register Address	0x06
Reset Value	0x00
Access Type	Read
Special Features	Clear on read
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT	TRIGGER TYPE
B[7:4]		Reserved	0b0000	N/A
B3	MBATTLOW_R	Low-Main Battery Interrupt 0 = V_{MON} has not fallen below V_{MONL} since the last time this bit was read. 1 = V_{MON} has fallen below V_{MONL} since the last time this bit was read.	0	Rising edge
B2	T_{JALRM1}_R	Interrupt 120C Thermal Flag Bit 0 = T_J has not risen above T_{JALRM1} since the list time this bit was read. 1 = T_J has risen above T_{JALRM1} since the list time this bit was read.	0	Rising edge
B1	T_{JALRM2}_R	Interrupt 140C Thermal Flag Bit 0 = T_J has not risen above $T_{JALRM21}$ since the list time this bit was read. 1 = T_J has risen above T_{JALRM2} since the list time this bit was read.	0	Rising edge
B0		Reserved	0	N/A

Step-Down Regulator Output Voltage Setting Registers

REGISTER NAME	VSDx
I2C Slave Address	0x3C
Register Address	0x18: SD2 0x19: SD3
Reset Value	SD2 0b 0xxx xx00 (“x” is an OTP bit) SD3: 0b xxxx xx00 (“x” is an OTP bit)
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION
B[7:0]	VSDx[7:0]	Target Voltage for SD2, SD3 See the *Step-Down Regulator 8-Bit Output Target Output Voltages (SD2, SD3)* table.

Step-Down Regulator Output Voltage Setting Registers

REGISTER NAME	VSD0
I2C Slave Address	0x3C.
Register Address	0x16
Reset Value	0b 0xxx xx00 (“x” is an OTP bit)
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION
B[7:0]	V[7:0]	Target Voltage for SD0 See the *Step-Down Regulator 8-Bit Output Target Output Voltages (SD0)* table.

Step-Down Regulator Output Voltage Setting Registers

REGISTER NAME	VSD1
I2C Slave Address	0x3C
Register Address	0x17
Reset Value	0b 0xxx xx00 (“x” is an OTP bit)
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION
B[7:0]	V[7:0]	Target Voltage for SD1 See the *Step-Down Regulator 8-bit Output Target Output Voltages (SD1)* table.

Step-Down Regulator Dynamic Voltage Scaling Output Setting Registers

REGISTER NAME	VDVSSD0
I^2C Slave Address	0x3C
Register Address	0x1B
Reset Value	0x20
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
B[7:0]	VDVSSD0[7:0]	Dynamic Voltage Management Target Voltage for SD0. See the *Step-Down Regulator 8-Bit Output Target Output Voltages (SD0)* table. To control DVS for SD0 through GPIO5, set AME5 = 1. DIR5 sets whether GPIO5 is active-high or active-low. With the GPIO5 input active, the step-down regulator's target voltage is set by VDVSSD0. With the GPIO5 input inactive, the step-down regulator's target voltage is set by VSD0.	0x20

Step-Down Regulator Dynamic Voltage Scaling Output Setting Registers

REGISTER NAME	VDVSSD1
I^2C Slave Address	0x3C
Register Address	0x1C
Reset Value	0x10
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
B[7:0]	VDVSSD1[7:0]	Dynamic Voltage Management Target Voltage for SD1. See the *Step-Down Regulator 8-bit Output Target Output Voltages (SD1)* table. To control DVS for SD1 through GPIO6, set AME6 = 1. DIR6 sets whether GPIO6 is active-high or active-low. With the GPIO6 input active, the step-down regulator's target voltage is set by VDVSSD1. With the GPIO6 input inactive, the step-down regulator's target voltage is set by VSD0.	0x10

Step-Down Regulator 8-Bit Output Target Output Voltages (SD2, SD3)

0x00 = reserved	0x20 = 1.0000V	0x40 = 1.4000V	0x60 = 1.8000V	0x80 = 2.2000V	0xA0 = 2.6000V	0xC0 = 3.0000V	0xE0 = 3.4000V
0x01 = reserved	0x21 = 1.0125V	0x41 = 1.4125V	0x61 = 1.8125V	0x81 = 2.2125V	0xA1 = 2.6125V	0xC1 = 3.0125V	0xE1 = 3.4125V
0x02 = 0.6250V	0x22 = 1.0250V	0x42 = 1.4250V	0x62 = 1.8250V	0x82 = 2.2250V	0xA2 = 2.6250V	0xC2 = 3.0250V	0xE2 = 3.4250V
0x03 = 0.6375V	0x23 = 1.0375V	0x43 = 1.4375V	0x63 = 1.8375V	0x83 = 2.2375V	0xA3 = 2.6375V	0xC3 = 3.0375V	0xE3 = 3.4375V
0x04 = 0.6500V	0x24 = 1.0500V	0x44 = 1.4500V	0x64 = 1.8500V	0x84 = 2.2500V	0xA4 = 2.6500V	0xC4 = 3.0500V	0xE4 = 3.4500V
0x05 = 0.6625V	0x25 = 1.0625V	0x45 = 1.4625V	0x65 = 1.8625V	0x85 = 2.2625V	0xA5 = 2.6625V	0xC5 = 3.0625V	0xE5 = 3.4625V
0x06 = 0.6750V	0x26 = 1.0750V	0x46 = 1.4750V	0x66 = 1.8750V	0x86 = 2.2750V	0xA6 = 2.6750V	0xC6 = 3.0750V	0xE6 = 3.4750V
0x07 = 0.6875V	0x27 = 1.0875V	0x47 = 1.4875V	0x67 = 1.8875V	0x87 = 2.2875V	0xA7 = 2.6875V	0xC7 = 3.0875V	0xE7 = 3.4875V
0x08 = 0.7000V	0x28 = 1.1000V	0x48 = 1.5000V	0x68 = 1.9000V	0x88 = 2.3000V	0xA8 = 2.7000V	0xC8 = 3.1000V	0xE8 = 3.5000V
0x09 = 0.7125V	0x29 = 1.1125V	0x49 = 1.5125V	0x69 = 1.9125V	0x89 = 2.3125V	0xA9 = 2.7125V	0xC9 = 3.1125V	0xE9 = 3.5125V
0x0A = 0.7250V	0x2A = 1.1250V	0x4A = 1.5250V	0x6A = 1.9250V	0x8A = 2.3250V	0xAA = 2.7250V	0xCA = 3.1250V	0xEA = 3.5250V
0x0B = 0.7375V	0x2B = 1.1375V	0x4B = 1.5375V	0x6B = 1.9375V	0x8B = 2.3375V	0xAB = 2.7375V	0xCB = 3.1375V	0xEB = 3.5375V
0x0C = 0.7500V	0x2C = 1.1500V	0x4C = 1.5500V	0x6C = 1.9500V	0x8C = 2.3500V	0xAC = 2.7500V	0xCC = 3.1500V	0xEC = 3.5500V
0x0D = 0.7625V	0x2D = 1.1625V	0x4D = 1.5625V	0x6D = 1.9625V	0x8D = 2.3625V	0xAD = 2.7625V	0xCD = 3.1625V	0xED = 3.5625V
0x0E = 0.7750V	0x2E = 1.1750V	0x4E = 1.5750V	0x6E = 1.9750V	0x8E = 2.3750V	0xAE = 2.7750V	0xCE = 3.1750V	0xEE = 3.5750V
0x0F = 0.7875V	0x2F = 1.1875V	0x4F = 1.5875V	0x6F = 1.9875V	0x8F = 2.3875V	0xAF = 2.7875V	0xCF = 3.1875V	0xEF = 3.5875V

Step-Down Regulator 8-Bit Output Target Output Voltages (SD2, SD3) (continued)

0x10 = 0.8000V	0x30 = 1.2000V	0x50 = 1.6000V	0x70 = 2.0000V	0x90 = 2.4000V	0xB0 = 2.8000V	0xD0 = 3.2000V	0xF0 = 3.6000V
0x11 = 0.8125V	0x31 = 1.2125V	0x51 = 1.6125V	0x71 = 2.0125V	0x91 = 2.4125V	0xB1 = 2.8125V	0xD1 = 3.2125V	0xF1 = 3.6125V
0x12 = 0.8250V	0x32 = 1.2250V	0x52 = 1.6250V	0x72 = 2.0250V	0x92 = 2.4250V	0xB2 = 2.8250V	0xD2 = 3.2250V	0xF2 = 3.6250V
0x13 = 0.8375V	0x33 = 1.2375V	0x53 = 1.6375V	0x73 = 2.0375V	0x93 = 2.4375V	0xB3 = 2.8375V	0xD3 = 3.2375V	0xF3 = 3.6375V
0x14 = 0.8500V	0x34 = 1.2500V	0x54 = 1.6500V	0x74 = 2.0500V	0x94 = 2.4500V	0xB4 = 2.8500V	0xD4 = 3.2500V	0xF4 = 3.6500V
0x15 = 0.8625V	0x35 = 1.2625V	0x55 = 1.6625V	0x75 = 2.0625V	0x95 = 2.4625V	0xB5 = 2.8625V	0xD5 = 3.2625V	0xF5 = 3.6625V
0x16 = 0.8750V	0x36 = 1.2750V	0x56 = 1.6750V	0x76 = 2.0750V	0x96 = 2.4750V	0xB6 = 2.8750V	0xD6 = 3.2750V	0xF6 = 3.6750V
0x17 = 0.8875V	0x37 = 1.2875V	0x57 = 1.6875V	0x77 = 2.0875V	0x97 = 2.4875V	0xB7 = 2.8875V	0xD7 = 3.2875V	0xF7 = 3.6875V
0x18 = 0.9000V	0x38 = 1.3000V	0x58 = 1.7000V	0x78 = 2.1000V	0x98 = 2.5000V	0xB8 = 2.9000V	0xD8 = 3.3000V	0xF8 = 3.7000V
0x19 = 0.9125V	0x39 = 1.3125V	0x59 = 1.7125V	0x79 = 2.1125V	0x99 = 2.5125V	0xB9 = 2.9125V	0xD9 = 3.3125V	0xF9 = 3.7125V
0x1A = 0.9250V	0x3A = 1.3250V	0x5A = 1.7250V	0x7A = 2.1250V	0x9A = 2.5250V	0xBA = 2.9250V	0xDA = 3.3250V	0xFA = 3.7250V
0x1B = 0.9375V	0x3B = 1.3375V	0x5B = 1.7375V	0x7B = 2.1375V	0x9B = 2.5375V	0xBB = 2.9375V	0xDB = 3.3375V	0xFB = 3.7375V
0x1C = 0.9500V	0x3C = 1.3500V	0x5C = 1.7500V	0x7C = 2.1500V	0x9C = 2.5500V	0xBC = 2.9500V	0xDC = 3.3500V	0xFC = 3.7500V
0x1D = 0.9625V	0x3D = 1.3625V	0x5D = 1.7625V	0x7D = 2.1625V	0x9D = 2.5625V	0xBD = 2.9625V	0xDD = 3.3625V	0xFD = 3.7625V
0x1E = 0.9750V	0x3E = 1.3750V	0x5E = 1.7750V	0x7E = 2.1750V	0x9E = 2.5750V	0xBE = 2.9750V	0xDE = 3.3750V	0xFE = 3.7750V
0x1F = 0.9875V	0x3F = 1.3875V	0x5F = 1.7875V	0x7F = 2.1875V	0x9F = 2.5875V	0xBF = 2.9875V	0xDF = 3.3875V	0xFF = 3.7875V

Step-Down Regulator 8-Bit Output Target Output Voltages (SD0)

0x00 = Reserved	0x10 = 0.8000V	0x20 = 1.0000V	0x30 = 1.2000V	0x40 = 1.4000V
0x01 = Reserved	0x11 = 0.8125V	0x21 = 1.0125V	0x31 = 1.2125V	0x41 to 0xFF are reserved and writes to this space are ignored.
0x02 = 0.6250V	0x12 = 0.8250V	0x22 = 1.0250V	0x32 = 1.2250V	
0x03 = 0.6375V	0x13 = 0.8375V	0x23 = 1.0375V	0x33 = 1.2375V	
0x04 = 0.6500V	0x14 = 0.8500V	0x24 = 1.0500V	0x34 = 1.2500V	
0x05 = 0.6625V	0x15 = 0.8625V	0x25 = 1.0625V	0x35 = 1.2625V	
0x06 = 0.6750V	0x16 = 0.8750V	0x26 = 1.0750V	0x36 = 1.2750V	
0x07 = 0.6875V	0x17 = 0.8875V	0x27 = 1.0875V	0x37 = 1.2875V	
0x08 = 0.7000V	0x18 = 0.9000V	0x28 = 1.1000V	0x38 = 1.3000V	
0x09 = 0.7125V	0x19 = 0.9125V	0x29 = 1.1125V	0x39 = 1.3125V	
0x0A = 0.7250V	0x1A = 0.9250V	0x2A = 1.1250V	0x3A = 1.3250V	
0x0B = 0.7375V	0x1B = 0.9375V	0x2B = 1.1375V	0x3B = 1.3375V	
0x0C = 0.7500V	0x1C = 0.9500V	0x2C = 1.1500V	0x3C = 1.3500V	
0x0D = 0.7625V	0x1D = 0.9625V	0x2D = 1.1625V	0x3D = 1.3625V	
0x0E = 0.7750V	0x1E = 0.9750V	0x2E = 1.1750V	0x3E = 1.3750V	
0x0F = 0.7875V	0x1F = 0.9875V	0x2F = 1.1875V	0x3F = 1.3875V	

Step-Down Regulator 8-bit Output Target Output Voltages (SD1)

0x00 = Reserved	0x10 = 0.8000V	0x20 = 1.0000V	0x30 = 1.2000V	0x40 = 1.4000V
0x01 = Reserved	0x11 = 0.8125V	0x21 = 1.0125V	0x31 = 1.2125V	0x41 = 1.4125V
0x02 = 0.6250V	0x12 = 0.8250V	0x22 = 1.0250V	0x32 = 1.2250V	0x42 = 1.4250V
0x03 = 0.6375V	0x13 = 0.8375V	0x23 = 1.0375V	0x33 = 1.2375V	0x43 = 1.4375V
0x04 = 0.6500V	0x14 = 0.8500V	0x24 = 1.0500V	0x34 = 1.2500V	0x44 = 1.4500V
0x05 = 0.6625V	0x15 = 0.8625V	0x25 = 1.0625V	0x35 = 1.2625V	0x45 = 1.4625V
0x06 = 0.6750V	0x16 = 0.8750V	0x26 = 1.0750V	0x36 = 1.2750V	0x46 = 1.4750V
0x07 = 0.6875V	0x17 = 0.8875V	0x27 = 1.0875V	0x37 = 1.2875V	0x47 = 1.4875V
0x08 = 0.7000V	0x18 = 0.9000V	0x28 = 1.1000V	0x38 = 1.3000V	0x48 = 1.5000V
0x09 = 0.7125V	0x19 = 0.9125V	0x29 = 1.1125V	0x39 = 1.3125V	0x49 = 1.5125V
0x0A = 0.7250V	0x1A = 0.9250V	0x2A = 1.1250V	0x3A = 1.3250V	0x4A = 1.5250V
0x0B = 0.7375V	0x1B = 0.9375V	0x2B = 1.1375V	0x3B = 1.3375V	0x4B = 1.5375V
0x0C = 0.7500V	0x1C = 0.9500V	0x2C = 1.1500V	0x3C = 1.3500V	0x4C = 1.5500V
0x0D = 0.7625V	0x1D = 0.9625V	0x2D = 1.1625V	0x3D = 1.3625V	0x4D to 0xFF are reserved and writes to this space are ignored.
0x0E = 0.7750V	0x1E = 0.9750V	0x2E = 1.1750V	0x3E = 1.3750V	
0x0F = 0.7875V	0x1F = 0.9875V	0x2F = 1.1875V	0x3F = 1.3875V	

Step-Down Regulator Configuration—Register 1

REGISTER NAME	CNFG1SDx		
I^2C Slave Address	0x3C		
Register Address	0x1D: SD0 0x1E: SD1	0x1F: SD2 0x20: SD3	
Reset Value	0b 01xx 00x0 (“x” is an OTP bit)		
Access Type	Read/write		
Reset Condition	Global shutdown		

BIT	BIT NAME	DESCRIPTION
B[7:6]	SR_SDx[1:0]	SDx Slew Rate During DVS 0x0 = 0b00 = 13.75mV/μs ramp rate 0x1 = 0b01 = 27.50mV/μs ramp rate 0x2 = 0b10 = 55.00mV/μs ramp rate 0x3 = 0b11 = 100mV/μs ramp rate (Note 10) The typical use case for SR_SDx is to set them to the desired value during system initialization and then leave them that way during the normal operation of the system. The SR_SDx bits should not be changed while its associated step-down regulator is in the middle of an output voltage slew rate event. See the *Dynamic Voltage Scaling* section for more information.
B[5:4]	PWR_MD_SDx_ [1:0]	SDx Power Mode Configuration When FPSSRC_SDx[1:0] = 0b11 0b00 = Disabled. SDx is off. EN2 can override this setting and enable SD0 when it is high. 0b01 = Group low-power mode. SDx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, SDx operates in low-power mode. 0b10 = Low-power mode. SDx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 5μA. 0b11 = Normal operation mode. SDx is forced into its normal operating mode. When FPSSRC_SDx[1:0]≠0b11 0b00 = SDx is disabled when the flexible power sequencer set by FPSSRC_SDx is disabled. SDx is enabled in normal-power mode when the flexible power sequencer is enabled. EN2 can override this setting and enable SD0 when it is high. 0b01 = SDx is disabled when the flexible power sequencer set by FPSSRC_SDx is disabled. SDx is enabled when the flexible power sequencer is enabled. When SDx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = SDx is disabled when the flexible power sequencer set by FPSSRC_SDx is disabled. SDx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = Same as 0b00. Note that SD0 is also controlled with the EN2 hardware pin. See Table 9 for the ENSD0 and PWR_MD_SD0[1:0] enable logic.

Step-Down Regulator Configuration—Register 1 (continued)

BIT	BIT NAME	DESCRIPTION
B3	nADE_SDx	Active-Low SDx Active Discharge Enable 0 = The active discharge function is enabled. When the step-down regulator is disabled, an internal 100Ω discharge resistor is connected to the output to discharge the energy stored in the output capacitor. When the step-down regulator is enabled, the discharge resistor is disconnected from the output. 1 = The active discharge function is disabled. When the step-down regulator is disabled, the internal 100Ω discharge resistor is not connected to the output, and the discharge rate is dependent on the output capacitance and the load present. When the step-down regulator is enabled, the discharge resistor is disconnected from the output.
B2	FPWM_SDx	SDx Forced PWM Mode Enable 0 = SDx regulator skips pulses under light load conditions, and operates at a fixed frequency with medium to heavy load conditions. The regulator automatically transitions between pulse skipping and fixed frequency as needed. 1 = SDx regulator operates with fixed frequency under all load conditions.
B1		Reserved. This bit must always be cleared to 0.
B0	nFSRADE_SDx	Active-Low SDx Falling Slew Rate Active-Discharge Enable This bit is a don’t care when a given step-down converter is in low-power mode. In low-power mode, the regulator behaves as if active discharge is always disabled. 0 = Active-discharge enabled. SDx operates in forced PWM mode during the time the output voltage decreases. With forced PWM mode enabled, SDx can sink current from the output capacitor to ensure that the output voltage falls at the rate programmed by SR_SDx[1:0]. To ensure a smooth output voltage decrease, the PMW mode remains engaged for 50μs after the output voltage decreases to its target voltage. 1 = Active-discharge disabled. SDx is allowed to operate in skip mode during the time the output voltage decreases (only if FPWM_SDx = 0). In skip mode, SDx cannot sink current from the output capacitor. Since SDx cannot sink current in skip mode the output voltage falling slew rate is a function of the external load on SDx. If the external load on SDx is heavy, then the output voltage falling slew rate is the rate programmed by SR_SDx[1:0]. If the external load on SDx is light, then the output voltage falling slew rate is a function of the output capacitance and the external load. Note that the SDx internal feedback string always imposes a 2μA load on the output.

Step-Down Regulator Configuration—Register 2

REGISTER NAME	CNFG2SD
I^2C Slave Address	0x3C
Register Address	0x22
Reset Value	0x07
Access Type	Read/write
Reset Condition	Global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
B[7:6]		Reserved. Write these bits to 0b00.	0b00
B[5:3]		Reserved. Write these bits to 0b000.	0b000
B2	ROVS_EN_SD0	SD0 Remote Output Voltage Sense Enable 0 = Disabled 1 = Enabled Note that when SD0 is operating in low-power mode, the ROVS function is automatically disabled, however; this bit is not affected. If this bit is set, then ROVS automatically re-enables when SD0 enters its normal operating mode.	1
B1	ROVS_EN_SD1	SD1 Remote Sense Enable 0 = Disabled 1 = Enabled Note that when SD1 is operating in low-power mode, the ROVS function is automatically disabled, however; this bit is not affected. If this bit is set, then ROVS automatically re-enables when SD1 enters its normal operating mode.	1
B0		Reserved	1

Step-Down Regulator Interrupt Request Register

REGISTER NAME	IRQSD
I^2C Slave Address	0x3C
Register Address	0x07
Reset Value	0x00
Access Type	Read
Special Features	Cleared upon read operation
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT	TRIGGER TYPE
B7	PFI_SD0	SD0 Power Fail Interrupt 0 = VSD0 has not fallen below VPOK_SDx since the last time this bit was read. 1 = VSD0 has fallen below VPOK_SDx since the last time this bit was read.	0	Falling edge
B6	PFI_SD1	SD1 Power Fail Interrupt 0 = VSD1 has not fallen below its target voltage since the last time this bit was read. 1 = VSD1 has fallen below its target voltage since the last time this bit was read.	0	Falling edge
B5	PFI_SD2	SD2 Power Fail Interrupt 0 = VSD2 has not fallen below its target voltage since the last time this bit was read. 1 = VSD2 has fallen below its target voltage since the last time this bit was read.	0	Falling edge
B4	PFI_SD3	SD3 Power Fail Interrupt 0 = VSD3 has not fallen below its target voltage since the last time this bit was read. 1 = VSD3 has fallen below its target voltage since the last time this bit was read.	0	Falling edge
B[3:0]		Reserved	0b0000	

Step-Down Regulator Interrupt Request Register Mask

REGISTER NAME	IRQMASKSD
I^2C Slave Address	0x3C
Register Address	0x0F
Reset Value	0xFF
Access Type	Read/write
Special Features	N/A
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	PFIM_SD0	SD0 Power Fail Interrupt Mask 0 = Unmasked 1 = Masked	1
B6	PFIM_SD1	SD1 Power Fail Interrupt Mask 0 = Unmasked 1 = Masked	1
B5	PFIM_SD2	SD2 Power Fail Interrupt Mask 0 = Unmasked 1 = Masked	1
B4	PFIM_SD3	SD3 Power Fail Interrupt Mask 0 = Unmasked 1 = Masked	1
B[3:0]		Reserved. Write 0b1111. Read is don’t care.	0b1111

Step-Down Regulator Status

REGISTER NAME	STATSD
I²C Slave Address	0x3C
Register Address	0x14
Reset Value	0xFF
Access Type	Read
Special Features	N/A
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	nPOK_SD0	SD0 Power Okay Status 0 = V_{SD0} above POK rising threshold–OK 1 = V_{SD0} below POK rising threshold–not OK	1
B6	nPOK_SD1	SD1 Power Okay Status 0 = V_{SD1} above POK rising threshold–OK 1 = V_{SD1} below POK rising threshold–not OK	1
B5	nPOK_SD2	SD2 Power Okay Status 0 = V_{SD2} above POK rising threshold–OK 1 = V_{SD2} below POK rising threshold–not OK	1
B4	nPOK_SD3	SD3 Power Okay Status 0 = V_{SD3} above POK rising threshold–OK 1 = V_{SD3} below POK rising threshold–not OK	1
B[3:0]		Reserved	0b1111

CNFG1_Lx: Linear Regulator Configuration Register (LDO0 to LDO8)

REGISTER NAME	CNFG1_Lx				
I^2C Slave Address	0x3C				
Register Address	0x23: LDO0 0x25: LDO1	0x27: LDO2 0x29: LDO3	0x2B: LDO4 0x2D: LDO5	0x2F: LDO6 0x31: LDO7	0x33: LDO8
Reset Value	0b 01xx 00x0 ("x" is an OTP bit)				
Access Type	Read/write				
Reset Condition	Global shutdown				

BIT	NAME	ACCESS TYPE	DESCRIPTION (DEFAULT VALUE IS SET WITH OTP)
7:6	PWR_MD_Lx[1:0]	R/W	LDOx Power Mode Configuration When FPSSRC_Lx[1:0] = 0b11 0b00: Output disabled. LDOx is off. 0b01: Group low-power mode. LDOx operates in normal mode when the global low-power mode signal is low. When the global low-power mode signal is high, LDOx operates in low-power mode. 0b10: Low-power mode. LDOx is forced into low-power mode. The maximum load current is 5mA and the quiescent supply current is 1.5μA. 0b11: Normal mode. LDOx is forced into its normal operating mode. When FPSSRC_Lx[1:0] ≠ 0b11 0b00 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in normal-power mode when the flexible power sequencer is enabled. 0b01 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled when the flexible power sequencer is enabled. When LDOx is enabled, it operates in normal mode when the global low-power mode signal is low, and it operates in low-power mode when the global low-power mode signal is logic high. 0b10 = LDOx is disabled when the flexible power sequencer set by FPSSRC_Lx is disabled. LDOx is enabled in low-power mode when the flexible power sequencer is enabled. 0b11 = Same as 0b00.

CNFG1_Lx: Linear Regulator Configuration Register (LDO0 to LDO8) (continued)

BIT	NAME	ACCESS TYPE	DESCRIPTION (DEFAULT VALUE IS SET WITH OTP)			
5:0	TV_Lx[5:0] (Target Voltage for FB String 1: LDO0, LDO1)	R/W	Target voltage for LDO0, LDO1			
			0x00 = 0.800V	0x10 = 1.200V	0x20 = 1.600V	0x30 = 2.000V
			0x01 = 0.825V	0x11 = 1.225V	0x21 = 1.625V	0x31 = 2.025V
			0x02 = 0.850V	0x12 = 1.250V	0x22 = 1.650V	0x32 = 2.050V
			0x03 = 0.875V	0x13 = 1.275V	0x23 = 1.675V	0x33 = 2.075V
			0x04 = 0.900V	0x14 = 1.300V	0x24 = 1.700V	0x34 = 2.100V
			0x05 = 0.925V	0x15 = 1.325V	0x25 = 1.725V	0x35 = 2.125V
			0x06 = 0.950V	0x16 = 1.350V	0x26 = 1.750V	0x36 = 2.150V
			0x07 = 0.975V	0x17 = 1.375V	0x27 = 1.775V	0x37 = 2.175V
			0x08 = 1.000V	0x18 = 1.400V	0x28 = 1.800V	0x38 = 2.200V
			0x09 = 1.025V	0x19 = 1.425V	0x29 = 1.825V	0x39 = 2.225V
			0x0A = 1.050V	0x1A = 1.450V	0x2A = 1.850V	0x3A = 2.250V
			0x0B = 1.075V	0x1B = 1.475V	0x2B = 1.875V	0x3B = 2.275V
			0x0C = 1.100V	0x1C = 1.500V	0x2C = 1.900V	0x3C = 2.300V
			0x0D = 1.125V	0x1D = 1.525V	0x2D = 1.925V	0x3D = 2.325V
			0x0E = 1.150V	0x1E = 1.550V	0x2E = 1.950V	0x3E = 2.350V
			0x0F = 1.175V	0x1F = 1.575V	0x2F = 1.975V	0x3F = 2.375V
	TV_Lx[5:0] (Target Voltage for FB String 2: LDO2, LDO3, LDO5, LDO6, LDO7, LDO8)	R/W	Target voltage for LDO2, LDO3, LDO5, LDO6, LDO7, LDO8			
			0x00 = 0.80V	0x10 = 1.60V	0x20 = 2.40V	0x30 = 3.20V
			0x01 = 0.85V	0x11 = 1.65V	0x21 = 2.45V	0x31 = 3.25V
			0x02 = 0.90V	0x12 = 1.70V	0x22 = 2.50V	0x32 = 3.30V
			0x03 = 0.95V	0x13 = 1.75V	0x23 = 2.55V	0x33 = 3.35V
			0x04 = 1.00V	0x14 = 1.80V	0x24 = 2.60V	0x34 = 3.40V
			0x05 = 1.05V	0x15 = 1.85V	0x25 = 2.65V	0x35 = 3.45V
			0x06 = 1.10V	0x16 = 1.90V	0x26 = 2.70V	0x36 = 3.50V
			0x07 = 1.15V	0x17 = 1.95V	0x27 = 2.75V	0x37 = 3.55V
			0x08 = 1.20V	0x18 = 2.00V	0x28 = 2.80V	0x38 = 3.60V
			0x09 = 1.25V	0x19 = 2.05V	0x29 = 2.85V	0x39 = 3.65V
			0x0A = 1.30V	0x1A = 2.10V	0x2A = 2.90V	0x3A = 3.70V
			0x0B = 1.35V	0x1B = 2.15V	0x2B = 2.95V	0x3B = 3.75V
			0x0C = 1.40V	0x1C = 2.20V	0x2C = 3.00V	0x3C = 3.80V
			0x0D = 1.45V	0x1D = 2.25V	0x2D = 3.05V	0x3D = 3.85V
			0x0E = 1.50V	0x1E = 2.30V	0x2E = 3.10V	0x3E = 3.90V
			0x0F = 1.55V	0x1F = 2.35V	0x2F = 3.15V	0x3F = 3.95V

CNFG1_Lx: Linear Regulator Configuration Register (LDO0 to LDO8) (continued)

BIT	NAME	ACCESS TYPE	DESCRIPTION (DEFAULT VALUE IS SET WITH OTP)			
	TV_Lx[5:0] (Target Voltage for FB String 3: LDO4)	R/W	Target voltage for LDO4			
			0x00 = 0.8000V	0x10 = 1.0000V	0x20 = 1.2000V	0x30 = 1.4000V
			0x01 = 0.8125V	0x11 = 1.0125V	0x21 = 1.2125V	0x31 = 1.4125V
			0x02 = 0.8250V	0x12 = 1.0250V	0x22 = 1.2250V	0x32 = 1.4250V
			0x03 = 0.8375V	0x13 = 1.0375V	0x23 = 1.2375V	0x33 = 1.4375V
			0x04 = 0.8500V	0x14 = 1.0500V	0x24 = 1.2500V	0x34 = 1.4500V
			0x05 = 0.8625V	0x15 = 1.0625V	0x25 = 1.2625V	0x35 = 1.4625V
			0x06 = 0.8750V	0x16 = 1.0750V	0x26 = 1.2750V	0x36 = 1.4750V
			0x07 = 0.8875V	0x17 = 1.0875V	0x27 = 1.2875V	0x37 = 1.4875V
			0x08 = 0.9000V	0x18 = 1.1000V	0x28 = 1.3000V	0x38 = 1.5000V
			0x09 = 0.9125V	0x19 = 1.1125V	0x29 = 1.3125V	0x39 = 1.5125V
			0x0A = 0.9250V	0x1A = 1.1250V	0x2A = 1.3250V	0x3A = 1.5250V
			0x0B = 0.9375V	0x1B = 1.1375V	0x2B = 1.3375V	0x3B = 1.5375V
			0x0C = 0.9500V	0x1C = 1.1500V	0x2C = 1.3500V	0x3C = 1.5500V
			0x0D = 0.9625V	0x1D = 1.1625V	0x2D = 1.3625V	0x3D = 1.5625V
			0x0E = 0.9750V	0x1E = 1.1750V	0x2E = 1.3750V	0x3E = 1.5750V
			0x0F = 0.9875V	0x1F = 1.1875V	0x2F = 1.3875V	0x3F = 1.5875V

CNFG2_Lx: Linear Regulator Configuration Register Details

REGISTER NAME	**CNFG2_Lx**				
I^2C Slave Address	0x3C				
Register Address	0x24: LDO0 0x26: LDO1	0x28: LDO2 0x2A: LDO3	0x2C: LDO4 0x2E: LDO5	0x30: LDO6 0x32: LDO7	0x34: LDO8
Reset Value	0b 01xx 00x0 (“x” is an OTP bit)				
Access Type	Read/write				
Reset Condition	Global shutdown				

BIT	NAME	ACCESS TYPE	DESCRIPTION (Default value is set with OTP)
7	OVCLMP_ EN_ Lx	R/W	Overvoltage Clamp Enable for LDOx 0 = Overvoltage clamp disabled 1 = Overvoltage clamp enabled (default)
6	ALPM_EN_ Lx Reserved	R/W	Auto Low-Power Mode Enable Bit 0 = Auto low-power mode is disabled 1 = Auto low-power mode is enabled (default) Reserved. This bit defaults to 1 and should be left at 1.
5	COMP_Lx_ [1:0]	R/W	Adjustable compensation for PDRVx LDOs (LDO2 to LDO6). For LDO0, LDO01, LDO7, and LDO8 these bits must be 0b00. LDO2 to LD06 support operation with a remote output capacitor. The optimum compensation for each LDO is dependent on the series R-L-C impedance from the LDO output (LDO_OUTx) and its ground (GND). The series resistance (R) is from parasitic resistance of the PCB and the ESR of the capacitor. A good rule of thumb for parasitic “R” on a PCB is 0.5mΩ per square for 1oz copper and 1.0mΩ per square for 0.5oz copper. The series inductance (L) is from the parasitic inductance of the PCB and the ESL of the capacitor. A good rule of thumb for parasitic “L” on the PCB is 5nH/cm of electrical length. The series C is the output capacitor itself. Note that the COMP_Lx bits should only be changed when the LDO is disabled. If the compensation bits are changed when the LDO is enabled, the output voltage glitches as the compensation changes. 0b00 = Fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 50mΩ, 5nH, and ≥ C_{OUT_x} (Table 1). This output impedance corresponds to an output capacitor that is placed directly at the output pins of the LDO (i.e., not remote). Load transient performance with this setting is 55mV typical between OUTxx and GND (default). 0b01 = Medium-fast transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 150mΩ, 10nH, and ≥ C_{OUT_x} (Table 1). This output impedance corresponds to an output capacitor that is relatively close to the output pins of the LDO (2cm electrical length). Load transient performance with this setting is 66mV typical between OUTxx and GND. 0b10 = Medium-slow transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 500mΩ, 35nH, and ≥ C_{OUT_x} (Table 1). This output impedance corresponds to an output capacitor that is placed at the point of load which may be a few centimeters from the output pins of the LDO (7cm electrical length). Load transient performance with this setting is 99mV typical between OUTxx and GND. 0b11 = Slow transconductance setting for internal amplifier. Use this setting when the LDOs output capacitor loop has a series R-L-C output impedance of 1000mΩ, 50nH, and ≥ C_{OUT_x} (Table 1). This output impedance corresponds to an output capacitor that is placed very far away from the output pins of the LDO (10cm electrical length). Load transient performance with this setting is 125mV typical between OUTxx and GND.
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CNFG2_Lx: Linear Regulator Configuration Register Details (continued)

BIT	NAME	ACCESS TYPE	DESCRIPTION (default value is set with OTP)
3	POK_Lxx	R	Voltage Okay Status Bit for LDOx 0 = The voltage is less than the POK threshold. 1 = The voltage is above the POK threshold.
2		R/W	Reserved. This bit must always be cleared to 0.
1	ADE_Lx	R/W	Active Discharge Enable for LDOx 0 = The active discharge function is disabled. When the regulator is disabled, the internal active-discharge resistor is not connected to its output and the output voltage decays at a rate that is determined by the output capacitance and the external load. When the regulator is enabled, the internal active-discharge resistor is not connected to its output. 1 = The active discharge function is enabled. When the regulator is disabled, an internal active-discharge resistor is connected to its output which discharges the energy stored in the output capacitance. When this regulator is enabled, the internal active-discharge resistor is disconnected from its output.
0	SS_Lx	R/W	Soft-Start Slew Rate Configuration for LDOx (Applies to both start-up and output voltage setting changes) 0 = Fast startup and dynamic voltage change–100mV/μs 1 = Slow startup and dynamic voltage change–5mV/μs

CNFG3_LDO: Linear Regulator Global Configuration Register

REGISTER NAME	CNFG3_LDO
I^2C Slave Address	0x3C
Register Address	0x35
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	ACCESS TYPE	DESCRIPTION
7:1		R/W	Reserved. Write 0b0000000. Read is a don’t care.
0	L_B_EN	R/W	LDO Bias Enable 0 = Bias is disabled if all LDOs are disabled (default). 1 = Bias is enabled.

IRQ_LVL2_Lx: Interrupt Registers

REGISTER NAME	**IRQ_LVL2_Lx**
I^2C Slave Address	0x3C
Register Address	0x08: IRQ_LVL2_L0-7 0x09: IRQ_LVL2_L8
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	ACCESS TYPE	DESCRIPTION
	IRQ_LVL2_Lx	R	IRQ Interrupt Bit 1: An interrupt has occurred. Cleared when read. 0: No interrupt has occurred since the last time this register was read.
IRQ_LVL2_L8, Register Address = 0x09, Default = 0x00			
7:0	IRQ_LVL2_Lx	R	Bit 7: Reserved Bit 6: Reserved Bit 5: Reserved Bit 4: Reserved Bit 3: Reserved Bit 2: Reserved Bit 1: Reserved Bit 0: IRQ_LVL2_L8
IRQ_LVL2_L0-7, Register Address = 0x08, Default = 0x00			
7:0	IRQ_LVL2_Lx	R	Bit 7: IRQ_LVL2_L7 Bit 6: IRQ_LVL2_L6 Bit 5: IRQ_LVL2_L5 Bit 4: IRQ_LVL2_L4 Bit 3: IRQ_LVL2_L3 Bit 2: IRQ_LVL2_L2 Bit 1: IRQ_LVL2_L1 Bit 0: IRQ_LVL2_L0

IRQ_MSK_Lx: Interrupt Mask Registers

REGISTER NAME	**IRQ_MSK_Lx**
I2C Slave Address	0x3C
Register Address	0x10: IRQ_MSK_L0-7 0x11: IRQ_MSK_L8
Reset Value	0xFF
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	ACCESS TYPE	DESCRIPTION
	MSK_Lx	R/W	Interrupt Mask Bit 1: Interrupt is masked and nIRQ is not driven low due to an LDO event. 0: Interrupt is unmasked.
IRQ_MSK_L8, Register Address = 0x11, Default = 0xFF			
7:0	IRQ_MSK_L8	R/W	Bit 7: Reserved Bit 6: Reserved Bit 5: Reserved Bit 4: Reserved Bit 3: Reserved Bit 2: Reserved Bit 1: Reserved Bit 0: IRQ_MSK_L8
IRQ_MSK_L0-7, Register Address = 0x10, Default = 0xFF			
7:0	IRQ_MSK_L0-7	R/W	Bit 7: IRQ_MSK_L7 Bit 6: IRQ_MSK_L6 Bit 5: IRQ_MSK_L5 Bit 4: IRQ_MSK_L4 Bit 3: IRQ_MSK_L3 Bit 2: IRQ_MSK_L2 Bit 1: IRQ_MSK_L1 Bit 0: IRQ_MSK_L0

CNFG_GPIOx: GPIO Configuration Register

REGISTER NAME	**CNFG1_GPIOx**			
I^{2}C Slave Address	0x3C			
Register Address	0x36 for GPIO0 0x37 for GPIO1	0x38 for GPIO2 0x39 for GPIO3	0x3A for GPIO4 0x3B for GPIO5	0x3C for GPIO6 0x3D for GPIO7
Reset Value	When AMEx = 0 → GPIO0/1/2/3/5/6/7 = 0x02, GPIO4 = 0x03 When AMEx = 1 → GPIO0/5/6 = 0x02, GPIO1/2/3 = 0x00, GPIO4 = 0x01, GPIO7 = 0x00			
Access Type	Read/write			
Reset Condition	Global shutdown			

BIT	NAME	DESCRIPTION
B[7:6]	DBNCx[1:0]	When set for GPO (DIRx = 0): DBNCx are don't care when GPO.
		When set for GPI (DIRx = 1): Debounce configuration. GPIx has the following debounce times for both rising and falling edges. 0b00 = No debounce 0b01 = 8ms 0b10 = 16ms 0b11 = 32ms
B[5:4]	REFE_IRQx[1:0]	When set for GPO (DIRx = 0): REFE_IRQx are don't care when GPO.
		When set for GPI (DIRx = 1): Rising edge and falling edge interrupt configuration. GPIx has the interrupt behavior which is programmed with REFE_IRQx. 0b00 = Mask interrupt 0b01 = Falling edge interrupt 0b10 = Rising edge interrupt 0b11 = Falling and rising edge interrupt
B3	DOx	When set for GPO (DIRx = 0): GPO output drive level is programmed with Dox. 0 = Logic low 1 = Logic high (DRVx = 1) and open-drain (DRVx = 0)
		When set for GPI (DIRx = 1): 0 = Clear DOx to 0 and set PUEx to 1 to enable the internal pullup. 1 = Set DOx to 1 and set PDEx to 1 to enable the internal pulldown. See the GPIO programming matrix (*Table 7. GPIO Programming Matrix*) for more information.
B2	DIx	When set for GPO (DIRx = 0): DIx is a don't care when GPO.
		When set for GPI (DIRx = 1): Input Drive Level. GPIOx input logic level is specified by DIx. 0 = Input logic low 1 = Input logic high When DIRx = 1, this bit is read only, writes to this bit are ignored.

CNFG_GPIOx: GPIO Configuration Register (continued)

BIT	NAME	DESCRIPTION
B1	DIRx	When AMEx = 0: GPIOx direction 0 = General purpose output (GPO) 1 = General purpose input (GPI) When AMEx = 1: When GPIO1/2/3/4 are set as an alternate mode output, write DIR1/2/3/4 (respectively) to 0 but note that the output is internally set to be active-high. When GPIO0/5/6 is set as an alternate mode input, DIR0/5/6 (respectively), determine if the signal is active-high or active-low. 0 = Active-low 1 = Active-high
B0	PPDRVx	When set for GPO (DIRx = 0): Push-pull output drive. GPIO output configuration is determined by PPDRVx. 0 = Open-drain 1 = Push-pull
		When set for GPI (DIRx = 1): PPDRVx is a don't care when GPI.

PUE_GPIO: GPIO Pullup Enable Register

REGISTER NAME	PUE_GPIO
I²C Slave Address	0x3C
Register Address	0x3E
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	PDE7	GPOIx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the GPIO programming matrix (Table 7) for more information. It is recommended that users disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.	0
B6	PDE6		0
B5	PDE5		0
B4	PDE4		0
B3	PDE3		0
B2	PDE2		0
B1	PDE1		0
B0	PDE0		0

PDE_GPIO: GPIO Pulldown Register

REGISTER NAME	PDE_GPIO
I²C Slave Address	0x3C
Register Address	0x3F
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	PDE7	GPOIx Pulldown Enable 0 = Pulldown disabled 1 = Pulldown enabled See the GPIO programming matrix (Table 7) for more information. It is recommended that the MAX77863 user disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.	0
B6	PDE6		0
B5	PDE5		0
B4	PDE4		0
B3	PDE3		0
B2	PDE2		0
B1	PDE1		0
B0	PDE0		0

AME_GPIO: Alternate Mode Enable GPIO Configuration Register

REGISTER NAME	AME_GPIO
I2C Slave Address	0x3C
Register Address	0x40
Reset Value	0b xxxx xxxx (“x” is an OTP bit)
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION
B7	AME7	Alternate Mode Enable for GPIO7 0 = Standard GPI or GPO as programmed by DIR7 1 = 1.25V buffered reference output. DBNC7 is a don’t care REFE_IRQx is a don’t care DO7 is a don’t care DI7 is a don’t care DIR7 is internally cleared to 0 PPDRV7 is a don’t care It is recommended that the MAX77863 user disable the pullup and pulldown resistors for GPIO7 when it operates in alternate mode.
B6	AME6	Alternate Mode Enable for GPIO6 0 = Standard GPI or GPO as programmed by DIR5 1 = SD1 dynamic voltage scaling input DBNC6 is valid REFE_IRQ6 is valid DO6 is a don’t care DI6 is valid DIR6 sets active low or active high PPDRV6 is a don’t care
B5	AME5	Alternate Mode Enable for GPIO5 0 = Standard GPI or GPO as programmed by DIR5 1 = SD0 dynamic voltage scaling input DBNC5 is valid REFE_IRQ5 is valid DO5 is a don’t care DI5 is valid DIR5 sets active-low or active-high PPDRV5 is a don’t care

AME_GPIO: Alternate Mode Enable GPIO Configuration Register (continued)

BIT	NAME	DESCRIPTION
B4	AME4	Alternate Mode Enable for GPIO4 0 = Standard GPI or GPO as programmed by DIR4 1 = 32kHz output (32k_OUT1) DBNC4 is a don't care REFE_IRQ4 is a don't care D04 is a don't care and the output logic level is set by the 32kHz oscillator. DI4 is a don't care DIR4 is internally cleared to 0 PPDRV4 is valid
B3	AME3	Alternate Mode Enable for GPIO3 0 = Standard GPI or GPO as programmed by DIR3 1 = Flexible power sequencer active-high output DBNC3 is a don't care, write to 0b00 REFE_IRQ3 is a don't care, write to 0b00 D03 is internally set by the flexible power sequencer in accordance with the FPS_GPIO3 register settings. DI3 is a don't care, write to 0 DIR3 is a don't care, write to 0 PPDRV3 is valid
B2	AME2	Alternate Mode Enable for GPIO2 0 = Standard GPI or GPO as programmed by DIR2 1 = Flexible power sequencer active-high output DBNC2 is a don't care, write to 0b00 REFE_IRQ2 is a don't care, write to 0b00 D02 is internally set by the flexible power sequencer in accordance with the FPS_GPIO2 register settings. DI2 is a don't care, write to 0 DIR2 is a don't care, write to 0 PPDRV2 is valid
B1	AME1	Alternate Mode Enable for GPIO1 0 = Standard GPI or GPO as programmed by DIR1 1 = Flexible power sequencer active-high output DBNC1 is a don't care, write to 0b00 REFE_IRQ1 is a don't care, write to 0x00 D01 is internally set by the flexible power sequencer in accordance with the FPS_GPIO1 register settings. DI1 is a don't care, write to 0 DIR1 is a don't care, write to 0 PPDRV1 is valid
B0	AME0	Alternate Mode Enable for GPIO0 0 = Standard GPI or GPO as programmed by DIR0 1 = Low-power mode control input DBNC0 is valid REFE_IRQ0 is valid DO0 is a don't care DI0 is valid DIR0 sets active-low or active-high PPDRV0 is a don't care

IRQ_LVL2_GPIO: GPIO Level 2 Interrupt Register

REGISTER NAME	IRQ_LVL2_GPIO
I2C Slave Address	0x3C
Register Address	0x0A
Reset Value	0b00000000
Access Type	Read
Special Features	Clear on read
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	EDGE7	GPIOx Edge Detection Interrupt 0 = No edges have been detected on GPIOx since the last time this bit was read. 1 = An edge corresponding to REFE_IRQx has been detected on GPIOx since the last time this bit was read. Note that REFE_IRQx = 0b00 sets an interrupt mask which forces EDGEx to 0.	0
B6	EDGE6		0
B5	EDGE5		0
B4	EDGE4		0
B3	EDGE3		0
B2	EDGE2		0
B1	EDGE1		0
B0	EDGE0		0

RTCINT: RTC Interrupt Register

REGISTER NAME	RTCINT
I^2C Slave Address	0x68
Register Address	0x00
Reset Value	0b00000000
Access Type	Read Only
Special Features	Clear on read
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	RTC60S	RTC 60 Second Timer Expired Interrupt 0 = 60s timer did not expire 1 = 60s timer expired	0
1	RTCA1	RTC Alarm 1 Interrupt 0 = No interrupt 1 = Interrupt	0
2	RTCA2	RTC Alarm 2 Interrupt 0 = No interrupt 1 = Interrupt	0
3	SMPL	SMPL Event Interrupt 0 = No interrupt 1 = Interrupt	0
4	RTC1S	RTC Periodic 1 Second Timer Expired Interrupt 0 = 1s timer did not expire 1 = 1s timer expired	0
5	WTSR	WTSR Interrupt 0 = No interrupt 1 = Interrupt Reserved. This bit is internally set to 0.	0
7:6	RSVD	Reserved	00

RTCINTM: RTC Interrupt Register Mask

REGISTER NAME	RTCINTM
I^2C Slave Address	0x68
Register Address	0x01
Reset Value	0x3F
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	RTC60SM	RTC 60 Second Timer Expired Interrupt Mask 0 = Not masked 1 = Masked	1
1	RTCA1M	RTC Alarm 1 Interrupt Mask 0 = Not masked 1 = Masked	1
2	RTCA2M	RTC Alarm 2 Interrupt Mask 0 = Not masked 1 = Masked	1
3	SMPLINTM	SMPL Event Interrupt Mask 0 = Not masked 1 = Masked	1
4	RTC1SM	RTC Periodic 1 Second Timer Expired Interrupt Mask 0 = Not masked 1 = Masked	1
5	RVSD	Reserved. This bit is a don't care.	1
7:6	RSVDM	Reserved	0b00

RTCCNTLM: RTC Control Mode Register

REGISTER NAME	RTCCNTLM
I^2C Slave Address	0x68
Register Address	0x02
Reset Value	0x03
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	BCDM	Access Control Of Bcd Bit In Register Rtccntl 0 = Writes to Bit 0 (BCD) of register address 0x03 (RTCCNTL) not allowed 1 = Writes to Bit 0 (BCD) of register address 0x03 (RTCCNTL) allowed	1
1	HRMODEM	Access Control of HRMODE Bit in Register RTCCNTL 0 = Writes to bit 0 (HRMODE) of register address 0x03 (RTCCNTL) not allowed 1 = Writes to bit 0 (HRMODE) of register address 0x03 (RTCCNTL) allowed	1
7:2	RSVD	Reserved	000000

RTCCNTL: RTC Control Register

REGISTER NAME	RTCCNTL
I^2C Slave Address	0x68
Register Address	0x03
Reset Value	0x00
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	BCD	Data Mode For Time And Calendar Updates 0 = Binary 1 = Binary-coded decimal (BCD) If BCDM = 0, writes to BCD are not allowed. When switching between binary and BCD, the time contents are no longer valid and must be reinitialized.	0
1	HRMODE	Hour Format Control 0 = 12-hour mode 1 = 24-hour mode Note that the AMPM bit is defined for the HOUR or HOURA register only which makes sense for the 12-hr mode as the 24-hr mode already has AM/PM implied. If HRMODEM = 0, writes to HRMODE are not allowed. When switching between 12-hour and 24-hour mode, the registers do not automatically update. The user must reprogram all registers.	0
7:2	RSVD	Reserved	000000

RTCUPDATE0: RTC Update 0 Register

REGISTER NAME	RTCUPDATE0
I^2C Slave Address	0x68
Register Address	0x04
Reset Value	0x0A
Access Type	Read/write
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	UDR	Access control to update RTC registers by transferring data from the “write buffers” to the actual registers. 0 = No action 1 = Update register Typical transfer time from write buffers to the timekeeper counters is 15ms after UDR is set. UDR is internally cleared to after the registers data has been transferred.	0
1	FCUR	Flags Cleared Upon Read Control Bit 0 = User must write 0 to clear UDF and RBUDF. 1 = UDF and RBUDF cleared upon read.	1
2	FREEZE_SEC	This Bit Freezes The Sec Counter From Incrementing 0 = SEC counter increments normally. 1 = SEC counter stops incrementing which stops all subsequent registers in the timer string (MIN, HOUR, DAY, etc). This setting effectively stops the clock.	0
3	Reserved	Reserved	1
4	RBUDR	Access control to update RTC registers by transferring data from the actual registers to the “read buffers.” 0 = No action 1 = Update “read buffers” Typical transfer time from timekeeper counters to read is 15ms after RBUDR is set. RBUDR is internally cleared to after the registers data has been transferred.	0
7:5	RSVD	Reserved	000

RTCUPDATE1: RTC Update 1 Register

REGISTER NAME	RTCUPDATE1
I²C Slave Address	0x68
Register Address	0x05
Reset Value	0x00
Access Type	Read only
Special Feature	Clear on read when FCUR is set
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	UDF	This bit is an update flag that indicates when an actual transfer of data from the “write Buffers” to the corresponding register occurs. When this bit is 1, then the user can initiate a new write operation, otherwise it is not safe to do so. 0 = Update not done 1 = Update done Typical update time is 15ms after the UDR bit is set. If FCUR bit (RTCUPDATE0 register) is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.	0
1	RBUDF	This bit is an update flag that indicates when an actual transfer of data from the actual registers to “Read Buffers” occurs. When this bit is 1, then the user can initiate a new read operation, otherwise it is not safe to do so. 0 = Update not done 1 = Update done Typical update time is 15ms after the RBUDR bit is set. If FCUR bit (RTCUPDATE0 register) is 1, this bit is automatically cleared after a read operation. If FCUR is 0, the user must write a 0 to clear it.	0
7:2	RSVD	Reserved	000000

RTCSMPL: RTC Sudden Momentary Power Loss Register

REGISTER NAME	RTCSMPL
I^2C Slave Address	0x68
Register Address	0x06
Reset Value	0x00
Access Type	Read/write
Reset Condition	V_{RTC} < $V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
1:0	RVSD	Reserved	0b00
3:2	SMPLT[1:0]	Sets the SMPL Timer Threshold 0b00 = 0.5s 0b01 = 1.0s 0b10 = 1.5s 0b11 = 2.0s	0b00
5:4	RSVD	Reserved	00
6	RVSD	Reserved. This bit is a don't care.	0
7	SMPL_EN	SMPL Feature Enable Control 0 = SMPL disabled 1 = SMPL enabled	0

RTCSEC: RTC Seconds Register

REGISTER NAME	RTCSEC
I^2C Slave Address	0x68
Register Address	0x07
Reset Value	0x00
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	V_{RTC} < $V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
6:0	SEC[6:0]	RTC Seconds Counter Register In binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format, valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.	0000000
7	RSVD	Reserved	0

RTCMIN: RTC Minutes Register

REGISTER NAME	RTCMIN
I^2C Slave Address	0x68
Register Address	0x08
Reset Value	0x00
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
6:0	MIN[6:0]	RTC Minutes Counter Register In binary format (BCD = 0), valid values for B6 through B0 are 0 through 59. In BCD format (BCD = 1), valid data for B6 through B4 are 0 through 5, and valid data for B3 through B0 are 0 through 9.	0b0000000
7	RSVD	Reserved	0

RTCHOUR: RTC Hours Register

REGISTER NAME	RTCHOUR
I^2C Slave Address	0x68
Register Address	0x09
Access Type	Read/write
Reset Value	0x01
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	Default
5:0	HOUR[5:0]	RTC Hours Counter Register Note that there would be two possibilities for values chosen for B5 through B0 depending on the current status of the HRMODE Bit: If HRMODE = 1 (24Hr Mode) Binary Mode (BCD = 0): B5 is zero, and B4 through B0 valid values are 0 through 23. BCD Mode (BCD = 1): Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 23). If HRMODE = 0 (12 Hr Mode) Binary Mode (BCD = 0): B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12. BCD Mode (BCD = 1): Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number does not exceed 12).	0b000001
6	AMPM	AM/PM Selection. AMPM is only valid when the clock is set for 12-hour mode (HRMODE = 0). When the clock is set for 24-hour mode, this bit is a don't care. 0 = AM 1 = PM	0
7	RSVD	Reserved	0

RTCDOW: RTC Day-of-Week Register

REGISTER NAME	RTCDOW
I^2C Slave Address	0x68
Register Address	0x0A
Reset Value	0x01
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	SUN	Bits B6 through B0 each represent one day of the week. As such, only one bit is set at a time. B[6:0] = 000_0001 represents Sunday B[6:0] = 000_0010 represents Monday B[6:0] = 000_0100 represents Tuesday B[6:0] = 000_1000 represents Wednesday B[6:0] = 001_0000 represents Thursday B[6:0] = 010_0000 represents Friday B[6:0] = 100_0000 represents Saturday	1
1	MON		0
2	TUE		0
3	WED		0
4	THU		0
5	FRI		0
6	SAT		0
7	RSVD	Reserved	0

RTCMONTH: RTC Month Register

REGISTER NAME	RTCMONTH
I^2C Slave Address	0x68
Register Address	0x0B
Reset Value	0x01
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	Default
4:0	MONTH[4:0]	RTC Months Counter Register In Binary format (BCD = 0), valid values for B4 through B0 are 1 through 12. In BCD format (BCD = 1), valid data for B4 is either 0 or 1, and valid data for B3 through B0 are 0 through 9 (the full value in BCD format does not exceed 12 and must be greater than zero).	0b00001
7:5	RSVD	Reserved	0b000

RTCYEAR: RTC Year Register

REGISTER NAME	RTCYEAR
I^2C Slave Address	0x68
Register Address	0x0C
Reset Value	0x00
Access Type	Read/write
Special Features	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
7:0	YEAR[7:0]	RTC Years Counter Register In Binary format (BDC = 0), valid values for B7 through B0 are 0 through 99. In BCD format (BCD = 1), valid data for B7 through B4 are 0 through 9, and similarly valid data for B3 through B0 are 0 through 9.	0b00000000

RTCDOM: RTC Day-of-Month Register

REGISTER NAME	RTCDOM
I^2C Slave Address	0x68
Register Address	0x0D
Reset Value	0x01
Access Type	Read/Write
Special Features	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
5:0	DAY[5:0]	RTC Days in a Month Register In Binary format (BCD = 0), valid values for B5 through B0 are 1 through 31. In BCD format (BCD = 1), valid data for B4 through B5 are 0 through 3, and valid data for B3 through B0 are 0 through 9 (the full value should be greater than 0 but not exceed 31). Furthermore, there is a restriction on choosing the number of days in a month according to the selected month and year as shown below: For months 1, 3, 5, 7, 8, 10, and 12 the selected value for B5 through B0 must be 1 through 31. For months 4, 6, 9, and 11 the selected value for B5 through B0 must be 1 through 30. For month 2, or month of Feb., the selected value for B5 through B0 must be 1 through 28 for normal years, or must be 1 through 29 for leap years. Does not account for solar years. Leap years are those that are evenly divisible by 4. 0, 4, 8, . . . 24, 28, . . .72, 76 . . . 92, 96	0b000001
7:6	RSVD	Reserved	0b000

Note: It is the responsibility of the user to make sure that days selected for the month actually matches the intended number of days in the month. For example, a user should not select 31 days for the months of February, April, June, September, or November.

RTCSECAx: RTC ALARMx Seconds Register

REGISTER NAME	RTCSECAx
I^2C Slave Address	0x68
Register Address	0x0E for RTCSECA1 0x15 for RTCSECA2
Reset Value	0x00
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	Default
6:0	SECAx[6:0]	RTC Seconds Alarm Register If the value of SECAx is equal to the value of SEC and AESECAx = 1, an RTCAx alarm interrupt is generated.	0b0000000
7	AESECAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

RTCMINAx: RTC ALARMx Minutes Register

REGISTER NAME	RTCMINAx
I^2C Slave Address	0x68
Register Address	0x0F for RTCMINA1 0x16 for RTCMINA2
Reset Value	0x00
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
6:0	MINAx[6:0]	RTC Minutes Alarm Register If the value of MINAx is equal to the value of MIN and AEMINAx is 1, an RTCAx alarm interrupt is generated.	0b0000000
7	AEMINAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

RTCHOURAx: RTC ALARMx Hours Register

REGISTER NAME	RTCHOURAx
I^2C Slave Address	0x68
Register Address	0x10 for RTCHOURA1 0x17 for RTCHOURA2
Reset Value	0x00
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
5:0	HOURAx[5:0]	RTC Hours Alarm Register If the value of HOURAx is equal to the value of HOUR and AEHOURAx is 1, an RTCAx alarm interrupt is generated. If HRMODE = 1 (24-hr mode) Binary mode: B5 is zero, and B4 through B0 valid values are 0 through 23. BCD mode: Valid values for B5 through B4 are 0 through 2, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 23). If HRMODE = 0 (12-hr mode) Binary mode: B5 and B4 are 0, and valid values for B3 through B0 are 1 through 12. BCD mode: Valid values for B5 through B4 are 0 through 1, and valid values for B3 through B0 are 0 through 9 (the full number should not exceed 12).	0b000000
6	AMPMAx	AM/PM selection, only valid during 12-hr mode. 0 = AM 1 = PM	0
7	AEHOURAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

RTCDOWA1: RTC ALARMx Day-of-Week Register

REGISTER NAME	RTCDOWAx
I^2C Slave Address	0x68
Register Address	0x11 for RTCDOWA1 0x18 for RTCDOWA2
Reset Value	0x01
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
0	SUNAx	RTC Day Of Week Alarm Register If the value of RTCDOWAx is equal to the value of DOW and AEDOWAx is 1, an RTCAx alarm interrupt is generated. Bits B6 through B0 each represents one day of the week. This would dictate that only one bit at a time is allowed to be set as shown below: B[6:0] = 0b000_0001 represents Sunday B[6:0] = 0b000_0010 represents Monday B[6:0] = 0b000_0100 represents Tuesday B[6:0] = 0b000_1000 represents Wednesday B[6:0] = 0b001_0000 represents Thursday B[6:0] = 0b010_0000 represents Friday B[6:0] = 0b100_0000 represents Saturday	1
1	MONAx		0
2	TUEAx		0
3	WEDAx		0
4	THUAx		0
5	FRIAx		0
6	SATAx		0
7	AEDOWAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

RTCMONTHAx: RTC ALARMx Month Register

REGISTER NAME	RTCMONTHAx
I^2C Slave Address	0x68
Register Address	0x12 for RTCMONTHA1 0x19 for RTCMONTHA2
Reset Value	0x01
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
4:0	MONTHAx[4:0]	RTC Month Alarm Register If the value of MONTHAx is equal to the value of MONTH and AEMONTHAx is 1, an RTCAx alarm interrupt is generated.	0b00001
6:5	RSVD	Reserved	0b00
7	AEMONTHAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

RTCYEARAx: RTC ALARMx Year Register

REGISTER NAME	RTCYEARAx
I^2C Slave Address	0x68
Register Address	0x13 for RTCYEARA1 0x1A for RTCYEARA2
Reset Value	0x00
Access Type	Read/write
Special Features	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
6:0	YEARAx[6:0]	RTC Year Alarm Register If the value of YEARAx is equal to the value of YEAR and AEYEARAx is 1, an RTCAx alarm interrupt is generated.	0b0000000
7	AEYEARAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

RTCDOMAx: RTC ALARMx Day-of-Month Register

REGISTER NAME	RTCDOMAx
I^2C Slave Address	0x68
Register Address	0x14 for RTCDOMA1 0x1B for RTCDOMA2
Reset Value	0x01
Access Type	Read/write
Special Feature	This is a double buffered register. Writes to this register are only uploaded to the RTC when UDR is set. This register is only updated from the RTC when RDUDR is set.
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
5:0	DAYAx[5:0]	RTC Day Of Month Alarm 1 Register If the value of DAYAx is equal to the value of DAY and AEDAYAx is 1, an RTCAx alarm interrupt is generated.	0b000001
6	RSVD	Reserved	0
7	AEDAYAx	Alarm Enable Control 0 = Alarm disable 1 = Alarm enable	0

Note: It is the responsibility of the user to make sure that days selected for the month actually matches the intended number of days in the month. For example, a user should not select 31 days for the months of February, April, June, September, or November.

RTC Block Issues

Issue 1: Does not account for solar year which induces a calendar error on Feb 29, 2100.

Issue 2: Does not allow alarms in BCD to be set past year 2079.

Issue 3: Does not have ability to set the century. This is not necessarily a problem but it means that the host has to control the century.

Pedigree

The RTC is shared between the PR83, PR80, and PQ63. PR61 and PR77 use a very similar RTC.

CNFG1_32K: 32kHz Oscillator Configuration 1

REGISTER NAME	CNFG1_32K
I^2C Slave Address	0x3C
Register Address	0x03
Reset Value	0b x1xx 11xx ("x" is an OTP bit)
Access Type	Read/write
Reset Condition	B[7:4] are reset by $V_{RTC} < V_{RTCUVLO}$ B[3:0] are reset by $V_{RTC} < V_{RTCUVLO}$ or global shutdown

BIT	BIT NAME	DESCRIPTION	DEFAULT
B7	32K_OK	Status of Crystal Driver Output 0 = Output frequency is not OK. 1 = Output frequency is OK. This is read only.	0
B6		Reserved	1
B[5:4]	32KLOAD[1:0]	Crystal Driver Load Capacitance 0b00 = 12pF per node 0b01 = 22pF per node 0b10 = No internal load cap selected 0b11 = 10pF per node	xx
B3		Reserved	1
B2	32K_OUT0_EN	32kHz Oscillator Output Enable 0 = Disabled 1 = Enabled	1
B[1:0]	PWR_MD_32K[1:0]	32kHz Oscillator Mode of Operation 0b00 = Low-power mode 0b01 = Global low-power mode. The oscillator operates in low-jitter mode when the global low-power mode signal is low. When the global low-power mode signal is high, the oscillator operates in low-power mode. 0b10 = Same as 0b00 0b11 = Low-jitter mode	xx

CNFGBBC: Backup Battery Configuration Register

REGISTER NAME	CNFGBBC
I^2C Slave Address	0x3C
Register Address	0x04
Reset Value	0x41
Access Type	Read/write
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	Default
7:6	BBCRS[1:0]	Output Resistor 0x00 = 0.1kΩ0x01 = 1kΩ 0x02 = 3kΩ 0x03 = 6kΩ	0b01
5	BBCLOWIEN	Low Charging Current Enable 0 = Enable 1 = Disable	0
4:3	BBCVS[1:0]	Charging Voltage Limit Setting 0x00 = 2.5V 0x01 = 3.0V 0x02 = 3.3V 0x03 = 3.5V	0b00
2:1	BBCCS[1:0]	Charging Current Setting BBCLOWIEN = 0 0x00 = 50мA 0x01 = 50μA 0x02 = 50μA 0x03 = 100μA BBCLOWIEN = 1 0x00 = 200μA 0x01 = 600μA 0x10 = 800μA 0x11 = 400μA	0b00
0	BBCEN	Backup Battery Charger Enable 0 = Backup battery charger off 1 = Backup battery charger on	1

ONOFFCNFG1: On/Off Controller Configuration Register 1

REGISTER NAME	ONOFFCNFG1
I^2C Slave Address	0x3C
Register Address	0x41
Reset Value	0b 0xxx x00x (“x” is an OTP bit)
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION
B7	SFT_RST	Software Reset. See Figure 4 for a flow diagram. 0 = No action 1 = Generates a global shutdown event that initiates the FPS0 and FPS1 power-down event and generates a reset. If both SFT_RST and PWR_OFF are set, the resulting action is SFT_RST. See the *SFT_RST and PWR_OFF Logic* table.
B6	RSVD	Reserved. Write 1. Read is don’t care.
B[5:3]	MRT[2:0]	Manual Reset Time 0b000 = 2s 0b100 = 6s 0b001 = 3s 0b101 = 8s 0b010 = 4s 0b110 = 10s 0b011 = 5s 0b111 = 12s
B2	SLPEN	Sleep Enable 0 = Pulling EN1 low does not place the AP into sleep mode 1 = Clears the latch that enables FPS1 from a wakeup event (“WAKE”). With this latch clear, the AP can be placed into sleep mode by pulling EN1 low. SLPEN is automatically cleared when the MAX77863 “OFF” signal rises or when a wakeup event occurs.
B1	PWR_OFF	Power Off. See Figure 4 0 = No action 1 = Generates a global shutdown event that initiates the FPS0 and FPS1 power-down event but does not generate a reset. Note that PWR_OFF is cleared at the end of any global shutdown event that it generates. If both SFT_RST and PWR_OFF are set, the resulting action is SFT_RST. See the *SFT_RST and PWR_OFF Logic* table.
B0	EN0DLY	EN0 Delay 0 = The only delay for EN0 is the debounce circuit. 1 = In addition to the debounce circuit, there is an addition 1 second delay for EN0.

SFT_RST and PWR_OFF Logic

SFT_RST	PWR_OFF	BEHAVIOR
0	0	No action
0	1	Power off function
1	0	Software reset function
1	1	Reserved

ONOFFCNFG2: On/Off Controller Configuration Register 2

REGISTER NAME	ONOFFCNFG2
I^2C Slave Address	0x3C
Register Address	0x42
Reset Value	0b 000x x111
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION
B7	SFT_RST_WK	Automatic Wakeup Due To Software Reset (Figure 4) 0 = Setting SFT_RST results in a power down and default off state where the device waits for a wakeup event. 1 = Setting SFT_RST results in a power cycle and the default on state.
B6	WD_RST_WK	Automatic Wakeup Due To System Watchdog Reset (Figure 4) 0 = A system watchdog timer expiring results in a power down and default-off state where the device waits for a wakeup event. 1 = a system watchdog time expiring results in a power cycle and the default on state
B5	nSLP_LPM_MSK	Active-Low, Low-Power Mode During Sleep Mask Bit 0 = Masked. EN1 cannot affect EN1_LPM and LPM_BUS. 1 = Unmasked. If the IC is not asserting RSO the EN1 signal can affect EN1_LPM and LPM_BUS. See Figure 8 for the simplified logic. nSLP_LPM_MSK is automatically cleared when the MAX77863 “OFF” signal rises.
B4	WK_ACOK	Wakeup on ACOK 0 = An ACOK event does not generate a wakeup signal. 1 = An ACOK event generates a wakeup signal.
B3	WK_LID	Wakeup on LID 0 = A LID event does not generate a wakeup signal. 1 = A LID event generates a wakeup signal.
B2	WK_ALARM1R	Wakeup on ALARM1_R 0 = An ALARM1_R event does not generate a wakeup signal. 1 = An ALARM1_R event generates a wakeup signal.
B1	WK_ALARM2R	Wakeup on ALARM2_R 0 = An ALARM2_R event does not generate a wakeup signal. 1 = An ALARM2_R event generates a wakeup signal.
B0	WK_EN0	Wakeup on EN0 0 = An EN0 event does not generate a wakeup signal. 1 = An EN0 event generates a wakeup signal.

ONOFFIRQ: On/Off Controller Interrupt Register

REGISTER NAME	ONOFFIRQ
I2C Slave Address	0x3C
Register Address	0x0B
Reset Value	0x00
Access Type	Read
Special Features	Clear on read
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	ACOK_R	ACOK Rising Interrupt 0 = No ACOK rising edges have occurred since the last time this bit was read. 1 = An ACOK rising edge as occurred since the last time this bit was read.	0
B6	ACOK_F	ACOK Falling Interrupt 0 = No ACOK falling edges have occurred since the last time this bit was read. 1 = An ACOK falling edge as occurred since the last time this bit was read.	0
B5	LID_R	LID Rising Interrupt 0 = No LID rising edges have occurred since the last time this bit was read. 1 = An LID rising edge as occurred since the last time this bit was read.	0
B4	LID_F	LID Falling Interrupt 0 = No LID falling edges have occurred since the last time this bit was read. 1 = An LID falling edge as occurred since the last time this bit was read.	0
B3	EN0_R	EN0 Rising Interrupt 0 = No EN0 rising edges have occurred since the last time this bit was read. 1 = An EN0 rising edge as occurred since the last time this bit was read.	0
B2	EN0_F	EN0 Falling Interrupt 0 = No EN0 falling edges have occurred since the last time this bit was read. 1 = An EN0 falling edge as occurred since the last time this bit was read.	0
B1	EN0_1SEC	EN0 Active for 1s Interrupt 0 = EN0 has not been active for 1 second since the last time this bit was read. 1 = EN0 has been active for 1 second since the last time this bit was read.	0
B0	MRWRN	Manual Reset Warning Interrupt The time for the hard power off warning is one setting shorter than what is programmed by MRT[2:0] (i.e., HRDPOW[2:0]-1). When MRT[2:0] = 0b000, MRWRN is essentially a don't care. 0 = EN0 has not been active for MRT[2:0]-1 since the last time this bit was read. 1 = EN0 has been active for MRT[2:0]-1 since the last time this bit was read.	0

ONOFFIRQM: On/Off Controller Interrupt Mask Register

REGISTER NAME	ONOFFIRQM
I^2C Slave Address	0x3C
Register Address	0x12
Reset Value	0x00
Access Type	Read/write
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B7	ACOK_RM	ACOK Rising Interrupt Mask 0 = Unmasked 1 = Masked	0
B6	ACOK_FM	ACOK Falling Interrupt Mask 0 = Unmasked 1 = Masked	0
B5	LID_RM	LID Rising Interrupt Mask 0 = Unmasked 1 = Masked	0
B4	LID_FM	LID Falling Interrupt Mask 0 = Unmasked 1 = Masked	0
B3	EN0_RM	EN0 Rising Interrupt Mask 0 = Unmasked 1 = Masked	0
B2	EN0_FM	EN0 Falling Interrupt Mask 0 = Unmasked 1 = Masked	0
B1	EN0_1SECM	EN0 Active for 1s Interrupt Mask 0 = Unmasked 1 = Masked	0
B0	MRWRNM	Manual Reset Warning Interrupt Mask 0 = Unmasked 1 = Masked	0

ONOFFSTAT: On/Off Controller Status Register

REGISTER NAME	ONOFFSTAT
I^2C Slave Address	0x3C
Register Address	0x15
Reset Value	0x00
Access Type	Read
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION	DEFAULT
B[7:3]		Reserved	0b00000
B2	EN0	EN0 Input Status For OTP_EN0AL = 0 0 = EN0 is not active (logic low). 1 = EN0 is active (logic high). For OTP_EN0AL = 1 0 = EN0 is not active (logic high). 1 = EN0 is active (logic low).	0
B1	ACOK	ACOK Input Status For OTP_ACOKAL = 0 0 = ACOK is not active (logic low). 1 = ACOK is active (logic high). For OTP_ACOKAL = 1 0 = ACOK is not active (logic high). 1 = ACOK is active (logic low).	0
B0	LID	LID Input Status For OTP_LIDAL = 0 0 = LID is not active (logic low). 1 = LID is active (logic high). For OTP_LIDAL = 1 0 = LID is not active (logic high). 1 = LID is active (logic low).	0

NVERC: Non-Volatile Event Recorder

REGISTER NAME	NVERC
I^2C Slave Address	0x3C
Register Address	0x0C
Reset Value	0x40
Access Type	Read only
Special Features	Clear on read
Reset Condition	$V_{RTC} < V_{RTCUVLO}$

BIT	BIT NAME	DESCRIPTION	DEFAULT
B7	RSTIN	Shutdown Due to Reset Input 0 = The reset input signal (RSI) did not cause a global shutdown. 1 = The reset input signal (RSI) caused a global shutdown.	0
B6	MBU	Shutdown Due to Main-Battery Undervoltage Lockout 0 = Main-battery did not cause a global shutdown. 1 = The main-battery caused a global shutdown by falling below its UVLO threshold ($V_{MBATT} < V_{MBATTUVLO}$). If the sudden momentary power loss (SMPL) function is enabled, the PMIC can automatically recover from a momentary power loss. See the *Voltage Monitors* section for more information.	1
B5	MBO	Shutdown Due to Main-Battery Overvoltage Lockout 0 = Main-battery did not cause a global shutdown. 1 = The main-battery caused a global shutdown by rising above its OVLO threshold ($V_{MBATT} < V_{MBATTOVLO}$).	0
B4	MBLSD	Shutdown Due to Main-Battery Low 0 = Main-battery low did not cause a global shutdown. 1 = Main-battery low caused a global shutdown because MBLPD is set and $V_{MON} < V_{MONL}$.	0
B3	TOVLD	Shutdown Due to Junction Temperature Overload 0 = the junction temperature did not cause a global shutdown 1 = the junction temperature caused a global shutdown by rising above T_{JSHDN}.	0
B2	HDRST	Shutdown Due to Hard-Reset (a.k.a. Manual Reset) 0 = The hard-reset function did not cause a global shutdown. 1 = The hard-reset function caused a global shutdown.	0
B1	WTCHDG	Shutdown Due to System Watchdog Timer 0 = The system watchdog timer did not cause a global shutdown. 1 = The system watchdog timer caused a global shutdown.	0
B0	SHDN	Shutdown Due to Shutdown Pin (SHDN) 0 = The shutdown pin did not cause a global shutdown. 1 = The shutdown pin caused a global shutdown.	0

NVERC: Non-Volatile Event Recorder (continued)

REGISTER ADDRESS (HEX)	REGISTER NAME	B7	B6	B5	B4	B3	B2	B1	B0
0x43	CNFGFPS0	RSVD	RSVD	TFPS0[2:0]			SRCFPS0[1:0]		ENFPS0
0x44	CNFGFPS1	RSVD	RSVD	TFPS1[2:0]			SRCFPS1[1:0]		ENFPS1
0x45	CNFGFPS2	RSVD	RSVD	TFPS2[2:0]			SRCFPS2[1:0]		ENFPS2
0x4F	FPS_SD0	FPSSRC_SD0[1:0]		FPSPU_SD0[2:0]			FPSPD_SD0[2:0]		
0x50	FPS_SD1	FPSSRC_SD1[1:0]		FPSPU_SD1[2:0]			FPSPD_SD1[2:0]		
0x51	FPS_SD2	FPSSRC_SD2[1:0]		FPSPU_SD2[2:0]			FPSPD_SD2[2:0]		
0x52	FPS_SD3	FPSSRC_SD3[1:0]		FPSPU_SD3[2:0]			FPSPD_SD3[2:0]		
0x53	FPS_SD4	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD
0x54	FPS_GPIO1	FPSSRC_GPIO1[1:0]		FPSPU_GPIO1[2:0]			FPSPD_GPIO1[2:0]		
0x55	FPS_GPIO2	FPSSRC_GPIO2[1:0]		FPSPU_GPIO2[2:0]			FPSPD_GPIO2[2:0]		
0x56	FPS_GPIO3	FPSSRC_GPIO3[1:0]		FPSPU_GPIO3[2:0]			FPSPD_GPIO3[2:0]		
0x57	FPS_RSO	FPSSRC_RSO[1:0]		FPSPU RSO[2:0]			FPSPD_RSO[2:0]		

CNFGFPSx : Flexible Power Sequencing x Master Configuration Register

This register contains the configuration information for the flexible power sequencing master timer x configuration.

REGISTER NAME	**CNFGFPS0/1**
I^2C Slave Address	0x3C
Register Address	0x43: CNFGFPS0 0x44: CNFGFPS1
Reset Value	0b 00xx xxxx (“x” is an OTP bit)
Access Type	Read/write
Special Features	
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION
MSB B7		Reserved for future use.
B6		Reserved for future use.
B5	TFPSx[2:0]	Timer Period. Specifies the time period between each sequencer event. 0x00 = 0b000 = 40µs 0x04 = 0b100 = 640µs 0x01 = 0b001 = 80µs 0x05 = 0b101 = 1,280µs 0x02 = 0b010 = 160µs 0x06 = 0b110 = 2,560µs 0x03 = 0b011 = 320µs 0x07 = 0b111 = 5,120µs
B4		
B3		
B2	SRCFPSx[1:0]	Enable Source. Specifies the enable source for the sequencer. 0b00 = EN0 hardware input 0b01 = EN1 hardware input 0b10 = ENFPSx software bit 0b11 = Reserved
B1		
LSB B0	ENFPSx	Software Enable 0 = Disable FPS0/1 1 = Enable FPS0/1 X = ENFPSx is a don’t care if SRCFPS0/1[1:0]≠0b10

CNFGFPSx : Flexible Power Sequencing x Master Configuration Register (continued)

REGISTER NAME	CNFGFPS2
I^2C Slave Address	0x3C
Register Address	0x45: CNFGFPS2
Reset Value	0b 00xx xxxx (“x” is an OTP bit)
Access Type	Read/Write
Special Features	
Reset Condition	Global Shutdown

BIT	NAME	DESCRIPTION
MSB B7		Reserved for future use.
B6		Reserved for future use.
B5	TFPS2[2:0]	Timer Period. Specifies the time period between each sequencer event. 0x00 = 0b000 = 40μs 0x01 = 0b001 = 80μs 0x02 = 0b010 = 160μs 0x03 = 0b011 = 320μs 0x04 = 0b100 = 640μs 0x05 = 0b101 = 1,280μs 0x06 = 0b110 = 2,560μs 0x07 = 0b111 = 5,120μs
B4		
B3		
B2	SRCFPS2[1:0]	Enable Source. Specifies the enable source for the sequencer. 0b00 = FPS2 enable follows FPS0 0b01 = FPS2 enable follows FPS1 0b10 = ENFPS2 software bit 0b11 = Reserved
B1		
LSB B0	ENFPS2	Software Enable 0 = Disable FPS2 1 = Enable FPS2 X = ENFPS2 is a don’t care if SRCFPS2[1:0]≠0b10

FPS_x: Flexible Power Sequencing Slave Configuration Register (FPSx)

This register contains the configuration information for the flexible power sequencing slave configuration register x.

REGISTER NAME	FPS_x
I2C Slave Address	0x3C
Register Address	18 total FPSx registers–0x46 to 0x57
Reset Value	0b xxxx xxxx (“x” is an OTP bit)
Access Type	Read/write
Special Features	
Reset Condition	Global shutdown

BIT	NAME	DESCRIPTION
B[7:6]	FPSSRCx[1:0]	Regulator Flexible Power Sequencer Source 0b00 = FPS0 0b01 = FPS1 0b10 = FPS2 0b11 = Not configured as part of a flexible power sequence: The LDO enables are controlled by PWR_MD_Lx. The step-down regulator enables are controlled by PWR_MD_SDx. nRST_IO is transparent with respect to the flexible power sequencers.
B[5:3]	FPSPUx[2:0]	Regulator Flexible Power Sequencer Power Up Period. Specifies the power up time slots. 0x0 = 0b000 = 0 0x1 = 0b001 = 1 0x2 = 0b010 = 2 0x3 = 0b011 = 3 0x4 = 0b100 = 4 0x5 = 0b101 = 5 0x6 = 0b110 = 6 0x7 = 0b111 = 7
B[2:0]	FPSPDx[2:0]	Regulator Flexible Power Sequencer Power Up Period. Specifies the power up time slots. 0x0 = 0b000 = 0 0x1 = 0b001 = 1 0x2 = 0b010 = 2 0x3 = 0b011 = 3 0x4 = 0b100 = 4 0x5 = 0b101 = 5 0x6 = 0b110 = 6 0x7 = 0b111 = 7

Typical Application Circuit

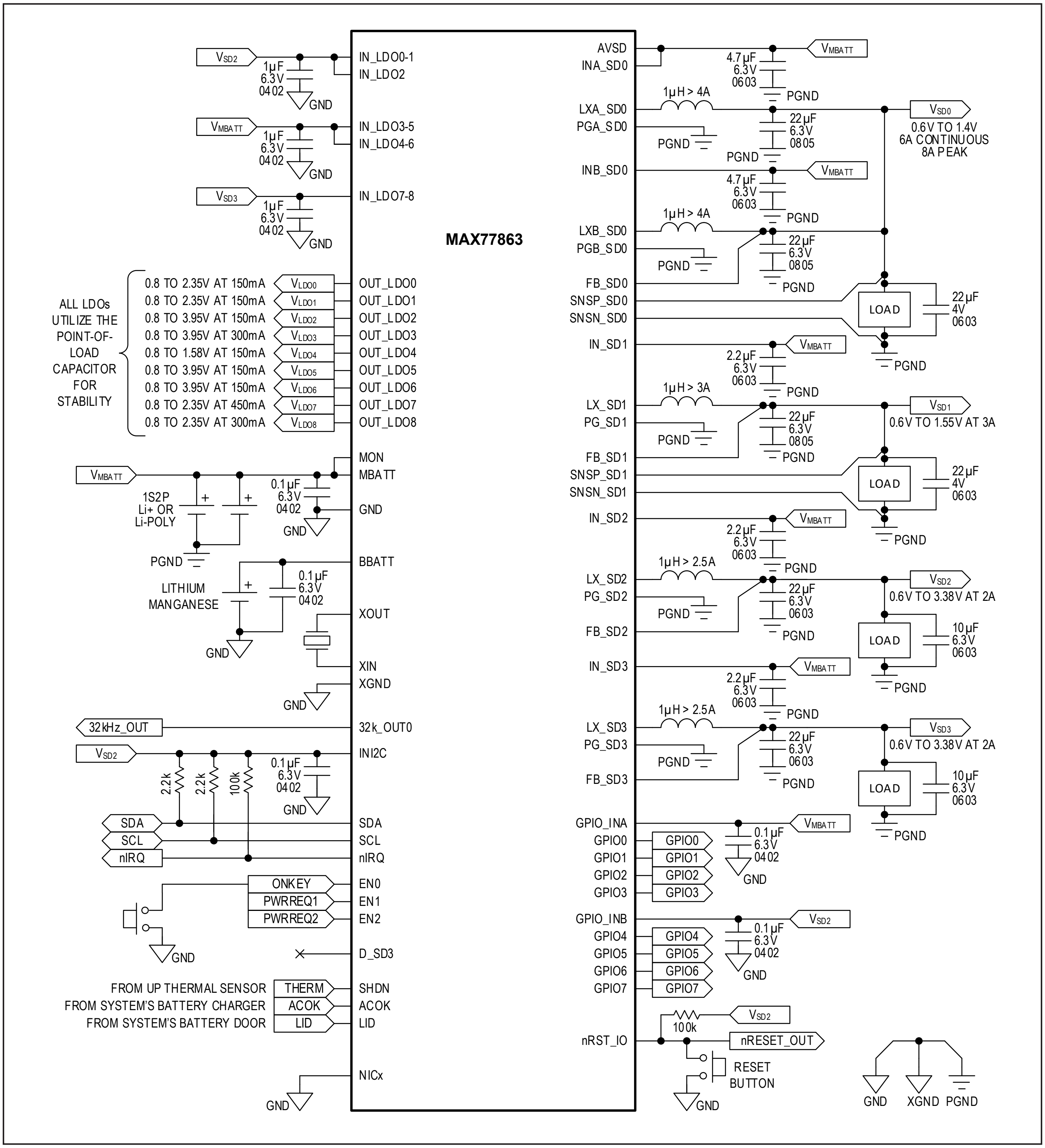

Figure 40. MAX77863 Typical Application Circuit for 1s Battery Configuration

Typical Application Circuit (continued)

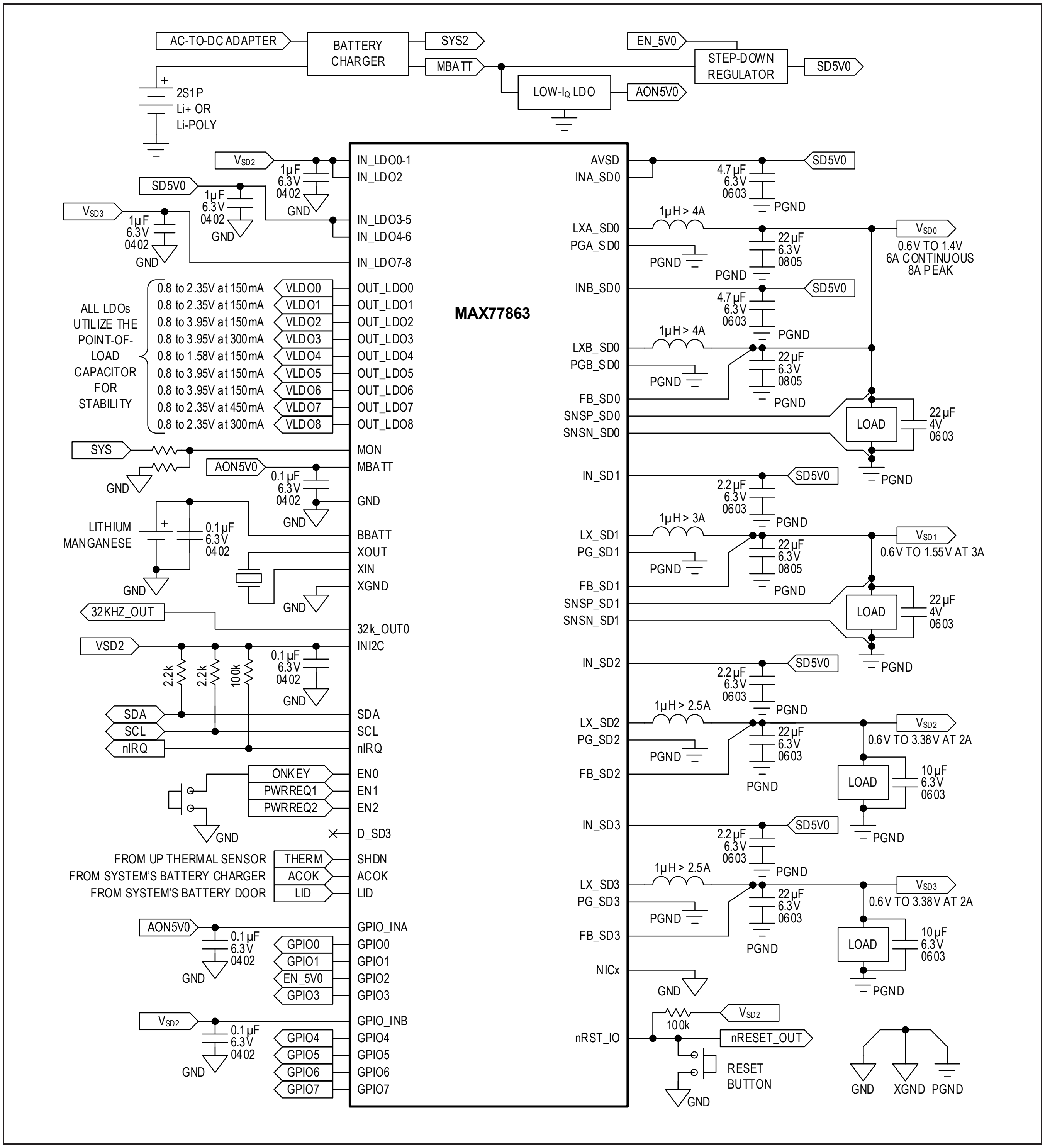

Figure 41. MAX77863 Typical Application Circuit for 2s Battery Configurations

Ordering Information

PART	PIN-PACKAGE	OPTIONS
MAX77863AEWJ+T	90-WLP, 0.4mm Pitch, 10 x 9 Array, 4.1mm x 3.8mm x 0.7mm	4 DC-to-DC OTP Version CID4 = 0x01

All devices are specified over the -40°C to +85°C ambient operating temperature range.
+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Table and reel.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
90 Bump, WLP 0.4mm Pitch, 10 x 9 Array 4.1 x 3.8 x 0.7mm	W903A4+1	**21-0573**	**Maxim's Application Note 1891**: Wafer-Level Package (WLP)

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/19	Initial release	—
1	2/20	Fixed typo in title	1–183

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.