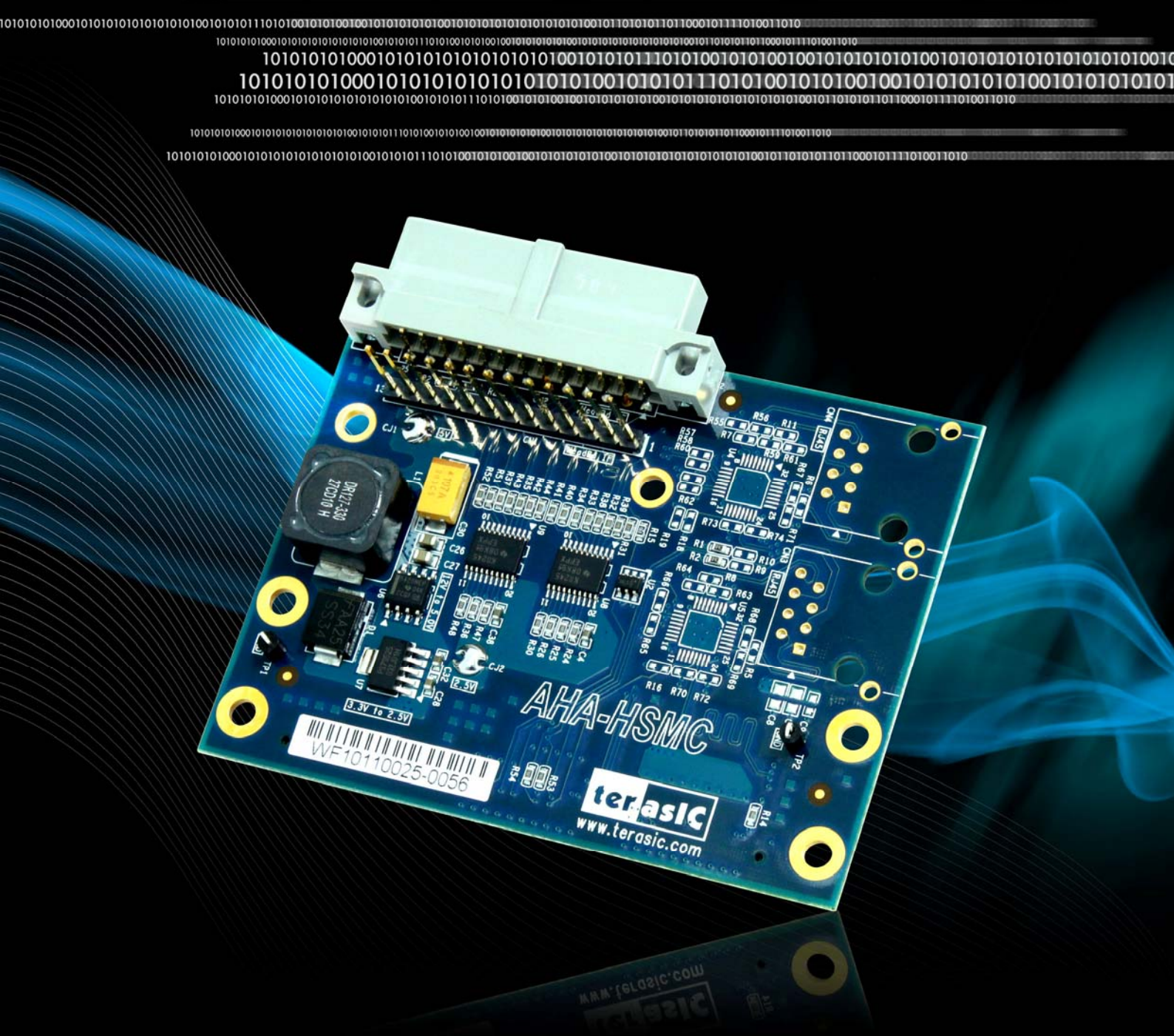
AHA-HSMC

Aptina Sensor Adapter Card

User Manual



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CONTENTS

Chapter 1

Introduction of the AHA-HSMC

FPGAs and image processing are two terms that are becoming linked together in recent years. This is due to the strong advantages FPGAs present when entering into the realm of video and images. By utilizing the inherent parallel structures and computation possible in an FPGA, algorithmic speed is increased dramatically. The birth of the AHA-HSMC daughter card combines the abilities of two giants in the FPGA industry and the image processing industry: Altera Corporation and Aptina Imaging Corporation.

The AHA-HSMC is Terasic Technologies' daughter card solution for sensors from Aptina Imaging Corporation. The AHA-HSMC makes it possible for users with High Speed Mezzanine Connector (HSMC) ports to connect Aptina image sensors to Altera FPGA development kits.

1.1 Features

Figure 1-1 shows a photograph of the AHA-HSMC Daughter Card.

Figure 1-1 Layout of the AHA-HSMC card

The key features of the card are listed below:

- Supports I2C configuration for Aptina sensor
- Support for standard Aptina parallel interface
- Support for Altera HSMC interface
- Shutter control function for Aptina Sensor

1.2 About the KIT

The AHA-HSMC kit will come with the following contents:

- AHA-HSMC Daughter Card
- System CD-ROM

The system CD contains technical documents of the AHA-HSMC daughter card, which includes components datasheet, reference designs, demonstrations, schematics, cable and user manual (this manual).

Figure 1-2 shows the photograph of the AHA-HSMC kit content.

Figure 1-2 AHA-HSMC kit package contents

1.3 Getting Help

Here is information of how to get help if you encounter any problem:

- Terasic Technologies
- Tel: +886-3-550-8800
- Email: support@terasic.com

Chapter 2

AHA-HSMC Card Architecture

This chapter provides information about architecture and block diagram of the AHA-HSMC card.

2.1 Layout and Components

The picture of the AHA-HSMC card is shown in **Figure 2-1** and **Figure 2-2**. It depicts the layout of the board and indicates the locations of the connectors and key components.

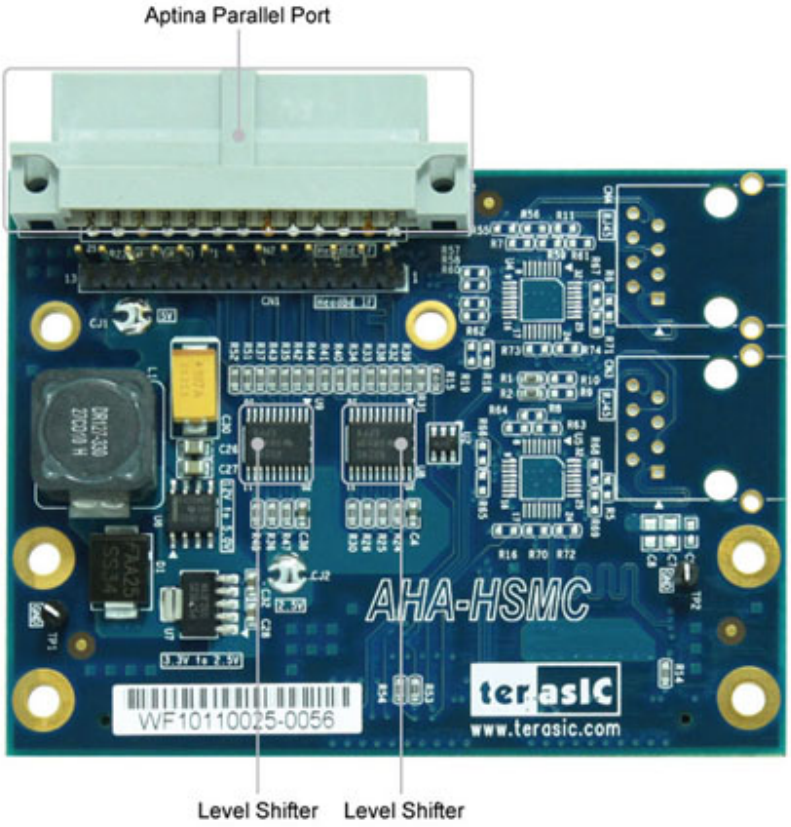

Figure 2-1 The AHA-HSMC Card PCB and component diagram (top view)

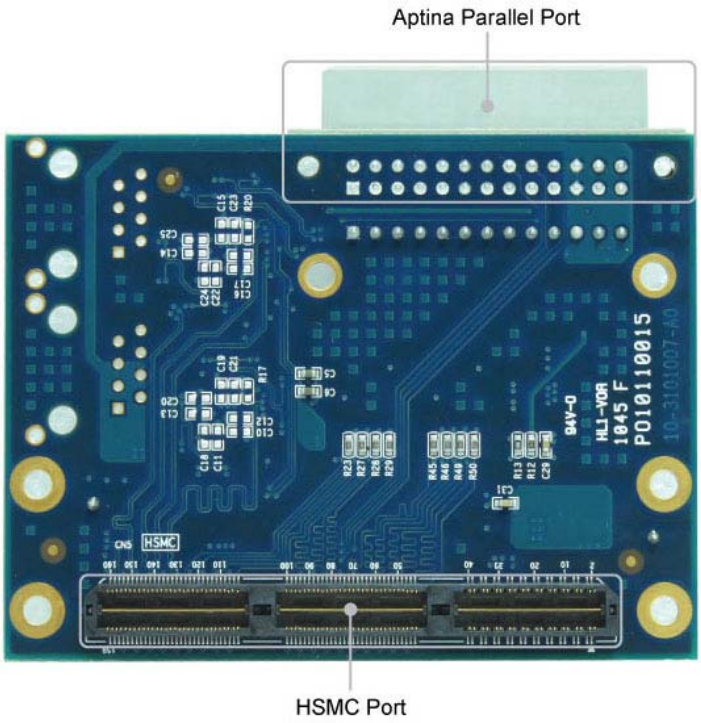

Figure 2-2 The AHA-HSMC Card PCB and component diagram (bottom view)

2.2 Block Diagram of the AHA Board

Figure 2-3 shows the block diagram of the AHA-HSMC card. The HSMC connector is housing all the wires from peripheral interfaces and makes direct connection to FPGA on the main board.

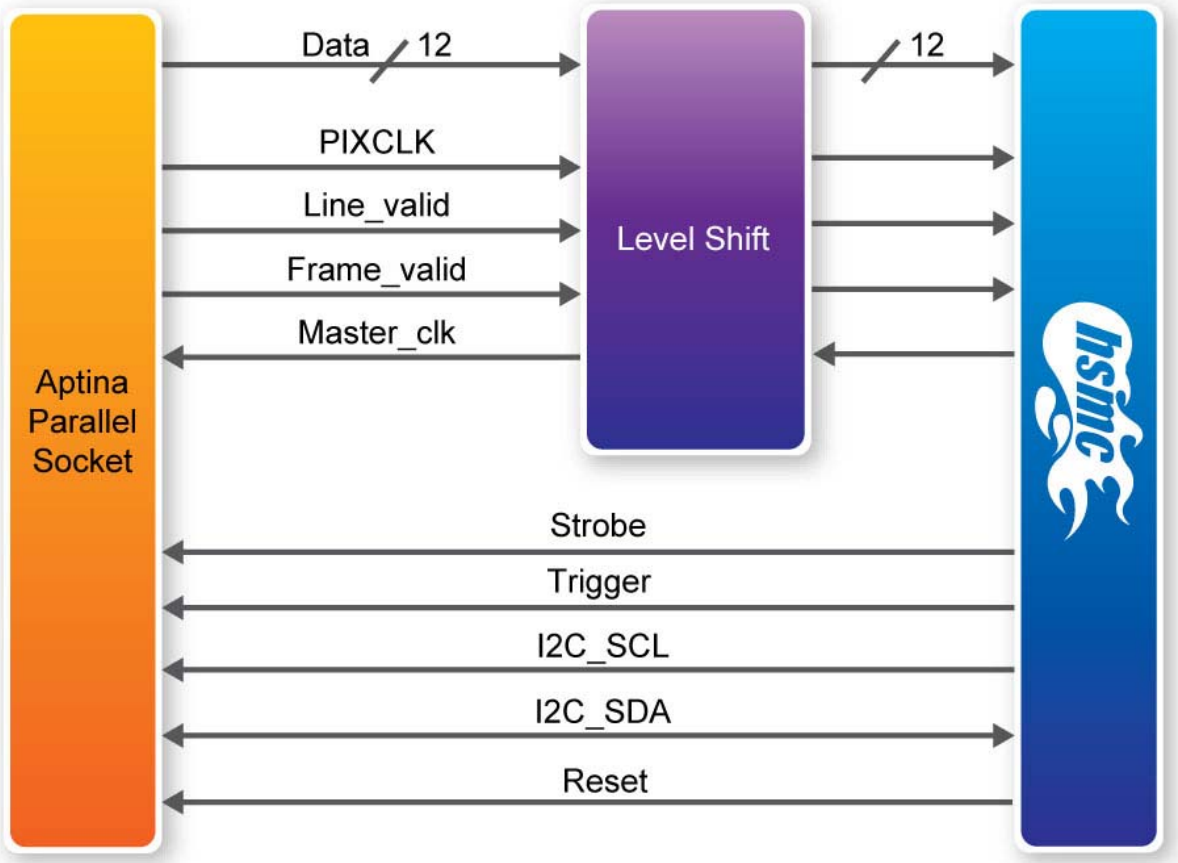

Figure 2-3 Block Diagram of AHA-HSMC card

Chapter 3

Board Components

3.1 HSMC Expansion Connector

The HSMC interface provides a mechanism to extend the peripheral set of an FPGA host board by means of a mezzanine card, which can address today's high speed signaling requirement as well as standard or legacy low-speed device interface support. Table 3-1

lists the pin assignments of the HSMC connector.

Table 3-1 Pin assignments and descriptions on HSMC connector

Pin Numbers	*Name*	*Direction*	*Description*
1-41	-		-
42	IMG_IN_FV	Input	Frame valid
43	CK_FPGA_MCLK	Output	External clock for sensor
44	-	-	-
45	VCC3P3	Power	Power 3.3V
46	VCC12	Power	Power 12V
47	-	-	-
48	IMG_IN_LV	Input	Line valid
49	-	-	-
50	-	-	-
51	VCC3P3	Power	Power 3.3V
52	VCC12	Power	Power 12V
53	-	-	-
54	IMG_DIN3	Input	Pixel data
55	-	-	-
56	-	-	-
57	VCC3P3	Power	Power 3.3V
58	VCC12	Power	Power 12V
59	-	-	-
60	IMG_DIN2	Input	Pixel data

61	SENSOR_RST	Output	sensor reset
62	-	-	-
63	VCC3P3	Power	Power 3.3V
64	VCC12	Power	Power 12V
65	-	-	-
66	IMG_DIN11	Input	Pixel data (MSB)
67	SHUTTER	Output	Shutter
68	-	-	-
69	VCC3P3	Power	Power 3.3V
70	VCC12	Power	Power 12V
71	-	-	-
72	IMG_DIN10	Input	Pixel data
73	DEMO2_I2C_SCL	Output	Serial clock
74	-	-	-
75	VCC3P3	Power	Power 3.3V
76	VCC12	Power	Power 12V
77	-	-	-
78	IMG_DIN9	Input	Pixel data
79	DEMO2_I2C_SDA	Input/Output	Serial data
80	-	-	-
81	VCC3P3	Power	Power 3.3V
82	VCC12	Power	Power 12V
83	-	-	-
84	IMG_DIN8	Input	Pixel data
85	BUF_HISPI_CLK0_EN	Output	LVDS outputs enable
86	-	-	-
87	VCC3P3	Power	Power 3.3V
88	VCC12	Power	Power 12V
89	-	-	-
90	IMG_DIN7	Input	Pixel data
91	BUF_HISPI_DATA0_EN	Output	LVDS outputs enable
92	-	-	-
93	VCC3P3	Power	Power 3.3V
94	VCC12	Power	Power 12V
95	-	-	-
96	CK_IMG_IN_PIXCLK	Input	Pixel clock
97	-	-	-
98	-	-	-
99	VCC3P3	Power	Power 3.3V
100	VCC12	Power	Power 12V
101	-	-	-
102	IMG_DIN6	Input	Pixel data
103	BUF_HISPI_DATA1_EN	Output	LVDS outputs enable
104	-	-	-
105	VCC3P3	Power	Power 3.3V

106	VCC12	Power	Power 12V
107	-	-	-
108	IMG_DIN5	Input	Pixel data
109	BUF_HISPI_DATA2_EN	Output	LVDS outputs enable
110	-	-	-
111	VCC3P3	Power	Power 3.3V
112	VCC12	Power	Power 12V
113	-	-	-
114	IMG_DIN4	Input	Pixel data
115	BUF_HISPI_DATA3_EN	Output	LVDS outputs enable
116	-	-	-
117	VCC3P3	Power	Power 3.3V
118	VCC12	Power	Power 12V
119	-	-	-
120	IMG_DIN1	Input	Pixel data
121	-	-	-
122	-	-	-
123	VCC3P3	Power	Power 3.3V
124	VCC12	Power	Power 12V
125	-	-	-
126	IMG_DIN0	Input	Pixel data
127	-	-	-
128	-	-	-
129	VCC3P3	Power	Power 3.3V
130	VCC12	Power	Power 12V
131	-	-	-
132	LVDS_DATA0_P	Input	HISPI serial data differential P
133	-	-	-
134	LVDS_DATA0_N	Input	HISPI serial data differential N
135	VCC3P3	Power	Power 3.3V
136	VCC12	Power	Power 12V
137	-	-	-
138	LVDS_DATA2_P	Input	HISPI serial data differential P
139	-	-	-
140	LVDS_DATA2_N	Input	HISPI serial data differential N
141	VCC3P3	Power	Power 3.3V
142	VCC12	Power	Power 12V
143	-	-	-
144	LVDS_DATA3_P	Input	HISPI serial data differential P
145	-	-	-
146	LVDS_DATA3_N	Input	HISPI serial data differential N
147	VCC3P3	Power	Power 3.3V
148	VCC12	Power	Power 12V
149	-	-	-
150	LVDS_DATA1_P	Input	HISPI serial data differential P

151	-	-	-
152	LVDS_DATA1_N	Input	HISPI serial data differential N
153	VCC3P3	Power	Power 3.3V
154	VCC12	Power	Power 12V
155	-	-	-
156	CK_LVDS_CLK0_P	Input	HISPI serial clock differential P
157	-	-	-
158	CK_LVDS_CLK0_N	Input	HISPI serial clock differential N
159	VCC3P3	Power	Power 3.3V
160	GND	Power	Power Ground

3.2 Aptina Parallel Port Interface

This section describes the Aptina Parallel Port interface on the AHA-HSMC.

The AHA-HSMC contains an Aptina Parallel Port interface with a 26-pin header and a 13-pin header. The 26-pin header is the main connector that connects with Aptina image sensor headboard. This header includes most of the control and data bus of the Aptina image sensor, and also provides 5V power to the Aptina image sensor headboard. The 13-pin header contains two sets of pixel data and one shutter control signal. All these signals on Aptina Parallel port are connected to HSMC connector via two level shift chips for logic-level transformation. **Table 3-2** and **Table 3-3** list the pin assignments of the 26-pin and 13-pin header of Aptina Parallel port, respectively.

Table 3-2 Pin assignments and descriptions for 26-pin header (Aptina Parallel)

Pin Numbers	*Name*	*Direction*	*Description*
1	SENSOR_D4	Output	Pixel data
2	SENSOR_D5	Output	Pixel data
3	SENSOR_D6	Output	Pixel data
4	SENSOR_D7	Output	Pixel data
5	SENSOR_D8	Output	Pixel data
6	SENSOR_D9	Output	Pixel data
7	SENSOR_D10	Output	Pixel data
8	SENSOR_D11	Output	Pixel data(MSB)
9	SENSOR_D2	Output	Pixel data
10	SENSOR_D3	Output	Pixel data
11	GND	Power	Power GND
12	GND	Power	Power GND
13	SENSOR_LV	Output	Line valid
14	-	-	-
15	-	-	-
16	SENSOR_RST	Input	Sensor Reset
17	SENSOR_FV	Output	Frame valid

18	SENSOR_SDA	Input/Output	Serial data
19	SENSOR_SCL	Input	Serial clock
20	-	-	-
21	VCC	Power	Power 5V
22	VCC	Power	Power 5V
23	CK_SENSOR_PIX	Output	Pixel clock
24	GND	Power	Power GND
25	GND	Power	Power GND
26	CK_DEMO2	Power	External clock for sensor

Table 3-3 Pin assignments and descriptions for 13-pin header (Aptina Parallel)

Pin Numbers	*Name*	*Direction*	*Description*
1	SENSOR_D0	Output	Pixel data
2	SENSOR_D1	Output	Pixel data
3-10	-	-	-
11	SHUTTER	Input	Shutter
12	-	-	-
13	GND	Power	Power GND

Chapter 4

Demonstrations

This chapter shows how to control and retrieve video frames from an Aptina sensor headboard and drive a display device to show the retrieved video. The demonstration requires the following hardware:

- FPGA Main Board with HSMC interface
- Terasic AHA-HSMC daughter card
- Aptina image sensor headboard
- LCD Display

In the demonstration, Aptina MT9M023 headboard is used. If users use other Aptina image sensor headboards, users will need to modify the design code by themselves for the demonstration to work.

4.1 Design Concept

The reference design is developed based on Altera Video and Image Processing Suite (VIP). A custom Camera VIP, provided by Terasic, is designed to retrieve raw image data from the image sensor and decode the raw data to RGB data.

Before the FPGA can retrieve the raw data, the image sensor should be configured. In this demonstration, the FPGA configure the registers in the image sensor through an I2C interface. The configure items include: display area, PLL, and gain. Please note: the registers control is sensor type dependent. Users need to refer the register data sheet provided by Aptina for register control.

The Camera VIP is a custom VIP-based on Altera VIP and Streaming specifications. It provides the following processes:

- Decode Frame-valid, Line-valid and Data-valid to retrieve video raw data - Bayer Pattern
- Translate Bayer Pattern to RGB Data
- Streaming RGB based on Altera VIP and Streaming Specification

Figure 4-1 shows the system generic block diagram of demonstration reference design.

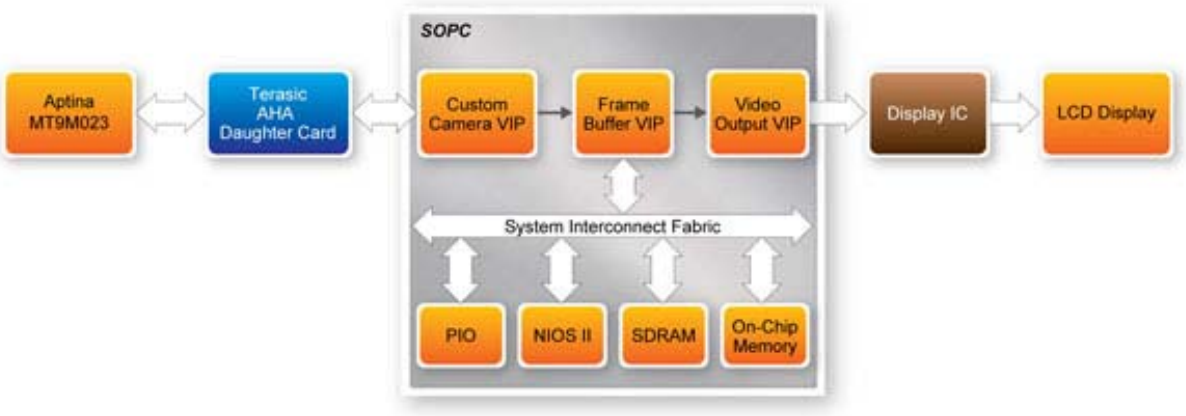

Figure 4-1 System Block Diagram of Aptina headboard Demonstration

4.2 Demonstration for Altera DE2-115 FPGA Board

This section shows how to setup the video demo on the Altera DE2-115 using camera resolution 800x600.

System Requirements

- Altera DE2-115 FPGA Board and USB Cable
- Terasic AHA-HSMC Daughter Card
- CMOS Image Sensor Headboard (MT9M023)
- VGA Display and VGA Cable

Hardware Setup

Figure 4-2 shows the hardware setup for Aptina headboard demonstration with DE2-115 FPGA board.

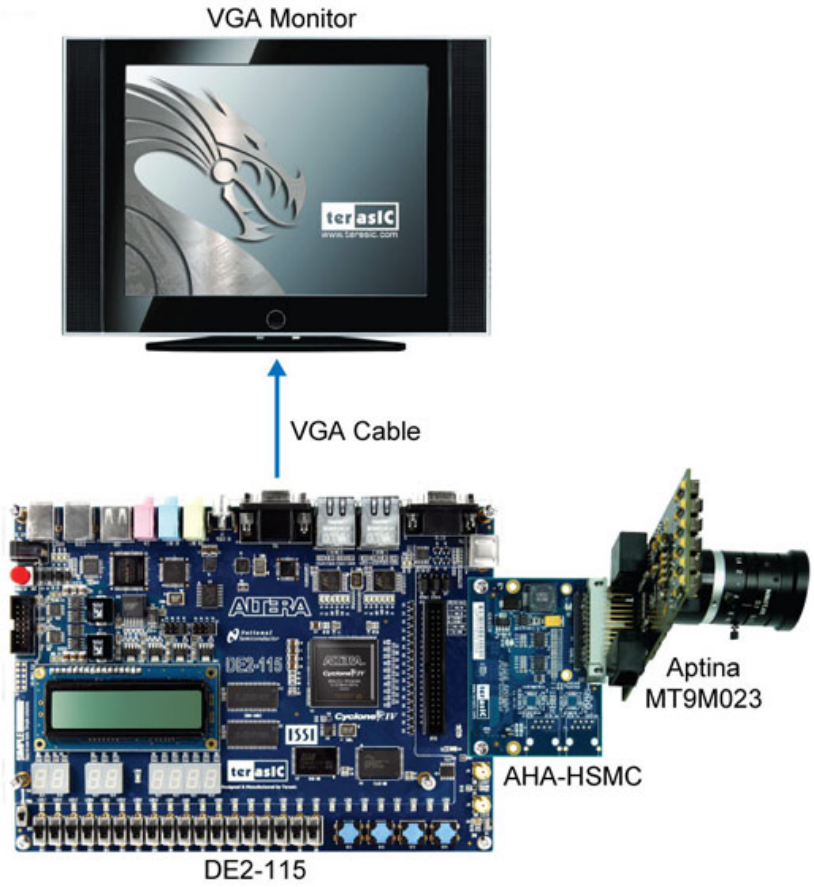

Figure 4-2 Aptina image sensor demonstration hardware setup with DE2-115

Demonstration Setup

1. Make sure the DE2-115 is powered off.
2. Mount the AHA-HSMC daughter card onto the DE2-115 HSMC connector.
3. Plug the Aptina headboard (MT9M023) to AHA-HSMC's parallel connector.

4. Connect VGA display and the DE2-115 VGA port with a VGA cable.
5. Connect the DE2-115 USB-Blaster USB-B port to the PC USB Port with a USB Cable.
6. Connect the power supply to the DE2-115 and turn on the DE2-115.
7. Make sure Quartus 10.1 and NIOS II 10.1 are installed on your system.
8. Copy the folder DE2-115-AHA-HSMC\demo_batch in the AHA-HSMC System CD onto your system and execute “test.bat”.
9. Now, you will see a video display on your VGA monitor. Users can adjust the aperture and focal length of the lens module mount on the Aptina headboard.

Demonstration Source Code

The source code of this demonstration is located in the following directory of the System CD.
Project directory: Demonstration\DE2_115_AHA

Note. The project is built by Quartus 10.1, and Altera VIP license is required.

4.3 Demonstration for Cyclone III Development Board

This section shows how to setup the video demo on the Altera Cyclone III Development Board. Two demo projects are included using camera resolution of 800x600 and 720p.

System Requirements

- Altera Cyclone III Development Board and USB Cable
- Terasic AHA-HSMC Daughter Card
- CMOS Image Sensor (MT9M023)
- DVI-HSMC Daughter Card
- DVI Display and DVI Cable

Hardware Setup

Figure 4-3 shows the hardware setup for Aptina headboard demonstration with Cyclone III development board.

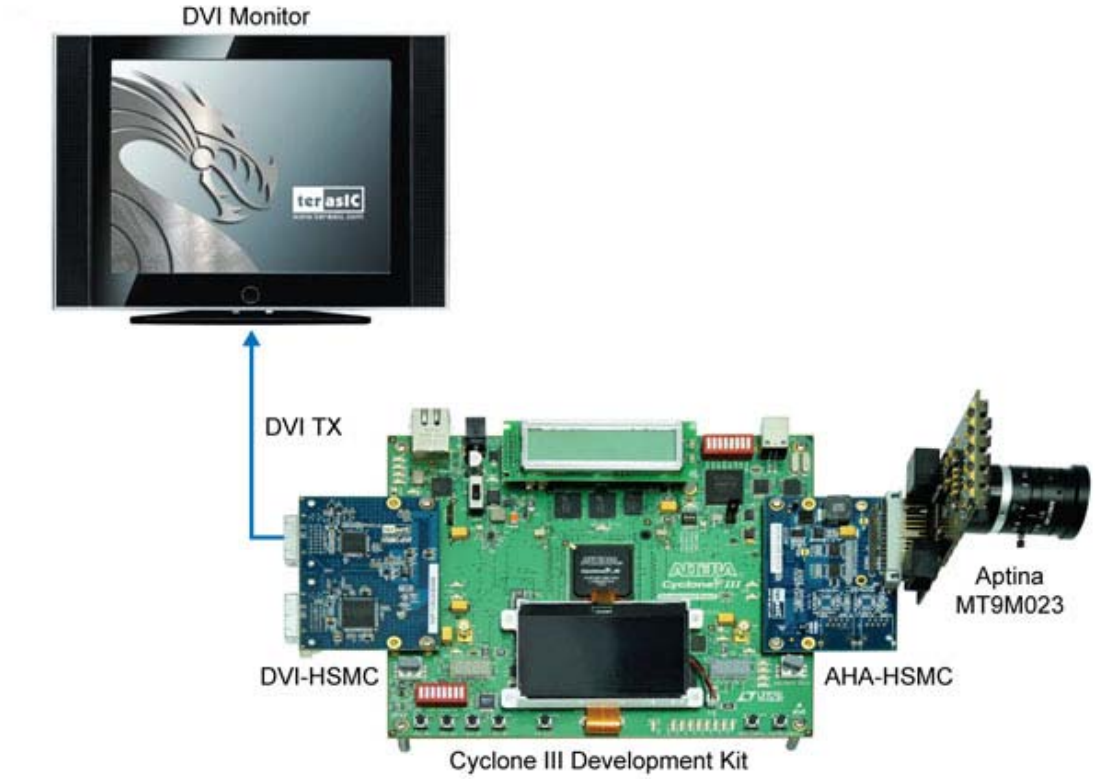

Figure 4-3 Aptina image sensor demonstration hardware setup with Cyclone III development board

Demonstration Setup

1. Make sure the Cyclone III development board is powered off.
2. Mount the AHA-HSMC daughter card onto the Cyclone III development board HSMC B connector.
3. Mount the DVI daughter card onto the Cyclone III development board HSMC A connector.
4. Plug the Aptina headboard (MT9M023) to AHA-HSMC's parallel connector.
5. Connect DVI display and the DVI daughter card TX port with a DVI cable.

6. Connect the Cyclone III development board USB-Blaster port to the PC USB Port with a USB Cable.
7. Connect the power supply to the Cyclone III development board and turn it on.
8. Make sure Quartus 10.1 and NIOS II 10.1 are installed on your system.
9. Copy the folder C3H-AHA\demo_batch in the AHA-HSMC System CD onto your system and execute “test.bat”.
10. Now, you will see a video display on your DVI monitor. Users can adjust the aperture and focal length of the lens module mount on the Aptina headboard.

Demonstration Source Code

The source code of this demonstration is located in the following directory of the System CD.
Project directory: Demonstration\C3H_AHA_800x600 and Demonstration\C3H_AHA_720p

Note. The project is built by Quartus 10.1, and Altera VIP license is required.

Chapter 5

Appendix

5.1 Revision History

Version	*Change Log*
V1.0	**Initial Version (Preliminary)**

5.2 Copyright Statement

Always visit AHA-HSMC webpage for new applications.

We will be continuing providing interesting examples and labs on our AHA-HSMC webpage. Please visit www.altera.com or aha.terasic.com for more information.

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