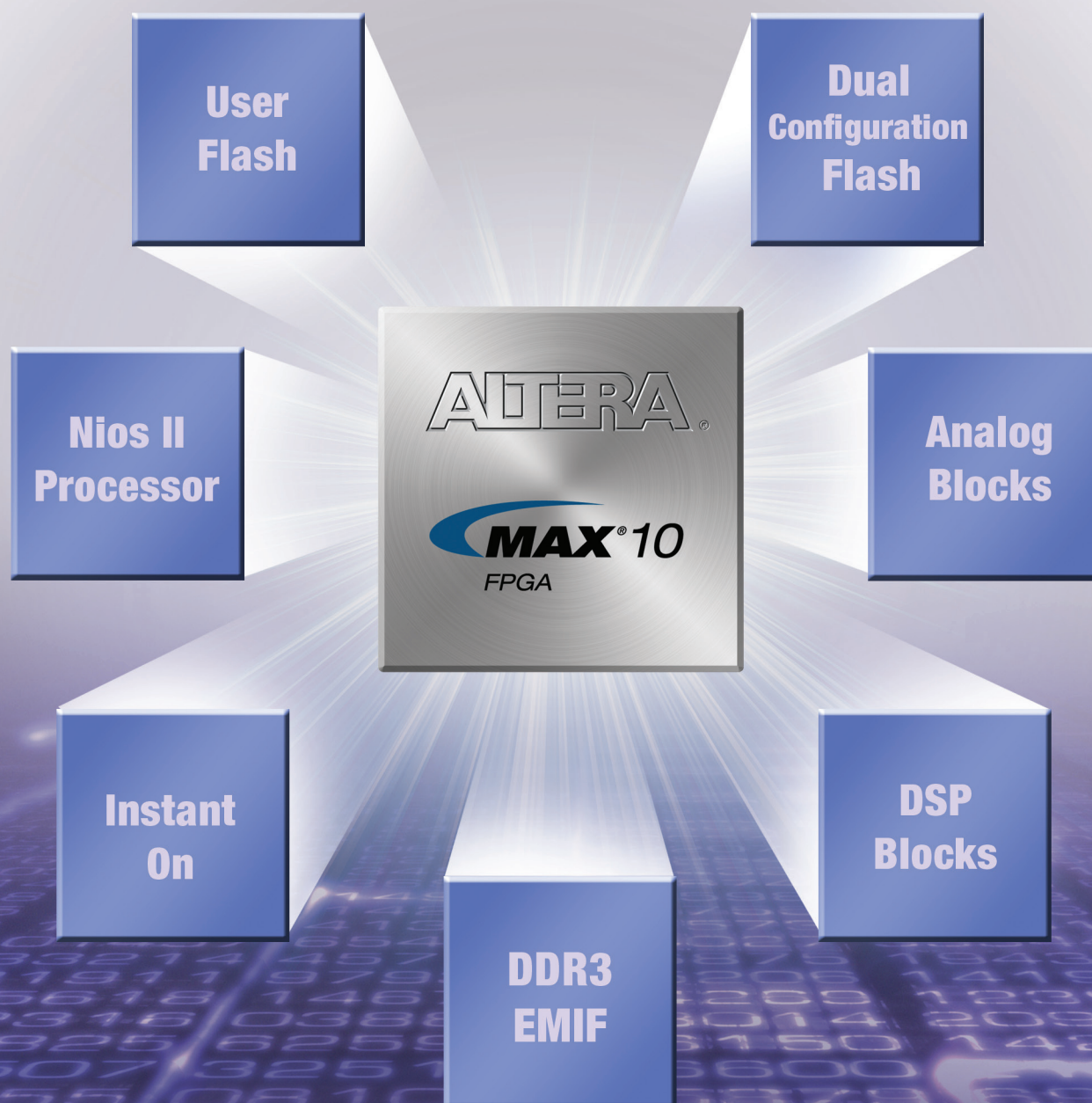


**REVOLUTIONIZING NON-VOLATILE INTEGRATION**



## Family Overview

Altera's MAX<sup>®</sup> 10 FPGAs revolutionize non-volatile integration by delivering advanced processing capabilities in a low-cost, single chip small form factor programmable logic device. Building upon the single chip heritage of previous MAX device families, densities range from 2K – 50KLE, using either single or dual power supplies. The MAX 10 FPGA family encompasses both small packaging and high I/O pin count packages.

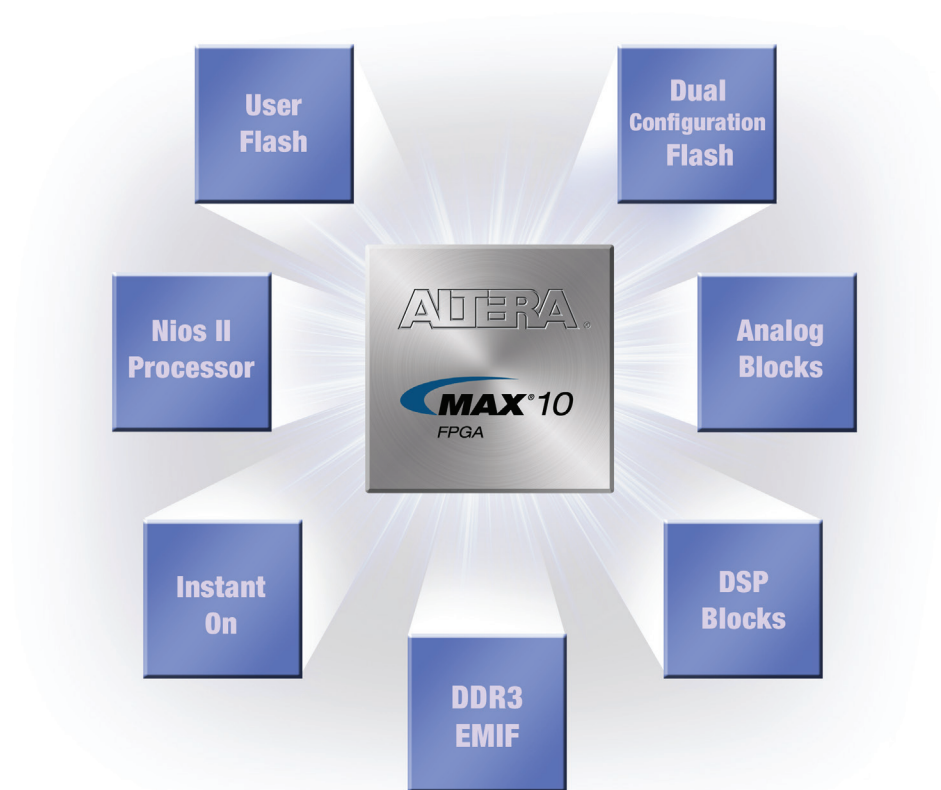
MAX 10 FPGAs are built on TSMC's 55 nm embedded NOR flash technology, enabling instant-on functionality. MAX 10 FPGAs include integrated analog-to-digital converters (ADCs) and dual configuration flash allowing you to store and dynamically switch between two images on a single chip. Unlike CPLDs, MAX10 FPGAs also include full featured FPGA capabilities such as Nios<sup>®</sup> II soft core embedded processor support, DSP blocks, and soft DDR3 memory controllers.

For Industrial and Automotive systems, the MAX 10 FPGA single-chip integration, including Nios II processor support, provide a reduced footprint with increased design security and product reliability while lowering system cost.

For control applications in computing, consumer, communications, and other markets, MAX 10 FPGAs ADC functionality allows integration of power-up sequencing and system control circuitry into a single device. The software-based system management using the Nios II processor further enhances board management integration in an advanced, reliable system controller.

## Device Family Details

The features highlighted in the figure below enable system simplification, increased capabilities, and single-chip integration benefits.



## Key Features

- Up to 50,000 logic elements (LEs)
- Maximum of 500 user I/O pins
- Non-volatile instant-on architecture
- Single chip
- Embedded SRAM
- High-performance phase-locked loops (PLLs)
- External memory interface (DDR3 SDRAM/DDR3L SDRAM/DDR2 SDRAM/LPDDR2)
- Nios II embedded processor support
- DSP blocks
- 3.3 V, LVDS, PCI™, and 30+ other I/O standards supported
- Embedded ADCs – 12 bit 1 Msps
  - Up to 18 analog input channels
  - Temperature sensor
- Single or dual-core voltage supply offering
- Embedded flash
  - Dual configuration flash
  - User flash memory
- Internal oscillator
- Power Saving Features
  - Sleep mode to reduce dynamic power by up to 95%
  - Input buffer power-down
- 128 bit Advanced Encryption Standard (AES) design security
- RoHS6 packaging

## MAX 10 FPGAs Product Table

Product Line	10M02	10M04	10M08	10M16	10M25	10M40	10M50
LEs (K)	2	4	8	16	25	40	50
Block memory (Kb)	108	189	378	549	675	1,260	1,638
User flash memory <sup>1</sup> (KB)	12	16 – 156	32 – 172	32 – 296	32 – 400	64 – 736	64 – 736
18 x 18 multipliers	16	20	24	45	55	125	144
PLLs <sup>2</sup>	1, 2	1, 2	1, 2	1, 4	1, 4	1, 4	1, 4
Internal configuration	Single	Dual	Dual	Dual	Dual	Dual	Dual
Analog-to-digital converter (ADC), temperature sensing diode (TSD) <sup>3</sup>	-	1, 1	1, 1	1, 1	2, 1	2, 1	2, 1
External memory interface (EMIF)	Yes <sup>4</sup>	Yes <sup>4</sup>	Yes <sup>4</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>	Yes <sup>5</sup>
Package Options and I/O Pins: Feature Set Options, GPIO, True LVDS Transceiver/Receiver							
V36 (D) <sup>6</sup>	WLCSP (3 mm, 0.4 mm pitch)	C, 27, 3/7	—	—	—	—	—
V81 (D) <sup>7</sup>	WLCSP (4 mm, 0.4 mm pitch)	—	—	C/F, 56, 7/17	—	—	—
F256 (D)	FBGA (17 mm, 1.0 mm pitch)	—	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54	C/A, 178, 13/54
U324 (D)	UBGA (15 mm, 0.8 mm pitch)	C, 160, 9/47	C/A, 246, 15/81	C/A, 246, 15/81	C/A, 246, 15/81	—	—
F484 (D)	FBGA (23 mm, 1.0 mm pitch)	—	—	C/A, 250, 15/83	C/A, 320, 22/116	C/A, 360, 24/136	C/A, 360, 24/136
F672 (D)	FBGA (27 mm, 1.0 mm pitch)	—	—	—	—	—	C/A, 500, 30/192
E144 (S) <sup>6</sup>	EQFP (22 mm, 0.5 mm pitch)	C, 101, 7/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/27	C/A, 101, 10/28	C/A, 101, 10/28
M153 (S)	MBGA (8 mm, 0.5 mm pitch) <sup>8</sup>	C, 112, 9/29	C/A, 112, 9/29	C/A, 112, 9/29	—	—	—
U169 (S)	UBGA (11 mm, 0.8 mm pitch)	C, 130, 9/38	C/A, 130, 9/38	C/A, 130, 9/38	—	—	—

### Notes:

1. Additional user flash may be available, depending on configuration options.
2. The number of PLLs available is dependent on the package option.
3. Availability of the ADC or TSD varies by package type. Smaller pin-count packages do not have access to the ADC hard IP.
4. SRAM only.
5. SRAM, DDR3 SDRAM, DDR2 SDRAM, or LPDDR2.
6. "D" = Dual power supply (1.2 V/2.5 V), "S" = Single power supply (3.3 V or 3.0 V).
7. V81 package does not support analog feature set. 10M08 V81 F devices support dual image with RSU.
8. "Easy PCB" utilizes 0.8 mm PCB design rules.
9. All data is correct at the time of printing, and may be subject to change without prior notice. For the latest information, please visit [www.altera.com](http://www.altera.com).

C, 27, 3/7

Indicates feature set options, GPIO count, and LVDS transmitter or receiver count. Feature set options: C = Compact (single image), F = Flash (dual image with RSU), A = Analog (analog features block). Each has added premiums.

— Indicates pin migration.

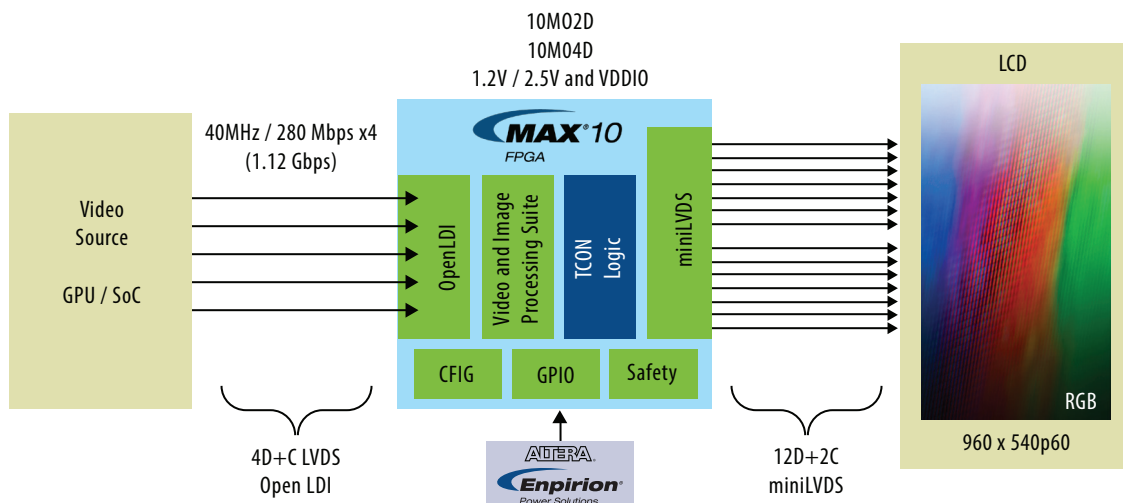
## Qualification and Certification

MAX 10 FPGAs are available in Commercial, Industrial, and Automotive (AEC-Q100) temperature grades. In addition, they will be supported in a future release of the functional safety pack, TUV Certified to IEC 61508 and ISO 26262, reducing development time and time to market.

## Market Solutions

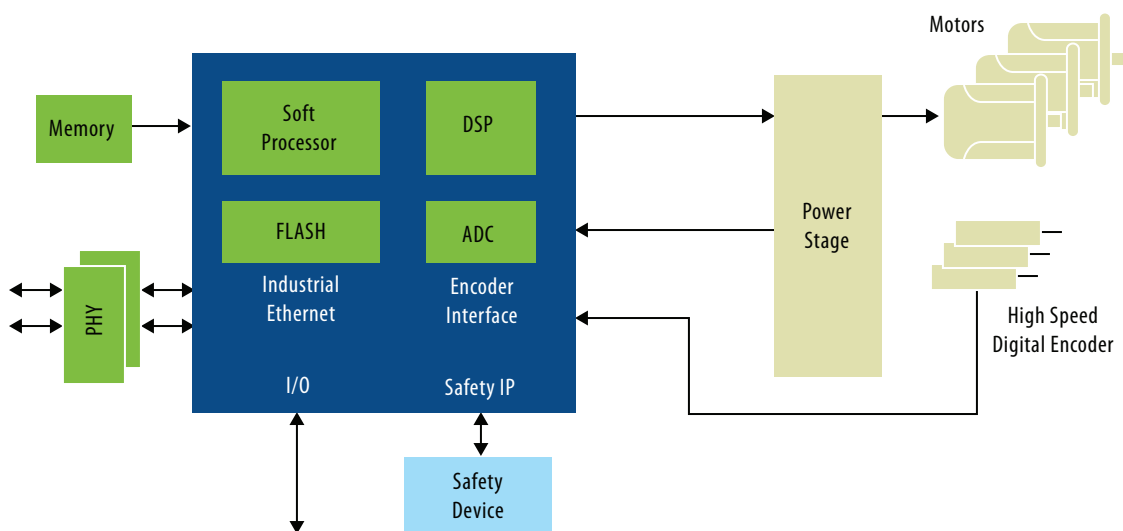
MAX 10 FPGAs serve many end market segments and enable a wide variety of applications.

### Automotive Infotainment



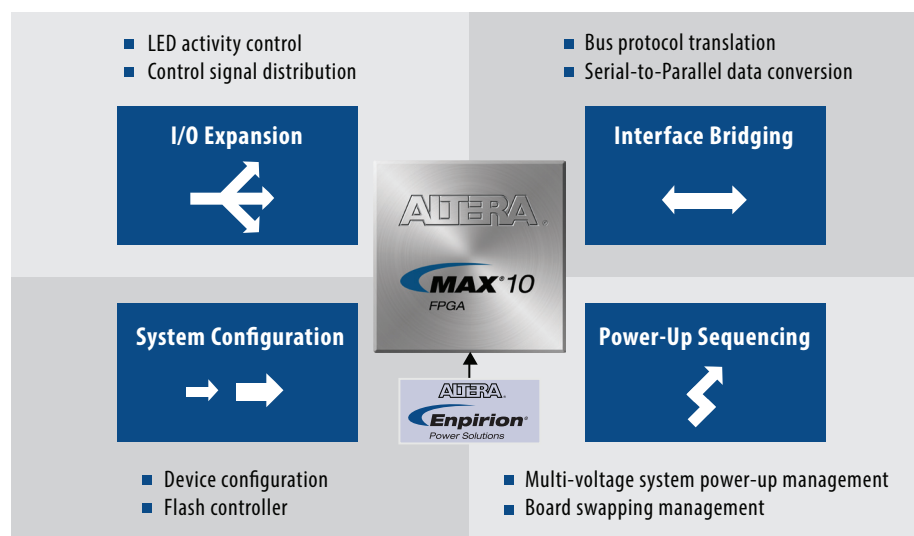
- I/O support flexibility - LVDS inputs, mini-LVDS outputs, and LVCMOS general-purpose input and output pins (GPIOs)
- Altera® intellectual property (IP) - ALT LVDS megafunction and Video and Image Processing Suite
- MAX 10 FPGA integration - Granular family offering to meet unique design needs and on-chip flash for reduced BOM

### Industrial Motor Control



- Higher-performance - High control loop update for high-speed motors and direct non-PWM control with parallel processing for precise timing
- Greater flexibility - High I/O counts, internal ADC, custom IP, and tailored resource usage to meet performance requirements
- Lower cost of ownership - Lower part count brings long design lifetime, matched by Altera's long supply lifetime

## System Management Applications



- System management – Power-up sequencing, temperature measurement
- Interface bridging – Translate bus protocol and voltages between incompatible devices
- I/O expansion – Increase the available I/O pins of standard devices

## Low-Cost Development Kit Solutions

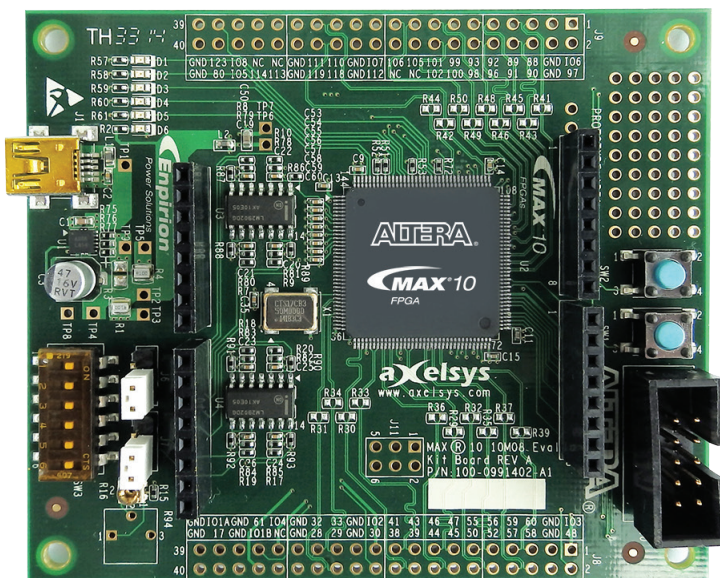
The MAX 10 FPGA evaluation and development kits feature **Altera Enpirion®** power products and PowerSoCs and can be ordered on [www.altera.com/max10](http://www.altera.com/max10) to get your next design up and running as quickly as possible.

With Arduino, PMOD and high-speed mezzanine card (HSMC) headers, both boards support a wealth of daughtercards from 3rd party vendors, such as Arduino ([www.arduino.cc](http://www.arduino.cc)), Terasic ([www.terasic.com](http://www.terasic.com)), and SLS ([www.slscorp.com](http://www.slscorp.com)).



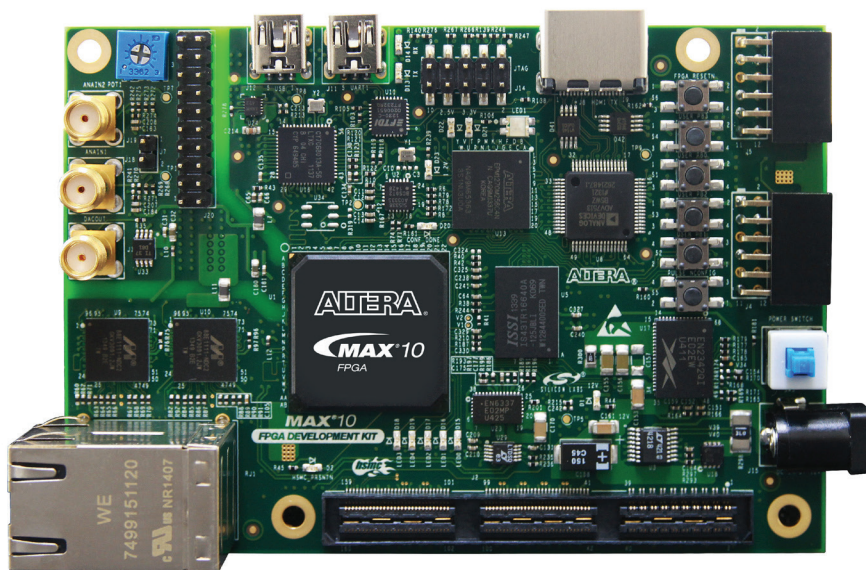
## MAX 10 FPGA 10M08 Evaluation Kit

MAX 10 FPGA Evaluation Kits Enable Fast Evaluation and Prototyping



## MAX 10 FPGA 10M50 Development Kit

MAX 10 FPGA Development Kits Provide a Platform for System-Level Development



## Getting Started

### Design Tools

Altera offers a range of design tools for MAX 10 FPGAs, including the free Quartus® Prime Design Software Web Edition, the Nios II Embedded Design Suite, and a host of analysis tools, including the Analog Toolkit, optimized to help get your design into production quickly.

### Powering MAX 10 FPGAs

Altera's Enpirion portfolio of power management products offers a broad selection of solutions ideally suited for powering the MAX 10 FPGA family. Together, Altera's MAX 10 FPGA with Enpirion power solutions enables the smallest, most reliable solution while minimizing cost and accelerating time to revenue. Designing a power tree for a MAX 10 FPGA is easy with Altera's suite of FPGA system design tools, such as Altera's PowerPlay Early Power Estimator tool, which seamlessly combines FPGA power consumption estimates with a recommended power tree with Enpirion power solutions. For more details and design support for creating the optimal MAX 10 FPGA power tree, please visit the [Powering FPGAs Resource Center](#).

## Want to Dig Deeper?

Get more details about our MAX 10 FPGA family by contacting your local Altera sales representative or FAE, or by visiting [www.altera.com/max10](http://www.altera.com/max10).



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<a href="#"><u>10M25DCF256C8G</u></a>	<a href="#"><u>10M16SCU169A7G</u></a>	<a href="#"><u>10M16SAU169C8G</u></a>	<a href="#"><u>10M08SAE144C8G</u></a>	<a href="#"><u>10M16SAE144C8G</u></a>