RM331x Series
32 - 256 Kbit Ultra-Low Power Non-volatile Serial Memory — SPI Bus

Advance Datasheet

Features

- Memory array: 32 - 256 Kbit EEPROM-compatible non-volatile serial memory
- Multiple supply voltages for minimum power consumption
  - VDDC-WR: 1.17 - 1.23V
  - VDDC-RD: 1.14 - 1.26V
  - VDDIO: 1.65 - 3.6V
- Serial peripheral interface (SPI) compatible
  - Supports SPI modes 0 and 3
- 1.0 MHz maximum clock rate
- Flexible Programming
  - Byte/Page Program (1 to 32 or 64Bytes)
  - Page size: 32 or 64 Bytes
- Hardware and Software Write Protection
- 128-byte OTP capability
- Ultra Low Energy Word Write
  - 32 bit Word Write consuming 50 nJ
- Low power consumption
  - 10 µA active Read current @ 500 kbit/s (Typical)
  - 10 µA active Write current @ 10 kbit/s (Typical)
  - 50 nA Ultra-Deep Power-Down current
- Auto Ultra-Deep Power-Down — Device can enter Ultra-Deep Power-Down automatically after finishing a Write operation
- Self-timed write cycles
- Hardware reset
- 8-lead 8S1 SOIC package
- RoHS-compliant and halogen-free packaging
- Data Retention: 10 years
- Industrial operating temperature: -40 °C to +85 °C
- Based on Adesto's proprietary CBRAM® technology

1. Description

The Adesto® RM331x Series is a 32 - 256 Kbit, serial memory device that utilizes Adesto's CBRAM® resistive technology.

The memory device is optimized for low power operation offering lowest available power for data-transfer, power-down, and writing. In order to efficiently optimize power consumption, the device makes use of two supplies V_{DDC}, and V_{DDIO}. The two V_{DDIO} supply signals must be tied together to supply write and I/O voltage (Figure 5-2). Read power is supplied from the V_{DDC} and the device consumes less than10 µW at 500 Kbit/s.

The RM331x Series is accessed through a 4-wire SPI interface consisting of a Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock (SCK), and Chip Select ($\overline{CS}$). The maximum clock (SCK) frequency in read mode is 1.0 MHz.

The device supports direct write eliminating the need to pre-erase. Writing into the device can be done from 1 to 32 or 64 bytes at a time and consumes less than 40 µW. All writing is internally self-timed.

The device has both Byte Word Write and Page Write capability. Page Write is from 1 to 32 or 64 bytes. The 32 bit word Write operation of CBRAM consumes only 10% of the energy consumed by a 32-bit word Write operation of EEPROM devices of similar size.

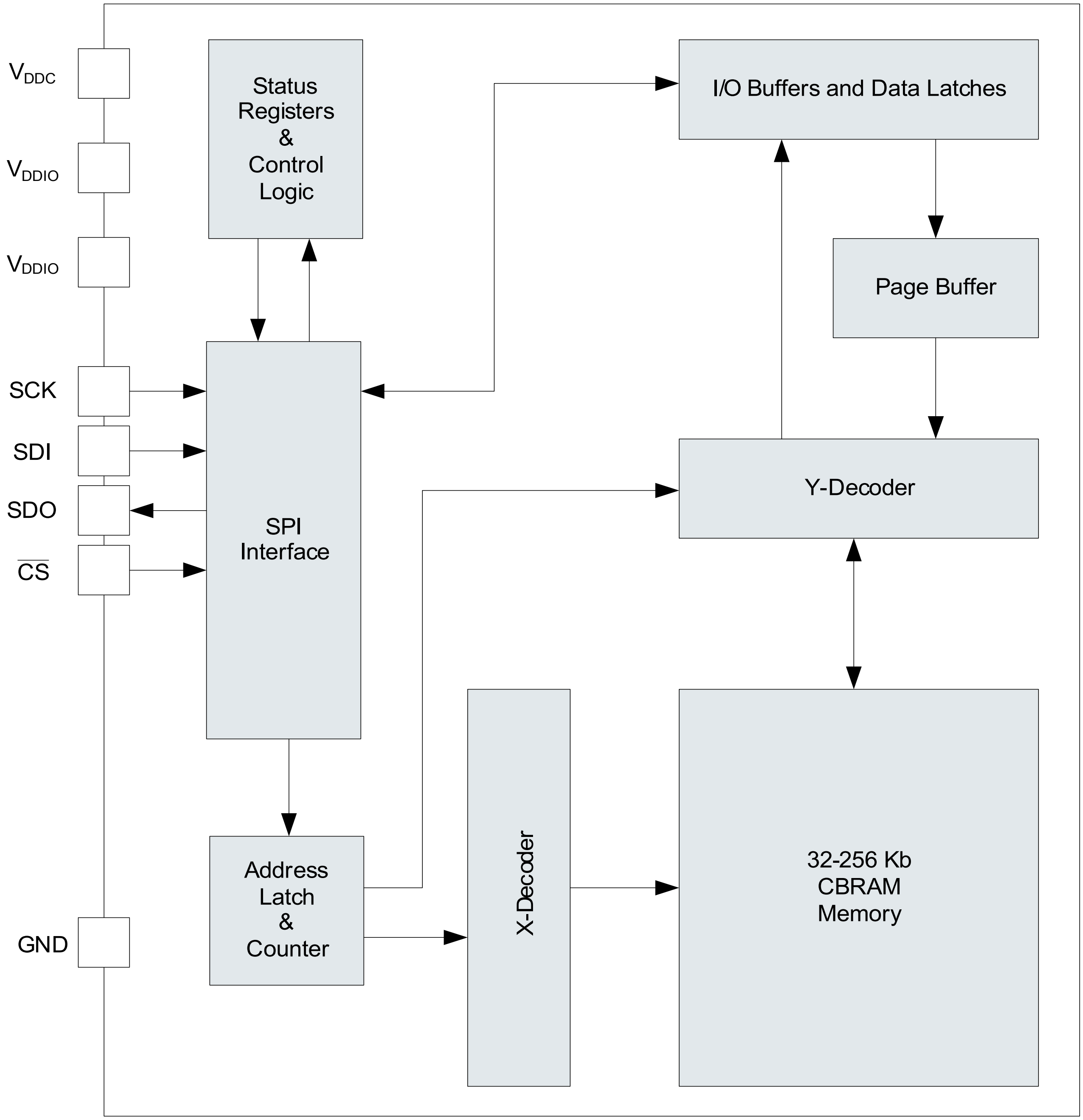
Both random and sequential reads are available. Sequential reads are capable of reading the entire memory in one operation.

The RM331x family contains the following memory and page sizes.

Product	Density	Page Size (bytes)
RM3316	256 Kbit	64
RM3315	128 Kbit	64
RM3314	64 Kbit	32
RM3313	32 Kbit	32

2. Block Diagram

Figure 2-1. Block Diagram



3. Electrical Specifications

3.1 Absolute Maximum Ratings

Table 3-1. Absolute Maximum Ratings (1)

Parameter	Specification
Operating ambient temp range	-40°C to +105°C
Storage temperature range	-65°C to +105°C
Input supply voltage, V_{DDC} to GND	- 0.3V to 1.45V(2)
Input supply voltage, V_{DDIO} to GND	- 0.3V to 3.6V
Voltage on any pin with respect to GND	-0.5V to (V_{DDIO} + 0.5V)
ESD protection on all pins (Human Body Model)	1 kV
Junction temperature	105 °C
DC output current	5 mA

(1). CAUTION: Stresses greater than Absolute Maximum Ratings may cause permanent damage to the devices. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in other sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may reduce device reliability.

(2). Part should not be operated above the 1.23V operating limit for write and 1.26V limit for read. The Hardware Reset command sequence should be applied after power up and the supply level is stable.

3.2 DC Operating Characteristics

Applicable over recommended operating range: T_A = -40°C to +85° C, V_{DDIO} = 1.65V - 3.6V, V_{DDC-WR} = 1.17V - 1.23V, V_{DDC-RD} = 1.14V - 1.26V, C = 3 pF (unless otherwise noted).

Table 3-2. DC Operating Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{DDC-WR}	Core Supply Range — Write (1)		1.17	1.20	1.23	V
V_{DDC-RD}	Core Supply Range — Read(1)		1.14	1.20	1.26	V
V_{DDIO}	I/O Supply Range (1) (2)		1.65	2.5	3.6	V
I_{DD1}	Supply Current, Read (3)	V_{DDC}= 1.2V @ 500 kbit/s		5.5		µA
		V_{DDIO}= 2.5V @ 500 kbit/s		4.5		µA
I_{DD2}	Supply Current, Standby	V_{DDC}= 1.2V		1.0	10.0	µA
		V_{DDIO}= 2.5V		1.0	10.0	µA
I_{DD3}	Supply Current, Write	V_{DDC}= 1.2V @ 10 kbit/s		4.5		µA
		V_{DDIO}= 2.5V @ 10 kbit/s		5.5		µA
I_{DD5}	Supply Current, Ultra-Deep Power-Down Mode 1	V_{DDC}= 1.2V		0.020		µA
		V_{DDIO}= 2.5V		0.05	0.50	µA

Table 3-2. DC Operating Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{IL}	Input Leakage	SCK, SDI, $\overline{CS}$ V_{IN} = 0V to V_{DDIO}			1	µA
I_{OL}	Output Leakage	SCK, SDI, $\overline{CS}$ = V_{DDIO} V_{IN} = 0V to V_{DDIO}			1	µA
V_{IL}	Input Low Voltage	SCK, SDI, $\overline{CS}$	-0.3		V_{DDIO} x0.3 0.3	V
V_{IH}	Input High Voltage	SCK, SDI, $\overline{CS}$	V_{DDIO} x0.7		V_{DDIO} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3.0 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 100 µA	V_{DDIO} x0.2			V

1. A low ESR 100nF capacitor should be connected between each supply pin and GND (see Figure 5-2).
2. There are no brownout or under voltage detectors. Users must ensure that VDDC and VDDIO are within operating range for correct operation of the device. After an under-voltage condition, memory contents will not be changed, but the Hardware Reset command sequence should be applied after powering back up and the supply level is stable.
3. Readings are averages for a series of one read after another; it is not the instantaneous peak current while making a single read.

3.3 AC Operating Characteristics

Applicable over recommended operating range: T_A = -40°C to +85° C, V_{DDIO} = 1.65V to 3.6V, V_{DDC-WR} = 1.17V to 1.23V, V_{DDC-RD} = 1.14V to 1.26V, C_L = 3pF (unless otherwise noted).

Table 3-3. AC Operating Characteristics

Symbol	Parameter	Min	Typ	Max	Units
f_{SCK}	SCK Clock Frequency for Read Mode			1	MHz
t_{SCK}	SCK Low Time	0.5			µs
t_{CS}	$\overline{CS}$ High Time	100			ns
t_{CL}	$\overline{CS}$ Low Time	100			ns
t_{CSS}	$\overline{CS}$ Setup Time	10			ns
t_{CSH}	$\overline{CS}$ Hold Time	10			ns
t_{DS}	Data In Setup Time	4			ns
t_{DH}	Data In Hold Time	4			ns
t_{OV}	Output Valid			15	ns
t_{OH}	Output Hold Time Normal Mode	0			ns
t_{DIS}	Output Disable Time			100	ns
t_{PW}	Page Write Cycle Time, 32/64 byte page		18/36		ms
t_{BP}	4 Byte Write Cycle Time		2.2		ms
t_{PUD}	V_{DDC} Power-up Delay (1)			200	µs

Table 3-3. AC Operating Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units
t_{XUDPD}	Exit Ultra-Deep Power-Down Time	200			µs
C_{IN}	SCK, SDI, $\overline{CS}$, V_{IN}= 0V			6	pF
C_{OUT}	SDO V_{IN} = 0V			3	pF
Endurance		10000			Write Cycles
Retention		10			Years

1. Note: There are no brownout or under voltage detectors. Users must ensure that V_{DDC} and V_{DDIO} are within operating range for correct operation of the device. V_{DDC} must be within range as depicted in Figure 4-2.

3.4 AC Test Conditions

Table 3-4. AC Test Conditions

AC Waveform	Timing Measurement Reference Level	
V_{LO} = 0.2V	Input	0.5 V_{DDIO}
V_{HI} = V_{DDIO} = 1.65V	Output	0.5 V_{DDIO}
C_L = 3pF (for max1.0 MHz SCK)		

4. Timing Diagrams

Figure 4-1. Synchronous Data Timing

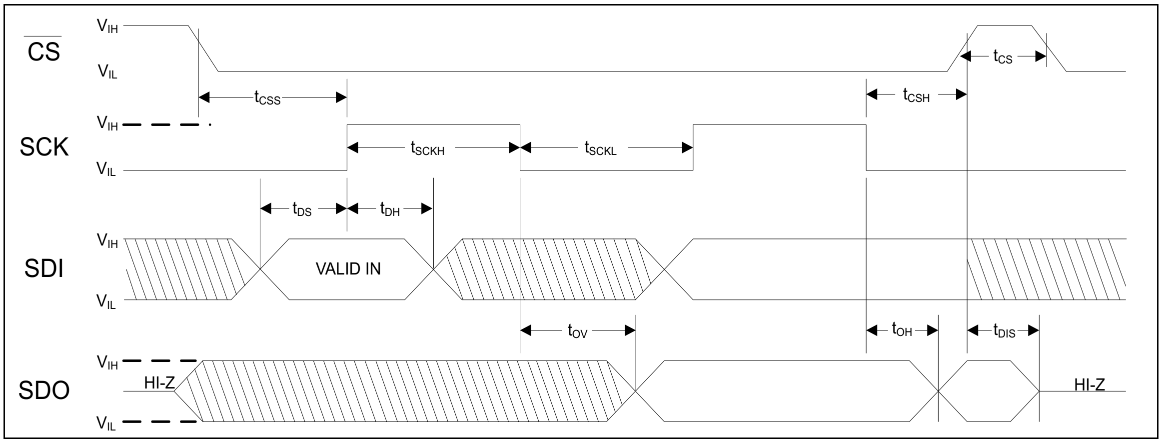
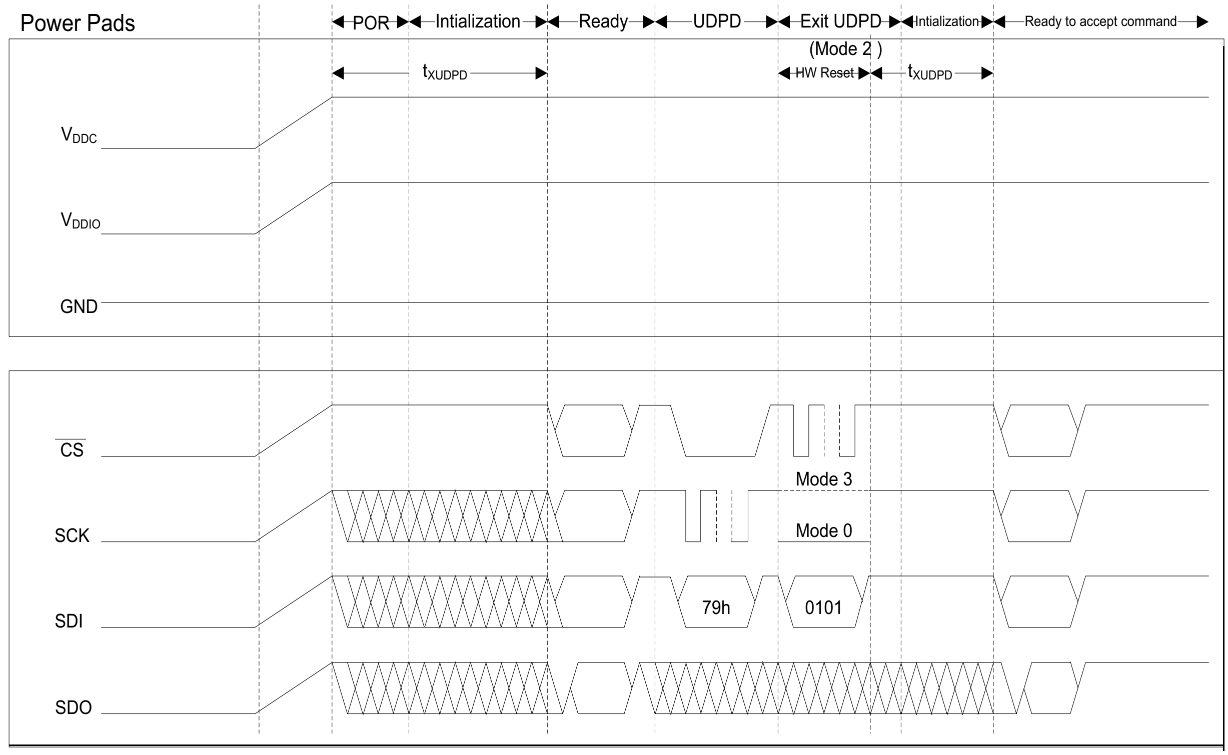
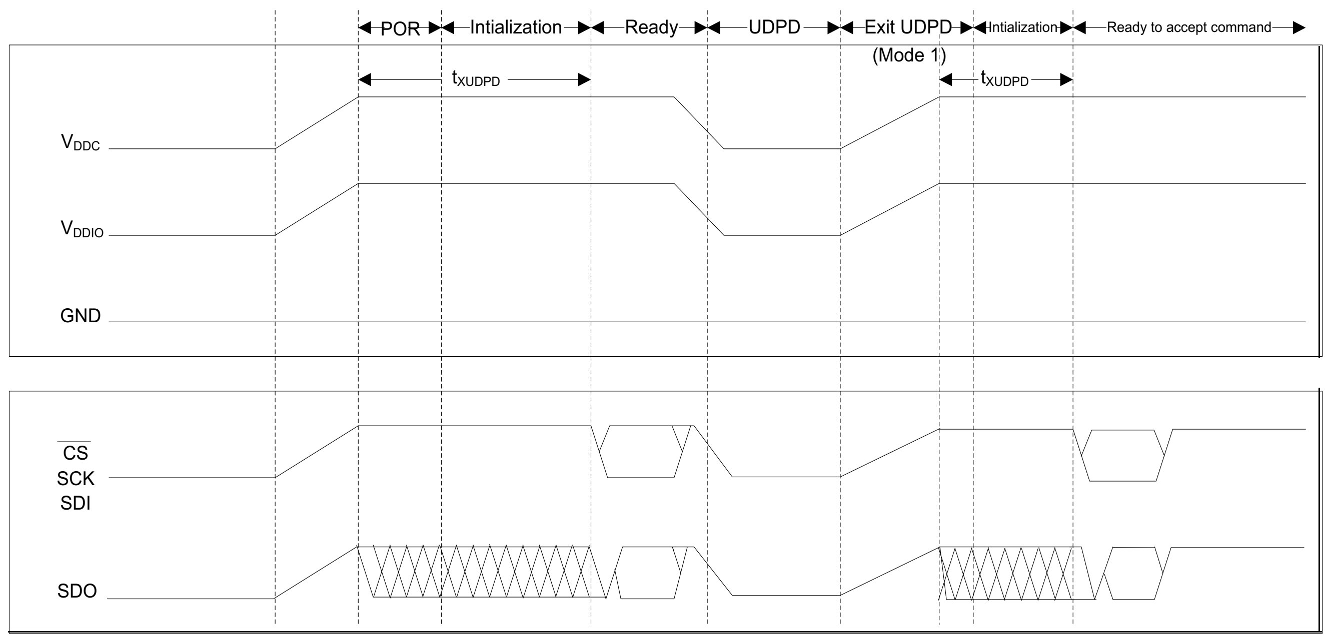


Figure 4-2. Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 1)



Note: V_{DDIO} and V_{DDC} must be powered up together. In order to READ or WRITE both voltages are required.

Figure 4-3. Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 2) [(1)]



1. VDDIO and VDDC must be powered up together. In order to READ or WRITE both voltages are required.

5. Pin Descriptions and Pin-out Diagrams

Table 5-1. Pin Descriptions

Mnemonic	Pin Number	Pin Name	Description
$\overline{CS}$	1	Chip Select	Making $\overline{CS}$ low activates the internal circuitry for device operation. Making $\overline{CS}$ high de-selects the device and switches into standby mode to reduce power. When the device is not selected ($\overline{CS}$ high), data is not accepted via the Serial Data Input pin (SDI) and the Serial Data Output pin (SDO) remains in a high-impedance state. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
SDO	2	Serial Data Out	Sends read data or status on the falling edge of SCK.
V_{DDC}	3	Core Power	Power Supply for digital controller and low voltage logic. A low ESR 100nF capacitor should be connected between each supply pin and GND.
GND	4	Ground	Ground pin.
SDI	5	Serial Data In	Device data input; accepts commands, addresses, and data on the rising edge of SCK. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
SCK	6	Serial Clock	Provides timing for the SPI interface. SPI commands, addresses, and data are latched on the rising edge on the Serial Clock signal, and output data is shifted out on the falling edge of the Serial Clock signal. To minimize power consumption, the master should ensure that this pin always has a valid logic level.
V_{DDIO}	7	I/O Power	I/O and Write Power Supply. A low ESR 100nF capacitor should be connected between each supply pin and GND (see Figure 5-2).
V_{DDIO}	8	I/O Power	I/O and Write Power Supply. A low ESR 100nF capacitor should be connected between each supply pin and GND (see Figure 5-2).

Figure 5-1. Pinout (Top View)

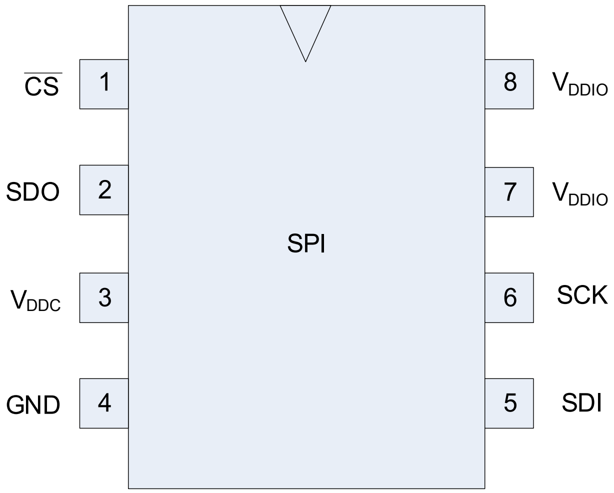
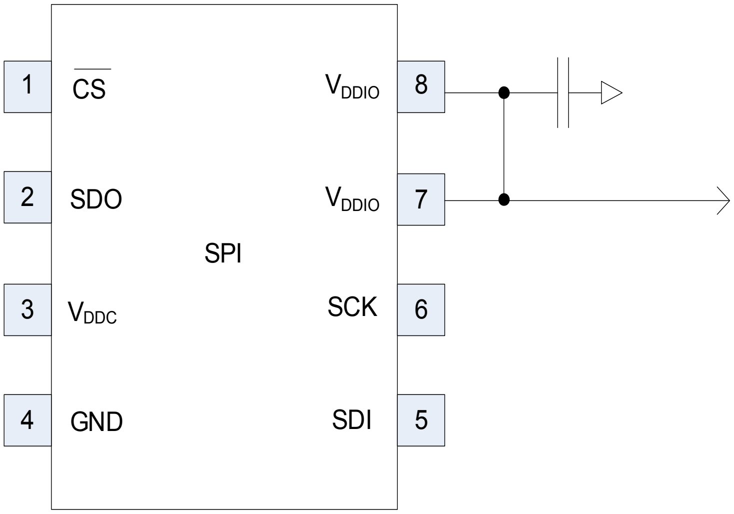


Figure 5-2. Suggested Signal Connections for Write Power Supply (Top View)



Note: The two VDDIO supply signals must be tied together to supply write and I/O voltage.

6. SPI Modes Description

Multiple Adesto SPI devices can be connected onto a Serial Peripheral Interface (SPI) serial bus controlled by an SPI master, such as a micro-controller, as shown in Figure 6-1.

Figure 6-1. Connection Diagram, SPI Master and SPI Slaves

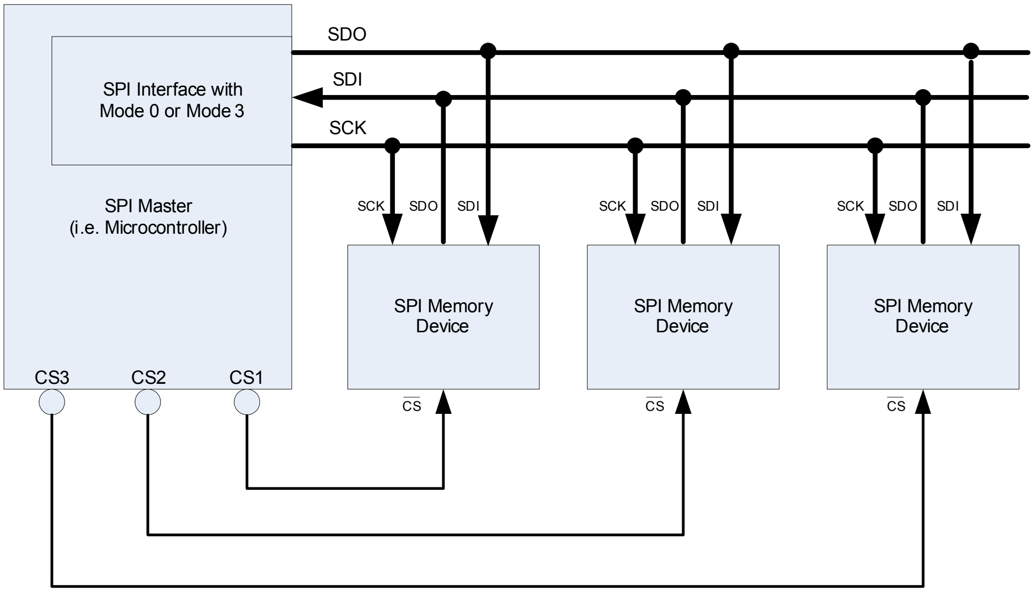
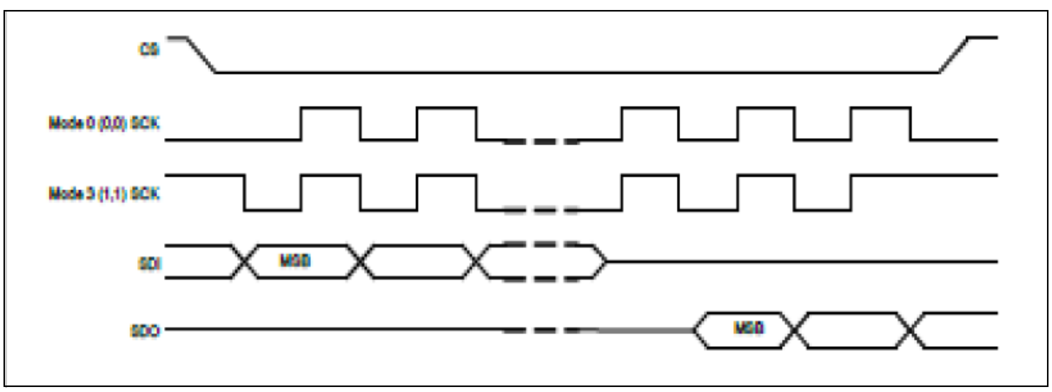


Figure 6-2. SPI Modes



7. Registers

7.1 Instruction Register

The Adesto RM331x Series uses a single 8-bit instruction register. The instructions and their operation codes are listed in Table 7-1. All instructions, addresses, and data are transferred with the MSB first, and begin transferring with the first low-to-high SCK transition after the $\overline{CS}$ pin goes low.

Table 7-1. Device Operating Instructions

Instruction	Description	Operation Code	Address Cycles	Dummy Cycles	Data Cycles
WRSR	Write Status Register	01h	0	0	1
WR	Write data to memory array	02h	2	0	1 - 64
READ	Read data from memory array	03h	2	0	1 - ∞
WRDI	Write Disable	04h	0	0	0
RDSR	Read Status Register	05h	0	0	1 - ∞
WREN	Write Enable	06h	0	0	0
WRSR2	Write Status Register2	31h	0	0	1
UDPD	Ultra-Deep Power- Down	79h	0	0	0

7.2 Status Register Byte 1

The Adesto RM331x Series uses a 2-byte Status Register. The BUSY and Write Enable (WEL) status of the device can be determined by reading the first byte of this register. The non-volatile configuration bits are also in the first byte. The Status Register can be read at any time, including during an internally self-timed write operation.

The Status Register Byte 1 format is shown in Table 7-2. The Status Register Byte 1 bit definitions are shown in Table 7-3.

Table 7-2. Status Register Byte 1 Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRWD	0	0	UDPD	BP1	BP0	WEL	BUSY

Table 7-3. Status Register Byte 1 Bit Definitions

Bit	Name	Description	R/W	Non-Volatile Bit
0	BUSY	Indicates the progress of a program or erase cycle. 0: Device is ready 1: Program/erase cycle is in progress and the device is busy	R	No
1	WEL	Write Enable Latch. 0: Device is disabled 1: Device is enabled	R/W	No
2	BP0	Block protection bits. 0: Specific blocks are not protected. 1: Specific blocks are protected.	R/W	Yes
3	BP1			

Table 7-3. Status Register Byte 1 Bit Definitions (Continued)

Bit	Name	Description	R/W	Non-Volatile Bit
4	UDPD	Ultra-Deep Power-Down Status. 0: Device is in Standby or in an active read/write operation. 1: Device is in Ultra-Deep Power-Down. Reading this bit after power-up or after exiting Ultra-Deep Power-Down indicates when the device is ready for operation.	R	No
5	N/A	Reserved. Read as 0.	N/A	No
6	N/A	Reserved. Read as 0.	N/A	No
7	SRWD	Status register hardware write protection. 0: Writable. User can write to the Status Register Byte1. 1: Protected. Status Register Byte 1 is locked.	R/W	Yes

7.3 Status Register Byte 2

The Adesto RM331x Series uses the second byte in the Status Register to hold volatile configuration bits. The Status Register Byte 2 format is shown in table Table 7-4 The Status Register Byte 2 bit definitions are shown in table Table 7-5.

Table 7-4. Status Register Byte 2 Format

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	SLOWOSC	AUDPD

Table 7-5. Status Register Byte 2 Bit Definitions

Bit	Name	Description	R/W	Non-Volatile Bit
0	AUDPD	Automatic Ultra-Deep Power-Down mode after write operation. 0: The device enters the Standby mode after a write operation is completed. 1: The device enters the Ultra-Deep Power-Down mode after a write operation is completed.	W	No
1	SLOWOSC	Slow oscillator during write operation. 0: During the self-times write operation the device does not slow down on-chip oscillator 1: During the self-times write operation the device periodically slows down on-chip oscillator.	W	No
2	N/A	Reserved. Read as 0.	N/A	No
3	N/A	Reserved. Read as 0.	N/A	No
4	N/A	Reserved. Read as 0.	N/A	No
5	N/A	Reserved. Read as 0.	N/A	No
6	N/A	Reserved. Read as 0.	N/A	No
7	N/A	Reserved. Read as 0.	N/A	No

8. Write Protection

The Adesto RM331x Series has two protection modes: Hardware write protection, and software write protection in the form of the SRWD, WEL, BP0, and BP1 bits in the Status Register.

8.1 Hardware Write Protection

There is one hardware write protection feature:

- All write instructions must have the appropriate number of clock cycles before $\overline{CS}$ goes high or the write instruction are ignored.
- The Status Register Byte 1 contains the BP[1:0] bits which are used to protect predefined regions in the Memory Array. The SRWD bit is used to prevent write access to the Status Register Byte1 to permanently set the Block Protection status. This is a non-volatile bit, and once the user sets it to 1, the Status Register Byte 1 is permanently locked.

Table 8-1. Hardware Write Protection on Status Register

SRWD	Status Register
0	Writable. User can write to the Status Register Byte 1.
1	Protected.Status Register Byte 1 is locked.

8.2 Software Write Protection

There are two software write protection features:

- Before any program, erase, or write status register instruction, the Write Enable Latch (WEL) bit in the Status Register must be set to a one by execution of the Write Enable (WREN) instruction. If the WEL bit is not enabled, all program, erase, or write register instructions are ignored.
- The Block Protection bits (BP0 and BP1) allow a part or the whole memory area to be write protected.

Table 8-2. Block Write Protect Bits

BP1	BP0	Protected Region	Protected Address	Protected Area Size
0	0	None	None	0
0	1	Top ¼	6000-7FFF	8K bytes
1	0	Top ½	4000-7FFF	16K bytes
1	1	All	0-7FFF	All

9. Reducing Energy Consumption

In normal operation, when the device is idle, ($\overline{CS}$ is high, no Write or Erase operation in progress), the device is in Standby Mode, waiting for the next command. To reduce device energy consumption, Ultra-Deep Power-Down modes may be used.

To minimize power consumption, the master should ensure that the SCK, SDI and $\overline{CS}$ pins always has a valid logic level, these pins should not be left floating when the device is in Standby or Ultra-Deep Power-Down modes.

9.1 Ultra-Deep Power-Down mode

The Ultra-Deep Power-Down mode allows the device to further reduce its energy consumption compared to the existing Standby mode by shutting down additional internal circuitry. The UDPD command (79h) is used to instruct the device to enter Ultra-Deep Power-Down mode (UDPD Mode 1). Alternately, for maximum power conservation, VDDC and VDDIO can be turned off externally (UDPD Mode 2).

To test if the device is in Ultra-Deep Power-Down (in UDPD mode 1) without risk of bringing it out of Ultra-Deep Power- Down mode, use the Read Status Register Byte 1 instruction. The UDPD bit in Status Register Byte 1 is 1 (pulled high by the internal pull-up resistor) if the device is in Ultra-Deep Power-Down mode, 0 otherwise.

When VDDC and VDDIO are turned off (UDPD Mode 2), all commands including the Read Status Register commands is ignored. Since all commands is ignored, the mode can be used as an extra protection mechanism against inadvertent or unintentional program and erase operations.

9.2 Auto Ultra-Deep Power-Down Mode after Write Operation

The Auto Ultra-Deep Power-Down Mode after Write Operation allows the device to further reduce its energy consumption by automatically entering the Ultra-Deep Power-Down Mode after completing an internally timed Write operation. The operation can be any one of the commands WR (Write), or WRSR (Write Status Register). Note that the WRSR2 command does not cause the device to go into Ultra-Deep Power-Down Mode. (See Table 7-5 for Status Register Byte 2 definition).

9.3 Slow Oscillator During Write Operation

The Slow Oscillator During Write Operation mode allows the device to further reduce its average current consumption by periodically slowing down the internal oscillator. This creates a duty cycle effect with time periods of high activity followed by timer periods of low activity. While this operating mode increases the effective Write time, the average current over this Write time is lower compared to the mode without this feature.

9.4 Exit Ultra-Deep Power-Down Mode

Only the Exit Ultra-Deep Power-Down signal sequences or power cycling described in Figure 4-2 and in Section 10.9 brings the device out of the Ultra- Deep Power-Down mode.

10. Instruction Descriptions

The RM331x Series memory devices support the following commands as described in Table 10-1.

Table 10-1. RM331x Series Command Listing

Hex Value	Acronym	Description
06h	WREN	Write enable command.
04h	WRDI	Write disable command.
05h	RDSR	Read Status register byte 1 command.
01h	WRSR	Write Status register byte 1 command.
31h	WRSR2	Write Status register byte 2 command.
03h	RD	Read data command. Used to read data from the Flash.
02h	WR	Write data command. Used to write data to the Flash.
9Bh	OTPP	OTP register program command. Sequence must be 9Bh, 00h, 00h to write the register.
77h	OTPR	Read OTP register command.
79h	UDPD	Ultra-deep power down command. Places the device in UDPD mode. Refer to Section 10.10 for the UDPD exit sequence.

10.1 WREN (Write Enable, 06h)

The device powers up with the Write Enable Latch (WEL) bit in the Status Register cleared to zero. This means that no write or erase instructions can be executed until the Write Enable Latch is set using the Write Enable (WREN) instruction. The WEL bit is also cleared to zero automatically after any non-read instruction. Therefore, all page programming instructions and erase instructions must be preceded by a Write Enable (WREN) instruction. The sequence for the Write Enable instruction is shown in Figure 10-1.

Figure 10-1. WREN Sequence (06h)

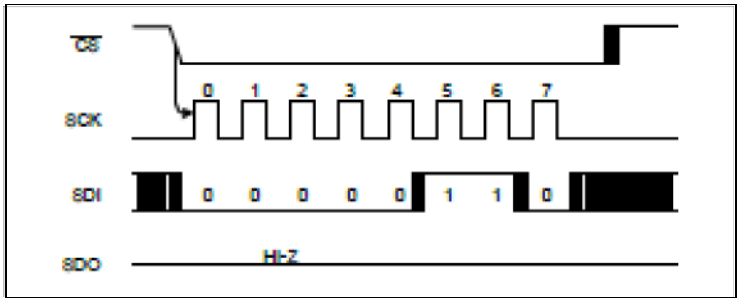


Table 10-2 is a list of actions that automatically clears the WEL bit when successfully executed. If an instruction is not successfully executed, for example if the $\overline{CS}$ pin is brought high before an integer multiple of 8 bits is clocked, the WEL bit is not reset.

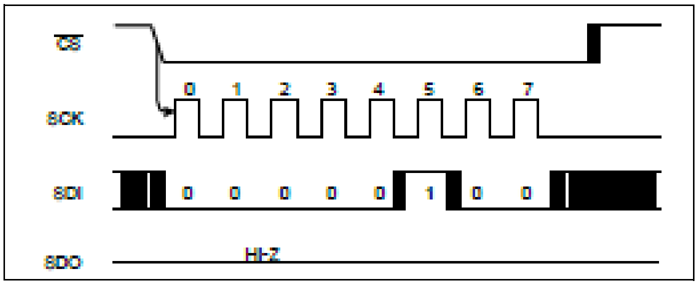
Table 10-2. Operations that Clear the Write Enable Latch Bit

Instruction/Operation
Power-Up
WRDI (Write Disable)
WR (Write)
WRSR (Write Status Register)
WRSR2 (Write Status Register 2)

10.2 WRDI (Write Disable, 04h)

To protect the device against inadvertent writes, the Write Disable instruction disables all write modes. Since the WEL bit is automatically reset after each successful write instruction, it is not necessary to issue a WRDI instruction following a write instruction. The WRDI sequence is shown in Figure 10-2.

Figure 10-2. WRDI Sequence (04h)

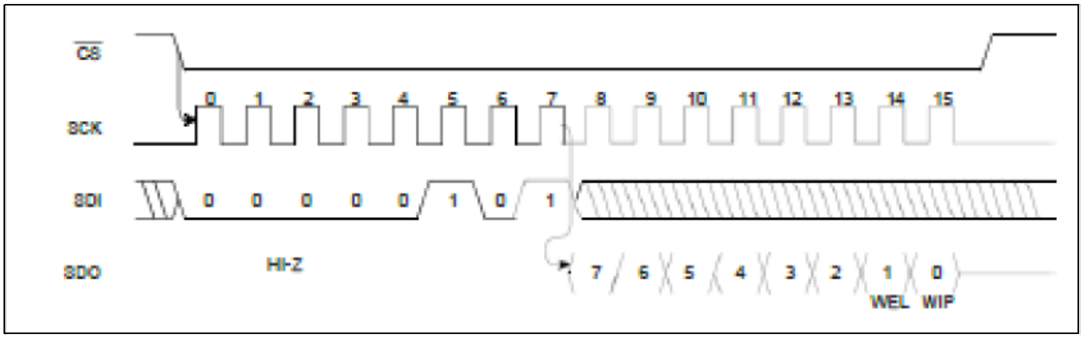


10.3 RDSR (Read Status Register Byte 1, 05h)

The Read Status Register Byte 1 instruction provides read access to the Status Register and indication of write protection status of the memory. Note that the BUSY and Write Enable Latch (WEL) bits indicate the status of the device.

The RDSR sequence is shown in Figure 10-3.

Figure 10-3. RDSR Sequence (05h)

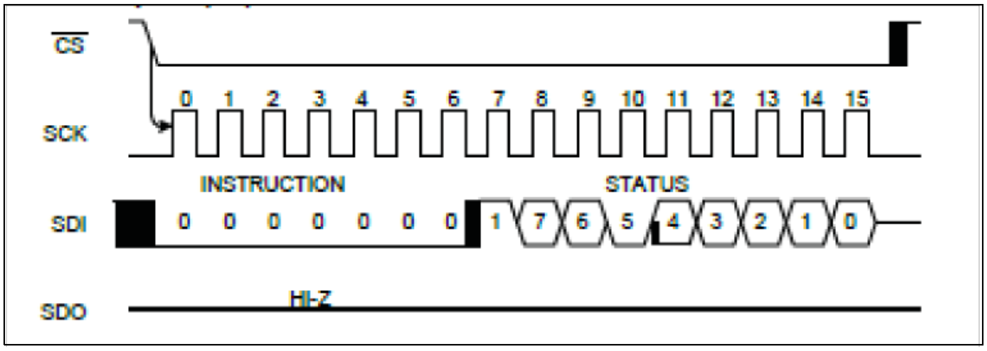


10.4 WRSR (Write Status Register Byte 1, 01h)

The Write Status Register (WRSR) instruction allows the user to select one of three levels of protection. The memory array can be block protected, or have no protection at all. The SRWD bit sets the write status of the Status Register (see Table 8-1).

Only the BP0, BP1 and SRWD bits are writable and are nonvolatile cells. The WRSR sequence is shown in Figure 10-4.

Figure 10-4. WRSR Sequence (01h)

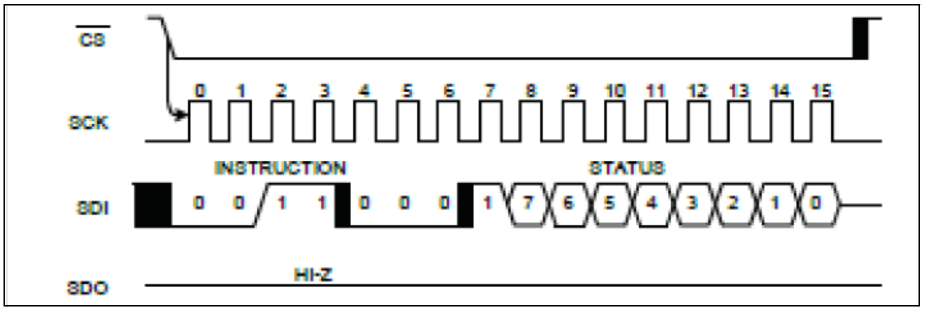


10.5 WRSR2 (Write Status Register Byte 2, 31h)

The Write Status Register Byte 2 (WRSR2) instruction allows the user to set or clear the SLOWOSC or AUDPD bits in Status Register 2. The user must set the WEL bit in the Status Register before issuing this command. Once the device accepts the WRSR2 command, hardware sets the BUSY bit to indicate that the device is busy. Once the device completes the operation, hardware clears the WEL and BUSY bits.

The WRSR sequence is shown in Figure 10-5.

Figure 10-5. WRSR2 Sequence (31h)



10.6 READ (Read Data, 03h)

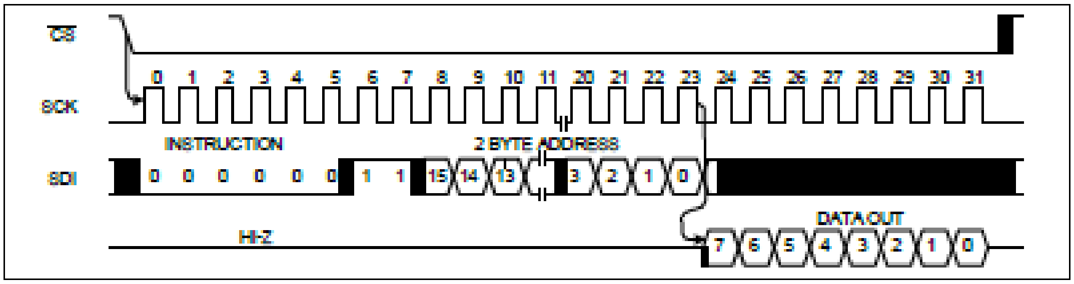
Reading the Adesto RM331x Series via the Serial Data Output (SDO) pin requires the following sequence:

1. The $\overline{CS}$ line is pulled low to select the device.
2. The 8-bit 03h op-code is transmitted via the SDI line.
3. The 16-bit read address is transmitted via the SDI line. Although not all 16 address bits are used, a full 2 bytes of address must be transmitted to the device. For the 32 - 256Kb device, only address A0 to A14 are used; the rest are don't cares and must be 0. Once the read instruction and address have been sent, any further data on the SDI line is ignored.

4. The data (D7-D0) fetched from the address specified in step 2 is shifted out onto the SDO line, with the most significant bit (D7) being transferred first. If only one byte is to be read, the $\overline{CS}$ line should be driven high after the byte of data comes out (on the 8th clock after the data transfer has started).
5. If additional bytes are to be read out, the READ sequence can be continued by keeping the $\overline{CS}$ low. At the end of the first data byte the byte address is internally incremented and the next highest address data byte is shifted out. When the highest address is reached, the address counter rolls over to the lowest address (00000), thus allowing the entire memory to be read in one continuous read cycle.

The READ sequence is shown in Figure 10-6.

Figure 10-6. Single Byte READ Sequence (03h)



10.7 WR (Write Data, 02h)

The Write (WR) instruction allows bytes to be written to the memory. But first, the device must be write-enabled via the WREN instruction (06h) described in Section 10.1. The $\overline{CS}$ pin must be brought high after completion of the WREN instruction; then the $\overline{CS}$ pin can be brought back low to start the WR instruction. The $\overline{CS}$ pin going high at the end of the WR input sequence initiates the internal write cycle. During the internal write cycle, all commands except the RDSR instruction are ignored.

A WR instruction requires the following sequence:

1. The $\overline{CS}$ line is pulled low to select the device.
2. The 8-bit WR (02h) opcode is transmitted via the SDI line.
3. Following the instruction opcode, the 16-bit address (A15-A0) is transmitted via the SDI line. For the 32 - 256 Kb devices, only address A0 to A14 are used; the rest are don't cares and must be 0.
4. Immediately following the address transfer, the data (D7 - D0) is transmitted via the SDI line. A write operation is capable of transferring between 1 - 64 bytes (32 bytes for the 32 Kbit and 64 Kbit products, and 64 bytes for 128 Kbit and 256 Kbit products).
5. The internal write cycle sequence starts after the $\overline{CS}$ pin is brought high. The low-to-high transition of the $\overline{CS}$ pin must occur during the SCK low-time immediately after clocking in the D0 (LSB) data bit.

The BUSY status of the device can be determined by initiating a Read Status Register (RDSR) instruction and monitoring the BUSY bit. If the BUSY bit is set, the write cycle is still in progress. If the BUSY bit is cleared, the write cycle has ended. Only the RDSR instruction is enabled during the write cycle.

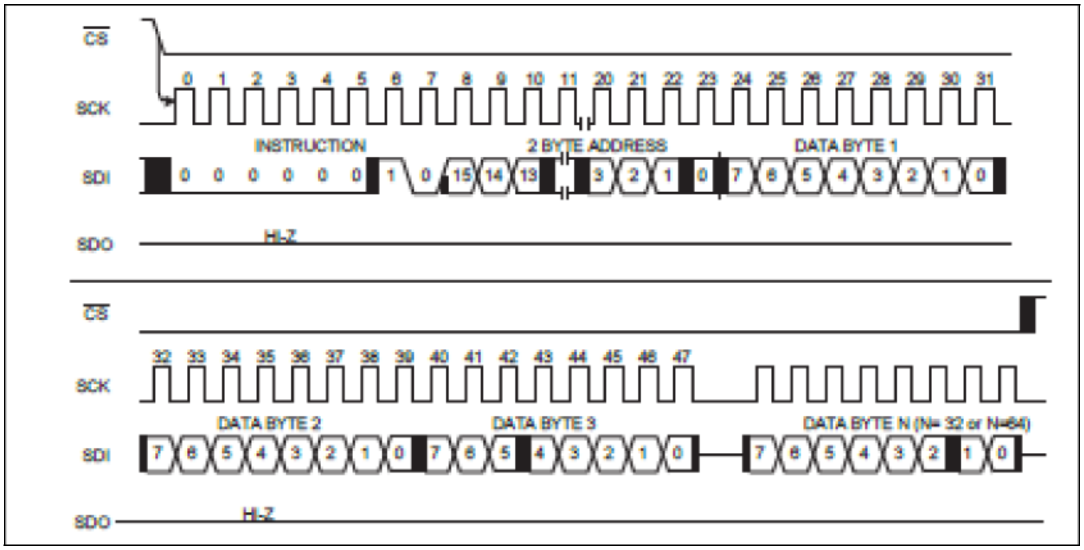
For devices with the 32 byte page size, after each byte of data is received, the five low-order address bits A4 - A0 are internally incremented by one; the high-order bits of the address remains constant. All transmitted data that goes beyond the end of the current page are written from the start address of the same page (from the address whose 5 least significant bits A4 - A0 are all zero). If more than 32 bytes are sent to the device, previously latched data are discarded and the last 32 data bytes are ensured to be written correctly within the same page. If less than 32 data bytes are sent to the device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

For devices with the 64 byte page size, after each byte of data is received, the six low-order address bits (A5 - A0) are internally incremented by one; the high-order bits of the address remains constant. All transmitted data that goes beyond the end of the current page are written from the start address of the same page (from the address whose 6 least significant bits A5-A0 are all zero). If more than 64 bytes are sent to the device, previously latched data are discarded and the last 64 data bytes are ensured to be written correctly within the same page. If less than 64 data bytes are sent to the device, they are correctly written at the requested addresses without having any effects on the other bytes of the same page.

The Adesto RM331x Series automatically returns to the write disable state at the completion of a program cycle. The sequence for the WR instruction is shown in Figure 10-7. Note that the multi-byte write operation is internally executed by sequentially writing the words in the Page Buffer.

NOTE: If the device is not write enabled (WREN) previous to the Write instruction, the device ignores the write instruction and return to the standby state when $\overline{CS}$ is brought high. A new $\overline{CS}$ falling edge is required to re initiate the serial communication.

Figure 10-7. WRITE Sequence (02h)



10.8 OTP Security Register

The RM331x device contains a specialized One-Time Programmable (OTP) Security Register that can be used for purposes such as unique device serialization or locked key storage. The register is comprised of a total of 128 bytes that is divided into two portions. The first 64 bytes (byte locations 0 through 63) of the Security Register are allocated as a One-Time Programmable space. Once these 64 bytes have been programmed, they cannot be erased or reprogrammed.

The remaining 64 bytes of the register (byte locations 64 through 127) are factory programmed by Adesto and contains a unique value for each device. The factory programmed data is fixed and cannot be changed.

Table 10-3. Security Register

Security Register Byte Number							
127	126	...	64	63	62	...	0
Factory Programmable by Adesto				One-Time User Programmable			

10.8.1 Programming the OTP Security Register (9Bh, 00h, 00h)

The user programmable portion of the Security Register does not need to be erased before it is programmed. To program the Security Register, a 3-byte opcode sequence of 9Bh, 00h, and 00h must be clocked into the device. After the last bit of the opcode sequence has been clocked into the device, the data for the contents of the 64-byte user programmable portion of the Security Register must be clocked in.

After the last data byte has been clocked in, the $\overline{CS}$ pin must be deasserted to initiate the internally self-timed program cycle. The programming of the Security Register should take place in a time of t_P, during which time the RDY/BUSY bit in the Status Register indicates that the device is busy. If the device is powered-down during the program cycle, then the contents of the 64-byte user programmable portion of the Security Register cannot be guaranteed.

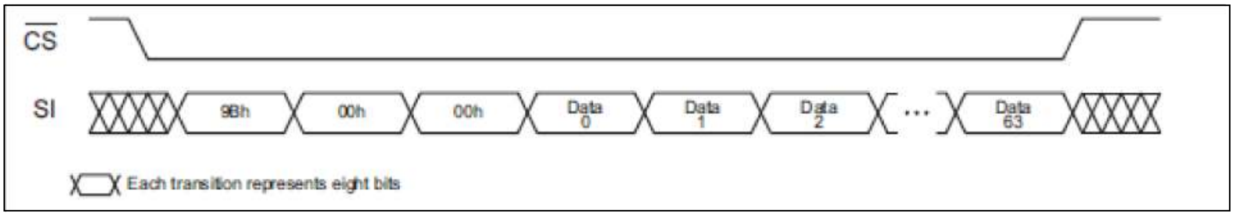
If the full 64 bytes of data are not clocked in before the $\overline{CS}$ pin is deasserted, then the values of the byte locations not clocked in cannot be guaranteed.

Example: If only the first two bytes are clocked in instead of the complete 64 bytes, then the remaining 62 bytes of the user programmable portion of the Security Register cannot be guaranteed. Furthermore, if more than 64 bytes of data is clocked into the device, then the data wraps back around to the beginning of the register. For example, if 65 bytes of data are clocked in, then the 65th byte is stored at byte location 0 of the Security Register.

Warning: The user programmable portion of the Security Register can only be programmed one time. Therefore, it is not possible, for example, to only program the first two bytes of the register and then program the remaining 62 bytes at a later time.

The Program Security Register command utilizes the internal buffer for processing. Therefore, the contents of the Buffer are altered from its previous state when this command is issued.

Figure 10-8. Program Security Register

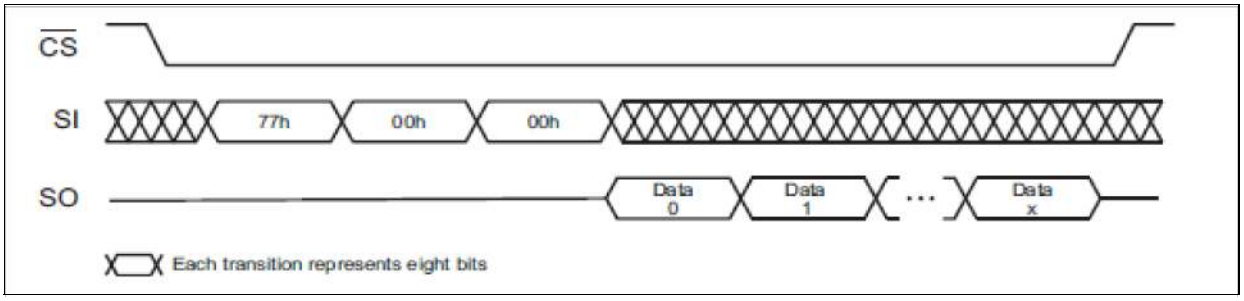


10.8.2 Reading the OTP Security Register (77h)

To read the Security Register, an opcode of 77h and two bytes of 00h must be clocked into the device. After the last dummy bit has been clocked in, the contents of the Security Register can be clocked out on the SO pin. After the last byte of the Security Register has been read, additional pulses on the SCK pin results in undefined data being output on the SO pin.

Deasserting the $\overline{CS}$ pin terminates the Read Security Register operation and put the SO pin into a high-impedance state.

Figure 10-9. Read Security Register



10.9 Ultra-Deep Power-Down (79h)

There are two different variations of Ultra-Deep Power-Down, UDPD mode 1 and UDPD mode 2. For UDPD mode 1, an SPI command is used to turn off the supply voltages internally on the chip. For UDPD mode 2, VDDC and VDDIO are turned off externally.

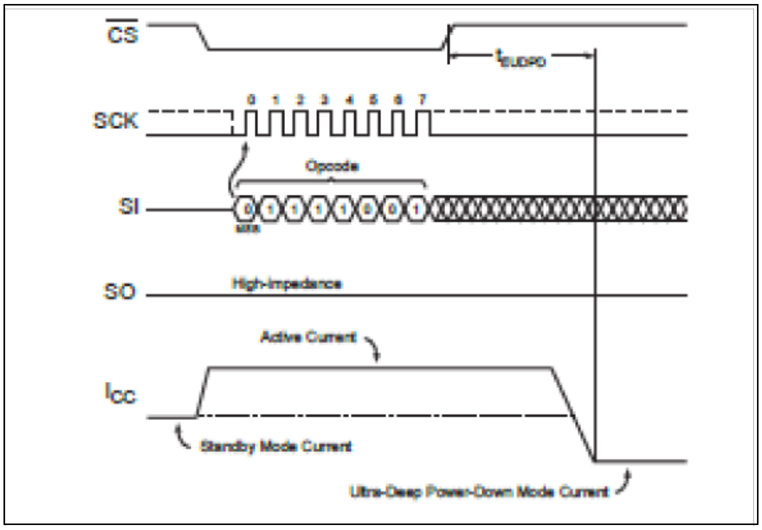
The Ultra-Deep Power-Down mode allows the device to further reduce its energy consumption compared to the existing Standby mode by shutting down additional internal circuitry. When the device is in the Ultra-Deep Power-Down mode (UDPD mode 2), all commands including the Read Status Register command is ignored. Since all commands are ignored, the mode can be used as an extra protection mechanism against inadvertent or unintentional program and erase operations.

10.9.1 UDPD Mode 1

Entering the Ultra-Deep Power-Down mode 1 is accomplished by simply asserting the $\overline{CS}$ pin, clocking in the opcode 79h, and then deasserting the $\overline{CS}$ pin. Any additional data clocked into the device after the opcode is ignored. When the $\overline{CS}$ pin is deasserted, the device enters the Ultra-Deep Power-Down mode within the maximum time of t_{EUDPD}. The complete opcode must be clocked in before the $\overline{CS}$ pin is deasserted; otherwise, the device aborts the operation and return to the standby mode once the $\overline{CS}$ pin is deasserted.

In addition, the device defaults to the standby mode after a power cycle. The Ultra-Deep Power-Down command is ignored if an internally self-timed operation such as a program or erase cycle is in progress. The sequence for UDPD is shown in Figure 10-10. See also Figure 4-2, Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 1).

Figure 10-10.Ultra-Deep Power-Down (79h)



10.9.2 UDPD Mode 2

In this mode, VDDC and VDDIO are turned off externally. Ideally both voltages should be turned off at the same time. If this is difficult to achieve, and there is a time difference between the shutoff of the two voltages, the system designer should make sure that VDDIO is turned off before VDDC.

Similarly, when the device is turned on again, VDDIO should be turned on before VDDC if it is not possible to turn both on at the same time.

See Figure 4-3, Power-up Timing (Enter/Exit Ultra-Deep Power-Down Mode 2).

10.10 Exit Ultra-Deep Power-Down

To exit from the Ultra-Deep Power-Down mode does not involve the execution of an instruction, but rather the issuance of a reset sequence. This reset sequence can be initiated in one of two ways as described below:

10.10.1 Exit Ultra-Deep Power-Down / JEDEC Hardware Reset

Initiate the Exit Ultra-Deep Power-Down / JEDEC Hardware Reset sequence as described in Section 11. JEDEC Hardware Reset.

10.10.2 Power Cycling

The use can also exit the Ultra-Deep Power mode by power cycling the device. The system must wait for the device to return to the standby mode before normal command operations can be resumed. Upon recovery from Ultra-Deep Power-Down, all internal registers are set to their power-on default state.

11. JEDEC Hardware Reset

The Exit Ultra-Deep Power-Down / JEDEC Hardware Reset sequence is used to reset the device to its power on state without cycling power. The other way is to power-cycle the device by removing power to the V_{DDIO} and V_{DDC} pins as described in Section 10.10.2. In this case, Adesto recommends performing a Hardware Reset sequence each time the device is powered up.

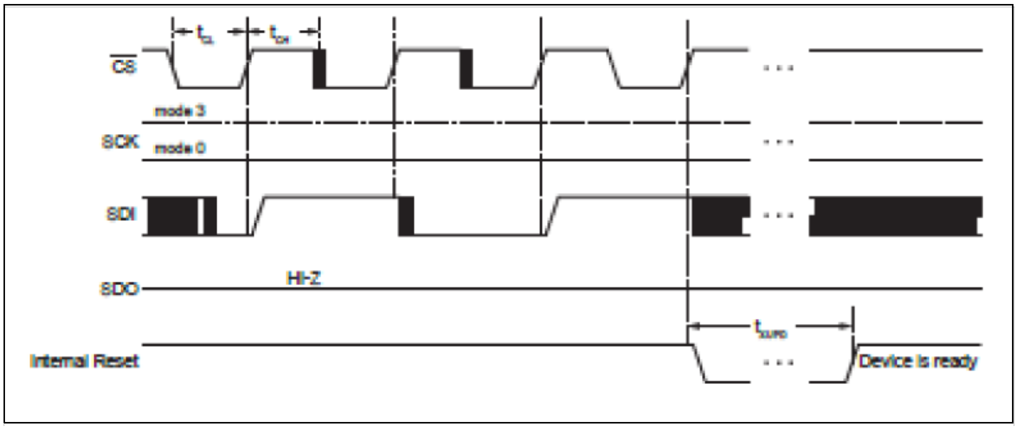
The reset sequence does not use the SCK pin. The SCK pin has to be held low (mode 0) or high (mode 3) through the entire reset sequence.This prevents any confusion with a command, as no command bits are transferred (clocked).

A reset is commanded when the data on the SDI pin is 0101 on four consecutive positive edges of the $\overline{CS}$ pin with no edge on the SCK pin throughout. This is a sequence where:

1. $\overline{CS}$ is driven active low to select the device. This powers up the SPI slave.
2. Clock (SCK) remains stable in either a high or low state.
3. SDI is driven low by the bus master, simultaneously with $\overline{CS}$ going active low. No SPI bus slave drives SDI low before a transition of SCK. In other words, the slave streaming output active is not allowed until after the first edge of SCK.
4. $\overline{CS}$ is driven inactive. The slave captures the state of SI on the rising edge of $\overline{CS}$. The above steps are repeated four times, each time alternating the state of SI.

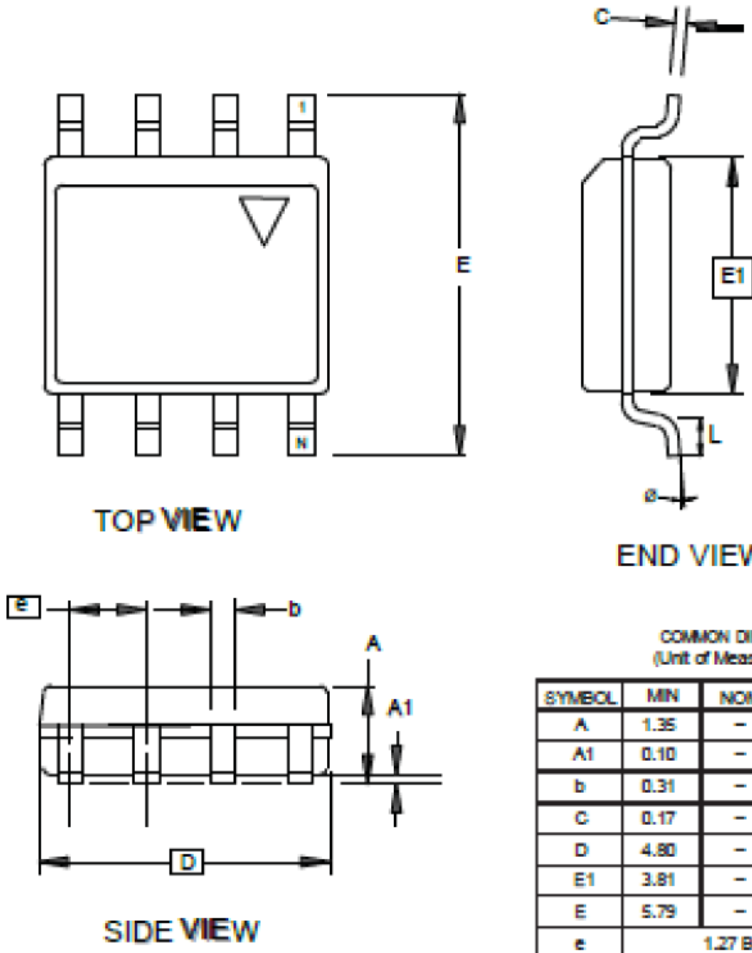
After the fourth $\overline{CS}$ pulse, the slave triggers its internal reset. SI is low on the first $\overline{CS}$, high on the second, low on the third, high on the fourth. This provides a 5h, unlike random noise. Any activity on SCK during this time halts the sequence and a Reset is not generated. Figure 11-1 below illustrates the timing for the Hardware Reset operation.

Figure 11-1. Hardware Reset



12. Package Information

12.1 8S1 — JEDEC SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	1.35	–	1.75	
A1	0.10	–	0.25	
b	0.31	–	0.51	
C	0.17	–	0.25	
D	4.80	–	5.05	
E1	3.81	–	3.99	
E	5.79	–	6.20	
e	1.27 BSC			
L	0.40	–	1.27	
ø	0°	–	8°	

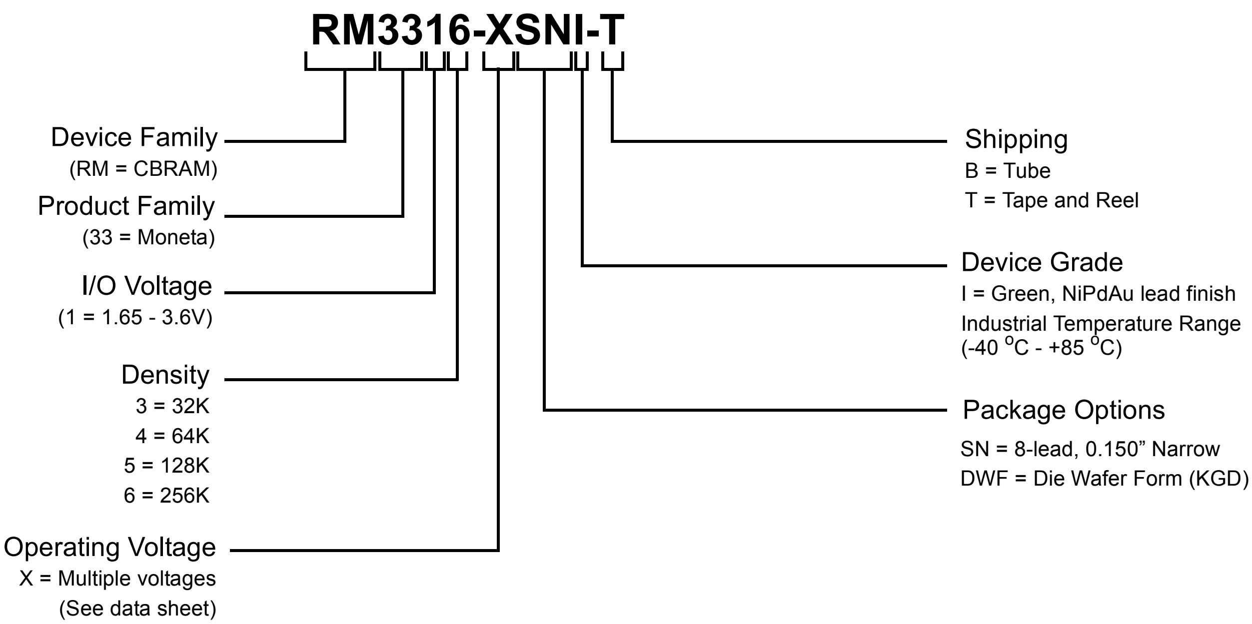
Notes: This drawing is for general information only. Refer to JEDEC Drawing MS-012, Variation AA for proper dimensions, tolerances, datums, etc.

8/20/14

	TITLE	GPC	DRAWING NO.	REV.
adesto Package Drawing Contact: contact@adestotech.com	8S1, 8-lead (0.150" Narrow Body), Plastic Gull Wing Small Outline Package (JEDEC SOIC)	SWB	8S1	G

13. Ordering Information

13.1 Ordering Detail



13.2 Ordering Codes

Ordering Code	Package	Density	Voltage	f_{sck}	Grade	Carrier
RM3316-XSNI-T	SN	256 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel
RM3315-XSNI-T	SN	128 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel
RM3314-XSNI-T	SN	64 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel
RM3313-XSNI-T	SN	32 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Reel
RM3316-XSNI-B	SN	256 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Bulk (Tubes)
RM3315-XSNI-B	SN	128 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Bulk (Tubes)
RM3314-XSNI-B	SN	64 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Bulk (Tubes)
RM3313-XSNI-B	SN	32 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Bulk (Tubes)

Ordering Code	Package	Density	Voltage	f_{sck}	Grade	Carrier
RM3316-X-DWF	DWF	256 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer
RM3315-X-DWF	DWF	128 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer
RM3314-X-DWF	DWF	64 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer
RM3313-X-DWF	DWF	32 Kbit	Multiple voltages	1 MHz	Commercial (-40°C to 85°C)	Wafer

Package Type	
SN	8-lead 0.150" wide, Plastic Gull Wing Small Outline (JEDEC SOIC)
DWF [1]	Die in Wafer Form (Known Good Die - KGD)

1. Contact Adesto for Wafer Die Map and other ordering information.

14. Revision History

Document Revision	Date	Comments
A	2/2017	Initial document release.
B	7/2017	Updated product description (page 1). Corrected UDPD specification on page 1. Updated command description in section 10.7 (Write Data - 02h). Added footnote to Table 3.1. Updated Status Register Byte 2 Bit Definitions (changed to Write only). Updated description of SRWD (Section 8.1). Added DWF package option.
C	11/2017	Added patent information.
D	03/2018	Updated specifications for V_{DDIO}. Add section on OTP register.
E	11/2018	Updated Figures 4-1 through 4-3, Synchronous Data Timing, Power Up Timing (mode 1) and Power Up Timing (mode 2). In Table 3-1, Input Supply Voltage - VDDC to GND, changed maximum value from 1.25V to 1.45V. In Table 3-1, added footnote 2 to the above value to indicate maximum voltages for read and write operations. In Table 3-2, split VDDC value into VDDC-WR and VDDC-RD and listed voltage ranges accordingly. In Table 3-2, add footnote 3 to IDD1 parameter. In Table 3-2, update text for footnote 2. In Table 3-3, update fSCK and tSCK table entries. Updated Revision History table from Rev D to Rev E. Standardized format of Revision History Table. Updated legal text on back page. Updated Title text at bottom of package drawing in Section 11.1, 8S1 Narrow SOIC package to change from Wide to Narrow for 0.150" package. Changed footer on all pages from Rev D to Rev E. Updated date code on all pages from 4/2018 to 11/2018. Updated maximum VDDC voltage on page 1 from 1.23V to 1.26V. Performed thorough technical of entire document. Reformatted and standardized all tables for consistency. Moved part number and memory densities table from the Write Instruction command in Section 10.7 to Section 1. Added Table 10-1. RM331x Series Command Listing

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