Dragster

Datasheet

Published by ams-OSRAM AG
Tobelbader Strasse 30, 8141 Premstaetten, Austria
Phone +43 3136 500-0
ams-osram.com

Table of contents

Dragster Line scan sensor

1 General description

Dragster is a platform of digital line-scan sensors. The sensor family is made using three types of basic elements: a single line element from 2K to 8K pixel resolution (7 µm pixel size and pitch), a dual line element from 2K to 8K pixel resolution (7 µm pixel size and pitch) and a single line element from 4K to 16K pixel resolution (3.5 µm (H) x 3.5 µm (V) pixel size). The chip versions with dual line are optionally available with Bayer Pattern RGB filters placed on the sensors.

The sensor features a low noise pixel with true CDS and global shutter for interleaved readout and integration operation. Each pixel has an on pixel 13-bit ADC and its gain can be programmed in a range of -6 dB till +20 dB by means of an 8-bit DAC controlled over the serial configuration interface.

The readout is made by two 13-bit wide digital taps organized in odd/even order for each 2K segment. For each line segment, 2K (7 µm pixel) or 4K (3.5 µm pixel), all pixels are read out. For sensor versions with 3.5 µm pixel pitch, two 2K segment readout circuits are placed on each side of the pixel line, to lead to a basic segment of 4K pixels, where even pixels are read out over the bottom readout and odd pixels are read out over the top readout.

Start and end of integration, as well as optional start of readout, are started upon individual external trigger events.

To enhance dynamic range multiple non-destructive readouts are possible.

1.1 Key benefits & features

The benefits and features of Dragster, Line scan sensor are listed below:

Table 1: Dragster benefits and features

Benefits	Features	Differentiators
Allows integration in inspection systems and cameras on the basis of the same electronics	High resolution, complete family 2K to 16K versions	Most complete sensor family on the market. Complete coverage of high resolution & high-speed Monochrome scanning needs
Allows inspection speed to increase => higher machine production speed.	Line rates up to 80 kHz for all resolutions	Competing products offer reduced line rates at higher resolution

Benefits	Features	Differentiators
Easy integration	Completely digital sensor	Improved camera quality compared to CCD based products
COB/Invar package	High mechanical stability and planarity of the die. Re-use of the same camera interface across different Dragster variants	

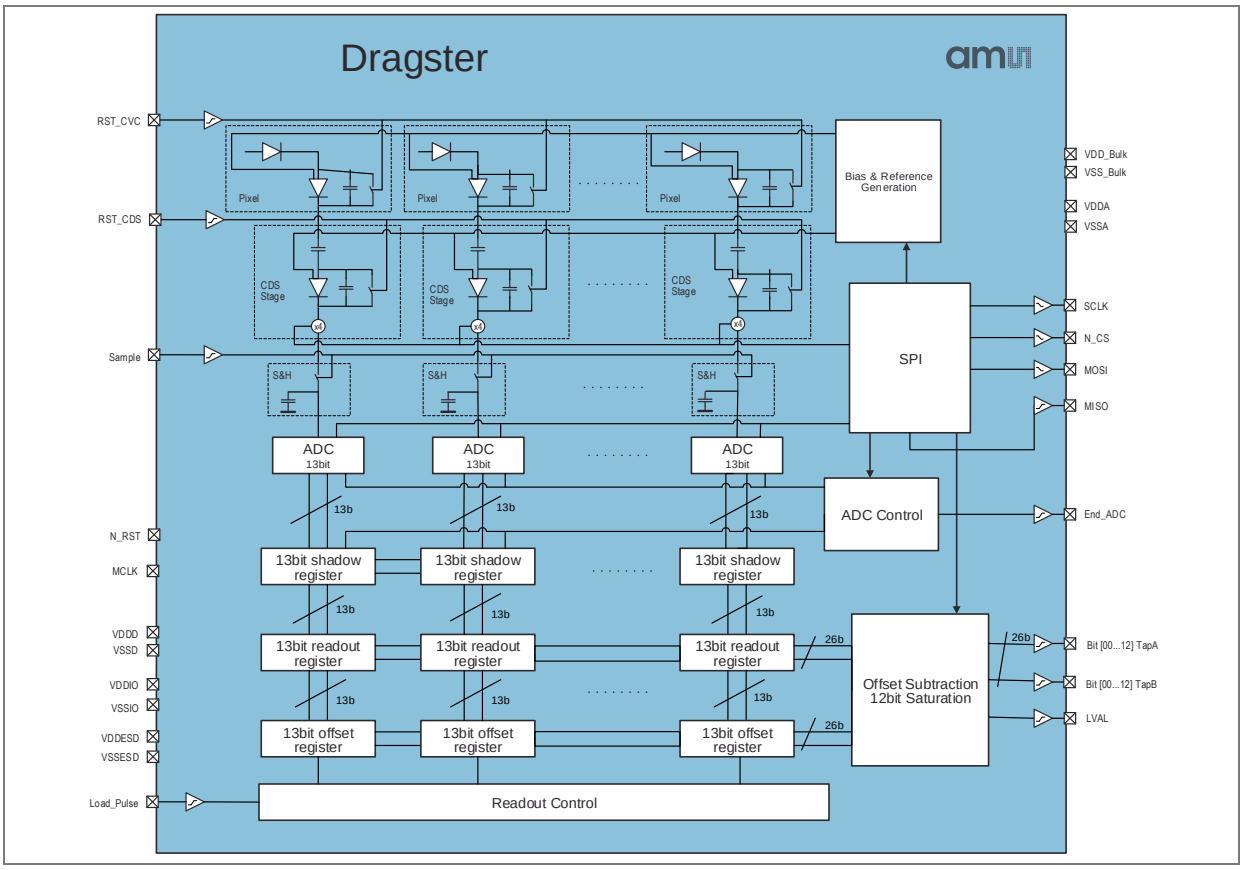
1.2 Applications

- Automated Optical Inspection (AOI) in (SMD, PCB, flat panel, web)
- Industrial sorting (e.g. food)

1.3 Block diagram

The functional blocks of this device are shown below:

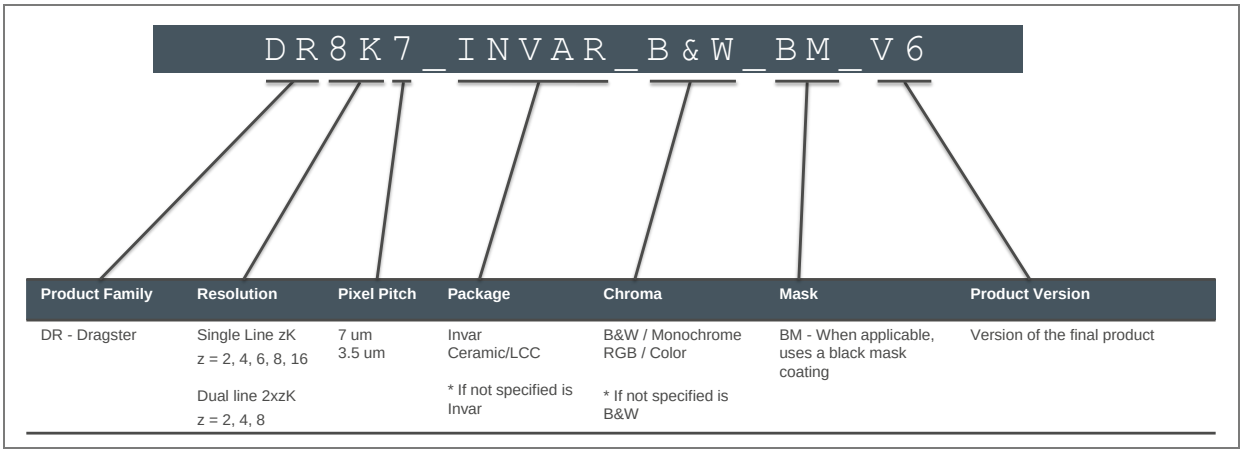
Figure 1: Dragster block diagram



2 Ordering information

Part number	Q number	Ordering code	Package	Chroma	Delivery quantity (pcs/tray)
301740016	Q65114A3364	DR2K7_Invar_B&W_BM_v6	Invar	Mono	4
301740011	Q65114A3362	DR2K7_LCC_B&W_BM_Ceramic_v1.0	Ceramic	Mono	12
301110006	Q65114A3337	DR2x2K7_LCC_B&W_Ceramic_v1.0	Ceramic	Mono	12
301720007	Q65114A3358	DR2x2K7_LCC_RGB_Ceramic_v1.0	Ceramic	Color	12
301110008	Q65114A3338	DR2x2K7_Invar_B&W_v6	Invar	Mono	4
301720008	Q65114A3359	DR2x2K7_Invar_RGB_v6	Invar	Color	4
301090010	Q65114A3335	DR4K3.5_Invar_B&W_v6	Invar	Mono	4
301090009	Q65114A3334	DR4K3.5_LCC_B&W_Ceramic_v1.0	Ceramic	Mono	12
301020013	Q65114A3330	DR4K7_Invar_B&W_BM_v5	Invar	Mono	4
301030008	Q65114A3331	DR2x4K7_Invar_B&W_v6	Invar	Mono	4
301040008	Q65114A3332	DR2x4K7_Invar_RGB_v6	Invar	Color	4
301240011	Q65114A3352	DR6K7_BM_v2	Invar	Mono	2
301250014	Q65114A3356	DR8K3.5_Invar_B&W_BM_v6	Invar	Mono	4
301750005	Q65114A3365	DR8K7_Invar_B&W_BM_v6	Invar	Mono	2
301120005	Q65114A3339	DR2x8K7_Invar_B&W_v5	Invar	Mono	2
301730005	Q65114A3360	DR2x8K7_Invar_RGB_v5	Invar	Color	2
301100006	Q65114A3336	DR16K3.5_Invar_B&W_v6	Invar	Mono	2

Figure 2: Ordering code



3 Pin assignment

3.1 Pin diagram

The available packages are organized in two main types: LCC Ceramic and INVAR. The LCC is a no lead package where the silicon's carrier is ceramic while the INVAR package uses a special nickel-iron alloy as heat dissipation and mechanical reference. While the LCC Ceramic package is oriented for size, resolution and cost conscious applications, the INVAR type is focused on high performance and robustness, where highest speed and high resolutions are the main advantages to the field application. All package types take a cover glass (anti-reflective coating) over sensor's silicon to protect from external dust particles.

For the customer, one of the most obvious advantages of Dragster packages is the use of commercially available INVAR connectors or low cost LCC Ceramic connections. This makes each camera development fast, easy and also brings other advantages: precise mechanical alignment to the optics by taking INVAR as reference and its CNC machined features, integrated heat dissipation plate that minimizes sensor stress in z-axis, maximization of sensor performance in speed and noise and customizable package to suit any requirement. The LCC Ceramic can also be mounted as a SMD part.

Dragster INVAR modules have up to four Molex connectors with 120-pin and reference 5010171203. On the camera side the matching part is 546841204.

Figure 3: Pin numbering of DR16K3.5 and DR2x8K7 (back view)

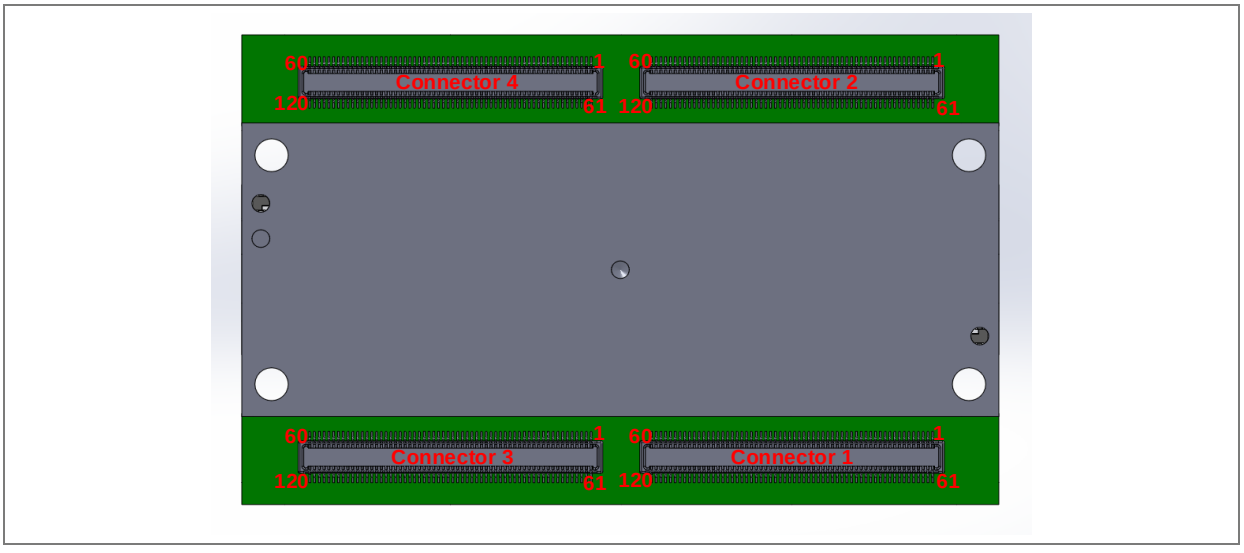


Figure 4: Pin numbering of DR6K7 (back view)

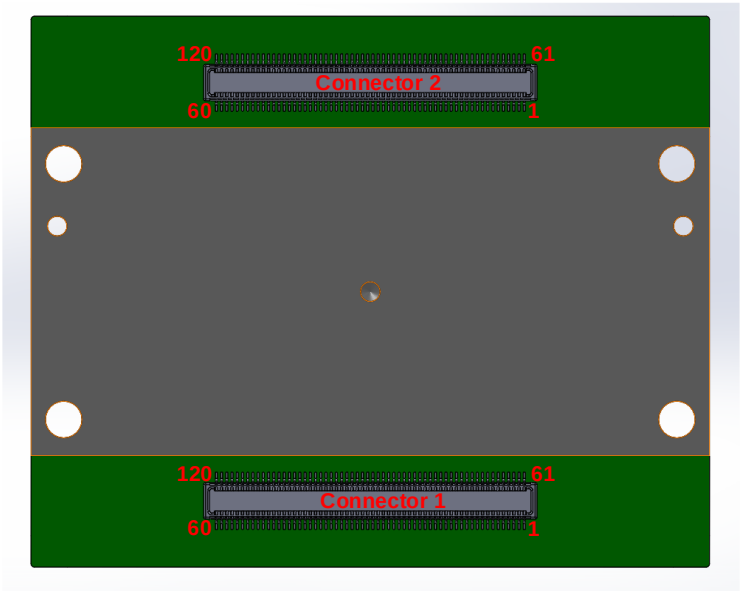
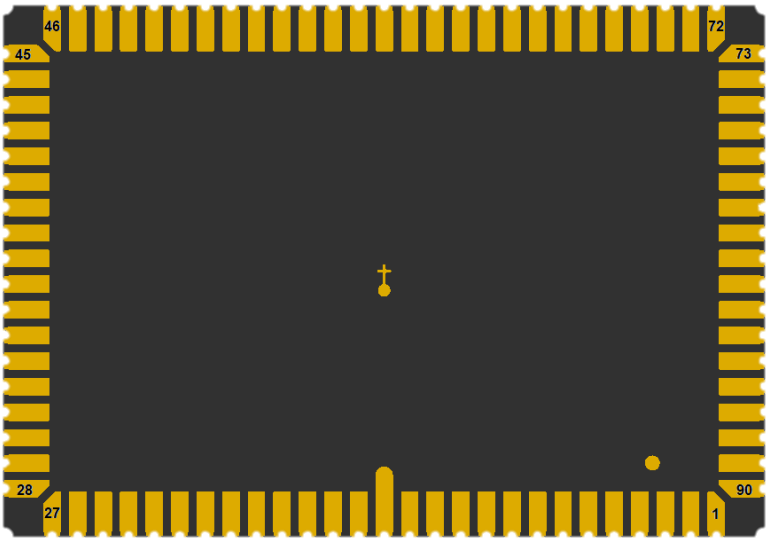


Figure 5: Pin numbering of LCC variant (back view)



The below table indicates which connectors are present for the different sensors versions.

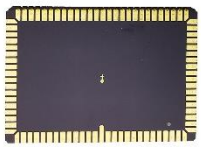
Table 2: Connector usage per sensor

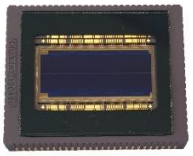
Sensor	Present connectors	Connector reference	Mating part
DR2K7_LCC_Ceramic	Not applied		
DR2x2K7_LCC_Ceramic			
DR4K3.5_LCC_Ceramic			
DR4K7_Invar	Connector 1	Molex 501017 1203	Molex 546841204
DR2K7-Invar(1)	Connectors 1 & 2		
DR2x2K7-Invar			
DR4K3.5-Invar			
DR2x4K7-Invar			
DR6K7-Invar			
DR8K3.5-Invar			
DR8K7-Invar	Connectors 1 & 3		
DR2x8K7-Invar	Connectors 1 - 4		
DR16K3.5-Invar			

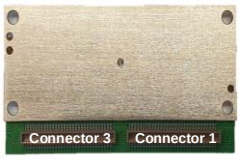
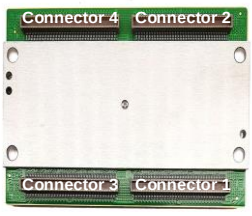
(1) For DR2K7_Invar, connector 2 is present but not required. Only the powers present on the connector are routed to the sensor. Connector 2 can be left completely unconnected for DR2K7_Invar.

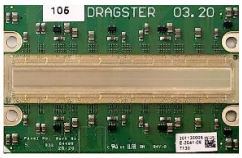
A package overview for all sensor versions is shown in the below table.

Table 3: Package overview

Part number	Ordering code	Top view	Bottom view
301740016	DR2K7_Invar_B&W_BM_v6		
301740011	DR2K7_LCC_B&W_BM_Ceramic_v1.0		
301110006	DR2x2K7_LCC_B&W_Ceramic_v1.0		

Part number	Ordering code	Top view	Bottom view
301720007	DR2x2K7_LCC_RGB_Ceramic_v1.0		
301110008	DR2x2K7_Invar_B&W_v6		
301720008	DR2x2K7_Invar_RGB_v6		
301090010	DR4K3.5_Invar_B&W_v6		
301090009	DR4K3.5_LCC_B&W_Ceramic_v1.0		
301020013	DR4K7_Invar_B&W_BM_v5		

Part number	Ordering code	Top view	Bottom view
301030008	DR2x4K7_Invar_B&W_v6		
301040008	DR2x4K7_Invar_RGB_v6		
301240011	DR6K7_BM_v2		
301250014	DR8K3.5_Invar_B&W_BM_v6		
301750005	DR8K7_Invar_B&W_BM_v6		
301120005	DR2x8K7_Invar_B&W_v5		
301730005	DR2x8K7_Invar_RGB_v5		

Part number	Ordering code	Top view	Bottom view
301100006	DR16K3.5_Invar_B&W_v6		

The table below exemplifies which sensor versions have a common headboard and footprint.

Table 4: Sensor shared headboard and footprint.

	Package	Sensor
Same headboard	Invar	DR2K7, DR2x2K7, DR4K3.5
		DR2x4K7, DR8K3.5
		DR2x8K7, DR16K3.5
Same footprint & pinout	LCC_Ceramic	DR2K7, DR2x2K7, DR4K3.5

4 Absolute maximum ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 5: Absolute maximum ratings of Dragster

Symbol	Parameter	Min	Max	Unit	Comments
Electrical parameters					
VDDD	Supply voltage to ground	-0.3	3.6	V	
VDDA	Supply vvoltage to ground	-0.3	3.6	V	
VIO	Input/ output pin voltage to digital inputs	-0.3	VDDIO + 0.3 or 3.6	V	
IIO	Input/ output DC forward bias current		-24 (source) + 24 (sink)	mA	
V_{IN}	Input pin voltage to ground		3.6	V	
Temperature ranges					
T_A	Operating temperature range(1)	0	60	°C	
$R_{TH, JC}$	Junction to case thermal resistance(2)		0.36	°C/W	
T_J	Operating junction temperature(3)	-55	125	°C	
Storage condition					
T_{STRG}	Storage temperature range	-30	40	°C	
RH_{NC_STRG}	Long term storage humidity	30	60	%	
	Shelf life		5	Years	Invar package
			2		Ceramic LCC package
MSL	Moisture sensitivity level		6		
	Bake out before soldering		24hrs @ 125ºC, ±5ºC		
Bump temperature (soldering) (4)					
T_{PEAK}	Peak temperature		245	°C	Refer to chapter 11
t_{WELL}	Well time above 217 °C	60	80	s	Refer to chapter 11

(1) The operating temperature range is regarding the ambient temperature that is more suitable for a good performance of the sensor. It is considered with no heat dissipation, since it is the environment temperature.
(2) Determined to DR16K3.5 Invar packaging, and calculated from the die to the bottom of the Invar plate. Relevant if a heat dissipater is attached to the Invar.
(3) Operating the silicon within this temperature range is manageable, though it does not ensure consistent device performance. It is worth noticing that prolonged exposure to such extreme temperature is not recommended.
(4) Relative to the ceramic LCC package.

5 Electrical characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Table 6: Electrical characteristics of Dragster

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDDA	Analogue power Supply		3.2	3.3	3.4	V
V_{nrms}VDDA	RMS noise on VDDA				5	mV
V_{npp}VDDA	Peak to peak noise on VDDA				20	mV
VDDD	Power supply voltage		3.2	3.3	3.4	V
V_{nrms}VDDD	RMS noise on VDDD				20	mV
V_{npp}VDDD	Peak to peak noise on VDDD				100	mV
VDDIO	Power supply voltage on IO's		2.4(1)	3.3	3.4	V
V_{nrms}VDDIO	RMS noise on VDDIO				20	mV
V_{npp}VDDIO	Peak to peak noise on VDDIO				100	mV
VDDESD	Power supply voltage ESD		3.2	3.3	3.4	V
VSSA	Ground for analogue power supply			0		V
VSSD	Ground for digital power supply			0		V
VSSIO	Ground for IO power supply			0		V
Duty Cycle	Input clock duty cycle	Up to 50 MHz	45	55	70	%
Duty Cycle	Input clock duty cycle	Up to >50 MHz	55	57	65	%
Jitter Clock	Input clock jitter				< 5% TCLK	% TCLK
C_{Load}	Load capacitance on digital IO's				10	pF
Input Clock Frequency			1(2)		85(3)	MHz
Characteristics for CMOS-LVTTL outputs						
V_{OL}	Low level output voltage				0.5	V
V_{OH}	High level output voltage		VDDIO-0.6			V
$T_{slew, rising}$(4)	Output slew rate of rising edge				5	ns
$T_{slew, falling}$(4)	Output slew rate of falling edge				5	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Characteristics for CMOS-LVTTL inputs						
V_{IL}	Low level input voltage		-0.3	0	0.4	V
V_{IH}	High level input Voltage		0.8 x VDDIO	VDDIO	VDDIO+0.3	V
I_{IL}	Low level input leakage	V_I = 0			±1	µA
I_{IH}	High level input leakage	V_I = VDDIO			±1	µA
$T_{slew, rising}$	Input slew rate of rising edge				2.5	ns
$T_{slew, falling}$	Input slew rate of falling edge				2.5	ns
T_{Setup}, Data In	Setup time for digital input signals relative to rising edge of MCLK	@ MCLK pin	3			ns
T_{Hold}, Data In	Hold time for digital input signals relative to rising edge of MCLK	@ MCLK pin	3			ns
T_{Setup}, Control Signals	Setup time for control signals relative to rising edge of MCLK		1			ns
T_{Hold}, Control Signals	Hold time for control signals relative to rising edge of MCLK		6			ns
T_{Setup}, MOSI	Setup time for MOSI input signals relative to rising edge of SCLK		3			ns
T_{Hold}, MOSI	Hold time for MOSI input signals relative to rising edge of SCLK		5			ns
Power Consumption[5]						
P_{Total}	Power consumption per 2K segment				500	mW
I_{VDDA}	Current to analogue devices per 2K segment				70	mA
I_{VDDD}	Current to Digital devices per 2K segment				35	mA
I_{VDDIO}	Current for IO per 2K segment				40	mA

(1) VDDIO < 3.0 V is not recommended for pixel clock speeds above 40 MHz and may not meet the slew rate specifications in all cases. As LCC Ceramic package has, VDDD/VDDIO/VDDESD wired internally, this situation is not applicable.
(2) The input clock frequency can be lower than 1 MHz. However, the ADC conversion accuracy might be reduced.
(3) The ADC can be clocked with up to 100MHz for faster conversion when using clock reduction for readout.
(4) The output swing on signal pixel clock, if enabled, may be smaller at pixel clock rates above 60 MHz.
(5) Typical values.

Table 7: Typical power consumption for Dragster(1)

Sensor	I_{VDDIO} (mA)	I_{VDDA} (mA)	I_{VDDD} (mA)	P_{Total} (mW)(1)
DR2K7	40	70	35	500
DR2x2K7	80	140	70	975
DR4K3.5	80	140	70	975
DR4K7	80	140	70	975
DR6K7	120	210	105	1450
DR2x4K7	160	280	140	1925
DR8K7	160	280	140	1925
DR8K3.5	160	280	140	1925
DR2x8K7	320	560	280	3850
DR16K3.5	320	560	280	3850

(1) VDDD = VDDA = VDDIO = 3.3 V, MCLK = 80 MHz.

6 Typical operating characteristics

6.1 Electro-optical characteristics

Table 8: Characteristics of Dragster sensor

Parameter	Value	Remark
Pixel type	Global shutter	Low noise pixel with true CDS
Shutter type	Pipelined global shutter	Exposure of next image during readout of the previous image
Fill factor	100%	
ADC programmable gain	-6dB to 20dB in 256 steps	
ADC resolution	12-bit	
Exposure time range	Minimal 2 µs	
Down time for integration	Minimal 2 µs + 7 MCLK pulses	Depends on the MCLK frequency
Data output	Tap Parallel/LVCMOS TTL	
Trigger delay	1 µs	
Integration & readout	Interleaved or Sequential	
Sensor planarity	30 µm	Invar packaging
	50 µm	Ceramic LCC packaging
Cover glass		AR-coated

Table 9: Sensor characteristics of Dragster 7µm

Parameter	Value	Remark
Pixel size	7 x 7 μm^2	
Pixel pitch x	7 µm	Distance from the center of a pixel to the center of the adjacent pixel (horizontal axis)
Pixel pitch y	7 µm	Distance from the center of a pixel to the center of the adjacent pixel (vertical axis)
Number of special pixels in the most left segment	32 pixels	Single line – 2K7
	2x32 pixels	Dual line – 2x2K7
Maximum line rate	80 kLines/s	2K7
	80 kLines/s	2x2K7 – 2:1 TDI Mode
	160 kLines/s	2x2K7 – Dual Line Mode
Number of output taps	2 per 2K Segment	
	4 per 2x2K Segment	
Configuration interface	Serial 4 Line	1 SPI Interface per 2K Segment

Parameter	Value	Remark
		2 SPI Interfaces per 2x2K7 Segment
Integration control(1)	Asynchronous	With 6 Digital Signals (MCLK, RST_CVC, RST_CDS, Sample, Load_Pulse, N_Reset)

(1) On the dual line sensor version, each line can be triggered individually.

Table 10: Sensor characteristics of Dragster 3.5µm

Parameter	Value	Remark
Pixel size	3.5 x 3.5 µm^2	
Pixel pitch x	3.5 µm	Distance from the center of a pixel to the center of the adjacent pixel (horizontal axis)
Pixel pitch y	7 µm	Distance from the center of a pixel to the center of the adjacent pixel (vertical axis)
Number of special pixels in the most left segment	64 pixels	
Maximum line rate	80 kLines/s	
Number of output taps	4 per 4K pixels segment	
Configuration interface	Serial 4 Line	2 Interfaces for each 4K Pixel Segment
Integration control	Asynchronous	With 6 Digital Signals (MCLK, RST_CVC, RST_CDS, Sample, Load_Pulse, N_Reset)

Table 11: Electro-optical parameter of Dragster 7µm, and 3.5µm, mono version

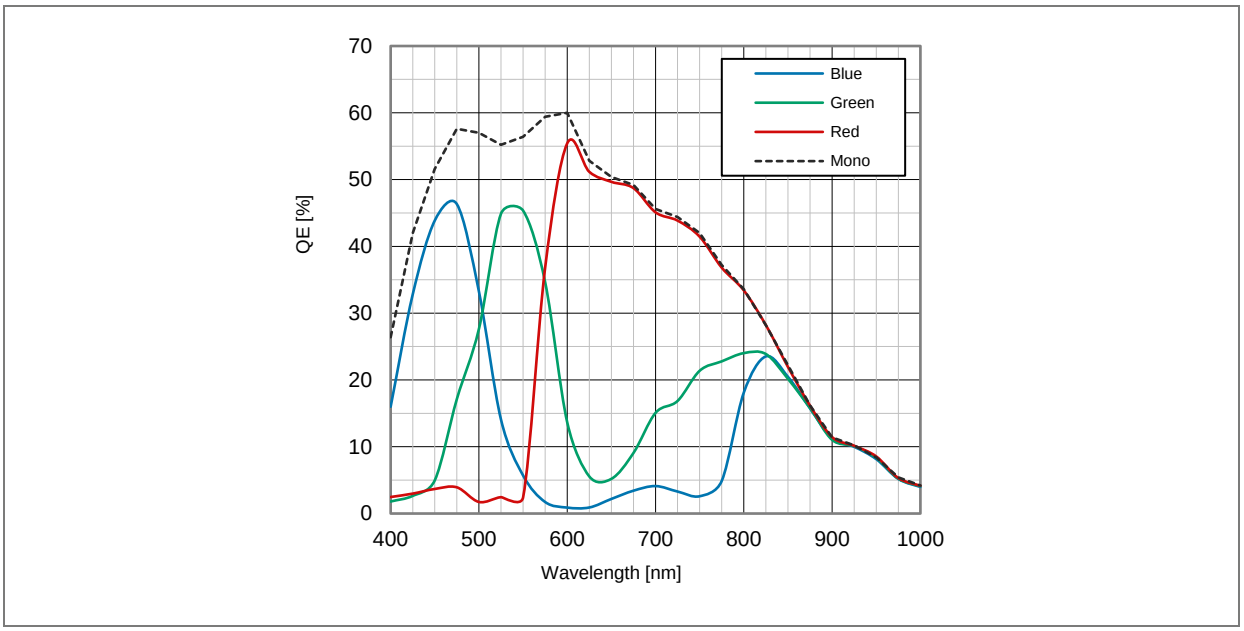
Parameter	7µm	3.5µm	Remark
QE @ 600 nm	60%	60%	
Full well capacity(1)	46ke-	23ke-	
Total system gain	0.076DN/e-	0.152DN/e-	CDS Unit Gain
Responsivity(2)(3)	77DN/nJ/cm^2	38.5DN/nJ/cm^2	CDS Unit Gain @ 12-bit
	308DN/nJ/cm^2	154DN/nJ/cm^2	CDS Gain 4x @ 12-bit
Dynamic range	66.4dB	60.4dB	
SNR	47dB	44dB	
Temporal dark noise(4)(5)	1.7DN	3.3DN	CDS Unit Gain
	22e-	22e-	
Dark current	3 e$^-$/ms	3 e$^-$/ms	@ 27 °C
$DSNU_{rms}$(2)(6)(7)	4DN	4DN	
$PRNU_{rms}$(2)(6)(7)	0.7%	0.7%	
Non linearity(8)	2%	2%	
Image lag	0%	0%	

Parameter	7µm	3.5µm	Remark
Crosstalk	2%	2%	Optical & electrical

(1) At Unity Gain (CDS_{Gain} = 0 -> x1, Inverse ADC Gain = 0x20H, End Counter 128 –> 4096 ADC levels).
(2) T_{int} = 10 µs, Unity Gain (CDS_{Gain} = 0 -> x1, Inverse ADC Gain = 0x20H).
(3) T= 27 °C, T_{int} = 20 µs, Unity Gain (CDS_{Gain} = 1 -> x4, Inverse ADC Gain = 0x20H).
(4) T= 27 °C, T_{int} = 20 µs, Unity Gain (CDS_{Gain} = 0 -> x1, Inverse ADC Gain = 0x20H).
(5) Temporal noise can further be reduced by subtracting from each line the average value of the dark reference pixels, which will reduce temporal noise components coupled over the supply at frequencies below the line rate.
(6) Ramp offset and ramp gain must be adjusted for all segments to match with each other.
(7) Per each 2K7µm and 4K3.5µm segment.
(8) Measured in % deviation from full scale signal for the signal range of 5% - 95%, according to EMVA1288 proposal for linearity measurement.

6.2 Spectral characteristics

Figure 6: Dragster QE(1)



(1) RGB spectral response extrapolated by supplier color filter transmittance data.

7 Functional description

7.1 General sensor description

The Dragster family has 17 variants, which each one them has one or two lines, from one up to four segments, different pixel size, color, package and resolution.

Table 12: Dragster variants

Sensor variant	# of lines	Pixel size (µm)	Chroma	Resolution	Package
DR2K7	1	7x7	Mono	2080x1	INVAR/LCC
DR2x2K7	2	7x7	Mono/RGB	2080x2	INVAR/LCC
DR4K7	1	7x7	Mono	4128x1	INVAR
DR4K3.5	1	3.5x3.5	Mono	4160x1	INVAR/LCC
DR2x4K7	2	7x7	Mono/RGB	4128x2	INVAR
DR6K7	1	7x7	Mono	6176x1	INVAR
DR8K7	1	7x7	Mono	8224x1	INVAR
DR8K3.5	1	3.5x3.5	Mono	8256x1	INVAR
DR2x8K7	2	7x7	Mono/RGB	8224x2	INVAR
DR16K3.5	1	3.5x3.5	Mono	16448x1	INVAR

Sensors with 3.5 µm pixels are structurally identical to sensors with 7 µm pixel. However, for the sensor with 3.5 µm, two independent readout blocks are placed, one on top of the sensor line, which reads out odd pixels and one at the bottom of the sensor line which reads out even pixels. Thus, for sensors with 3.5 µm pixel, two independent segments are always placed together to form a segment with double resolution compared to the segment with 7 µm pixel. The lowest and maximum resolutions for 7 µm pixel are 2K and 2x8K, respectively. Regarding 3.5 µm pixel, the lowest and maximum resolutions are 4K and 16K, respectively.

The first line of the first 2K segment (7 µm) is built of a line of 2080 pixels, having 32 special pixels counting from the left. Similarly, the first 4K segment (3.5 µm) is built of a line of 4160 pixels with 64 special pixels in the beginning. The first 32 (or 64) pixels are used to have a reference for dark current and signal offsets. The remaining 2048 (or 4096) pixels are the light sensitive, responsible for the image effective resolution.

For sensors with multiple segments, the added 2K (7 µm) and 4K (3.5 µm) segments have only 2048 or 4096 sensitive pixels, respectively. Regarding readout, these segments are completely independent. This can be exploited to align the readout of the light sensitive pixels

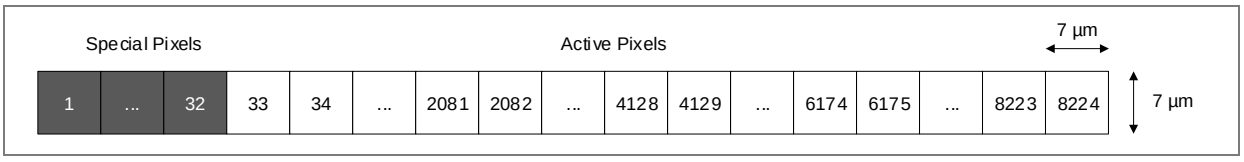
from each segment. To do so, the readout is started in the most left segment 16 pixel clock cycles earlier than the segments farther to the right. The individual start of readout for different segments can also be exploited to reduce the required signal bandwidth by sequentially addressing the SRAM blocks of different 2K/4K segments and multiplexing the data lines.

The sensor features a 13-bit ramp ADC[1] with programmable conversion gain and end of range stage. The on chip digital control circuit generates all necessary control for conversion and the readout modes. However, the readout of a new line can be triggered over an external signal if required. The ADC conversion range (maximum number of bits) can be programmed over the serial interface. Higher conversion range requires longer ADC conversion time.

7.1.1 Placement of pixels

7.1.1.1 DR-XK-7

Figure 7: Placement of pixels sensors with 7 µm pixel pitch (DR8K7)



The first 32 pixels include not only dark pixels but also special pixels like described:

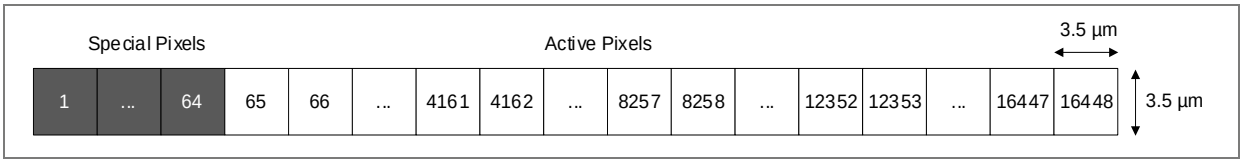
- The output from the first pixel is directly connected to the pad 1.[2]
- The output from the second pixel is directly connected to the pad 21.[2]
- The third pixel is a black pixel, electrically fixed to ADC low saturation.
- The fourth pixel is a white pixel, electrically fixed to ADC high saturation.
- The pixels 5 - 24 are normal pixels however, the photo diode is covered by a metal light shield. They serve as a dark reference. However, at longer wavelengths the metal shield will not completely shield light any more.

[1] It is recommended to only use 12-bit ADC resolution, making use of “Enable Saturation” feature (register CONTROL 1 (0x01), bit 5). For more details, check Section 9.1.1.
[2] These pixels are light sensitive. The respective outputs are connected to a test point on the headboard for debugging purpose in certain package variations.

- The pixels 25 - 32 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used check the validity of the dark pixels 5 - 24, or to compensate for line by line ADC offset variations.

7.1.1.2 DR-XK-3.5

Figure 8: Placement of pixels sensors with 3.5 µm pixel pitch (DR16K3.5)



The first 64 pixels include not only dark pixels but also special pixels like described:

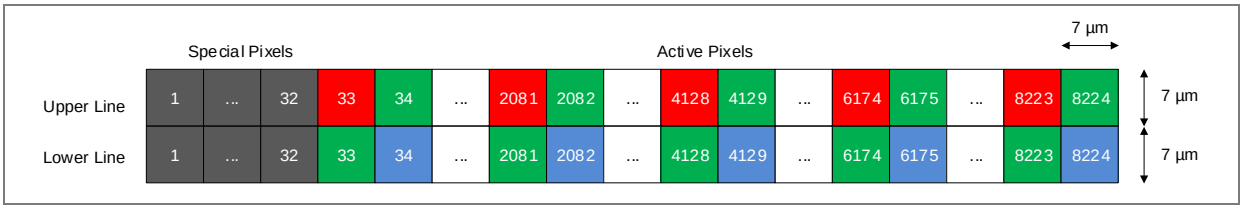
- The output from the first & second pixels are directly connected to the pad 1 of the most left segments on top and bottom.[3]
- The output from the third and fourth pixels are directly connected to the pad 2 of the most left segments on top and bottom.[2]
- The fifth and sixth pixels are a black pixel, electrically fixed to ADC low saturation.
- The seventh and eight pixels are white pixel, electrically fixed to ADC high saturation.
- The pixels 9 - 48 are normal pixels however, the photo diode is covered by a metal light shield. They serve as a dark reference. However at longer wavelengths the metal shield will not completely shield light any more.
- The pixels 49 - 64 are electrical black pixels. In these pixels the photo diode is disconnected electrically from the readout chain. These pixels will follow all analogue and digital offset variations, however not integrate dark current or any photo current. They can be used to check the validity of the dark pixels 9 - 48, or to compensate for line by line ADC offset variations.

[3] These pixels are light sensitive. The respective outputs are connected to a test point on the headboard for debugging purpose in certain package variations.

7.1.2 Color filter arrangement for RGB Dragster versions

On the dual line Dragster there is a possibility to have RGB filters that are organized in both lines as shown in the Figure 9.

Figure 9: Color filter arrangement on Dragster dual line (DR2x8K7)

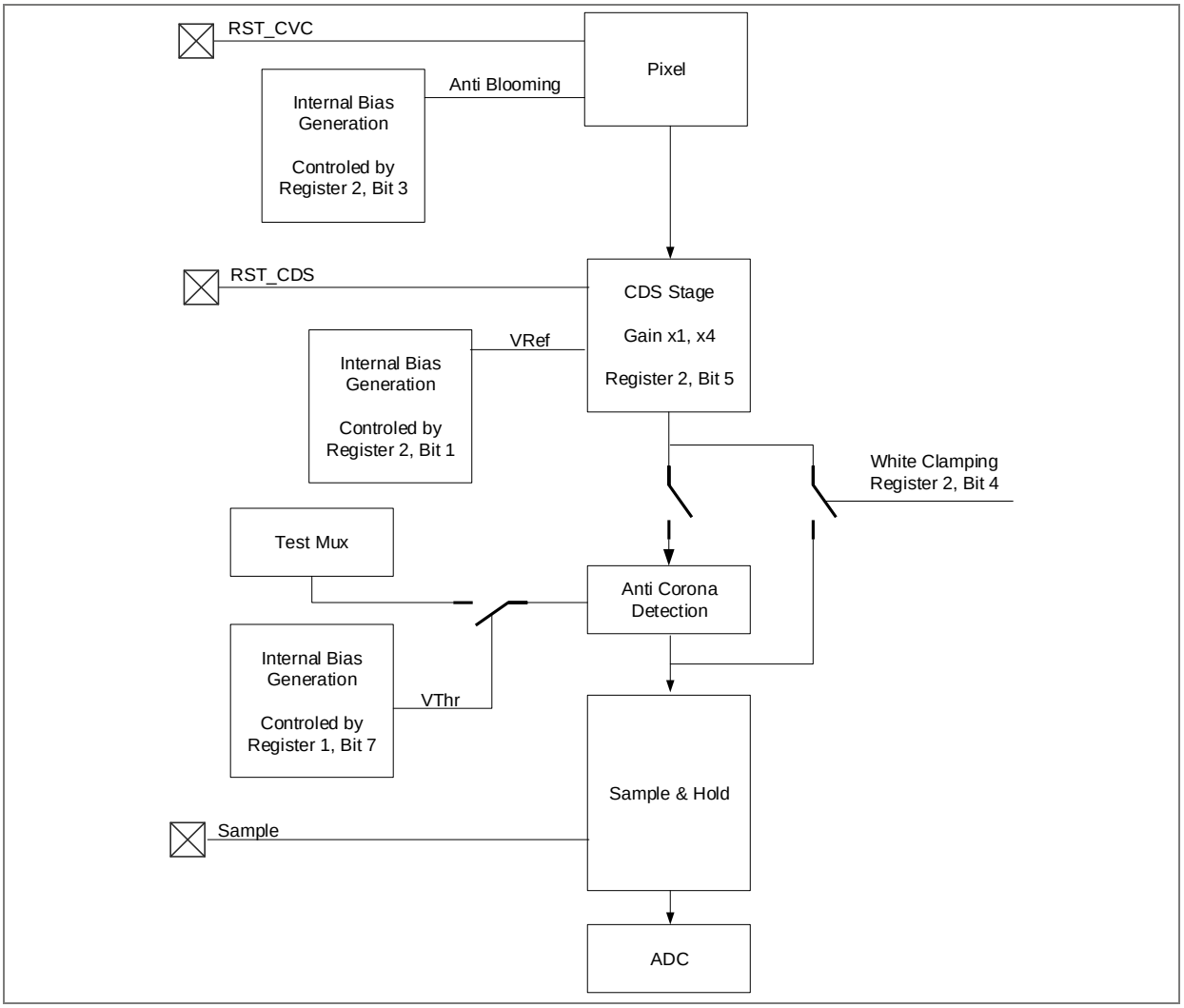


7.2 Description Dragster pixel

The Dragster line scan sensors features a pixel which provides true CDS capability for elimination of reset noise. Other features include programmable analogue gain, anti-blooming and anti-corona circuits that can be activated by register configuration. Each pixel features a programmable 12-bit ADC and memory. Pixels integration, AD conversion and line readout can be made fully pipelined so that line rate is limited by the longest operation and not by the sum of all three.

An overview of the most important blocks of the analogue part and their functionality as well as the register bits which control the features are described below.

Figure 10: Overview of the functional blocks for the analogue part of the pixel



7.2.1 Anti-blooming circuitry

“Blooming” is a phenomenon observed when a single pixel is heavily over exposed and saturates. Photo generated charges then tend to spill in neighboring pixels. This is prevented by an internal circuit, which will drain charges when the pixel is saturated and prevent them from spilling into neighboring pixels. This circuit is controlled by register 0x02 bit '3'. This bit should be set to ‘0’ for most applications, as it grants the largest linear signal range. Under extreme over exposure conditions, this bit can be set to ’1’, which will start draining excessive charges earlier.

7.2.2 Anti-corona circuitry

“Corona effect” is a phenomenon sometimes observed under heavy over exposure condition when the most exposed pixels start to become dark again instead of white. This condition can be detected by a special circuitry and saturated pixels are then clamped to the white reference value before AD conversion. This circuitry can be enabled or bypassed by means of register 0x01 bit '7'. The bit set to ‘0’ will disable the anti-corona circuitry and bypass the signal, while ’1’ will enable it.

7.2.3 Analogue gain

The pixel features a programmable analogue gain of factor x4 at CDS stage level. This gain is controlled by register 0x02 bit '5'. The bit set to ‘0’ unity gain is set and ’1’ sets the gain to x4.

7.2.4 CDS reference generation

The reference voltage for all CDS stages is generated in parallel by the internal bias generation block. The power consumption of the driver to this voltage can be regulated by means of register 0x02 bit '1'. A value of ‘1’ will use an adaptive bias scheme to the buffer for this voltage, which will reduce power consumption when this driver is not used (recommended). A ‘0’ will choose a fixed bias value, which will result in a higher overall consumption.

The reference voltage of the CDS stage is sampled at start of integration for each line, and thus influences the finally digitized analogue value. Any noise on this signal also influences the final signal value as noise will be added equally to all pixels in the line. For ultimate noise performance, it is advised to compute the average of the first dark pixels 16^{th} to 20^{th} and subtract this value from the finally read out pixels for each line. This computation has to be done off chip, but will lead to better noise performance than the one specified.

7.2.5 Analogue voltage references

The analogue voltage references, especially the references to define the ADC start voltage and the ADC gain are interconnected along the sensor line, however remain individual for odd an even pixels in the case of 3.5 µm pixels sensors. Each segment comprises an individual SPI block to configure these voltages. Normally, it is recommended to program the registers controlling an interconnected voltage with the same settings. The figures below illustrate how analogue voltages are interconnected over multiple segments and controlled over the respective SPI interfaces for sensors with 7 µm and 3.5 µm pixel pitch respectively.

Figure 11: Interconnection of ADC reference voltages in case of 7 µm pixel pitch sensors with multiple segments

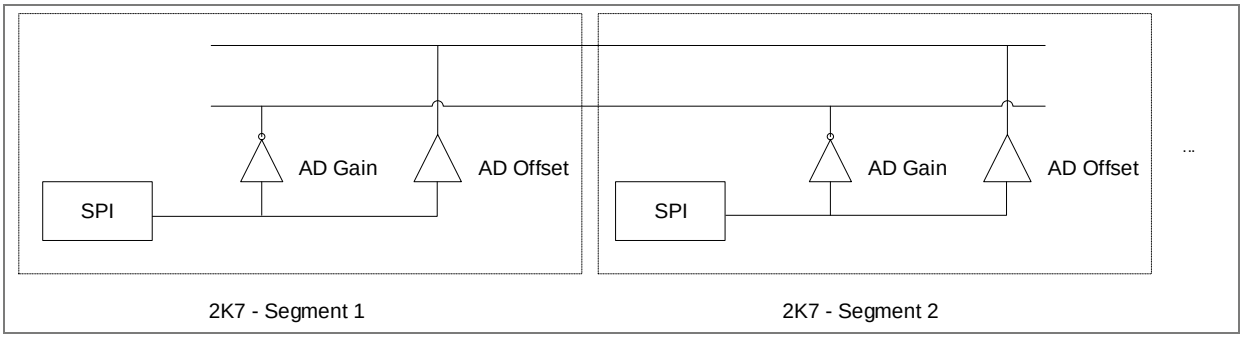
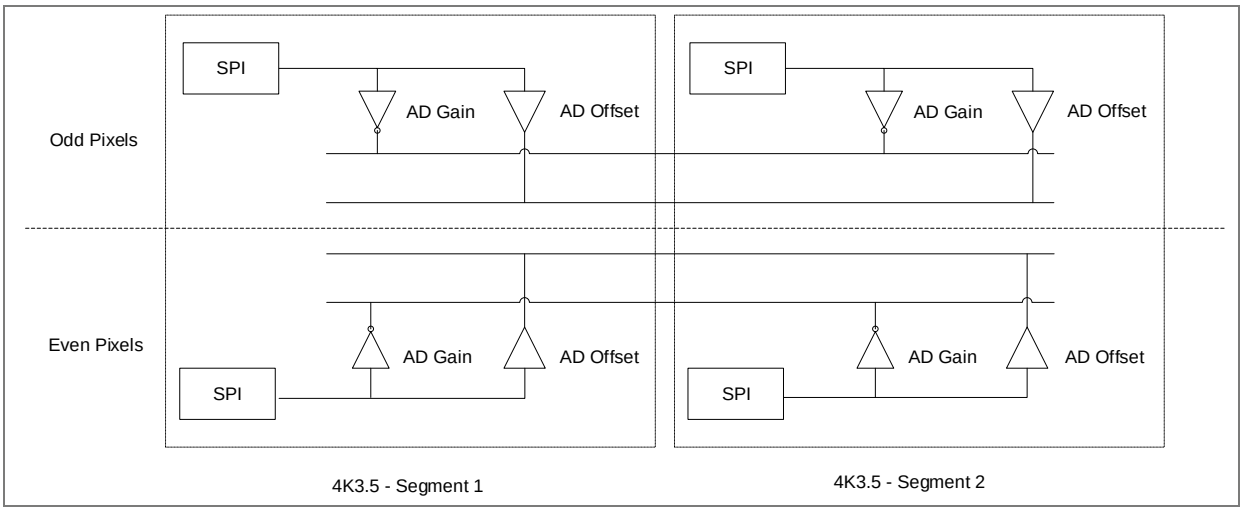


Figure 12: Interconnection of ADC reference voltages in case of 3.5 µm pixel pitch sensors with multiple segments



7.3 Startup sequence

To avoid latch up problems that can create faulty operation points, the correct sequential power on sequence for all devices in INVAR headboard package is:

1. VDDESD
2. VDDA
3. VDD_BULK
4. VDDD

5. VDDIO
6. Ramp up signals on any inputs
7. Release N_RESET_#

If the control overall supplies is not possible, at least care must be taken for the sensor supplies to raise up in the following order:

1. VDDESD
2. VDD_BULK, VDDA, VDDD, VDDIO
3. Ramp up signals on any inputs
4. Release N_RESET_#

For the LCC Ceramic package versions, it is important that VDD ramps prior to any digital input signal.

The Power Off sequence is the inverse order of Power On, for above both situations.

Information: In any condition, the two following situations are to be avoided:

- **Fault A**: Any VDDx is supplied before VDDESD or to a higher value than VDDESD.
- **Fault B**: Digital inputs are supplied prior to supply of VDDESD

7.4 Conversion cycle

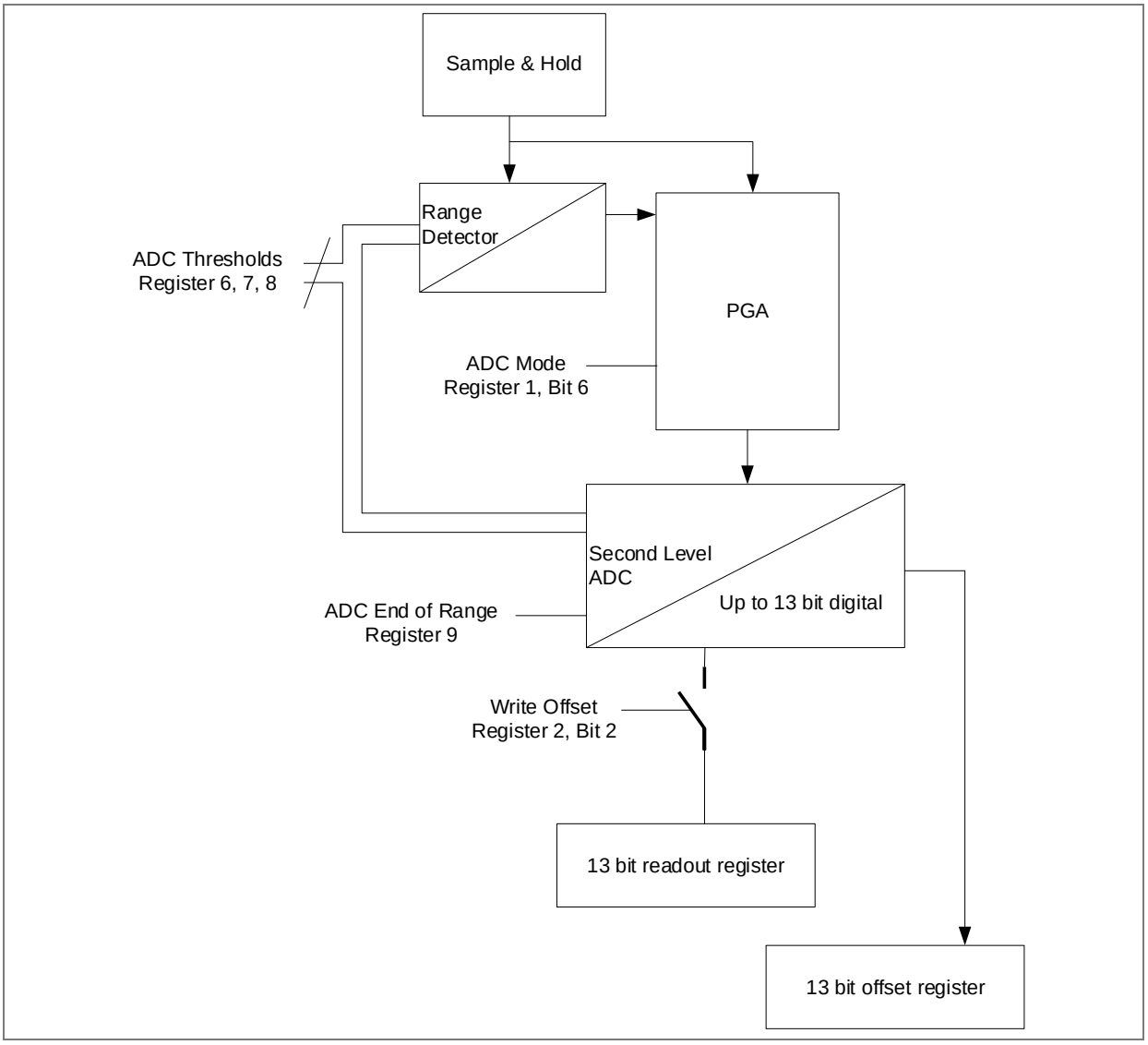
7.4.1 General description

The A/D conversion happens when END_ADC signal is at low state. As soon as sampling stage ends (falling edge of SAMPLE) the END_ADC signal leaves reset state and the sensor starts the A/D conversion.

Each pixel features a multi stage ADC, which minimizes the offset and gain error between individual pixels and segments. The physical block diagram of the ADC and a description of the main functional modes, are given in Figure 13.

For a high resolution, low noise ADC functionality, the ADC is made such that the critical analogue blocks can run at relatively low speed.

Figure 13: Functional block diagram of the pixel level ADC



The ADC features two modes of operation: Linear AD conversion and Companding A/D conversion.

7.4.2 ADC linear mode

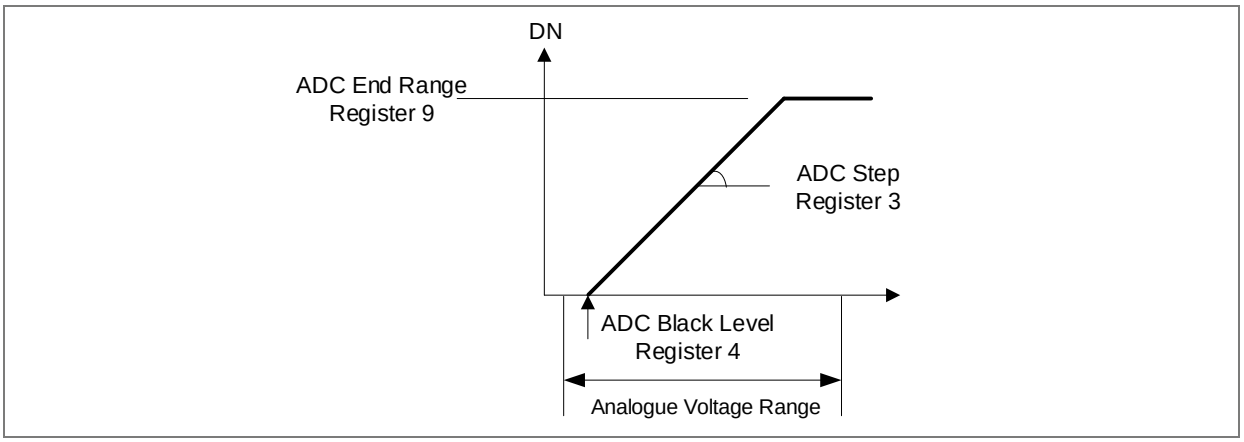
On linear conversion the ADC will require as many clock cycles as the register programmed ADC end of range. Figure 14 shows a diagram of the ADC linear response function and the effect of the different registers on the transfer function.

Information:

It is important to program the end of range according to the pixel data bit width. If digital saturation logic is not enabled in the register 0x01 bit '5', ADC end of range is above 4095 DN and only 12 LSBs are read out, this can create signal “wrap around” artefacts when the pixel value is over 4095 DN.

In order to reduce the ADC conversion time, comparing to readout time and keep the ADC in linear mode, the conversion can be operated at a higher clock frequency than the remaining circuitry. This is done by directly supplying the higher clock frequency to the chip main clock and programming the internal clock divider (register 0x01 bits 1 and 2) such that the clock frequency in chip's readout remains below 50 MHz.

Figure 14: ADC transfer function in linear mode and registers defining the ADC parameters



When in linear mode conversion time (CT) is obtained by the Equation below:

Equation 1:

$$CT = End\ of\ Range\ Register\ \times 32 \times \frac{1}{MCLK}$$

7.4.3 ADC companding mode

An alternative to running the ADC at higher clock rate is to use the ADC companding mode. As for an optical signal, the photon shot noise increases with signal level, a very small quantization step is only required at the very low signal values. For higher impinging optical signals, the ADC quantization step can be increased such as to match the shot noise present

in the light signal. This may significantly reduce the total ADC time required to generate a 12-bit value, while no information is lost. Figure 15 and Figure 16 illustrates the companding ADC mode and the registers involved in programming it is response function.

Figure 15: ADC transfer function in companding mode

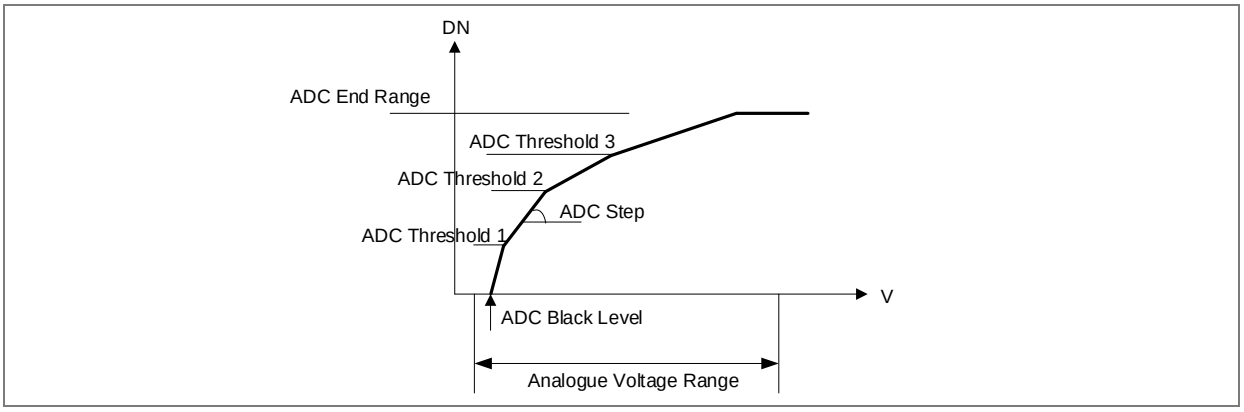
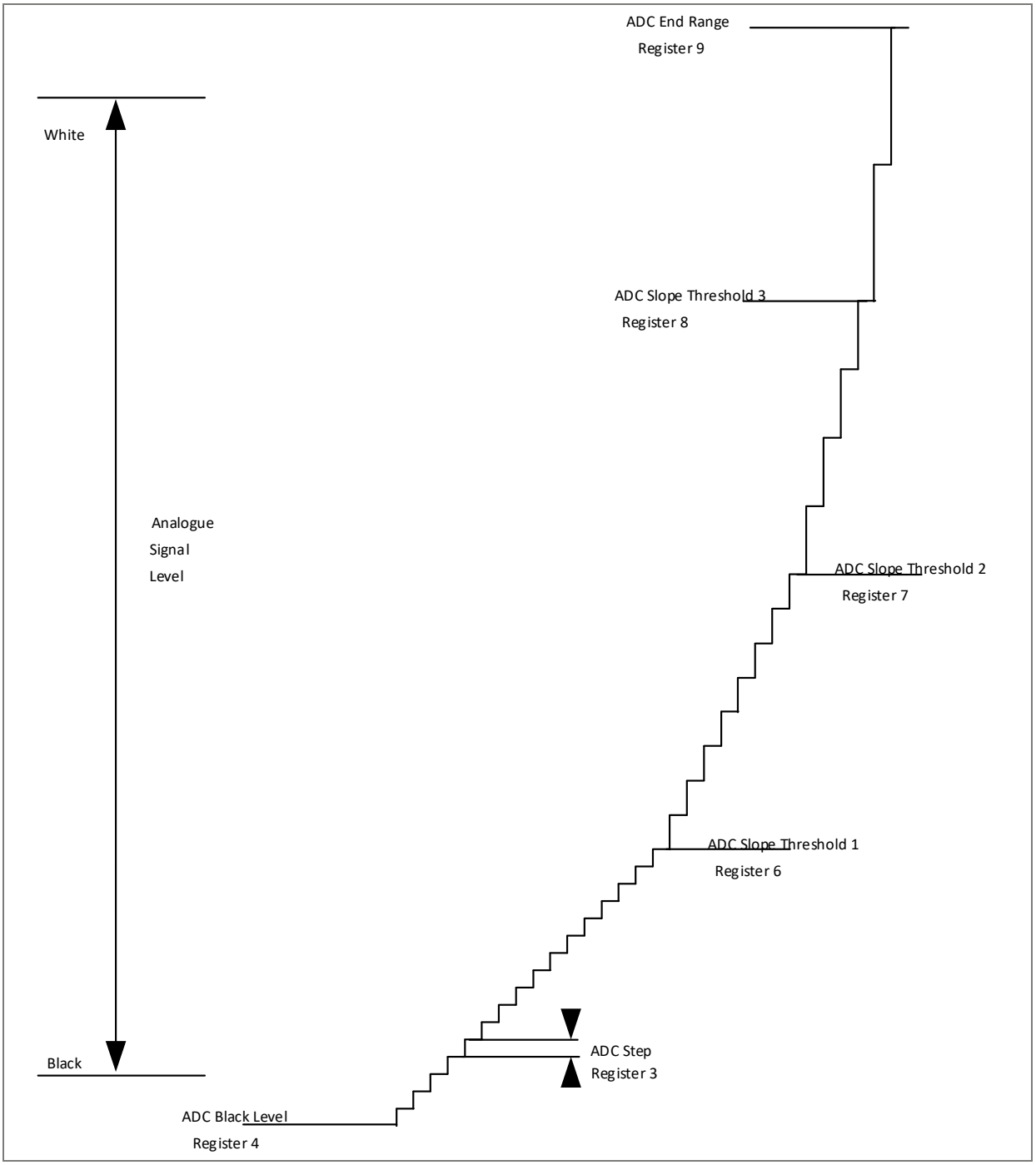


Figure 16: Adaptation of the ADC conversion step in companding ADC mode



When using companding ADC mode, to reduce conversion time it is possible to still produce a linear sensor output by enabling on chip digital re-linearization circuitry (register 0x05 bit '1'). When using on chip re-linearization, the histogram will show missing codes in the range where the ADC was working in companding mode, that can be corrected by enabling on chip dithering (register 0x01 bit '3').

When in companding mode conversion time (CT) is obtained by the Equation 2:

Equation 2:

$$CT = \left[Th1 + \frac{Th2 - Th1}{2} + \frac{Th3 - Th2}{4} + \frac{End_{Range} - Th3}{8}\right] \times 32 \times \frac{1}{MCLK}$$

Information:

When using the ADC in companding mode, it is important to program the three thresholds strictly monotonously increasing, and smaller than the end of range value. Otherwise, the ADC will not function correctly and produce strongly distorted output signals

7.5 Readout cycle

As the pixel level ADC signal is stored in an SRAM bench (LOAD_PULSE rising edge), the digital readout is triggered by LOAD_PULSE falling edge. LOAD_PULSE signal can either be provided externally or be generated internally (register 0x02 bit '0'). This signal must be sent after the end of A/D conversion (rising edge of END_ADC), at the earliest possible time, based on the state of the integration time controlling signals (RST_CVC; RST_CDS, SAMPLE) and the programmed ADC end range. The readout is started from the most left pixel to the right. An LVAL signal is generated to indicate valid pixel data.

Each Dragster variant has a specific number of outputs (taps).

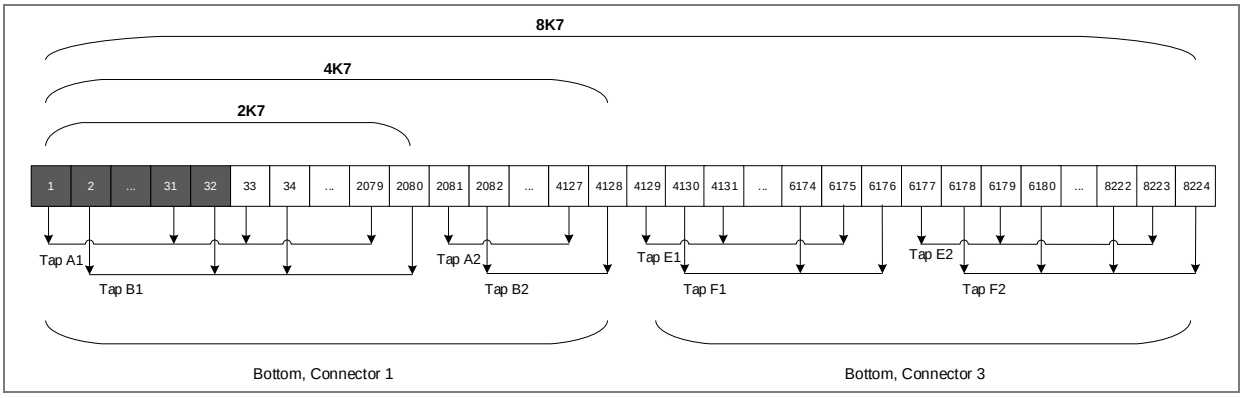
Table 13: Dragster outputs per variant

Sensor variant	# Lines	# Outputs	Outputs	Connectors
DR2K7	1	2	A1, B1	1
DR2x2K7	2	4	A1, B1, C1, D1	1 & 2
DR4K7	1	4	A1, A2, B1, B2	1
DR4K3.5	1	4	A1, B1, C1, D1	1 & 2
DR2x4K7	2	8	A1, A2, B1, B2, C1, C2, D1, D2	1 & 2

Sensor variant	# Lines	# Outputs	Outputs	Connectors
DR6K7	1	6	A1, A2, B1, B2, E1, F1	1 & 2
DR8K7	1	8	A1, A2, B1, B2, E1, E2, F1, F2	1 & 3
DR8K3.5	1	8	A1, A2, B1, B2, C1, C2, D1, D2	1 & 2
DR2x8K7	2	16	A1, A2, B1, B2, C1, C2, D1, D2, E1, E2, F1, F2, G1, G2, H1, H2	1 - 4
DR16K3.5	1	16	A1, A2, B1, B2, C1, C2, D1, D2, E1, E2, F1, F2, G1, G2, H1, H2	1 - 4

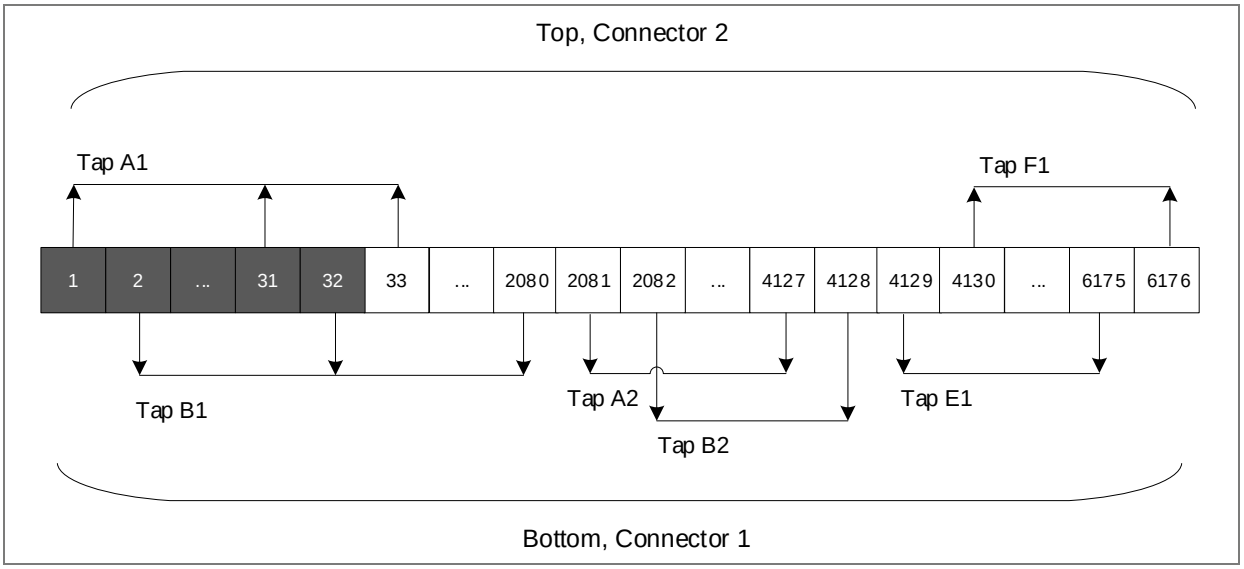
7.5.1 Tap organization DR2K7, DR4K7, DR8K7

Figure 17: Tap organization DR2K7, DR4K7, DR8K7



7.5.2 Tap organization DR6K7

Figure 18: Tap organization DR6K7

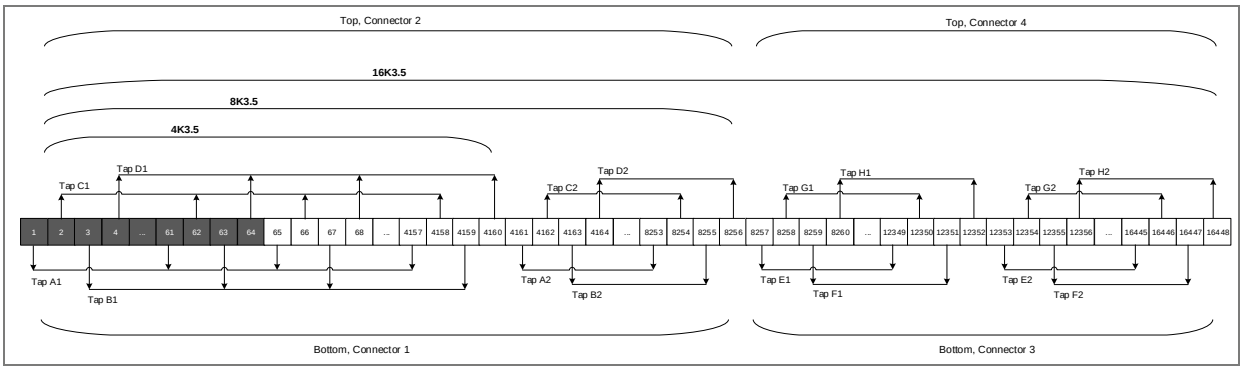


Information:

For the DR6K7, all data taps are 12-bit and not 13-bit like on all other remaining variants.

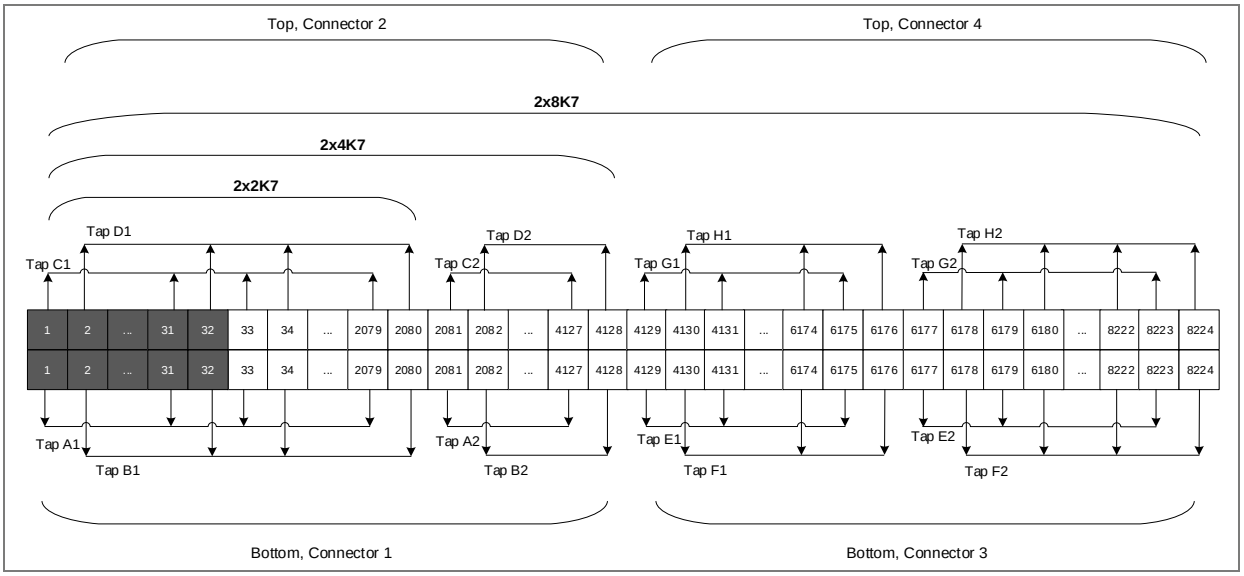
7.5.3 Tap organization DR4K3.5, DR8K3.5, DR16K3.5

Figure 19: Tap organization DR4K3.5, DR8K3.5, DR16K3.5



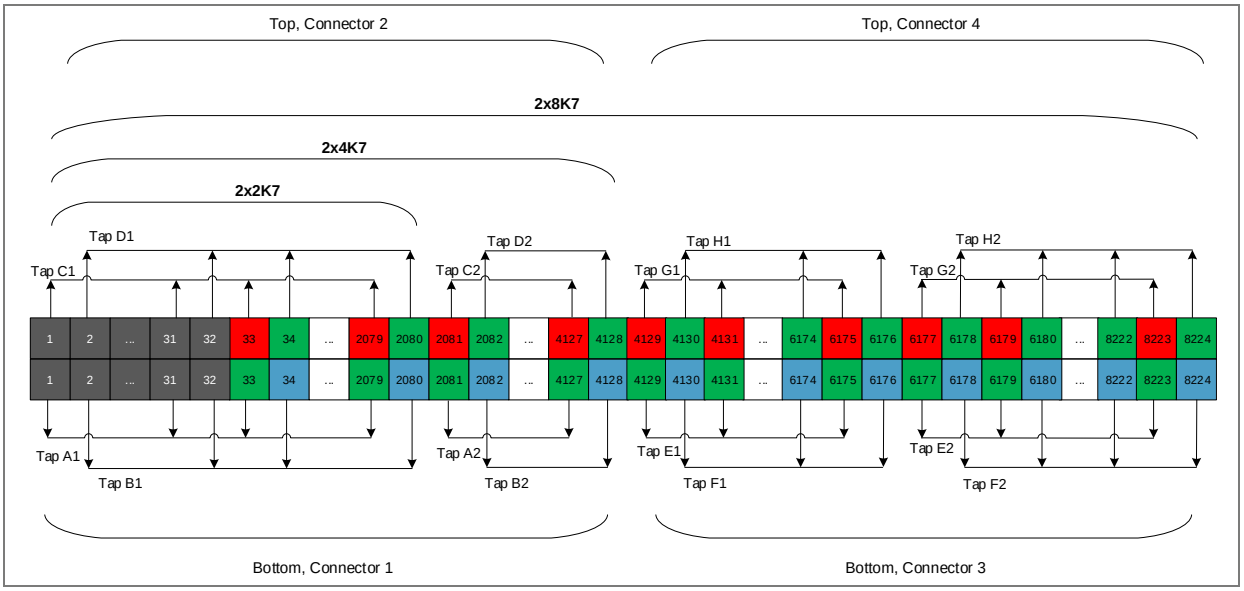
7.5.4 Tap organization DR2x2K7, DR2x4K7, DR2x8K7

Figure 20: Tap organization DR2x2K7, DR2x4K7, DR2x8K7



7.5.5 Tap organization DR2x2K7_RGB, DR2x4K7_RGB, DR2x8K7_RGB

Figure 21: Tap organization DR2x2K7_RGB, DR2x4K7_RGB, DR2x8K7_RGB



7.6 Timings

For proper sensor operation, the digital control signals must set with correct timings. This section shows the recommended Dragster timings.

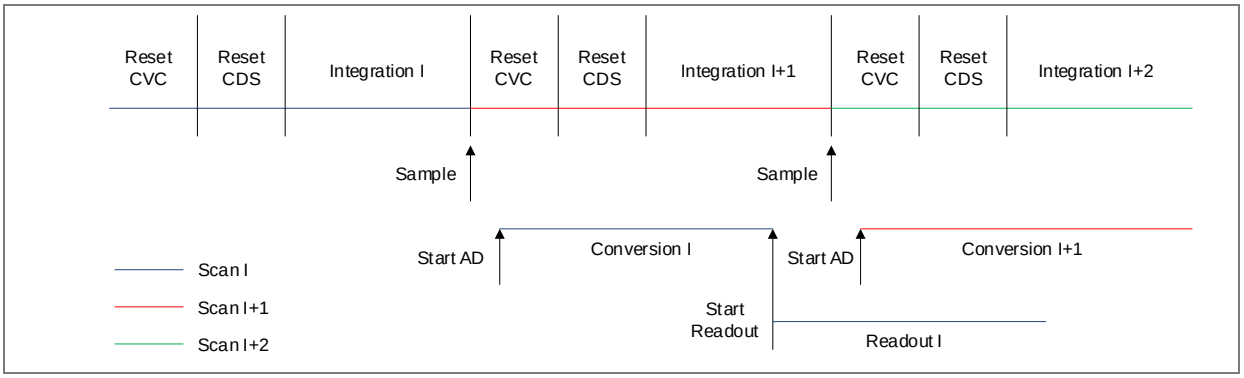
7.6.1 Timing diagram considerations

- When stated a value in time (usually ns or µs), this is a fixed or minimum value (indicated by greater than or equal to symbol (≥)) .
- When stated a time duration in 'X' times MCLK, this is number of clocks that must be respected, independently of the clock frequency.

7.6.2 Dragster interleaved integration timing

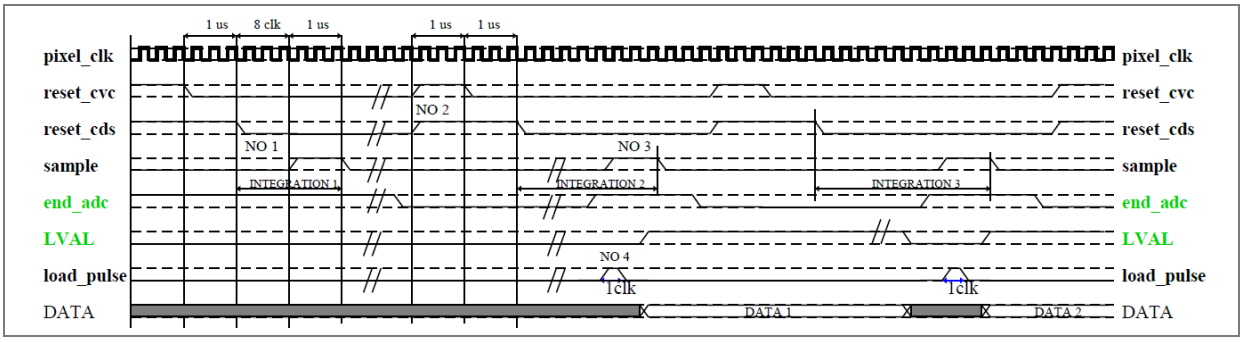
The sensor enables interleaved integration, A/D conversion and readout, where the next integration is performed after the previous one, during A/D conversion and Readout. Therefore, the overall pipeline delay is two minimum line times.

Figure 22: Pipelined integration timing



Below is an example timing for Dragster sensor, when in the interleaved mode.

Figure 23: Dragster interleaved integration timing



Integration - The time between the falling edge of RST_CDS and the falling edge of SAMPLE signal.

NO 1 - To start the integration the user should send the falling edge of RST_CVC and with a delay of 1 µs the falling edge of RST_CDS, only after at least 8 clocks the user can send the raising edge of SAMPLE. However, the rising edge of SAMPLE should never be sent before the end of the active ADC conversion. SAMPLE should be high for at least 1 µs.

NO 2 - The user can send the rising edge of RST_CVC and RST_CDS earliest 7 clocks after falling edge of sample. Please note that 6 clock after falling edge of sample, END_ADC will have its falling edge.

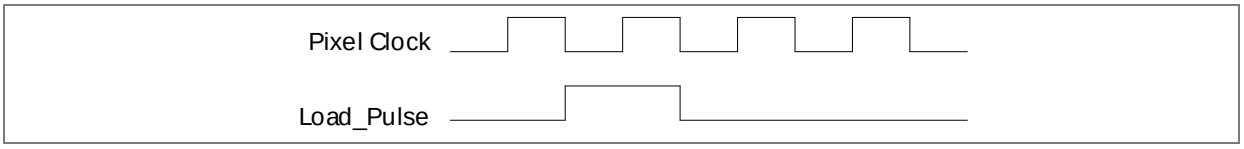
NO 3 - The raising edge of SAMPLE should only be sent if END_ADC is high.

NO 4 - The load pulse should be sent, with at least 4 clocks delayed to the latest event of falling edge of LVAL or rising edge of END_ADC.

The LOAD_PULSE signal is at the sensor side latched with the rising edge of pixel clock, thus the phase in which it is generated must be adjusted such that at the sensor pin. The LOAD_PULSE is high only during one rising edge of pixel clock. For low temperatures (below 10 ºC) it is recommended to use a pulse width of 2 x Pixel Clock period.

In case of problems with stable LVAL generation (no LVAL generated or LVAL signal not with the correct length), please change the phase on which the LOAD_PULSE is generated.

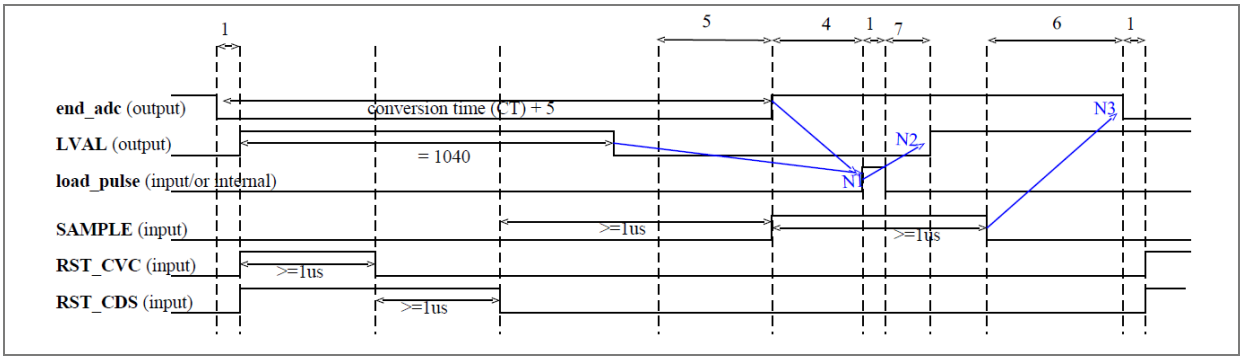
Figure 24: LOAD_PULSE signal generated with correct timing (1)



(1) The drawing signals are indicated, as they are present on the pin of the chip.

Figure 25 shows the detailed pulse timings for each control signal.

Figure 25: Detailed Dragster interleaved integration timing



NO 1 - Rising of load = the latter of (rising edge END_ADC, falling edge LVAL) + 4.

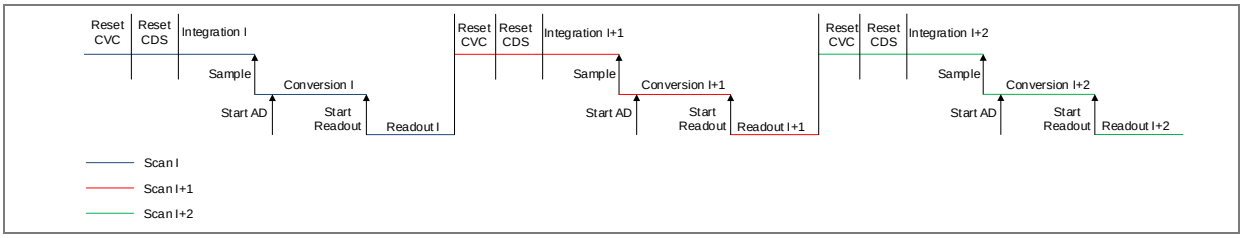
NO 2 - Rising of LVAL = rising edge of LOAD_PULSE + 8.

NO 3 - Falling of END_ADC = falling edge of SAMPLE + 6.

7.6.3 Dragster sequential/pipeline timing

While in Pipeline mode the next integration is performed after the previous one, during A/D conversion and Readout, the Sequential mode, as the name refers, each stage of Integration, A/D conversion and Readout are done sequentially, not in parallel with the other timing stages.

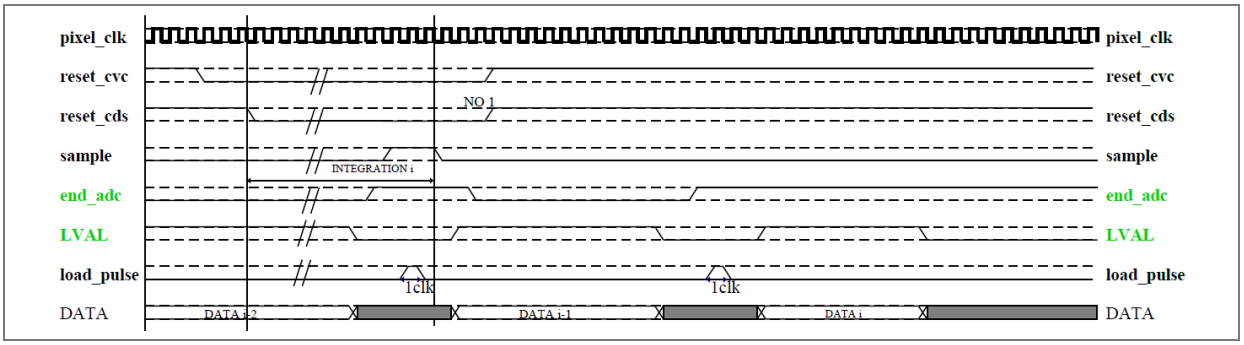
Figure 26: Dragster sequential timings



7.6.4 Dragster idle mode

Below is an example how to put sensor in idle mode.

Figure 27: Timing diagram – end of readout entering idle



NO 1 - To put the sensor in idle mode, the user should send the rising edge of RST_CVC and RST CDS, and keep the signal at high level, as well SAMPLE and LOAD_PULSE signals must stay at low level.

8 Digital interface

The sensor features two different types of control interfaces: SPI interface (using on chip registers) and digital control lines.

8.1 Digital control lines

The digital control lines allows a dynamic control that grant maximum flexibility for readout control operations, CVC control, CDS control and test control signals. Most of these signals changes the logic state during pixel integration and readout that cannot be done using static configuration, due to read and write operation times.

Table 14: Digital control lines

Signal	DIG In/Out	Function
N_RESET	In	Low active global reset signal
RST_CVC	In	Reset signal to CVC block
RST_CDS	In	Reset signal to CDS block
SAMPLE	In	Performs the signal sampling at the ADC input
LOAD_PULSE	In	Starts the readout of last converted line
END_ADC	Out	Indication from counter being in reset
LVAL	Out	When at high informs that the line data is valid

8.2 Serial 4-wire configuration interface

8.2.1 General description

The SPI interface controls static configuration data, such as operation modes, ADC gain, black level and other special features. It is present in every segment, top and bottom sides. This interface is based on 8-bit registers and addressed using 8-bit addresses.

The interface uses the following signals:

Table 15: SPI signals

Signal	DIG In/Out	Function
MISO	Out	Master In, Slave Out
MOSI	In	Master Out, Slave In
N_CS	In	Low active chip select
SCLK	In	Serial interface clock

For access to the internal registers of the sensor, a serial interface with four wires are implemented. The interface consists in four different lines, one clock line (SCLK), one receive (MOSI) and transmit (MISO) line which are synchronous to each other. The fourth line is the chip select (N_CS) and must be low to send/receive data through the lines. The sensor is always slave in the application. By the use of the N_CS signal, the master can activate the serial interface of an individual segment or several segments together. The bus frequency range is from DC to 20 MHz, but must always be lower than MCLK/2.

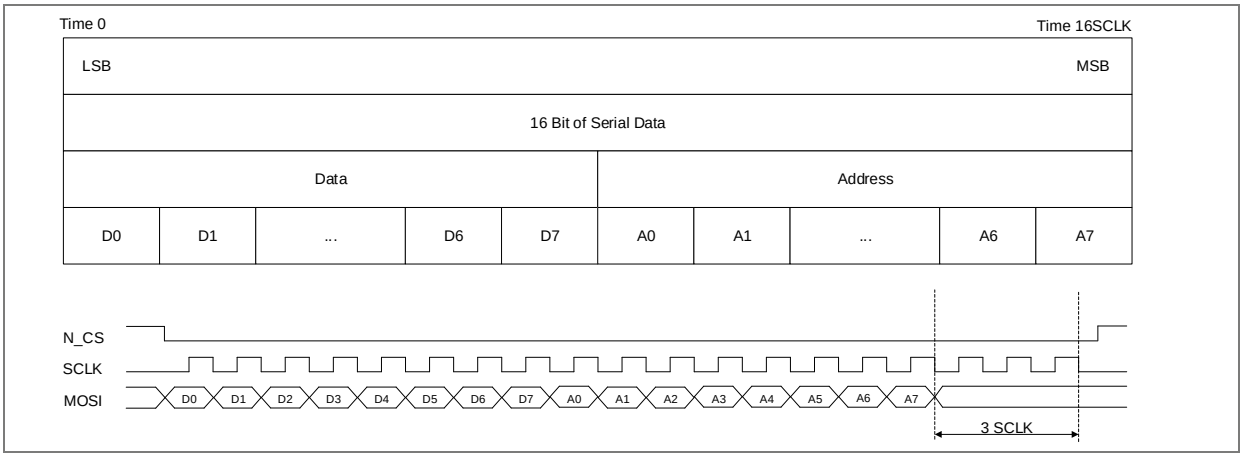
8.2.2 Writing operation

The writing operation is performed by sending the word containing the data and the address. No acknowledge signal or indication is given back.

The data is sent from LSB to MSB. The command word has a length of 16 bits and contains the data of the register and the register address. It is possible to write multiple registers consecutively, sending data and address each 16 SCLK. After the last written word, the SCLK should be sent for minimum of two extra clocks, (maximum 4 SCLK) while N_CS is still low.

The updating to the registers is performed after update request bit is sent at the next rising edge of END_ADC signal. The last word sent to the registers has to be always to register 0x01 and containing the update request bit, otherwise the update is not performed.

Figure 28: Writing operation

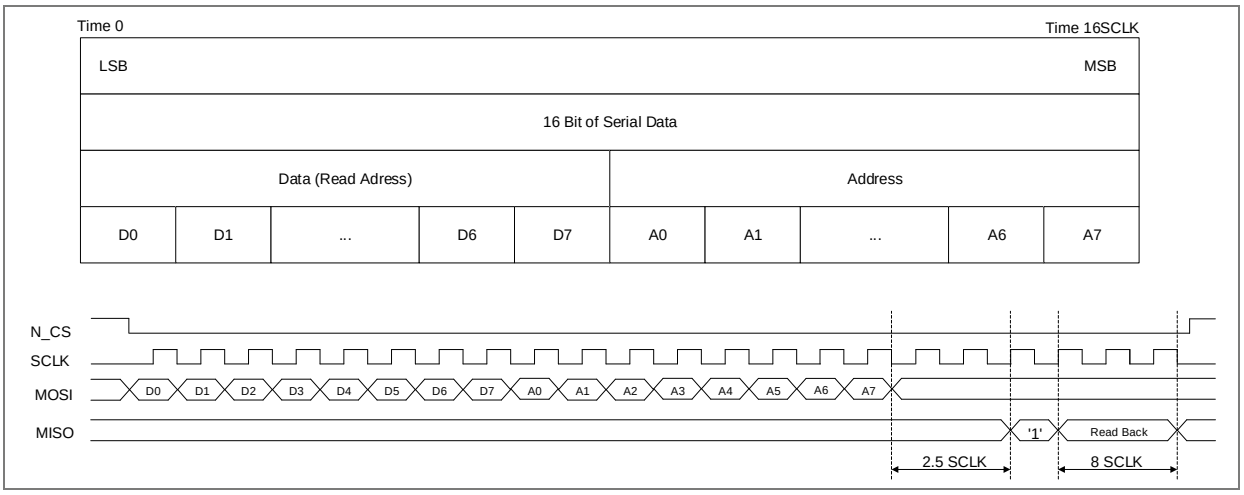


8.2.3 Reading operation

To perform a read operation, the address for the register to be read, has to be written on register 0x15 (as data). After two and half SCLKs relative to the last MOSI bit (A7), the MISO line will send a leading ‘1’, followed by the 8-bit output data (LSB to MSB).

It is only possible to read one register at a time, but it is possible to perform consecutive reads from the same segment and register. The raise of N_CS signal can be made right after the complete read of the last bit and SCLK should be placed on hold.

Figure 29: Reading operation



9 Register description

Every internal status of the sensor will be controlled by the serial interface and be written to the internal registers. All registers are 8-bit oriented. The unused bits on a register are set to zero and reserved for future use.

9.1 Detailed register description

9.1.1 Control register 1 (Address 0x01)

Table 16: Control register 1

Address: 0x01		Default value: 0xA8	Access: Read/Write
Bit	**Bit name**	**Default value**	**Bit description**
7:7	V_{Thr} Bit	1b	Set to '0' - For test purposes only. Do not use. Set to '1' - The threshold voltage for the white clamping is given internally.
6:6	ADC Mode Bit	0b	Set to '0' - Linear ADC conversion is used. Set to '1' - Companding ADC conversion is used.
5:5	Enable Saturation(1)(2)	1b	Set to '0' - The digital saturation is not enabled, so the output will cover full 13-bit. If 12 bits are read out "wrap around" error may occur if End ADC range is not properly configured. Set to '1' - Digital saturation is enabled, the output will be saturated to the 12 LSB's (4095 DN).
4:4	Offset Subtraction(3)	0b	Set to '0' - The digital offset is not subtracted from the read value. Set to '1' - The value stored in the offset register is subtracted from the readout signal.
3:3	Dithering	1b	Set to '0' - Dithering deactivated (for ADC linear mode). Set to '1' - Dithering activated (noise generated for ADC). This bit enables the on chip dithering logic to avoid missing codes in the output histogram when on chip re-linearization is used in combination with companding ADC mode.
2:2	Clock Division 2	0b	These bits are responsible for the definition of readout clock (pixel clock), the different values are presented in Table 17.
1:1	Clock Division 1	0b	

Address: 0x01		Default value: 0xA8	Access: Read/Write
Bit	**Bit name**	**Default value**	**Bit description**
0:0	Update Request	0b	In order to activate a set of new register values uploaded over SPI, this bit has to be set to 1. Register data does not change unless this bit was set to 1 and a rising edge of End ADC occurred. When this bit is set, at the next rising edge of End ADC signal the register values are updated.

(1) The 13th bit should be ignored if on chip saturation is enabled, it holds an overflow identification flag in this case.
(2) It is recommended to configure ADC resolution to 12bits, enable saturation set to '1' and End of Range Register (register 0x09) to 0x80H, which allows for an output of 4095DN.
(3) The digital subtraction feature enabled (bit set to '1') is not recommended, creating artifacts in the image. Still, if using this feature, the bit 2 in Control Register 3 (register 0x05) "Enable Offset SRAM" must be set to '1', at user's responsibility.

Table 17: Clock division

Bit 2	Bit 1	Description
0	0	Readout clock set to MCLK
0	1	Readout clock set to MCLK/2 ADC CLK remains at MCLK
1	0	Readout clock set to MCLK/4 ADC CLK remains at MCLK
1	1	Do not use, clock not generated

9.1.2 Control register 2 (Address 0x02)

Table 18: Control register 2

Address: 0x02		Default value: 0x12	Access: Read/Write
Bit	**Bit name**	**Default value**	**Bit description**
7:6	N/A	00b	Not used
5:5	Analogue Gain	0b	Set to '0' – No analogue gain (x1) in the CDS. Set to '1' – Analogue gain (x4) in the CDS.
4:4	Enable White Clamping (Anti-Corona)	1b	Set to '0' – The white clamp is not active. Set to '1' – The clamping of white values set. White clamp is used to avoid contrast inversion of heavily over exposed scenes (corona effect)

Address: 0x02		Default value: 0x12	Access: Read/Write
Bit	**Bit name**	**Default value**	**Bit description**
3:3	Enable Anti-Blooming(1)	0b	Set to '0' – Additional anti blooming feature OFF. Set to '1' – Additional anti blooming feature ON.
2:2	White Offset(2)	0b	Set to '0' – Not active, values of the A/D conversion go to the readout registers. Set to '1' – When active, a new value is written to the offset registers.
1:1	Enable Control V_{Ref}	1b	Set to '0' – V_{Ref} buffer bias is in constant power mode. Set to '1' – V_{Ref} buffer bias in low power mode (recommended).
0:0	Auto Gen Load Pulse	0b	Set to '0' – The pulse for readout has to be provided externally. Set to '1' – The pulse for readout is generated internally, immediately after completed AD conversion and once the LVAL of the previous line readout is back to zero. Multiple readouts of the same data occur if no new A/D conversion has been started after finalization of the line readout.

(1) The pixels inherent anti-blooming structures will under normal conditions prevent any kind of blooming. Only under the most extreme over exposure condition, this additional anti-blooming circuitry may be required.
(2) Feature related to digital subtraction, which is not recommended to be set to ‘1’. Still, if using this feature, the bit 2 in Control Register 3 (register 0x05) "Enable Offset SRAM" must be set to ‘1’, at user’s responsibility.

9.1.3 Inversed ADC gain register (Address 0x03)

Table 19: Inversed ADC gain register

Address: 0x03		Default value: 0x1D	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	Inversed ADC Gain Register	00011101b	Responsible for ADC conversion gain. Respectively the ADC conversion step. The register is proportional to the voltage step required for 1 DN. Higher value on this register, results in a lower ADC gain (higher voltage step for 1 DN).

9.1.4 Offset register (Address 0x04)

Table 20: Offset register

Address: 0x04		Default value: 0xC8	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	Offset Register	11001000b	Responsible for ADC black level offset. The lower the value of the offset register the closer the output signal will be to the white level, with the increasing of the register value the output signal will become more black.

9.1.5 Control register 3 (Address 0x05)

Table 21: Control Register 3

Address: 0x05		Default value: 0x12	Access: Read/Write
Bit	**Bit name**	**Default value**	**Bit description**
7:6	N/A	00b	Not used
5:3	Bandgap Switch	010b	These bits can be used to trim the reference current generated by the bandgap circuit of different segments. The bits configuration is shown in Table 22.
2:2	Enable Offset SRAM(1)	0b	Set to '0' – Offset SRAM is powered down. Stored offset values are lost. Set to '1' – Offset SRAM is enabled.
1:1	Re-linearization	1b	Set to '0' – In companding ADC mode the piece wise linear compressed data is given out. Set to '1' – When using the companding ADC mode, the compressed data is re-linearized on chip to a linear 12 bits representation. It is recommended to use dithering (control register 0x01 bit 3) together with this feature to avoid missing codes in the output signal.
0:0	Pixel Clock Output Enable	0b	Set to '0' – The pixel clock pad is in tristate mode. No pixel clock in given out. Set to '1' – The pixel clock is provided to the user on the pad.

(1) Feature related to digital subtraction, which is not recommended to be set to ‘1’. Still, if using this feature, it is at user’s responsibility.

Table 22: Bandgap switch

Bit 5	Bit 4	Bit 3	Relative current to nominal(1)
0	0	0	132%
0	0	1	77%
0	**1**	**0**	**100%**
0	1	1	64%
1	0	0	112%
1	0	1	70%
1	1	0	86%
1	1	1	59%

(1) The generated reference current can be observed at the TEST_MUX output pins. The target is 100 µA. These bits can be used to tune the general reference back to target values, in case production parameters spread leads to strong deviation. Further these bits can be used to reduce overall power consumption, though the reference voltages, (namely ADC zero reference will drift from target values) and may have to be over driven to get proper operation at lower overall current. (Register 0x0A, channel 0x0F).

9.1.6 Threshold register 1 (Address 0x06)

Table 23: Threshold register 1

Address: 0x06		Default value: 0x01	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	Threshold Register 1	00000001b	This register is responsible for holding the value for the first ADC threshold in companding mode. The register content is multiplied by 32.

9.1.7 Threshold register 2 (Address 0x07)

Table 24: Threshold register 2

Address: 0x07		Default value: 0x06	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	Threshold Register 2	00000110b	This register is responsible for holding the value for the second ADC threshold in companding mode. The register content is multiplied by 32.

9.1.8 Threshold register 3 (Address 0x08)

Table 25: Threshold register 3

Address: 0x08		Default value: 0x6D	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	Threshold Register 3	01101101b	This register is responsible for holding the value for the third ADC threshold in companding mode. The register content is multiplied by 32.

9.1.9 End of range register (Address 0x09)

Table 26: End of range register

Address: 0x09		Default value: 0x7F	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	End of Range Register	01111111b	This register is responsible for holding the value to configure the end of the ADC range (the highest digital value computed by the ADC). The register holds the 8 MSB's of a 13-bit value (the 5 LSB's are set by hard wiring to zero). The time in master clock cycles the ADC requires for a conversion equals the value in this register multiplied by 32. Use this register to choose between 10-bit, 11-bit, 12-bit ADC resolution. The ADC resolution trades versus the ADC conversion time. Higher resolution thus requires longer line periods, or the ADC to be run at higher clock frequency.

9.1.10 Test multiplexer register (Address 0x0A)

Table 27: Test multiplexer Register

Address: 0x0A		Default value: 0x00(1)	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:7	hv_3	0b	This register is responsible for holding the value to configure the test multiplexer. It defines the channel (Table 28) that will select as output for the test multiplexer.
6:6	hv_2	0b	
5:5	hv_1	0b	
4:4	hv_0	0b	
3:3	Test_3	0b	
2:2	Test_2	1b	
1:1	Test_1	1b	
0:0	Test_0	0b	

(1) It is recommended to write value 0x0F which helps to stabilize V_{Ref} for the chip and reducing significantly line by line offset noise.

Table 28: Test multiplexer channels

Channel	Signal	Comment
0x00	VSS	Reset default
0x01	V_{bg}	Internal bandgap reference voltage
0x02	Bias_V_{Ref}	Bias reference of on chip CDS reference buffer
0x03	GND_RST_CVC	Anti-blooming reference voltage
0x04	PCAS_CDS	Internal reference voltage
0x05	NCAS_CDS	Internal reference voltage
0x06	V_{Bias}_CDS	Internal reference voltage
0x07	V_{Bias}_White_Clamp	Internal reference voltage
0x08	V_{Thr}	Threshold voltage for saturation detection
0x09	V_{Bias}_CVC	Internal reference voltage
0x0A	I_{Ref}	Current output (measure towards VSS) for internal bias generation. The target value is 100 µA
0x0B	V_{Bias}_Comp_1	Internal reference voltage
0x0C	RST_CVC	Monitor of digital control signal RST_CVC
0x0D	V_{RST}	Internal reference voltage
0x0E	Rmp	Internal reference voltage
0x0F	ADC_Reference	Reference voltage for ADC zero level. Can be overdriven. Additional decoupling on this signal may improve noise performance.

9.1.11 Read request register (Address 0x0F)

Table 29: Read request register

Address: 0x0F		Default value: 0x00	Access: Read/Write
Bit	**Bit name**	**Default**	**Bit description**
7:0	Address to Read	00000000b	Defines the register address to be read in a read back operation over SPI interface.

9.2 Register mapping overview

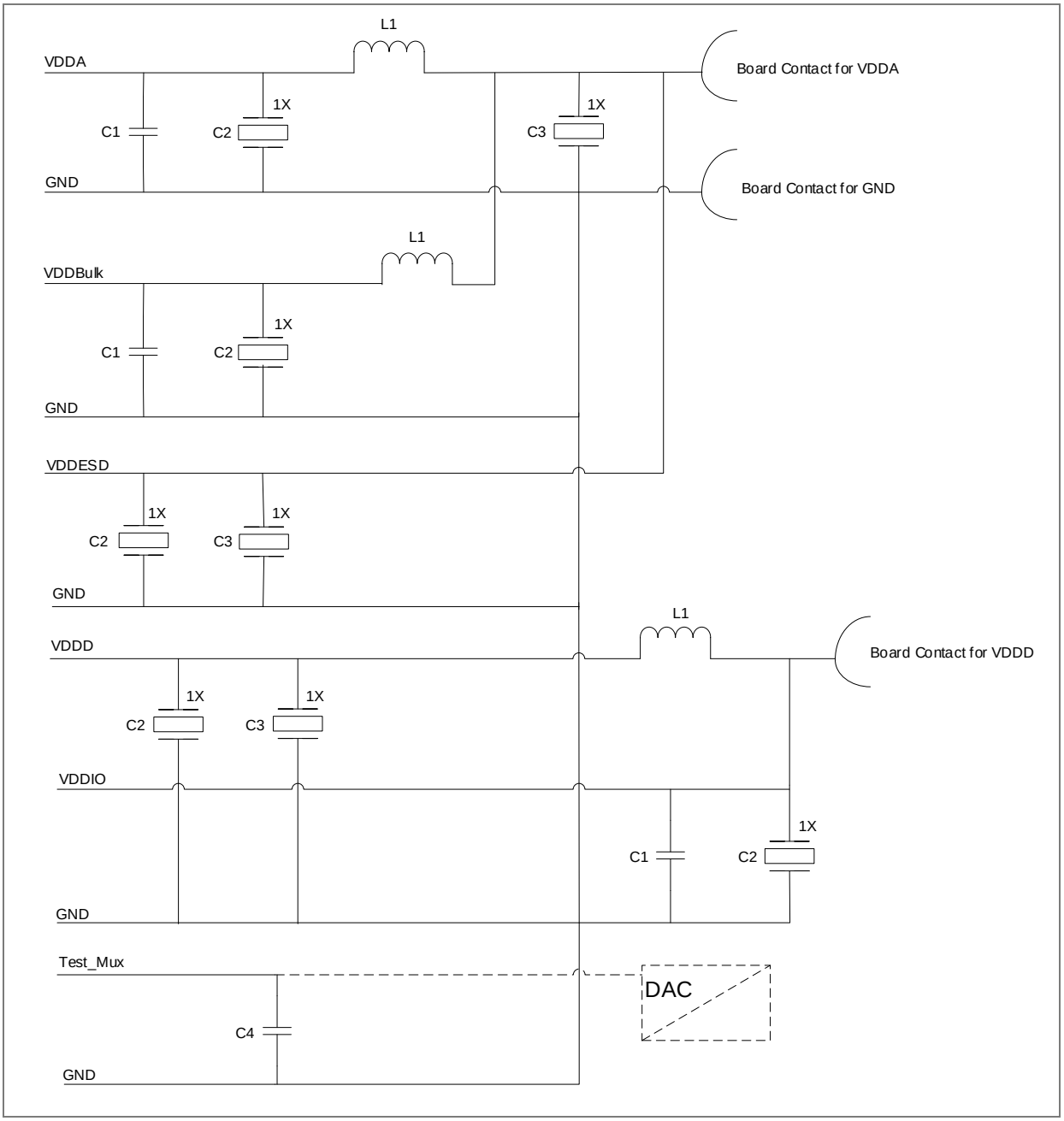
Table 30: Default sensor register setting

Address	Register ID and description	Default value
0x01	Control register 1 – Holds several configuration bits	0xA8
0x02	Control register 2 – Holds several configuration bits	0x12
0x03	Inverse ADC Gain – Sets the analogue gain (step size of ADC)	0x1D
0x04	Offset – Sets the black level reference for the ADC	0xC8
0x05	Control register 1 – Holds several configuration bits	0x12
0x06	Threshold register 1 – Sets the first knee point for companding ADC mode	0x01
0x07	Threshold register 2 – Sets the second knee point for companding ADC mode	0x06
0x08	Threshold register 3 – Sets the third knee point for for companding ADC mode	0x6D
0x09	End of range – Sets the end of range for the ADC (highest ADC code & ADC conversion time)	0x7F
0x0A	Test multiplexer – Sets the output of test multiplexer to the test analogue pad	0x00
0x0F	Read Request – Defines the register address to be read in a read back operation over SPI interface	0x00

10 Application information

10.1 External components

Figure 30: Recommended power supply strategy for the sensor headboard



Information:

Please note that in the above image the component DAC is optional.

Table 31: Recommended values for capacitors and inductances

Component	Description	Nominal value	Tolerance	Voltage range
C_1	Power decoupling capacitor, close to each VDDx connector pin Low ESR Ceramic	10 nF	±25%	>3.6 V
C_2	Power decoupling capacitor, placed one time per power supply Tantalum type	10 µF	±25%	>3.6 V
C_3	Power decoupling capacitor, placed one time per power supply Tantalum type	100 µF	±25%	>3.6 V
L_1	Power decoupling inductance	10 nH	±25%	Dimension according power consumption of respective sensor variation
C_4	Additional decoupling capacitor on the outputs of Test_Mux(1)	100 nF	±25%	>3.6 V

(1) If the Test_Mux_# signals are accessible an additional capacitance should be placed in this signal and then by writing on register 0x0A with the value 0x0F the line by line offset noise is reduced significantly.

If added an external DAC, the circuit schematic to be used is shown in Figure 31. If the Test_Mux_# signals are accessible, this option allows to set the ADC offset (black reference) in more fine steps and possibly, with better temperature stability. In order to perform this operation, the Test_Mux_# outputs should be connected and the value 0x0F should be written to register 0x0A in all segments. Also, make sure the DAC output impedance is higher than 200 kΩ. On chip there is an 8-bit resolution DAC for this purpose, but an external DAC can provide benefit if more fine adjustment steps are required.

For sensors with 3.5 µm pixel and dual line sensors, once there are individual SPI blocks, it is recommended to connect a DAC for top (DAC1) and bottom (DAC2) side separately, though is not mandatory. Once the individual DAC offsets are equalized over the external connection, the black level can be adjusted by writing the same value to the registers on each segment.

Figure 31: External components for the option to control the ADC offset by an external DAC for the case of a sensor with four segments

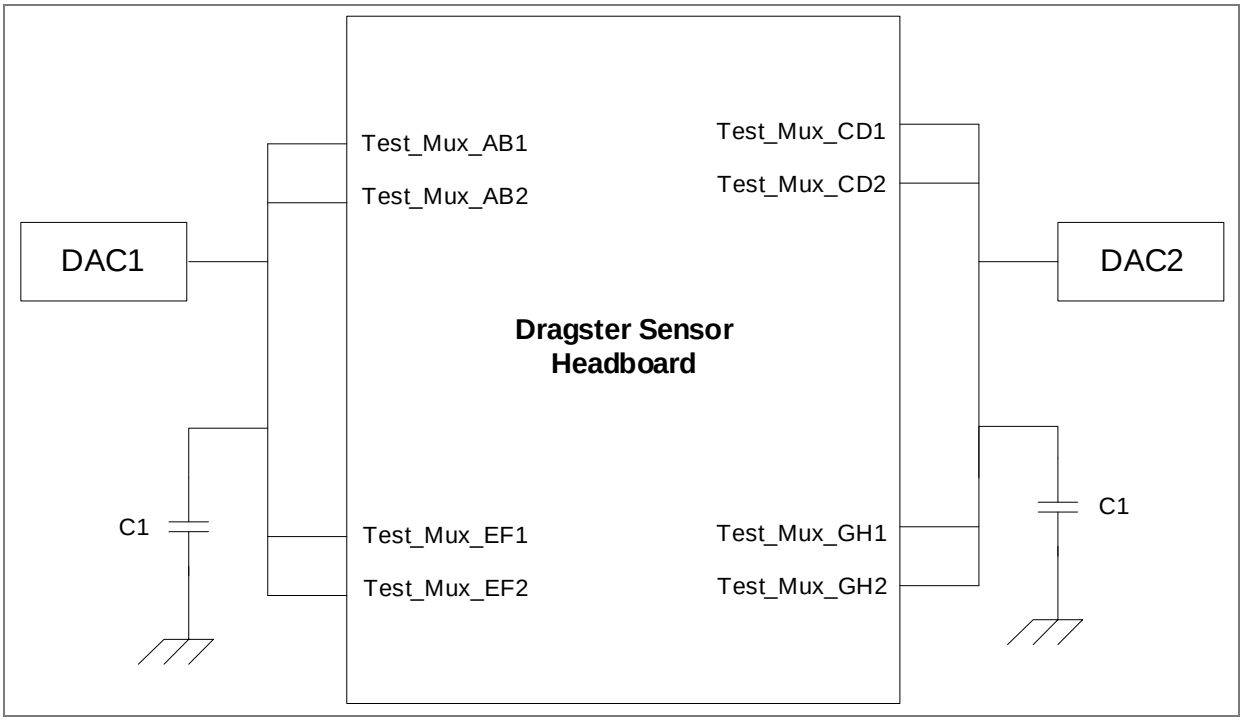


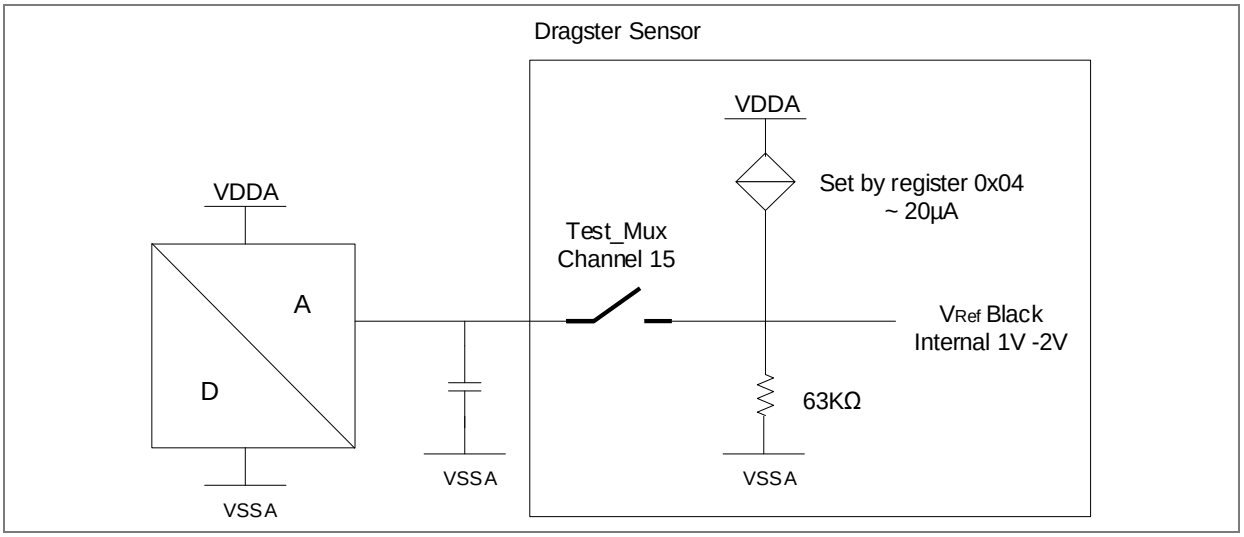
Table 32: Optional external components

Component	Description	Nominal value	Tolerance	Voltage range
DAC1/DAC2	Optional additional DAC on outputs of Test_Mux	1 V-2.5 V (or wider)	Output resistance <1 kΩ V_{Noise_rms} < 0.5 mV	>3.6 V
C_1	Optional decoupling capacitor Low ESR Ceramic	100 nF	±25%	>3.3 V

In order to adjust the ADC black reference an external reference voltage is supplied via the DAC where lowering the voltages shifts the output signal to higher digital values.

Figure 32 illustrates the equivalent internal circuit when using an external DAC to set the black level reference. The load circuit, the DAC sees, is in parallel to as many segments that are connected to the same DAC.

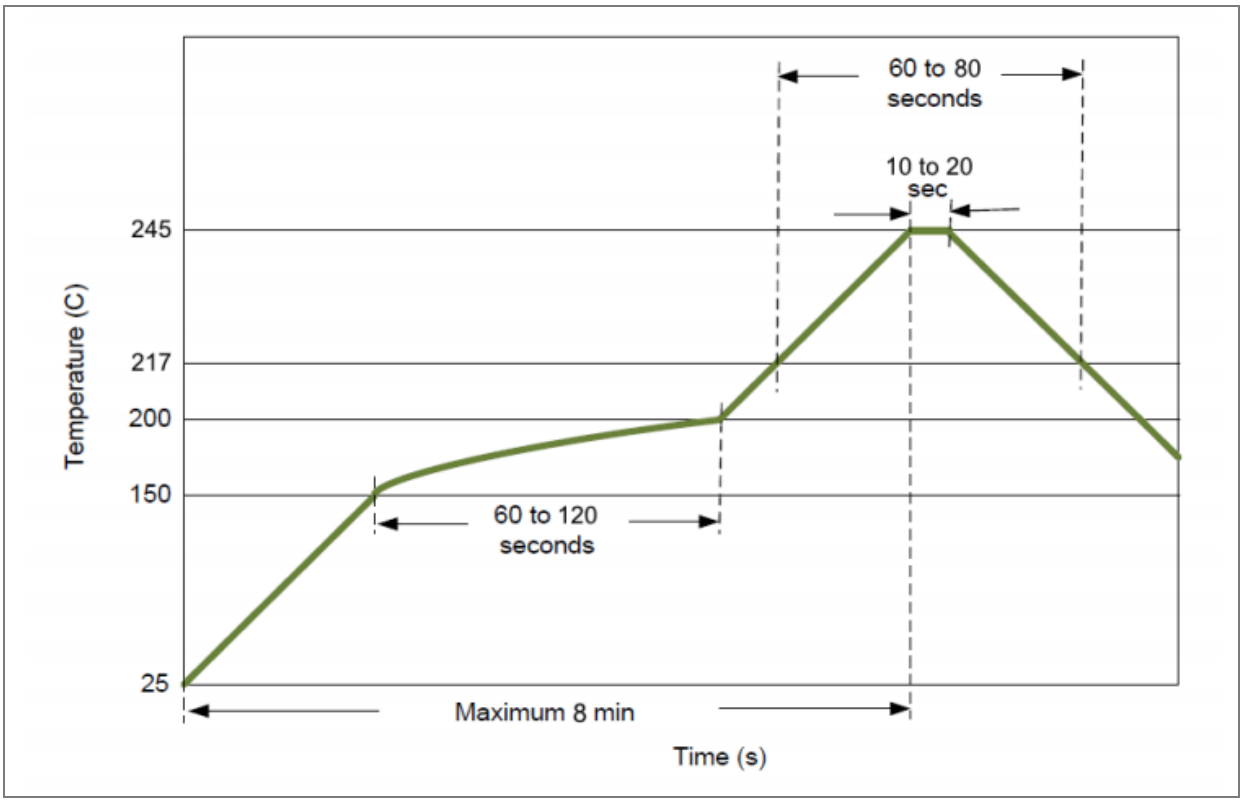
Figure 32: Equivalent load scheme for use of external DAC



11 Soldering information

Figure 33 shows the maximum recommended thermal profile for a reflow soldering system (following Standard J-STD-020), relative to LCC ceramic package. If the temperature/time profile exceeds these recommendations, damage to the image sensor can occur.

Figure 33: Solder reflow profile graph



Attention

Image sensors with color filter arrays (CFA) are especially sensitive to high temperatures. Prolonged heating at elevated temperatures may result in deterioration of the optical performance of the sensor.

A socket is the safest way to avoid any thermal stress. When not using a socket, to avoid heating up the device we recommend to use manual hand soldering. Wave soldering can be used with precautions (see below). Reflow soldering is not recommended.

Manual soldering: Use partial heating method and use a soldering iron with temperature control. The soldering iron tip temperature is not to exceed 350°C with a 270°C maximum pin temperature. Touch for a 2 seconds maximum duration per pin. Avoid touching and global heating of the ceramic package during soldering. Failure to do so may alter device performance and reliability.

Wave soldering: Wave solder dipping can cause damage to the glass and harm the imaging capability of the device. Avoid the solder to come in contact with the glass or ceramic body.

12 Pin description

12.1 Signal assignment to LCC ceramic packaging

Table 33: Pinout DR2K7_LCC_Ceramic, DR2x2K7_LCC_Ceramic, DR4K3.5_LCC_Ceramic

Pin number	Pin name (DR4K3.5_LCC_Ceramic DR2x2K7_LCC_Ceramic)	Pin name (DR2K7_LCC_Ceramic)	Pin type[1]
1	Tap A1 Bit 11	Tap A1 Bit 11	DO
2	Tap A1 Bit 9	Tap A1 Bit 9	DO
3	Tap A1 Bit 7	Tap A1 Bit 7	DO
4	Tap A1 Bit 5	Tap A1 Bit 5	DO
5	Tap A1 Bit 3	Tap A1 Bit 3	DO
6	Tap A1 Bit 1	Tap A1 Bit 1	DO
7	VSS	VSS	GND
8	LVAL Tap A1/B1	LVAL Tap A1/B1	DO
9	Tap A1 Bit 12	Tap A1 Bit 12	DO
10	Tap A1 Bit 10	Tap A1 Bit 10	DO
11	Tap A1 Bit 8	Tap A1 Bit 8	DO
12	Tap A1 Bit 6	Tap A1 Bit 6	DO
13	Tap A1 Bit 4	Tap A1 Bit 4	DO
14	Tap A1 Bit 2	Tap A1 Bit 2	DO
15	Tap A1 Bit 0	Tap A1 Bit 0	DO
16	Pixel_CLK_Tap A1/B1	Pixel_CLK_Tap A1/B1	DO
17	End_ADC_Tap A1/B1	End_ADC_Tap A1/B1	DO
18	VSS	VSS	GND
19	Tap B1 Bit 1	Tap B1 Bit 1	DO
20	Tap B1 Bit 3	Tap B1 Bit 3	DO
21	Tap B1 Bit 5	Tap B1 Bit 5	DO
22	Tap B1 Bit 7	Tap B1 Bit 7	DO
23	Tap B1 Bit 9	Tap B1 Bit 9	DO
24	Tap B1 Bit 11	Tap B1 Bit 11	DO
25	Tap B1 Bit 0	Tap B1 Bit 0	DO
26	Tap B1 Bit 2	Tap B1 Bit 2	DO
27	Tap B1 Bit 4	Tap B1 Bit 2	DO
28	VSS	VSS	GND

Pin number	Pin name (DR4K3.5_LCC_Ceramic DR2x2K7_LCC_Ceramic)	Pin name (DR2K7_LCC_Ceramic)	Pin type[1]
29	Tap B1 Bit 6	Tap B1 Bit 6	DO
30	Tap B1 Bit 8	Tap B1 Bit 8	DO
31	Tap B1 Bit 10	Tap B1 Bit 10	DO
32	Tap B1 Bit 12	Tap B1 Bit 12	DO
33	VSS	VSS	GND
34	VDDA	VDDA	3.3 V Analogue
35	VDD	VDD	3.3 V Supply
36	VDD	VDD	3.3 V Supply
37	VDD	VDD	3.3 V Supply
38	VDDA	VDDA	3.3 V Analogue
39	N_Reset	N_Reset	DI
40	VSS	GND	GND
41	Tap D1 Bit 12	*Not connected*	DO
42	Tap D1 Bit 10	*Not connected*	DO
43	Tap D1 Bit 8	*Not connected*	DO
44	Tap D1 Bit 6	*Not connected*	DO
45	VSS	VSS	GND
46	Tap D1 Bit 4	*Not connected*	DO
47	Tap D1 Bit 2	*Not connected*	DO
48	Tap D1 Bit 0	*Not connected*	DO
49	Tap D1 Bit 11	*Not connected*	DO
50	Tap D1 Bit 9	*Not connected*	DO
51	Tap D1 Bit 7	*Not connected*	DO
52	Tap D1 Bit 5	*Not connected*	DO
53	Tap D1 Bit 3	*Not connected*	DO
54	Tap D1 Bit 1	*Not connected*	DO
55	VSS	GND	GND
56	End_ADC_Tap C1/D1	*Not connected*	DO
57	Pixel_CLK_Tap C1/D1	*Not connected*	DO
58	Tap C1 Bit 0	*Not connected*	DO
59	Tap C1 Bit 2	*Not connected*	DO
60	Tap C1 Bit 4	*Not connected*	DO
61	Tap C1 Bit 6	*Not connected*	DO
62	Tap C1 Bit 8	*Not connected*	DO
63	Tap C1 Bit 10	*Not connected*	DO
64	Tap C1 Bit 12	*Not connected*	DO

Pin number	Pin name (DR4K3.5_LCC_Ceramic DR2x2K7_LCC_Ceramic)	Pin name (DR2K7_LCC_Ceramic)	Pin type(1)
65	LVAL Tap C1/D1	*Not connected*	DO
66	VSS	GND	GND
67	MISO C1/D1	*Not connected*	DO
68	Tap C1 Bit 1	*Not connected*	DO
69	Tap C1 Bit 3	*Not connected*	DO
70	Tap C1 Bit 5	*Not connected*	DO
71	Tap C1 Bit 7	*Not connected*	DO
72	Tap C1 Bit 9	*Not connected*	DO
73	VSS	GND	GND
74	Tap C1 Bit 11	*Not connected*	DO
75	RESET_CDS	DI	DI
76	N_CS C1/D1	*Not connected*	DI
77	MOSI	DI	DI
78	Main_CLK	DI	DI
79	Load_Pulse	DI	DI
80	VSS	GND	GND
81	VDD	3.3V	3.3 V
82	VDD	3.3V	3.3 V
83	VDDA	VDDA	3.3 V Analogue
84	VDDA	VDDA	3.3 V Analogue
85	N_CS A1/B1	DI	DI
86	Sample	DI	DI
87	RST_CVC	DI	DI
88	SCLK	DI	DI
89	MISO A1/B1	DO	DO
90	VSS	GND	GND

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

12.2 Connector signal assignment for Invar headboard variations DR2x2K7, DR4K3.5, DR2K7

For DR2K7_Invar, connector 2 is present but not required. Only the powers present on the connector are routed to the sensor. Connector 2 can be left completely unconnected for DR2K7_Invar.

Table 34: Connector 1 pinout

Pin number	Pin name	Pin type[1]
1	N_CS_AB_1	DI
2	MISO_AB_1	DO
3	VDDA	VDDA
4	VDDD	VDDD
5	VSSA	GND
6	VSS_Bulk	GND
7	VSSD	GND
8	Load_Pulse_AB_1	DI
9	VDDIO	VDDIO
10	End_ADC_AB_1	DI
11	VDDA	VDDA
12	VDD_Bulk	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSA	GND
16	VSS_Bulk	GND
17	VSSD	GND
18	VDDIO	VDDIO
19	Test_Mux_AB_1	Analogue Monitor - Leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSA	GND
23	VSS_Bulk	GND
24	VSSD	GND
25	VSSESD/IO	GND
26	Pixel_CLK_AB_1	DO
27	VClamp_AB_1	VDDA
28	Sample_AB	DI
29	RST_CDS_AB	DI
30	RST_CVC_AB	DI

Pin number	Pin name	Pin type[1]
31	*Not connected*	
32	SCLK_AB_EF	DI
33	MOSI_AB_EF	DI
34	*Not connected*	
35	VDDA	VDDA
36	VDD_Bulk	VDD_Bulk
37	VDDD	VDDD
38	VDDESD	VDDESD
39	VSSA	GND
40	VSS_Bulk	GND
41	VSSD	GND
42	*Not connected*	
43	VDDIO	VDDIO
44	*Not connected*	
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSA	GND
48	VSSD	GND
49	VDDIO	VDDIO
50	*Not connected*	
51	VDDA	VDDA
52	VDD_Bulk	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSA	GND
56	VSS_Bulk	GND
57	VSSD	GND
58	N_Reset_AB	DI
59	*Not connected*	
60	*Not connected*	
61	VSSESD/IO	GND
62	LVAL_AB_1	DO
63	Bit_12_Tap_A1	DO
64	Bit_11_Tap_A1	DO
65	Bit_10_Tap_A1	DO
66	Bit_09_Tap_A1	DO
67	Bit_08_Tap_A1	DO
68	Bit_07_Tap_A1	DO

Pin number	Pin name	Pin type[1]
69	Bit_06_Tap_A1	DO
70	Bit_05_Tap_A1	DO
71	Bit_04_Tap_A1	DO
72	Bit_03_Tap_A1	DO
73	Bit_02_Tap_A1	DO
74	Bit_01_Tap_A1	DO
75	Bit_00_Tap_A1	DO
76	VSSESD/IO	GND
77	Bit_00_Tap_B1	DO
78	Bit_01_Tap_B1	DO
79	Bit_02_Tap_B1	DO
80	Bit_03_Tap_B1	DO
81	Bit_04_Tap_B1	DO
82	Bit_05_Tap_B1	DO
83	Bit_06_Tap_B1	DO
84	Bit_07_Tap_B1	DO
85	Bit_08_Tap_B1	DO
86	Bit_09_Tap_B1	DO
87	Bit_10_Tap_B1	DO
88	Bit_11_Tap_B1	DO
89	Bit_12_Tap_B1	DO
90	Main_CLK	DI
91	VSSESD/IO	GND
92	*Not connected*	
93	*Not connected*	
94	*Not connected*	
95	*Not connected*	
96	*Not connected*	
97	*Not connected*	
98	*Not connected*	
99	*Not connected*	
100	*Not connected*	
101	*Not connected*	
102	*Not connected*	
103	*Not connected*	
104	*Not connected*	
105	*Not connected*	
106	VSSESD/IO	GND

Pin number	Pin name	Pin type(1)
107	*Not connected*	
108	*Not connected*	
109	*Not connected*	
110	*Not connected*	
111	*Not connected*	
112	*Not connected*	
113	*Not connected*	
114	*Not connected*	
115	*Not connected*	
116	*Not connected*	
117	*Not connected*	
118	*Not connected*	
119	*Not connected*	
120	VSSESD/IO	GND

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

Information:

SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. The user can provide the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI, taking the advantage that two IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

Table 35: Connector 2 pinout

Pin number	Pin name	Pin type(1)
1	VSSESD/IO	GND
2	LVAL_CD_1	DO
3	Bit_12_Tap_C1	DO
4	Bit_11_Tap_C1	DO
5	Bit_10_Tap_C1	DO
6	Bit_09_Tap_C1	DO
7	Bit_08_Tap_C1	DO

Pin number	Pin name	Pin type[1]
8	Bit_07_Tap_C1	DO
9	Bit_06_Tap_C1	DO
10	Bit_05_Tap_C1	DO
11	Bit_04_Tap_C1	DO
12	Bit_03_Tap_C1	DO
13	Bit_02_Tap_C1	DO
14	Bit_01_Tap_C1	DO
15	Bit_00_Tap_C1	DO
16	VSSESD/IO	GND
17	Bit_00_Tap_D1	DO
18	Bit_01_Tap_D1	DO
19	Bit_02_Tap_D1	DO
20	Bit_03_Tap_D1	DO
21	Bit_04_Tap_D1	DO
22	Bit_05_Tap_D1	DO
23	Bit_06_Tap_D1	DO
24	Bit_07_Tap_D1	DO
25	Bit_08_Tap_D1	DO
26	Bit_09_Tap_D1	DO
27	Bit_10_Tap_D1	DO
28	Bit_11_Tap_D1	DO
29	Bit_12_Tap_D1	DO
30	*Not connected*	
31	VSSESD/IO	GND
32	*Not connected*	
33	*Not connected*	
34	*Not connected*	
35	*Not connected*	
36	*Not connected*	
37	*Not connected*	
38	*Not connected*	
39	*Not connected*	
40	*Not connected*	
41	*Not connected*	
42	*Not connected*	
43	*Not connected*	
44	*Not connected*	
45	*Not connected*	

Pin number	Pin name	Pin type[1]
46	VSSESD/IO	GND
47	*Not connected*	
48	*Not connected*	
49	*Not connected*	
50	*Not connected*	
51	*Not connected*	
52	*Not connected*	
53	*Not connected*	
54	*Not connected*	
55	*Not connected*	
56	*Not connected*	
57	*Not connected*	
58	*Not connected*	
59	*Not connected*	
60	VSSESD/IO	GND
61	N_CS_CD_1	DI
62	MISO_CD_1	DO
63	VDDA	VDDA
64	VDDD	VDDD
65	VSSA	GND
66	VSS_Bulk	GND
67	VSSD	GND
68	Load_Pulse_CD_1	DI
69	VDDIO	VDDIO
70	End_ADC_CD_1	DO
71	VDDA	VDDA
72	VDD_Bulk	VDD_Bulk
73	VDDD	VDDD
74	VDDESD	VDDESD
75	VSSA	GND
76	VSS_Bulk	GND
77	VSSD	GND
78	VDDIO	VDDIO
79	Test_Mux_CD_1	Analogue Monitor - Leave n.c.
80	VDDA	VDDA
81	VDDD	VDDD
82	VSSA	GND
83	VSS_Bulk	GND

Pin number	Pin name	Pin type[1]
84	VSSD	GND
85	VSSESD/IO	GND
86	Pixel_CLK_CD_1	DO
87	VClamp_CD_1	VDDA
88	Sample_CD	DI
89	RST_CDS_CD	DI
90	RST_CVC_CD	DI
91	*Not connected*	
92	SCLK_CD_GH	DI
93	MOSI_CD_GH	DI
94	*Not connected*	
95	VDDA	VDDA
96	VDD_Bulk	VDD_Bulk
97	VDDD	VDDD
98	VDDESD	VDDESD
99	VSSA	GND
100	VSS_Bulk	GND
101	VSSD	GND
102	*Not connected*	
103	VDDIO	VDDIO
104	*Not connected*	
105	VDDA	VDDA
106	VDDD	VDDD
107	VSSA	GND
108	VSSD	GND
109	VDDIO	VDDIO
110	*Not connected*	
111	VDDA	VDDA
112	VDD_Bulk	VDD_Bulk
113	VDDD	VDDD
114	VDDESD	VDDESD
115	VSSA	GND
116	VSS_Bulk	GND
117	VSSD	GND
118	N_Reset_CD	DI
119	*Not connected*	
120	*Not connected*	

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

Information:

SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user can provide the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI, taking the advantage that two IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

12.3 Connector signal assignment for Invar headboard variations DR4K7, DR8K7, DR8K3.5, DR16K3.5, DR2x4K7, DR2x8K7

Table 36: Connector 1 pinout

Pin number	Pin name	Pin type(1)
1	N_CS_AB_1	DI
2	MISO_AB_1	DO
3	VDDA	VDDA
4	VDDD	VDDD
5	VSSA	GND
6	VSS_Bulk	GND
7	VSSD	GND
8	Load_Pulse_AB_1	DI
9	VDDIO	VDDIO
10	End_ADC_AB_1	DI
11	VDDA	VDDA
12	VDD_Bulk	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSA	GND
16	VSS_Bulk	GND
17	VSSD	GND

Pin number	Pin name	Pin type[1]
18	VDDIO	VDDIO
19	Test_Mux_AB_1	Analogue Monitor - Leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSA	GND
23	VSS_Bulk	GND
24	VSSD	GND
25	VSSESD/IO	GND
26	Pixel_CLK_AB_1	DO
27	VClamp_AB_1	VDDA
28	Sample_AB	DI
29	RST_CDS_AB	DI
30	RST_CVC_AB	DI
31	N_CS_AB_2	DI
32	SCLK_AB_EF	DI
33	MOSI_AB_EF	DI
34	MISO_AB_2	DO
35	VDDA	VDDA
36	VDD_Bulk	VDD_Bulk
37	VDDD	VDDD
38	VDDESD	VDDESD
39	VSSA	GND
40	VSS_Bulk	GND
41	VSSD	GND
42	Load_Pulse_AB_2	DI
43	VDDIO	VDDIO
44	End_ADC_AB_2	DO
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSA	GND
48	VSSD	GND
49	VDDIO	VDDIO
50	Test_Mux_AB_2	Analogue Monitor - Leave n.c.
51	VDDA	VDDA
52	VDD_Bulk	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSA	GND

Pin number	Pin name	Pin type[1]
56	VSS_Bulk	GND
57	VSSD	GND
58	N_Reset_AB	DI
59	Pixel_Clock_AB_2	DO
60	VClamp_AB_2	VDDA
61	VSSESD/IO	GND
62	LVAL_AB_1	DO
63	Bit_12_Tap_A1	DO
64	Bit_11_Tap_A1	DO
65	Bit_10_Tap_A1	DO
66	Bit_09_Tap_A1	DO
67	Bit_08_Tap_A1	DO
68	Bit_07_Tap_A1	DO
69	Bit_06_Tap_A1	DO
70	Bit_05_Tap_A1	DO
71	Bit_04_Tap_A1	DO
72	Bit_03_Tap_A1	DO
73	Bit_02_Tap_A1	DO
74	Bit_01_Tap_A1	DO
75	Bit_00_Tap_A1	DO
76	VSSESD/IO	GND
77	Bit_00_Tap_B1	DO
78	Bit_01_Tap_B1	DO
79	Bit_02_Tap_B1	DO
80	Bit_03_Tap_B1	DO
81	Bit_04_Tap_B1	DO
82	Bit_05_Tap_B1	DO
83	Bit_06_Tap_B1	DO
84	Bit_07_Tap_B1	DO
85	Bit_08_Tap_B1	DO
86	Bit_09_Tap_B1	DO
87	Bit_10_Tap_B1	DO
88	Bit_11_Tap_B1	DO
89	Bit_12_Tap_B1	DO
90	Main_CLK	DI
91	VSSESD/IO	GND
92	LVAL_AB_2	DO
93	Bit_12_Tap_A2	DO

Pin number	Pin name	Pin type(1)
94	Bit_11_Tap_A2	DO
95	Bit_10_Tap_A2	DO
96	Bit_09_Tap_A2	DO
97	Bit_08_Tap_A2	DO
98	Bit_07_Tap_A2	DO
99	Bit_06_Tap_A2	DO
100	Bit_05_Tap_A2	DO
101	Bit_04_Tap_A2	DO
102	Bit_03_Tap_A2	DO
103	Bit_02_Tap_A2	DO
104	Bit_01_Tap_A2	DO
105	Bit_00_Tap_A2	DO
106	VSSESD/IO	GND
107	Bit_00_Tap_B2	DO
108	Bit_01_Tap_B2	DO
109	Bit_02_Tap_B2	DO
110	Bit_03_Tap_B2	DO
111	Bit_04_Tap_B2	DO
112	Bit_05_Tap_B2	DO
113	Bit_06_Tap_B2	DO
114	Bit_07_Tap_B2	DO
115	Bit_08_Tap_B2	DO
116	Bit_09_Tap_B2	DO
117	Bit_10_Tap_B2	DO
118	Bit_11_Tap_B2	DO
119	Bit_12_Tap_B2	DO
120	VSSESD/IO	GND

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

Information:

SCLK and MOSI are connected between connector 1 and connector 3 in the headboard, resulting names are SCLK_AB_EF and MOSI_AB_EF. The user can provide the headboard one pair of this signals to connector 1 or 3 to communicate with the SPI, taking the advantage that two IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

Table 37: Connector 2 pinout

Pin number	Pin name	Pin type(1)
1	VSSESD/IO	GND
2	LVAL_CD_1	DO
3	Bit_12_Tap_C1	DO
4	Bit_11_Tap_C1	DO
5	Bit_10_Tap_C1	DO
6	Bit_09_Tap_C1	DO
7	Bit_08_Tap_C1	DO
8	Bit_07_Tap_C1	DO
9	Bit_06_Tap_C1	DO
10	Bit_05_Tap_C1	DO
11	Bit_04_Tap_C1	DO
12	Bit_03_Tap_C1	DO
13	Bit_02_Tap_C1	DO
14	Bit_01_Tap_C1	DO
15	Bit_00_Tap_C1	DO
16	VSSESD/IO	GND
17	Bit_00_Tap_D1	DO
18	Bit_01_Tap_D1	DO
19	Bit_02_Tap_D1	DO
20	Bit_03_Tap_D1	DO
21	Bit_04_Tap_D1	DO
22	Bit_05_Tap_D1	DO
23	Bit_06_Tap_D1	DO
24	Bit_07_Tap_D1	DO
25	Bit_08_Tap_D1	DO
26	Bit_09_Tap_D1	DO
27	Bit_10_Tap_D1	DO

Pin number	Pin name	Pin type[1]
28	Bit_11_Tap_D1	DO
29	Bit_12_Tap_D1	DO
30	*Not connected*	
31	VSSESD/IO	GND
32	LVAL_CD_2	DO
33	Bit_12_Tap_C2	DO
34	Bit_11_Tap_C2	DO
35	Bit_10_Tap_C2	DO
36	Bit_09_Tap_C2	DO
37	Bit_08_Tap_C2	DO
38	Bit_07_Tap_C2	DO
39	Bit_06_Tap_C2	DO
40	Bit_05_Tap_C2	DO
41	Bit_04_Tap_C2	DO
42	Bit_03_Tap_C2	DO
43	Bit_02_Tap_C2	DO
44	Bit_01_Tap_C2	DO
45	Bit_00_Tap_C2	DO
46	VSSESD/IO	GND
47	Bit_00_Tap_D2	DO
48	Bit_01_Tap_D2	DO
49	Bit_02_Tap_D2	DO
50	Bit_03_Tap_D2	DO
51	Bit_04_Tap_D2	DO
52	Bit_05_Tap_D2	DO
53	Bit_06_Tap_D2	DO
54	Bit_07_Tap_D2	DO
55	Bit_08_Tap_D2	DO
56	Bit_09_Tap_D2	DO
57	Bit_10_Tap_D2	DO
58	Bit_11_Tap_D2	DO
59	Bit_12_Tap_D2	DO
60	VSSESD/IO	GND
61	N_CS_CD_1	DI
62	MISO_CD_1	DO
63	VDDA	VDDA
64	VDDD	VDDD
65	VSSA	GND

Pin number	Pin name	Pin type[1]
66	VSS_Bulk	GND
67	VSSD	GND
68	Load_Pulse_CD_1	DI
69	VDDIO	VDDIO
70	End_ADC_CD_1	DO
71	VDDA	VDDA
72	VDD_Bulk	VDD_Bulk
73	VDDD	VDDD
74	VDDESD	VDDESD
75	VSSA	GND
76	VSS_Bulk	GND
77	VSSD	GND
78	VDDIO	VDDIO
79	Test_Mux_CD_1	Analogue Monitor - Leave n.c.
80	VDDA	VDDA
81	VDDD	VDDD
82	VSSA	GND
83	VSS_Bulk	GND
84	VSSD	GND
85	VSSESD/IO	GND
86	Pixel_CLK_CD_1	DO
87	VClamp_CD_1	VDDA
88	Sample_CD	DI
89	RST_CDS_CD	DI
90	RST_CVC_CD	DI
91	N_CS_CD_2	DI
92	SCLK_CD_GH	DI
93	MOSI_CD_GH	DI
94	MISO_CD_2	DO
95	VDDA	VDDA
96	VDD_Bulk	VDD_Bulk
97	VDDD	VDDD
98	VDDESD	VDDESD
99	VSSA	GND
100	VSS_Bulk	GND
101	VSSD	GND
102	Load_Pulse_CD_2	DI
103	VDDIO	VDDIO

Pin number	Pin name	Pin type(1)
104	End_ADC_CD_2	DO
105	VDDA	VDDA
106	VDDD	VDDD
107	VSSA	GND
108	VSSD	GND
109	VDDIO	VDDIO
110	Test_Mux_CD_2	Analogue Monitor - Leave n.c.
111	VDDA	VDDA
112	VDD_Bulk	VDD_Bulk
113	VDDD	VDDD
114	VDDESD	VDDESD
115	VSSA	GND
116	VSS_Bulk	GND
117	VSSD	GND
118	N_Reset_CD	DI
119	Pixel_CLK_CD_2	DO
120	VClamp_CD_2	VDDA

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

Information:

SCLK and MOSI are connected between connector 2 and connector 4 in the headboard, resulting names are SCLK_CD_GH and MOSI_CD_GH. The user can provide the headboard one pair of this signals to connector 2 or 4 to communicate with the SPI, taking the advantage that two IO lines from the control unit (FPGA or CPLD) are saved. Each SPI can be selected individually by selecting respective negative chip select pin.

Table 38: Connector 3 pinout

Pin number	Pin name	Pin type(1)
1	N_CS_EF_1	DI
2	MISO_EF_1	DO
3	VDDA	VDDA
4	VDDD	VDDD

Pin number	Pin name	Pin type[1]
5	VSSA	GND
6	VSS_Bulk	GND
7	VSSD	GND
8	Load_Pulse_EF_1	DI
9	VDDIO	VDDIO
10	End_ADC_EF_1	DO
11	VDDA	VDDA
12	VDD_Bulk	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSA	GND
16	VSS_Bulk	GND
17	VSSD	GND
18	VDDIO	VDDIO
19	Test_Mux_EF_1	Analogue Monitor - Leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSA	GND
23	VSS_Bulk	GND
24	VSSD	GND
25	VSSESD/IO	GND
26	Pixel_CLK_EF_1	DO
27	VClamp_EF_1	VDDA
28	Sample_EF	DI
29	RST_CDS_EF	DI
30	RST_CVC_EF	DI
31	N_CS_EF_2	DI
32	SCLK_AB_EF	DI
33	MOSI_AB_EF	DI
34	MISO_EF_2	DO
35	VDDA	VDDA
36	VDD_Bulk	VDD_Bulk
37	VDDD	VDDD
38	VDDESD	VDDESD
39	VSSA	GND
40	VSS_Bulk	GND
41	VSSD	GND
42	Load_Pulse_EF_2	DI

Pin number	Pin name	Pin type[1]
43	VDDIO	VDDIO
44	End_ADC_EF_2	DO
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSA	GND
48	VSSD	GND
49	VDDIO	VDDIO
50	Test_Mux_EF_2	Analogue Monitor - Leave n.c.
51	VDDA	VDDA
52	VDD_Bulk	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSA	GND
56	VSS_Bulk	GND
57	VSSD	GND
58	N_Reset_EF	DI
59	Pixel_Clock_EF_2	DO
60	VClamp_EF_2	VDDA
61	VSSESD/IO	GND
62	LVAL_EF_1	DO
63	Bit_12_Tap_E1	DO
64	Bit_11_Tap_E1	DO
65	Bit_10_Tap_E1	DO
66	Bit_09_Tap_E1	DO
67	Bit_08_Tap_E1	DO
68	Bit_07_Tap_E1	DO
69	Bit_06_Tap_E1	DO
70	Bit_05_Tap_E1	DO
71	Bit_04_Tap_E1	DO
72	Bit_03_Tap_E1	DO
73	Bit_02_Tap_E1	DO
74	Bit_01_Tap_E1	DO
75	Bit_00_Tap_E1	DO
76	VSSESD/IO	GND
77	Bit_00_Tap_F1	DO
78	Bit_01_Tap_F1	DO
79	Bit_02_Tap_F1	DO
80	Bit_03_Tap_F1	DO

Pin number	Pin name	Pin type[1]
81	Bit_04_Tap_F1	DO
82	Bit_05_Tap_F1	DO
83	Bit_06_Tap_F1	DO
84	Bit_07_Tap_F1	DO
85	Bit_08_Tap_F1	DO
86	Bit_09_Tap_F1	DO
87	Bit_10_Tap_F1	DO
88	Bit_11_Tap_F1	DO
89	Bit_12_Tap_F1	DO
90	Main_CLK	DI
91	VSSESD/IO	GND
92	LVAL_EF_2	DO
93	Bit_12_Tap_E2	DO
94	Bit_11_Tap_E2	DO
95	Bit_10_Tap_E2	DO
96	Bit_09_Tap_E2	DO
97	Bit_08_Tap_E2	DO
98	Bit_07_Tap_E2	DO
99	Bit_06_Tap_E2	DO
100	Bit_05_Tap_E2	DO
101	Bit_04_Tap_E2	DO
102	Bit_03_Tap_E2	DO
103	Bit_02_Tap_E2	DO
104	Bit_01_Tap_E2	DO
105	Bit_00_Tap_E2	DO
106	VSSESD/IO	GND
107	Bit_00_Tap_F2	DO
108	Bit_01_Tap_F2	DO
109	Bit_02_Tap_F2	DO
110	Bit_03_Tap_F2	DO
111	Bit_04_Tap_F2	DO
112	Bit_05_Tap_F2	DO
113	Bit_06_Tap_F2	DO
114	Bit_07_Tap_F2	DO
115	Bit_08_Tap_F2	DO
116	Bit_09_Tap_F2	DO
117	Bit_10_Tap_F2	DO
118	Bit_11_Tap_F2	DO

Pin number	Pin name	Pin type(1)
119	Bit_12_Tap_F2	DO
120	VSSESD/IO	GND

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

Table 39: Connector 4 pinout

Pin number	Pin name	Pin type(1)
1	VSSESD/IO	GND
2	LVAL_GH_1	DO
3	Bit_12_Tap_G1	DO
4	Bit_11_Tap_G1	DO
5	Bit_10_Tap_G1	DO
6	Bit_09_Tap_G1	DO
7	Bit_08_Tap_G1	DO
8	Bit_07_Tap_G1	DO
9	Bit_06_Tap_G1	DO
10	Bit_05_Tap_G1	DO
11	Bit_04_Tap_G1	DO
12	Bit_03_Tap_G1	DO
13	Bit_02_Tap_G1	DO
14	Bit_01_Tap_G1	DO
15	Bit_00_Tap_G1	DO
16	VSSESD/IO	GND
17	Bit_00_Tap_H1	DO
18	Bit_01_Tap_H1	DO
19	Bit_02_Tap_H1	DO
20	Bit_03_Tap_H1	DO
21	Bit_04_Tap_H1	DO
22	Bit_05_Tap_H1	DO
23	Bit_06_Tap_H1	DO
24	Bit_07_Tap_H1	DO
25	Bit_08_Tap_H1	DO
26	Bit_09_Tap_H1	DO
27	Bit_10_Tap_H1	DO
28	Bit_11_Tap_H1	DO

Pin number	Pin name	Pin type[1]
29	Bit_12_Tap_H1	DO
30	*Not connected*	
31	VSSESD/IO	GND
32	LVAL_GH_2	DO
33	Bit_12_Tap_G2	DO
34	Bit_11_Tap_G2	DO
35	Bit_10_Tap_G2	DO
36	Bit_09_Tap_G2	DO
37	Bit_08_Tap_G2	DO
38	Bit_07_Tap_G2	DO
39	Bit_06_Tap_G2	DO
40	Bit_05_Tap_G2	DO
41	Bit_04_Tap_G2	DO
42	Bit_03_Tap_G2	DO
43	Bit_02_Tap_G2	DO
44	Bit_01_Tap_G2	DO
45	Bit_00_Tap_G2	DO
46	VSSESD/IO	GND
47	Bit_00_Tap_H2	DO
48	Bit_01_Tap_H2	DO
49	Bit_02_Tap_H2	DO
50	Bit_03_Tap_H2	DO
51	Bit_04_Tap_H2	DO
52	Bit_05_Tap_H2	DO
53	Bit_06_Tap_H2	DO
54	Bit_07_Tap_H2	DO
55	Bit_08_Tap_H2	DO
56	Bit_09_Tap_H2	DO
57	Bit_10_Tap_H2	DO
58	Bit_11_Tap_H2	DO
59	Bit_12_Tap_H2	DO
60	VSSESD/IO	GND
61	N_CS_GH_1	DI
62	MISO_GH_1	DO
63	VDDA	VDDA
64	VDDD	VDDD
65	VSSA	GND
66	VSS_Bulk	GND

Pin number	Pin name	Pin type[1]
67	VSSD	GND
68	Load_Pulse_GH_1	DI
69	VDDIO	VDDIO
70	End_ADC_GH_1	DO
71	VDDA	VDDA
72	VDD_Bulk	VDD_Bulk
73	VDDD	VDDD
74	VDDESD	VDDESD
75	VSSA	GND
76	VSS_Bulk	GND
77	VSSD	GND
78	VDDIO	VDDIO
79	Test_Mux_GH_1	Analogue Monitor - Leave n.c.
80	VDDA	VDDA
81	VDDD	VDDD
82	VSSA	GND
83	VSS_Bulk	GND
84	VSSD	GND
85	VSSESD/IO	GND
86	Pixel_CLK_GH_1	DO
87	VClamp_GH_1	VDDA
88	Sample_GH	DI
89	RST_CDS_GH	DI
90	RST_CVC_GH	DI
91	N_CS_GH_2	DI
92	SCLK_CD_GH	DI
93	MOSI_CD_GH	DI
94	MISO_GH_2	DO
95	VDDA	VDDA
96	VDD_Bulk	VDD_Bulk
97	VDDD	VDDD
98	VDDESD	VDDESD
99	VSSA	GND
100	VSS_Bulk	GND
101	VSSD	GND
102	Load_Pulse_GH_2	DI
103	VDDIO	VDDIO
104	End_ADC_GH_2	DO

Pin number	Pin name	Pin type(1)
105	VDDA	VDDA
106	VDDD	VDDD
107	VSSA	GND
108	VSSD	GND
109	VDDIO	VDDIO
110	Test_Mux_GH_2	Analogue Monitor - Leave n.c.
111	VDDA	VDDA
112	VDD_Bulk	VDD_Bulk
113	VDDD	VDDD
114	VDDESD	VDDESD
115	VSSA	GND
116	VSS_Bulk	GND
117	VSSD	GND
118	N_Reset_GH	DI
119	Pixel_CLK_GH_2	DO
120	VClamp_GH_2	VDDA

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

12.4 Connector signal assignment for Invar headboard variant DR6K7

Information:

In this module, analogue and digital grounds are in separate nets. When providing proper decoupling to these signals, the noise parameters can be reduced to a minimum.

The data pin order differs from the other variations but the sensor control signals are placed in the same pins. With this it is possible to control the sensor with the same electronics and only changing the data pins reassignment on the processing board.

Table 40: Connector 1 pinout

Pin number	Pin name	Pin type(1)
1	N_CS_AB_1	DI

Pin number	Pin name	Pin type[1]
2	MISO_AB_1	DO
3	VDDA	VDDA
4	VDDD	VDDD
5	VSSD	GND
6	VSSD	GND
7	VSSA	GND
8	Load_Pulse_AB_1	DI
9	VDDIO	VDDIO
10	End_ADC_AB_1	DI
11	VDDA	VDDA
12	VDD_Bulk	VDD_Bulk
13	VDDD	VDDD
14	VDDESD	VDDESD
15	VSSD	GND
16	VSSD	GND
17	VSSA	GND
18	VDDIO	VDDIO
19	Test_Mux_AB_1	Analogue Monitor - Leave n.c.
20	VDDA	VDDA
21	VDDD	VDDD
22	VSSD	GND
23	VSSD	GND
24	VSSD	GND
25	VSSA	GND
26	Pixel_CLK_AB_1	DO
27	*Not connected*	
28	Sample_AB	DI
29	RST_CDS_AB	DI
30	RST_CVC_AB	DI
31	N_CS_AB_2	DI
32	SCLK_AB_EF	DI
33	MOSI_AB_EF	DI
34	MISO_AB_2	DO
35	VDDA	VDDA
36	VDD_Bulk	VDD_Bulk
37	VDDD	VDDD
38	VDDESD	VDDESD
39	VSSD	GND

Pin number	Pin name	Pin type[1]
40	VSSD	GND
41	VSSA	GND
42	Load_Pulse_AB_2	DI
43	VDDIO	VDDIO
44	End_ADC_AB_2	DO
45	VDDA	VDDA
46	VDDD	VDDD
47	VSSD	GND
48	VSSA	GND
49	VDDIO	VDDIO
50	*Not connected*	
51	VDDA	VDDA
52	VDD_Bulk	VDD_Bulk
53	VDDD	VDDD
54	VDDESD	VDDESD
55	VSSD	GND
56	VSSD	GND
57	VSSA	GND
58	N_Reset_AB	DI
59	Pixel_Clock_AB_2	DO
60	*Not connected*	
61	VSSD	GND
62	LVAL_AB_1	DO
63	*Not connected*	
64	Bit_00_Tap_B1	DO
65	Bit_01_Tap_B1	DO
66	Bit_02_Tap_B1	DO
67	Bit_03_Tap_B1	DO
68	Bit_04_Tap_B1	DO
69	Bit_05_Tap_B1	DO
70	Bit_06_Tap_B1	DO
71	Bit_07_Tap_B1	DO
72	Bit_08_Tap_B1	DO
73	Bit_09_Tap_B1	DO
74	Bit_10_Tap_B1	DO
75	Bit_11_Tap_B1	DO
76	VSSD	GND
77	Bit_11_Tap_A2	DO

Pin number	Pin name	Pin type[1]
78	Bit_10_Tap_A2	DO
79	Bit_09_Tap_A2	DO
80	Bit_08_Tap_A2	DO
81	Bit_07_Tap_A2	DO
82	Bit_06_Tap_A2	DO
83	Bit_05_Tap_A2	DO
84	Bit_04_Tap_A2	DO
85	Bit_03_Tap_A2	DO
86	Bit_02_Tap_A2	DO
87	Bit_01_Tap_A2	DO
88	Bit_00_Tap_A2	DO
89	*Not connected*	
90	Main_CLK	DI
91	VSSD	GND
92	LVAL_AB_2	DO
93	*Not connected*	
94	Bit_00_Tap_B2	DO
95	Bit_01_Tap_B2	DO
96	Bit_02_Tap_B2	DO
97	Bit_03_Tap_B2	DO
98	Bit_04_Tap_B2	DO
99	Bit_05_Tap_B2	DO
100	Bit_06_Tap_B2	DO
101	Bit_07_Tap_B2	DO
102	Bit_08_Tap_B2	DO
103	Bit_09_Tap_B2	DO
104	Bit_10_Tap_B2	DO
105	Bit_11_Tap_B2	DO
106	VSSD	GND
107	Bit_11_Tap_E1	DO
108	Bit_10_Tap_E1	DO
109	Bit_09_Tap_E1	DO
110	Bit_08_Tap_E1	DO
111	Bit_07_Tap_E1	DO
112	Bit_06_Tap_E1	DO
113	Bit_05_Tap_E1	DO
114	Bit_04_Tap_E1	DO
115	Bit_03_Tap_E1	DO

Pin number	Pin name	Pin type(1)
116	Bit_02_Tap_E1	DO
117	Bit_01_Tap_E1	DO
118	Bit_00_Tap_E1	DO
119	*Not connected*	
120	VSSD	GND

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

Table 41: Connector 2 pinout

Pin number	Pin name	Pin type(1)
1	VSSD	GND
2	LVAL_EF_1	DO
3	*Not connected*	DO
4	Bit_11_Tap_A1	DO
5	Bit_10_Tap_A1	DO
6	Bit_09_Tap_A1	DO
7	Bit_08_Tap_A1	DO
8	Bit_07_Tap_A1	DO
9	Bit_06_Tap_A1	DO
10	Bit_05_Tap_A1	DO
11	Bit_04_Tap_A1	DO
12	Bit_03_Tap_A1	DO
13	Bit_02_Tap_A1	DO
14	Bit_01_Tap_A1	DO
15	Bit_00_Tap_A1	DO
16	VSSD	GND
17	*Not connected*	
18	*Not connected*	
19	*Not connected*	
20	*Not connected*	
21	*Not connected*	
22	*Not connected*	
23	*Not connected*	
24	*Not connected*	
25	*Not connected*	

Pin number	Pin name	Pin type[1]
26	*Not connected*	
27	*Not connected*	
28	*Not connected*	
29	*Not connected*	
30	*Not connected*	
31	VSSD	GND
32	*Not connected*	
33	*Not connected*	
34	*Not connected*	
35	*Not connected*	
36	*Not connected*	
37	*Not connected*	
38	*Not connected*	
39	*Not connected*	
40	*Not connected*	
41	*Not connected*	
42	*Not connected*	
43	*Not connected*	
44	*Not connected*	
45	*Not connected*	
46	VSSD	GND
47	Bit_00_Tap_F1	DO
48	Bit_01_Tap_F1	DO
49	Bit_02_Tap_F1	DO
50	Bit_03_Tap_F1	DO
51	Bit_04_Tap_F1	DO
52	Bit_05_Tap_F1	DO
53	Bit_06_Tap_F1	DO
54	Bit_07_Tap_F1	DO
55	Bit_08_Tap_F1	DO
56	Bit_09_Tap_F1	DO
57	Bit_10_Tap_F1	DO
58	Bit_11_Tap_F1	DO
59	*Not connected*	
60	VSSD	GND
61	N_CS_EF_1	DI
62	MISO_EF_1	DO
63	*Not connected*	

Pin number	Pin name	Pin type[1]
64	*Not connected*	
65	VSSD	GND
66	VSSD	GND
67	VSSA	GND
68	Load_Pulse_EF_1	DI
69	*Not connected*	
70	End_ADC_EF_1	DO
71	*Not connected*	
72	*Not connected*	
73	*Not connected*	
74	*Not connected*	
75	VSSD	GND
76	VSSD	GND
77	VSSA	GND
78	*Not connected*	
79	*Not connected*	
80	*Not connected*	
81	*Not connected*	
82	VSSD	GND
83	VSSD	GND
84	VSSD	GND
85	VSSA	GND
86	Pixel_CLK_EF_1	DO
87	*Not connected*	
88	Sample_EF	DI
89	RST_CDS_EF	DI
90	RST_CVC_EF	DI
91	ID_Chip	
92	*Not connected*	
93	*Not connected*	
94	*Not connected*	
95	*Not connected*	
96	*Not connected*	
97	*Not connected*	
98	*Not connected*	
99	VSSD	GND
100	VSSD	GND
101	VSSA	GND

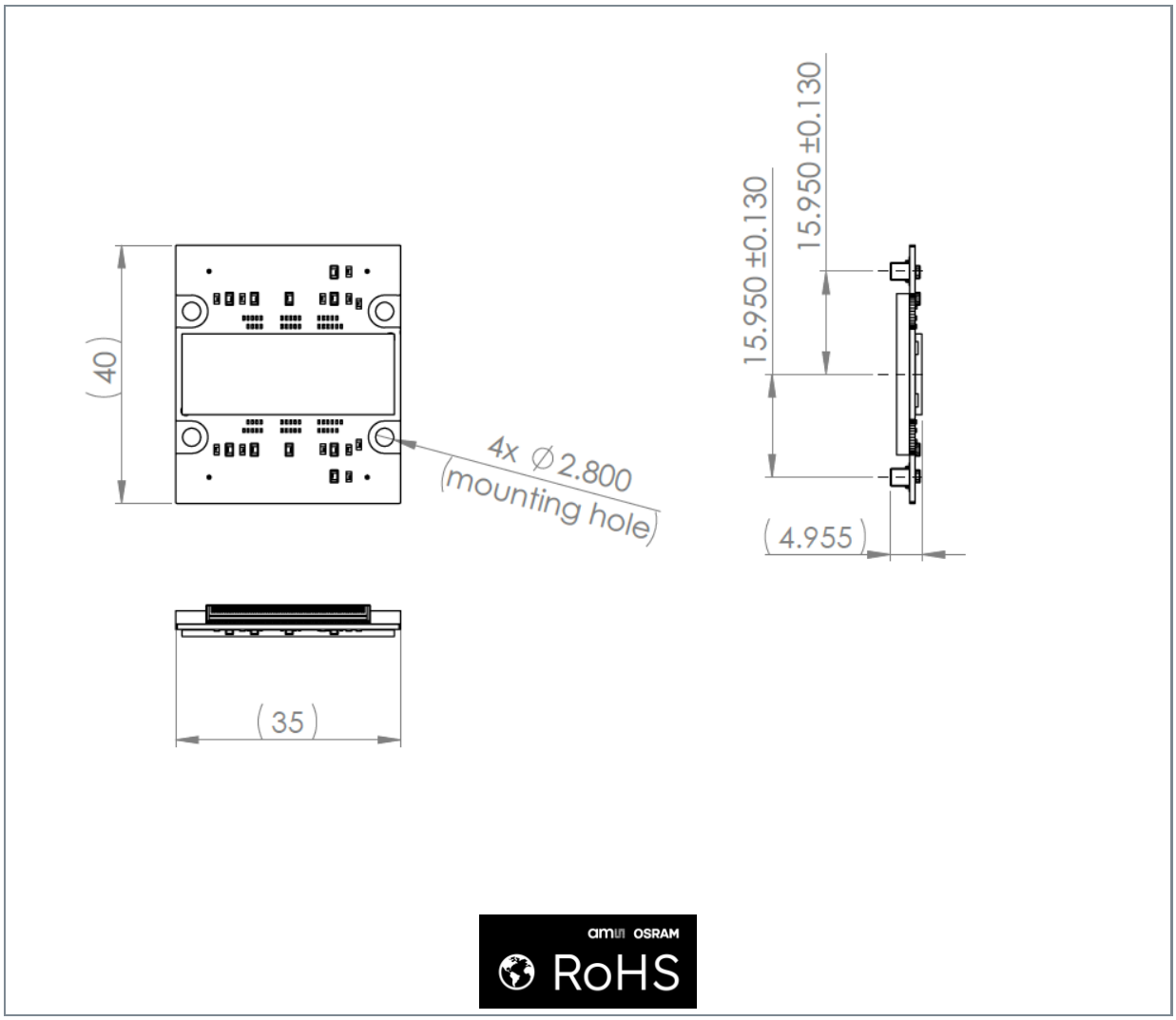
Pin number	Pin name	Pin type(1)
102	*Not connected*	
103	*Not connected*	
104	*Not connected*	
105	*Not connected*	
106	VDDD	3.3V
107	VSSD	GND
108	VSSA	GND
109	*Not connected*	
110	*Not connected*	
111	*Not connected*	
112	*Not connected*	
113	*Not connected*	
114	VDDD	3.3V
115	VSSD	GND
116	VSSD	GND
117	VSSA	GND
118	N_Reset_EF	DI
119	*Not connected*	
120	*Not connected*	

(1) Explanation of abbreviations:
DI Digital Input
DO Digital Output

13 Package drawings & markings

13.1 DR2K7 / DR2x2K7 / DR4K3.5 INVAR

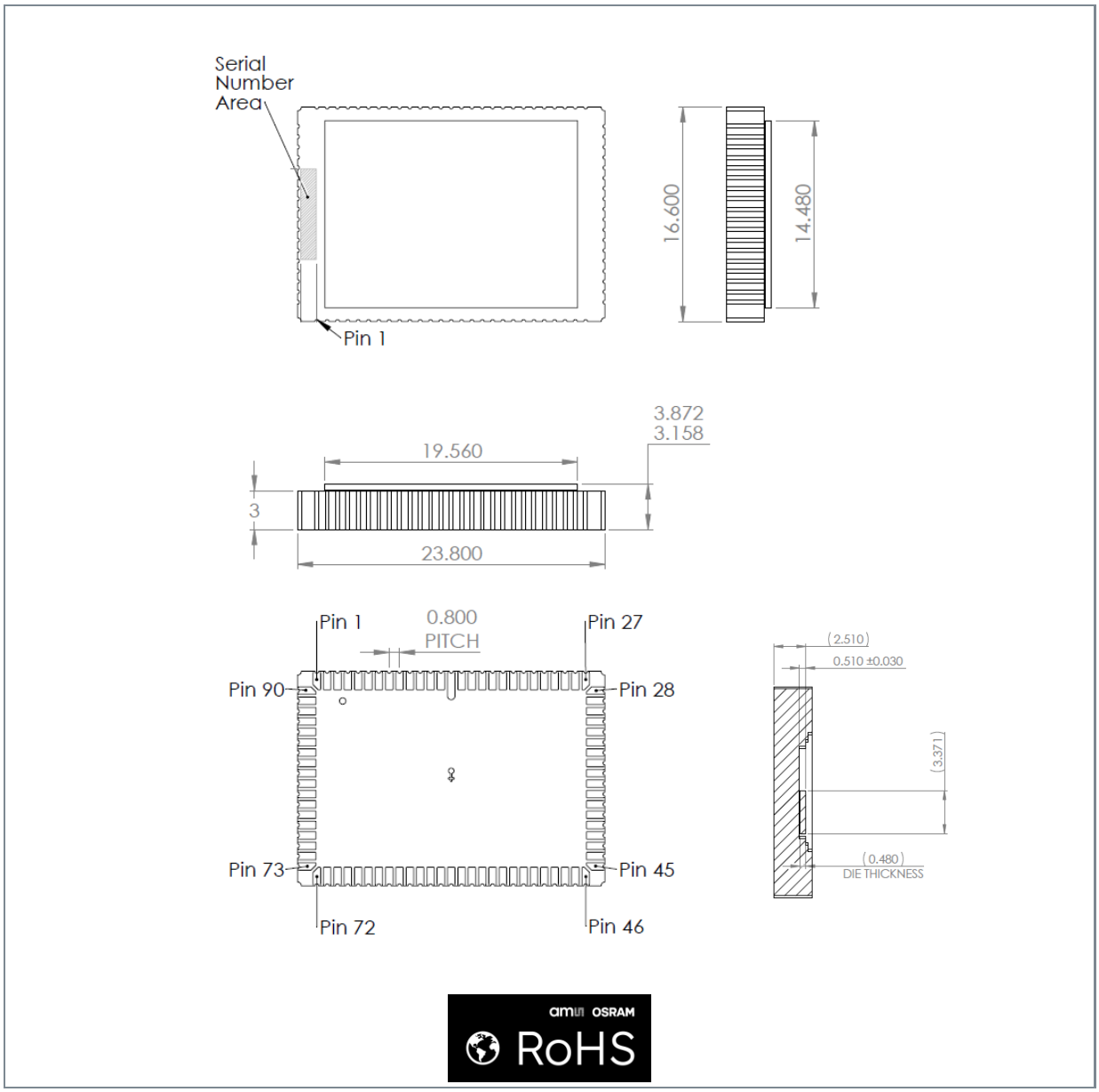
Figure 34: DR2K7 / DR2x2K7 / DR4K3.5 Invar package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.2 DR2K7 LCC ceramic

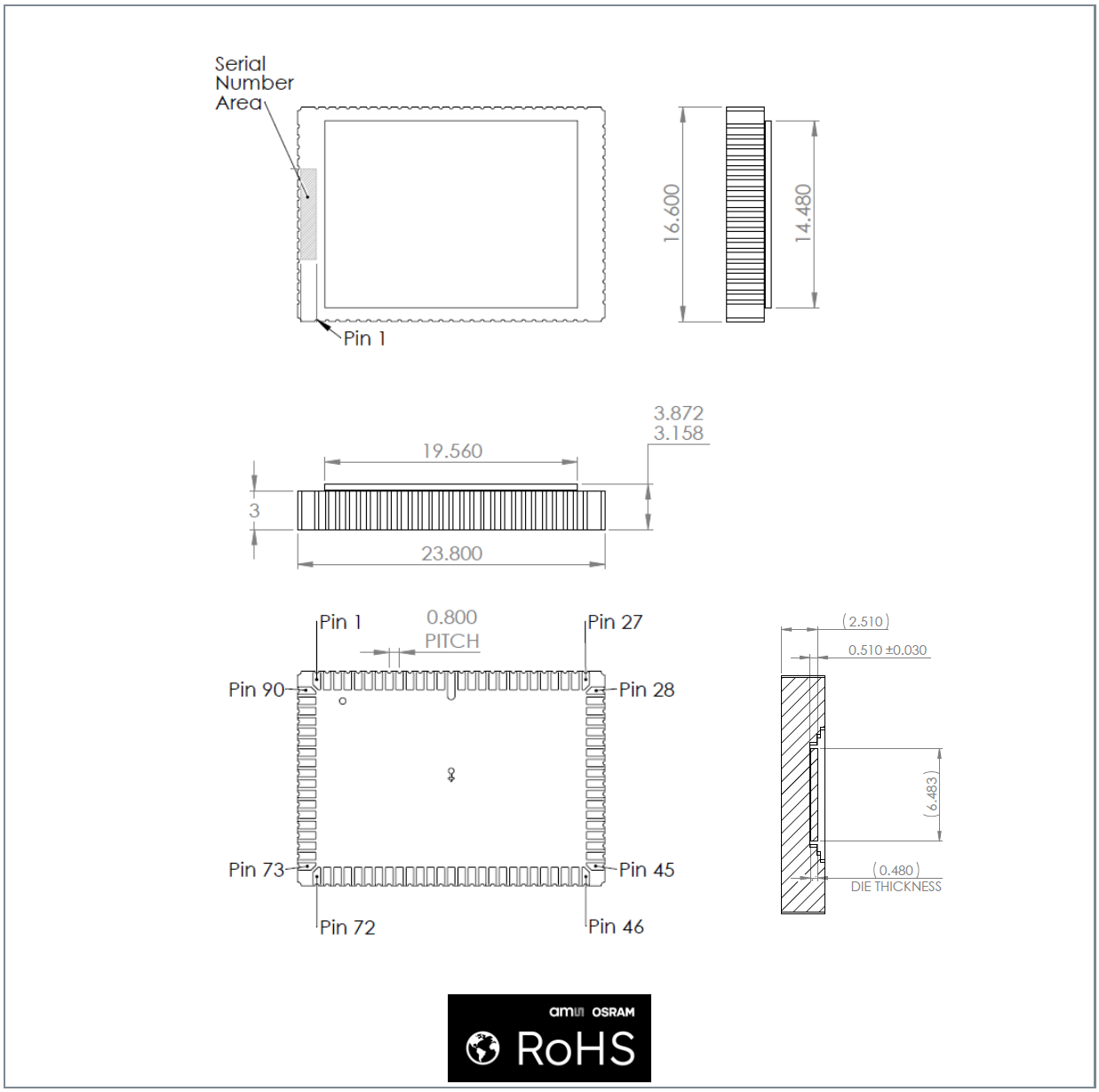
Figure 35: DR2K7 LCC ceramic package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.3 DR2x2K7 LCC ceramic

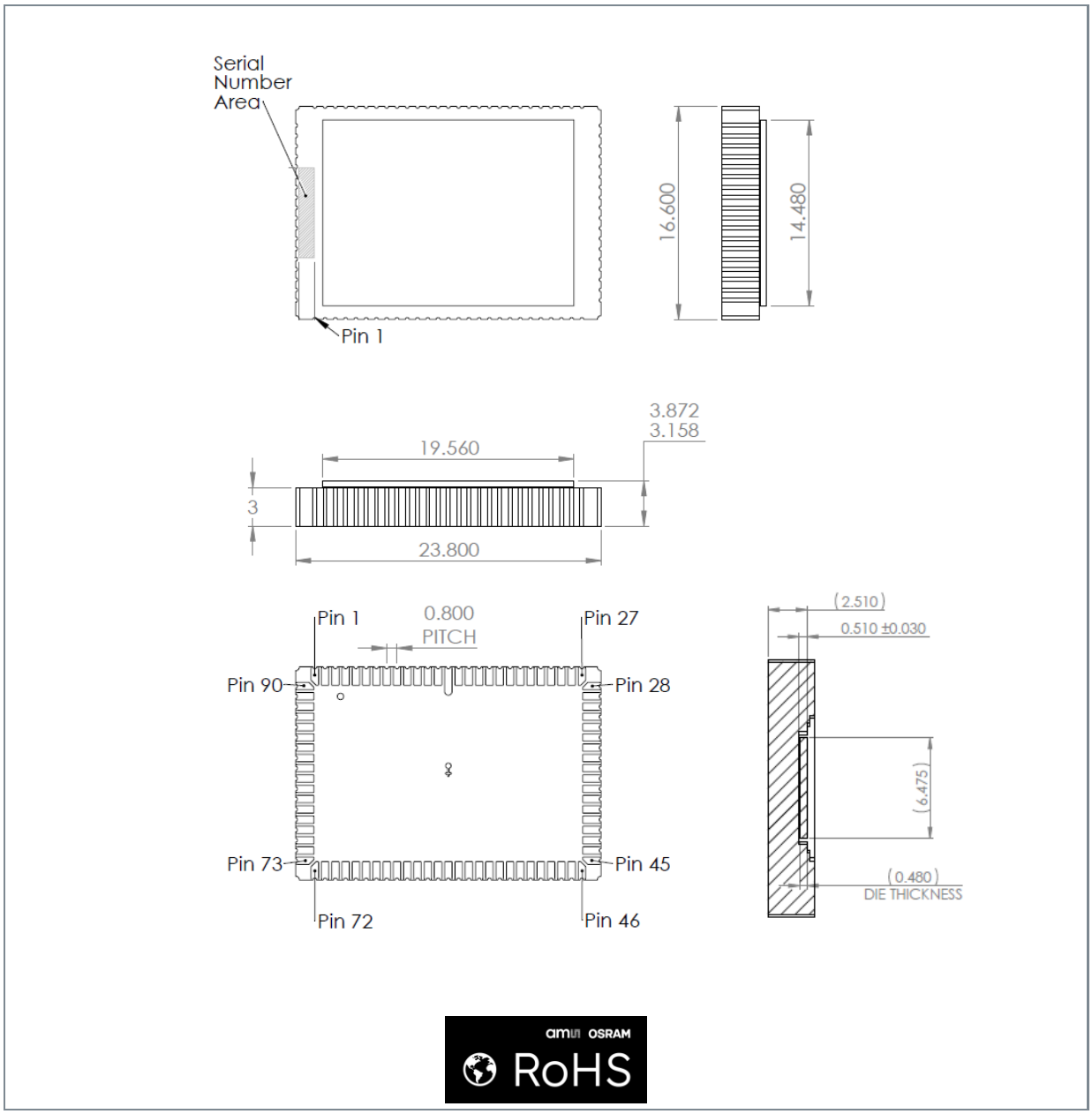
Figure 36: DR2x2K7 LCC ceramic package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.4 DR4K3.5 LCC ceramic

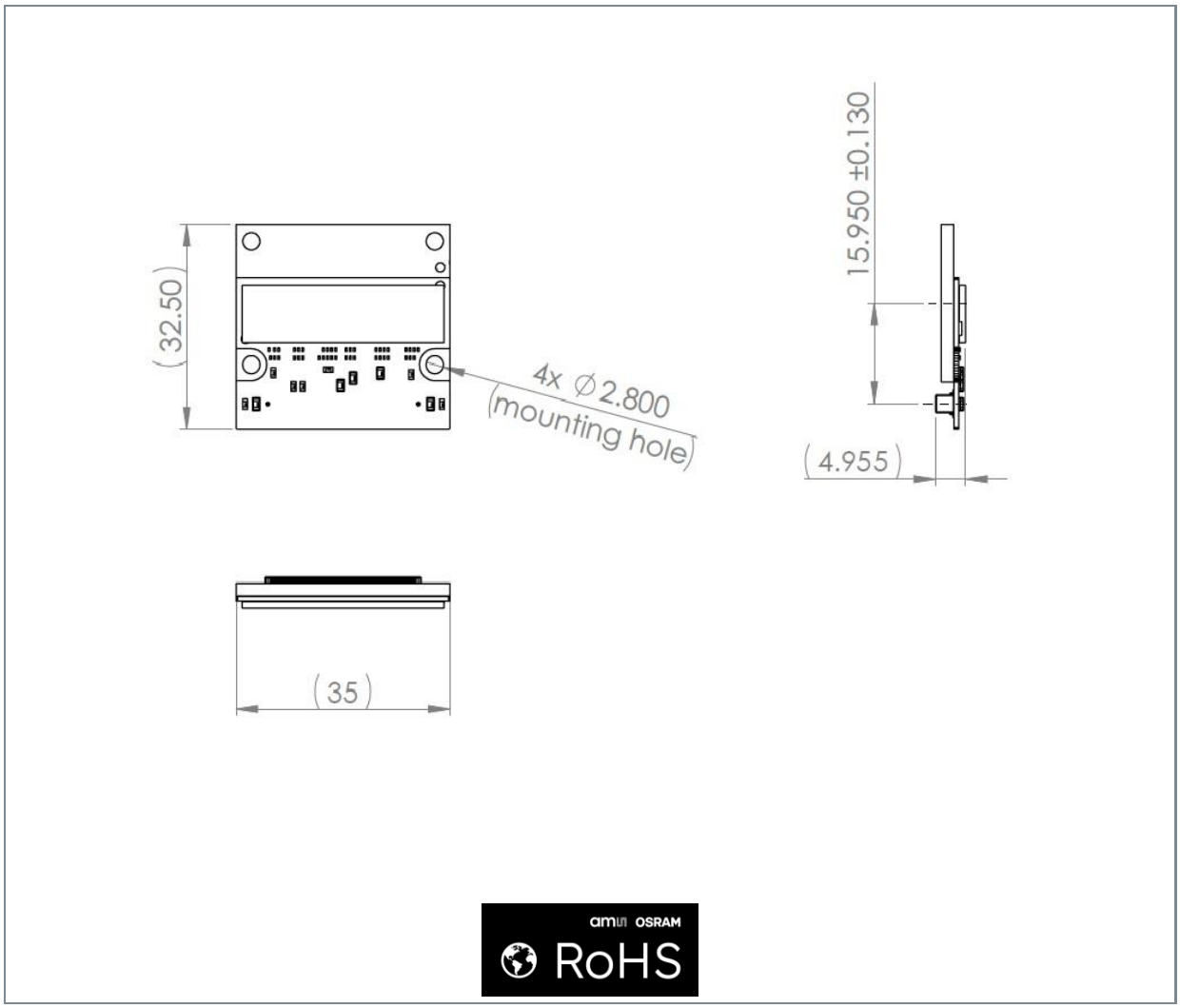
Figure 37: DR4K3.5 LCC ceramic package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.5 DR4K7 INVAR

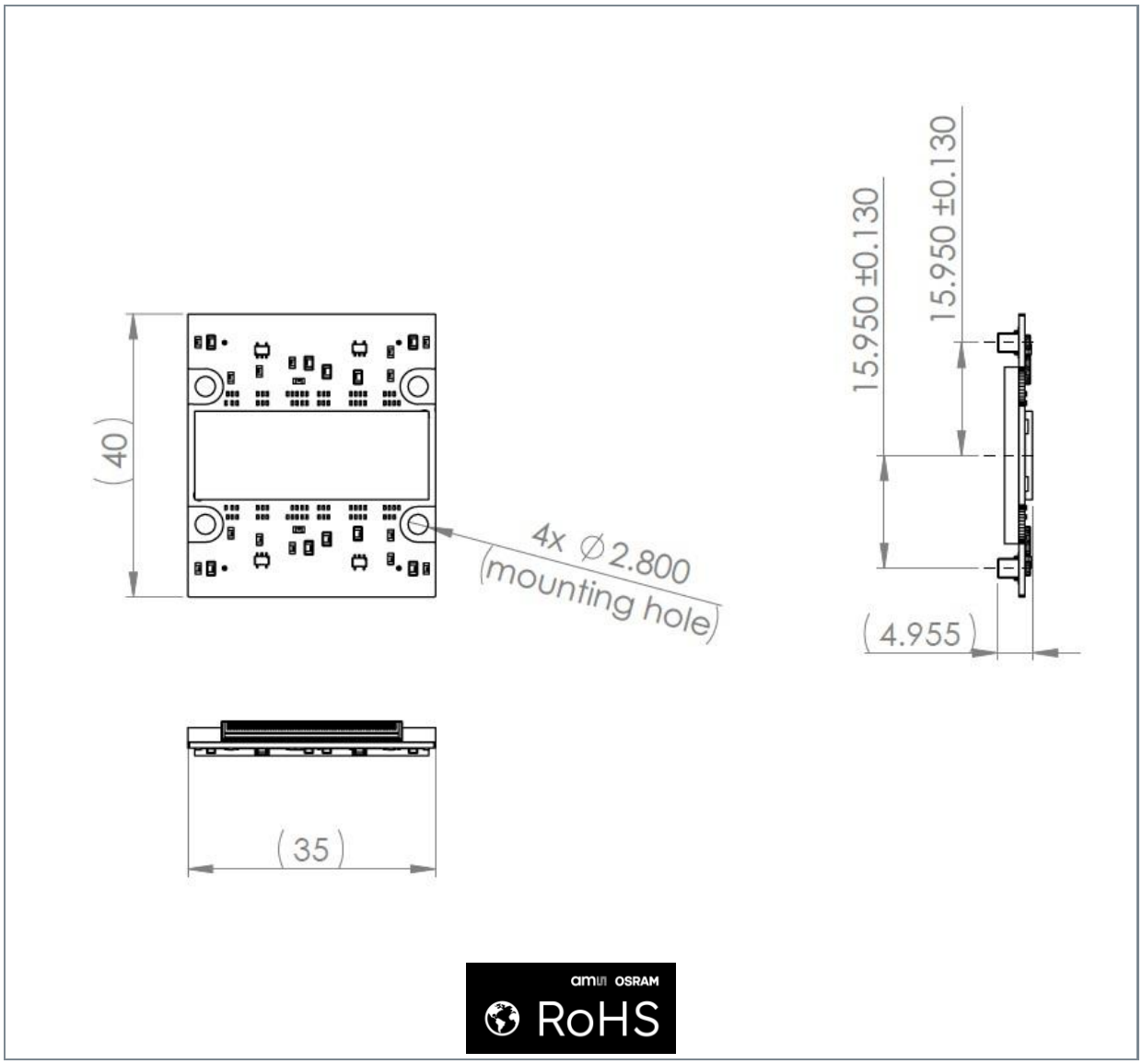
Figure 38: DR4K7 Invar package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.6 DR2x4K7 / DR8K3.5 INVAR

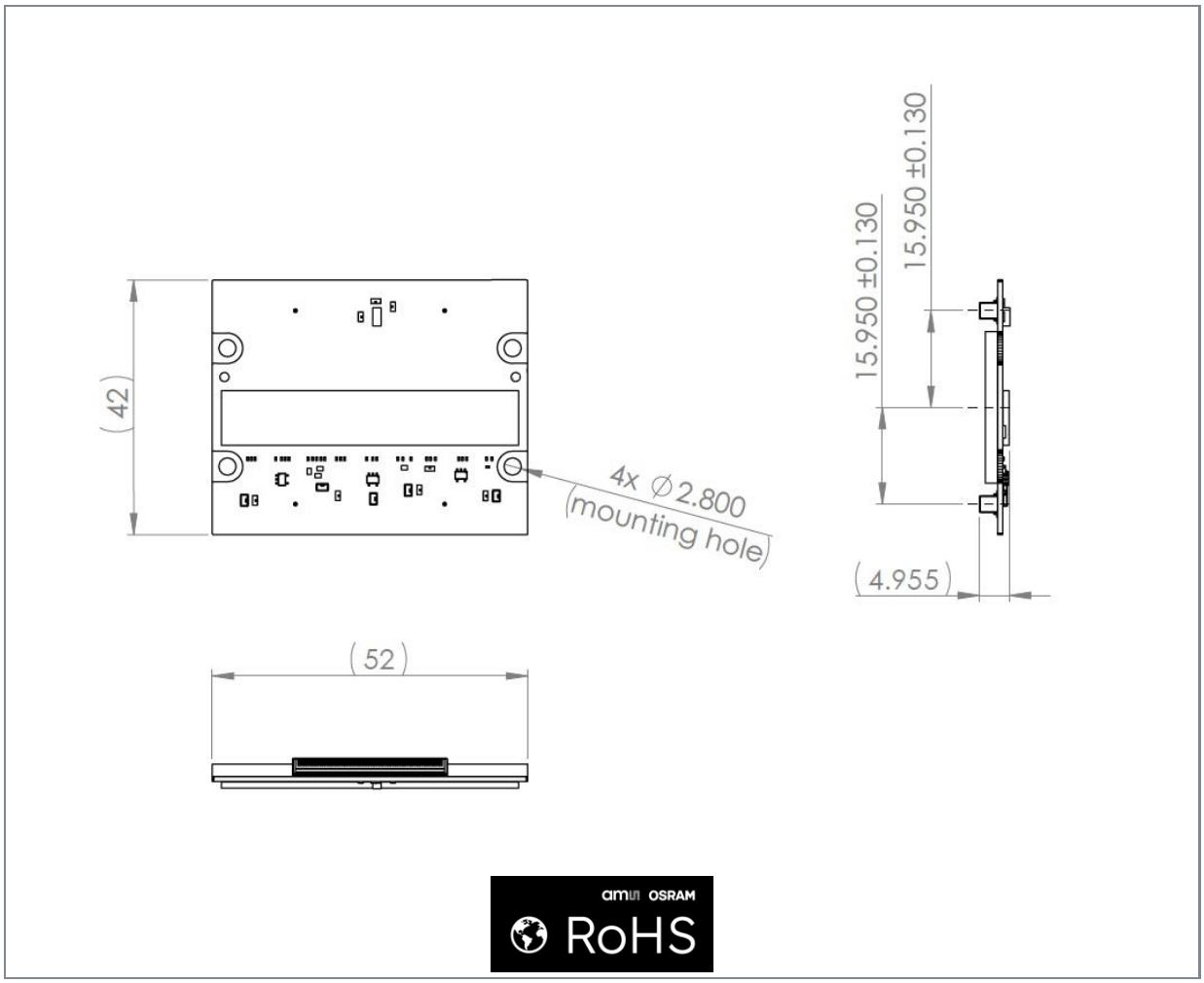
Figure 39: DR2x4K7 / DR8K3.5 Invar package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.7 DR6K7 INVAR

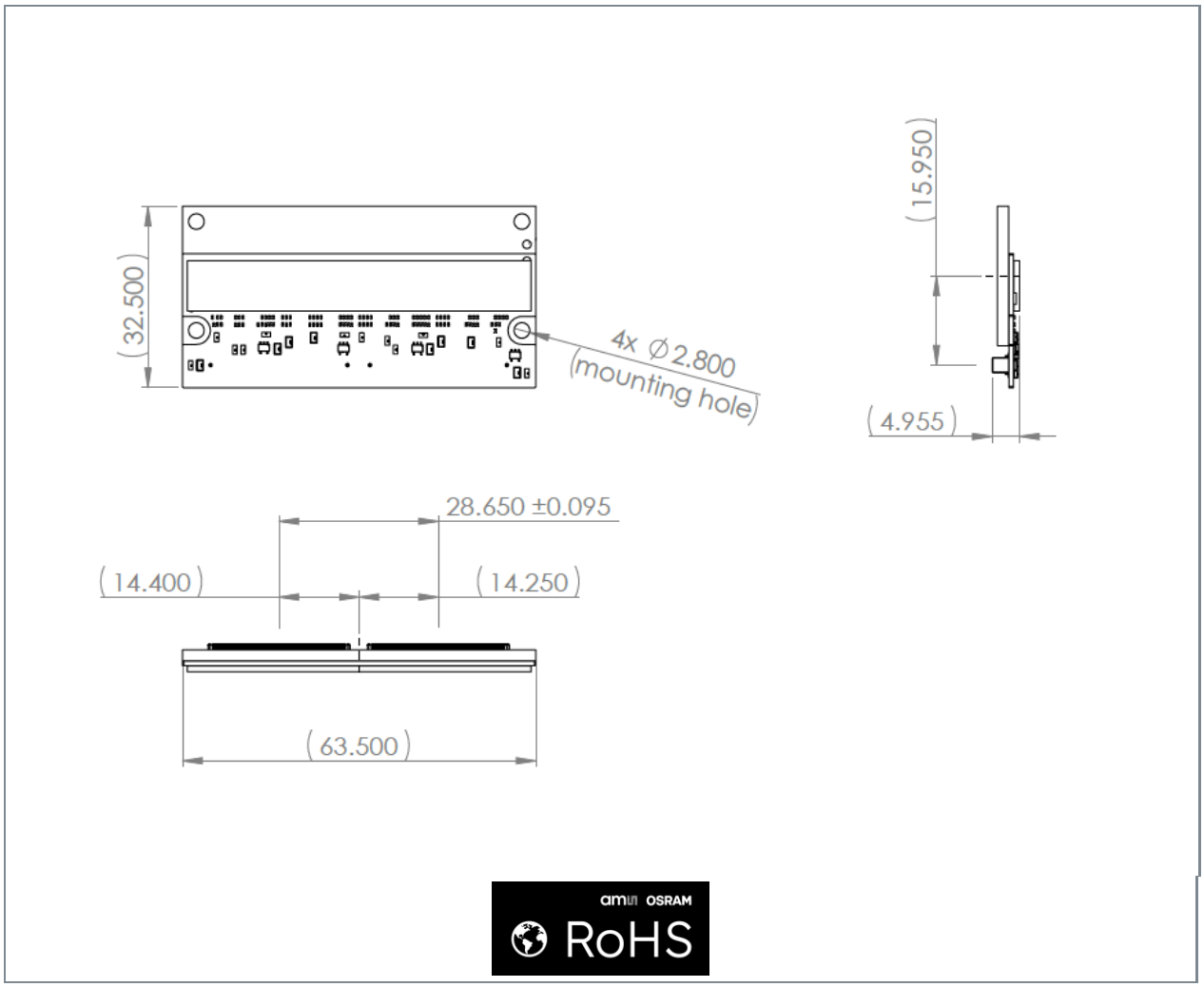
Figure 40: DR6K7 Invar package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.8 DR8K7 INVAR

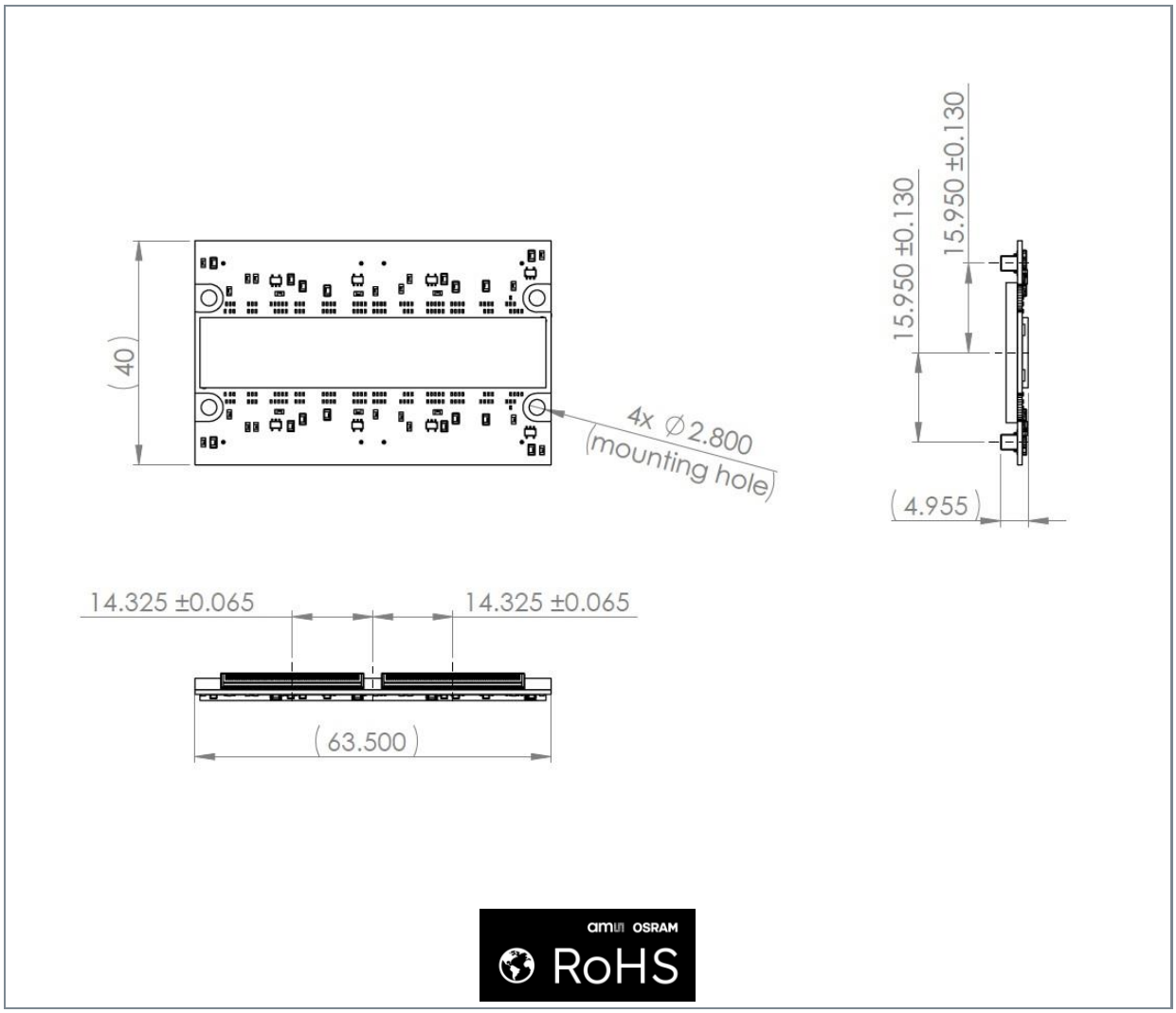
Figure 41: DR8K7 Invar package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

13.9 DR2x8K7 / DR16K3.5 INVAR

Figure 42: DR2x8K7 / DR16K3.5 Invar package outline drawing



(1) All dimensions are in millimeters. Angles in degrees.
(2) If not otherwise noted all tolerances are ±0.1 mm.
(3) This package contains no lead (Pb).
(4) This drawing is subject to change without notice.

Information: Indicates useful practical hints.

For additional support on mechanical drawings, please contact the Technical Support Team

14 Revision information

Document status	Product status	Definition
Product Preview	Pre-development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams-OSRAM AG standard warranty as given in the General Terms of Trade

Other definitions

Draft / Preliminary:
The draft / preliminary status of a document indicates that the content is still under internal review and subject to change without notice. ams-OSRAM AG does not give any warranties as to the accuracy or completeness of information included in a draft / preliminary version of a document and shall have no liability for the consequences of use of such information.

Short datasheet:
A short datasheet is intended for quick reference only, it is an extract from a full datasheet with the same product number(s) and title. For detailed and full information always see the relevant full datasheet. In case of any inconsistency or conflict with the short datasheet, the full datasheet shall prevail.

Changes from previous released version to current revision v4-01	Page
Changes from v3.2.8 to v4-00	
Update to ams OSRAM template	all
Updated Ordering Information	7
Added table regarding the sensor's shared headboard and footprint	13
Updated typical power consumption values	16, 17
Updated Spectral Response Graph	20
Added comment on ADC resolution	22, 44-45
Added comment on offset subtraction feature	45
Updated mechanical drawings	91-99
Changes from v4-00 to v4-01	
Updated soldering information	57-58
Updated mechanical drawings	91- 99

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

15 Legal information

Copyright & disclaimer

Devices sold by ams-OSRAM AG are covered by the warranty and patent indemnification provisions appearing in its General Terms of Trade. ams-OSRAM AG makes no warranty, express, statutory, implied, or by description regarding the information set forth herein. ams-OSRAM AG reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with ams-OSRAM AG for current information. This product is intended for use in commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by ams-OSRAM AG for each application. This product is provided by ams-OSRAM AG “AS IS” and any express or implied warranties, including, but not limited to the implied warranties of merchantability and fitness for a particular purpose are disclaimed.

ams-OSRAM AG shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interruption of business or indirect, special, incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of ams-OSRAM AG rendering of technical or other services.

Product and functional safety devices/applications or medical devices/applications:
ams-OSRAM AG components are not developed, constructed or tested for the application as safety relevant component or for the application in medical devices. ams-OSRAM AG products are not qualified at module and system level for such application.

In case buyer – or customer supplied by buyer – considers using ams-OSRAM AG components in product safety devices/applications or medical devices/applications, buyer and/or customer has to inform the local sales partner of ams-OSRAM AG immediately and ams-OSRAM AG and buyer and /or customer will analyze and coordinate the customer-specific request between ams-OSRAM AG and buyer and/or customer.

ams OSRAM semiconductor RoHS compliance statement

RoHS compliant: The term RoHS compliant means that ams-OSRAM AG semiconductor products fully comply with current RoHS directives. Our semiconductor products do not contain any chemicals for all 6 substance categories plus additional 4 substance categories (per amendment EU 2015/863), including the requirement that lead not exceed 0.1% by weight in homogeneous materials.

Important information: The information provided in this statement represents ams-OSRAM AG knowledge and belief as of the date that it is provided. ams-OSRAM AG bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. ams-OSRAM AG has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. ams-OSRAM AG and ams-OSRAM AG suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

Headquarters
ams-OSRAM AG
Tobelbader Strasse 30
8141 Premstaetten
Austria, Europe
Tel: +43 (0) 3136 500 0

Please visit our website at ams-osram.com
For information about our products go to Products
For technical support use our Technical Support Form
For feedback about this document use Document Feedback
For sales offices and branches go to Sales Offices / Branches
For distributors and sales representatives go to Channel Partners

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

ams OSRAM:

DR2X2K7_INVAR_B&W_V6 DR2X2K7_INVAR_RGB_V6 DR2X4K7_INVAR_B&W_V6 DR2X4K7_INVAR_RGB_V6 DR2X8K7_INVAR_B&W_V5 DR2X8K7_INVAR_RGB_V5 DR4K3.5_INVAR_B&W_V6 DR6K7_BM_V2 DR2K7_LCC_B&W_BM_CERAMIC_V1.0 DR2X2K7_LCC_B&W_CERAMIC_V1.0 DR2X2K7_LCC_RGB_CERAMIC_V1.0 DR16K3.5_INVAR_B&W_V6 DR2K7_INVAR_B&W_BM_V6 DR4K7_INVAR_B&W_BM_V5 DR8K3.5_INVAR_B&W_BM_V6 DR8K7_INVAR_B&W_BM_V6 DR4K3.5_LCC_B&W_Ceramic_V1.0