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Coverpage: AS89010 Datasheet

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DATASHEET
AS89010

16 bit 4-channel analog-to-digital converter (ADC) with I²C control/output
SSOP16
Order No.: 305030004
Status: preliminary

FEATURES

- Conversion of 4 sensor signals of photodiodes (e.g. RGB/XYZ color plus one blank channel for compensation of parasitic currents or temperature conversion) or other sensors with current signal output
- Configurable conversion gain and integration time supports a very high dynamic range of 1 – 2.68E+08
- Up to 16 bit (internal 20 bit) signal resolution by achievable sensitivity up to 20 fA/LSB – scaling (by a divider) the internal 20 bit on 16 bit output
- Adjustable operation modes like continuous, by command and externally synchronized (by given start and start/end signal) measurement
- Option: external control of integration time and reference current (gain)
- High linearity of amplifying, no cross talking
- High absolute accuracy without additional sources
- High reliability internal reference source generation
- Consideration of negative offset
- Measurement of current for both polarities
- Measurement of integration time
- Supply and temperature independent response
- Insensitive to 50 Hz/60 Hz external disturbances
- 16 Bit/400 kHz fast I²C interface with programmable slave addresses
- Very low current consumption in active, in *Power down* and Standby mode
- Supply voltage 2.7 V to 3.6 V
- Temperature range -40°C to 125°C
- Deliverable in SMD package and as bare die

APPLICATIONS

- Precise conversion of average e.g. integral photo current for optical sensors and arrays (e.g. UV, VIS, IR) and other sensors with current output
- In combination with ams Sensors Germany's color sensors: measurement of lights – chromaticity coordinates (XYZ CIE 1931, DIN 5033 and similar) or color temperatures to control and process displays and backlights (e.g. LED, CCFL)
- In combination with ams Sensors Germany's color and spectral sensors: measurement of reflective and/or transmitted light – chromaticity coordinates (XYZ CIE1931, DIN5033 and similar) measurement of objects and surfaces for analyzes, quality management, sorting, etc.

MARKET SEGMENTS

- Lighting SSL, Photometry
- Chemical and biochemical analyses
- Industrial process control
- Medical and environment instrumentation
- Industrial/commercial lighting
- Infotainment (backlights and video walls) and monitors
- High quality consumer displays and tablets

1 GENERAL DESCRIPTION

The ASIC AS89010 is a low noise sensor interface application specific standard product (ASSP) and suitable for coupling of multi-channel optical sensors or sensors using current output. It converts input currents of for example photodiodes (both polarities) to a digital output and realizes a continuous or triggered measurement via current integration. Optional the integration time and sensitivity can be controlled by external programming to extend the internal functions and parameters. The four signal channels convert directly and simultaneously the input currents to a digital representation of the measured average. The channels may be divided into three signal channels and one dummy channel for compensation of parasitic currents. This ASIC is especially suitable for signal conditioning of photodiodes of array sensors like color or other optical sensors with maximum of 4 channels per chip[1]. A configurable conversion gain factor and integration time support a dynamic range[2] of 1 - 2.68E+08 and achieves an accuracy of up to 16 bit signal resolution with sensitivity up to 20 fA/LSB.

The internal reference generations offers a high reliability. The converter is insensitive to a 50 Hz/60 Hz external disturbances and was especially designed to accommodate high accuracy at high sensitivity offering high robustness. Automatic *Power down* (sleep function) between subsequent measurements offers operation with very low current c60onsumption. Further, it offers a wide range of reference currents (1.25 nA to 5 µA), integration times (1 ms to 1 s), synchronized mode and other control modes adjustable by user programming. The conversion data can be accessed via 16 bit/400 kHz fast I²C Interface with programmable slave addresses. Measurement of actual integration time for a full triggered measurement can be performed.

AS89010's supported operating modes depending on required performance:

- *CMD Mode* – single measurement and conversion (controlled via I²C bus),
- *CONT Mode* - continuous measurement and conversion (periodically recurring measuring cycles) until "Stop" controlled via I²C bus,
- SYN[x] modes - synchronized measurement and conversion:
  - [*SYNS Mode*] synchronization of start,
  - [*SYND Mode*] synchronization of start and stop of measuring cycle on the falling edge of the SYN pin.

The settings for the input current range and integration time are not affected by alternative modes. Further the converter supports functions like *Power down* and *Standby*. It represents a low power solution and is also suitable for mobile applications.

Based on the high flexibility the AS89010 is suitable as converter for a width range of multi-channel sensors with current output. The device achieves a high dynamic range especially in (back) light applications and in measurements of integral intensity of pulsed light. The combination of ams Sensors Germany's color sensors with AS89010 is excellently suited for photometry applications (brightness, color coordinate and/or color temperature), for determining current values for control of spectrally mixed LED light sources or as sensors for display and (back)light calibration and mobile devices for light measurement. The sensor signal IC is available in SMD housing or can be supplied as a bare die.

[1] Upon consideration of that I²C address more ASICs may be used in parallel to a sensor to convert more than 4 sensor channels. In that case special operating notes must be considered.

[2] $$Dynamic\ Range = \frac{MAX\ measureable\ value\ = Max.Full\ Scale\ Range}{MIN\ measureable\ value = Min.Least\ Significant\ Bit}$$

2 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Violations of absolute maximum conditions are not allowed under any circumstances; otherwise the IC can be destroyed.

All voltages are referenced to VSSA = VSS = 0 V.

Table 1: Maximum conditions

PARAMETER	NAME	MIN	MAX	UNIT
Power Supply (analog)	VDDA	-0.5	5.0	V
Input and Output Voltages (analog)	VIOA	-0.5	VDDA+0.5	V
Power Supply (digital)	VDD	-0.5	5.0	V
Input and Output Voltages (digital)	VIOD	-0.5	VDD+0.5	V
Supply Voltage Difference[3] VDDD-VDDA	DIFF_VDD		0.3	V
Ambient Temperature	TOP	-40	125	°C
Storage Temperature	TSTG	-55	150	°C
Weight	m		0.076	g

2.2 Recommended Operating Conditions

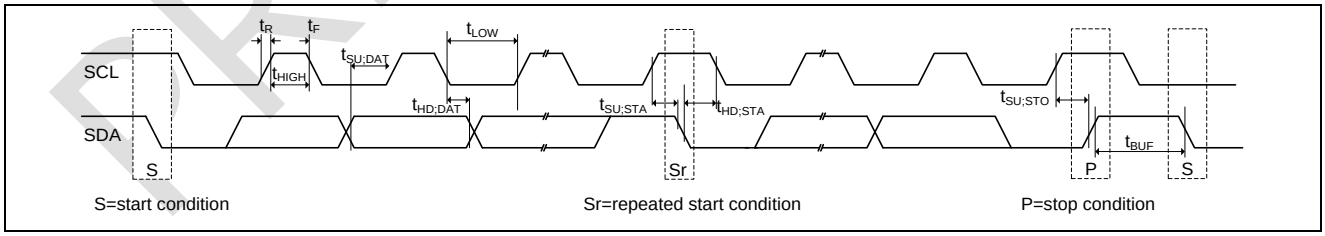
Table 2: Operational conditions; VSSA=VSS=0 V

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Supply Voltage	VDDA VDD	2.7	3.3	3.6	V	|VDDA-VDD| < 0.3 V
External Resistor[4]	REXT		3.3		MΩ	±1%
Temperature Coefficient of REXT	TC_{REXT}			50[5]	ppm/K	
Operating Temperature	T_{AMB}	-40		125	°C	
Pull Up Resistance at SCL, SDA	R_{I2C}	1.8[6]	4.7		kΩ	
Load Capacity at SDA	C_L			200	pF	
Input High Level	VIH	0.7			VDD	

[3] For the Digital Supply Voltage VDD it is not allowed to use a voltage above VDDA+0.3 V. This condition must be also complied during the ramp-up phase of the supply voltages.
[4] The resistor directly influences the generating of the reference current for the signal conversion. Therefore, the temperature coefficient of resistance has an important role. The smaller the temperature coefficient and the resistor value tolerance (1% better than 5%, etc.) result the more accurate the result of the converting.
[5] The smaller the better - the result depend on the sum of all TKs of the full sensor system (photo diode, REXT, converter, …)
[6] Lower resistance on request

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Input Low Level	VIL			0.3	VDD	
Output High Level	VOH	0.8			VDD	I_{Load} = 2.5 mA
Output Low Level	VOL			0.4	V	I_{Load} = 1.8 mA
Input Capacity at IN0 to IN3	CPD			80	pF	
SCL frequency	f_{SCL}	0		400	kHz	
SCL high pulse width	tHIGH	0.6			µs	
SCL high pulse width	tLOW	1.3			µs	
SCL, SDA rise time	tR			0.3	µs	
SCL, SDA fall time	tF			0.3	µs	
Hold time start condition	tHD;STA	0.6			µs	
Setup time start condition	tSU;STA	0.6			µs	
Data hold time write[7]	tHD;DATM	0.02		0.9	µs	
Data setup time	tSU;DAT	0.1			µs	
Setup time stop condition	tSU;STO	0.6			µs	
Bus free time between a stops and start condition	tBUF	1.3			µs	
SYN negative pulse width	tSYN	1.5			µs	SYN recognized as start/end of integration

Figure 1: I²C interface timing diagram



[7] Data transfer direction from Master to slave (AS89010) - Write

2.3 Electrical Characteristics

Table 3: Specifications; VSSA=VSS=0 V; VDDA=VDD=2.7 V to 3.6 V REXT=3.3 MΩ; TAMB = –25°C to 85°C, unless otherwise noted

PARAMETER	NAME	MIN	TYP	MAX	UNIT	CONDITION
Analog Supply Current	IVDDA		0.72	1	mA	measurement active
Digital Supply Current	IVDD		0.23	0.29	mA	measurement active or Standby mode
Power down Supply Current IPD = IVDDA_PD + IVDD_PD	IPD		0.01	1	µA	*Power down* mode
Analog Standby Supply Current	IVDDA _SBY	200		400	µA	*Standby* mode, no measurement
Clock Frequency	f_{CLK}	0.75	1.024	1.25	MHz	
ADC Resolution	NR	10		20	bit	internal resolution
Conversion Time Tolerance	ΔTINT	-30		30	%	–40°C to 125°C
Integral Nonlinearity	INL	-0.2 -0.05		0.2 0.05	%	R=000b to 001b R=010b to 100b
Differential Nonlinearity	DNL			0.9	LSB	no missing codes
Start Up Time from Power down	T_{START}		500		µS	pp to measurement start
SYN Trigger Delay	T_{SYNDEL}			5	µs	from falling SYN edge to measurement start
Full-Scale-Range Error	EIFSR	-5		6	%	referred to nominal value
Gain Error (CONT, CMD, SYNS, SYND with processing of OUTINT time)	E_{GAIN}	-5		6	%	referred to nominal value
Gain Error (SYND without processing of OUTINT time)	E_{GAIN}	-20		20	%	referred to nominal value
Gain Matching Error[8]	E_{MATCH}	-2 -1.5		2 1.5	%	R=000b R=001b to 100b
Gain Temperature Drift	T_{CGAIN}		50	200	ppm/K	CONT, CMD, *SYNS Mode*
Gain Temperature Drift @ SYND	T_{CGSYND}		200	700	ppm/K	*SYND Mode*
Effective Resolution (TINT=64 ms, DIR=1)	ER	13.5 14.5 15.5	14 15 16		bit	R=000b R=001b to 011b R=100b
Data hold time read[9]	$t_{HD;DATS}$	0.3[1]		0.9[1]	µs	

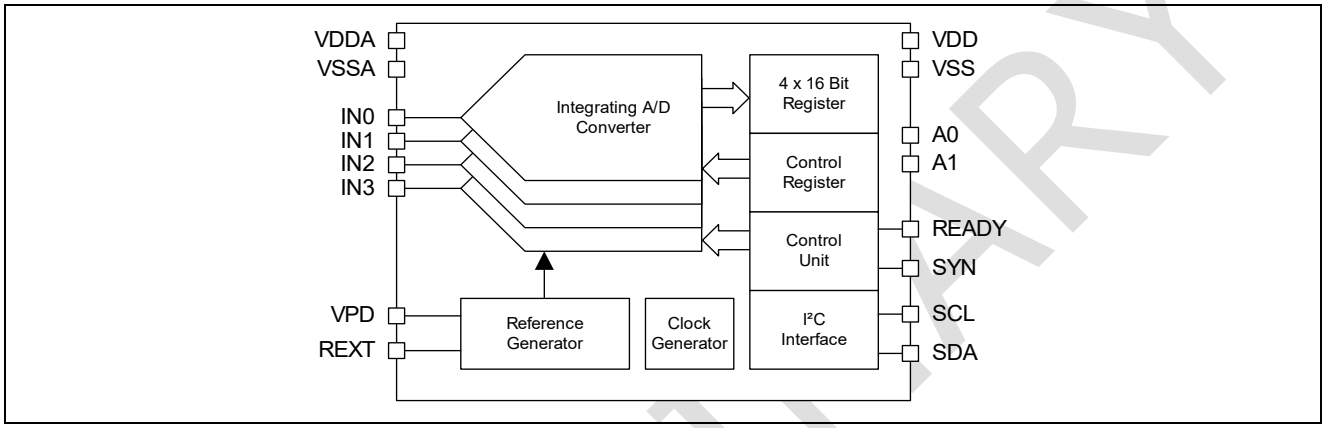
[8] Up to -1.5%...+1.5% for all gains available on request

[9] Data transfer direction from slave (AS89010) to Master (Read). The AS89010 provides a hold time of at least 300 ns and maximum of 900 ns for the SDA signal.

3 BLOCK DIAGRAM

The main components of the AS89010 are shown in Figure 2. The input currents are directly converted by Delta-Sigma to digital converter. The reference current for the A/D converters and optionally the bias voltage for the photodiodes VPD (see Figure 19) are provided by the internal reference generator[10]. The results of the A/D conversion are stored in four 16 bit registers and can be accessed via I²C interface. The input SYN can be used for an externally triggered start or start and stop of the measurement, the output READY gives the information of the status of the conversion. The I²C slave address is set by pins A0 and A1. Separated analog and digital power supply pins are used for noise decoupling.

Figure 2: Block diagram



4 PIN ASSIGNMENT

The Pin assignment is shown in the following table.

Table 4: Pin assignment (Analog/Digital)

PIN	TYPE	A/D	DESCRIPTION
VDDA	power	A	analog power supply voltage
VSSA	power	A	analog power supply voltage
VDD	power	D	digital power supply voltage (VDDA = VDD)
VSS	power	D	digital power supply voltage (VSSA = VSS)
IN0, IN1, IN2, IN3	input	A	input current
REXT	input	A	external resistor of 3.3 MΩ
VPD	output	A	photodiodes bias voltage (cathode or anode)
SCL	input	D	I²C clock input
SDA	input / output	D	I²C data input / output, open drain output stage
SYN	input	D	externally controlled conversion
READY	output	D	conversion status, push pull output stage
A0, A1	input	D	variable I²C slave address

[10] The external resistor REXT directly influences the generating of the reference current for the signal conversion. Therefore, the temperature coefficient of resistance has an important role. The smaller the temperature coefficient and the resistor value tolerance (1% better than 5%, etc.) result the more accurate the result of the converting.

5 DESCRIPTION OF FUNCTION

The AS89010 performs current to digital conversion by four parallel A/D converters. The sensitivity, start and stop of conversion are user defined and should be adapted to the application of interest. Upon the end of each conversion, the digital equivalents of the input currents are stored in the output register (OUT0 to OUT3). Pin READY stays at low logic level all the time during the conversion. Rising edge and following high logic level of READY signalizes the end of conversion.

5.1 Measurement Modes

There are four available modes how the measurement can be performed. According to the assignment of register CREGH:MODE (Table 11) one of four possible measurements can be performed by the device. However, it is always recommended regardless of the mode, to transfer no data via I²C during the measurement process. It is suggested to use the measurement-free time cycles for data transfer via I²C.

5.1.1 Continuous Measurement Mode (*CONT Mode*)

The A/D conversion will be performed sequentially. The first conversion starts with setting the SS bit in OSR register. If the *Standby* was active, the device deactivates it and initializes the continuous measurement. Measurement can only be stopped by resetting the SS bit. The conversion time (integration time TINT) is determined by the full-scale of the register CREGL:T (T). The rising edge of READY signalizes the end of each conversion. It is recommended to read output data during the break time between two consequent conversions in order to not disturb the integration operation. This break time can be configured in 4 µs steps up to 1,021 µs (see Table 13). The break time should be configured long enough to prevent overlapping of data fetch activity with the measurement. For further details see also Figure 21.

Figure 3: *CONT Mode* timing with short break time

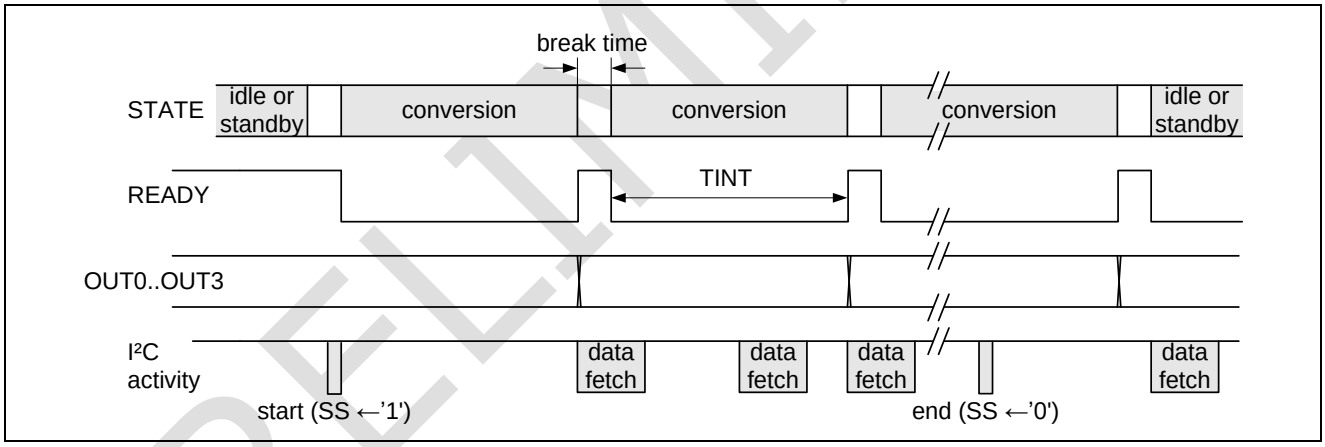
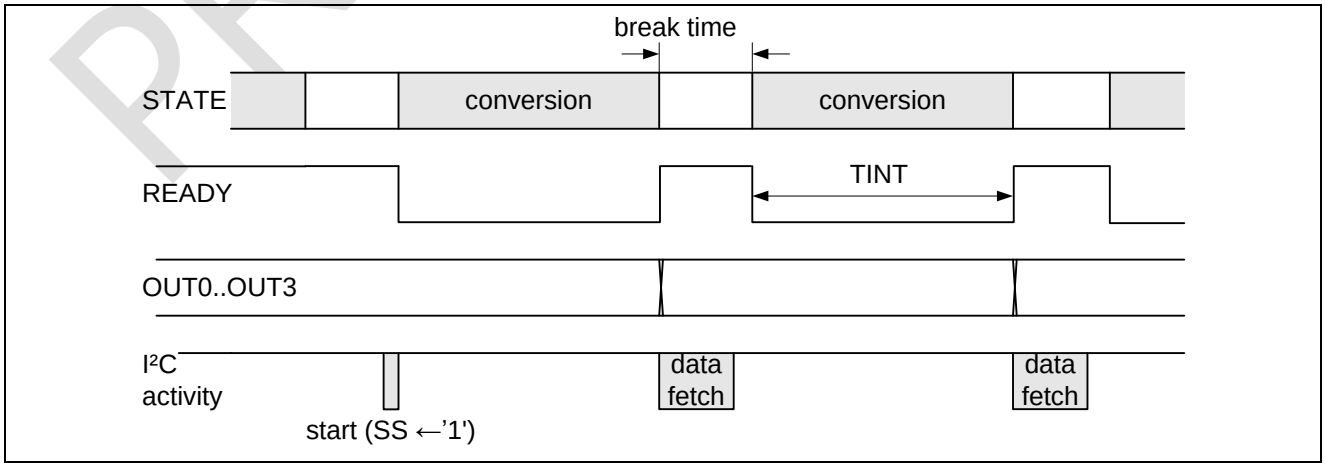


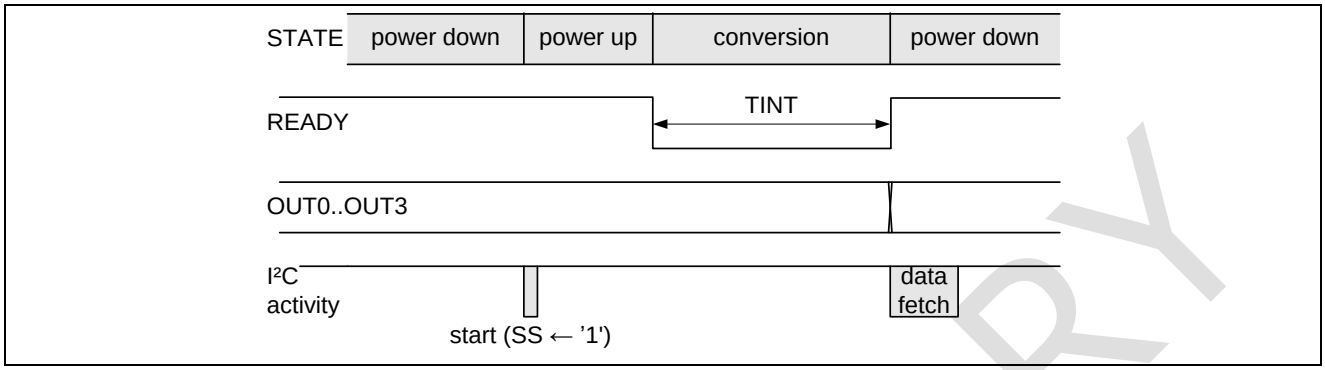
Figure 4: *CONT Mode* timing with long enough break time between subsequent conversions



5.1.2 Command Measurement Mode (*CMD Mode*)

This measurement enables a 'software start' of single conversion. Each conversion starts by setting the SS bit to '1' of OSR register. However, actually start of conversion depends on the chosen *Power down* activity. For further details see also Figure 21.

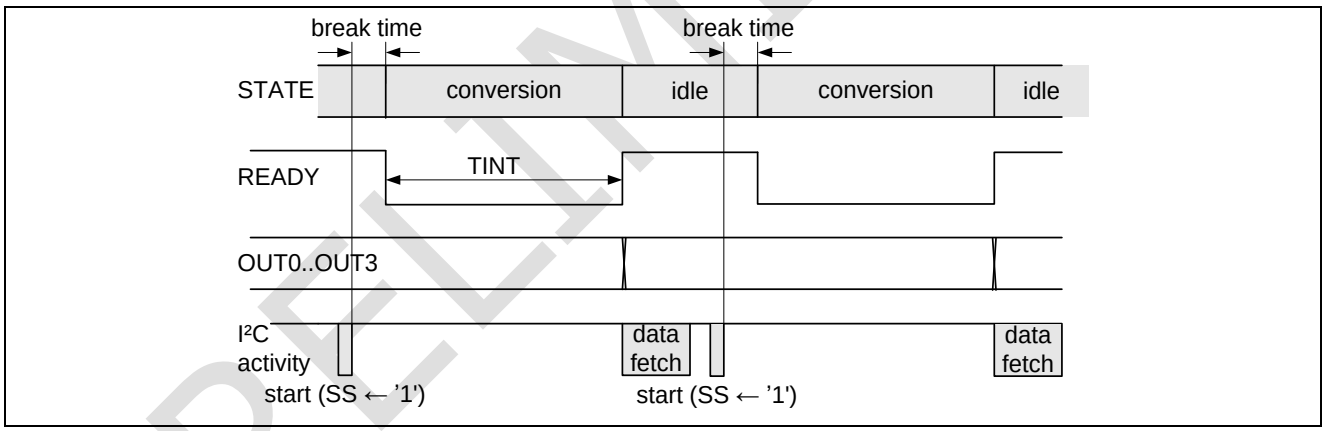
Figure 5: *CMD Mode* timing with activated *Power down*



If *Power down* has been activated (PD bit in OSR) the conversion starts after the Power-up, approximately 500 µs after the SS bit has been set (Figure 5). Otherwise it starts immediately after delay time defined by the content of BREAK register which can be configured in 1 µs steps up to 255 µs (Figure 6).

The rising edge of READY signalizes the end of conversion and the output data can be read via the I²C-Inteface (data fetch). After the conversion, the device returns to the *Power down* mode or stays active waiting (idle) for a new action according to the programmed configuration. The conversion time (integration time TINT) is determined by contents of the register CREGL:T (T).

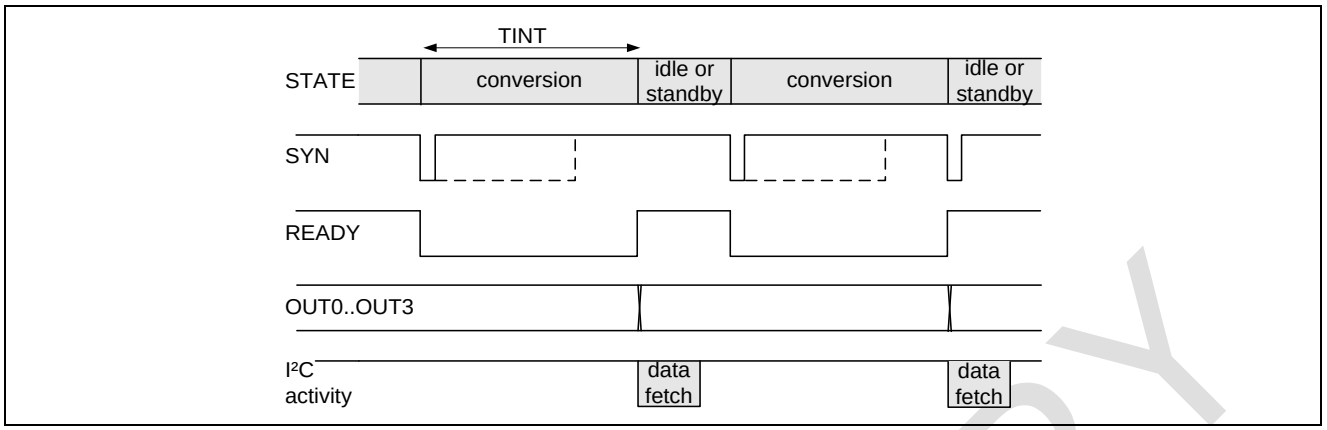
Figure 6: *CMD Mode* timing without *Power down*



5.1.3 Synchronous Measurement Start Mode (*SYNS Mode*)

The input pin SYN acts as a trigger event for the conversion start. The falling edge starts the measurement. The READY pin signalizes the progress of conversion, at rising edge the measurement is stopped and the current conversion results are stored into output registers. Data fetch should be performed between the rising edge of READY signal and the next falling edge of SYN in order to allow distortion free measurement. After the conversion the device changes its state to *Standby* or stays active waiting (idle), according to assignment of SB bit (CREGH register). The conversion time (integration time TINT) is determined by the contents of register CREGL:T (T). For further details see also Figure 22.

Figure 7: *SYNS Mode* timing[11]



5.1.4 Synchronous Measurement Start and Stop Mode (*SYND Mode*)

The start and the stop of the measurement are completely controlled by the SYN signal. When the device is in the idle or *Standby* state the first coming falling edge starts the measurement. Each following falling edge of SYN, which occurs within the conversion, can stop or continue the measurement. The content of EDGES register determines which edge is the stopping one. This means that the measurement will not stop until a certain number of falling edges passed within the conversion time. This certain number of edges is represented by a value of register EDGES (see Figure 8 and Figure 9). For further details see also Figure 22.

Figure 8: *SYND Mode* timing, register EDGES = 1

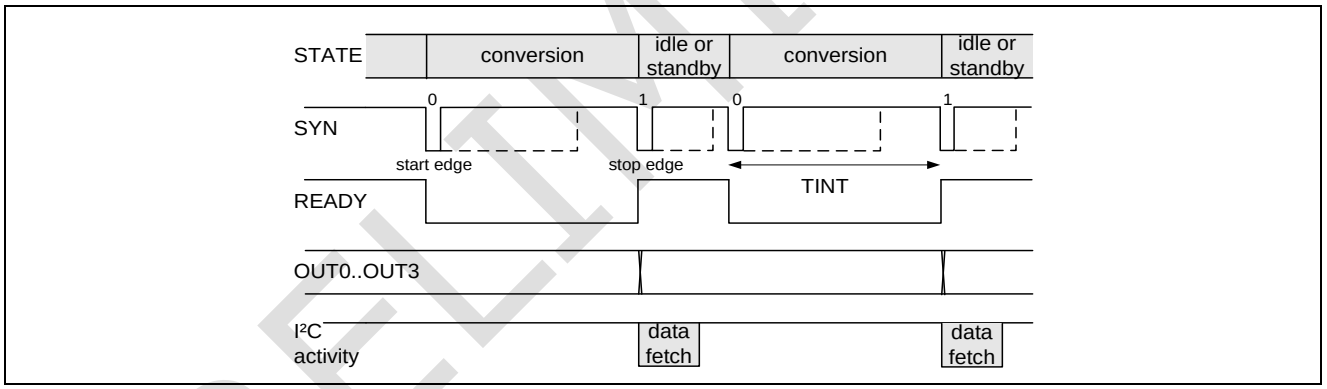
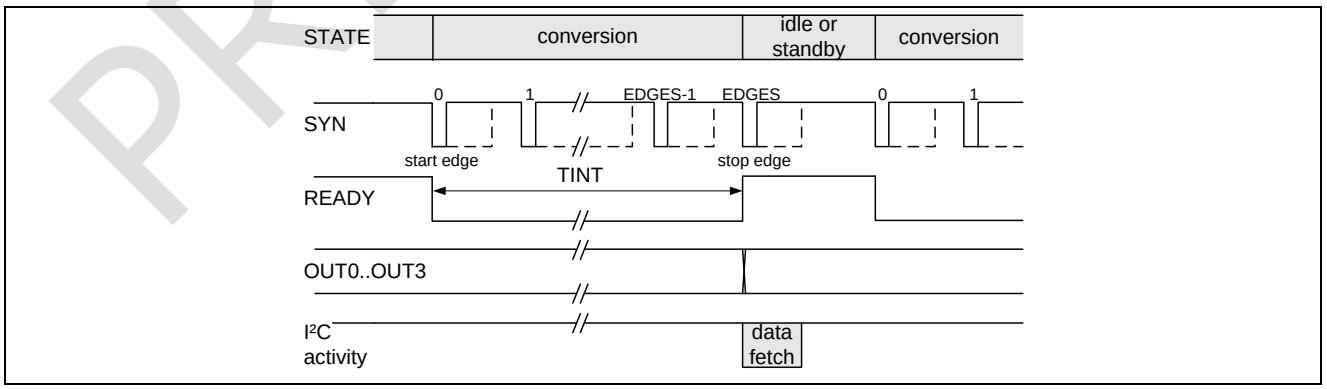


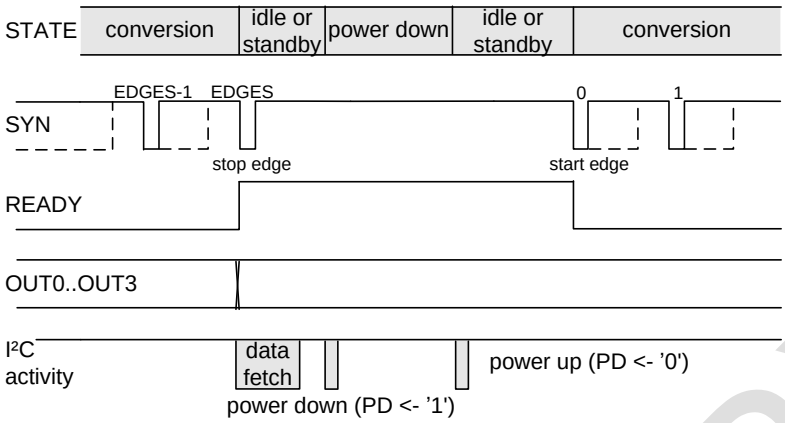
Figure 9: *SYND Mode* timing, register EDGES > 1



Data fetch should be performed between the rising edge of READY signal and the next falling edge of SYN in order to allow distortion free measurement.

[11] Dash lines indicate variable conditions

Figure 10: *SYND Mode* timing with *Power down*, EDGES > 1[12]



Between the subsequent conversions the device alters its state to *Standby* or idle according to assignment of SB bit (CREGH register). In this measurement mode it is also possible to switch the device into *Power down*. If the *Power down* is activated, the SYN signal would be ignored and no measurement will be performed.

The conversion time (integration time TINT) is determined by the duration between start and stop edge of the SYN signal. The distance between the falling edges determines the duration of the integration time TINT. It is possible to set the number of edges after which the integration time is terminated. In this way, the synchronization can be performed on different pulsed light sources. The minimum integration time TINT is 90µs, which corresponds to a resolution of at least 6Bit. The maximum integration time is 800ms.

In order to prevent measurement failures as a result of 'gain changing' (register CREGL:R), it is highly recommended to set the CMD mode or the Power down mode, before activating SYNS or SYND mode. In the case of using the Power down modus, a startup time of 500µs has to be respected to ensure that all parts of the AS89010 are fully functional again and the measurement does not start before awaking the AS89010 (CMD and CONT mode).

This waiting time can be prevented by inserting a "dummy" CMD mode before SYNS or SYND. Setting of Power down mode is not needed in this case.

5.2 Power Down

In *Power down* the clock generator and analog part of the device are turned off. The digital part stays idle, the full communication via the I²C interface is granted. Reading of measurement data and start of a measurement by setting the SS-Bit in *CMD Mode* is possible.

Power down is configured by the PD bit in OSR register (Table 8). By setting the OSR:PD bit to "1" the AS89010 immediately changes to *Power down*. By resetting the OSR:PD bit to "0" the AS89010 changes back to the measurement/idle or *Standby* depending on the settings of the CREGH register. This change to the operational state is delayed by the *Start up time* of about 500µs to ensure that all parts of the AS89010 are fully functional again. Only in the CMD measurement mode a single conversion can be started during *Power down* state by setting the OSR:SS bit to 1. In this case the *Start up time* of 500 µs between the I2C command and the start of the conversion becomes active too. After the conversion the AS89010 changes back into the *Power down* state.

5.3 Standby

In *Standby* only the A/D converters are powered down, thus the power consumption will be reduced. The *Standby* operation can be configured by the SB bit of CREGH register (Table 11).

[12] Dash lines indicate variable conditions

In the *CONT Mode* the *Standby* is automatically deactivated by starting the measurement with setting the OSR:SS bit to 1. If the OSR:SS bit is set to 0 the *Standby* becomes active again.

In the SYNS and SYND operation mode together with an activated *Standby* the start of the measurement automatically deactivates the *Standby* bit in the CREGH register. In the CMD operation mode the *Standby* cannot be activated.

5.4 A/D Conversion

In general the implemented A/D converter represents a delta-sigma converter, which performs and uses a charge balancing between the input I_{IN} and a reference current I_{REF} as result OUT of ADC. The input current integration takes place onto the integrator whose result is a pulse density modulated digital signal f_{CLK}, further filtered by up to 20 bit counter. At the end of integration the output OUT of this counter represents a digital equivalent of the average input current I_{IN} within the integration time interval TINT.

The transfer function of the A/D converter can be expressed as:

$$OUT = \frac{I_{IN}}{I_{IREF}} N_{CLK}\,, \tag{1}$$

or:

$$OUT = \frac{I_{IN}}{I_{IREF}} TINT \cdot f_{CLK}\,. \tag{2}$$

OUT : Digital output of conversion (corresponds to the content of output register)

I_{IN} : Average input current within a conversion time interval

I_{REF} : Reference current

$TINT$: Integration e.g. conversion time interval

N_{CLK} : Number of clock cycles within the conversion time interval

f_{CLK} : Clock frequency

In the *CONT, CMD* and *SYNS Mode* the integration time is internally generated[13]. Number of clock counts within this interval is a constant number, so that output remains independent of clock frequency. In this case an output can be represented by the equation (1).

In the *SYND Mode* integration time is externally generated, conversion result is represented by equation (2). If the conversion time measurement is activated (CREGH:ENTM = ”1b”, see chapter 5.5), the number of clock counts within the integration time can be also internally measured, so that conversion results may be calculated as:

$$OUT = \frac{I_{IN}}{I_{IREF}} OUTINT\,. \tag{3}$$

OUTINT: Integration time duration expressed as the number of clock counts within this time. In this way the input current can be measured independently of internal frequency and furthermore external integration time variations in *SYND Mode*. The reference current and internal integration time are determined by the

[13] The system clock is internally generated using an RC oscillator. It may have a little technological-inflicted tolerance, e.g. the exemplary period of time may vary slightly. This must be considered when calculating the time to be programmed (e.g. BREAK or integration time).

content of register CREGL: R and T bits (T). Their values determine directly the sensitivity e.g. LSB and full-scale range (FSR) current of A/D conversion. One overview of the possible configurations is shown in Table 5.

Table 5: Programmable FSR and LSB current (CONT, CMD, SYNS Mode)

T [b]	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010
N_{CLK}	1024	2048	4096	8129	16384	32768	65536	131072	262144	524288	1048576
Resolution [bit]	10	11	12	13	14	15	16	17	18	19	20
R [b]	**IFSR [nA]**										
000	20							10	5	2.5	1.25
001	80							40	20	10	5
010	320							160	80	40	20
011	1280							640	320	160	80
1XX	5120							2560	1280	640	320
R [b]	**LSB [pA]**										
000	19.53	9.77	4.88	2.44	1.22	0.61	0.31	0.15	0.08	0.04	0.02
001	78.13	39.06	19.53	9.77	4.88	2.44	1.22	0.61	0.31	0.15	0.08
010	312.5	156.25	78.12	39.06	19.53	9.77	4.88	2.44	1.22	0.61	0.31
011	1250	625	312.5	156.25	78.13	39.06	19.53	9.77	4.88	2.44	1.22
1XX	5000	2500	1250	625	312.5	156.25	78.13	39.06	19.53	9.77	4.88

T: bit 3 to 0 of CREGL
R: bit 6 to 4 of CREGL
IFSR: full-scale range current
LSB: last significant bit
Resolution: internal A/D resolution
$N_{CLK} = TINT \cdot f_{CLK}$

The maximum value of conversion result in the *SYND Mode* depends on the external integration time duration. This maximum achievable count is equal to *OUTINT* and differs from the full-scale count achievable in CMD, CONT and *SYNS Mode.* The value of T defines the number of clock counts during the integration time. It defines the integration e.g. conversion time duration and maximum of resolution of the A/D conversion. This is valid for the CONT, CMD and *SYNS Mode*.

In the *SYND Mode* the value of T has no meaning, integration time duration is externally defined. The values of T higher than 0110b internally lead to A/D conversion with a higher resolution up to 20 bit. But only the 16 most significant bits will be further processed and stored. As only the lower part of results is evaluated, the FSR is lower for internal resolution higher than 16 bit. The value of R defines the A/D converter reference current (see T). In combination with the values of T or the integration time duration it also defines the full-scale range current and thus the sensitivity of the A/D conversion.

During a conversion an overflow of input integrator of the A/D converter must be avoided. The maximum input current must not exceed the double value of reference current for the maximum of one clock duration, otherwise integrator overflow can occur and conversion result would be incorrect:

$$I_{IN}^{MAX} < 2 \cdot I_{IREF} \quad (4)$$

I_{IN}^{MAX} : Peak Input Current

For more details and necessary steps to find the optimal parameters for amplifying please see our notices in the application note "AppNote specifying the optimal gain parameters for AS89010.pdf"[14].

[14] Please contact our sales team - see page 40

5.4.1 Offset of the A/D Converter

Ideally no or a very small amount of offset would be presented in the conversion output. However, an offset presented in input signal cannot be overcome. If an input leakage current occurs (at printed circuit board for example), it is possible that input current takes negative sign and makes conversion unable to operate for very low level currents. In such a case a well-known amount of an internal offset can be introduced in order to add the positive offset to the A/D transfer characteristic. Therefore, even low level negative currents can be measured precisely. This option should be set by configuring the ZERO values in OPT register (Table 12).

For this case the output of the A/D conversion can be expressed as:

$$OUT = \frac{I_{IN}}{I_{IREF}} N_{CLK} + OUT_{ZERO} \quad (5)$$

or for *SYND Mode*:

$$OUT = \frac{I_{IN}}{I_{IREF}} TINT \cdot f_{CLK} + \frac{TINT \cdot f_{CLK}}{2^{ZEROSYND}} = \frac{I_{IN}}{I_{IREF}} OUTINT + \frac{OUTINT}{2^{ZEROSYND}} \quad (6)$$

OUT_{ZERO} : Offset in CONT, CMD and *SYNS Mode*: 0, 15, 31 or 63 depends on the ZERO values of OPTREG

$ZEROSYND$: Offset factor in *SYND Mode*: TINT·f_{CLK} /2^7, TINT·f_{CLK} /2^{11} or TINT·f_{CLK} /2^{15} depending on the ZERO values of OPTREG

The offset generation is activated only for ZERO≠00b. Please note, the internally generated offset has to be subtracted from the result value by the user specific control program. It will not be performed internally or automatically.

5.4.2 Divider

For the purpose to further expand the measurement ranges an internal implemented digital divider can be used to scale the result. This may be necessary if the resolution of the conversion is set to a value of >16 bit. If the digital divider is used the conversion result is downscaled according to:

$$OUT_{DIV} = \frac{OUT}{DIV} \cdot \quad (7)$$

OUT_{DIV} : Digital output

DIV : Divider factor (2, 4, 8, 16), see Table 11

Therefore the divider acts as digital downscaling feature of the converter gain. It increases the effective dynamic range of device without changing its sensitivity or integration time.

5.5 Conversion Time Measurement

In case of SYND measurement mode the conversion time is fully controlled by the external signal at pin SYN. The relative deviation of this time to the internal clock frequency[15] can produce some deviations in the conversion output. However, this time can be internally measured in time units of system clock (typically 1024 MHz) up to 20 bit word. It gives the opportunity to calculate more precisely measured input currents. That could increase the accuracy for the converter.

Even further, the measured result can be compensated for any deviation which can occur in the clock frequency due to temperature or supply voltage variations.

The time measurement can be enabled by setting the ENTM bit of register CREGH (Table 11). The result is stored into the output register OUTINT (Table 15) after a conversion has been made, synchronous with the storing of the A/D conversion data. The stored value follows the relation:

$$OUTINT = TINT \cdot f_{CLK} \quad (8)$$

The register OUTINT is only valid if this mode has been activated.

5.6 I²C Communication

The two wire serial interface is compatible to the fast mode I²C protocol and timing[16]. The SDA wire carries the data while the SCL wire synchronizes the transmitter and receiver. The device that initiates a data transfer is called a master and the responding device is called a slave. A device that sends data to the bus is called transmitter and a device receiving the data is called receiver.

The AS89010 can operate only as slave with unique slave address 11101'*A1 A0'* (7 address bit's plus read/write bit, see Figure 11), with the two lower bits defined by the input pins *A1, A0*. Each data transfer begins with a start (S) condition, defined by a high to low transition of SDA while SCL is high. The transfer terminates by a stop (P) condition, defined by a low to high transition of SDA while SCL is high. A repeated start condition (Sr) can be generated instead of a stop condition, if the transfer should be continued with the new data packet.

The start and repeated start condition are functionally equivalent. The data transfer consists of 8 bit long data. Each byte has to be followed by an acknowledge bit (A) (see Figure 11). The bits arrive with the MSB first. The acknowledge signal shall be pulled low by the receiver during the high period of the 9th clock pulse, while transmitter releases the SDA line. When SDA stays high during this clock pulse then this is defined as the not acknowledge signal (NA). After the not acknowledge signal, the master can either generate a stop or repeated start condition, depends on whether the master wants to abort or start a new transfer. The AS89010 generates a not acknowledge only in case when received data are not understood. The data transfer is implemented as shown in Figure 11.

A master generates the start condition and sends a 7 bit long slave address followed by the 8th bit which is a data direction bit (h). With the data direction bit set to '1' a master indicates a request for data read with a '0' a transmission is indicated. A data transfer terminates by a stop condition, but the master can also generate a repeated start condition instead of stop condition if the communication should be continued.

The sequences for a read and write data transfer are shown in Figure 12.

[15] It depends on technology parameters in manufacturing. So variations and tolerances from one IC to another can occur.

[16] The requirements for bus termination using standard Pull-Up's according I²C should be considered. It concerns especially noise environments and EMC in PCB design.

Figure 11: I²C bus data transfer

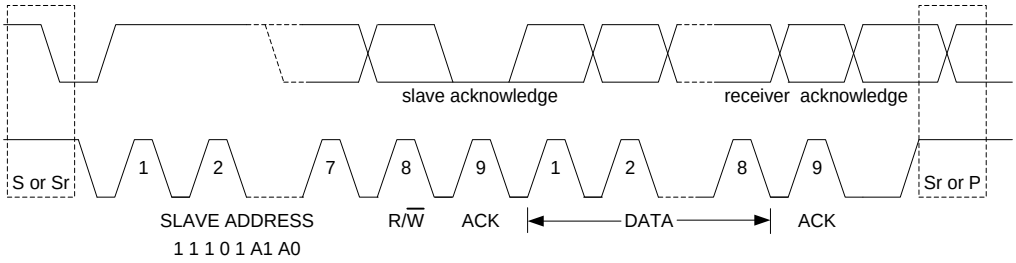
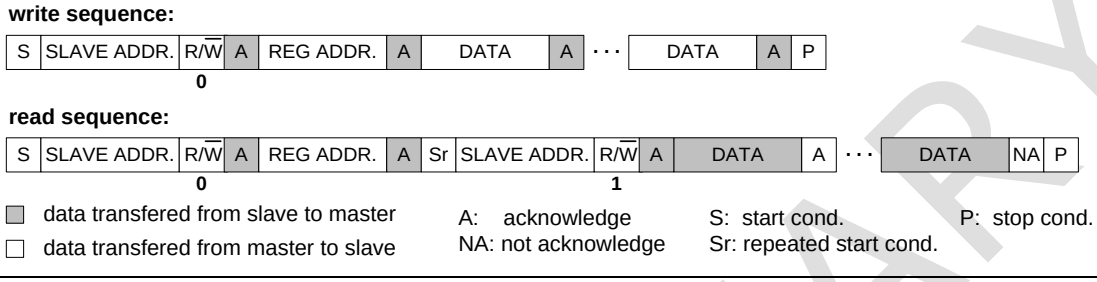


Figure 12: Write and read data sequences



5.6.1 Write Protocol

The start byte consists of the slave address, followed by R/$\overline{W}$ set to set to '0' for the write direction. The first byte after the start byte is always the address pointer to the internal register which the master wants to write. The device acknowledges this byte (REG ADDR. in Figure 12). If the master generates a stop condition the transfer is aborted and a new write sequence must be started from the beginning. If master sends the next byte, this one will be stored in the internal register, addressed by the address pointer (REG ADDR.). The device sends acknowledge and internally increments the address pointer by 1. Then each next data byte transferred from the master will be stored sequentially in the internal register.

5.6.2 Read Protocol

The slave address is followed by R/$\overline{W}$ set to '0' for the write direction. The first transferred byte after the start byte is always the address pointer to the internal register the master wants to read. The device acknowledges this byte (REG ADDR. see Figure 12). The master sends a repeated start condition and repeats the slave address but with the R/$\overline{W}$ bit reversed. The slave acknowledges this byte and starts the data transfer to the master. The first transferred byte is the content of the internal register which is pointed by address pointer. Each transferred byte is acknowledged by the master. If not acknowledge occurs the master sends as next the stop condition and the transfer is finished. Internal address pointer increments carries out that the subsequent transferred data are sequentially read out from internal register.

5.6.3 I²C Addressable Register Space

Table 6 shows the overview of the internal register which can be accessed via I²C interface. The control register bank can be accessed in the configuration state and these registers are all 8 bit long.

The output registers can only be accessed for read in the measurement state. They are 16 bit long, except OUTINT which is 24 bit long. The device transfers the output data registers with the lowest byte first. The output registers data transfer can start at any address. If the transfer starts not at address (hex) 00h and during the sequential data read the highest possible address is arrived (ENTM=1: Address 04 with 3 byte; ENTM=0: Address 03 with 2 byte), the internal pointer resets back to the address 00h so that next data byte transferred corresponds to the low byte of OUT0. In this manner transfer continues with the first register (OUT0). However, the maximum of number of output data transferred must not exceed a total number of bytes accessible at all (8 bytes if integration time measurement is not activated otherwise 11 bytes). The OUTINT is only valid if CREGH:ENTM bit has been set.

Table 6: Register access overview

ADDRESS [hex]	ACCESS IN CONFIGURATION STATE		ACCESS IN MEASUREMENT STATE	
	Write	Read	Write	Read
00	OSR	–	OSR	OUT0
01	–		–	OUT1
02	–	AGEN	–	OUT2
03	–		–	OUT3
04	–		–	OUTINT
05	–		–	–
06	CREGL		–	–
07	CREGH		–	–
08	OPTREG		–	–
09	BREAK		–	–
0A	EDGES		–	–

5.6.4 Examples of using I²C-interface

An example of usual I²C communication set of sequences is shown in Figure 13. After a Power-up, the device is in a default configuration state. User can now set up the device for the application by writing control register. Success of the configuration can be proven by reading the control register.

Before a measurement can be started, the device must change its state into the measurement mode. In the last three bits of OSR '011b' should be loaded. Now a conversion can be started, it will start accordingly to the measurement mode selected by CREGH:MODE. When a conversion ends, rising edge of READY signalizes this (not in *SYND Mode*), the conversion data can be read.

If a new configuration should be implemented, the device has to change its state back to configuration mode, by loading '010b' into the last three bits of OSR. At this action all control registers will reset to their default values. New configuration can be made now.

Figure 13: An example of configuration and measurement I²C sequences

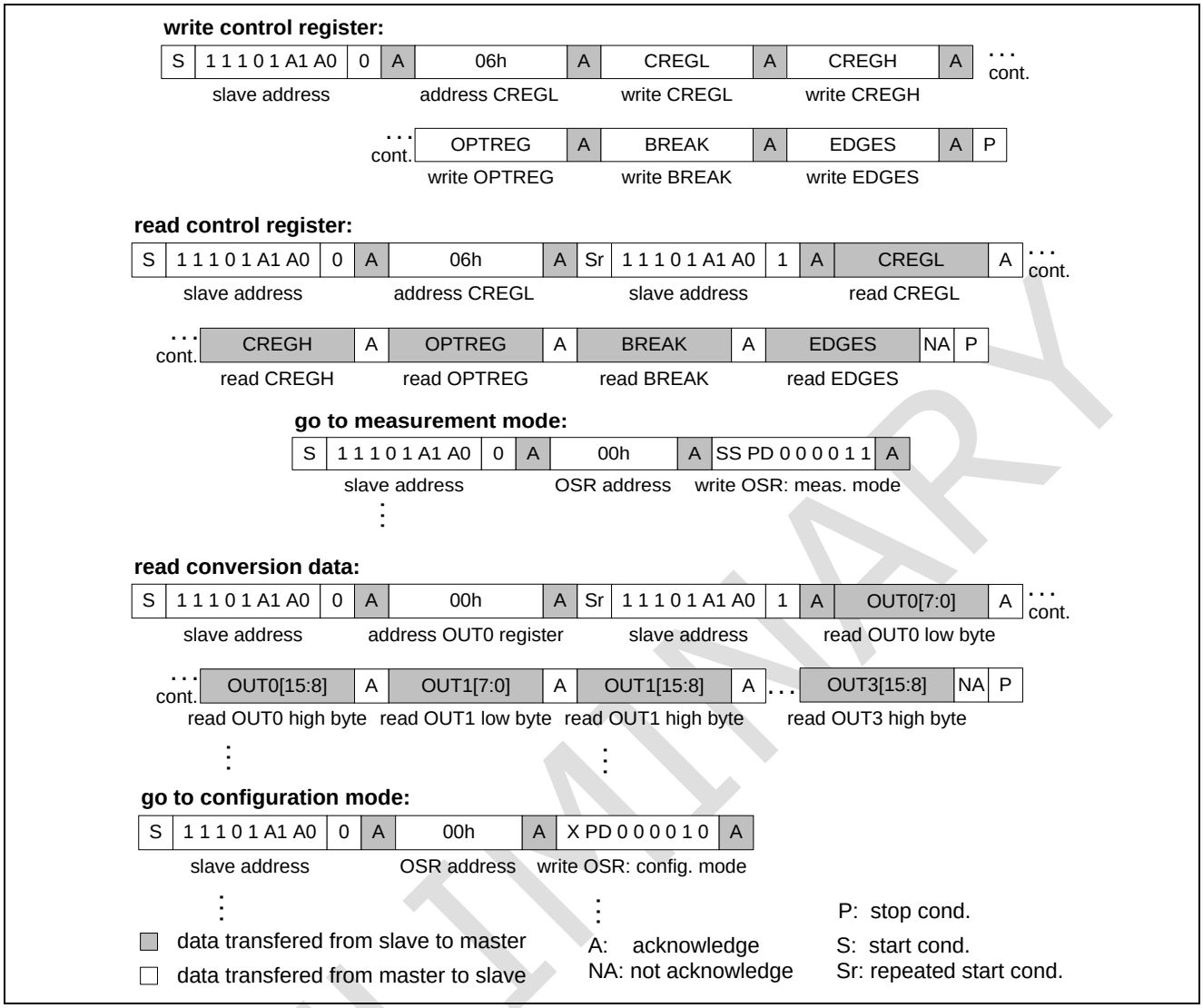
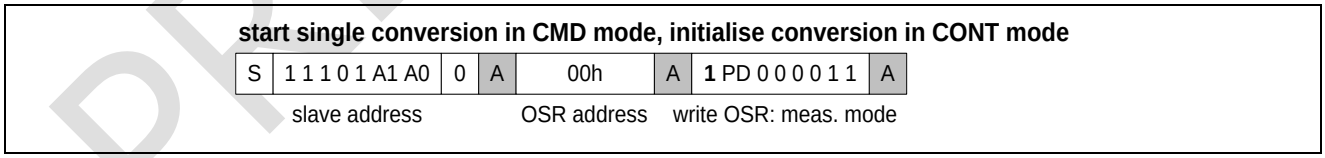


Figure 14 shows I²C sequence for starting a conversion in CMD or *CONT Mode* by setting the SS bit to '1'. The two last bits of the OSR register could also be set to '00' if the device is already in the measurement mode.

Figure 14: Start conversion in CMD or *CONT Mode*



6 DESCRIPTION OF REGISTERS

6.1 Control Register Bank

AS89010 configuration and operational state are controlled by the registers content defined in Table 7. The value size of all registers is 8 bit. Writing and reading of all registers is implemented in byte.

Table 7: Register addressing space

ADDRESS [hex]	ACCESS[17]	NAME	DEFAULT [hex]	DESCRIPTION
00	wo	OSR	42[18]	operational state register
01	-	-	-	reserved
02	ro	AGEN	20	API generation
03	-	-	-	reserved
04	-	-	-	reserved
05	-	-	-	reserved
06	rw	CREGL	B6	configuration register
07	rw	CREGH	08	configuration register
08	rw	OPTREG	00	options register
09	rw	BREAK	20	break register
0A	rw	EDGES	01	edges register

6.2 Operational State Register – OSR

This write only register OSR[19] controls the device operational state (DOS) of the AS89010 according to Table 8. This register can be written at any time, independently of the actual operational state. Please note, reading this register only results in 00 [hex] because the access is write only.

Table 8: OSR register - Address 00h

OPERATIONAL STATE REGISTER OSR	NAME	VALUE [b]	AFFECTED OPERATIONAL STATE
		0[20]	stop measurement
		1	start measurement
		0	no *Power down* mode
		1[21]	activate *Power down* mode
bit 5 to 3	-	-	reserved
		000	reserved
		001	reserved

[17] ro – Read-only, wo – Write-only, rw – Read-write

[18] Reading register with access Write-only results in 00 [hex]

[19] The OSR register of the AS89010 is Write-only. It's not possible to readout the content of this register, sadly. Any readout this register will always result the value 0.

[20] Default after power-on-reset and state change from measurement to configuration.

[21] Default after power-on-reset.

OPERATIONAL STATE REGISTER OSR	NAME	VALUE [b]	AFFECTED OPERATIONAL STATE
	Operational State	010[20]	operational state: **configuration**
		011	operational state: **measurement**
		1XX	reserved

DOS switches the operational state of the device between configuration and measurement. The configuration state enables the access to the register bank (Table 7). No measurement takes place.

The measurements can only be performed in the measurement state and any access to the control register bank (except OSR) is not permitted. The control register would be reset to their default values each time the operational state is switched back to the configuration state.

The start of the measurement is controlled by the value of the **SS** bit. These signals are evaluated only in the measurement state and only in the CONT and *CMD Mode* (refer to chapter 5.1).

The *Power down* mode is controlled by the **PD** value. The *Power down* takes effect in both operational states. If the PD is active in the measurement state, the *Power down* would be performed only during the breaks between two consequent conversions.

6.2.1 API Generation Register – AGEN

The value of this read only register indicates the generation of the Control Register Bank. The value of the register changes whenever any formal modification is introduced to the Control Register Bank. This case indicates that the Application Programming Interface (API) has been changed.

Table 9: AGEN register - Address 02h

AGEN	NAME	VALUE [b]	DESCRIPTION
bit 7 to 4	DEVID	0010	Device ID number; the value 0010b is reserved for MCDC devices
bit 3 to 0	MUT	0000	Mutation number of Control Register Bank

6.2.2 Configuration Register – CREGL and CREGH

The configuration register CREGL mainly serves to define full-scale-range, sensitivity and conversion time of the device.

Table 10: CREGL register - Address 06h

CREGL	NAME	VALUE [b]	AFFECTED CONFIGURATION	
		0	input current direction out of the IN0-IN4 pins (the cathodes of the photodiode connected to the input pins)	
		1[22]	input current direction into the IN0-IN4 pin (the anodes of the photodiodes connected to the input pins)	
			ADC Reference Current IREF	ADC LSB Current (TINT=1024 ms)
		000	20 nA	20 fA
		001	80 nA	80 fA
		010	320 nA	320 fA

[22] Default after power-on-reset and state change from measurement to configuration.

CREGL	NAME	VALUE [b]	AFFECTED CONFIGURATION	
		011[22]	1.28 µA	1.28 pA
		1XX	5.12 µA	5.12 pA
			Integration Time (internal f_{CLK}=1.024 MHz)	
			TINT (ms)	number of clock counts
		0000	1	1024
		0001	2	2048
		0010	4	4096
		0011	8	8192
		0100	16	16384
		0101	32	32768
		0110[22]	64	65536
		0111	128	131072
		1000	256	262144
		1001	512	524288
		1010	1024	1048576
		1011 to 1111	1	1024

TINT = integration time = measurement time = conversion time

It has to be set by the proper assignment of the DIR bit in which direction the input current flows. The bit R define device sensitivity, it internally sets the reference current of the A/D converters (see chapter 5.4 and Table 5 for more information).

The content of **T** controls the integration time duration and is a multiple of the internal clock periods. If start and stop of measurement are externally controlled by *SYND* signal (*SYND* Mode), T is ignored.

The register CREGH generally defines the measurement modes of the device.

Table 11: CREGH register - Address 07h

CREGH	NAME	VALUE [b]	AFFECTED CONFIGURATION
		0[23]	access to time counts for internal integration times (register OUTINT) is disabled
		1	access to time counts for internal integration times (register OUTINT) is enabled
		0[23]	*Standby* disable
		1	*Standby* enable
bit 5	VR	0[23]	reserved (must be set to '0')
		00	continuous measurement mode (CONT)
		01[23]	command measurement mode (CMD)
		10	synchronous measurement start (SYNS)

[23] Default after power-on-reset and state change from measurement to configuration.

CREGH	NAME	VALUE [b]	AFFECTED CONFIGURATION
		11	synchronous measurement start and stop (SYND)
		00[23]	divide by 2
		01	divide by 4
		10	divide by 8
		11	divide by 16
		0[23]	disable digital divider
		1	enable digital divider

The measurement mode is controlled by the value of **MODE**. This assignment gives the opportunity to accommodate the current measurement to the given application (see chapter 5.1 for more details).The internally implemented divider which acts as digital downscaling of the converter gain can be set by the bits **ENDIV** and **DIV**. The bit **SB** controls the *Standby* operation of the device. In *SYND Mode* the bit **ENTM** enables the access to OUTINT to get time counts for internal measurement of the integration time, which can be of special interest if this time has been externally controlled. The time is measured as the number of internal clock counts with a width of up to 20 bit. The result is stored in register OUTINT that can be accessed via I²C interface (refer to chapter 5.5 for more details).

6.2.3 Options Register - OPTREG

This register sets additional options of the device which can enhance performance according to the given application.

Table 12: OPTREG register - Address 08h

OPTREG	NAME	VALUE [b]	AFFECTED CONFIGURATION
bit 7 to 2	--	000000[24]	must be used
			Offset Value (conversion output for zero input current)
		00[24]	0dec (disable offset generation)
		01	15dec (in *SYND Mode*: TINT·f_{CLK} /2^7)
		10	31dec (in *SYND Mode*: TINT·f_{CLK} /2^{11})
		11	63dec (in *SYND Mode*: TINT·f_{CLK} /2^{15})

The **ZERO** enables an internal offset generation to the input current and conversion result, too. It makes the device able to measure very low e.g. zero input current even in presence of the negative leakage current, which would normally lead to an underflow.

6.2.4 Register – BREAK

Table 13: BREAK register - Address 09h

BREAK	NAME	VALUE [dec]	AFFECTED CONFIGURATION
bit 7 to 0	BREAK	1 - 255	break between measurements (only in CONT measurement mode) CONT: BREAK / f_{CLK} typically; 5 µs to 1021 µs in steps (1 µs + 4 µs * break time) CMD: BREAK / f_{CLK} typically; 1 µs to 255 µs in 1 µs steps

This register takes effect only in CONT and CMD measurement mode. In the *CONT Mode* it defines the break between two consequent measurements[25]. In the *CMD Mode* it defines the delay between a command for measurement start and the actually start of the measurement. This register gives a chance to the device to perform the measurement in the time when no disturbances occur during the I²C communication. Value of '0' cannot be written and will be ignored. The default value is 20h.

[24] Default after power-on-reset and state change from measurement to configuration.

[25] In case of an active I²C communication the AS89010 should not be active in converting. Therefore the break time between two measurements should be a minimum of >300 µs. (25 µs / Byte * (2 x 4 signal bytes+ 2 x control byte) * 1.25 clock tolerance).

6.2.5 Register – EDGES

This register takes effect only in SYND measurement mode. It defines a number of falling edges at SYN input at the end of the integration. Value of '0' cannot be written and will be ignored. The default value is 01h.

Table 14: EDGES - Address 0Ah

EDGES	NAME	VALUE [dec]	AFFECTED CONFIGURATION
bit 7 to 0	EDGES	1 - 255	number of SYN falling edges

6.3 Output Register Bank

The results of the conversion are stored into four 16 bit registers, addressing is shown in the Table 15. Register OUT0 to OUT3 store the conversion results and can be read at any time. During the SYND measurement mode the externally controlled conversion time can be internally measured in time units of the system clock (see chapter 5.5). This time measurement is enabled by setting the ENTM bit of CREGH register (Table 11). If enabled, the result is stored into the output register OUTINT (Table 15). In the 24 bit register OUTINT only the first 20 bits LSB are valid. This detected time value for the integration time depends on the internal clock frequency. Because clock frequency can differ from one AS89010 to another the value of OUTINT can be used to normalize the conversion results delivered in output registers OUT0 to OUT3 (see chapter 5.4). Additionally, the value of OUTINT can be used to estimate the current level of magnitude. At the end of each conversion e.g. measurement, the value of all available register will be refreshed. If a measurement finishes during the readout cycle of the output register, then the refresh of these new values is delayed until the read cycle is completed.

Table 15: Output register addressing space

ADDRESS [hex]	ACCESS[26]	NAME	NO. OF BITS	DESCRIPTION
00	ro	OUT0	16	output register, conversion result for current at IN0
01	ro	OUT1	16	output register, conversion result for current at IN1
02	ro	OUT2	16	output register, conversion result for current at IN2
03	ro	OUT3	16	output register, conversion result for current at IN3
04	ro	OUTINT[27]	24	result of integration time measurement (only 20 bits are valid)

The register OUTINT is only needed in the SYND mode. It measures the time of the measurement in units of the internal clock. For all other modes this time is internally defined by the programmed value CREGL:T. So use equation (1) with the value N_CLK from Table 5 or Table 10.

For the SYND mode use equation (3) with the OUTINT value from the result register 4 to calculate the input current. Only with CREGL:ENTM=1 gives valid results. This means CREGH:ENTM=0 will produce wrong data here. Other modes than SYND also gives wrong values. Unfortunately there are some values there in this cases. For the Reading of the results I suggest to address the first result register (OUT0 @ internal address 0) and then to read 8 bytes with the auto increment of the internal address.

[26] ro – Read-only

[27] This register is only valid if the integration time measurement has been chosen (ENTM=1b), but in *SYND Mode* only.

For SYND mode please also address first result register (address 0) and then read 11 bytes. Take care, the internal counter is only 20 bit. Another way to get the Value of OUTINT is to read this with an address for each result. Because all output registers are 16 bit, the MSB part of OUTINT is located at address 5. Then this codes examples will work:

```
ulOutint=((ULONG)(usaMeasure[5]&0x00ff))<<16;
ulOutint=(ULONG)usaMeasure[4];
```

6.4 I²C Interface

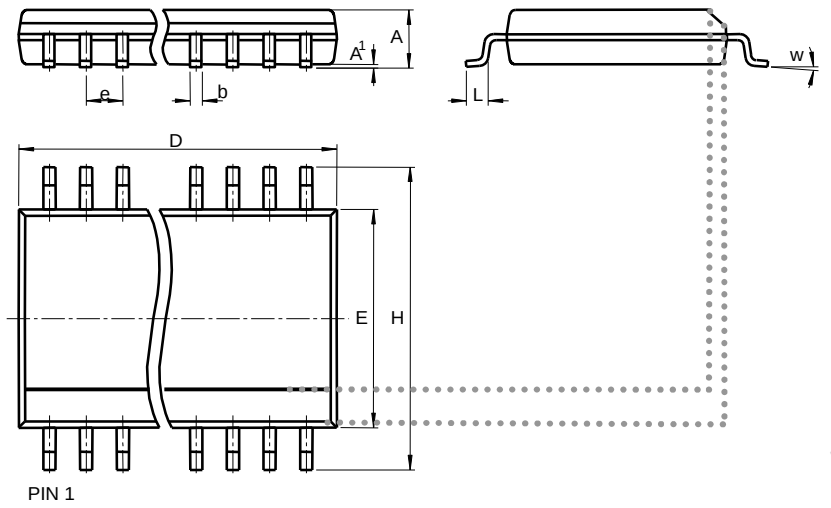
The two wire serial interface is compatible to the fast mode I²C protocol[28] and timing. The AS89010 can only operate as slave with slave address 11101A1A0, with the two lower bits defined by the input pins A1, A0. For more details refer to chapter 5.6. The I²C interface timing diagram is shown in Figure 1, timing specification in Table 2.

[28] In cases of strong interferences (long I²C cables, EMC or others) errors in I²C communication could be possible. In these cases we suggest to use PCB EMC-protection e.g. an external I²C repeater.

7 PACKAGE

7.1 Shape and Dimensions

Figure 15: Shape for package



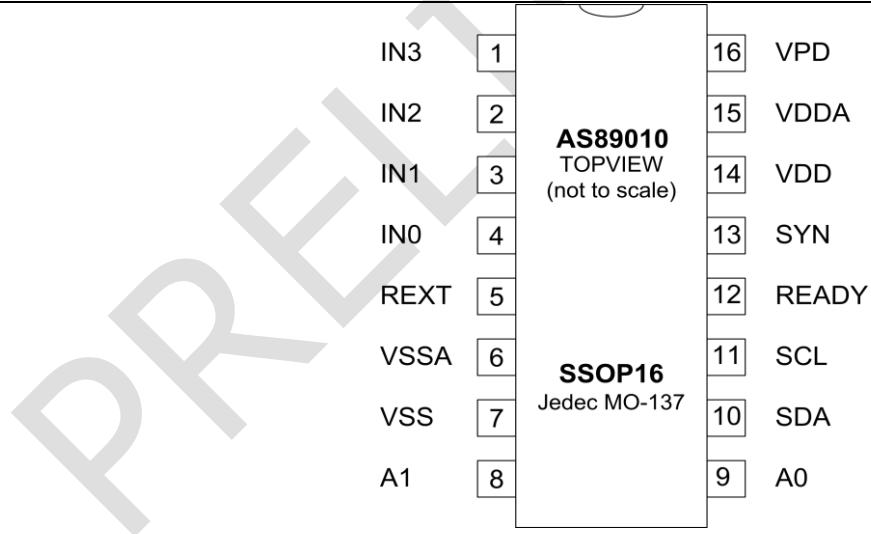
1) As shown in the figure PIN 1 is located on the bottom of the left corner of the outline.

Table 16: Dimensions for package (dimensions – mm)

TYP	PACKAGE	D	E	H	A	A1	e	b	L	w
AS89010	SSOP16 JEDEC MO-137	4.80 - 5.00	3.81 - 3.98	5.79 - 6.20	1.35 - 1.75	0.10 - 0.25	0.635	0.20 - 0.30	0.40 - 1.27	0 - 8

7.2 Pin Configuration

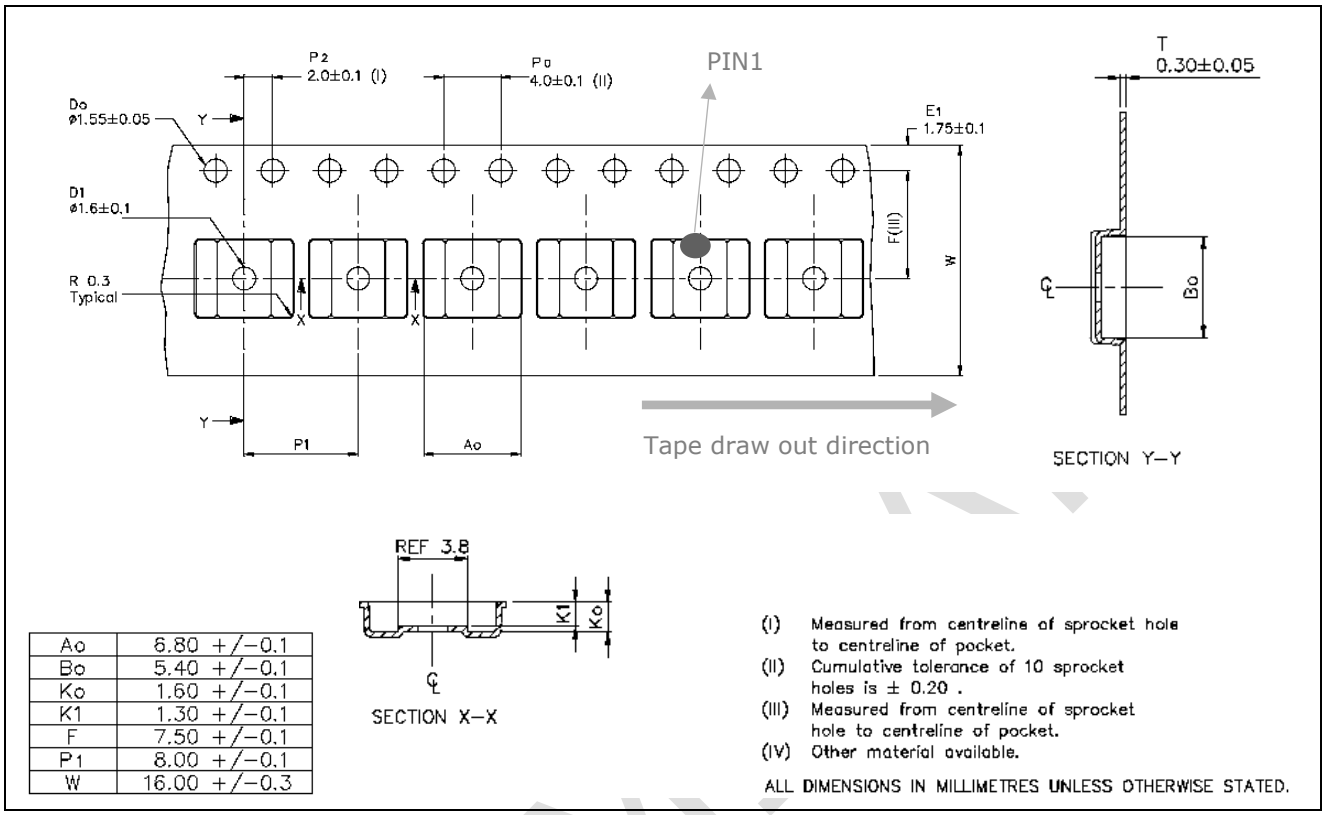
Figure 16: Pin configuration



7.3 Packing Information

Standard packing is tape and reel. Otherwise it has to be discussed with our sales team.

Figure 17: Details for tape & reel



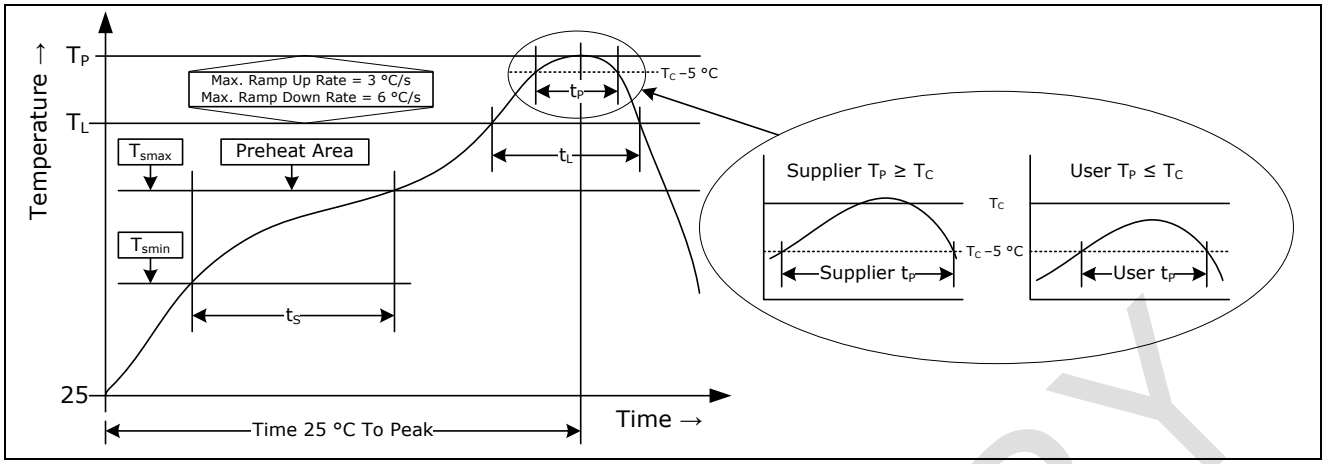
Ao	6.80 +/−0.1
Bo	5.40 +/−0.1
Ko	1.60 +/−0.1
K1	1.30 +/−0.1
F	7.50 +/−0.1
P1	8.00 +/−0.1
W	16.00 +/−0.3

7.4 Soldering Information

Table 17: Profile features according JEDEC

	IPC/JEDEC J-STD-020D.1 (Pb-Free)	RECOMMENDED DATA
Time [s] from 150°C to 200°C (preheat)	60 - 120	100
Average ramp-up rate [°C/s] (200°C to peak temperature)	max. 3.0	0,5 - 1,0
Liquid's temperature [°C] Time [s] above liquid's (217°C)	217 60 - 150	217 110
T_P Peak package body temperature [°C]	max. 260	≤ 260
Time [s] within 5°C of the classification temperature T_C	min. 30	35 - 45
Average ramp-down rate [°C/s] (Peak temperature to 200°C)	max. 6.0	3.0
Time [s] from 25°C to peak temperature	max. 480	350

Figure 18: recommend soldering profile



Do not to exceed the recommended values. For further information see JEDEC J-STD-020D.1.

8 APPLICATION NOTES

Figure 19 shows typical connection of external devices to the AS89010. If digital and analog grounds are separately routed onto the printed circuit build, they should be together, connected near the device.

Figure 19: Typical connection circuitry; (a) common cathode photodiode array (CREGL:DIR='1b'), (b) common anode photodiode array (CREGL:DIR='0b')

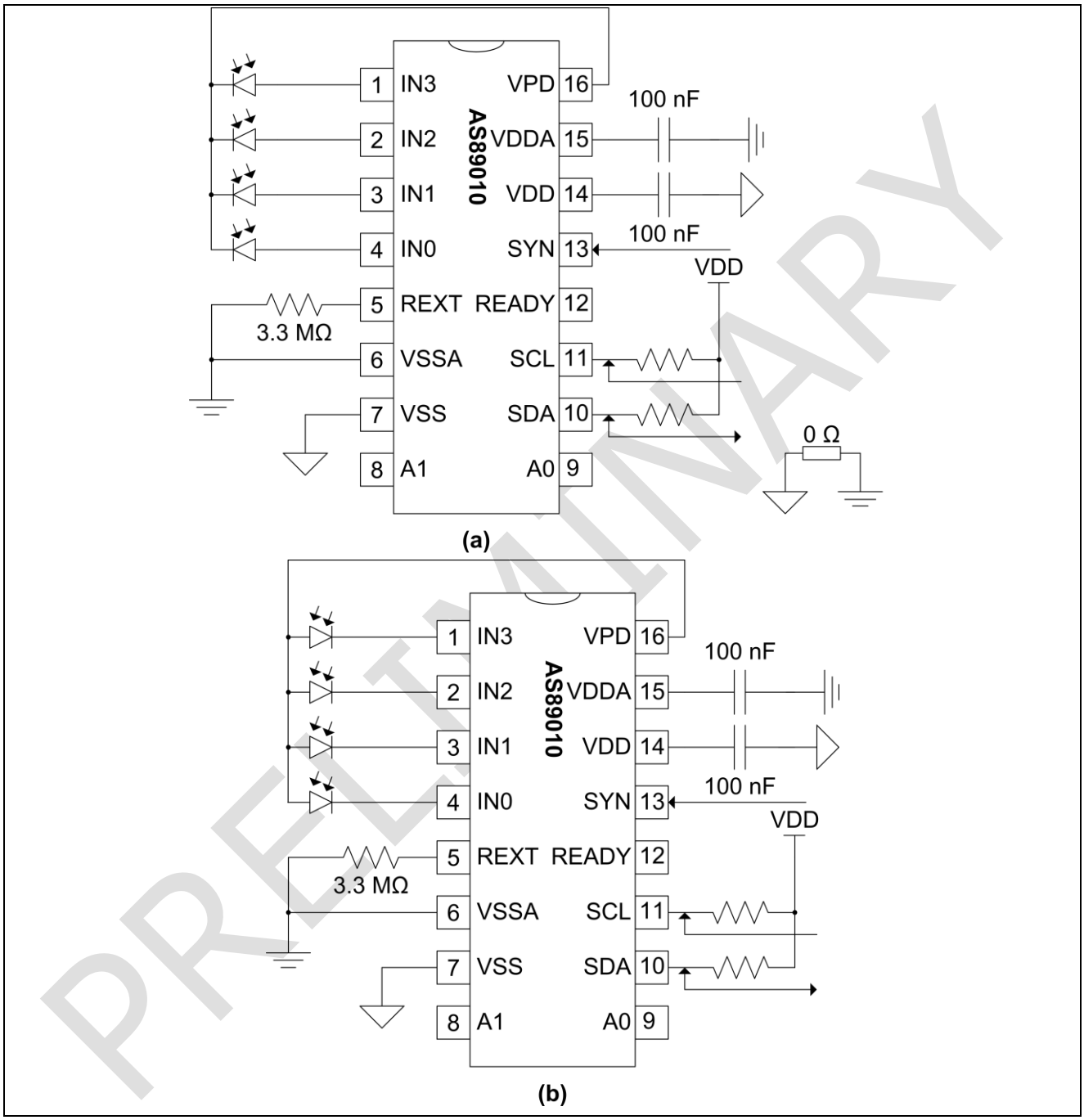
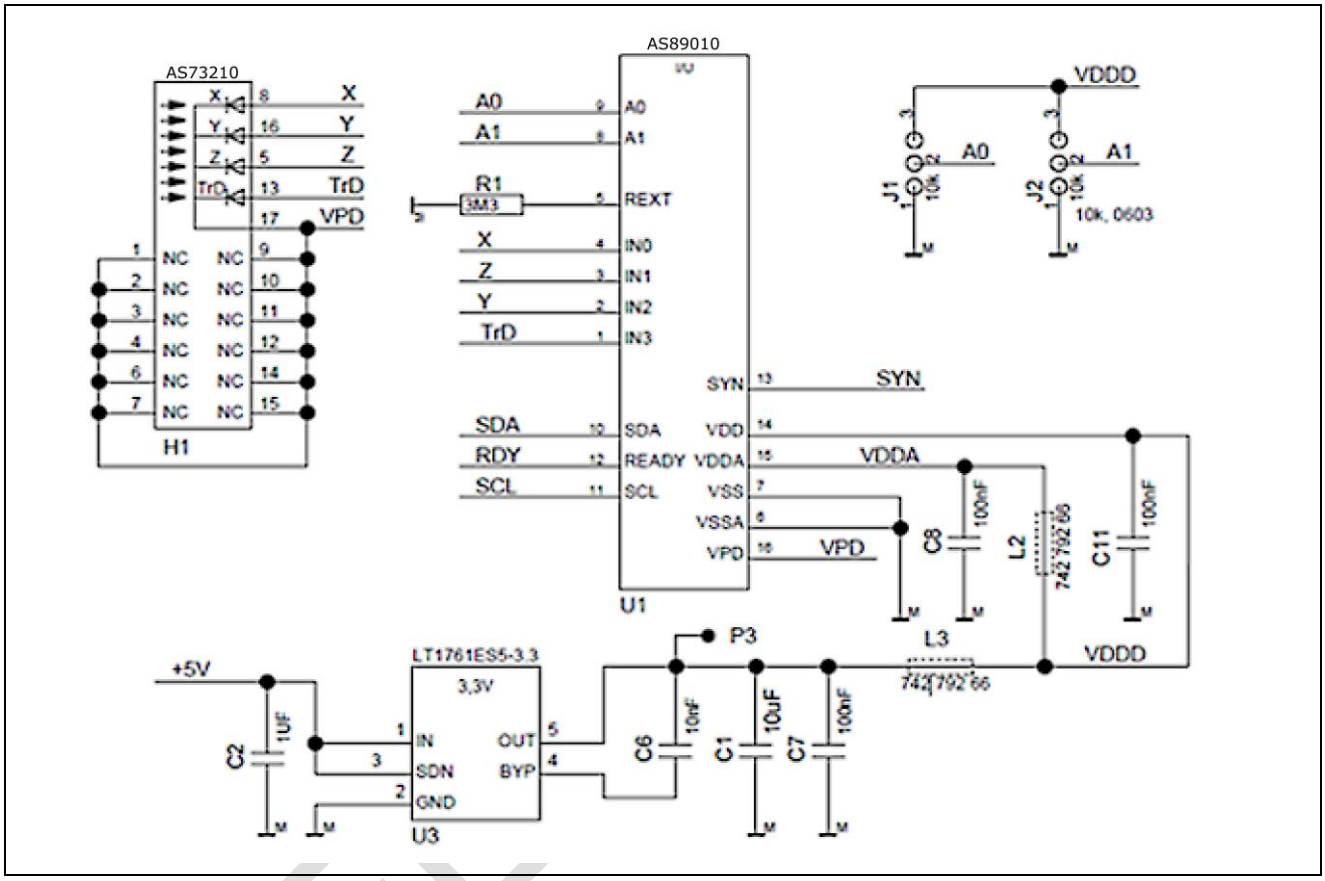


Figure 20 shows the schematic of an application specific board with a 4 channel sensor (e.g. Color Sensor MTCSiCF of ams Sensors Germany but all statements are also valid for other similar sensors with current output), AS89010 and environment of electronics e.g. power supply. Please make sure that all specified components are operated in the application circuit according to their working range. For example, color sensor (input current) and voltage regulators (workspace load current, separated analog and digital OR decoupled power supplies base on a common regulator) are selected and to be operated according to the parameters in the data sheet. Otherwise problems, noise or deviations can occur during operation.

Figure 20: Schematic of reference design



Note, X Y Z pins are the True Color Sensor signals, cathode is the common connector and TrD is an added-isolation diode to split up the potential of the 3 functional PIN diodes XYZ. It has to be connected to the same potential as the functional diodes - at IN3 of AS89010.

It is important to shield the single pin diodes for XYZ detection to minimize cross-talk among the 3 filtered areas/diodes.

The next figures show principle steps of programming the command and continuous measurement mode for SYNS and *SYND Mode*. Please note in configuration state the modifications for RAM must be adapted specific to your application by parameters described in this data sheet.

Figure 21: Principle program steps of a µC based software to control the converter in CMD and CONT Mode

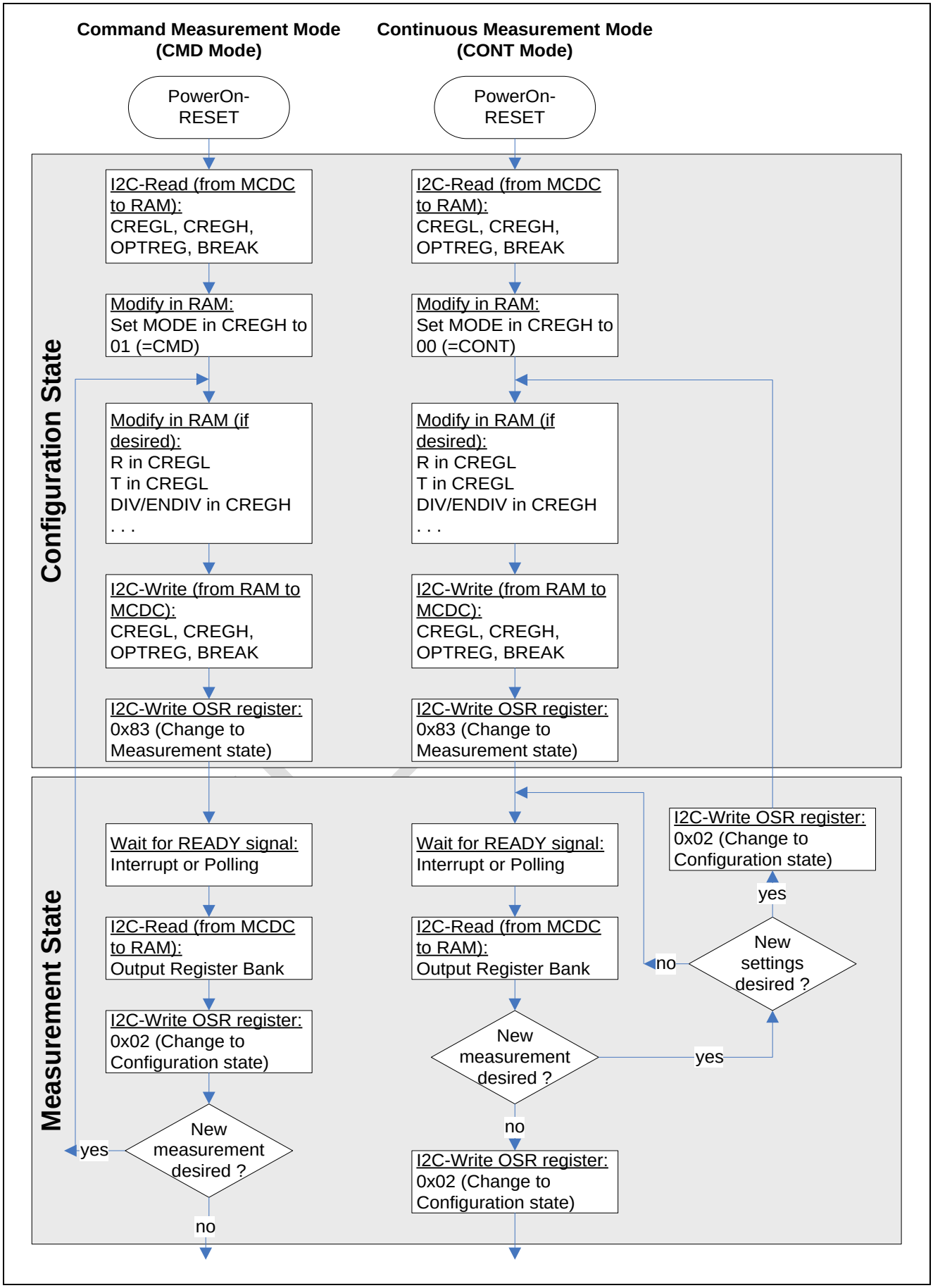
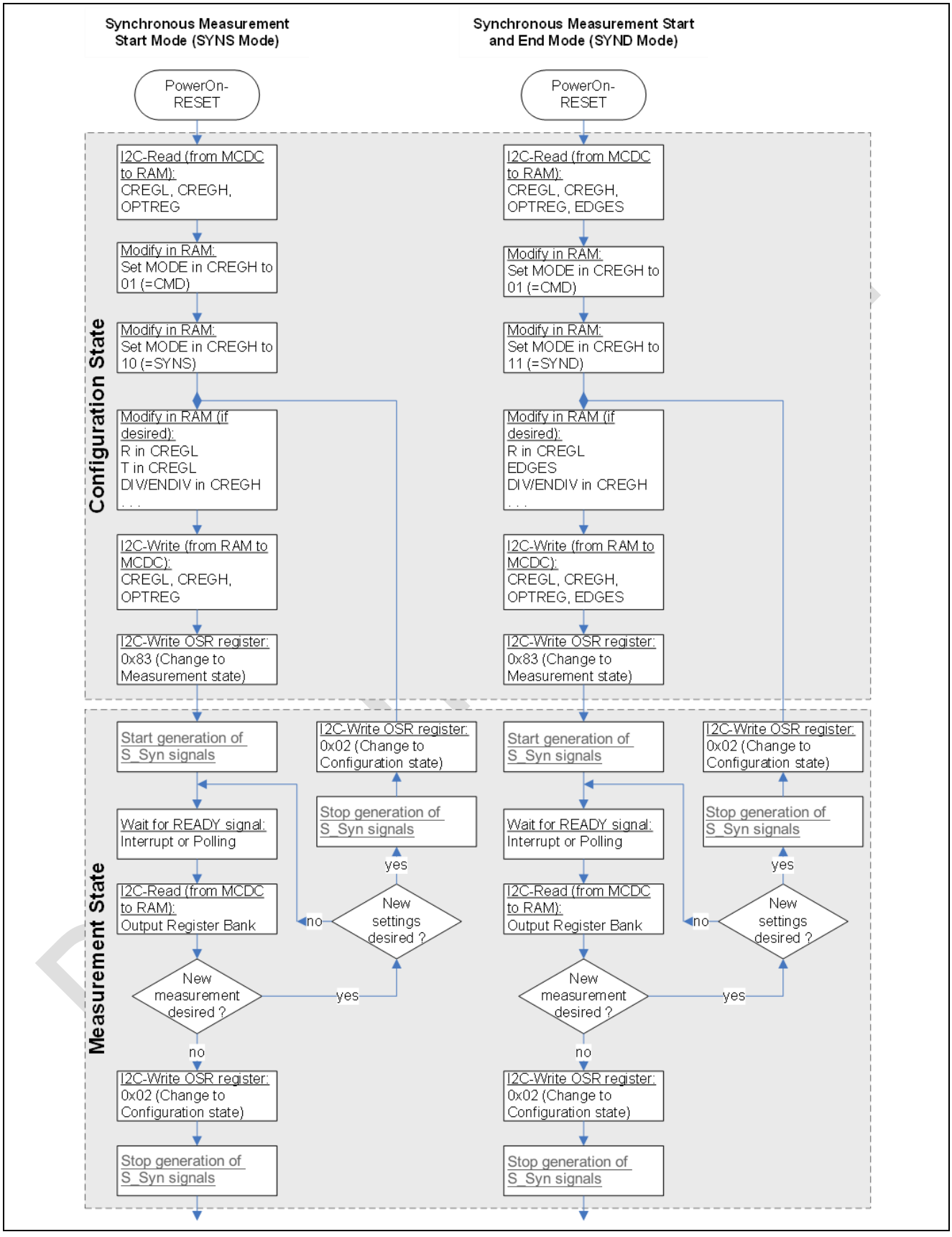


Figure 22: Principle program steps of a µC based software to control the converter in SYNS and SYND Mode[29]



[29] S_Syn is a Software variable of a µC based software to control the converter in SYNS and SYND Mode which is generated from the external SYN signal

The following pseudo code illustrates the procedures for principle program steps for functions I²C-Write and I²C-Read.

```
BOOL I2cMasterSendData(BYTE I2cAddr, USHORT RegAddr, BYTE *Data, SHORT Datasize)
{
    BOOL ErrReturn = (Datasize > 0) ? TRUE : FALSE;
    BYTE ErrCode=0;
    ULONG WaitLoop;

    // clear RX
    I2C_ReceiveData(I2C_INTERFACE);

    // Datasize must be greater 0
    while(ErrReturn==TRUE)
    {
        // send I2C START
        I2C_GenerateSTART(I2C_INTERFACE, ENABLE);

        // test for completion
        if(I2cWaitEvent(I2C_EVENT_MASTER_MODE_SELECT) == FALSE)
        {
            ErrCode = 0x81;
            ErrReturn = FALSE;
            break;
        }
        // send I2C slave address (R/W=Write)
        I2C_Send7bitAddress(I2C_INTERFACE, I2cAddr, I2C_Direction_Transmitter);

        // test for completion, TXE, master mode activ, TRA
        if(I2cWaitEvent(I2C_EVENT_MASTER_TRANSMITTER_MODE_SELECTED) == FALSE)
        {
            ErrCode = 0x82;
            ErrReturn = FALSE;
            break;
        }
        // send register adress
        I2C_SendData(I2C_INTERFACE, RegAddr));

        // data transmission loop
        while(Datasize--)
        {
            // wait for BTF
            if(I2cWaitEvent(I2C_EVT_BTF) == FALSE)
            {
                ErrCode = 0x84;
                ErrReturn = FALSE;
                break;
            }
            // send data byte
            I2C_SendData(I2C_INTERFACE, *Data);

            // prepare next
            Data++;
```

```
        }

        // wait for transmission complete
        if(I2cWaitEvent(I2C_EVENT_MASTER_BYTE_TRANSMITTED) == FALSE)
        {
            ErrCode = 0x85;
            ErrReturn = FALSE;
            break;
        }

        // generate STOP
        I2C_GenerateSTOP(I2C_INTERFACE, ENABLE);
        // wait a moment
        WaitLoop = 0;
        while(WaitLoop++ < 20);

        // completion
        break;
    }

    // in case of error: I2C reinit */
    if(ErrReturn==FALSE)
    {
        I2C_GenerateSTOP(I2C_INTERFACE, ENABLE);
        ReinitI2cMaster(ErrCode);
    }
    return ErrReturn;
}


BOOL I2cMasterReadData(BYTE I2cAddr, BYTE Addr, BYTE *Data, SHORT Datasize)
{
    BOOL ErrReturn = (Datasize > 0) ? TRUE : FALSE;
    BYTE ErrCode=0;
    ULONG WaitLoop;

    // clear RX
    I2C_ReceiveData(I2C_INTERFACE);

    // Datasize must be greater 0
    while(ErrReturn==TRUE)
    {
        // send I2C START
        I2C_GenerateSTART(I2C_INTERFACE, ENABLE);

        // test for completion
        if(I2cWaitEvent(I2C_EVENT_MASTER_MODE_SELECT) == FALSE)
        {
            ErrCode = 0x01;
            ErrReturn = FALSE;
            break;
        }
```

```
        // send I2C slave address (R/W=Write)
        I2C_Send7bitAddress(I2C_INTERFACE, I2cAddr, I2C_Direction_Transmitter);

        // test for completion, TXE, master mode activ, TRA
        if(I2cWaitEvent(I2C_EVENT_MASTER_TRANSMITTER_MODE_SELECTED) == FALSE)
        {
            ErrCode = 0x02;
            ErrReturn = FALSE;
            break;
        }

        // send register adress
        I2C_SendData(I2C_INTERFACE, Addr);

        // wait for transmission complete
        if(I2cWaitEvent(I2C_EVENT_MASTER_BYTE_TRANSMITTED) == FALSE)
        {
            ErrCode = 0x04;
            ErrReturn = FALSE;
            break;
        }

        // only if Datasize>1: enable ACK
        if(Datasize>1)
        {
            I2C_AcknowledgeConfig(I2C_INTERFACE, ENABLE);
        }

        // send I2C START
        I2C_GenerateSTART(I2C_INTERFACE, ENABLE);

        // test for completion
        if(I2cWaitEvent(I2C_EVENT_MASTER_MODE_SELECT) == FALSE)
        {
            ErrCode = 0x05;
            ErrReturn = FALSE;
            break;
        }

        // send I2C slave address (R/W=Read)
        I2C_Send7bitAddress(I2C_INTERFACE, I2cAddr, I2C_Direction_Receiver);

        // MSL, ADDR, BUSY
        if(I2cWaitEvent(I2C_EVENT_MASTER_RECEIVER_MODE_SELECTED) == FALSE)
        {
            ErrCode = 0x06;
            ErrReturn = FALSE;
            break;
        }

        // data receive loop
        while(Datasize > 1)
        {
```

```
            // wait for data byte
            if(I2cWaitEvent(I2C_EVT_RXNE) == FALSE)
            {
                ErrCode = 0x07;
                ErrReturn = FALSE;
                break;
            }

            // read data byte
            *Data = I2C_ReceiveData(I2C_INTERFACE);

            // prepare next
            Data++;
            Datasize--;
        }

        // disable ACK
        I2C_AcknowledgeConfig(I2C_INTERFACE, DISABLE);

        // wait for last data byte
        if(I2cWaitEvent(I2C_EVT_RXNE) == FALSE)
        {
            ErrCode = 0x08;
            ErrReturn = FALSE;
            break;
        }
        // read data byte
        *Data = I2C_ReceiveData(I2C_INTERFACE);

        // generate STOP
        I2C_GenerateSTOP(I2C_INTERFACE, ENABLE);
        // wait a moment
        WaitLoop = 0;
        while(WaitLoop++ < 20);

        // completion
        break;
    }

    // in case of error: I2C reinit */
    if(ErrReturn==FALSE)
    {
        I2C_GenerateSTOP(I2C_INTERFACE, ENABLE);
        ReinitI2cMaster(ErrCode);
    }

    return ErrReturn;
}
```

9 NOTES FOR PCB LAYOUT

The connections to the inputs IN0…IN3 of the AS89010 have to be protected against any kind of electromagnetic coupling and have to be guarded with VRT potential to avoid leakage currents. Without guarding layers at the inputs the isolation resistance of the PCB gives leakage currents with equivalent values like the sensor currents!

The analog supply for AS89010 must be placed as close as possible to the converter. The connection between the analog and digital ground should be beneath (LP level) and/or near the AS89010.

Digital signals and circuit lines with high current loads must not be used directly beneath and next to the photodiode sensor as well as the AS89010.

The AS89010 converter operates internally with minimal currents (pAmps). Therefore, protection measures need to be performed to shield the ASIC against EMC stress or external interferences.

The connections between the photodiode sensor (anode and de) and the AS89010 should be as short as possible (<10 mm) and without interlayer connections.

Photodiode Sensor, AS89010 and its R_{EXT} should be placed on the same PCB side. The signal VRT (common cathode or common anode) should have the same cross-section as the four sensor connectors.

Around signal lines a conductor connected with VRT should be created. One level below the signals a VRT potential area should be created that extends only to the analog inputs and the signal lines.

ORDERING INFORMATION

NAME	Status	PACKAGE	Article
AS89010	Series	SSOP16	305030004

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