

# AS7220

## Calibrated CCT and Lumen Maintenance Smart Lighting Manager

### General Description

The AS7220 Smart Lighting Manager is part of the **ams** Cognitive Lighting™ family of products that enable lights to autonomously adapt to human lighting and energy conservation needs. The device is equipped with an advanced Cognitive Lighting Engine (CLE) to optimize CCT and lumen maintenance and color maintenance via a combination of PWM and/or 0-10V controls with dimming ballasts. Daylight harvesting can also be performed by adding an I<sup>2</sup>C connected **ams** ambient light sensor.

AS7220 XYZ chromatic white/color sensing provides mapping to x, y (z) of the CIE 1931 2-dimensional color gamut coordinates and scales the coordinates to the CIE 1976 u'v' coordinate system. The AS7220 integrates standard observer filters into standard silicon via nano-optic deposited interference filters which deliver high-stability over time and temperature. The LGA package includes a built-in aperture to control light entering the sensor array. Integrated intelligence enables lifetime CCT calibration to within 2-4 Macadam steps.

The AS7220 connects to standard 0-10V dimmer inputs and drives 0-10V dimming ballasts/drivers to enable a highly cost-effective white tunable current-steering luminaire design with a single-channel constant current ballast. Direct PWM inputs can also interface to standard LED drivers or multi-channel ballasts for constant voltage LED lighting architectures.

*[Ordering Information](#) and [Content Guide](#) appear at end of datasheet.*

## Key Benefits & Features

The benefits and features of this device are listed below:

**Figure 1:**  
**Added Value of Using AS7220**

| Benefits  | Features   |
|---|--|
| <ul style="list-style-type: none"> <li>Accurate maintenance of CCT and daylight responsive lighting</li> </ul>                    | <ul style="list-style-type: none"> <li>Calibrated XYZ tri-stimulus color sensing for direct translation to CIE 1931/1976 standard observer color maps</li> </ul>                       |
| <ul style="list-style-type: none"> <li>Lifetime-calibrated sensing with minimal drift over time or temperature</li> </ul>         | <ul style="list-style-type: none"> <li>Filter set realized by silicon interference filters</li> </ul>  |
| <ul style="list-style-type: none"> <li>Optional user/manufacture configurable CCT maintenance and/or Lumen maintenance</li> </ul> | <ul style="list-style-type: none"> <li>If enabled, desired CCT and/or Lumen settings are read by the Cognitive Light Engine and maintained by using spectrally tuned light</li> </ul>  |
| <ul style="list-style-type: none"> <li>Compatible with standard dimmer controls and occupancy sensors</li> </ul>                  | <ul style="list-style-type: none"> <li>Directly interfaces to 0-10V dimmer controls and standard occupancy sensors</li> </ul>  |
| <ul style="list-style-type: none"> <li>Directly interfaces to LED string circuitry via PWM outputs</li> </ul>                     | <ul style="list-style-type: none"> <li>Built-in PWM generators to dim and control warm/cool luminaire LED strings</li> <li>12-bit resolution for precise control down to 1%</li> </ul> |
| <ul style="list-style-type: none"> <li>Directly interfaces to ballast via 0-10V</li> </ul>  | <ul style="list-style-type: none"> <li>0-10V analog output for control of conventional dimming ballasts in a current steering design</li> </ul>  |
| <ul style="list-style-type: none"> <li>Small package, wide operating range with critical optics built-in</li> </ul>               | <ul style="list-style-type: none"> <li>20-pin LGA package 4.5mm x 4.7mm x 2.5mm with integrated aperture</li> <li>-40 °C to 85°C</li> </ul>  |

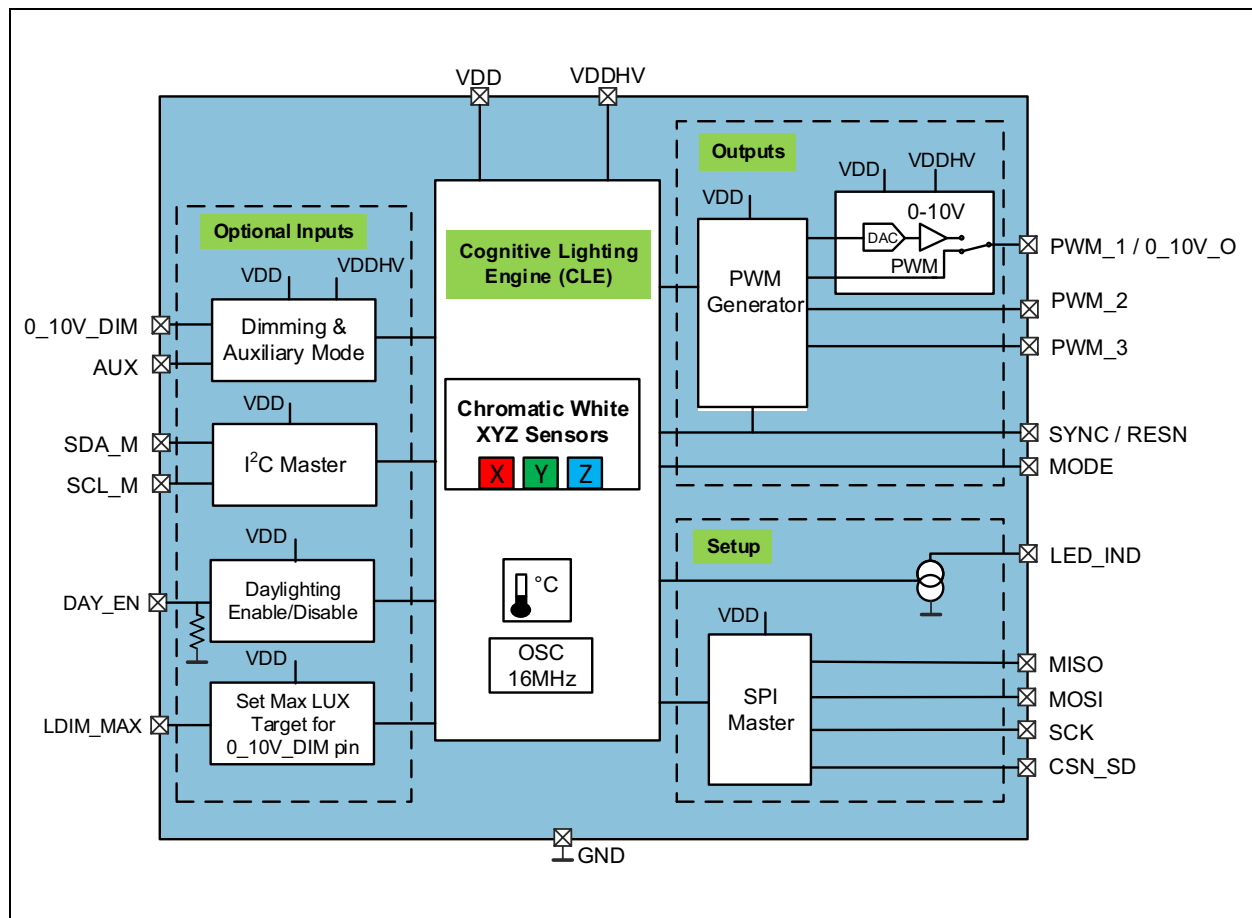
## Applications

Autonomous, solid-state lighting manager for precision fixed CCT and daylight harvesting:

- Configurable CCT and/or lumen maintenance applications
- luminaires intended to meet California Title 24 daylighting requirements

## Block Diagram

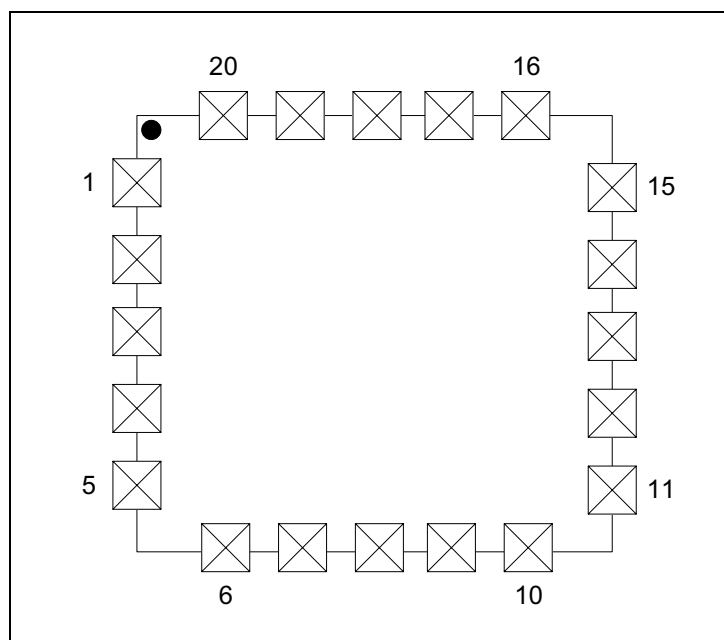
**Figure 2:**  
**Functional Blocks of AS7220**



**Functional Blocks of AS7220:** The AS7220 provides closed loop Chromatic White sensing and PWM tuning while interfacing to local controls or other sensors

## Pin Assignments

**Figure 3:**  
Pin Diagram of AS7220 (Top View)



**Figure 4:**  
Pin Description of AS7220 (20 Pin LGA)

| Pin Number | Pin Name | Description   |
|------------|----------|---|
| 1          | PWM_3    | Digital PWM 3   |
| 2          | SYNC     | SYNC input  |
|            | RESN     | Reset pin, active low   |
| 3          | SCK      | SPI serial clock  |
| 4          | MOSI     | SPI MOSI  |
| 5          | MISO     | SPI MISO  |
| 6          | CSN_EE   | Chip select for the required external serial flash memory, active low |
| 7          | CSN_SD   | Chip select for SD Card interface, active low                         |
| 8          | AUX      | Auxiliary mode input pin  |
| 9          | SCL_M    | I <sup>2</sup> C master clock pin                                     |
| 10         | SDA_M    | I <sup>2</sup> C master data pin                                      |
| 11         | DAY_EN   | Daylight enable, active high  |
| 12         | LDIM_MAX | Sets maximum lumen for 0_10V_DIM inputs                               |

| Pin Number | Pin Name  | Description                                       |
|------------|-----------|---|
| 13         | 0_10V_DIM | 0-10V input dimming pin                           |
| 14         | VDDHV     | High voltage supply                               |
| 15         | MODE      | Mode selection pin                                |
| 16         | GND       | Ground  |
| 17         | VDD       | Low voltage supply                                |
| 18         | LED_IND   | LED driver output for indicator LED, current sink |
| 19         | PWM_1     | Digital PWM 1                                     |
|            | 0_10V_O   | 0-10V output pin                                  |
| 20         | PWM_2     | Digital PWM 2                                     |

## Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The device is not designed for high energy UV (ultraviolet) environments, including upward looking outdoor applications, which could affect long term optical performance.

**Figure 5:**  
**Absolute Maximum Ratings**

| Symbol                                    | Parameter                          | Min   | Max         | Units | Comments   |
|---|------------------------------------|-------|-------------|-------|--|
| Electrical Parameters                     |                                    |       |             |       |  |
| V <sub>DD_MAX</sub>                       | Supply Voltage VDD                 | -0.3  | 5           | V     | Pin VDD to GND, Low voltage pin  |
| V <sub>DDHV_MAX</sub>                     | Supply Voltage VDDHV               | -0.3  | 20          | V     | Pin VDDHV to GND, High voltage pin   |
| V <sub>DD_IO</sub>                        | Input/Output Pin Voltage           | -0.3  | VDD + 0.3   | V     | Low voltage pins to GND  |
| V <sub>DDHV_IO</sub>                      | Input/Output Pin Voltage           | -0.3  | VDDHV + 0.3 | V     | High voltage pins to GND   |
| I <sub>SCR</sub>                          | Input Current (latch-up immunity)  | ± 100 |             | mA    | JESD78D  |
| Electrostatic Discharge                   |                                    |       |             |       |  |
| ESD <sub>HBM</sub>                        | Electrostatic Discharge HBM        | ±1000 |             | V     | JS-001-2014  |
| ESD <sub>CDM</sub>                        | Electrostatic Discharge CDM        | ±500  |             | V     | JSD22-C101F  |
| Temperature Ranges and Storage Conditions |                                    |       |             |       |  |
| T <sub>strg</sub>                         | Storage Temperature                | -40   | 85          | °C    |  |
| T <sub>body</sub>                         | Package Body Temperature           |       | 260         | °C    | IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices” |
| RH <sub>NC</sub>                          | Relative Humidity (non-condensing) | 5     | 85          | %     |  |
| MSL                                       | Moisture Sensitivity Level         | 3     |             |       | Represents a 168 hour max. floor lifetime  |

## Electrical Characteristics

All limits are guaranteed with  $V_{DD} = 3.3V$ ,  $V_{DDHV} = 12V$ ,  $T_{AMB} = 25^{\circ}C$ . The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

If  $V_{DD}$  and  $V_{DDHV}$  are to be the same voltage, they should be sourced by the same 2.97-3.6V supply.

**Figure 6:**  
Electrical Characteristics

| Symbol                                   | Parameter                        | Conditions                                | Min      | Typ | Max   | Unit        |
|--|----------------------------------|---|----------|-----|-------|-------------|
| <b>General Operating Conditions</b>      |                                  |   |          |     |       |             |
| $V_{DD}$                                 | Low Voltage Operating Supply     |   | 2.97     | 3.3 | 3.6   | V           |
| $V_{DDHV}$                               | High Voltage Operating Supply    |   | $V_{DD}$ | 12  | 15    | V           |
| $T_{AMB}$                                | Operating Temperature            |   | -40      | 25  | 85    | $^{\circ}C$ |
| $I_{VDD}$                                | Operating Current                |   |          |     | 5     | mA          |
| <b>Internal RC Oscillator</b>            |                                  |   |          |     |       |             |
| $F_{OSC}$                                | Internal RC Oscillator Frequency |   | 15.7     | 16  | 16.3  | MHz         |
| $t_{JITTER}^{(1)}$                       | Jitter                           | @25 $^{\circ}C$                           |          |     | 1.2   | ns          |
| <b>0-10V Output (0_10V_O pin)</b>        |                                  |   |          |     |       |             |
| $R_{OUT\_10}$                            | Resistive Load                   |   | 1        |     |       | k $\Omega$  |
| $I_{S\_10}$                              | Source Current                   |   | 10       |     |       | mA          |
| $I_{SINK\_10}$                           | Sink Current                     |   | -10      |     |       | mA          |
| $I_{LEAK\_HV}$                           | HV Output Leakage Current        | $V_{IN}=12V$ , DAC and PWM1 both disabled | -1.6     |     | -0.73 | mA          |
| $C_{LOAD\_10}$                           | Capacitive Load                  |   |          |     | 100   | pF          |
| $V_{OUT\_10}^{(2)}$                      | Output Swing                     |   | 0        |     | 10    | V           |
| <b>AUX Input</b>                         |                                  |   |          |     |       |             |
| $AUX_{IN}$                               | AUX Input Voltage                | For 100% AUX A/D Conversion               |          | 3.0 |       | V           |
| $R_{IN\_AUX}$                            | Analog Input Resistance          |   | 168      | 240 | 312   | k $\Omega$  |
| <b>0-10V Inputs (0_10V_DIM and LDIM)</b> |                                  |   |          |     |       |             |
| $R_{IN\_HV}$                             | Analog Input Resistance          | $V_{DDHV} \geq 12V$                       | 138      | 200 | 315   | k $\Omega$  |

| Symbol                            | Parameter   | Conditions          | Min      | Typ | Max        | Unit               |
|-----------------------------------|---|---------------------|----------|-----|------------|--------------------|
| <b>DAY_EN and LDIM Inputs</b>     |   |                     |          |     |            |                    |
| $V_{MAX\_DAY\_EN}$                | Maximum Pin Voltage for DAY_EN                            |                     |          |     | VDD + 0.3  | V                  |
| $V_{MAX\_LDIM}$                   | Maximum Pin Voltage for LDIM                              |                     |          |     | VDDHV+ 0.3 | V                  |
| $R_{INT\_DAY\_EN}$                | Internal Resistor (to GND) for DAY_EN Pin                 |                     |          | 10  |            | k $\Omega$         |
| <b>Temperature Sensor</b>         |   |                     |          |     |            |                    |
| $D_{TEMP}$                        | Absolute Accuracy of the Internal Temperature Measurement |                     | -8.5     |     | 8.5        | $^{\circ}\text{C}$ |
| <b>Indicator LED</b>              |   |                     |          |     |            |                    |
| $I_{IND}$                         | LED Current   |                     | 1        |     | 8          | mA                 |
| $I_{ACC}$                         | Accuracy of Current                                       |                     | -30      |     | 30         | %                  |
| $V_{LED}$                         | Voltage Range of Connected LED                            | Vds of current sink | 0.3      |     | VDD        | V                  |
| <b>Digital Inputs and Outputs</b> |   |                     |          |     |            |                    |
| $I_{IH}, I_{IL}$                  | Logic Input Current                                       | Vin=0V or VDD       | -1       |     | 1          | $\mu\text{A}$      |
| $I_{IL}$<br>SYNC/RESN             | Logic Input Current (SYNC/RESN pin)                       | Vin=0V              | -1       |     | -0.2       | mA                 |
| $V_{IH}$                          | CMOS Logic High Input                                     |                     | 0.7* VDD |     | VDD        | V                  |
| $V_{IL}$                          | CMOS Logic Low Input                                      |                     | 0        |     | 0.3* VDD   | V                  |
| $V_{OH}$                          | CMOS Logic High Output                                    | I=1mA               |          |     | VDD-0.4    | V                  |
| $V_{OL}$                          | CMOS Logic Low Output                                     | I=1mA               |          |     | 0.4        | V                  |
| $t_{RISE}^{(1)}$                  | Current Rise Time   | C(Pad)=30pF         |          |     | 5          | ns                 |
| $t_{FALL}^{(1)}$                  | Current Fall Time   | C(Pad)=30pF         |          |     | 5          | ns                 |

**Note(s):**

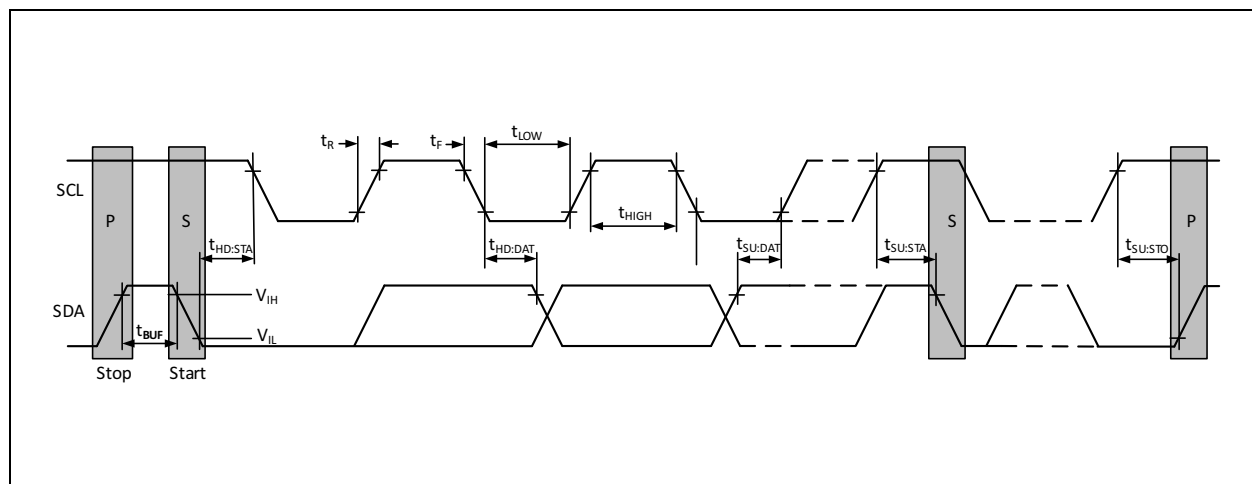
- Guaranteed, not production tested
- For VDDHV>10.5, output max is 10V, else output max tracks VDDHV



**Figure 7:**  
**I<sup>2</sup>C Master Timing Characteristics**

| Symbol                          | Parameter                              | Conditions                                   | Min | Typ | Max | Unit          |
|---------------------------------|--|--|-----|-----|-----|---------------|
| <b>I<sup>2</sup>C Interface</b> |  |  |     |     |     |               |
| $f_{\text{SCLK}}$               | SCL Clock Frequency                    |  |     | 100 | 400 | kHz           |
| $t_{\text{BUF}}$                | Bus Free Time Between a STOP and START |  | 1.3 |     |     | $\mu\text{s}$ |
| $t_{\text{HD:STA}}$             | Hold Time (Repeated) START             |  | 0.6 |     |     | $\mu\text{s}$ |
| $t_{\text{LOW}}$                | LOW Period of SCL Clock                |  | 1.3 |     |     | $\mu\text{s}$ |
| $t_{\text{HIGH}}$               | HIGH Period of SCL Clock               |  | 0.6 |     |     | $\mu\text{s}$ |
| $t_{\text{SU:STA}}$             | Setup Time for a Repeated START        |  | 0.6 |     |     | $\mu\text{s}$ |
| $t_{\text{HD:DAT}}$             | Data Hold Time                         |  | 0   |     | 0.9 | $\mu\text{s}$ |
| $t_{\text{SU:DAT}}$             | Data Setup Time                        |  | 100 |     |     | ns            |
| $t_{\text{R}}$                  | Rise Time of Both SDA and SCL          |  | 20  |     | 300 | ns            |
| $t_{\text{F}}$                  | Fall Time of Both SDA and SCL          |  | 20  |     | 300 | ns            |
| $t_{\text{SU:STO}}$             | Setup Time for STOP Condition          |  | 0.6 |     |     | $\mu\text{s}$ |
| $C_{\text{B}}$                  | Capacitive Load for Each Bus Line      | CB — total capacitance of one bus line in pF |     |     | 400 | pF            |
| $C_{\text{I/O}}$                | I/O Capacitance (SDA, SCL)             |  |     |     | 10  | pF            |

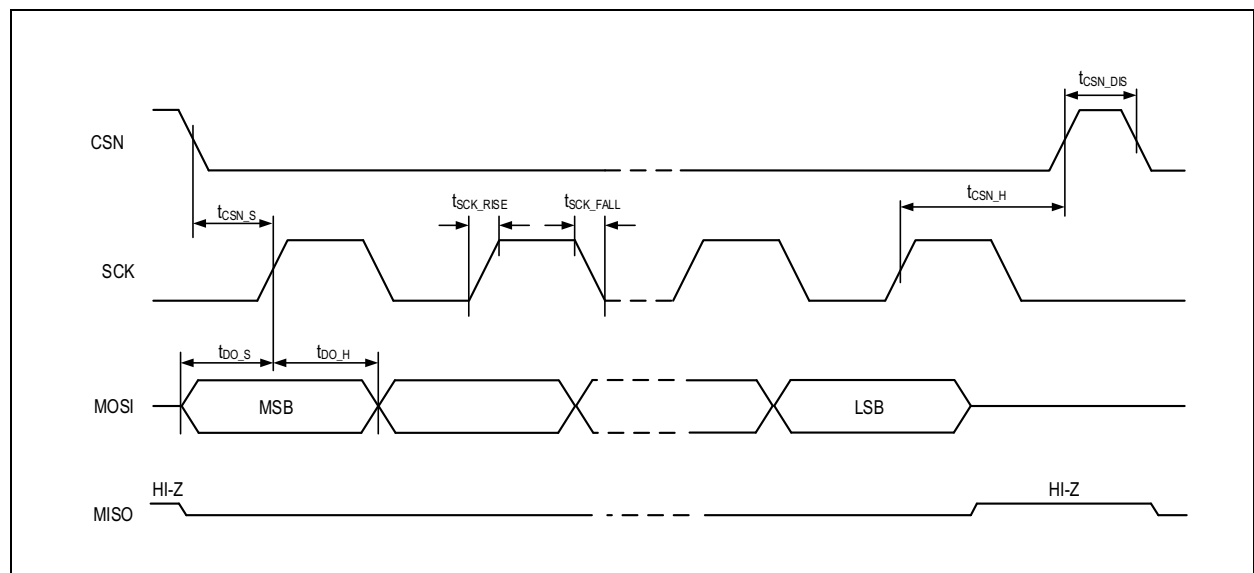
**Figure 8:**  
**I<sup>2</sup>C Master Timing Diagram**



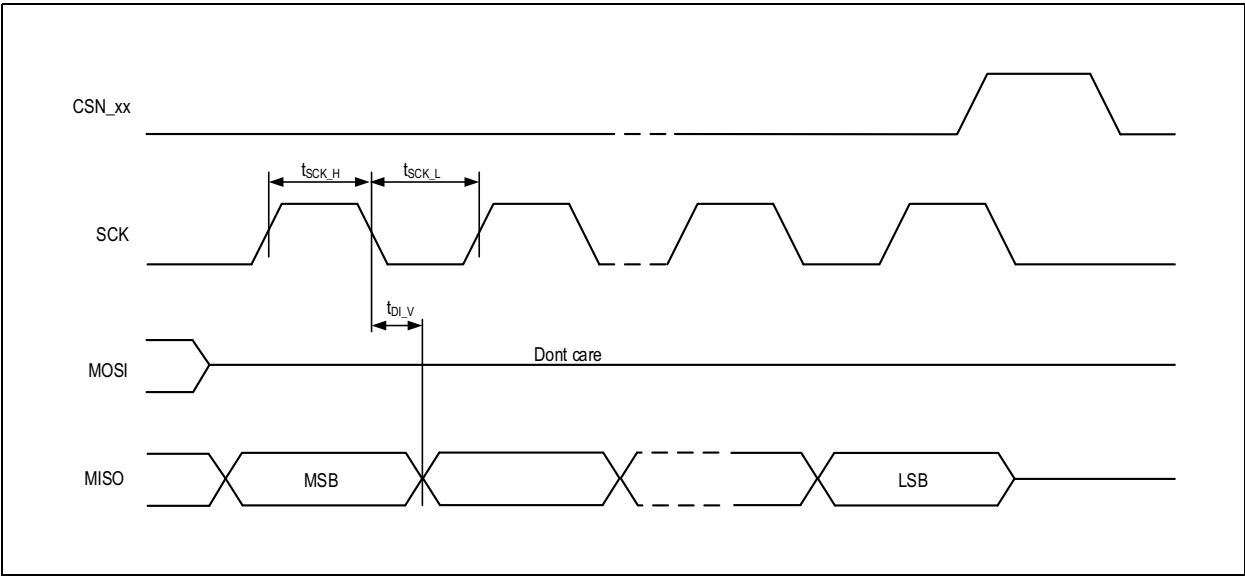
**Figure 9:**  
SPI Timing Characteristics

| Symbol               | Parameter           | Conditions  | Min | Typ | Max | Unit |
|----------------------|---------------------|---|-----|-----|-----|------|
| <b>SPI Interface</b> |                     |   |     |     |     |      |
| $f_{SCK}$            | Clock Frequency     |   | 0   |     | 16  | MHz  |
| $t_{SCK\_H}$         | Clock High Time     |   | 40  |     |     | ns   |
| $t_{SCK\_L}$         | Clock Low Time      |   | 40  |     |     | ns   |
| $t_{SCK\_RISE}$      | SCK Rise Time       |   | 5   |     |     | ns   |
| $t_{SCK\_FALL}$      | SCK Fall Time       |   | 5   |     |     | ns   |
| $t_{CSN\_S}$         | CSN Setup Time      | Time between CSN high-low transition to first SCK high transition | 50  |     |     | ns   |
| $t_{CSN\_H}$         | CSN Hold Time       | Time between last SCK falling edge and CSN low-high transition    | 100 |     |     | ns   |
| $t_{CSN\_DIS}$       | CSN Disable Time    |   | 100 |     |     | ns   |
| $t_{DO\_S}$          | Data-Out Setup Time |   | 5   |     |     | ns   |
| $t_{DO\_H}$          | Data-Out Hold Time  |   | 5   |     |     | ns   |
| $t_{DI\_V}$          | Data-In Valid       |   | 10  |     |     | ns   |

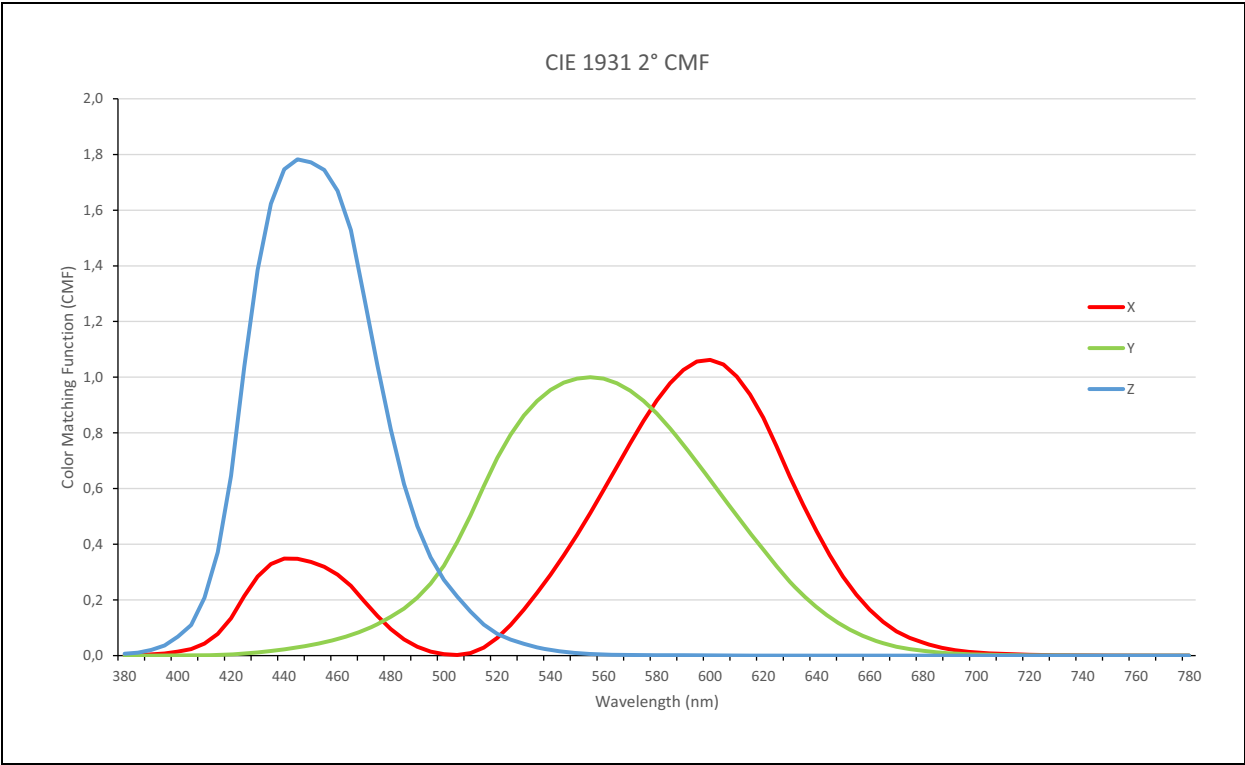
**Figure 10:**  
SPI Master Write Timing Diagram



**Figure 11:**  
**SPI Master Read Timing Diagram**



**Figure 12:**  
**Typical Spectral Responsivity**



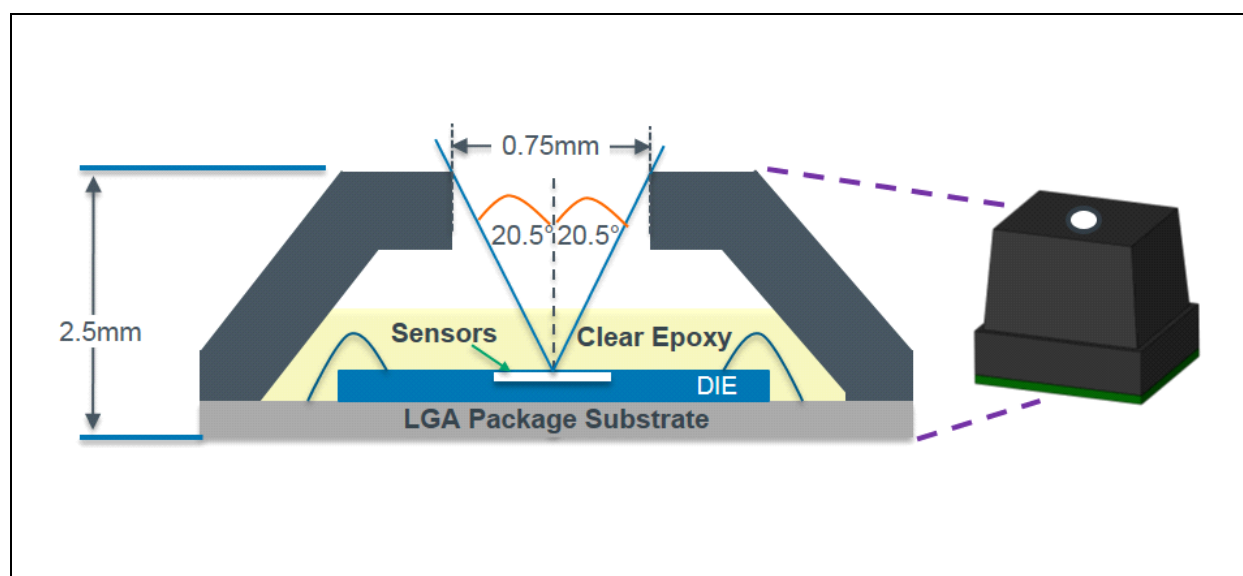
**Figure 13:**  
**AS7220 Optical Characteristics**

| Symbol                 | Parameter                  | Conditions                                    | Min   | Typ <sup>(1)</sup> | Max   | Unit                                     |
|------------------------|----------------------------|---|-------|--------------------|-------|--|
| Color_m <sup>(2)</sup> | Color Measurement Accuracy | White Light CCT=2700K, 3500K, 4500K and 5700K |       | 0.002              |       | du'v'                                    |
| Z_count                | Z Channel Count Accuracy   | White light CCT = 5700K                       | 3.375 | 4.5                | 5.625 | counts/<br>( $\mu\text{W}/\text{cm}^2$ ) |

**Note(s):**

1. Typical values at Lux  $\geq 50$ , Integration time=400.4ms, Gain=1x,  $T_{\text{AMB}} = 25^\circ\text{C}$ .
2. Calibration and measurements are made using diffused light.

**Figure 14:**  
**AS7220 LGA Package Field of View**



## Detailed Description

### AS7220 Smart Lighting Manager - Overview

The Cognitive Light Engine (CLE) is the “brains” of the Smart Lighting Manager. The CLE constantly processes information from the calibrated XYZ chromatic white/color sensor and inputs while controlling outputs. AS7220 initial setup and ongoing parameter storage is automatically performed by software within the required external serial flash memory, via SPI bus.

XYZ color point response is implemented via standard observer interference filters which are extremely stable over time and temperature. Filter accuracy is affected by the optical angle of incidence which itself is limited by an integrated aperture and an internal micro-lens structure in the AS7220. The package field of view (PFOV) is  $\pm 20.5^\circ$  to deliver the specified accuracy. External optics can be used as needed to expand or reduce this built in PFOV.

A luminaire solution for chromatic white/color maintenance with CCT maintenance and/or lumen maintenance requires the AS7220. A luminaire solution with chromatic white color/maintenance, lumen maintenance and daylighting requires only the addition of an **ams** TSL4531 single chip ambient light sensor, connected via I<sup>2</sup>C. Refer to the table in [Figure 15](#) below.

Overall AS7220 timing generation uses an on chip 16MHz temperature compensated oscillator for master clock timing.

Refer to the separate AS7220 User Guide for additional usage and setup information.

**Figure 15:**  
**AS7220 Solution Chart**

| Solution Required           |                   |             | Device Orientation<br>(from luminaire light source) |                     |
|-----------------------------|-------------------|-------------|---|---------------------|
| Chromatic Color Maintenance | Lumen Maintenance | Daylighting | AS7220  | TSL4531 (optional)  |
| ✓                           | ✓                 | ✗           | ↑<br>(into luminaire)                               | ✗<br>(not required) |
| ✓                           | ✓                 | ✓           | ↑<br>(into luminaire)                               | ↓<br>(into room)    |

## XYZ Chromatic White Color Sensor

The XYZ chromatic white/color sensor, part of the AS7220 Cognitive Light Engine (CLE), is a next-generation digital color sensor device. The sensor contains an integrating analog-to-digital converter (16-bit resolution ADC), which integrates current from photodiodes. Upon completion of the conversion cycle, the result is transferred to the corresponding data registers. Transfers are double-buffered to ensure integrity of the data is maintained.

## AS7220 Inputs

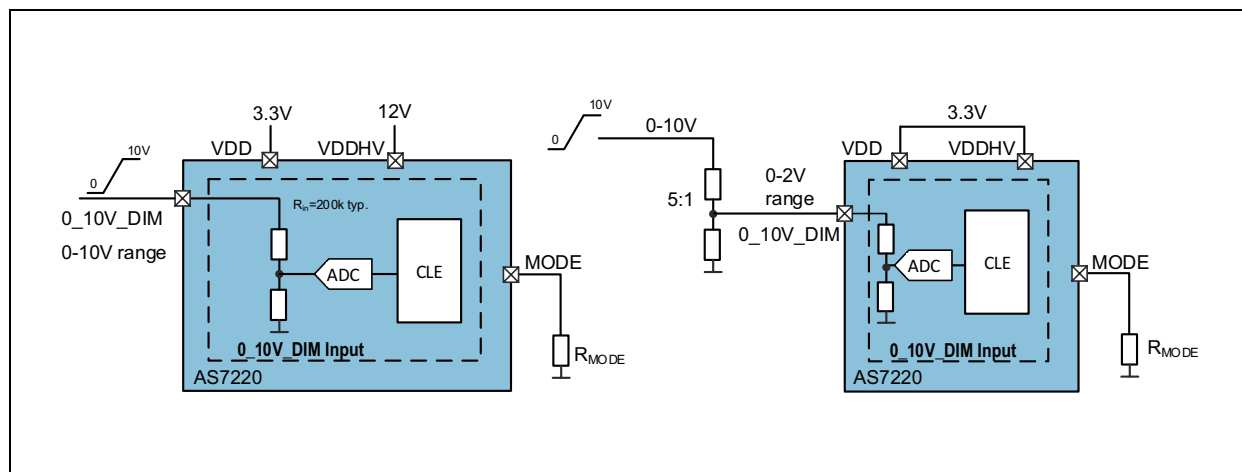
**Figure 16:**  
VDDHV Based Settings for Inputs

| VDDHV                   | Dimming   |
|-------------------------|---|
| 10.5-15V                | Direct input for 0_10V_DIM, dimming input                                 |
| 2.97-10V <sup>(1)</sup> | External 5:1 resistor divider for 0-10V_DIM, dimming input <sup>(2)</sup> |

**Note(s):**

1. For VDDHV ≤ 3.6V, VDDHV and VDD should be tied together.
2. With external dividers connected to 0-10V inputs, the max voltage to the device input is 2V.

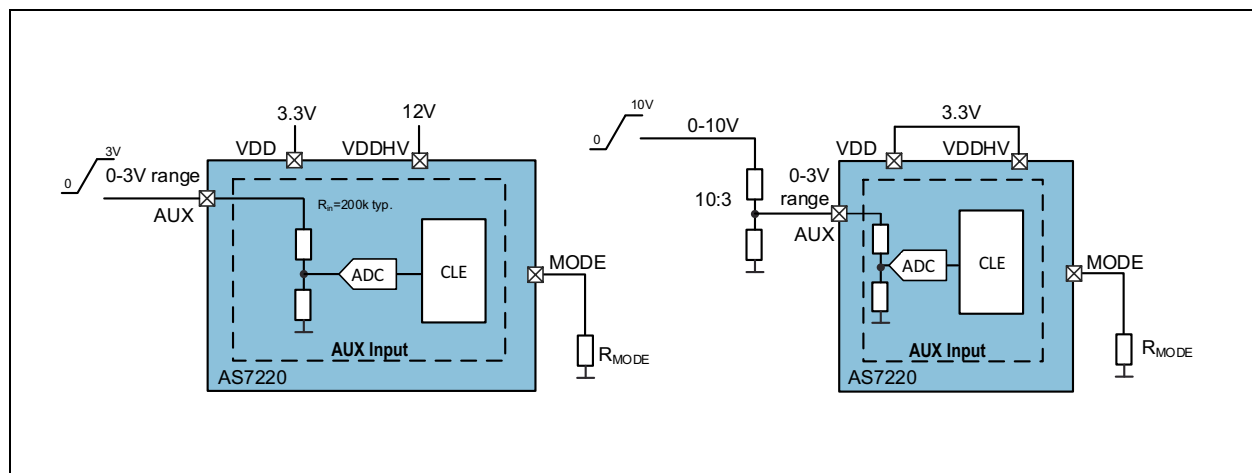
**Figure 17:**  
0-10V Dimming Pin Input



For the AS7220, dimming is accomplished from the input pin (0\_10V\_DIM). Local hardware inputs can be provided by, for example, a slide control dimmer. The 0-10V DIM analog input signal is downscaled by the AS7220 with an internal voltage divider and converted to a 10 bit digital value, 0V=full dimming, 10V=no dimming. When using the internal voltage divider the voltage at the VDDHV pin has to be higher than 10V, typically 12V.

If a second supply is not available, VDDHV and VDD are tied together and the downscale has to be implemented using an external resistor divider. The maximum range in the downscaled input is limited to 2V. Hence to accept a full range 10V signal the input resistor divider has to be 5:1 ratio. Dependent on the level at pin VDDHV the Smart Lighting Manager automatically scales the internal A/D for either a 0-2V or 0-10V range. Refer to the Figures above. If the 0\_10V\_DIM pin is not used, an external resistor pull-up connecting it to VDDHV is recommended.

**Figure 18:**  
**AUX Input**



The AUX input is used as a sensor input to allow additional control, in addition to the 0-10V slider dimming function the 0\_10V\_DIM pin does. The sensed AUX voltage is scaled and used to multiply the dimming scale. The auxiliary sensor input (AUX) has a 0-3V range for its default analog sensing mode. With this 0-3V range external ranges such as 0-10V can be accommodated using external resistor divider networks such as a 10:3 network for a 0-10V occupancy sensor. The AUX pin can also be configured for digital sensing (0, 1 where 1=VDD) in one of two ways. A flash memory reserved location can be set when programming the Flash device for operation, or external I<sup>2</sup>C access port expanders native to the AS7220 can be used to set digital sensing. Refer to the separate AS7220 User Guide for detailed design information for AUX usage. If the AUX pin is not used, an external resistor pull-up connecting it to VDD is recommended.

External sensors with native support by the AS7220 can be added via the I<sup>2</sup>C master interface. For example the **ams** TSL4531 can be used to add Daylighting operation to the AS7220. Once the TSL4531 is detected by the AS7220, and the DAY\_EN pin has been set to 1 (VDD), daylighting operation begins.

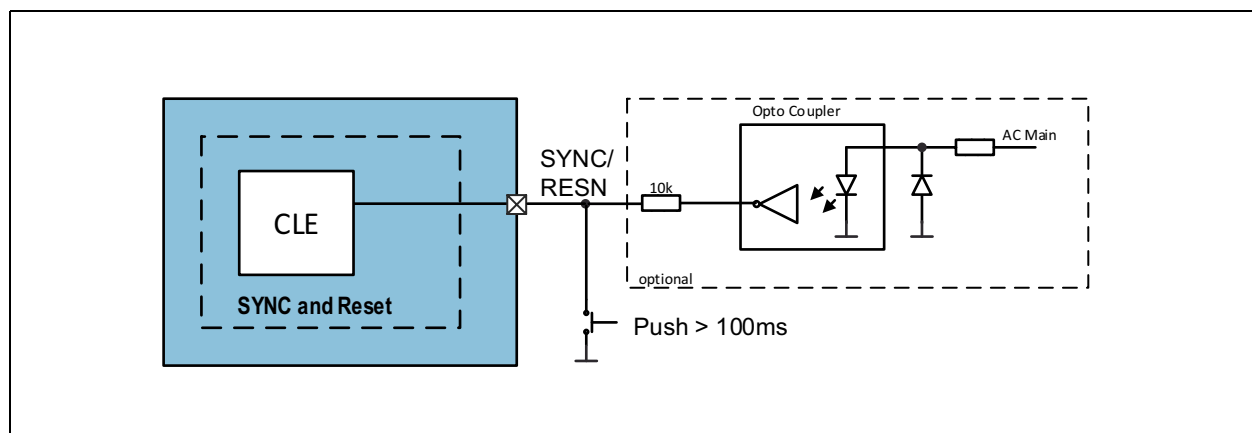
Lumen and/or CCT maintenance can also be configured two ways. One is by programming reserved AS7220 flash memory locations when the entire memory is being programmed.

Alternately, for the flexibility of being able to set these maintenance functions with dip switches designed into the luminaire, the AS7220 I<sup>2</sup>C master interface can be used to interface to I<sup>2</sup>C port expanders that are native to the AS7220. These ports are then automatically used to read dip-switch settings for maintenance. Refer to the separate AS7220 User Guide for detailed design information for Lumen and CCT maintenance.

The AS7220 can also use an input, the LDIM pin, to set a maximum LUX target for the dimmer input (0\_10V\_DIM pin). The LDIM pin voltage is converted to one of five max LUX target settings: 0 (LDIM off), 100, 250, 500 or 1000. An LDIM setting, other than 0 (off), is only used if daylighting is enabled (DAY\_EN pin) and the AS7220 detects an external **ams** TSL4531 needed for daylighting as described above. The daylighting LUX target is set one of two ways. If LDIM is off, the LUX target is set after every movement of the dimmer input by briefly opening the daylighting control loop and measuring LUX. If LDIM is on, the dimmer input sets the LUX target by percentage (0-100%) of the LDIM LUX maximum setting. Refer to the separate AS7220 User Guide for detailed design information for LDIM operation.

### Synchronization and Reset

**Figure 19:**  
**Synchronization and Reset Circuit**



**Synchronization and Reset Circuit:** This figure shows the basic diagram when using reset and synchronization function together.

AS7220 provides optional synchronization of the PWMs. This sync signal can be derived from the AC mains to enable all luminaires in a room to be synchronized to prevent beat frequency flicker. If the SYNC pin is left open, synchronization is automatically disabled by the internal pull-up connected to the SYNC/RESN pin.

Refer to the Figure above. When pulled down for more than 100ms the SYNC/RESN pin will reset the AS7220 Smart Lighting Manager. In this case the push-button “overrides” the output of the opto-coupler. Therefore a resistor should be placed in series with the opto-coupler.



## AS7220 Outputs

The AS7220 outputs, used to control dimming and LED warm/cool strings, can be configured as either three PWM outputs, two PWMs and one analog output, or two PWMs. The PWMs are 12 bit and are factory set to 888 Hz. Refer to the Figure below.

The three PWM outputs, PWM\_1, PWM\_2 and PWM\_3 all switch with the same frequency, but not simultaneously for better EMI performance.

The PWM\_1 output can be set to either analog (0-VDDHV) or digital (0-VDDHV) dimming. Analog dimming range is 0-100%. Digital Dimming range is 0-100%. PWM2 and PWM3 are used for cool white and warm white LED color controlling. Either string can be warm or cool as the AS7220 automatically configures string color type. Range is 0-100% for both PWM2 and PWM3.

To set the desired device operation MODE use the appropriate  $R_{MODE}$  resistor, also shown in the Figure below.

**Figure 20:**  
**Outputs**

| MODE | $R_{MODE}$    | Setting                   | Outputs                              |                                 |
|------|---------------|---------------------------|--------------------------------------|---------------------------------|
|      |               |                           | PWM_1/0_10V_O                        | PWM_2 and PWM_3                 |
| 0    | 100 $\Omega$  | 0-10V analog              | Analog 0-VDDHV <sup>(1)</sup>        | Digital PWMs (0-VDD)            |
| 1    | 470 $\Omega$  | 0-10V digital             | Digital PWM (0-VDDHV) <sup>(1)</sup> | Digital PWMs (0-VDD)            |
| 2    | 1000 $\Omega$ | Digital 2-CH color tuning | n.a.                                 | Digital PWMs (0-VDD), w/Dimming |

**Note(s):**

1. For VDDHV>10.5, output max is 10V, else output max tracks VDDHV.

### Indicator LED

An LED, connected to pin LED\_IND, is used to indicate programming progress of the device. During programming of the AS7220 via an external SD card, the indicator LED starts blinking operation. When programming is finished the indicator LED stays on. The LED\_IND pin is set for 1 mA operation by the AS7220 factory firmware, and is not under user control.

Refer to the separate **ams** document for a complete description of AS7220 Firmware Update Methodology.

## I<sup>2</sup>C Master Interface (Local Sensor Interface)

The I<sup>2</sup>C Master interface can be used to connect external sensors native to the AS7220 (such as Daylight, Occupancy, CO sensors, etc.). Refer to the separate **ams** Application note for external sensor usage with the AS7220.

### I<sup>2</sup>C Feature List

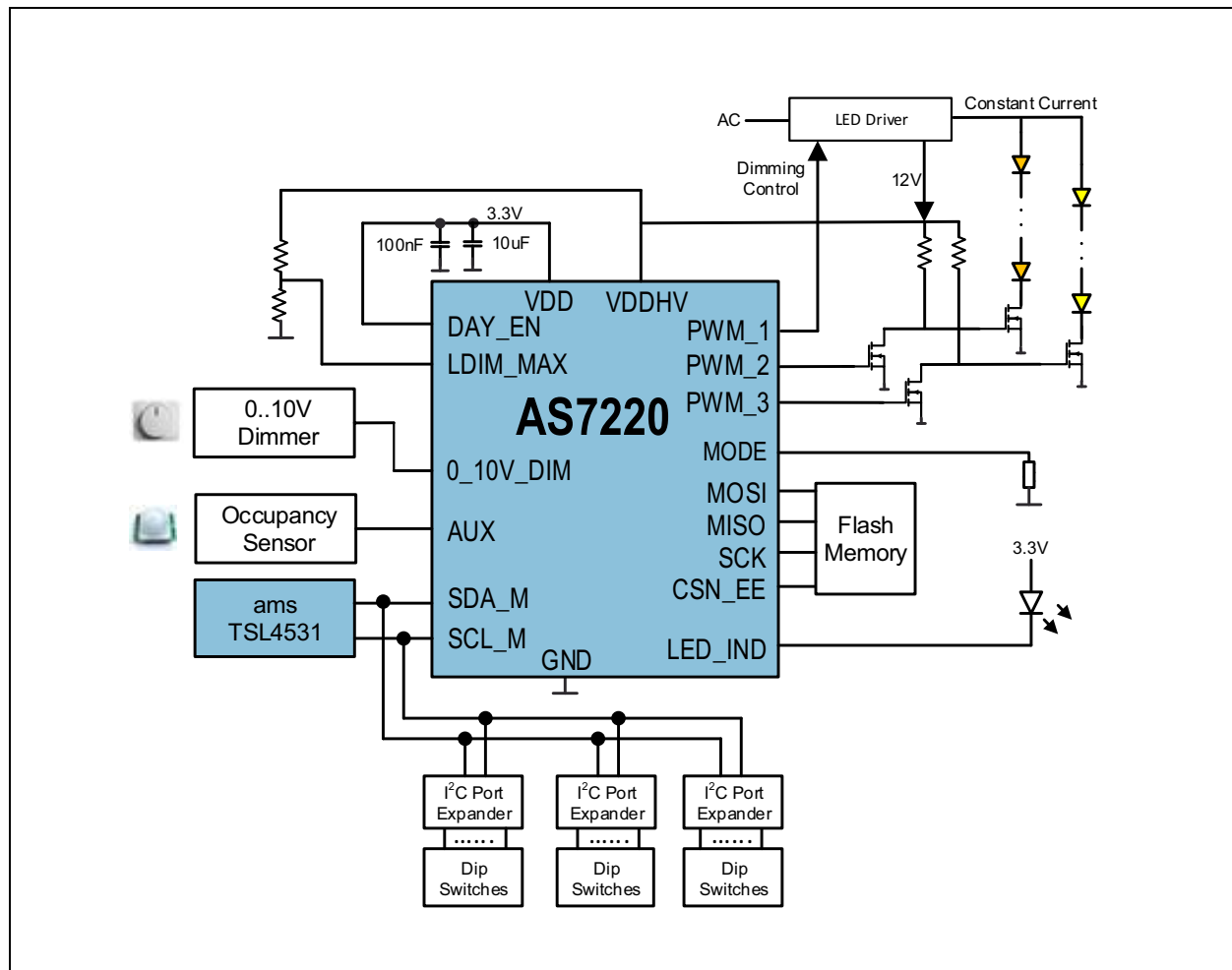
- Clock is set to 100kHz
- 7+1-bit addressing mode.
- **Write formats:** Single-Byte-Write, Page-Write
- **Read formats:** Random-Read, Sequential-Read

The AS7220 is compatible to the NXP two wire specifications.  
[http://www.nxp.com/documents/user\\_manual/UM10204.pdf](http://www.nxp.com/documents/user_manual/UM10204.pdf)  
 Version 4.0 Feb 2012 for standard mode and fast mode.

## Application Information

### Schematics

**Figure 21:**  
**LED Chromatic Color and Lumen Maintenance with Daylighting**



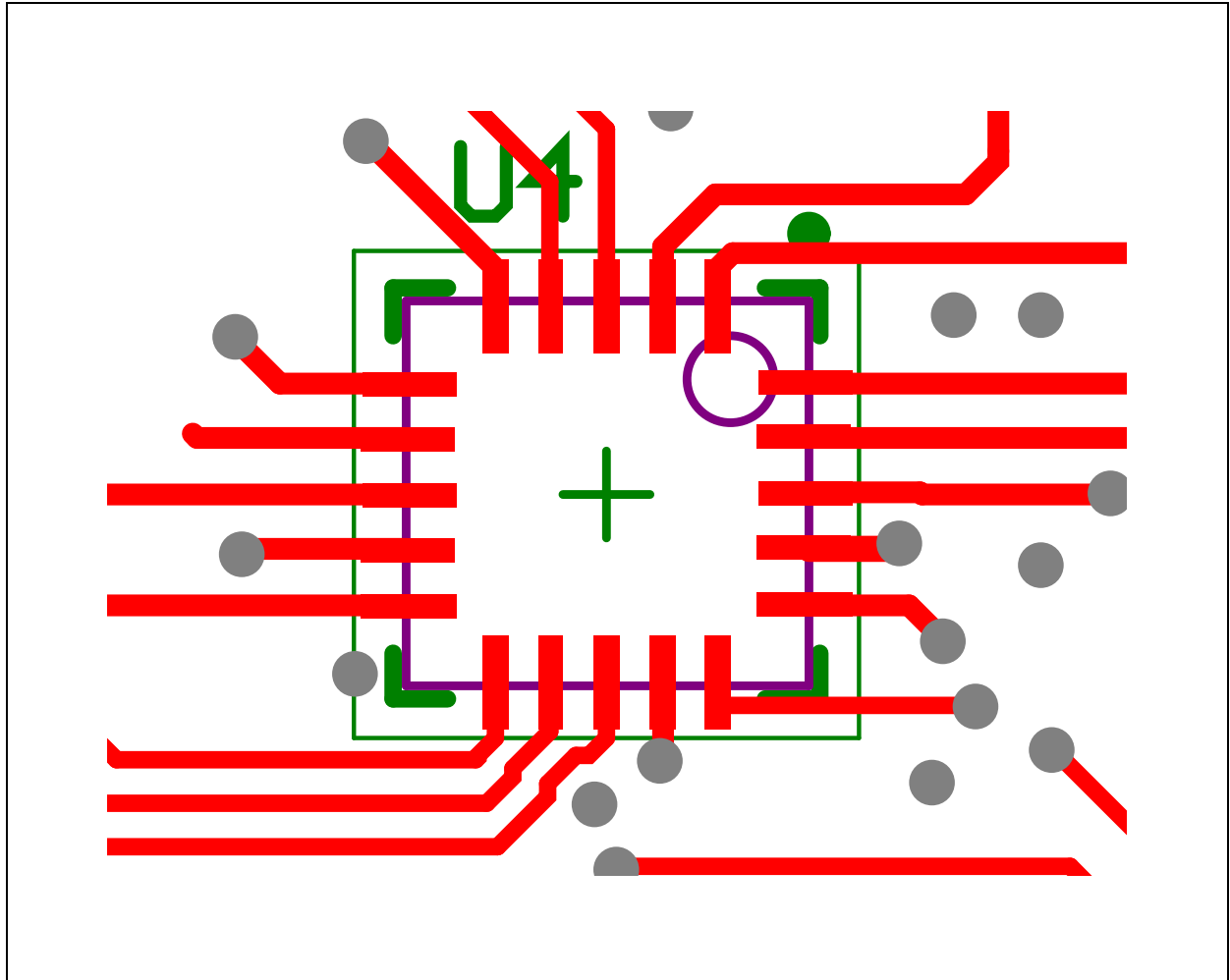
**Note(s):**

1. Mechanically, the AS7220 is inward luminaire looking for color tuning and the **ams** TSL4531 is outward luminaire looking to support Daylighting.
2. The I<sup>2</sup>C port expanders and dip switches are only needed to allow field setting of desired Color and Lumen Maintenance values. The port expanders are not needed if a one time setting of maintenance values when the luminaire is manufactured is desired, as one time settings can be made in the external flash memory at the time of flash programming.
3. Refer to the AS7220 User Guide for detailed design and general information regarding Lumen and CCT maintenance.

## PCB Layout

Suggested PCB pad layout guidelines for the LGA package are shown. Flash Gold is recommended as a surface finish for the landing pads.

**Figure 22:**  
Typical Layout Routing

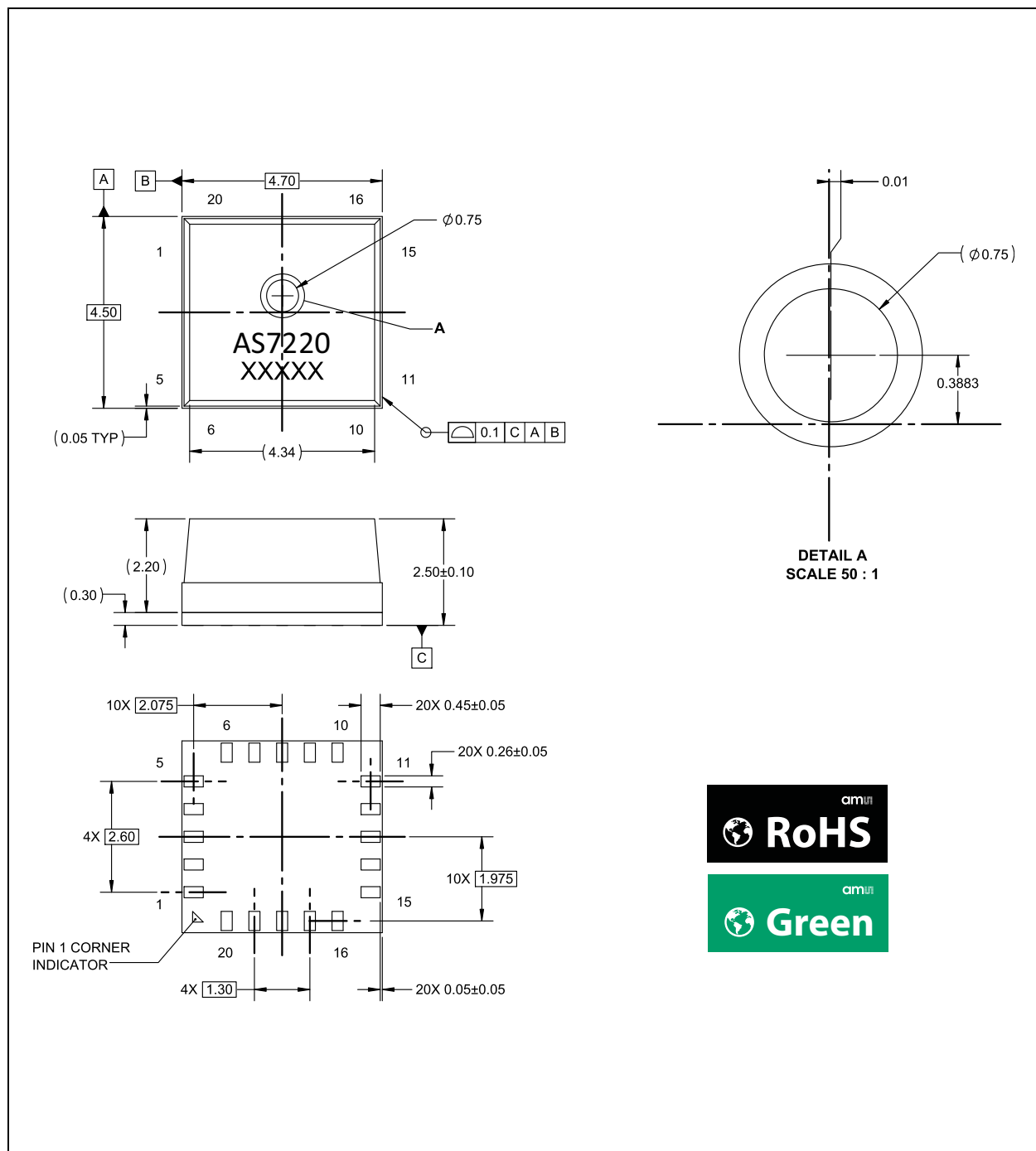


In order to prevent interference, avoid trace routing feedthroughs with exposure directly under the AS7220. An example routing is illustrated in the diagram.

The AS7220 Smart Lighting Integration Kit (SLIK) demo board with schematic and PCB layout documentation is available from **ams** for additional design information.

## Package Drawings & Markings

**Figure 23:**  
Package Drawing



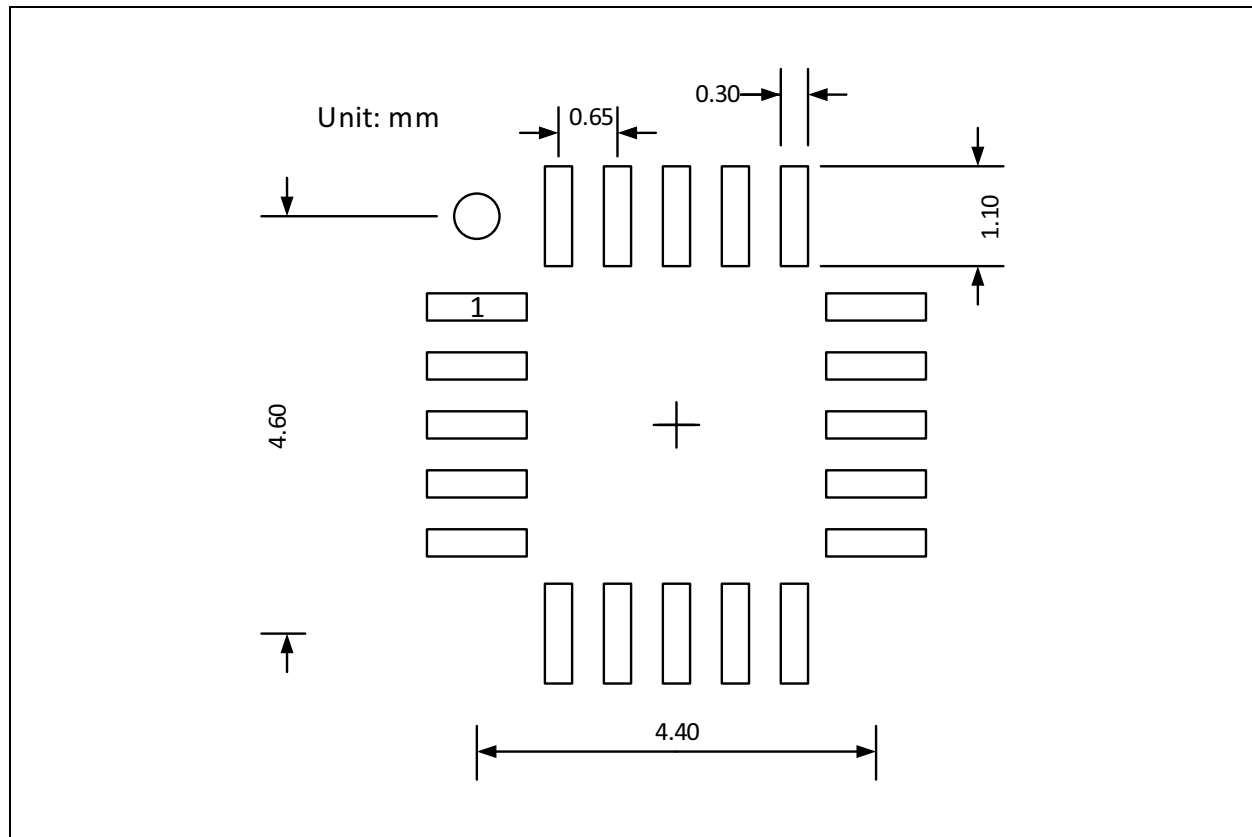
**Note(s):**

1. XXXXX = tracecode
2. Unless otherwise specified, all dimensions are in millimeters.
3. Tolerances: Angular ( $\pm 0.5^\circ$ ), Two Place Decimal ( $\pm 0.015$ ), Three Place Decimal ( $\pm 0.010$ )
4. Contact finish is Au.
5. This package contains no lead (Pb).
6. This drawing is subject to change without notice.

## PCB Pad Layout

Suggested PCB pad layout guidelines for the LGA package are shown. Flash Gold is recommended as a surface finish for the landing pads.

**Figure 24:**  
Recommended PCB Pad Layout

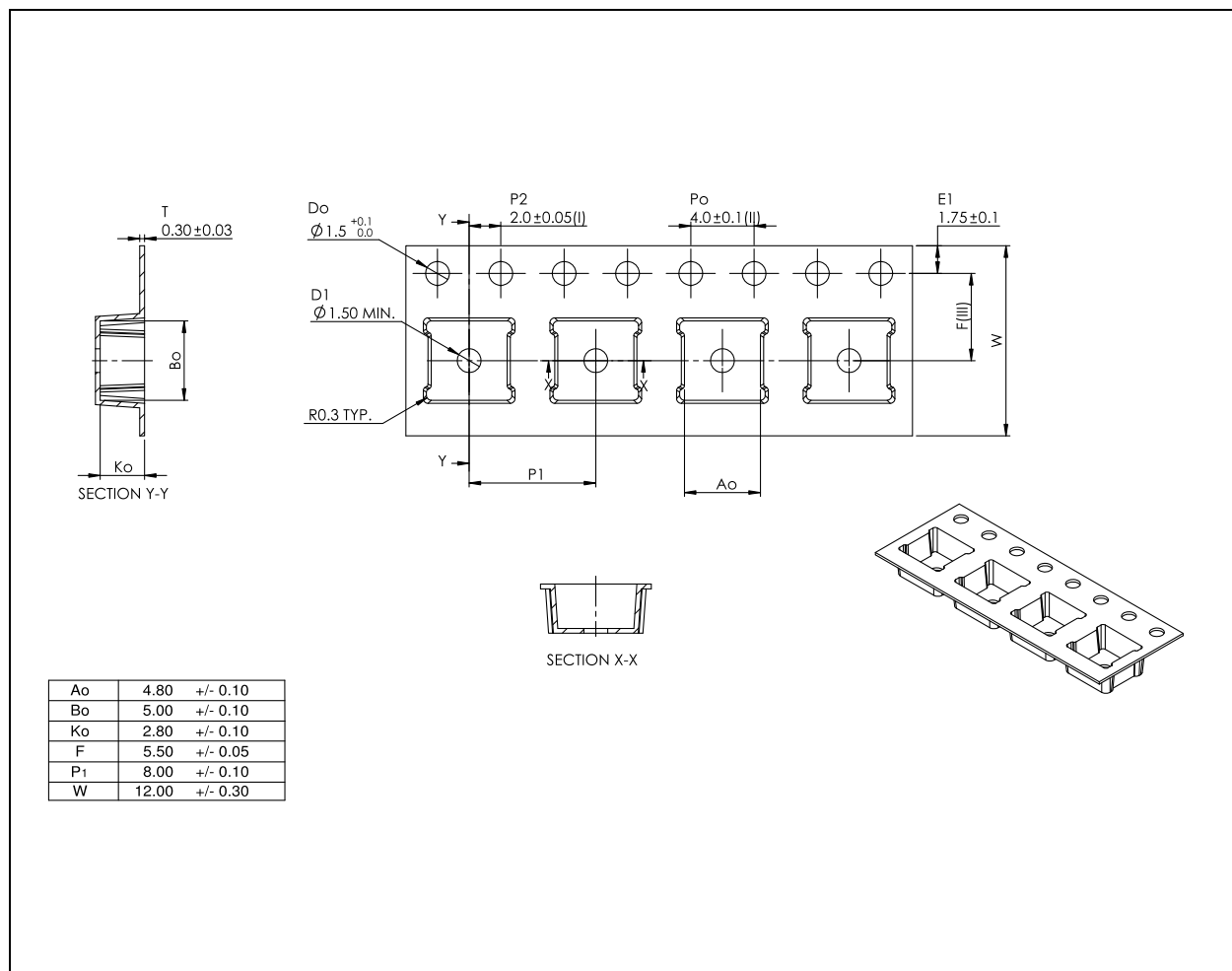


**Note(s):**

1. Unless otherwise specified, all dimensions are in millimeters.
2. Dimensional tolerances are  $\pm 0.05\text{mm}$  unless otherwise noted.
3. This drawing is subject to change without notice.

## Mechanical Data

**Figure 25:**  
Tape & Reel Information



**Note(s):**

1. All dimensions in millimeters unless of otherwise stated.
2. Measured from centreline of sprocket hole to centreline of pocket.
3. Cumulative tolerance of 10 sprocket holes is  $\pm 0.20$ .
4. Measured from centreline of sprocket hole to centreline of pocket.
5. Other material available.

## Soldering, Manufacturing Process Considerations & Storage Information

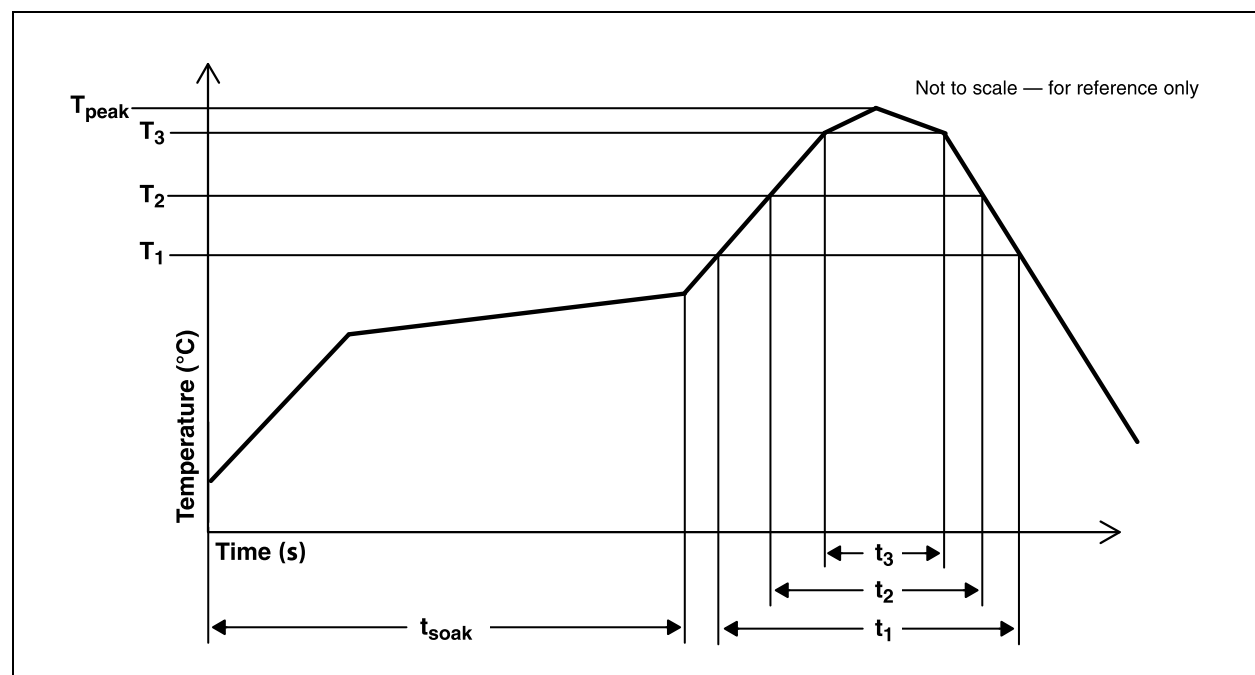
### Solder Reflow Profile

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

**Figure 26:**  
Recommended Reflow Soldering Profile

| Profile Feature                                      | Reference         | Device         |
|--|-------------------|----------------|
| Average temperature gradient in preheating           |                   | 2.5°C/s        |
| Soak Time  | $t_{\text{SOAK}}$ | 2 to 3 minutes |
| Time above 217°C (T1)                                | $t_1$             | Max 60s        |
| Time above 230°C (T2)                                | $t_2$             | Max 50s        |
| Time above $T_{\text{peak}} - 10^\circ\text{C}$ (T3) | $t_3$             | Max 10s        |
| Peak temperature in reflow                           | $T_{\text{peak}}$ | 260°C          |
| Temperature gradient in cooling                      |                   | Max - 5°C/s    |

**Figure 27:**  
Soldering Profile Graph





## Manufacturing Process Considerations

The AS7220 package is compatible with standard reflow no-clean and cleaning processes including aqueous, solvent or ultrasonic techniques. However, as an open-aperture device, precautions must be taken to avoid particulate or solvent contamination as a result of any manufacturing processes, including pick and place, reflow, cleaning, integration assembly and/or testing. Temporary covering of the aperture is allowed. To avoid degradation of accuracy or performance in the end product, care should be taken that any temporary covering and associated sealants/debris are thoroughly removed prior to any optical testing or final packaging.

## Storage Information

Moisture Sensitivity Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

### **Shelf Life**

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

**Floor Life**

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

**Rebaking Instructions**

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

## Ordering & Contact Information

**Figure 28:**  
**Ordering Information <sup>(1)</sup>**

| Ordering Code | Description   | Package    | Marking | Delivery Form | Delivery Quantity |
|---------------|---|------------|---------|---------------|-------------------|
| AS7220- BLGT  | Calibrated CCT and Lumen Maintenance Smart Lighting Manager | 20-pin LGA | AS7220  | Tape & Reel   | 2000 pcs/reel     |

**Note(s):**

1. Required companion serial flash memory (must be **ams** verified) is ordered from the flash memory supplier (e.g. AT25SF041-SSHD-B from Adesto Technologies).
2. AS7220 flash memory software is available from **ams**.

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|--------------------------|-----------------|--|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice  |
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## Revision Information

Initial production version 1-00

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