Product Document

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User Guide

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AS7058

Evaluation Kit

User Guide

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Content Guide

1 Introduction

The AS7058 is an integrated circuit (IC) designed to measure photoplethysmography (PPG), electrocardiogram (ECG), bioelectrical impedance (BioZ), and electrodermal activity (EDA).

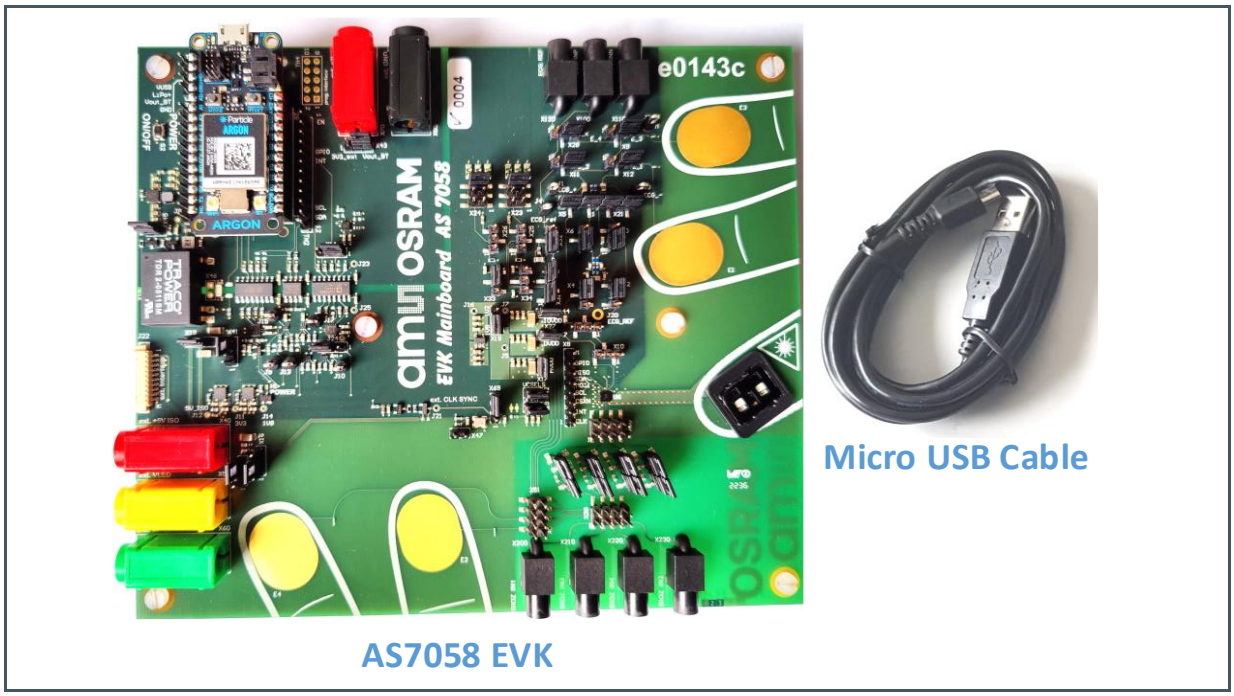
The AS7058 Evaluation Kit (EVK) is a platform to evaluate the functionalities of the AS7058 vital signs sensor. It has two components – the evaluation hardware (HW), and evaluation software (SW). The evaluation HW contains the AS7058 analog front-end (AFE), and all the necessary electronics on a printed circuit board (PCB) necessary to test the intended applications of the biosensor. The evaluation SW includes the necessary firmware (FW) and graphical user interface (GUI) to allow the user to connect the test HW to a personal computer (PC) and perform measurements.

This EVK user guide provides an overview of the evaluation HW and SW, including the installation and update of SW components, device configuration, and running measurements.

1.1 Kit Content

- AS7058 EVK
- Micro USB Cable

Figure 1:
AS7058 EVK



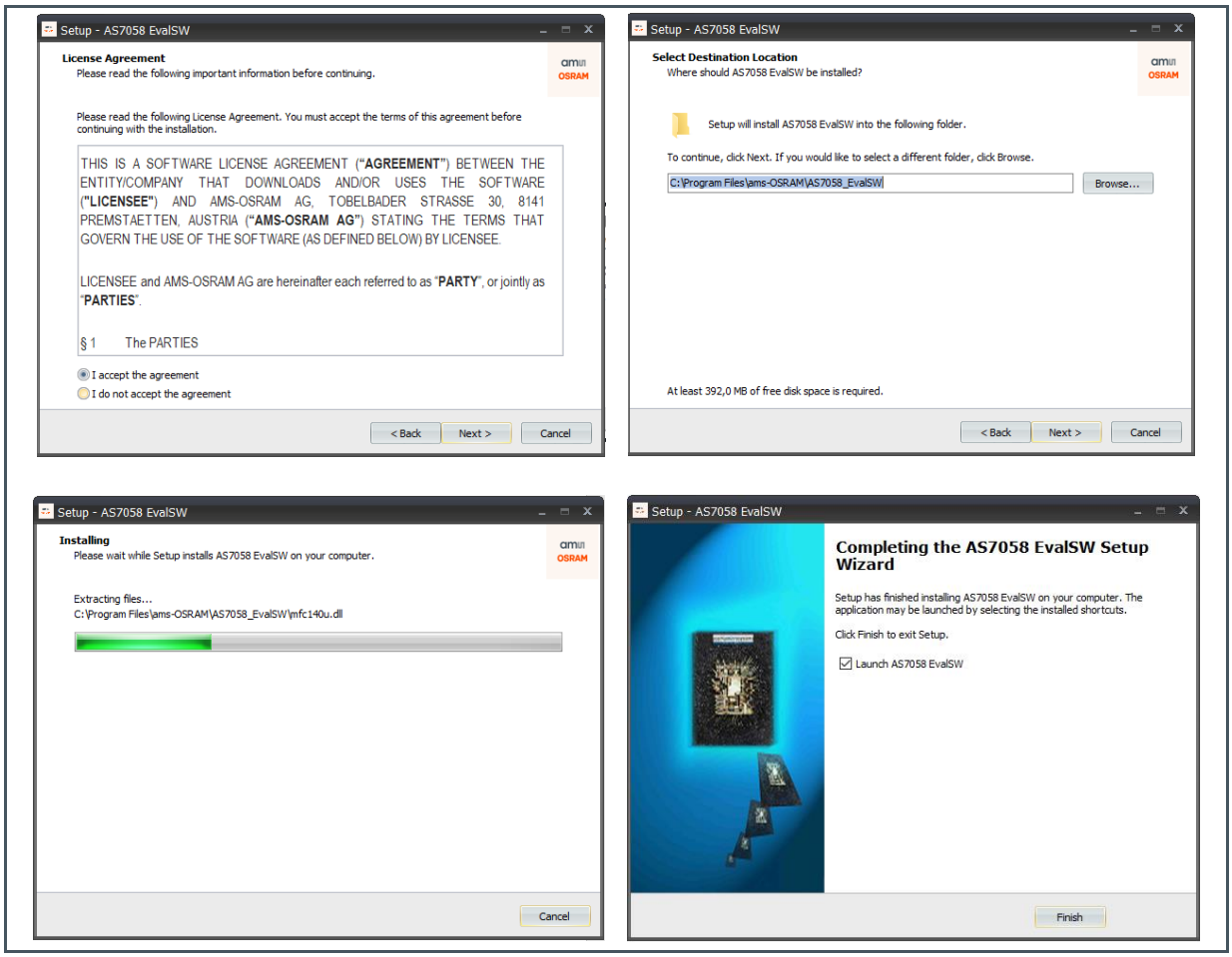
1.2 Ordering Information

Ordering Code	Description
990601269 / Q65113A5684	AS7058 Evaluation Kit

2 Getting Started

The latest version of the AS7058 EVK software is available for download (please contact the ams OSRAM support team for the download link). To install, start the installer executable and follow the instructions, as shown in Figure 2 (moving from left to right, top to bottom).

Figure 2:
AS7058 Evaluation Kit Software Installation



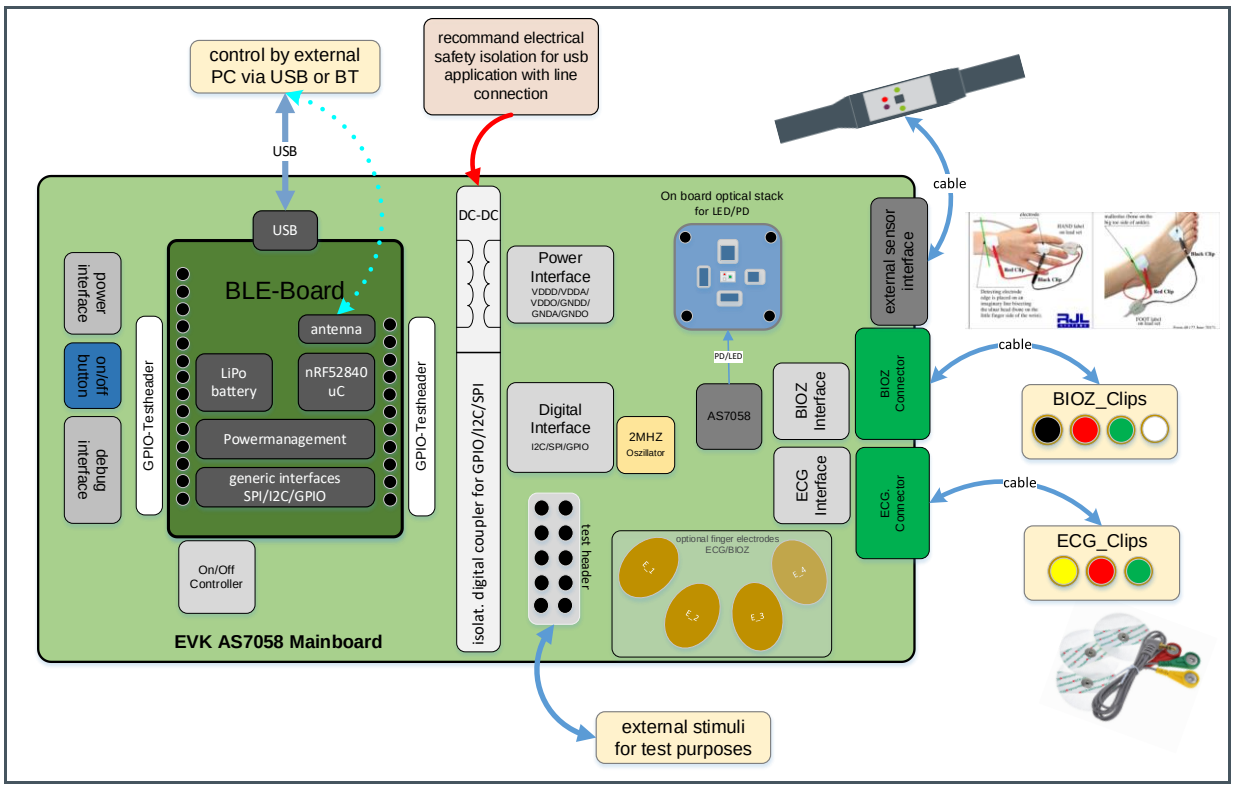
3 Hardware Description

The AS7058 EVK is designed as a system with two PCB boards for the full flexibility of the AS7058 vital sign chip. The first board is the BLE Board, and the second is the Mainboard. The BLE board is used for power management, connectivity, and signal post-processing. On the Mainboard, there are different optical LED/VCSEL/PD setups, electrodes for Electrocardiogram (ECG), electrodermal activity (EDA), and bioimpedance (BioZ), as well as an AS7058 sensor. The EVK has been developed such that more than one measurement concept can be used.

3.1 Hardware Architecture

The overview of the hardware architecture in Figure 3 visualizes the main electrical components of the EVK platform.

Figure 3:
Hardware Architecture



The AS7058 EVK contains all the circuitry necessary for linearization and accurate power detection. Figure 3 references the hardware architecture, and this chapter describes the various sections of the hardware present on the EVK.

3.1.1 BLE Module

The EVK contains a BLE module that can support the required functionality. This module is based on the Nordic Semiconductor's nRF52840-xxAA 2.4 GHz wireless system-on-chip (SoC) that includes a 2.4 GHz transceiver, a 32-bit ARM Cortex™-M4F CPU, a 1 MB flash memory, a 256 kB RAM, and analog and digital functions with integrated peripherals, and it also supports I²C operation at 100 kHz and 400 kHz.

3.1.2 Power Management

The AS7058 EVK offers a battery-powered operation option. It includes a USB rechargeable battery and power management.

Specification of the different power modes:

- **Powered by USB:** The USB and the battery in charging mode power the device.
- **Battery-operated:** A battery operates the device.

3.1.3 USB Interface

The USB connection has two different main tasks:

- Providing power to the system while simultaneously and independently charging the internal LiPo battery.
- Communicating with the AS7058 EVK device via a host application (e.g. PC GUI).

Use a standard micro USB cable.

3.1.4 Battery

The device can be powered with a single-cell LiPo (3.7 V) for wireless applications.

For example:

- Manufacturer: SHENZEN Pknergy ENERGY CO., LTD
- Provider: Eckstein-shop.de; ZB07004
- Order number: LIPO503035 500 mAh 3.7 V or similar type
- Features: Rated Voltage: 3.7V; nominal capacity: 500 mAh

The BLE module has an integrated LiPo charger that charges via USB when connected to a PC. The AS7058 EVK is powered via the USB interface or the LiPo without a USB connection.

3.1.5 Debug Interface

The board contains pin headers for debugging and evaluation.

- A pin header with access to all digital signals of the BTLE module is available.

- A pin header with access to the appropriate power supply.

3.1.6 On/Off Push-Button

An on/off push-button is used to control the supply voltage to the EVK board. This part includes a push-button input with independently programmable ON and OFF debounce times.

Functions of the push button include:

- Short press <1 s: Switches ON the device.
- Long press 1..2 s: Switches OFF the device.

3.1.7 Electrical Isolation

To avoid electrical hazards for users, the power management part and the user usage part of the mainboard are separated by electrical isolation. DC/DC converters and digital isolators are used as the isolation barriers.

3.1.8 Electrodes for ECG, EDA and BioZ

ECG, EDA, and BioZ measurements require electrical contacts between the body and the test hardware. Four gold-plated contact pads are provided on the EVK for contact with the fingers.

3.1.9 External ECG Connector

An external ECG signal (for instance, a signal generator) can be fed to the AS7058 EVK using the provided connectors. The jumper configuration must be adapted to direct such a signal to the AS7058.

3.1.10 External BioZ Connector

Similar to ECG, an external BioZ signal (for instance, a signal generator) can be fed to the AS7058 EVK using the provided connectors. The jumper configuration must be adapted to direct such a signal to the AS7058.

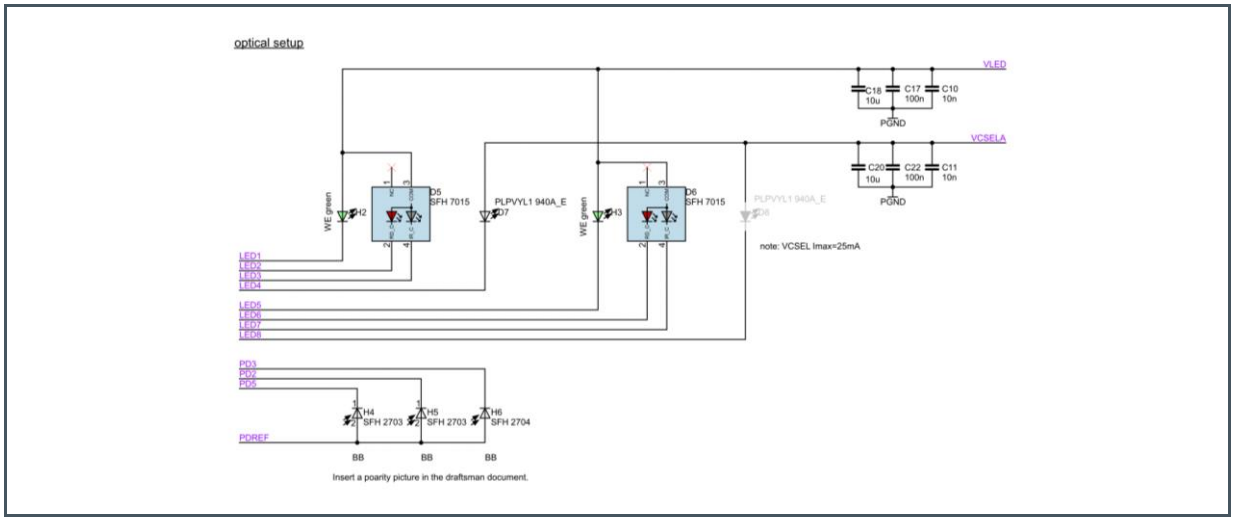
3.1.11 External Sensor Interface

The wired wristband can be connected to the AS7058 EVK mainboard via an external sensor interface. The corresponding connector is part of the AS7058 EVK, and the cable is part of the wired wristband.

3.1.12 Optical Component for PPG Measurements

The AS7058 EVK contains the necessary emitters and photodiodes to enable the user to perform PPG measurements in reflection mode on the finger. It includes two green LEDs (WE green) and two red IR LED modules (SFH 7015) as the main emitters for PPG measurements. The two broadband photodiodes (SFH 2703) are the two main detectors. There is also an IR VCSEL laser diode (PLPVYL1 940A) and another broadband photodiode (SFH 2703). These are used to demonstrate the proximity detection capability of the software algorithm.

Figure 4:
Optical Setup



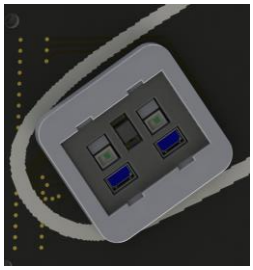
The optical setup of the AS7058 EVK contains the following:

- Only one mounted VCSEL part for laser safety reasons.
- Two mounted RED-IR modules.
- Two mounted green LEDs.
- Three installed photodiodes.

3.1.13 Optical Stack

An optical stack is used to protect the LEDs and photodiodes (PDs) and reduce crosstalk, allowing for optimized PPG signal acquisition.

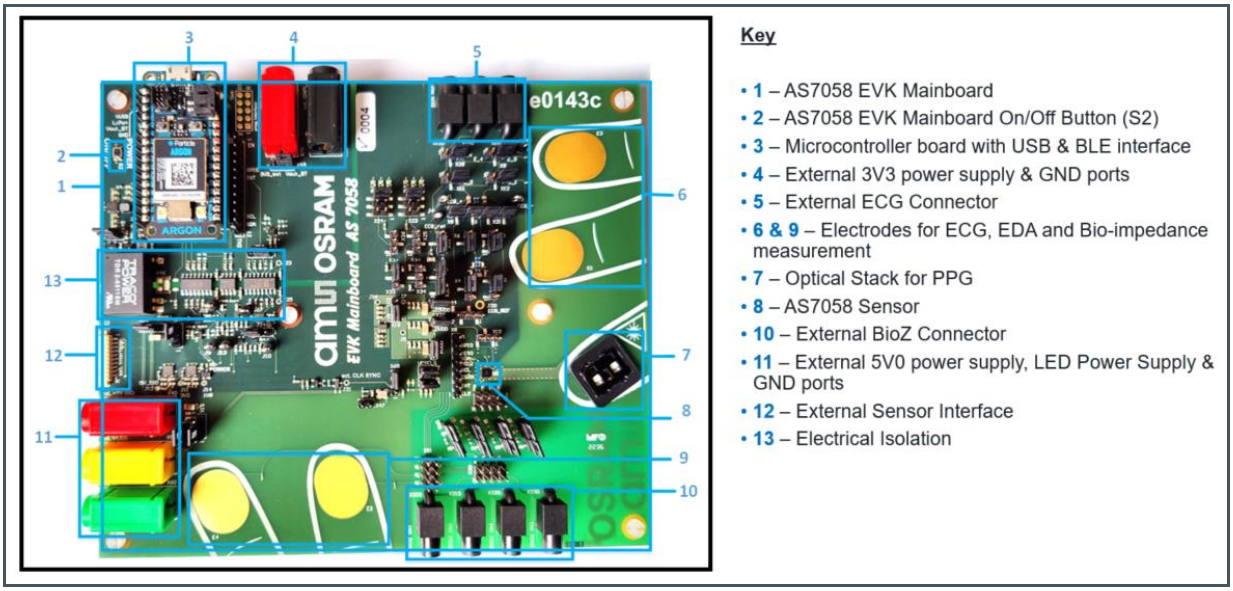
Figure 5:
Optical Stack



3.2 AS7058 Evaluation Kit (EVK)

The AS7058 EVK, as shown in Figure 6, is an evaluation platform for the AS7058 Biosensor Converting Unit. The board can be connected via the BLE or micro USB. The purpose of the EVK is to allow the user to get used to the device first and perform more advanced measurements, such as feeding external ECG and BioZ signals and evaluating the performance of the device. There are multiple pin headers and jumpers to sample the signal, measure current, etc. The evaluation kit consists of two boards - the BLE module and the AS7058 mainboard. Figure 6 shows the assembled AS7058 EVK with the mounted BLE module.

Figure 6:
Top View of the AS7058 EVK



3.2.1 AS7058 EVK Jumper Settings

Various jumpers are present on the AS7058 EVK. Various configurations can be achieved by appropriately connecting the jumper pins on the board. Care should be taken before placing these jumpers. The corresponding jumper connection is described in chapter 7.

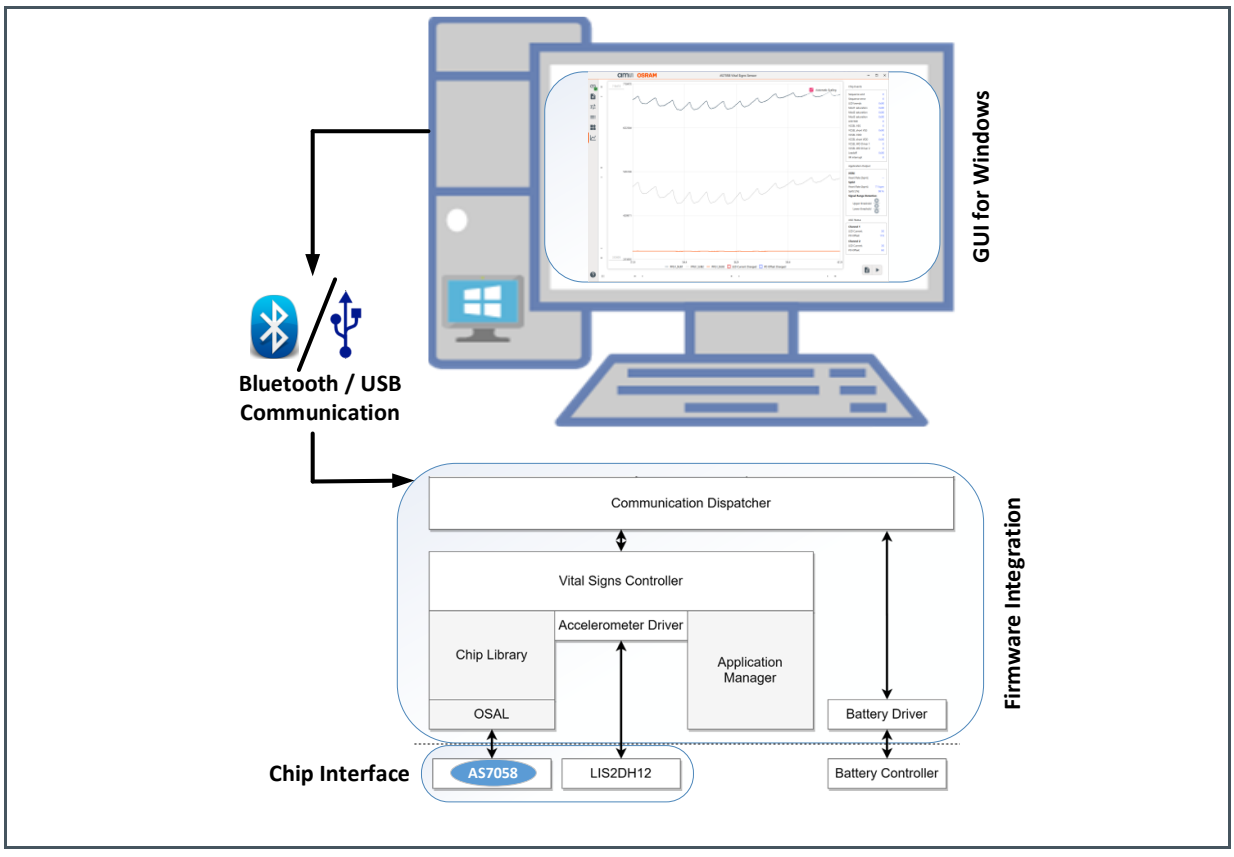
4 Software Description

The chapter aims to describe the essential workability of the AS7058 AFE. The software module provides software components, which enable a user to rapidly prototype their solutions.

4.1 Software Architecture

As shown in Figure 7, a Windows 10 operating system or a MAC OS system is needed to run the GUI application, which can connect to the BLE board/Firmware over USB or via the BLE (BT). The main components of the Firmware Integration are also shown.

Figure 7:
Software Architecture for the Windows GUI



4.2 Graphical User Interface

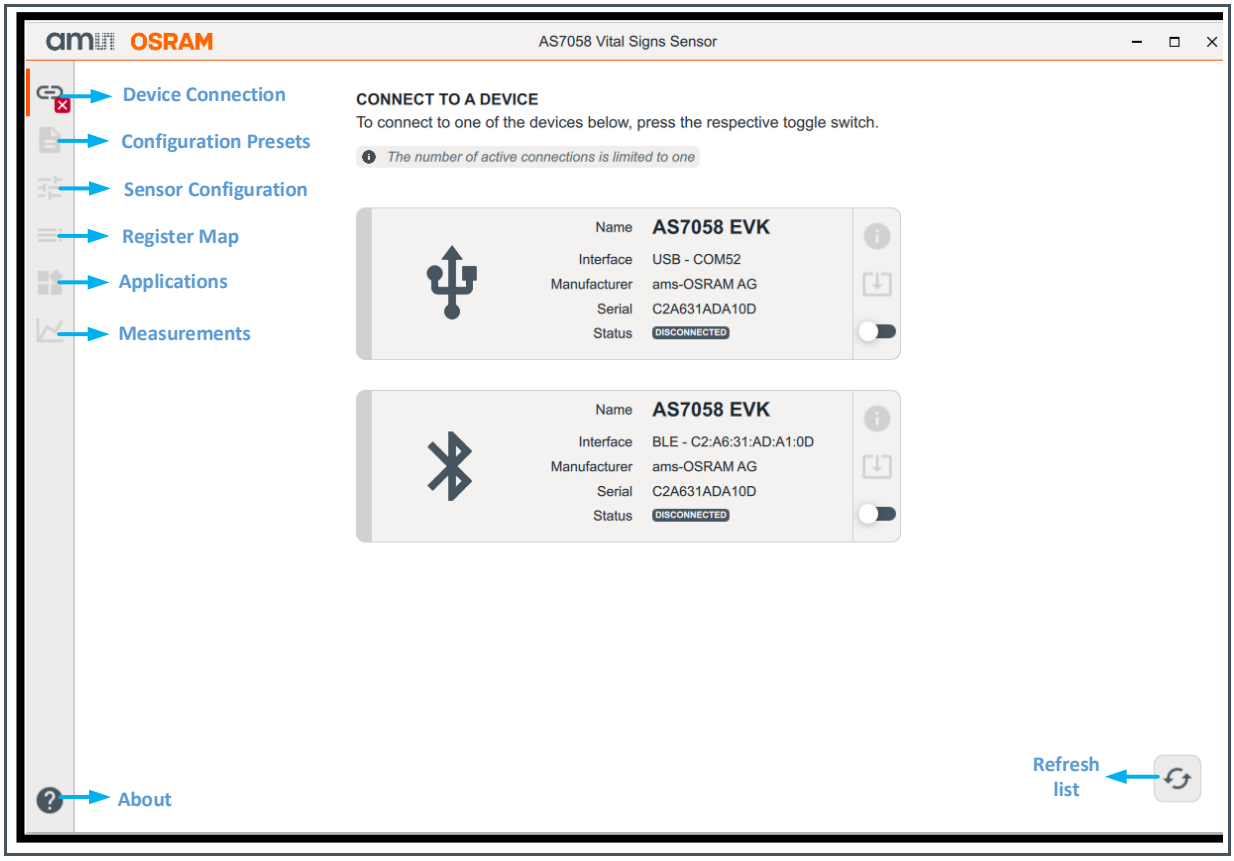
This section describes the Graphical User Interface (GUI) of the AS7058 Vital Sign Sensor application. The application is designed to be used with the AS7058 sensor evaluation kits.

4.2.1 Overview

The GUI consists of seven main segments highlighted in Figure 8.

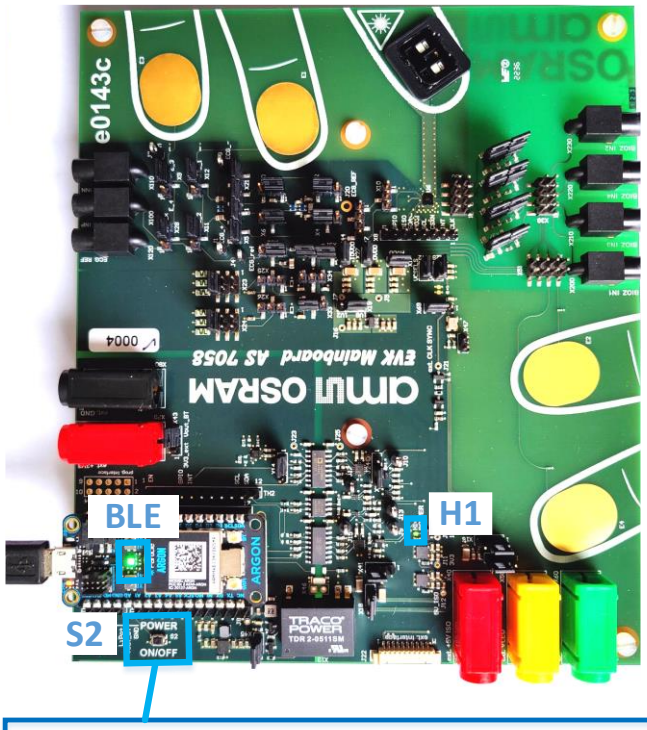
- **Device Connection:** To connect the AS7058 EVK to the software and show firmware information.
- **Configuration Presets:** A few configuration presets are provided to allow the user to quickly start using the device.
- **Sensor Configuration:** Adjusts the settings for individual parameters.
- **Register Map:** Displays the value of each register and can control the status of the sensor.
- **Applications:** Vital signs application-related parameters can be found in this tab.
- **Measurements:** This tab displays HRM, SpO_2, ECG, EDA and Bio-impedance readings, along with a graph of the ADC count.
- **About:** Shows, among others, information regarding the software and Python package version.
- **Refresh:** Press this button if Windows does not automatically detect the device, and wait for the board to be recognized.

Figure 8:
GUI Overview



When the GUI establishes communication with the AS7058 EVK, the green LED (USB connection) or blue LED (BLE connection) on the BLE module will switch on. The green LED (H1) on the mainboard also lights up, as shown in Figure 9.

Figure 9:
AS7058 EVK On/Off Button



5 Software Block Description

This AS7058 software consists of the following blocks, which are further described in this chapter along with their link with the register map if needed:

- Device Connection
- Configuration Presets
- Sensor Configurations
- Register Map
- Applications
- Measurements
- About

5.1 Device Connection

After launching the AS7058 EVK GUI, the “Device Connection” tab is displayed.

The GUI has two ways to communicate with the device:

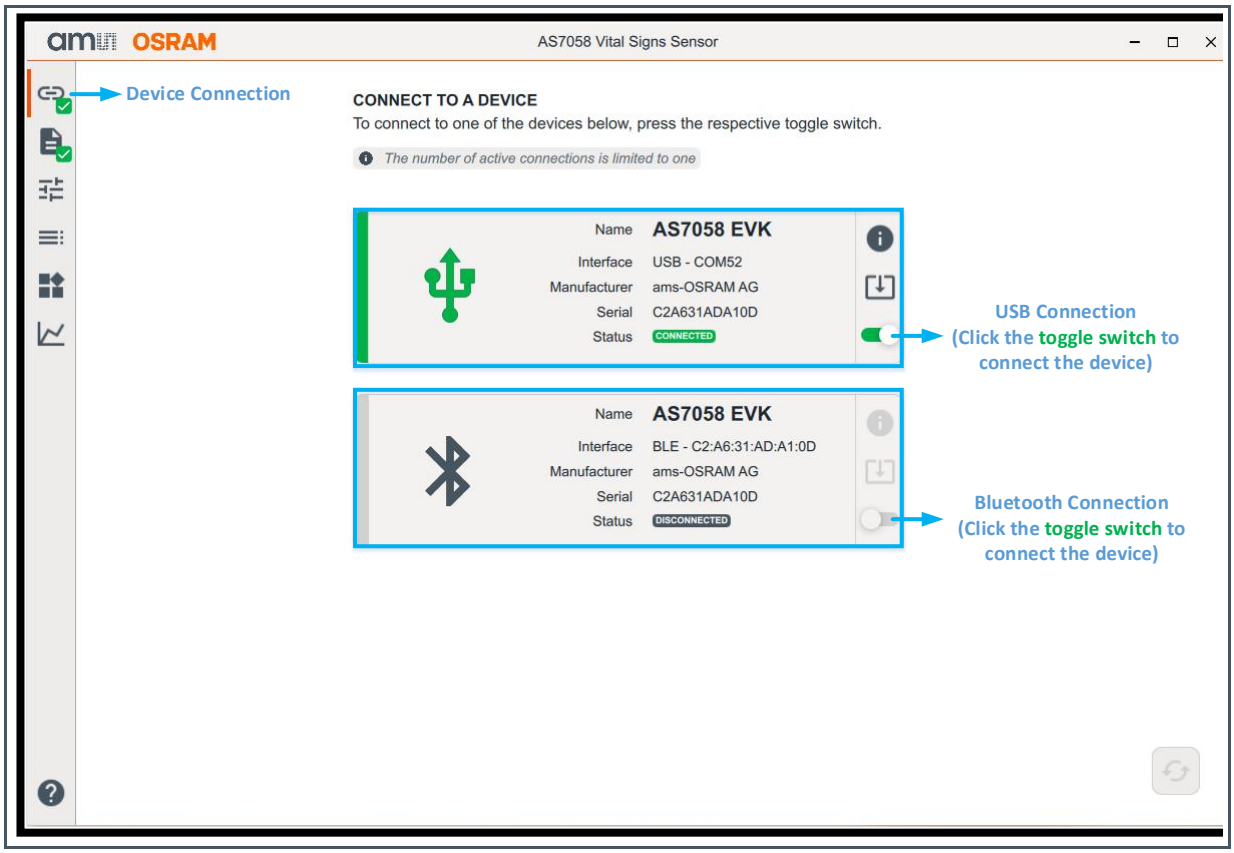
1. Wired connection via a micro USB connector.
2. Wireless connection via the BLE.

The GUI application is available on Windows-based PCs and macOS.

Information

The best performance for ECG and PPG can be achieved with a BTH connection and a power bank or external power supply connected to the USB.

Figure 10:
Device Connection



5.1.1 Connection

1. Connect the AS7058 EVK via the correct COM port or BLE number.
2. After it is successfully connected, the USB or BLE icon will change color to green.
3. The Green LED (USB connection) or Blue LED (BLE connection) on the microcontroller board starts to blink when a connection is established between the evaluation board and the GUI.

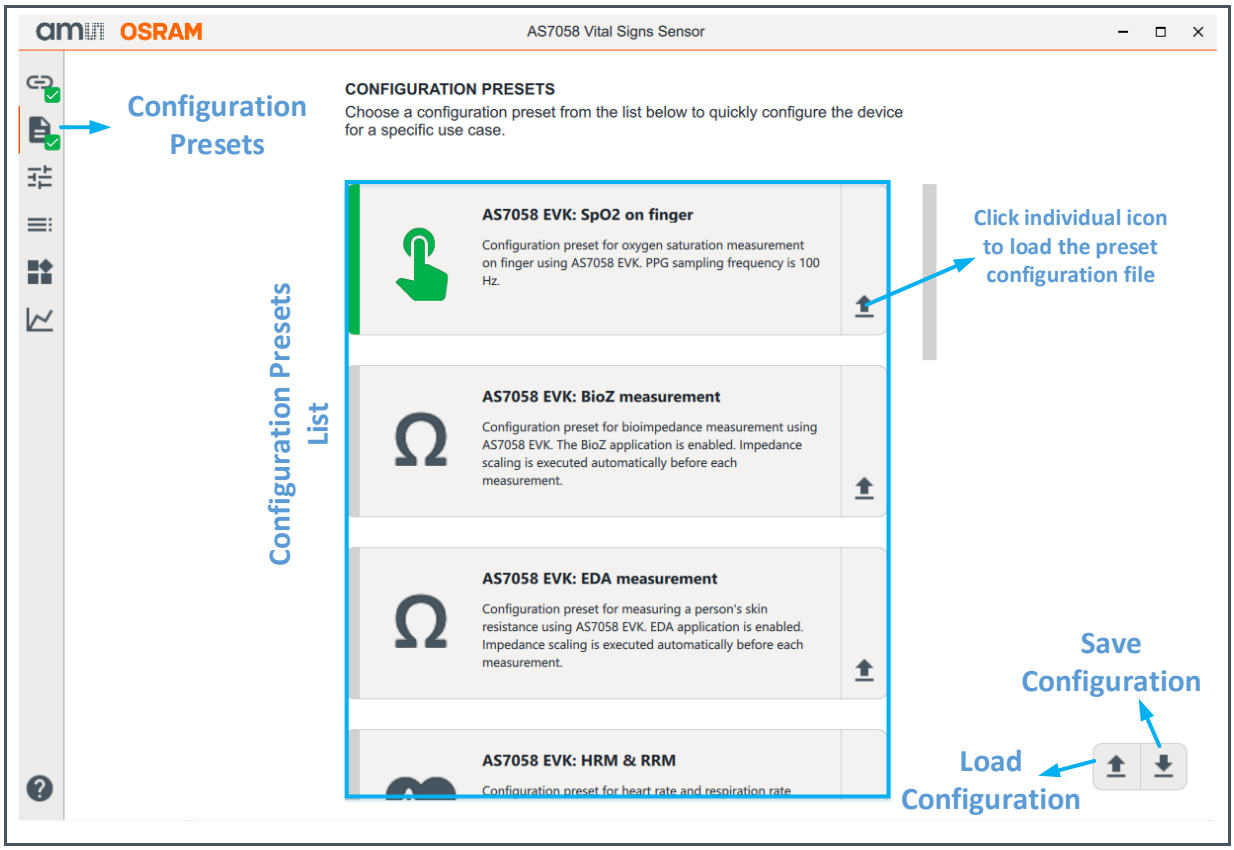
5.2 Configuration Presets

A few configuration presets are provided to help the user quickly start using the device. These presets can be chosen from the “Configuration Presets” Tab. Each file comes with a description that lets the user know which measurements could be done using them:

- **AS7058 EVK: SpO_2 on finger -** SpO_2 monitoring on the finger at a PPG sampling frequency of 100 Hz. The SpO_2 result is not calibrated.
- **AS7058 EVK: PPG & ECG -** This is a test configuration for simultaneous ECG and PPG measurements using the EVK.

- **AS7058 EVK: ECG 1 kHz -** For an ECG measurement on the finger using the EVK. The sampling frequency is 1 kHz, and the total gain is 128.
- **AS7058 EVK: ECG & Lead-off -** For an ECG measurement on the finger and lead-off detection using the AS7058 EVK.
- **AS7058 EVK: HRM & RRM -** Heart Rate and respiration rate monitoring on the finger at a PPG sampling frequency of 200 Hz, with PRV measurement enabled.
- **AS7058 EVK: EDA Measurement -** This is a configuration for measuring changes in a person's skin resistance.
- **AS7058 EVK: BioZ Measurement -** This is a configuration for measuring a person's body impedance with the AS7058 EVK.
- **AS7058 Wired-WB: HRM on wrist -** Heart Rate monitoring on the wrist when a wired wrist demo is connected.
- **AS7058 Wired-WB: SpO_2 on wrist -** SpO_2 measurement on the wrist when a wired wrist demo is connected.

Figure 11:
Configuration Tab Overview



The AS7058 configuration preset settings are located in the JSON configuration files of the latest release.

The individual settings of each of the AS7058 blocks can be found in a JSON file. Moreover, new settings can be saved in the JSON file.

By default, the configuration presets are located in the folder "*C:\Program Files\ams-OSRAM\AS7058_EvalSW\config-files*", or the user directory (depending on the installation folder), after the AS7058 software is installed.

Application-specific default preset configuration JSON files store almost all the register information for the AS7058 AFE that are easy to read, as shown in Figure 12.

Information

Please note that the configuration preset files can be changed with each new version of the GUI.

Figure 12:
Default Configuration Preset Files

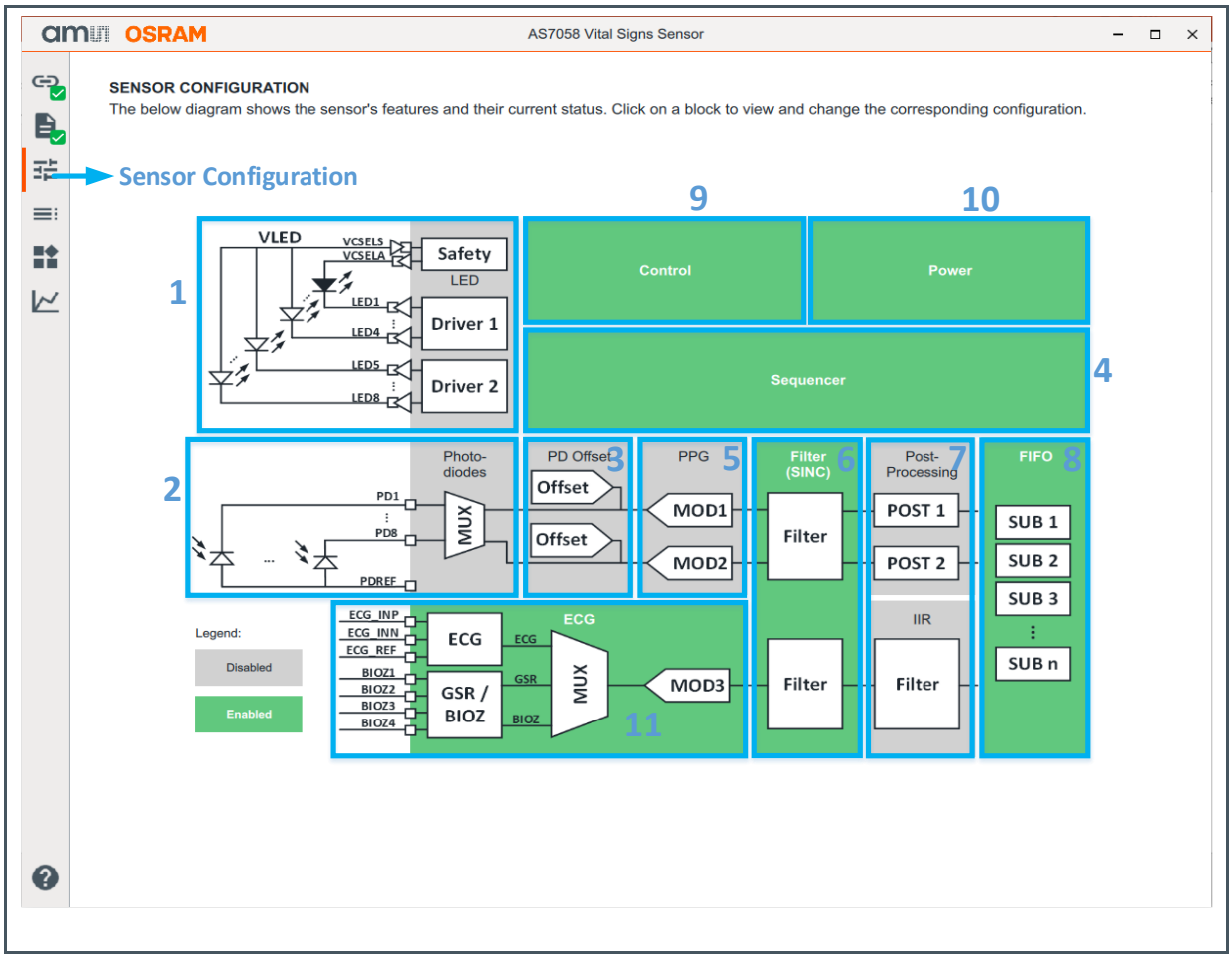
(1) All the register values displayed here are in hexadecimal. However, decimals are also supported (0-255), without quotation marks

5.3 Sensor Configurations

The device parameters can be configured in the "Sensor Configuration" tab. This tab presents the various functional blocks of the AS7058 as separate rectangular blocks. After choosing a configuration preset, the enabled blocks are highlighted in green (Figure 13) and the disabled blocks are shown in grey (Figure 13).

The parameters contained within each block can be monitored/modified by selecting the individual blocks.

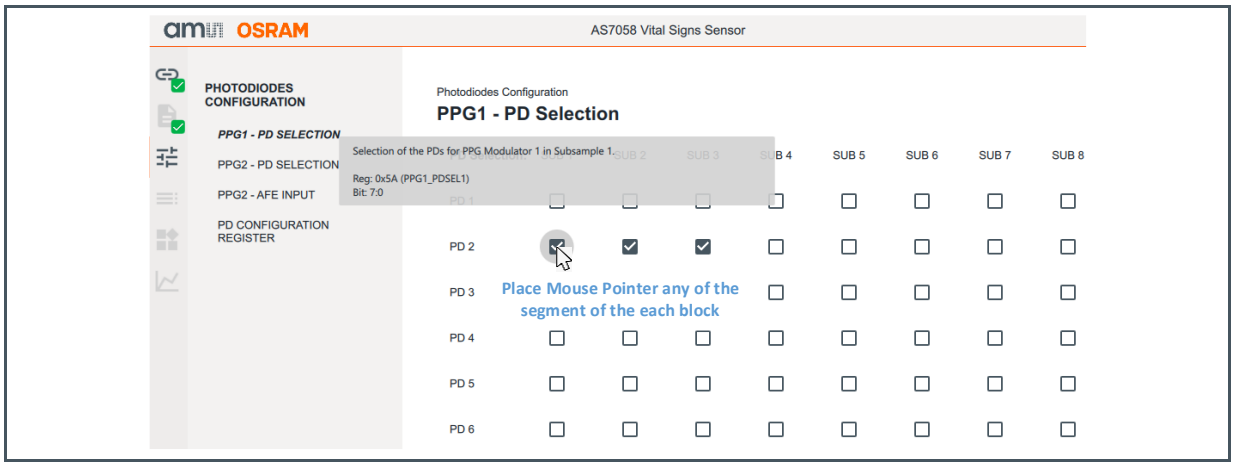
Figure 13:
Sensor Configuration



1 LED/VCSEL Driver Configuration
2 Photodiode Configuration
3 PD-Offset Configuration
4 Sequencer Configuration
5 Modulator Configuration
6 Filter Configuration
7 Post-Processing Configuration
8 FIFO Configuration
9 Control Configuration
10 Power Configuration
11 ECG & GSR/BIOZ Configuration

Each block provides a good starting point for gaining a thorough understanding of the AS7058. Each of the blocks is explained in the following chapters with a short register description. However, it is possible to observe the function of each block segment when the mouse pointer is placed on the respective part, as shown in Figure 14.

Figure 14:
Register Information



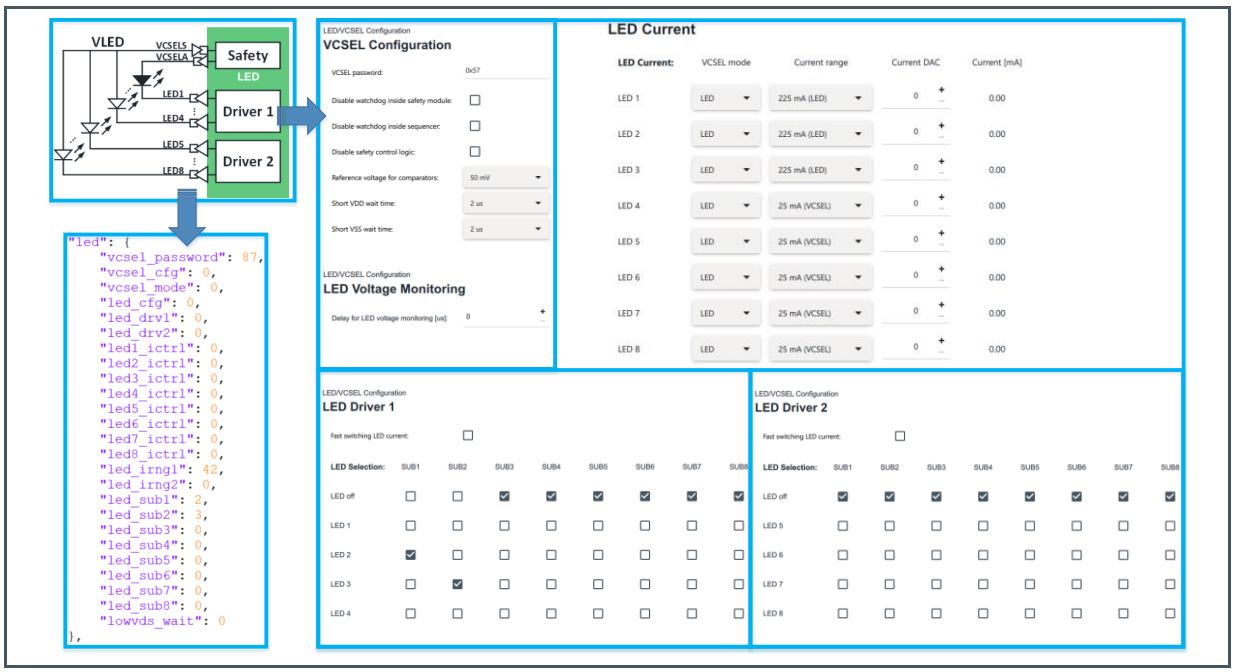
For further information, please refer to the following documents:

- See the ams OSRAM AS7058 datasheet for more information on each individual register.

5.3.1 LED/VCSEL Driver Configuration

The AS7058 contains two LED drivers. Each LED driver controls four LEDs.

Figure 15:
LED Driver Configuration



VCSEL Configuration for Safety Protection

Each driver has its VCSEL safety protection block, but the AS7058 has only one VCSEL power supply switch for both drivers.

The VCSEL safety protection provides functional monitoring of the VCSEL driver. The VCSEL safety protection controller generates the control signals for the VCSEL short circuit. The watchdog automatically starts if the VCSEL switches on. If a watchdog event occurs, the VCSEL and power switch will turn off.

The following parameter settings can be seen under the VCSEL Configuration, as shown in Figure 15:

- **VCSEL password:** The VCSEL password must be set to enable the VCSEL.
- **Disable watchdog inside safety module:** Enable/Disable the signal for the watchdog function inside the VCSEL safety function.
- **Disable watchdog inside sequencer:** Enable/Disable the watchdog for the VCSEL LED within the Sequencer. The VCSEL LED watchdog occurs at t > 1.0 ms.
- **Disable safety control logic evaluation**: Enable/Disable the safety control logic evaluation of the short to VSS/VDD signals.
- **Reference voltage for comparators:** Select the reference voltage (50 mV, 100 mV, 150 mV, and 200 mV) for the VDD short comparators.

- **Short VDD wait time:** The Short VDD wait time (2 µs, 4 µs, 8 µs, and 12 µs) defines the time between switching on short detection and the valid result. All VCSEL LEDs use the same time.
- **Short VSS wait time:** The Short VSS wait time (2 µs, 4 µs, 8 µs, and 12 µs) defines the time between switching on short detection and the valid result. All VCSEL LEDs use the same time.

LED Voltage Monitoring

This contains the following setting:

- **Delay for LED voltage monitoring [µs]:** The time between switching an LED on and the start of voltage monitoring. All the LEDs use the same time.

Equation 1:

$$Time = lowvds\_wait \times 1\mu s \quad | \text{Where, lowvds\_wait} = 0 \ldots 255$$

LED Current

The AS7058 has eight LED output pins, but only two of them can be used simultaneously. The default configuration of the eight output pins of the LED/VCSEL drivers is VCSEL.

The VCSEL safety protection is activated if the current range for the LED Driver is set to 25 mA.

In case of any error, the measurement should not be started or immediately stopped (e. g. watchdog event). An interrupt should be generated, and the status register should show the source of the error (a short to VSS, a short to VCSELS, or a watchdog event).

The drivers are implemented as a low-voltage current sink with a high-voltage output multiplexer. LED driver 1 controls the outputs LED1, LED2, LED3, and LED4. Driver 2 controls the outputs LED5, LED6, LED7, and LED8.

Each driver supports four output current ranges (25 mA for VCSEL, 150 mA, 225 mA, and 300 mA for LEDs).

The LED current can be adjusted in 255 steps in each range.

The driver contains a low output voltage detection. If the LED is on and the voltage at the LEDn pad is below the selected reference voltage, then the output low is set, and it is assumed that the expected output current is not reached. In the digital part, the output signal is synchronized with the current status of the LED on the signals to avoid false detections.

- **VCSEL mode (Reg: 0x42):** Select the normal LED or VCSEL mode for LED1 to LED8.
- **Current range (Reg: 0x4E & 0x4F):** Select a current range for LED1 (max 300 mA)/VCSEL1 (25 mA) to LED8 (max 300 mA)/VCSEL8 (25 mA).
- **Current DAC (Reg: 0x46 to 0x4D):** The LED/VCSEL current can also be programmed. The current can be adjusted in 255 steps.

Equation 2:

$$LED\ Current\ (mA) = Current\ DAC \times \frac{Current\ range\ (25mA, 150mA, 225mA, and\ 300mA)}{255}$$

LED Driver 1 & LED Driver 2

This block represents all the LED drivers. It contains all the sub-blocks necessary to provide the complete functionality for eight LED driver pins. Note that the LED/VCSEL current can be programmed for each sequence but not for each subsample.

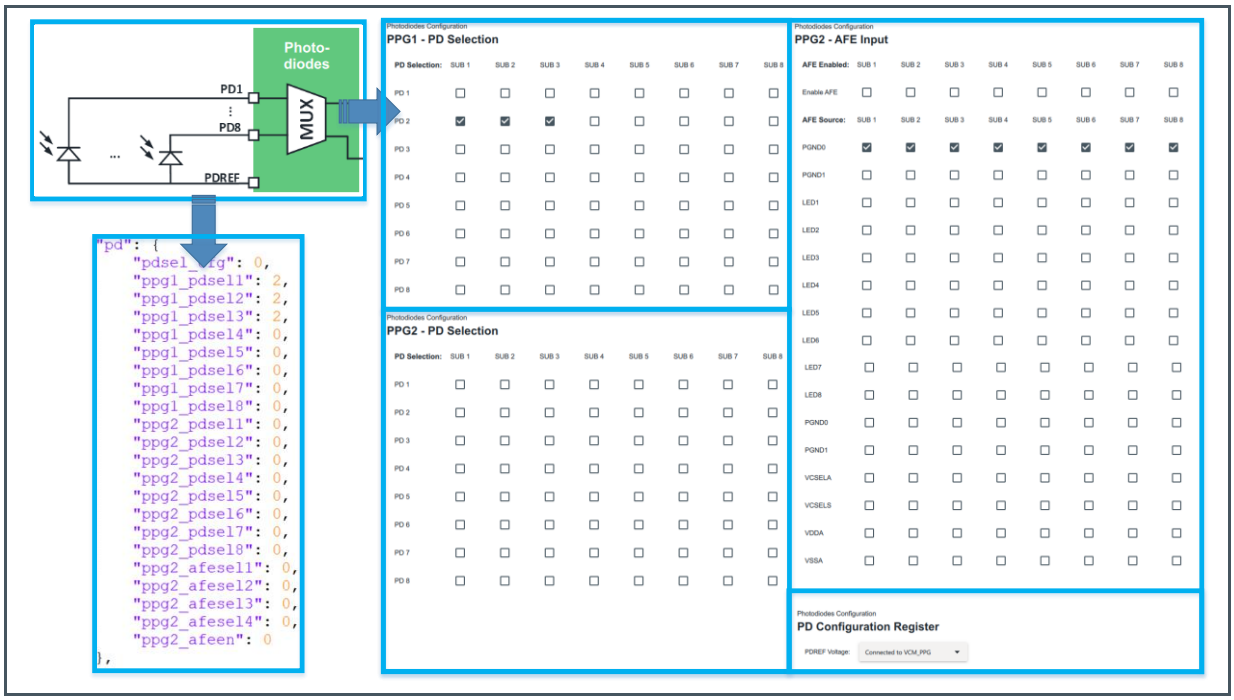
- **Fast switching LED current (Reg: 0x44 (LED Driver1) & 0x45 (LED Driver 2)):** Enables the fast switching of the LED current.
- **Internal BIAS current (Reg: 0x44 (LED Driver1) & 0x45 (LED Driver 2)):** Select an internal bias current for LED drivers 1 and 2. The values can be set, with zero as the lowest value and 15 as the highest value.
- **LED Selection (Reg: 0x51):** Only one register is used to select which LED, out of the available eight, should be connected to which subsample. Note that only one LED/VCSEL can be selected for every subsample for LED drivers 1 and 2.

5.3.2 Photodiode Configuration

The PPG signal acquisition chain has a flexible input multiplexer per channel that can be connected independently to different combinations of external photodiodes.

The PPG front-end consists of three main functional blocks: photodiode (PD) selection, PD offset, and the PPG ADC. The PD selection supports up to eight different photodiodes. The photodiodes are connected via a multiplexer to the PPG ADC. To minimize daylight impacts, the photodiode input currents can be compensated by the PD offset. After amplifying and converting the PD currents, the digital PD output signals pass to the digital PPG filter inside the digital block of the AS7058.

Figure 16:
Photodiode Configuration



PPG1 & PPG2 – PD Selection

PD selection is performed by connecting the external photodiodes (PD1, PD2, PD3, PD4, PD5, PD6, PD7, and PD8) to the internal PPG channels (PPG1, PPG2). Sixteen registers are used to select which PD, out of the available eight, should be connected to which subsample and modulator. Each PD could be connected to any subsample inside the sequence. If two or all eight PDs are connected to MOD1 or MOD2, they must be interleaved in time, since, at one time, only one MOD can be connected to a PD. However, two different PDs can be simultaneously connected to different MODs. For instance, PD1 is connected to MOD2, and PD2 can be applied to MOD1 simultaneously.

- **PD Selection (Reg: 0x51 to 0x61 (PPG1)):** Selection of the PDs for PPG modulator 1 in subsample 1 to 8.
- **PD Selection (Reg: 0x62 to 0x69 (PPG2)):** Selection of the PDs for PPG modulator 2 in subsample 1 to 8.

PPG2 – AFE Input

PPG2/MOD2 can be connected to external voltages instead of the PDs. Note that MOD1 is configured to be connected only to PDs and not any external voltage, while MOD2 can be configured to be connected to either PDs or external voltages.

- **AFE Enabled (Reg: 0x6E):** Enable the AFE Input for PPG modulator 2 in subsamples 1 to 8.

- **AFE Source (Reg: 0x6A to 0x6D):** Select the AFE Input for PPG Modulator 2 in subsamples 1 to 8.

PD Configuration Register

The PDREF (photodiode reference voltage) can be selected between VSSA (analog ground) and VCM_PPG (common mode voltage for PPG channel). When PDREF_SEL (selection of PDREF voltage) is logical “1”, then PDREF is connected to VSSA. When PDREF_SEL is logical “0”, then PDREF is connected to VCM_PPG, if the signal PPG1_EN (enable PPG1 channel) or PPG2_EN (enable PPG2 channel) is digital high (otherwise, PDREF is connected to VSSA).

- **PDREF Voltage (Reg: 0x59):** Selection of the PDREF voltage.

5.3.3 PD-Offset Configuration

The AS7058 offers an Advanced Automatic Offset Control (AAOC) to balance and reduce ambient light currents automatically. This chapter describes the configuration of this feature.

Figure 17:
PD-Offset Configuration

PPG1 & PPG2 – PD Offset

PD Offset is part of the PPG ADC. It can be configured by the digital register or used as a part of the integrated AAOC loop. The PD Offset DAC consists of 8 bits. Apart from the configuration, before or after a measurement cycle, it is also possible to adjust the PD offset registers during a measurement by an external microcontroller.

- **PPG1 – PD Offset (Reg: 0x7A to 0x81):** PD Offset for PPG modulator 1 in subsamples 1 to 8.
- **PPG2 – PD Offset (Reg: 0x82 to 0x89):** PD Offset for PPG modulator 2 in subsamples 1 to 8.

Offset Compensation When LED is off

PD offset configuration applies to Double and Triple sampling. Double measurement measures two values within a subsample, and the Triple measurement function measures three values within a subsample.

- **Disable using LED on offset (Reg: 0x8B):** Disables the use of the common PD Offset for all subsamples during LEDoff sampling. If the common PD Offset is disabled, the PD Offset from LEDon sampling will also be used for LEDoff sampling.
- **Fixed PD Offset for all subsamples (Reg: 0x8A):** If the common PD Offset is not disabled, the PD Offset will be used during LEDOff sampling. This means that when using a common PD Offset set to the value 0, no PDOffset will be used for LEDOff sampling.

SAR Configuration

The AS7058 offers the ability to use an Advanced Automatic Offset Control (AAOC) measurement technique to reduce data loss when measuring with motion or widely varying ambient light conditions. If the AAOC feature is enabled, the timing will change.

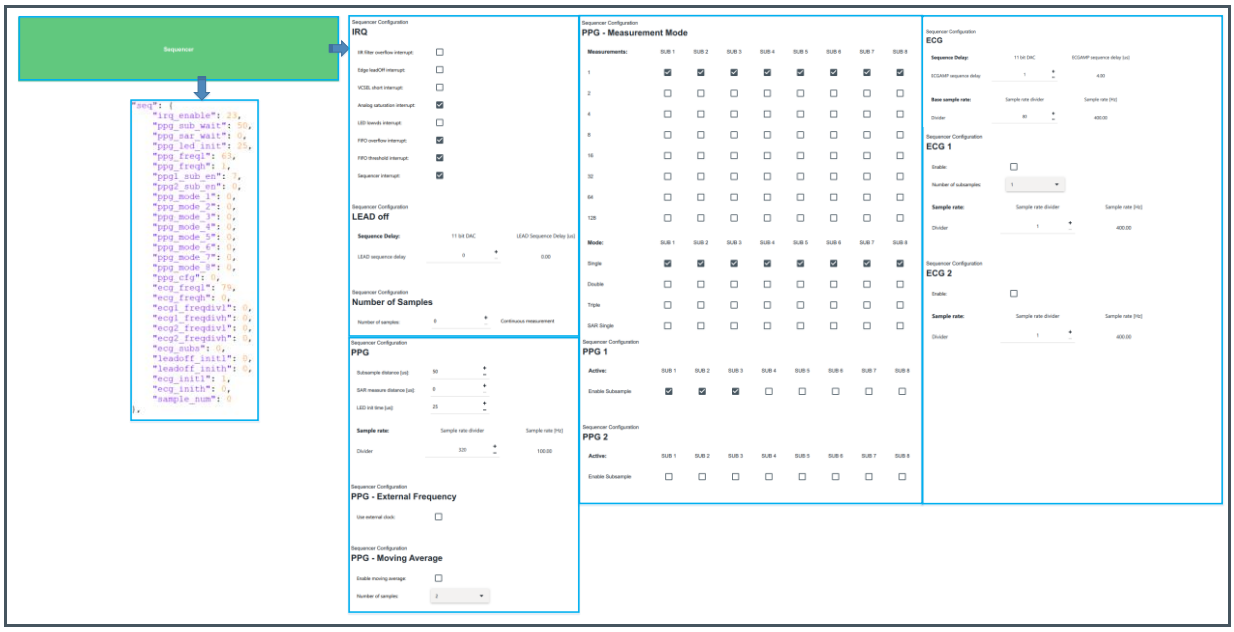
The SAR single sample function measures the value within one subsample after automatically calculating the upper four bits of the PD offset. This feature aims for advanced automatic offset control. It sets the PD Offset DAC immediately before the measurement. The FIFO stores the AAOC data and the ADC results.

- **Target ADC (Reg: 0x8C):** Select the target ADC for SAR single measurement.
- **Disable SAR for the following range (Reg: 0x8D):** A particular SAR range will be disabled.
- **Disabled SAR range (Reg: 0x8D):** Select the disabled SAR range for SAR single measurement. If the SAR following range is activated, the AAOC will only update the PD Offset value if the new sample is outside this range. This feature can minimize the number of PD Offset current switching.
- **PPG1 - SAR Configuration (Reg: 0x8E):** This feature enables the use of the last estimated PD offset value from a single SAR sample for other subsamples. For example, if SUB1 is configured for SAR Single, the estimated PD offset value from that sample could be reused for SUB2 if “Use SAR Value” is enabled for SUB2. AAOC is only activated for the subsamples configured to use SAR sampling mode in the sequencer section.
- **PPG2 - SAR Configuration (Reg: 0x8F):** This feature enables the use of the last estimated PD offset value from a single SAR sample for other subsamples. For example, if SUB1 is configured for SAR Single, the estimated PD offset value from that sample could be reused for SUB2 if “Use SAR Value” is enabled for SUB2. AAOC is only activated for the subsamples configured to use SAR sampling mode in the sequencer section.

5.3.4 Sequence Configuration

The sequencer controls all the timing and signals required to carry out the measurements. PPG and ECG have independently programmable sample frequencies.

Figure 18:
Sequencer Configuration



IRQ

A high active interrupt can be programmed for continuous data acquisition. With IRQ_ENABLE, the sources for generating an interrupt are enabled.

- **IIR filter overflow interrupt (Reg: 0x95):** Enable IIR filter overflow interrupt.
- **Edge leadOff interrupt (Reg: 0x95):** Enable edge leadOff interrupt.
- **VCSEL short interrupt (Reg: 0x95):** Enable VCSEL short to VDD/VSS or VCSEL watchdog detection.
- **Analog saturation interrupt (Reg: 0x95):** Enable analog saturation interrupt.
- **LED lowvds interrupt (Reg: 0x95):** Enable LED lowvds interrupt.
- **FIFO overflow interrupt (Reg: 0x95):** Enable FIFO overflow interrupt.
- **FIFO threshold interrupt (Reg: 0x95):** Enable FIFO threshold interrupt. When FIFO is almost full, FIFO_LEVEL > FIFO_THRESHOLD.
- **Sequencer interrupt (Reg: 0x95):** Enable sequencer interrupt.

LEAD off

When the skin does not touch the electrode, it is called leadoff. The ECG_leadoff circuit is a differential DAC current intended to apply a stimulus to the inputs. Each leadoff data is compared with the leadoff threshold. If it is larger than the leadoff threshold, the output signal, “leadoff”, will be high.

- **LEAD sequence delay (Reg: 0xAE & 0xAD):** This programs the delay from the beginning of each LEAD sequence to the beginning of the LEAD sample measurement. If the decimal value of this register is N, then the delay is N*4µs.

Number of Samples

- **Sample Number (Reg: 0x81):** Number of samples for the active channel. If seq_sample = 0, the sequencer runs continuously.

PPG

Simultaneous PPG signal acquisition is possible with the AS7058. To do this, two PPG signals must be activated. The PPG acquisition channels run in parallel and operate with the same sampling frequency. For this, the sampling frequency and the frequency divider for the partial sequences must be programmed.

Each data sample is constructed from a set of individual measurements called subsamples. The sequencer supports eight subsamples per PPG channel. Subsample numbers can be programmed in the sequence block.

The AS7058 provides a very flexible setting for different ambient light removal options: single measurement, double measurement, and triple measurement. Both modulators work with the same measurement method when the subsample is enabled.

- **Subsample distance [µs] (Reg: 0x96):** Select the distance between the subsamples.

Equation 3:

$$Distance\ between\ subsamples = N \times 1\mu s \quad | \text{Where, N} = 0...255$$

- **SAR measure distance [µs] (Reg: 0x97):** Select the distance between the SAR measurements.

Equation 4:

$$SAR\ measurement\ distance = N \times 1\mu s \quad | \text{Where, N} = 0...255$$

- **LED init time [µs] (Reg: 0x98):** Setup time after turning on the LEDs.

Equation 5:

$$LED\ setup\ time = N \times 1\mu s \quad | \text{Where, N} = 0...255$$

- **Sample rate Divider (Reg: 0x9A & Reg: 0x99):** Configuration of the PPG sequence sample period. The Divider for calculating the sample rate (Hz) for the sequence configuration is shown below in Equation 6.

Equation 6:

$$Sample\ Rate = \frac{1}{(Divider \times 31.25\mu s)} \times 10^6 \qquad | \text{Where, Divider} = [1 \ldots 2^{16}]$$

> The divider value is configured as a 16-bit value [0… (2^16-1)]

PPG – External Frequency

When using an external frequency, the frequency register of the PPG and ECG will be disabled. A rising edge on an external clock pin starts the measurement of one sample.

- **Use external clock (Reg: 0xA5):** Activate the external clock and disable the PPG and ECG set frequencies.

PPG – Moving Average

A post-processing moving average filter has been implemented to enhance the quality of a signal and reduce noise levels.

- **Enable moving average (Reg: 0xA5):** Enable the moving average for the PPG.
- **Number of samples (Reg: 0xA5):** Select the value (2, 4, 8, and 16) of the moving average for the PPG.

PPG – Measurement Mode (Reg: 0x9D & 0xA4):

Select the number of measurements (1, 2, 4, 8, 16, 32, 64, and 128) for PPG subsamples 1 to 8.

The Single measurement method is intended for sampling the PPG signals without digital ambient light canceling, whereby raw PPG signals (LEDon) and ambient light signals (LEDoff) can be measured.

Two measurement methods are available for digitally suppressing ambient light - Double and Triple measurement.

The SAR single measurement samples the value within one subsample after the automatic calculation of the upper four bits of the PD-Offset. Due to the fast response time of SAR sampling (AAOC), it is possible to measure PPG signals in the event of movement or rapidly changing ambient light without signal loss. Select “Measure mode” for PPG subsamples 1 to 8.

PPG1 & PPG2

The PPG contains PPG1 and PPG2, based on the two modulators that can be operated at the same frequency. For this, the sampling frequency and divider must be programmed. Each sample consists of two PPGs with eight subsamples.

- **Enable Subsample (Reg: 0x9B & 0x9C):** Enable the subsample for PPG modulators 1 and 2.

ECG

Simultaneous ECG signal acquisition is possible with the AS7058. To do this, the ECG ADC channel can be configured as two sequences - seq 1 and seq 2. The ECG acquisition channels run in parallel and operate with different sampling frequencies. For this, the sampling frequency and the two frequency dividers for the partial sequences must be programmed.

- **Sequence Delay:**
  - **ECGAMP sequence delay (Reg: 0xB0 & 0xAF):** Delay from the beginning of the ECGAMP sample measurement.
- **Divider (Reg: 0xA6 & Reg: 0xA7):** Configuration of the ECG sequence sample period. The Divider for calculating the sample rate (Hz) for the sequence configuration is shown below in Equation 7.

Equation 7:

$$Sample\ Rate = \frac{1}{(Divider \times 31.25\mu s)} \times 10^6 \qquad | \text{Where, Divider} = [1...2^{16}]$$

> The divider value is configured as a 16-bit value [0… (2^16-1)]

ECG1

- **Enable ECG 1 (Reg: 0xAC):** Enables ECG1.
- **Number of subsamples (Reg: 0xAC):** Select the number of subsamples (1 and 2) for ECG1.
- **Sample rate Divider (Reg: 0xA8 & Reg: 0xA9):** This gives the configuration of the ECG1 sample period. The divider for calculating the sample rate (Hz) for the ECG1 configuration is shown below in Equation 8.

Equation 8:

$$Sample\ Rate = \frac{Base\ Sample\ Rate}{Divider} \qquad | \text{Where, Divider} = [1...2^{16}]$$

> The divider value is configured as a 16-bit value [0… (2^16-1)]

ECG2

- **Enable ECG 2 (Reg: 0xAC):** Enables ECG2
- **Sample rate Divider (Reg: 0xAA & Reg: 0xAB):** This gives the configuration of the ECG 2 sample period. The divider for calculating the sample rate (Hz) for the ECG 2 configuration is shown below in Equation 9.

Equation 9:

$$Sample\ Rate = \frac{Base\ Sample\ Rate}{Divider} \quad | \text{ Where, Divider} = [1 \ldots 2^{16}]$$

- The divider value is configured as a 16-bit value [0… (2^16-1)]

5.3.5 Modulator Configuration

The PPG ADCs, also known as Modulators, are currently input ADCs and could be configured in the Modulator configuration.

Figure 19:
Modulator Configuration

The PPG ADCs are input current 20-bit ADCs controlled by the sequencer for each time slot. The reference DAC full-scale range and the ADC Input Full-Scale Range of PDs have to be programmed to get a suitable PPG ADC. A stable operation is enabled by proper operating conditions from a DAC with bipolar references. The modulator is used to scale the reference DAC current.

PPG Modulator

The PPG signal acquisition channel consists of two low-power, multichannel, simultaneous-sampling, current-mode 20-bit ADC conversions. PPGMOD_CFG registers are designed to enable the PPG block, support Full-Scale Range adjustment, and enable special configurable operation modes. Since there are two PPG channels, there are two sets of configuration registers.

- **PPGMOD_CFG1 & PPGMOD_CFG2 (Reg: 0x37 & Reg: 0x38):** The PPGMOD_CFG1 and PPGMOD_CFG2 registers control the bias current for MOD1 and MOD2 circuit blocks. This 2-bit register can be set to 1, which enables the reduction of the bias current.
- **PPG modulator reset delay (Reg: 0x39):** Reset time for all the modulators. Internal reset process time = N * MOD_CLK.
- **Clock frequency MOD_CLK (Reg: 0x39):**
  - **MOD_CLK (Modulator clock frequency)** – The frequencies 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz can be set. With a reduction of the Modulator clock frequency, the converting time will be increased. The power consumption of the AS7058 will also increase.

PPG Modulator 1

- **Enable Modulator 1 (Reg: 0x3A):** Enables modulator 1.
- **Full scale range (Reg: 0x3A & Reg: 0x3C):** The adjustable gain/full-scale range can be chosen from one of seven input current dynamic range settings (1 µA, 2 µA, 4 µA, 8 µA, 16 µA, 32 µA, or 64 µA) with each channel separated.
- **Multiplex IOSDAC1 (Reg: 0x39 & Reg: 0x3B):** Select the Multiplex of IOSDAC1 to modulator 1 for the calibration. “Multiplex IOSDAC1 to MOD2” acts like the PD current source, and “IOSDAC1 connected MOD1” is used as the offset correction.
- **Offset DAC full scale range (Reg: 0x3B):** This is used to set the IOS DAC Full-Scale current. Setting the three bits to 111, enables the IOS DAC current up to 128 µA.
- **ADC (current reference DAC) scale factor (Reg: 0x3B):** Current reference DAC IRN (Negative reference current)/IRNmax scale factor.

PPG Modulator 2

Enable Modulator 2 (Reg: 0x3D): Enables modulator 2.

Full scale range (Reg: 0x3D & Reg: 0x3F): The adjustable gain/full-scale range can be chosen from one of seven input current dynamic range settings (1 µA, 2 µA, 4 µA, 8 µA, 16 µA, 32 µA, or 64 µA) with each channel separated.

Multiplex IOSDAC2 (Reg: 0x3D & Reg: 0x3E): Select the Multiplex of IOSDAC1 to modulator 1 for the calibration. “Multiplex IOSDAC2 to MOD1” acts like the PD current source, and “IOSDAC2 connected MOD1” is used as the offset correction.

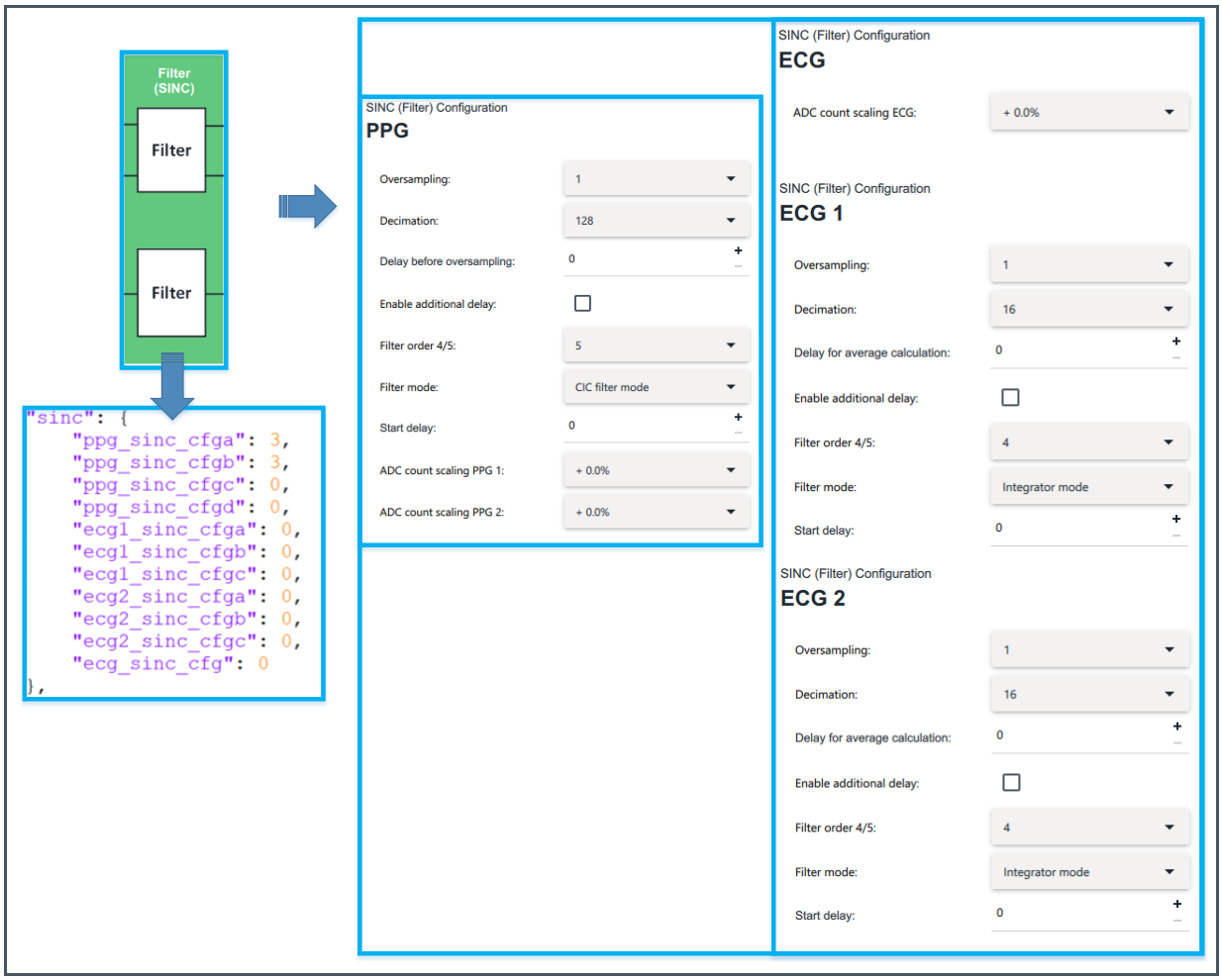
Offset DAC full scale range (Reg: 0x3E): This is used to set the IOS DAC Full-Scale current. Setting the three bits to 111 enables the IOS DAC current up to 128 µA.

ADC (current reference DAC) scale factor (Reg: 0x3E): Current reference DAC IRN (Negative reference current)/IRNmax scale factor.

5.3.6 Filter Configuration

The AS7058 offers different filter modes, which are accessible on that settings page.

Figure 20:
Filter Configuration



The digital filter can be flexibly configured according to filter type, filter order, and filter decimation rate. The SINC Filter is implemented as a CIC filter. It can be configured as a fourth or fifth order Filter. The filter can also run in an integrator-only mode.

PPG

The PPG SINC filter is a type of signal processing that removes all unwanted frequencies above a certain cutoff frequency without affecting the lower frequency. The PPG digital filter's configuration

results in a different ADC conversion time (ADC) and the effective number of bits of the ADC (ENOBs).

- **Decimation (Reg: 0x6F):** Select the value for the decimation of the SINC filter to lower the sampling frequency of the signal. During the A/D conversion process, the decimation filter can reduce the noise, maintain the signal power, and improve the SNR value.
- **Filter order 4/5 (Reg: 0x70):** The SINC filter can be configured as a fourth or fifth order filter.
- **Filter mode (Reg: 0x70):** The SINC filter is implemented as a CIC filter or can also run in integrator mode.
- **Start delay (Reg: 0x71):** Select PPG start delay.
- **ADC count scaling PPG 1 (Reg: 0x72):** Enlargement of the measured value of the SINC filter PPG1.
- **ADC count scaling PPG 2 (Reg: 0x72):** Enlargement of the measured value of the SINC filter PPG2.

ECG

The ECG SINC filter is a type of signal processing that removes all unwanted frequencies above a certain cutoff frequency without affecting the lower frequency. The ECG digital filter's configuration results in a different ADC conversion time (ADC) and the effective number of bits of the ADC (ENOBs).

- **ADC count scaling ECG (Reg: 0x79):** This is a SINC filter ADC count scaling that increases the ADC counts by the selected value for ECG. The fractions used for summation within the scaling are 50%, 25%, 12.5% & 6.25%.

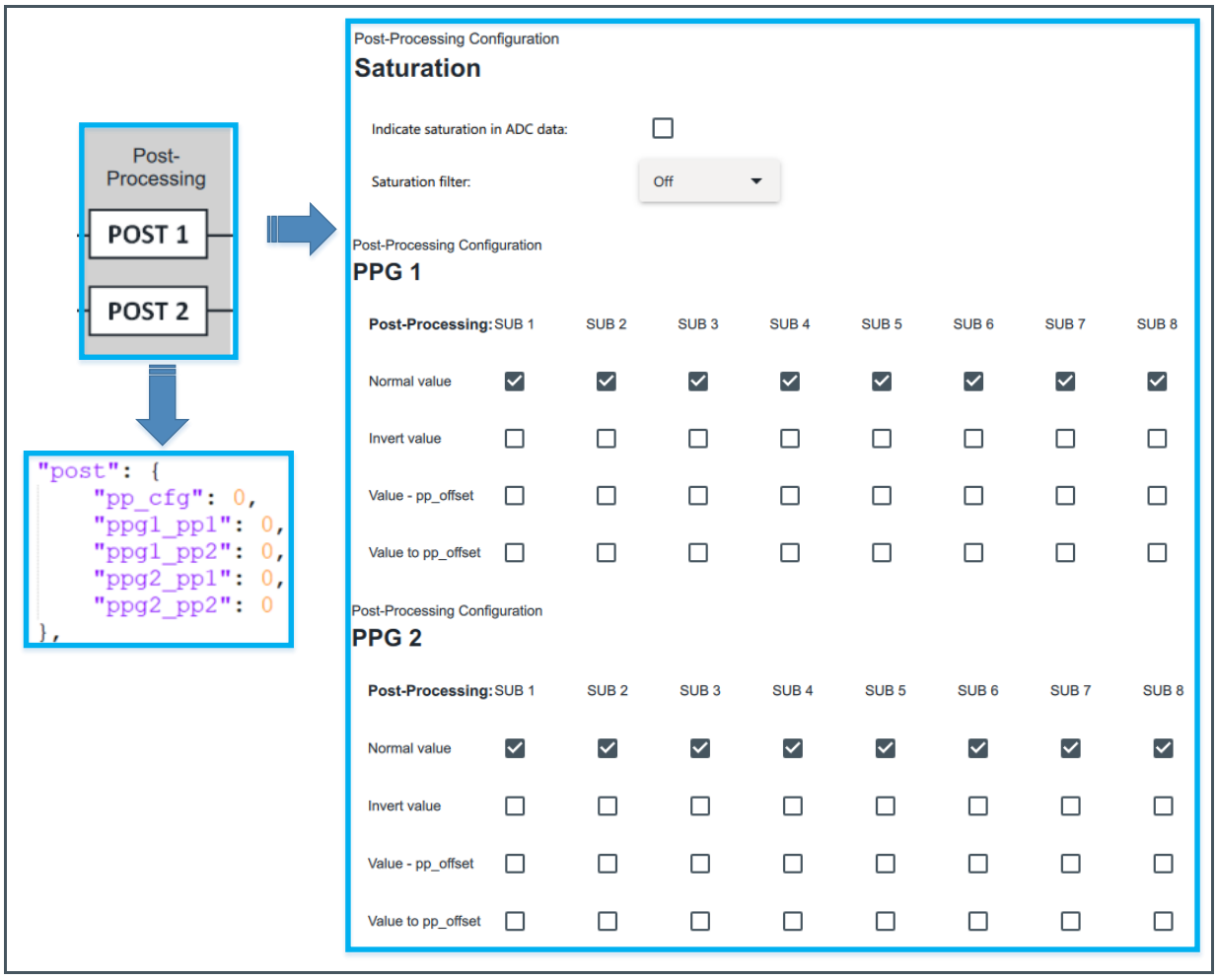
ECG1 & ECG2

- **Decimation (ECG1: Reg: 0x73 & ECG2: Reg: 0x76):** Select the value for the decimation of the SINC filter to lower the sampling frequency of the signal. During the A/D conversion process, the decimation filter can reduce the noise, maintain the signal power, and improve the SNR value.
- **Delay for averaging calculation (ECG1: Reg: 0x74 & ECG2: Reg: 0x77):** The delay after which data is valid for the average calculation.
- **Filter order 4/5 (ECG1: Reg: 0x74 & ECG2: Reg: 0x77):** The SINC Filter can be configured as a fourth or fifth order filter.
- **Filter mode (ECG1: Reg: 0x74 & ECG2: Reg: 0x77):** The SINC Filter is implemented as a CIC filter or can also run in integrator mode.
- **Start delay (ECG1: Reg: 0x75 & ECG2: Reg: 0x78):** Selects the ECG start to a delay.

5.3.7 Post-Processing Configuration

This chapter describes the adjustment of the post-processing configuration.

Figure 21:
Post-Processing Configuration



Analog Saturation

If analog saturation occurs in the modulator during a measurement, the measured value can be set to the maximum value according to the sign.

- **Indicate the saturation in the ADC data (Reg: 0x90):** This enables the indication of saturation in the ADC data, which is analog saturation. If the bit is enabled, 0% to 20% of the ADC range is set to 0, and 80% to 100% of the range is set to maximum (0xFFFF).
- **Saturation filter (Reg: 0x90):** Selects the digital filter for analog saturation. The filter removes smaller peaks than configured. For example, if the register value is set to 1 - remove 100 ns peaks.

PPG1 & PPG2

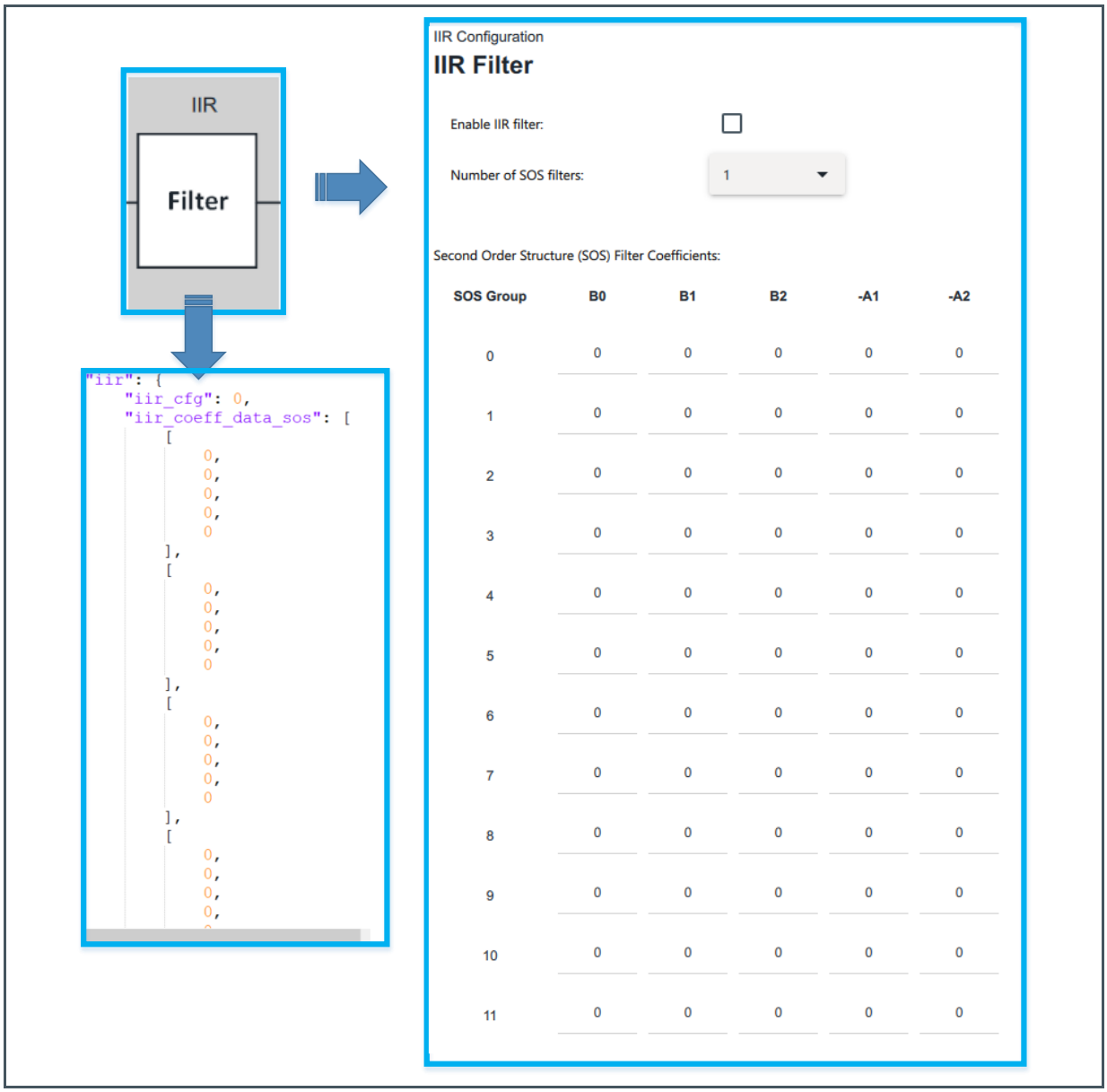
Each subsample uses, independently of one another, one of the following functions for post-processing:

- **Post-Processing (PPG1: Reg: 0x91 & 0x92 & PPG2: Reg: 0x93 & 0x94):**
  - 2'b00 – Transmission of the measured value -> Normal value
  - 2'b01 – Transmission of the inverted measured value -> Invert value
  - 2'b10 – Transfer of the result = measured value - PP offset -> (Value – pp_offset)
  - 2'b11 – Writing the measured value in the PD offset and transmission it -> Value to pp_offset

5.3.8 IIR Filter

A post-processing IIR Filter has been implemented to enhance the quality of a signal and reduce noise levels.

Figure 22:
IIR Filter



An IIR filter with the parameter is used to realize the Low-Pass filter functionality. The IIR filter is implemented sequentially as a second-order transposed DF-II structure (SOS). The filter can be configured as a higher-order filter up to the 12th order based on the SOS structure.

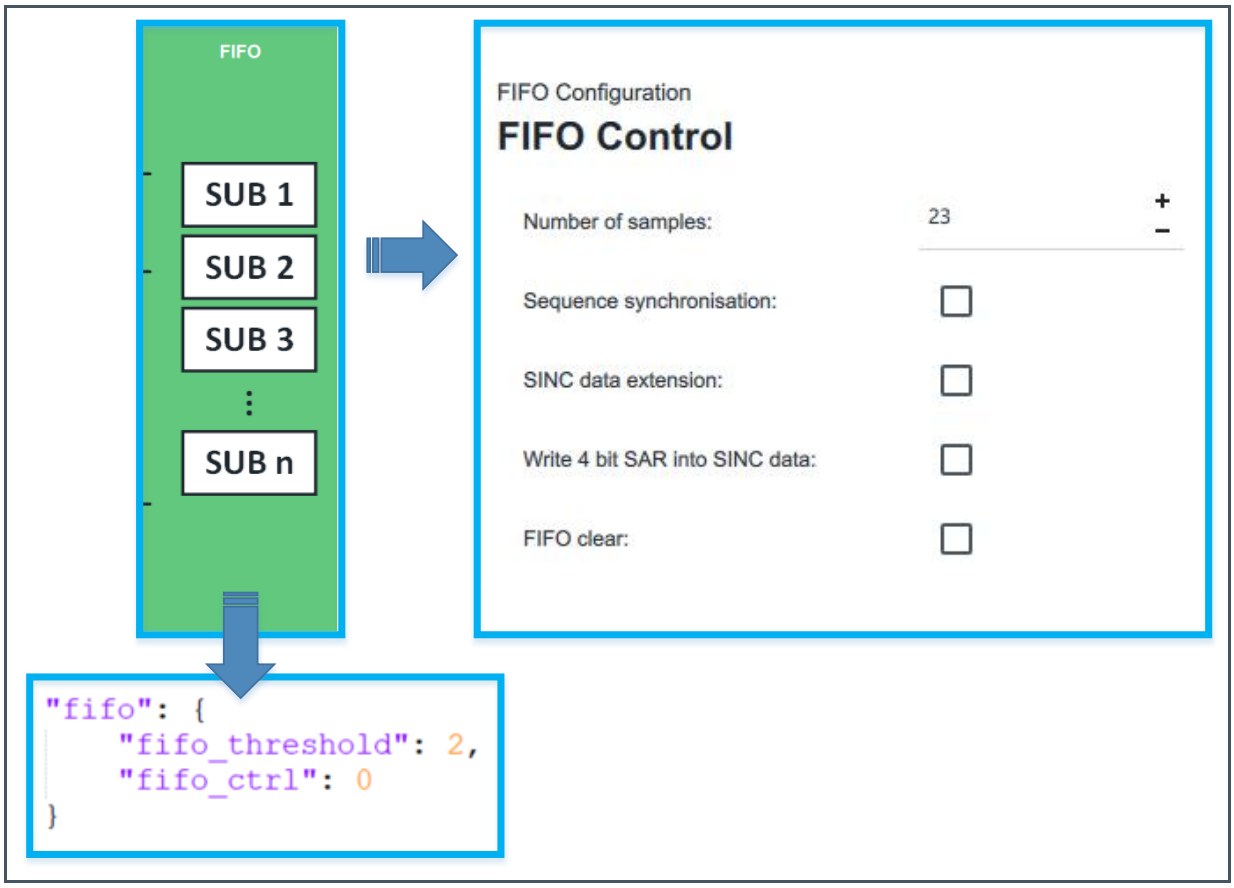
- **Enable IIR filter (Reg: 0xC7):** Enable the IIR filter.
- **Number of SOS filters (Reg: 0xC7):** Select the filter number of the cascaded SOS structure. The IIR filter can be configured as a higher-order filter up to the 12th order based on the SOS structure.

- **Second Order Structure (SOS) Filter Coefficient:** Users can program the different coefficient tables according to the evolution of their Low-pass Filter. It depends on what should be the cutoff frequency and filter settling time.

5.3.9 FIFO Configuration

The AS7058 provides a 1.5 kB FIFO. This chapter describes how the FIFO configuration can be adjusted.

Figure 23:
FIFO Configuration



The measurement data are saved in the FIFO register for the data output to an external microcontroller via the I²C communication interface. The FIFO buffering allows the external MCU to stay in idle mode during the measurements for power saving.

A FIFO data has a width of 24 bits. In addition to the measured value with a length of 20 bits, it contains 1 bit for the block frame and 3 bits for the data marker.

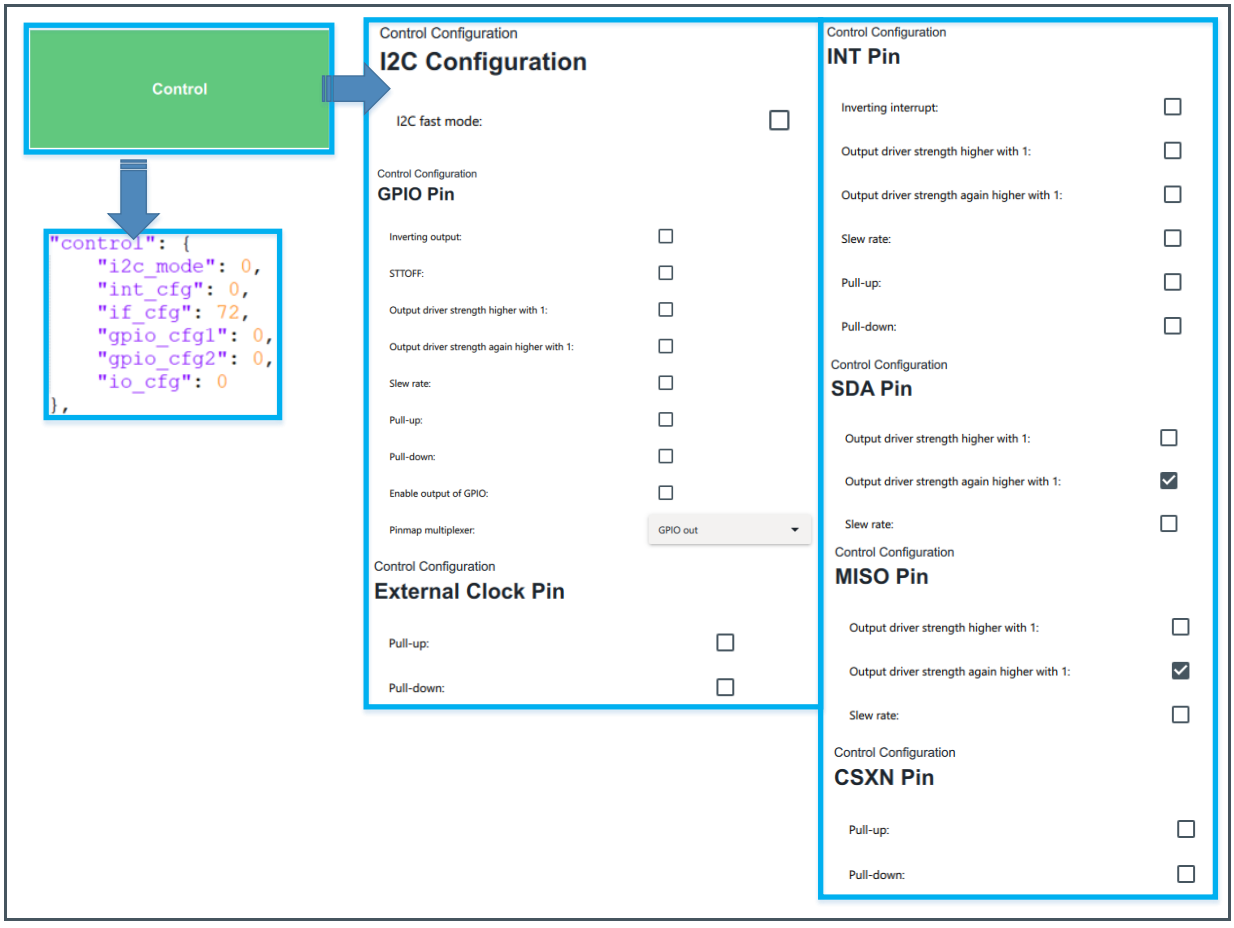
- **FIFO threshold (Reg: 0xCA & Reg: 0xCB):** Select the FIFO threshold [1, 2 … 512].

- **Sequence synchronization (Reg: 0xCB):** Enable the writing of synchronization information. If the bit is activated, a special SYNC message is inserted into the status word of the FIFO.
- **SINC data extension (Reg: 0xCB):** Enable the SINC data extension. When the SINC data extension is enabled, random data for the SINC filter configuration is added, which do not result in a data of 20-bits. Otherwise, zeros are inserted.
- **Write 4-bit SAR into SINC data (Reg: 0xCB):** Write a 4-bit SAR into the SINC data bit [3:0] .
- **FIFO clear (Reg: 0xCB):** Enable the clearing of the FIFO.

5.3.10 Control Configuration

All Interface configurations can be adjusted in the control configuration section.

Figure 24:
Control Configuration



I²C Configuration

I²C fast mode (Reg: 0x31): Enable I²C fast mode with 1 MHz. By enabling this function, the internal clock will be switched to 1 MHz from the standard 100 kHz or 400 kHz in the fast mode.

GPIO Pin

The GPIO pin combines the INPUT and OUTPUT functionalities. It also offers the option of routing an analog signal (also pin) to the pad (pin IO). The GPIO can share the "ON" signal of the internal LED/VCSEL driver for synchronization/control of external LED driver devices. The polarity of the signal is switchable. The GPIO can read external logic inputs or drive internal signals to the output.

- **Inverting output (Reg: 0x34):** Enable the inverting output of the GPIO.
- **STTOFF (Reg: 0x34):** Switch off the input Schmitt-Trigger if the LDE driver is on. (It is recommended to also disable the other part).
- **Output driver strength higher with 1 (Reg: 0x34):** Set the output driver strength high with 1.
- **Output driver strength again higher with 1 (Reg: 0x34):** Set output driver strength high again with 1.
- **Slew rate (Reg: 0x34):** Set the slew rate to another value with 1.
- **Pull-up (Reg: 0x34):** Activate the pull-up current at the IO pin (pull-up in the range of VDD to GND).
- **Pull-down (Reg: 0x34):** Activate the pull-down current at the IO pin (pull-down in the range of VDD to GND).
- **Enable output of GPIO (Reg: 0x34):** 1 = enable output; 0 = disable output.
- **Pinmap multiplexer (Reg: 0x31):** Select GPIO1/2 as the output.

External Clock Pin

It is possible to replace the internal system clock with an external clock. Only one clock with a frequency of 2 MHz or 4 MHz can be connected to the external clock input.

- **Pull-up (Reg: 0x36):** Activate pull-up at the IO.
- **Pull-Down (Reg: 0x36):** Activate pull-down at the IO.

INT Pin

The interrupt events are processed by the interrupt manager. These interrupt events must be released for processing via an interrupt enable register.

- **Inverting interrupt (Reg: 0x32):** Enable the inverting interrupt.
- **Output driver strength higher with 1 (Reg: 0x32):** Set the output driver strength high with 1.
- **Output driver strength again higher with 1 (Reg: 0x32):** Set the output driver strength high again with 1.
- **Slew rate (Reg: 0x32):** Set the slew rate to another value with 1.
- **Pull-up (Reg: 0x32):** Activate pull-up if IO is activated.
- **Pull-down (Reg: 0x32):** Activate pull-down if IO is activated.

SDA Pin

- **Output driver strength higher with 1 (Reg: 0x33):** Set the output driver strength high with 1.
- **Output driver strength again higher with 1 (Reg: 0x33):** Set the output driver strength high again with 1.

- **Slew rate (Reg: 0x33):** Set the slew rate to another value with 1.

MISO Pin

- **Output driver strength higher with 1 (Reg: 0x33):** Set the output driver strength high with 1.
- **Output driver strength again higher with 1 (Reg: 0x33):** Set the output driver strength high again with 1.
- **Slew rate (Reg: 0x33):** Set the slew rate to another value with 1.

CSXN Pin

When used as an I²C interface, the CSXN signal must be permanently pulled to level 1.

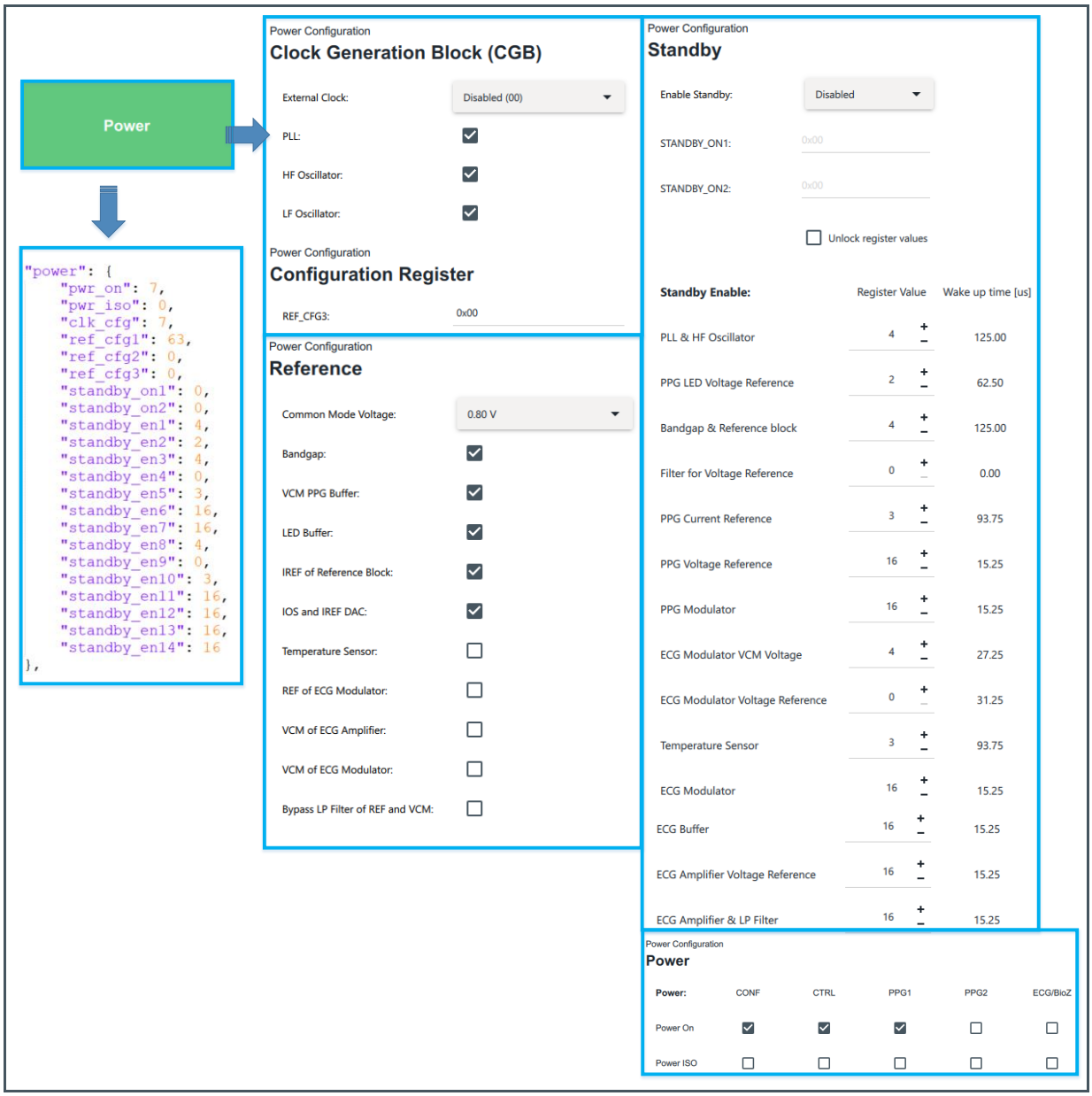
When transmitting an SPI protocol, an active SCL with CSXN = 0, the interface is set internally to the SPI protocol.

- **Pull-up (Reg: 0x33):** Activate pull-up if IO is activated.
- **Pull-down (Reg: 0x33):** Activate pull-down if IO is activated.

5.3.11 Power Configuration

The reference voltage/current configuration can be set, and the basic clock configuration can also be set in the reference configuration.

Figure 25:
Power Configuration



Clock Generation Block (CGB)

The clock generator block contains two oscillators: one for 32 kHz and one for 2 MHz. The additional 20 MHz clock is the result of a PLL within the block using the root clock of 2 MHz. The 10 MHz clock and the clocks for the modulators are derived from the 20 MHz clock.

- **External Clock (Reg: 0x18):** Select the external clock frequency. Only one clock with a frequency of 2 MHz or 4 MHz can be connected to the external clock input.

- **PLL (Reg: 0x18):** Switch on the 20 MHz PLL. The 20 MHz PLL clock is used for the modulators and is the highest frequency available in the system. It runs together with the high-frequency oscillator and is enabled on-demand by the digital core.
- **HF Oscillator (Reg: 0x18):** Switch on the 2 MHz Oscillator. The oscillator is the source of the 20 MHz PLL. The 2 MHz high-frequency oscillator is used as a clock basis for the PLL and recalibrates the low-frequency clock. The digital core controls this activity.
- **LF Oscillator (Reg: 0x18):** Switch on the 32 kHz Oscillator. The 32 kHz low-frequency clock is always active to enable low power consumption over the whole time. That clock is needed by the digital part to generate the time basis for the sampling windows.

Configuration Register

- **REF_CFG3 (Reg: 0x1B):** The power configuration group for the current selection in the common mode.

Reference

The Reference Block provides voltage and current references for all the blocks within the analog part and the LED/VCSEL drivers. It consists of a low voltage bandgap reference, which provides trimmable 0.9 V and 0.6 V voltages, a set of buffers for delivering reference voltages to the PPG channels and LED/VCSEL drivers, and a current reference circuit.

- **Common Mode Voltage (Reg: 0x19):** Select the reference voltage level for VCM – The voltage reference for the ADC. All signals are centered around this voltage. Bit 0 = 0.8 V and Bit 1 = 0.75 V.
- **Bandgap (Reg: 0x19):** Enable the bandgap. The bandgap is the main voltage reference that is used to generate all internal voltages and currents. It must be enabled for the modulator measurement and disabled in standby mode.
- **VCM PPG Buffer (Reg: 0x19):** Enable the VCM PPG Buffer – The voltage reference for the ADC is enabled before the measurement, and disabled in standby mode.
- **LED Buffer (Reg: 0x19):** Enable the LED Buffer; Voltage reference for the LED driver.
- **IREF of Reference Block (Reg: 0x19):** Enable IREF of the Reference Block.
- **IOS and IREF DAC (Reg: 0x19):** Enable IREF_DAC and IOS_DAC – The current bias reference for the MOD operation.
- **Temperature Sensor (Reg: 0x1A):** Digital input interface to enable the temperature sensor.
- **REF of ECG Amplifier (Reg: 0x1A):** Enable the Reference voltage for the ECG Amp (typ. 0.8 V).
- **VCM of ECG Amplifier (Reg: 0x1A):** Enable the common mode voltage reference (VCM) of the ECG amplifier.
- **VCM of ECG Modulator (Reg: 0x1A):** Enable the common mode voltage reference (VCM) of the ECG modulator.
- **Bypass LP Filter of REF and VCM (Reg: 0x1A):** The bypass of the low-pass filter of Reference voltage and VCM.

Standby

The power management configuration of the AS7058 can be set in the standby configuration.

- **Enable Standby (Reg: 0x1C & Reg: 0x1D):** Enable the Standby wake up times for Standby_on1 and Standby_on2.
- **STANDBY_ON1 (Reg: 0x1C):** Enable the Standby wake up times 1 to 8.
- **STANDBY_ON2 (Reg: 0x1D):** Enable the Standby wake up times 9 to 14.

Standby Enable

The standby registers are part of the AS7058 power management to reduce the power consumption of the AS7058 and the measurement system itself. Also, during continuous measurements, blocks such as the ADCs, clock generation, or reference block can switch to standby mode between several PPG and ECG sample slots if they are inactive. For usage of the standby functionality, the dedicated registers have to be activated. In the standard default setting, the automatic standby is disabled.

- **PLL & HF Oscillator (Reg: 0x1E):** Wake up time for enabling the PLL and HF Oscillator. It is necessary for each measurement (ECG & PPG).

Equation 10:

$$Wake\ up\ time = 31.25\mu s \times N$$

- **PPG LED Voltage Reference (Reg: 0x1F):** The wake up time for enabling the buffer inside the reference block, which provides the reference voltage for the LED driver. It is necessary when using the PPG modulator. Equation 10 shows the calculation of the wake up time.
- **Bandgap & Reference block (Reg: 0x20):** The wake up time for enabling the bandgap and the current reference blocks inside the reference block. It is necessary for each measurement. Equation 10 shows the calculation of the wake up time.
- **Filter for Voltage Reference (Reg: 0x21):** The wake up time for enabling a low pass filter inside the reference block used by the common-mode voltages of the modulators. The filter starts bypassing to make power-up faster. It is necessary for each measurement. Equation 10 shows the calculation of the wake up time.
- **PPG Current Reference (Reg: 0x22):** The wake up time for enabling the bias currents for the reference DACs inside the PPG modulators. It is necessary when using the PPG modulators. Equation 10 shows the calculation of the wake up time.
- **PPG Voltage Reference (Reg: 0x23):** The wake up time for enabling the buffer inside the reference block, which provides the VCM voltage for the PPG modulators. It is necessary when using the PPG modulators.

Equation 11:

$$Wake\ up\ time = N \times TCLK\_2MHz$$

- **PPG Modulator (Reg: 0x24):** The wake up time for enabling the configured PPG modulators. It is necessary when using the PPG modulators. Equation 11 shows the calculation of the wake up time.

- **ECG Modulator VCM Voltage (Reg: 0x25):** The wake up time for enabling the buffer inside the reference block, which provides the VCM voltage for the ECG modulators. It is necessary when measuring the ECG signals, BioZ signals, or temperature. Equation 11 shows the calculation of the wake up time.
- **ECG Modulator Voltage Reference (Reg: 0x26):** The wake up time for enabling the buffer inside the reference block, which provides the reference voltage for ECG modulators. It is necessary, when measuring ECG signals, BioZ signals or temperature. Equation 11 shows the calculation of the wake up time.
- **Temperature Sensor (Reg: 0x27):** The wake up time for enabling the temperature sensor inside the reference block. It is only necessary when measuring temperature, which is measured through the ECG modulator. Equation 10 shows the calculation of the wake up time.
- **ECG Modulator (Reg: 0x28):** The wake up time for enabling the ECG modulator. It is necessary when measuring the ECG signals, BioZ signals, or temperature. Equation 11 shows the calculation of the wake up time.
- **ECG Buffer (Reg: 0x29):** The wake up time for enabling the buffer, which provides the signal to the ECG modulator. It is necessary when measuring ECG signals, BioZ signals, or temperature. Equation 11 shows the calculation of the wake up time.
- **ECG Amplifier Voltage Reference (Reg: 0x2A):** The wake up time for enabling the buffer inside the reference block, which provides the VCM voltage for the ECG amplifier. It is necessary when measuring ECG signals through the ECG modulator. Equation 11 shows the calculation of the wake up time.
- **ECG Amplifier & LP Filter (Reg: 0x2B):** The wake up time for enabling the ECG amplifier and the anti-aliasing low pass filter. It is necessary when measuring ECG signals of the filtered temperature signal through the ECG modulator. Equation 11 shows the calculation of the wake up time.

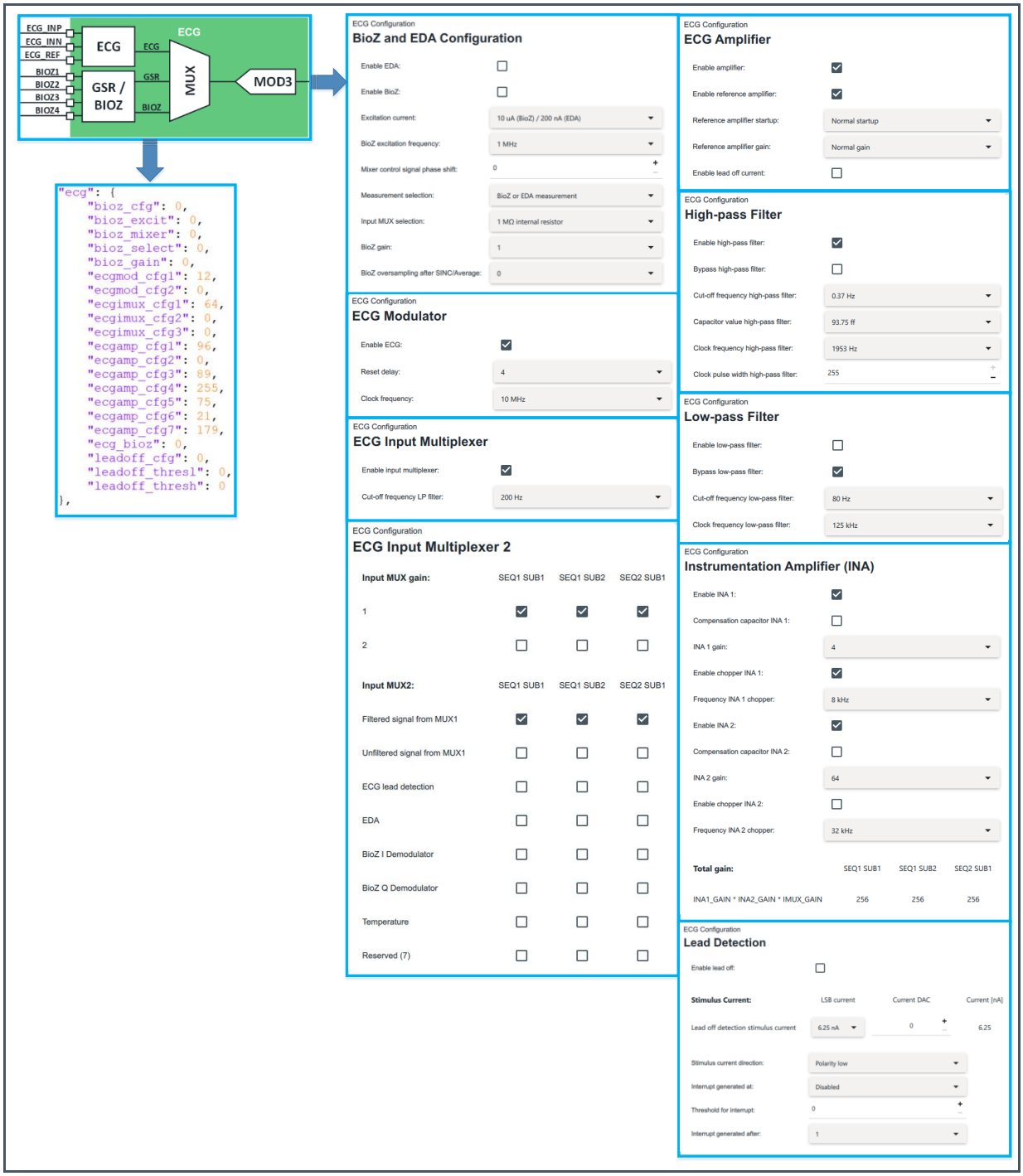
Power

Switchable power domains consist of CONF, CTRL, PPG1, PPG2, and ECG/BioZ.

- **Power On (Reg: 0x2D):** Select Power On for CONF, CTRL, PPG1, PPG2, and ECG/BioZ.
- **Power ISO (Reg: 0x2E):** Select Power ISO for CONF, CTRL, PPG1, PPG2, and ECG/BioZ.

5.3.12 ECG & GSR/BIOZ Configuration

Figure 26:
ECG & GSR/BIOZ Configuration



BioZ and EDA Configuration

A small alternating current (AC) is applied to flow through the body, and the voltage is measured such that the bio-impedance can be calculated. The Bio-impedance channel is controlled via several signals from the sequencer and the I²C registers. The 10 µA currents, 1 µA currents, and BIOZ_VCM are provided by the reference block.

- **Enable EDA (Reg: 0xB2):** Enables the EDA measurement.
- **Enable BioZ (Reg: 0xB2):** Enables the BioZ measurement.
- **Excitation current (Reg: 0xB3):** Select the BioZ excitation current amplitude from 10 µA to 115 µA.
- **BioZ excitation frequency (Reg: 0xB3):** Select the BioZ excitation signal frequency from 1 kHz to 1 MHz.
- **Mixer control signal phase shift (Reg: 0xB4):** Select the Mixer control signal phase shift.

  Equation 12:

  $$1MHz\ excitation\ frequency = mix\_ph\_con \times 18° \rightarrow Max\ value\ (19) = 342°$$

  Equation 13:

  $$non-1MHz\ excitation\ frequency = mix\_ph\_con \times 9° \rightarrow Max\ value(31) = 279°$$

- **Measurement selection (Reg: 0xB5):** The BioZ Measurement selection. For example,
  - 0: Bioimpedance or GSR measurement;
  - 1: Offset (0 Ω) measurement;
  - 2: Internal 2 kΩ resistor measurement;
  - 3: Internal 1 MΩ resistor measurement;
  - 4: Internal 1 kΩ resistor measurement;
  - 5: Internal 500 Ω resistor measurement
- **Input MUX selection (Reg: 0xB5):** The BioZ input MUX selection.
- **BioZ gain (Reg: 0xB6):** Select the BioZ gain.
  - 0 - x1 gain;
  - 1 - x2 gain
- **Oversampling after SINC/Average (Reg: 0xC3):** Select oversampling after the SINC/Average.

ECG Modulator

Electrodes capture the voltage difference, filter out noise, and amplify the signal. The ECG modulator modulates the amplitude of the ECG signal. ECG modulation can be enabled to modulate the ECG signal. DSM gain can also be enabled. An anti-aliasing filter (AAF) is used in the ECG-ADC input selection before the signal sampler or ECG-ADC voltage input to restrict the bandwidth of a signal and satisfy the band over the band of interest.

- **Enable ECG (Reg: 0xB7):** Enable the ECG modulator.
- **ADC gain (Reg: 0xB7):** Select the ADC gain.

- 0: Default gain
- 1: High gain

- **ADC current (Reg: 0xB7):** Select the ADC current.
  - 0: 10 µA;
  - 1: 5 µA;
  - 2: 12.5 µA;
  - 4: 6.25 µA
- **Reset delay (Reg: 0xB8):** Select the reset time for the ECG modulator = N * MOD_CLK.
- **Clock frequency (Reg: 0xB8):**
  - MOD_CLK (Modulator clock frequency) – The frequencies 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz can be set. With a reduction of the Modulator clock frequency, the converting time will be increased, and the signal-to-noise ratio will improve. Also, the power consumption of the AS7058 will increase.

ECG Input Multiplexer

This block selects among 16 inputs and connects to an anti-aliasing filter (AAF). The output of this block is connected to the ECG DSM block.

- **Enable input multiplexer (Reg: 0xB9):** Enables the input multiplexer of the ECG modulator.
- **Cut-off frequency LP filter (Reg: 0xB9):** Selects the nominal cut-off frequency of the antialiasing low pass filer – 200 Hz, 270 Hz, 400 Hz, and 800 Hz.
- **Input voltage MUX1 (Reg: 0xB9):** Selects the input voltage for the first stage multiplexer.

ECG Input Multiplexer 2

To implement measurement sequences there is a second stage multiplexer that is controlled by the digital sequencer.

- **Input MUX gain (Reg: 0xBA & Reg: 0xBB):** Selects the gain (0: Gain = 1 and 1: Gain = 2) of the output buffer of ECGMOD_IMUX for the referred sub-sequence (sub1, sub2, or sub3).
- **Input MUX2:** Selects the input of the second stage multiplexer (MUX2) for the referred sub-sequence (sub1, sub2, or sub3).
- **Filtered Signal from MUX1 (Reg: 0xBA & Reg: 0xBB):** Filtered signal coming from the first stage multiplexer for subsamples 1 to 3.
- **Unfiltered signal from MUX1 (Reg: 0xBA & Reg: 0xBB):** Unfiltered signal coming from the first stage multiplexer for subsamples 1 to 3.
- **ECG lead detection (Reg: 0xBA & Reg: 0xBB):** ECG lead detection (ECG_LEAD_P/ECG_LEAD_N) for subsamples 1 to 3.
- **EDA (Reg: 0xBA & Reg: 0xBB):** EDA/GSR signal (GSR_OUTP/GSR_OUTN) for subsamples 1 to 3.
- **BioZ I Demodulator (Reg: 0xBA & Reg: 0xBB):** I DEMOD (IDEMOD_OUTP/IDEMOD_OUTN) for subsamples 1 to 3.
- **BioZ Q Demodulator (Reg: 0xBA & Reg: 0xBB):** Q DEMOD (QDEMOD_OUTP/QDEMOD_OUTN) for subsamples 1 to 3.

- **Temperature (Reg: 0xBA & Reg: 0xBB):** The temperature (VTEMP/VCM_ECG) for subsamples 1 to 3.
- **Reserved (Reg: 0xBA & Reg: 0xBB):** Not used (VCM_ECG, VCM_ECG) for subsamples 1 to 3.

ECG Amplifier

The ECG (electrocardiogram) amplifier is a high impedance, low noise instrumentation amplifier with analog circuitry to a high-pass filter that amplifies the signal.

- **Enable amplifier (Reg: 0xBC):** Enable the ECG amplifier.
- **Enable reference amplifier (Reg: 0xBC):** Enable the ECG reference amplifier.
- **Reference amplifier startup (Reg: 0xC3):** ECG reference amplifier fast startup, where 0 - normal startup and 1 - fast startup.
- **Reference amplifier gain (Reg: 0xBC):** ECG reference amplifier high gain, where 0 - normal gain and 1 - high gain.
- **Enable LEAD off current (Reg: 0xBC):** Enable LEAD off current during the ECG amplifier signal measurement.

High-Pass Filter

This filter employs a fully differential first-order high-pass filter topology. The filter is controlled by the digital block.

- **Enable high-pass filter (Reg: 0xBE):** Enable the ECG SC high-pass filter.
- **Bypass high-pass filter (Reg: 0xBE):** Enable the Bypass ECG SC high-pass filter.
- **Cut-off frequency high-pass filter:** Select the cut-off frequency for the ECG amplifier high-pass filter, where
    - 0.22 Hz,
    - 0.37 Hz,
    - 5 Hz
    - 10 Hz
- **Capacitor value high-pass filter (Reg: 0xBE):** Select the capacitor value for the ECG SC high-pass filter, where
    - 0: 750 fF,
    - 1: 750 fF/2,
    - 2: 750 fF/4, and
    - 3: 750 fF/8
- **Clock frequency high-pass filter (Reg: 0xBE):** Select the clock frequency in the ECG SC high-pass filter, where,
    - 0: 977 Hz (1 MHz/1024),
    - 1: 1953 Hz (1 MHz/512),
    - 2: 3906 Hz (1 MHz/256),
    - 3: 7813 Hz (1 MHz/128),
    - 4: 15.6 kHz (1 MHz/64),

- 5: 250 kHz,
- 6: 500 kHz, and
- 7: 1 MHz

- **Clock pulse with high-pass filter (Reg: 0xBF):** Select the clock pulse width in the ECG SC high-pass filter.
  - 0: 0.5 µs;
  - 1: 1 µs;
  - 2: 2 µs; …; 254: 254 µs;
  - 255: 50% duty cycle

Low-pass Filter

The ECG amplifier includes a switched capacitor low-pass filter whose cutoff frequency depends on the frequency of the clock signal.

- **Enable low-pass filter (Reg: 0xC0):** Enable the ECG SC low-pass filter.
- **Bypass low-pass filter (Reg: 0xC0):** Enable the Bypass ECG SC low-pass filter.
- **Cut-off frequency high-pass filter:** Select the cut-off frequency for the ECG amplifier low-pass filter:
  - 80 Hz,
  - 160 Hz,
  - 320 Hz
  - 640 Hz
- **Clock frequency low-pass filter (Reg: 0xC0):** Select the clock frequency in the ECG SC low-pass filter.
  - 0: 1MHz/8 (fc_lpf=80Hz),
  - 1: 1MHz/4 (fc_lpf=160Hz),
  - 2: 1MHz/2 (fc_lpf=320Hz), and
  - 3: 1MHz/1 (fc_lpf=640Hz)
- **Clock low-pass filter (Reg: 0xBE):** Select the clock for the ECG SC low-pass filter.

Instrumentation Amplifier (INA)

The ECG amplification is obtained from two stages of amplification, INA1 and INA2. Both amplifiers have the possibility to enable the chopper.

- **Enable INA1 (Reg: 0xC0):** Enable the ECG INA1.
- **Bypass INA1 (Reg: 0xC0):** Bypass the ECG INA1.
- **INA1 gain (Reg: 0xC0):** Select the gain of INA1, where,
  - 0: gain = 1,
  - 1: gain = 2,
  - 2: gain = 3, and
  - 3: gain = 4

- **Enable chopper INA1 (Reg: 0xC2):** Enable the chopper for INA1.
- **Frequency INA1 chopper (Reg: 0xC2):** Select the frequency of the INA1 chopper modulators clock. When the INA1 chopper is enabled, the frequency is 1 kHz – 32 kHz. If the INA1 chopper is disabled, the frequency must be zero.
- **Enable INA2 (Reg: 0xC1):** Enable ECG INA2.
- **Bypass INA2 (Reg: 0xC1):** Bypass ECG INA2.
- **INA2 gain (Reg: 0xC1):** Select gain of INA2.
    - 0: gain = 1;
    - 1: gain = 2;
    - 2: gain = 4;
    - 3: gain = 8;
    - 4: gain = 16;
    - 5: gain = 32;
    - 6: gain = 64;
    - 7: gain = 128
- **Enable chopper INA2 (Reg: 0xC2):** Enable the chopper for INA2.
- **Frequency INA2 chopper (Reg: 0xC2):** Select the frequency of the INA2 chopper modulators clock. When the INA2 chopper is enabled, the frequency is 4 kHz – 100 kHz. If the INA2 chopper is disabled, the frequency must be zero.

LEAD Detection

The ECG leadoff circuit is a differential DAC current intended to apply a stimulus to the inputs. The lead-off data have several different modes. In the lead-off detection block, each lead-off data is compared with the lead-off threshold.

- **Enable LEAD off (Reg: 0xC4):** Select the lead-off detection stimulus current range.
- **Stimulus current (Reg: 0xBD):**
    - **Lead-off detection stimulus current:** The most significant bit selects between normal ranges and a special low current range. Normal ranges follows 2 bits - select the LSB current (6.25 nA, 12.5 nA, 18.75 nA, 25 nA). Special low current range follows the LSB which is 1.6 nA.
- **Stimulus current direction (Reg: 0xBC):** Select the behavior of the lead-off polarity signal during lead-off detection sequence.
- **Interrupt generated at (Reg: 0xC4):** Select “enable event” for generation of the lead-off interrupt.
- **Threshold for interrupt (Reg: 0xC5 & Reg: 0xC6):** Select the threshold for the lead-off.
- **Interrupt generated after (Reg: 0xC4):** Select oversampling for the lead-off.

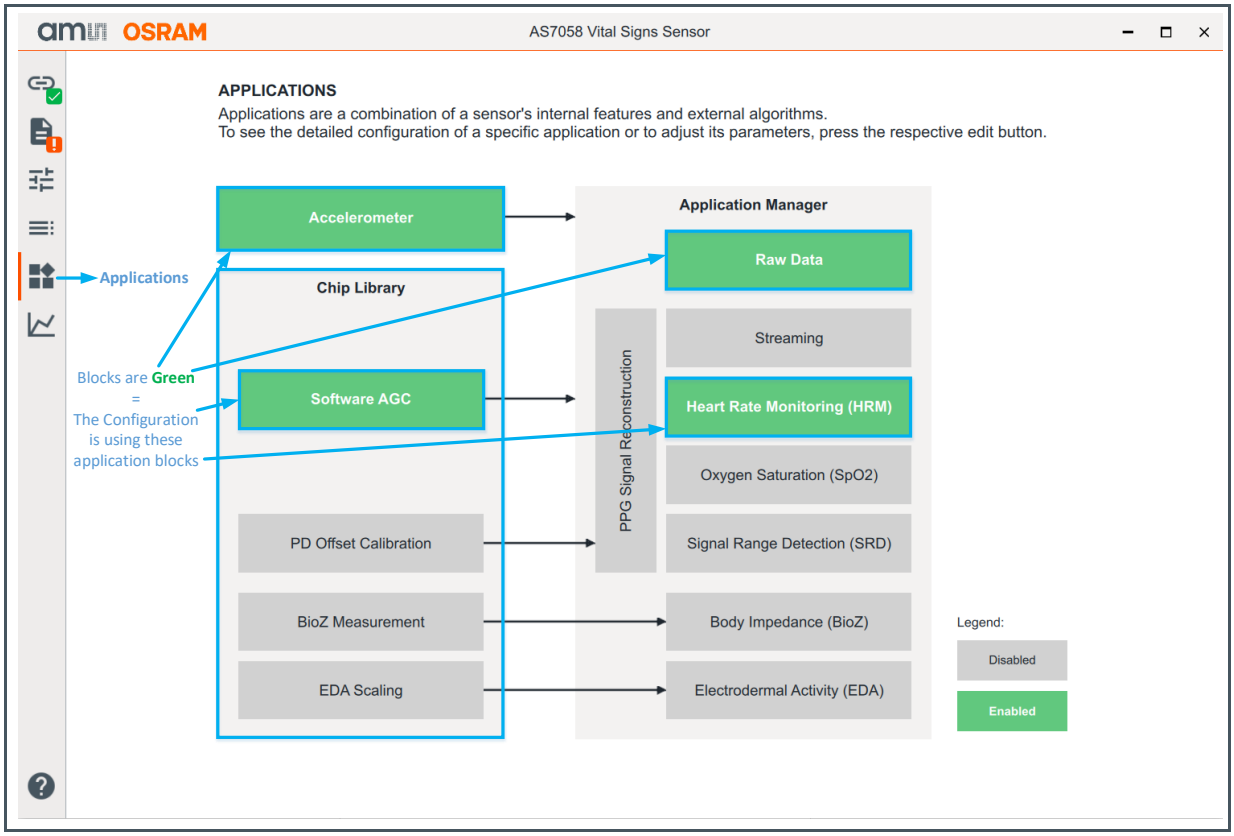
5.4 Applications

Application-related algorithms and vital signs parameters are described under the Application tab.

This block features the AGC configuration that controls PD offset and LED current, as well as algorithms such as HRM and SpO_2. Under these tabs, the parameters related to these applications can be checked and adjusted individually. The accelerometer (ACC) can also be enabled or disabled with HRM and SpO_2 applications.

Various applications such as Electrocardiogram (ECG), Body Impedance (BMI), and Electrodermal Activity (EDA) can also be activated.

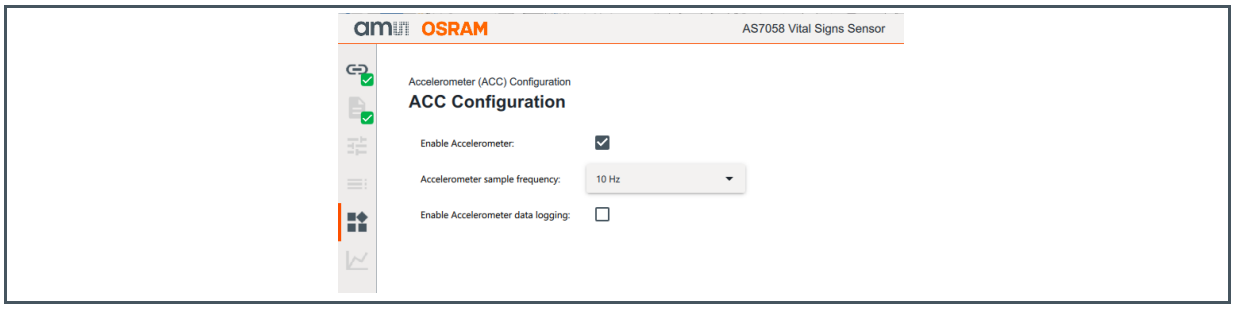
Figure 27:
Application Tab Overview



5.4.1 Accelerometer (ACC)

The accelerometer is also activated when the HRM algorithm is selected. However, the accelerometer can be enabled and disabled via the user interface.

Figure 28:
Accelerometer



The accelerometer is used for displacement information. The HRM application includes this accelerometer data and uses it for motion compensation.

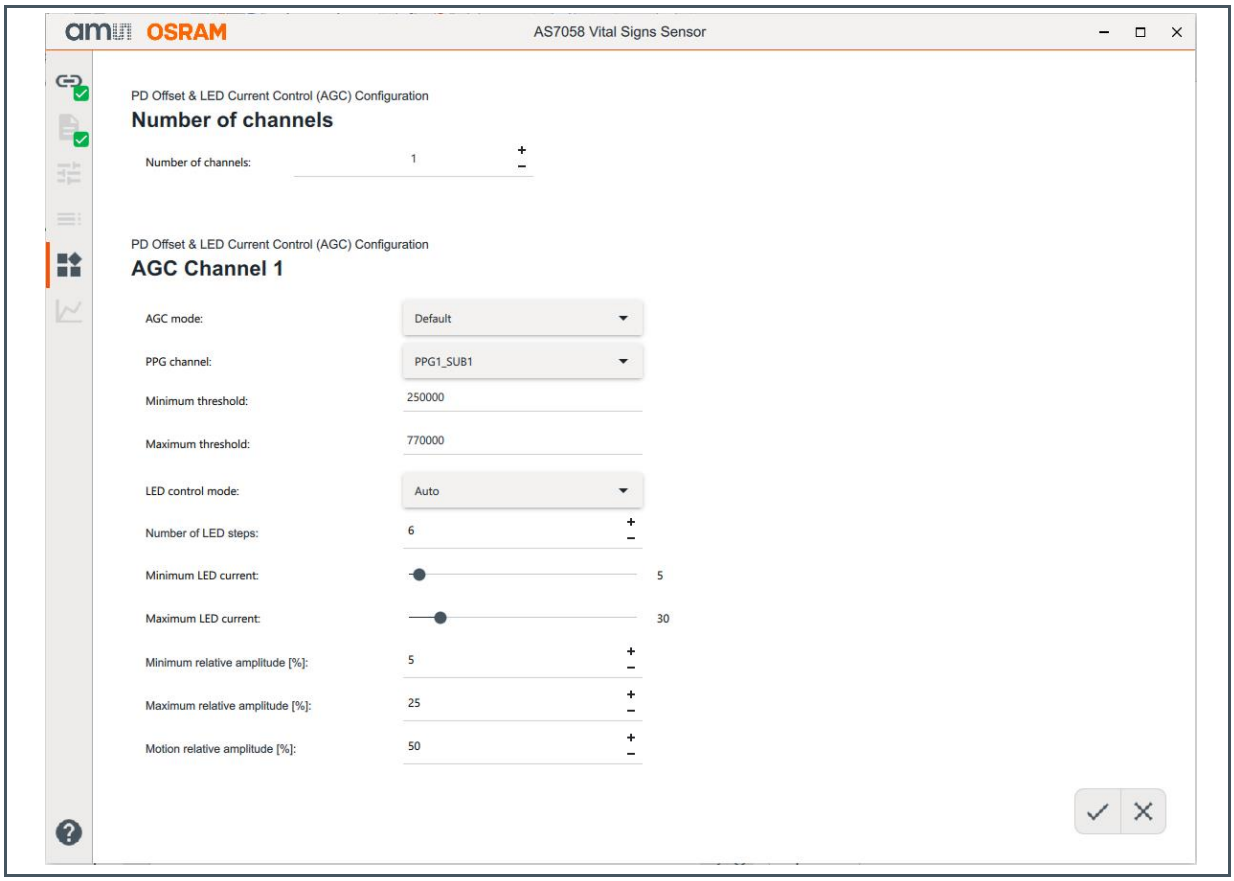
5.4.2 Chip Library

The AS7058 Chip Library implements a driver for the AS7058 AFE, which handles communication with the AFE and is used to configure the device and perform measurements. It also integrates the Automatic Gain Control (AGC) Algorithm, which adjusts LED and photodiode offset currents by analyzing the PPG data acquired by the AS7058 AFE.

5.4.3 Software AGC (Automatic Gain Control)

The PD offset and LED current control is an algorithmic approach to increase the signal quality of the PPG signals. The algorithm continuously monitors the ADC outputs and, if necessary, reconfigures the AS7058 while measuring to ensure ideal conditions.

Figure 29:
PD Offset and LED Current Control Submenu



The firmware supports up to four AGC instances, each running independently. Thus, each AGC instance controls a single PPG channel, where one of the eight available PPG sub-samples from each ADC could be selected.

The AGC attempts to keep the PPG signal within a configured range by controlling the PD offset & LED current. It is also possible to enable the control mode of the PPG amplitude. When enabled, the AGC attempts to keep the PPG amplitude within a configured range by controlling the current of the LEDs assigned to that PPG channel.

- **Automatic gain control (AGC) Mode:** Enables the AGC algorithm for the channel.
- **PPG Channel:** The PPG Signal is assigned to the AGC channel and is required when the channel is enabled.
- **Minimum/Maximum Threshold:** The minimum or maximum threshold specifies the range in ADC counts to keep the PPG signal within.
- **LED Control Mode:** PPG amplitude control can be disabled or enabled in automatic or external mode via the LED control mode. In Auto mode, amplitude control is performed by the AGC itself. In the external mode, the LED current can be increased or decreased by an external algorithm however, this mode is not yet implemented.

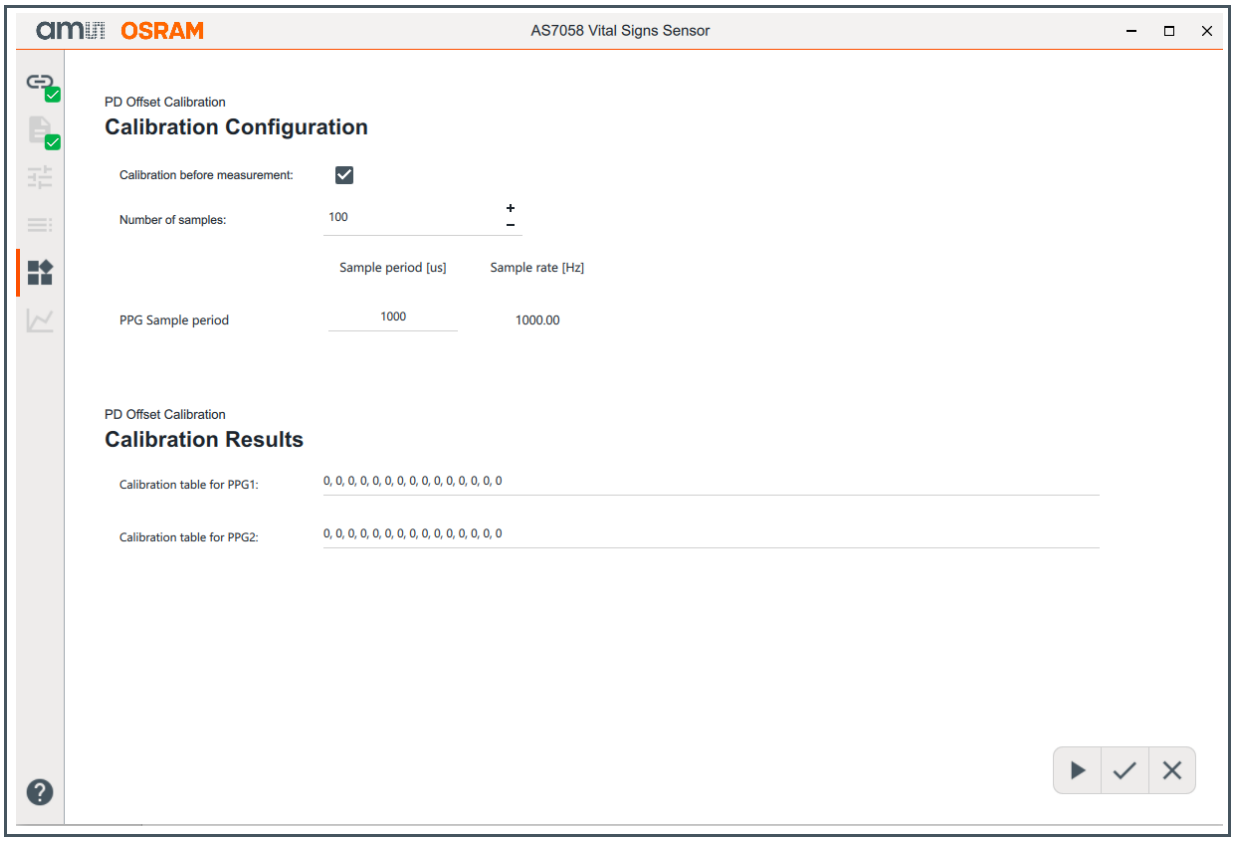
- **Number of LED steps:** The number of LED steps specifies the number of LED current increments to step through the configured LED current range. This parameter determines the granularity/speed of the amplitude control. When the AGC algorithm determines that the LED current needs to be increased or decreased and the bounds of the LED current range are not yet reached, the LED current is adjusted by one step.
- **Minimum/Maximum LED Current [mA]:** The minimum or maximum LED current limits the LED current output by the PPG amplitude control.
    - Configuration Notes - The minimum current should be low enough to keep the PPG amplitude within the configured amplitude range for high perfusion/bright skin tones. The maximum current should be high enough to keep the PPG amplitude within the configured amplitude range for low perfusion/dark skin tones.
- **Minimum/Maximum Relative Amplitude [%]:** The minimum or maximum relative amplitude specifies the target PPG amplitude range, relative to the configured PPG range, in percent (in the example shown in Figure 29, the minimum PPG amplitude would be 200000 ADC counts, and the maximum PPG amplitude would be 400000 ADC counts).
    - Configuration Notes - Consider the dynamic range of the use case signal and the PPG signal requirements of the vital sign algorithm being used. For use cases with strong motion artifacts, the PPG amplitude would typically be considered low, while for use cases with limited motion artifacts, the PPG amplitude could typically be considered high. The selected PPG amplitude range is related to the configured LED current range. The AGC algorithm tends to overestimate the PPG amplitude.
- **Motion Relative Amplitude [%]:** The Motion Relative Amplitude sets the limit relative to the configured PPG range in percent. If the occurrences of the signal amplitudes are higher than the set value, then it is considered with motion artifacts, and the PPG amplitude control does not adjust the LED current.

5.4.4 PD Offset Calibration

PD Offset Calibration is used to perform PPG measurements with enabled hardware-implemented PD offset control. This also referred to as Advanced Automatic Offset Control (AAOC). The AAOC is developed to ensure that the PPG signals are placed in the not saturated area of the ADC range.

The newly developed AAOC hardware algorithm uses a different behavior to estimate the value of the PPG signal and control the DAC current. The AAOC does a very short pre-measurement to estimate the latest value of the PPG signal, calculates the offset current and adjusts the DAC to use the new value. After the pre-measurement, a single sampling (measurement) is carried out and the measured value is processed as usual. With this new method, it is possible to measure PPG signals without loss of information (saturation), although there is a large influence on the signal, such as a rapidly changing ambient light during movement. If the impact on the signal is greater than the regulation limits, which depend on the sensor configuration (DAC-FSR, ADC-FSR, LED, etc.) the signal will be saturated.

Figure 30:
PD Offset Calibration



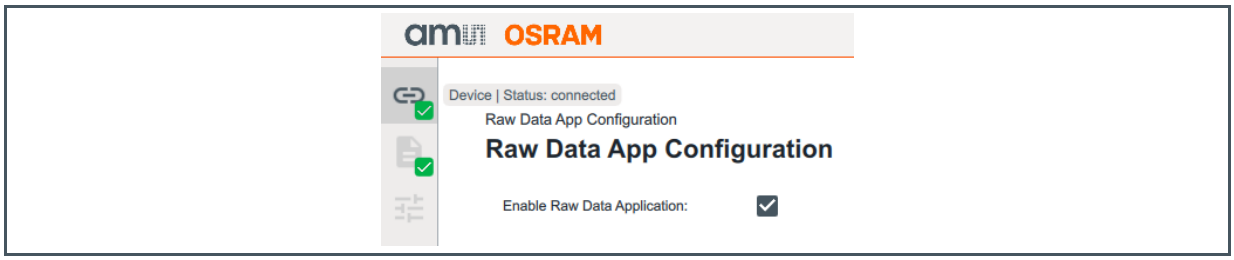
5.4.5 Application Manager

The application manager connects the chip library with the included bio applications. It receives measurement data from the AS7058 chip library and combines it with accelerometer data.

5.4.6 Raw Data

Instead of HRM, RRM and SpO_2, raw data can be selected. The results of an analog to digital converter's (ADC) conversion are represented as a digital number with varying resolution on the bit length and settings used.

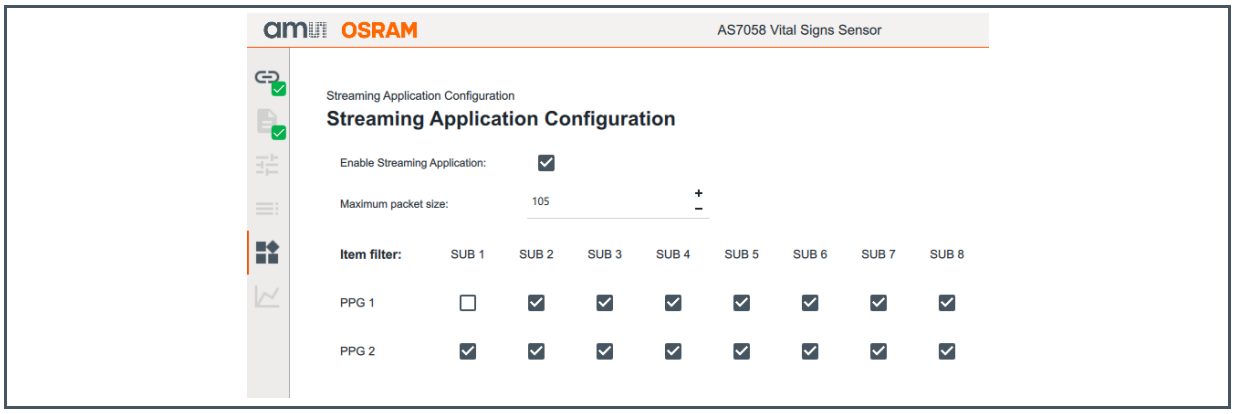
Figure 31:
Raw Data App Configuration



5.4.7 Streaming

The streaming application transmits extended ADC values which additionally include the corresponding PD offset value.

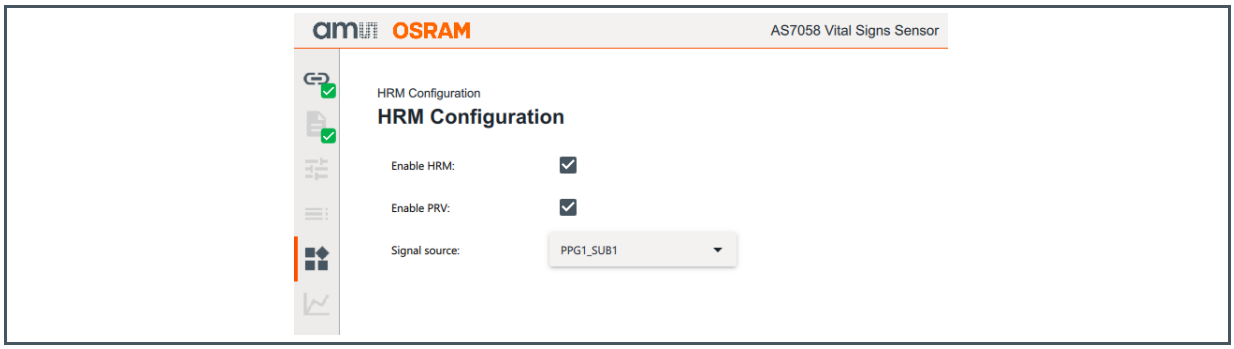
Figure 32:
Streaming Application Configuration



5.4.8 Heart Rate Monitoring (HRM)

The HRM application takes the defined PPG signal as an input and estimates the heart rate in beats per minute.

Figure 33:
HRM Configuration

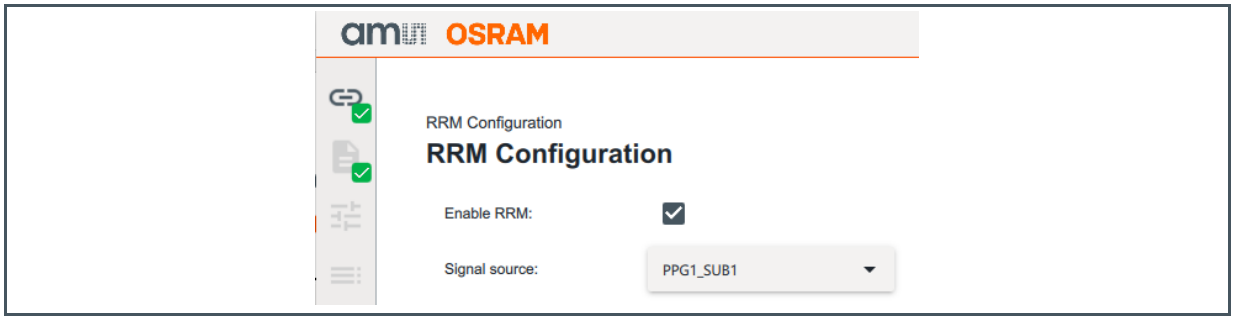


Pulse Rate Variability (PRV) can be enabled for HRM when sample rate >=100 Hz.

5.4.9 Respiration Rate (RRM)

The RRM application takes the defined PPG signal as an input and estimates the respiration rate in beats per minute.

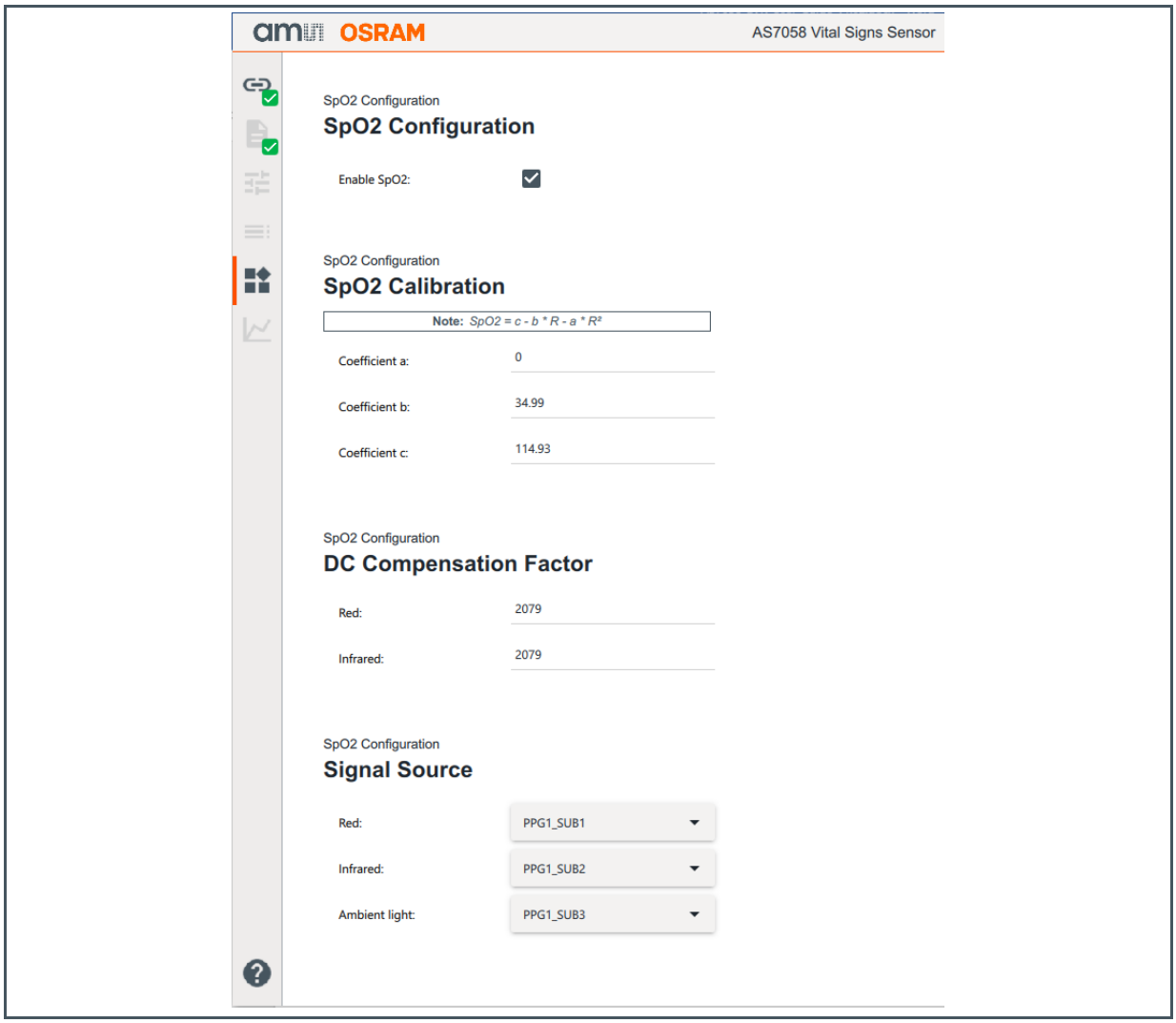
Figure 34:
RRM Configuration



5.4.10 Oxygen Saturation (SpO_2)

"SpO_2" is for configuring the SpO_2 Parameters. Enter the parameters associated with the specific settings of the AS7058 in the SpO_2 configuration settings. Due to production and assembly tolerances, it is recommended that the below-mentioned factors must be determined for the device under development after the sensor has been integrated and the optical configuration is finalized.

Figure 35:
SpO₂ Configuration



SpO₂ Calibration

The R-value, calculated by the firmware, is used to calculate oxygen saturation. Different models are proposed in the literature for this purpose. For the AS7058, both the quadratic (Equation 14) and the linear model (Equation 15) are implemented:

Equation 14:

$$SpO2 = c - b \times R - a \times R^2$$

Equation 15:

$$SpO2 = -b.R + c$$

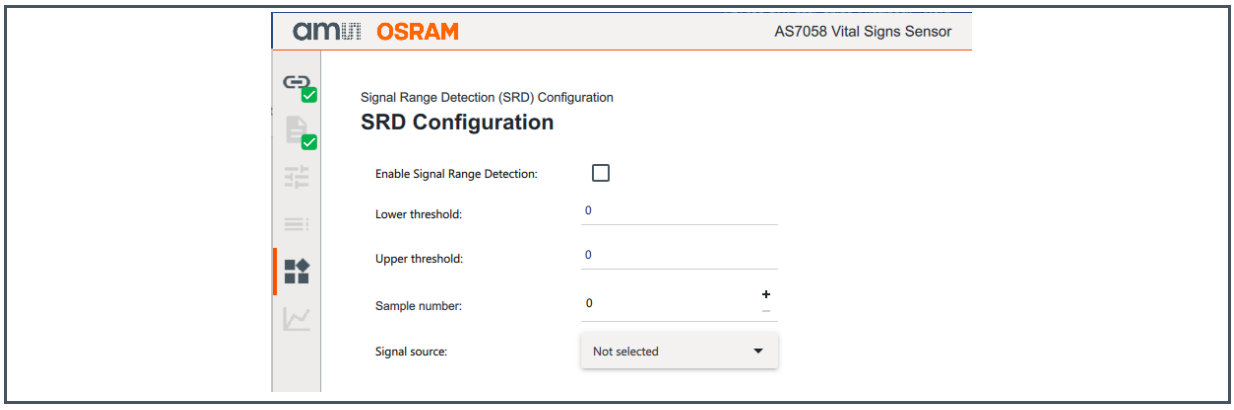
DC Compensation

The resulting factors for the DC compensation, the RED photodiode offset factor, and the photodiode offset factor IR for the evaluation kit depend on the different settings of the ADC range, the PD offset range, and the PPG clock frequency. These factors, associated with the specific settings of the AS7058, must then be entered in the SpO_2 configuration settings.

5.4.11 Signal Range Detection (SRD)

The SRD application is used to support proximity detection. The software proximity output is an additional signal that uses one of the PPG & ECG signal outputs. The separately programmable proximity detection has high and low thresholds, such that the high threshold is greater than the low threshold.

Figure 36:
Signal Range Detection (SRD)

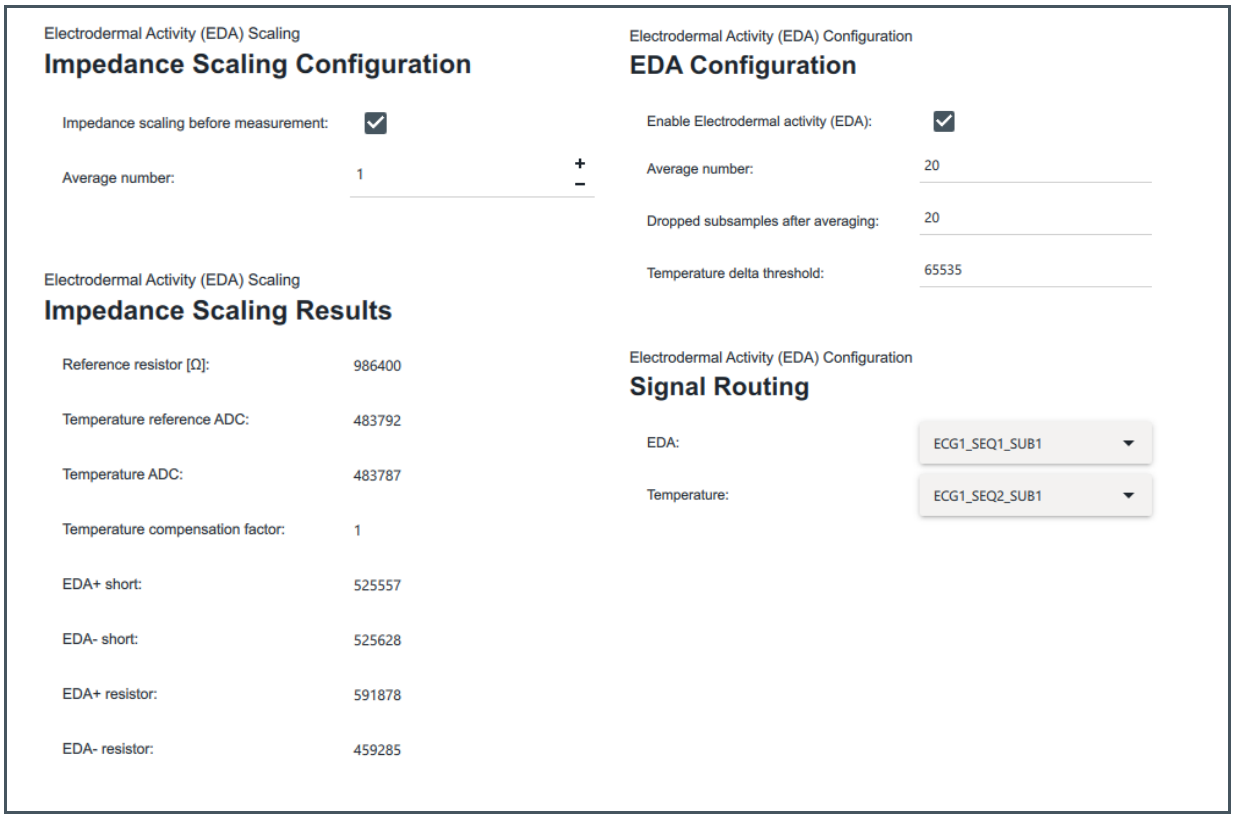


- **Enable Signal Range Detection:** Enables the Signal Range Detection (SRD) application.
- **Lower threshold:** The minimum threshold for proximity with a value range of [0: 2^20 – 1].
- **Upper threshold:** The maximum threshold for proximity with a value range of [0: 2^20 – 1].
- **Sample Number:** Select the minimum number of consecutive samples that need to fall into the new signal status region before the signal status change may trigger.
- **Signal Source:** Select the signal source for the SRD application.

5.4.12 Electrodermal Activity (EDA) & EDA Scaling

The EDA application block is for estimating the resistance of the body component between the electrodes. The application works by injecting a low amplitude current having a square waveform and measuring the potential difference across the electrodes. The voltage signal is converted to ADC counts, and the resistance is estimated from it. The measured resistance is displayed in the GUI in Ohm.

Figure 37:
EDA Configuration



Impedance Scaling Configuration

Enable executing the impedance scaling before starting measurement on the measurement page.

Impedance Scaling

There is no continuous measurement for EDA as PPG or ECG. There are two measurement stages for EDA. In the first measurement stage, the reference measurement is carried out using impedance scaling. This measurement mode measures different resistances by reconfiguring the AS7058 AFE between each measurement. In the second measurement stage, the EDA measurement is carried out in the "Measurement" tab.

EDA Configuration

The EDA configuration is used for EDA measurement. Significant samples must be averaged for a single EDA calculation to get a more constant value.

It is not important to obtain EDA values frequently, so a significant number of samples should be dropped to get a consistent result.

If the temperature changes, the temperature threshold triggers a recalibration alert. Therefore, the impedance scaling should be performed again.

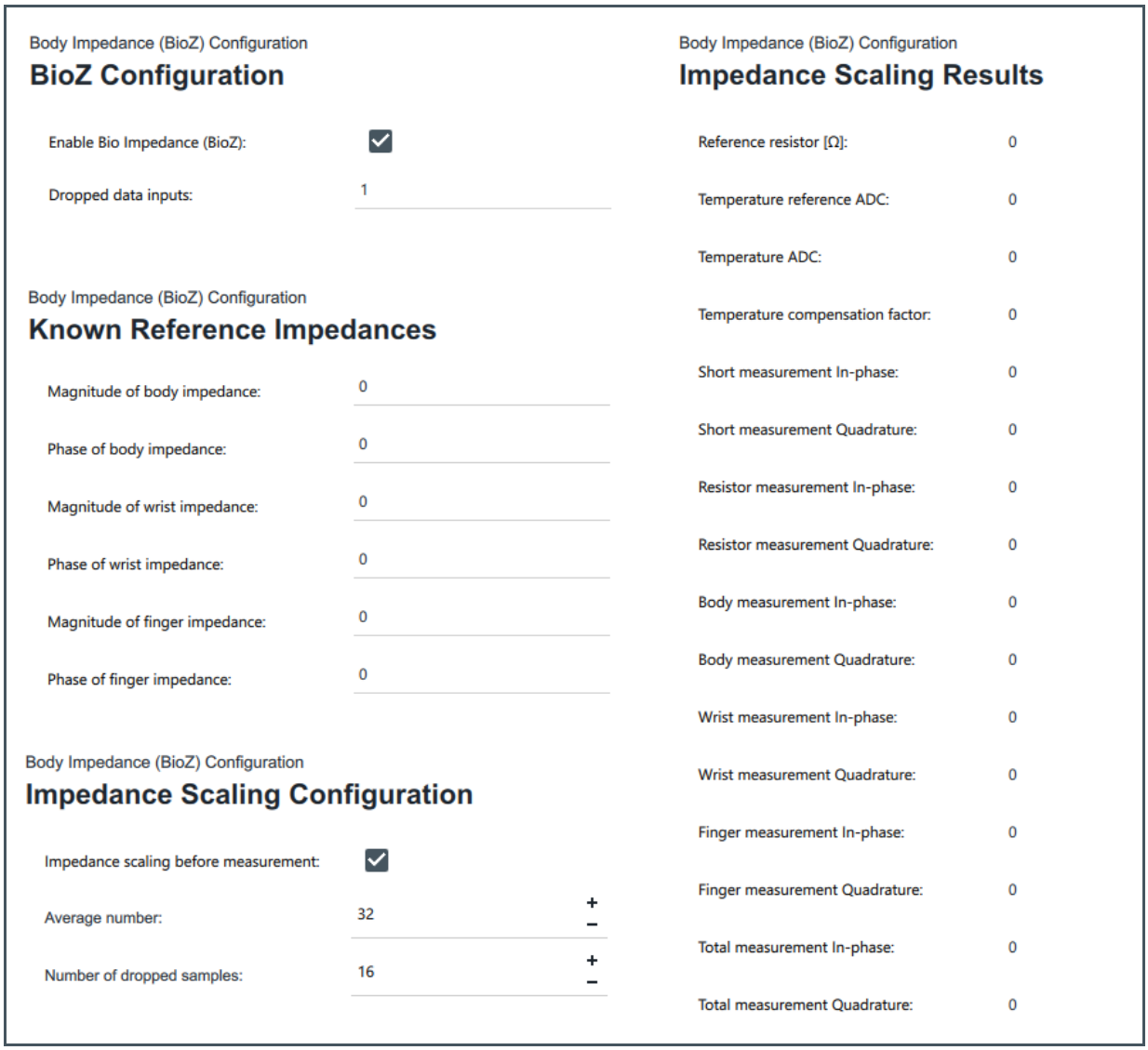
Signal Routing

EDA only needs to use one channel for signal routing. It must be configured on the ECG component. The signal routing temperature must also be configured for the EDA application.

5.4.13 Body Impedance (BioZ) & BioZ Measurement

The BioZ application block estimates the bioelectrical impedance of the body. The AS7058 supports BioZ measurement using a tetra polar electrode configuration. The measurement works by injecting sinusoidal electrical current via the low driving electrodes and measuring the potential difference using the two sensing electrodes. The software algorithm estimates the BioZ parameters, namely the magnitude of the electrical impedance and the phase angle, and the values are displayed in the GUI.

Figure 38:
BioZ Configuration



BioZ Configuration

BioZ configuration is for the BioZ measurement. To get a constant value, a significant number of samples should be dropped to get a consistent result.

Known Reference Impedance

A BioZ reference board for calibration and measurement is required to carry out the BioZ measurement. Also, the body, wrist, and finger impedance values of the BioZ reference board used for the calibration must be known.

Impedance Scaling Configuration

Before starting the impedance scaling, the average number and number of dropped samples need to be set, to get a definitive value.

Before starting the impedance scaling, the average sample number and the number of dropped samples must be set to get a definitive value.

Impedance Scaling Results

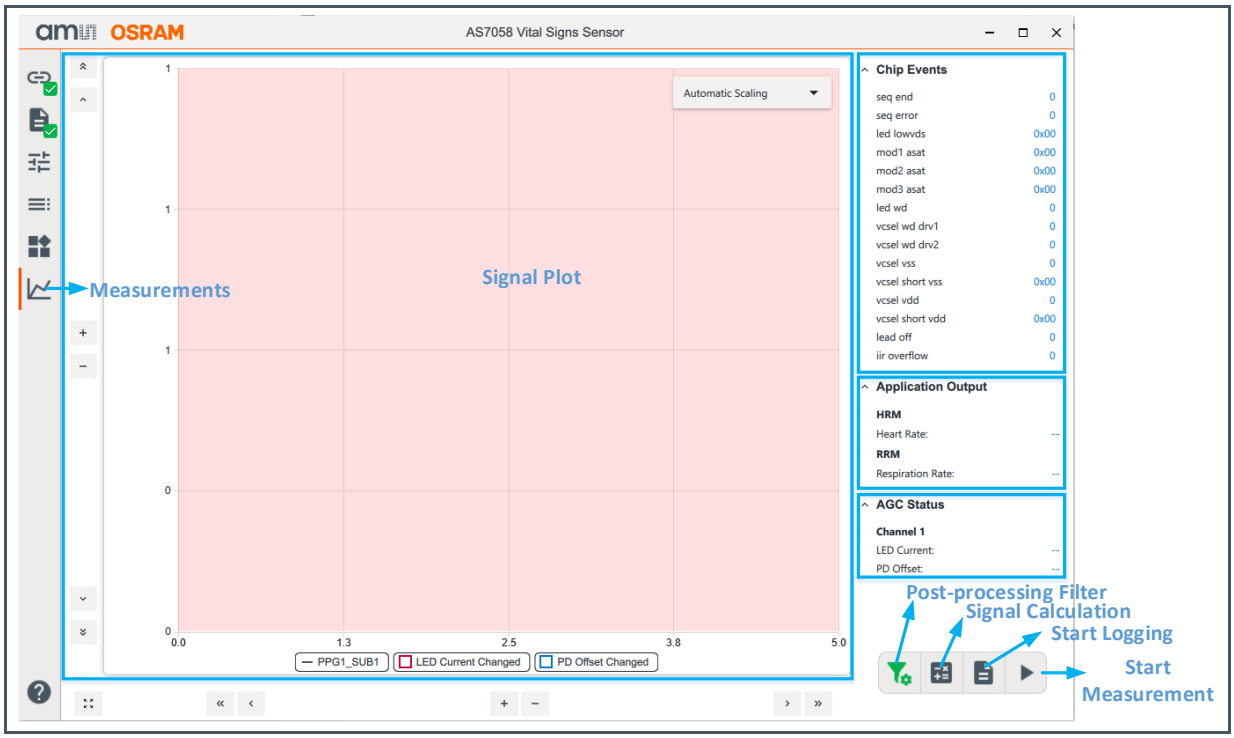
The BioZ works in two measuring stages. In the first measurement stage, the calibration is carried out using impedance scaling. This measurement mode measures different impedances by automatically reconfiguring the AS7058 AFE between each measurement. During this calibration stage, the BioZ reference board to be used for the calibration needs to be connected to the AS7058 EVK board.

In the second measurement stage, the BioZ measurement is carried out in the "Measurement" tab. During the second measurement stage, the BioZ reference board to be used for measurements must be connected to the AS7058 EVK board.

5.5 Measurements

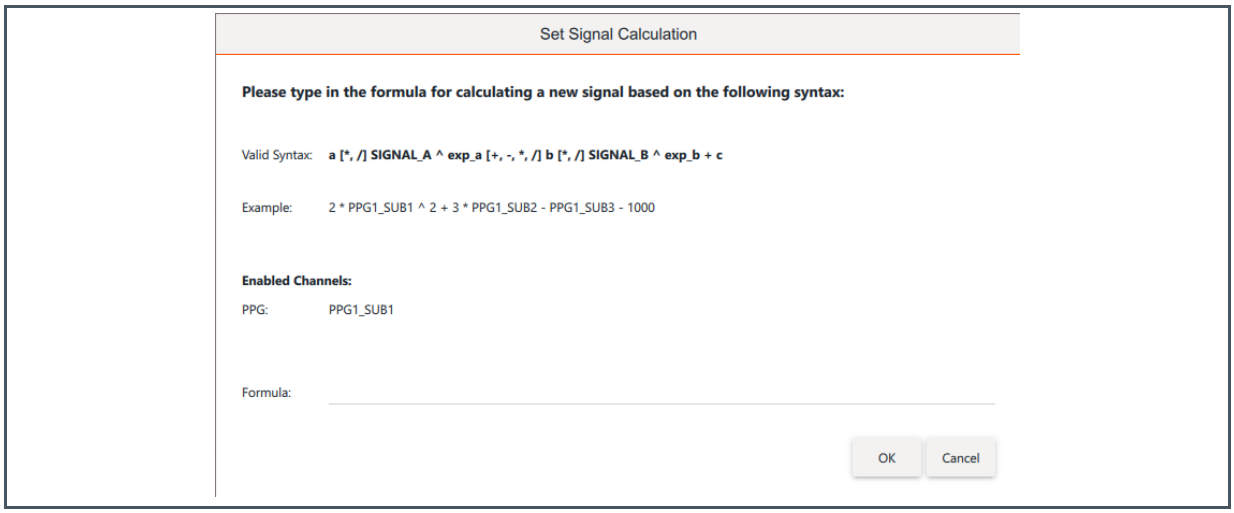
The measurement tab gives access to start and stop the continuous measurement, visualize the chip events, and check the application output and the AGC Status. The PPG ADC and ECG counts can also be displayed here.

Figure 39:
Measurement Tab Overview



- **Chip Event:** This shows the current values' Proximity, VCSEL/LED, MOD1, and MOD2. Sequence conditions can also be observed.
- **Application Output:** This shows the current Heart Rate, RRM, and SpO_2 values.
- **AGC Status:** The AGC status for the LED current and PD offset. It shows the change in information of the PD Offsets for channels A and B (at min, max, increased, decreased).
- **Signal Calculation:** It is possible to combine PPG signals & ECH signal with a mathematical formula. The formula can be typed in and activated by the Set Signal Calculation dialog. The new calculated signal will be shown together in the plot area, but they can be shifted to another plot area.

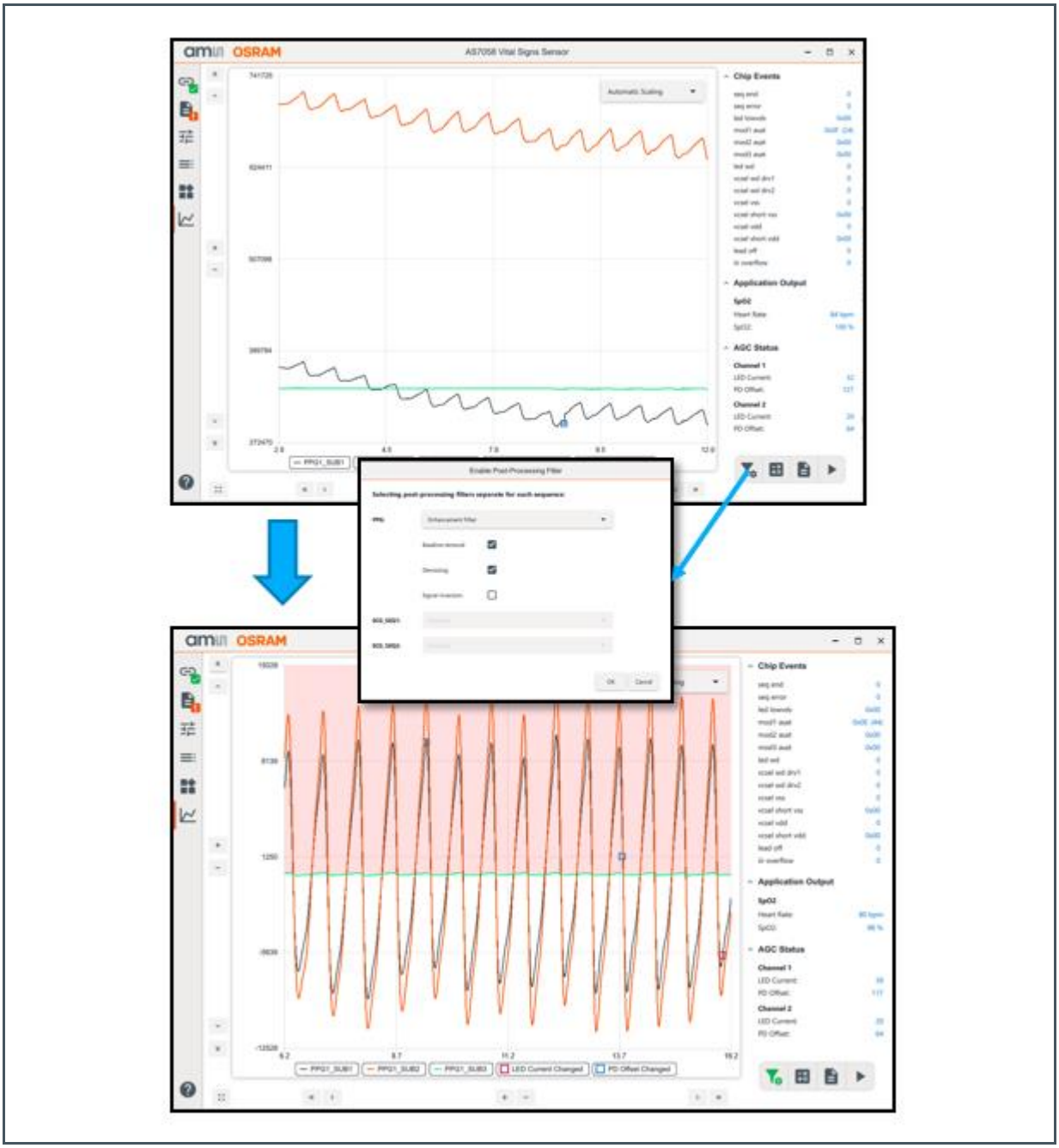
Figure 40:
Signal Calculation Tab



- **Post-processing:** A post-processing filter has been implemented to enhance the quality of a signal and reduce the noise levels. A moving average filter, Enhancement Filter, FIR filter, and IIR filter are implemented.

Enhancement Filter

Figure 41:
Enable Post-Processing Enhancement Filter



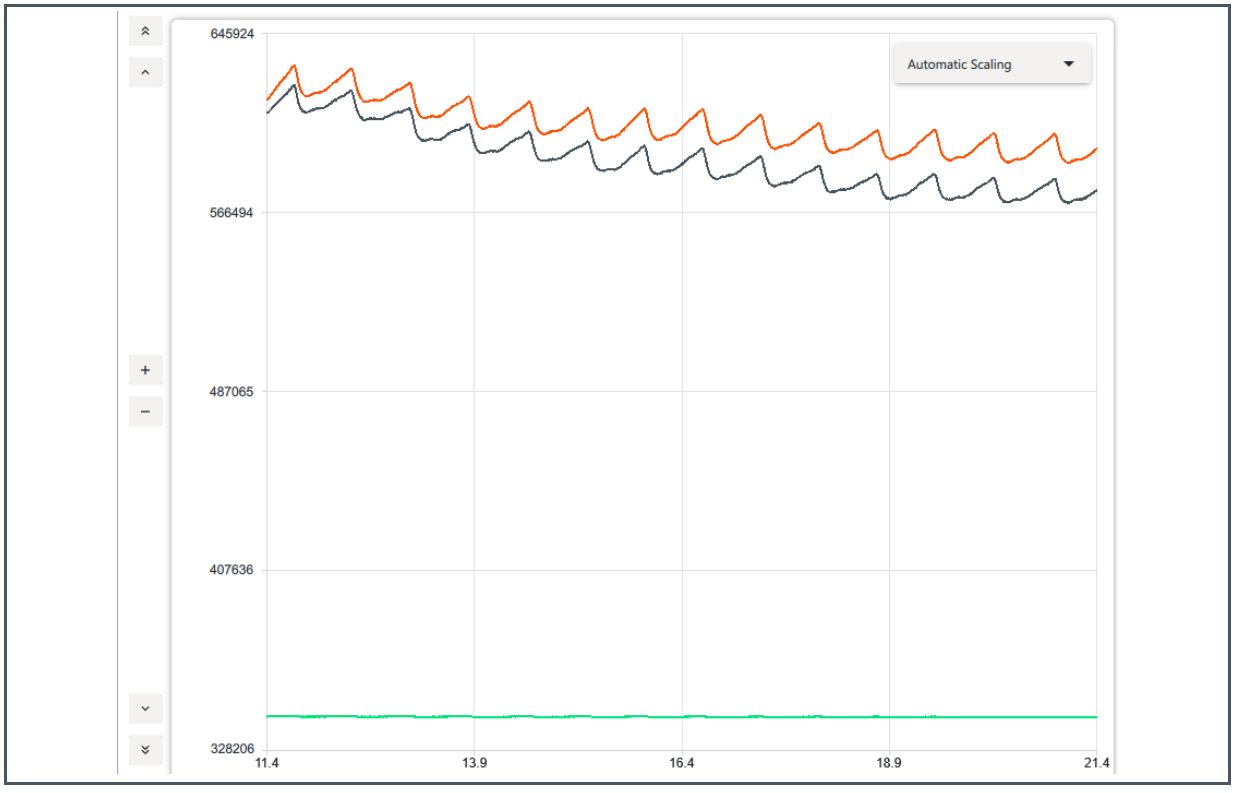
- The ECG and the PPG enhancement filters are provided for signal visualization.
- The ECG enhancement filter
  - Works for every possible sampling frequency starting with 100 Hz. The filter was tested with sampling frequencies in the range of 100…4000 Hz

    - Allows to reduce noise and AC power line interferences and to remove baseline wander. The filtered signal can be inverted. All filter stages can be enabled or disabled independently.
  - The PPG enhancement filter
    - Works for every possible sampling frequency starting with 20 Hz. The filter was tested with sampling frequencies in the range of 20…400 Hz
    - Allows to reduce noise and to remove baseline wander. The filtered signal can be inverted. All filter stages can be enabled or disabled independently.
    - Prevents signal ringing or other filter settling artifacts on signal discontinuities caused by LED current and/or PD offset current changes. If baseline wander removal is enabled, signal discontinuities will be compensated so that the signal segments are connected seamlessly.
- **Measurement button:** A button for starting and stopping the measurement.
  - “Start Measurement”
  - “Stop Measurement”
- **Plot area:** This displays the signals up to three plots.

Plotting

The user interface provides a few functions and signals that are displayed in the plot area.

Figure 42:
Plotting



When “Automatic Scaling” is enabled, the display automatically sets the minimum and maximum values of the y-axis. The minimum and maximum values of the x-axis are automatically set.

Figure 43:
Selection of Plotting Area

The display area can plot a maximum of three plots for a signal. By default, the plot area displays all the signals in one plot. By left-clicking on the channel name in the legend, a dialog box will open to represent the signal in another plot area, as shown in Figure 43. The plot area contains a few functions for automatic scaling, manual scaling, and zooming.

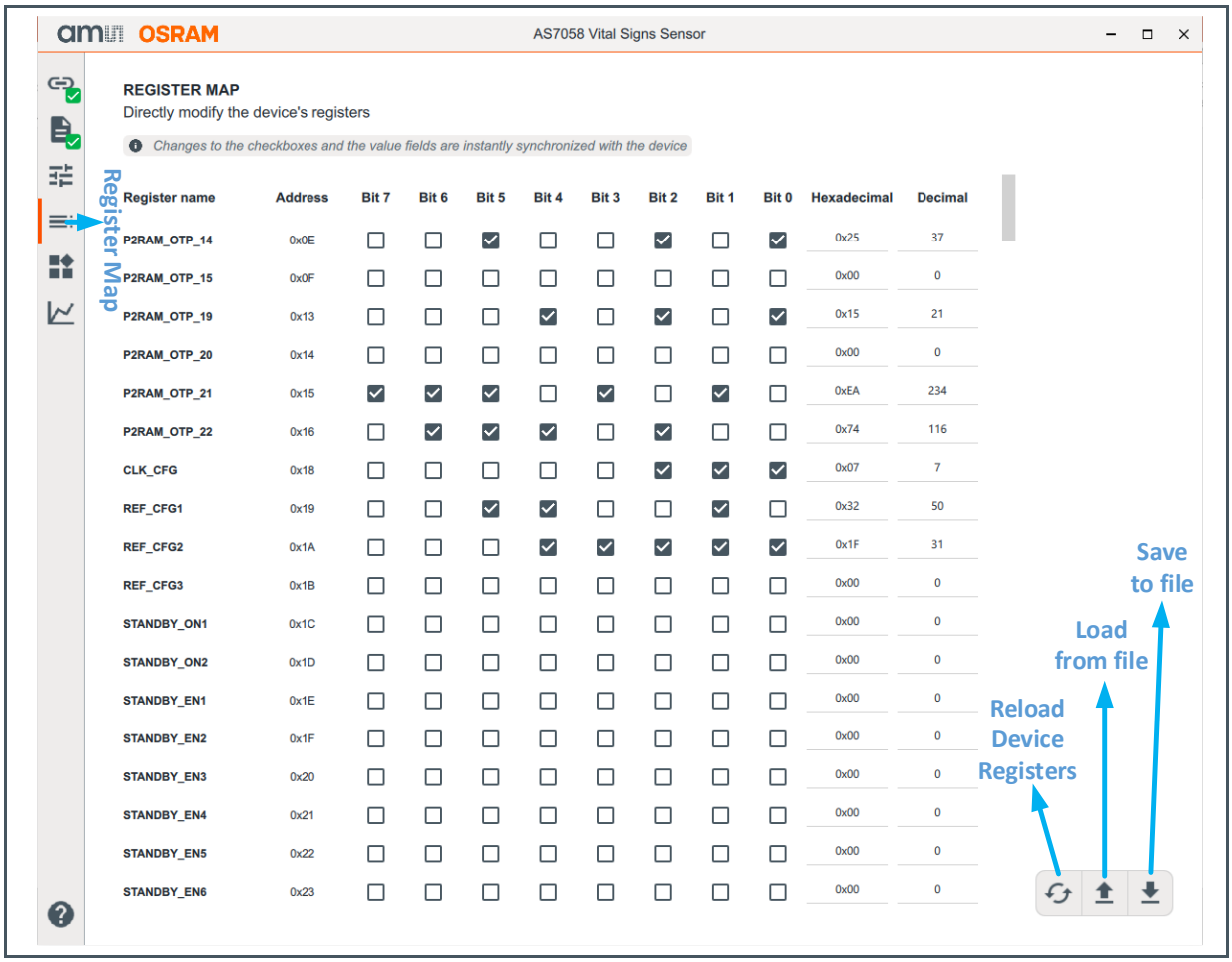
5.6 Register Map

The “Register Map” window is used to view/change the contents of the complete set of the AS7058 user register. To check the current register map, click on the tab “Register Map” as shown in Figure 44.

- In the Register Map window:
  - The register values can be updated.
  - New register values can be entered.

- To save the current register map, click on “Register Export”. This will open the Save dialog box. Enter a file name, choose the file location, and save it as a CSV file. Click “Save” to save the file.
- To load a new register list (CSV file), click “Register Import”. This will open the Open dialog box. Select the CSV file you want to load, and click Open.

Figure 44:
Register Map List



5.7 Saving the Current Configuration Settings to a File

The current configuration settings can be exported to a file. To save the current configuration settings, click “Save Configuration”, as shown in Figure 11. This will open the Save Configuration File dialog box. Enter a file name, choose the file location, and save it as a JSON file. Finally, click “Save” to save the file.

5.8 Loading Configuration Settings from a File

To load a previously exported configuration (JSON file), click “Load Configuration” as shown in Figure 11. This will open the Select Configuration File dialog box. Select the JSON configuration file you want to load, and click Open.

The settings imported from the file can be reviewed in the relevant configuration windows.

If the GUI is connected to the board, the newly imported settings will be applied immediately; otherwise, upon successful connection to the board.

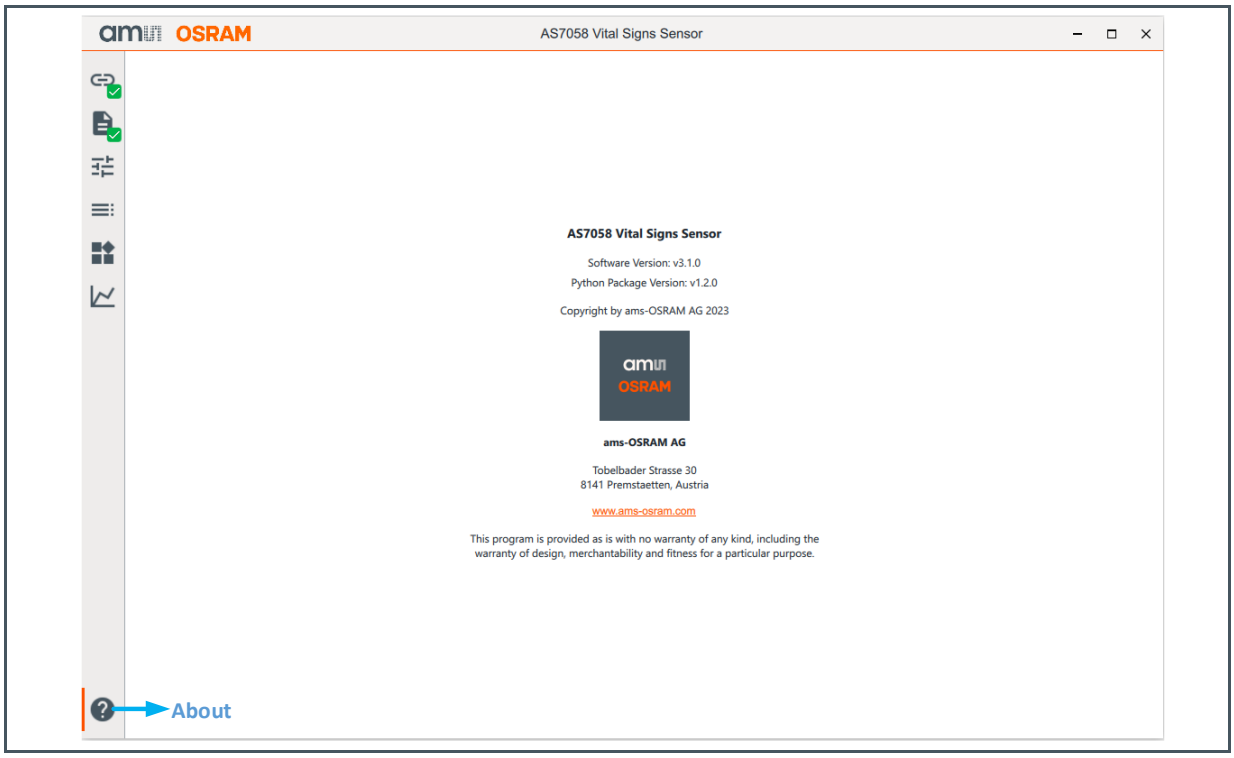
5.9 Raw Data Logging and Exporting

Before starting the measurement by clicking “Start measurement”, click “Start Logging” as shown in Figure 39, to save the raw data from the AS7058. A pop-up window will appear for selecting the file location and saving the CSV file. When a measurement is stopped with the “Stop measurement” button, click “Stop Logging” afterward.

5.10 About Tab

As shown in Figure 45, the “About tab” provides the software name, software version number, python package version number, and copyright with the company link.

Figure 45:
About Tab

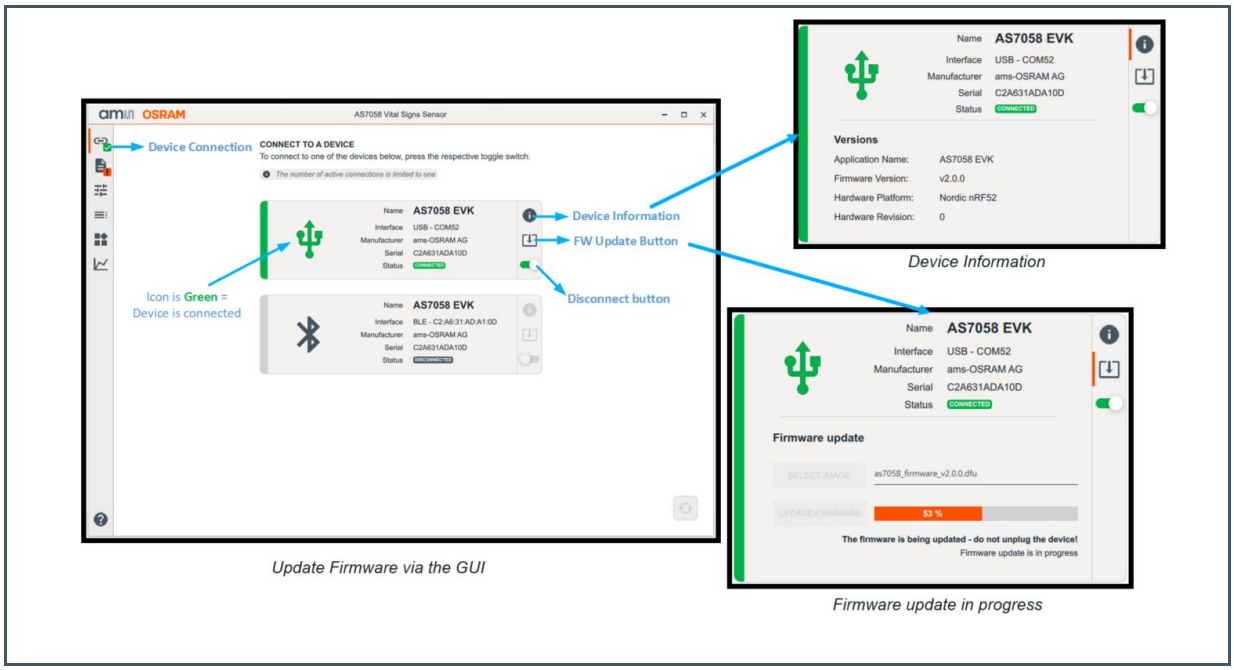


5.11 Firmware Update

There is an option to upgrade the firmware (FW). To achieve this, perform the following steps:

1. Obtain the latest "*.dfu" firmware file from ams OSRAM.
2. Click on the tab Device Connection → Firmware Update → SELECT IMAGE … to navigate to the "*.dfu" file (latest firmware file) → click UPDATE FIRMWARE.

Figure 46:
Firmware Update



3. During the update process, the green LED on the Bluetooth module will turn red and then multicolored.
4. After a successful update, the red and multicolored LED will turn green again.

6 Customized Settings from the Configuration Presets

Some configuration presets are provided for a user to quickly start using the device. However, it is possible to access all the parameters, create a custom configuration file, and save it for further access.

The default configuration files are based on the AS7058 EVK with the fingers as the target position. Therefore, a custom configuration is required when there is new hardware or optical design and the target position is a different body part such as the wrist, upper arm, peaches, etc.

To create a custom configuration file, the following parameters must be checked and set:

- ✔ AGC algorithm, LED current, ADC full scale, DAC full scale, LED numbers, PD numbers, Integration time, Sample rate, sub-samples, ECG, BioZ, signal post-processing, FIFO size, filters, algorithms, etc.

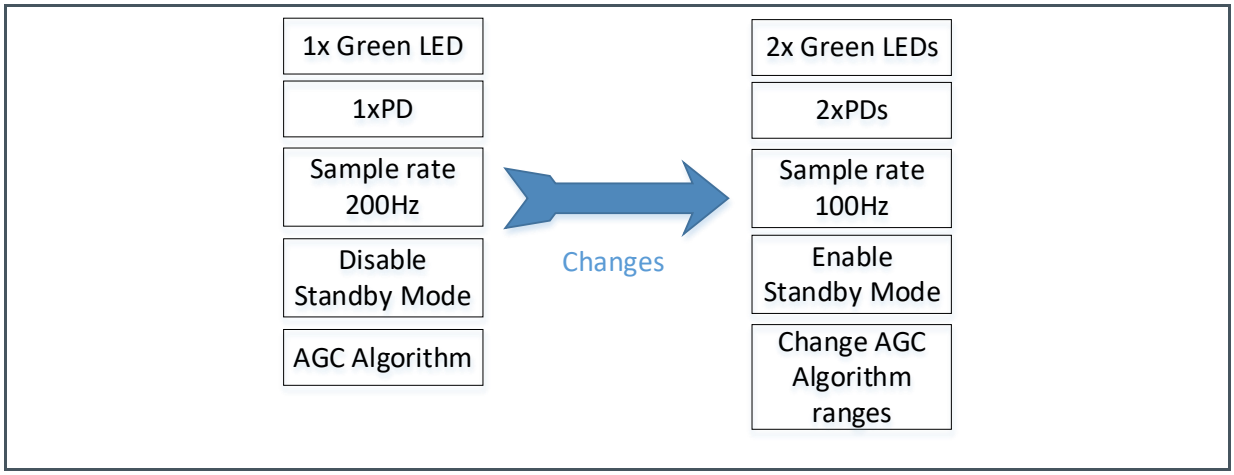
Information

These examples are for demonstration purposes only to show the user how to change the parameters of the existing configuration presets and create a new configuration JSON file.

6.1.1 Changing the HRM Parameters

This example provides a systematic configuration of how to create a new HRM configuration file.

Figure 47:
HRM Configuration

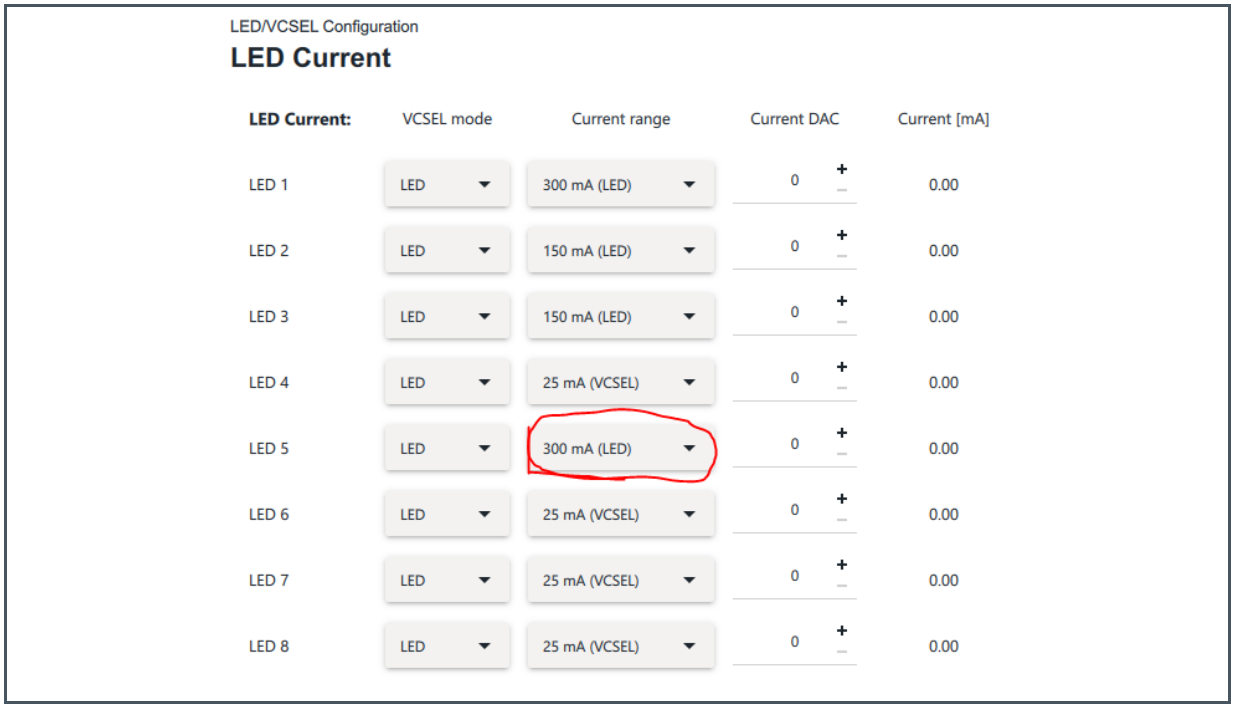


Step 1

There are two green LEDs on the optical part of the AS7058 EVK, but only one green LED was used for the HRM configuration. Then, two green LEDs are activated, as shown below in Figure 48:

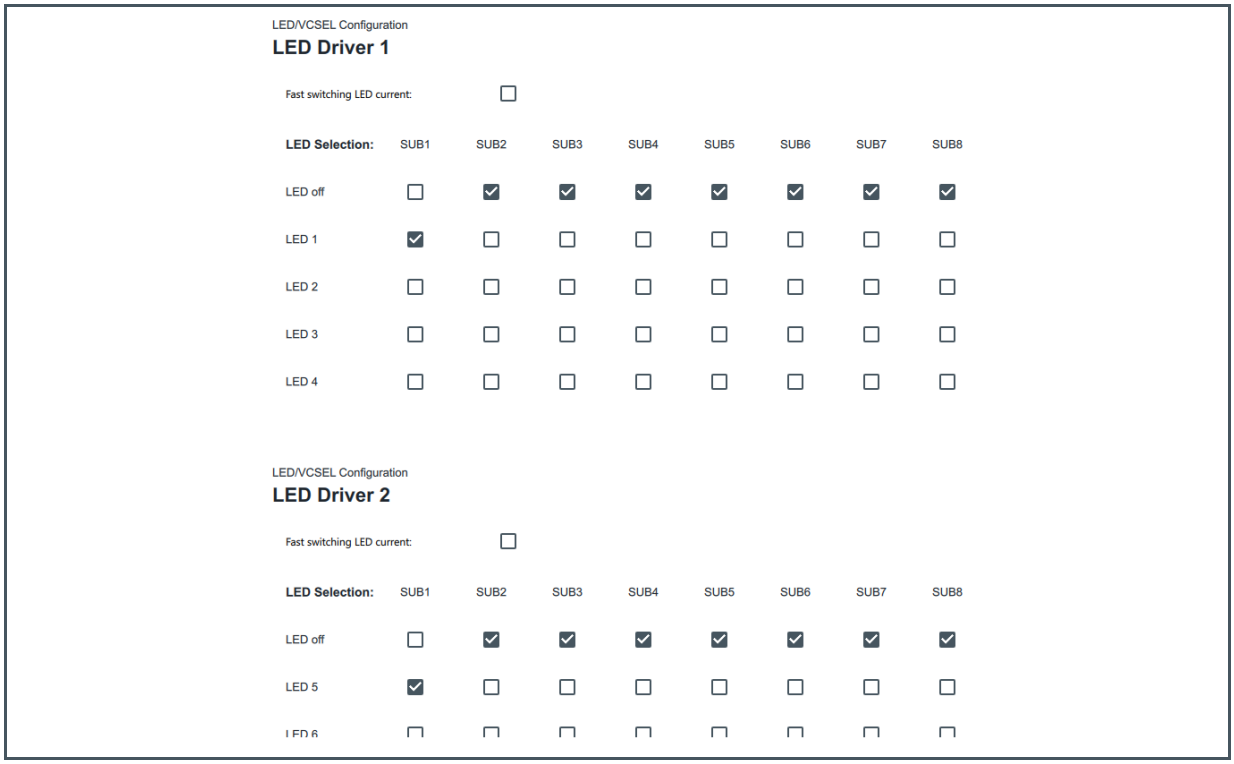
1. Select the “AS7058 EVK: HRM & RRM” configuration preset.
2. Afterward, go to “Sensor Configuration” => click on the “LED configuration” block => LED1 under “LED Current” will already be set to 300 mA => Set LED5 to 300 mA current range, as shown in Figure 48.

Figure 48:
LED Current for HRM



3. LED1 under “LED Driver1” will already be selected => Select LED5 under “LED Driver2”, as shown below in Figure 49.
4. There is no need to change the LED current since the AGC algorithm has been used for HRM to control the LED current.

Figure 49:
Enable LEDs for HRM



Step 2

There are two broadband PDs on the optical part of the AS7058 EVK, but only one PD was used for the HRM configuration. Here, two PDs are activated.

- Click on the “Photodiodes” block => PD2 under “PPG1 – PD Selection” will already be selected => Select PD5, as shown below in Figure 50.

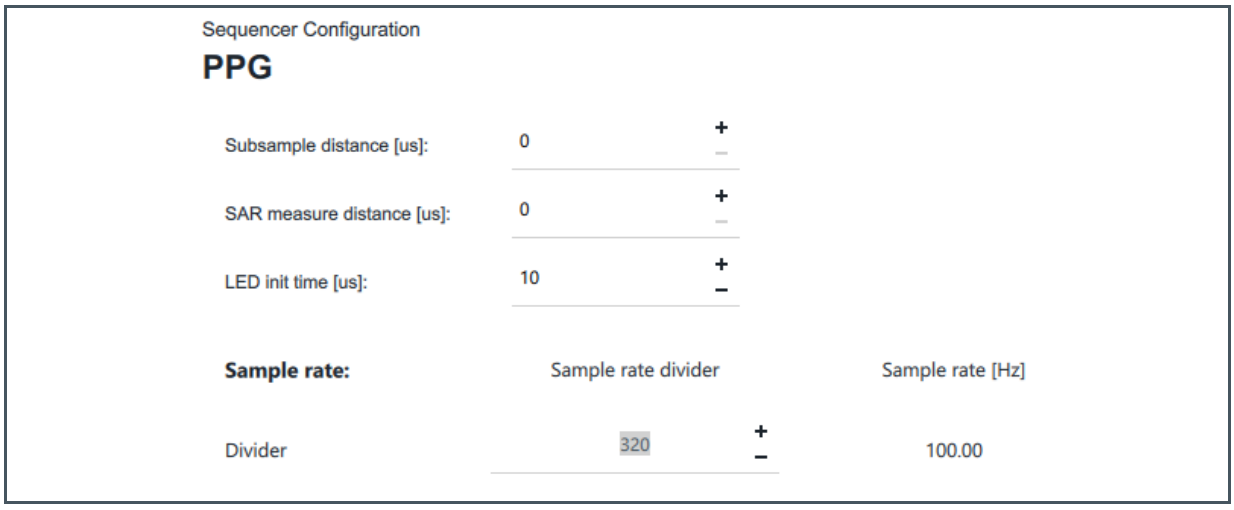
Figure 50:
PD Selection for HRM

Step 3

In the preset HRM configuration file, the sampling frequency is set to 200 Hz. Here, it is set to 100 Hz as shown below in Figure 51.

- Click on the “Sequencer” block => change the divider from 160 to 320, to set 100 Hz from 200 Hz under “PPG – Sample rate”, as shown below in Figure 51.

Figure 51:
Sequencer Setup for HRM

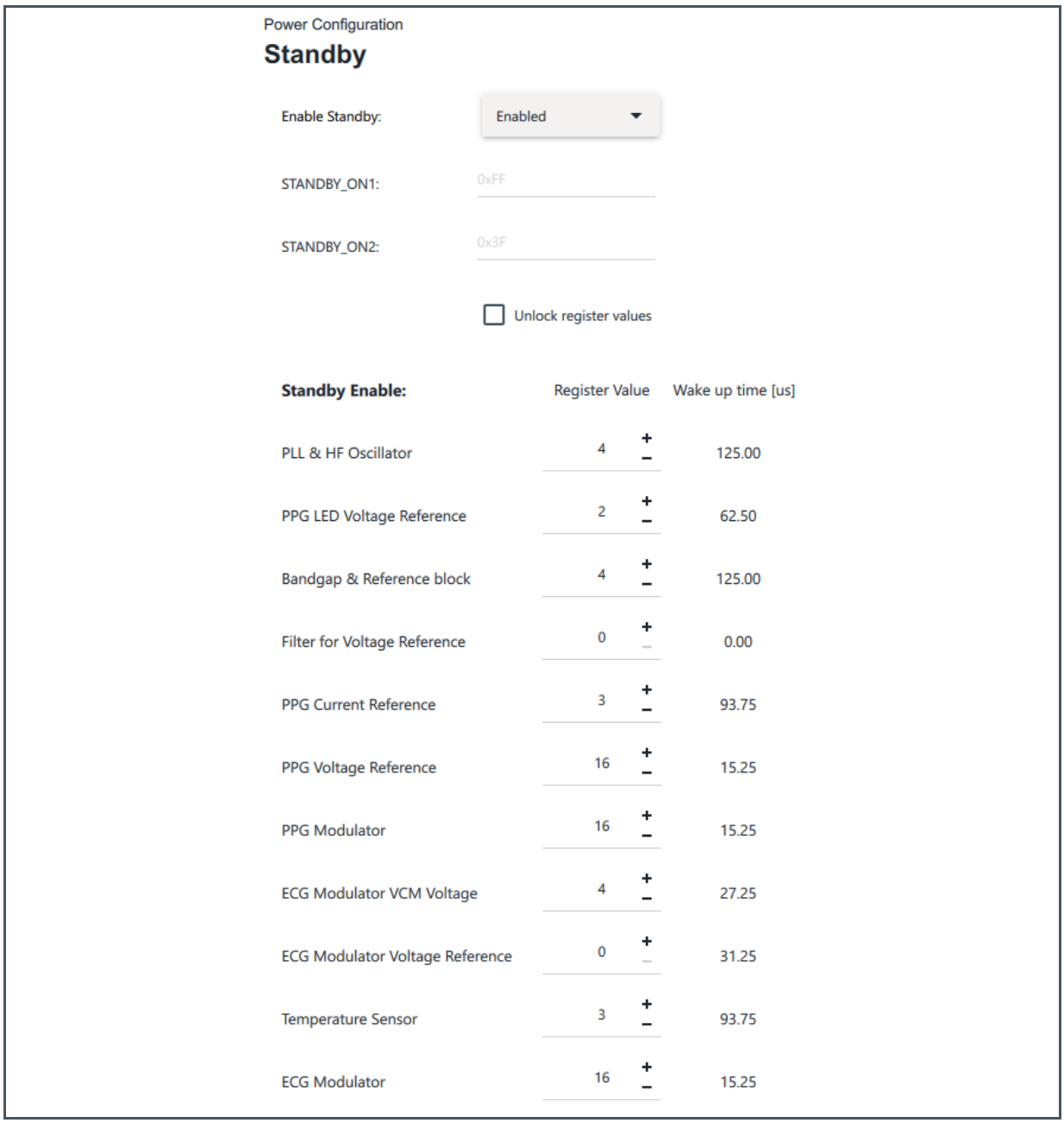


Step 4

Enable standby mode to reduce the power consumption.

- Click on the “Power” block => Enable “Standby” under “Power Configuration - Standby”, as shown in Figure 52.

Figure 52:
Standby Mode for HRM

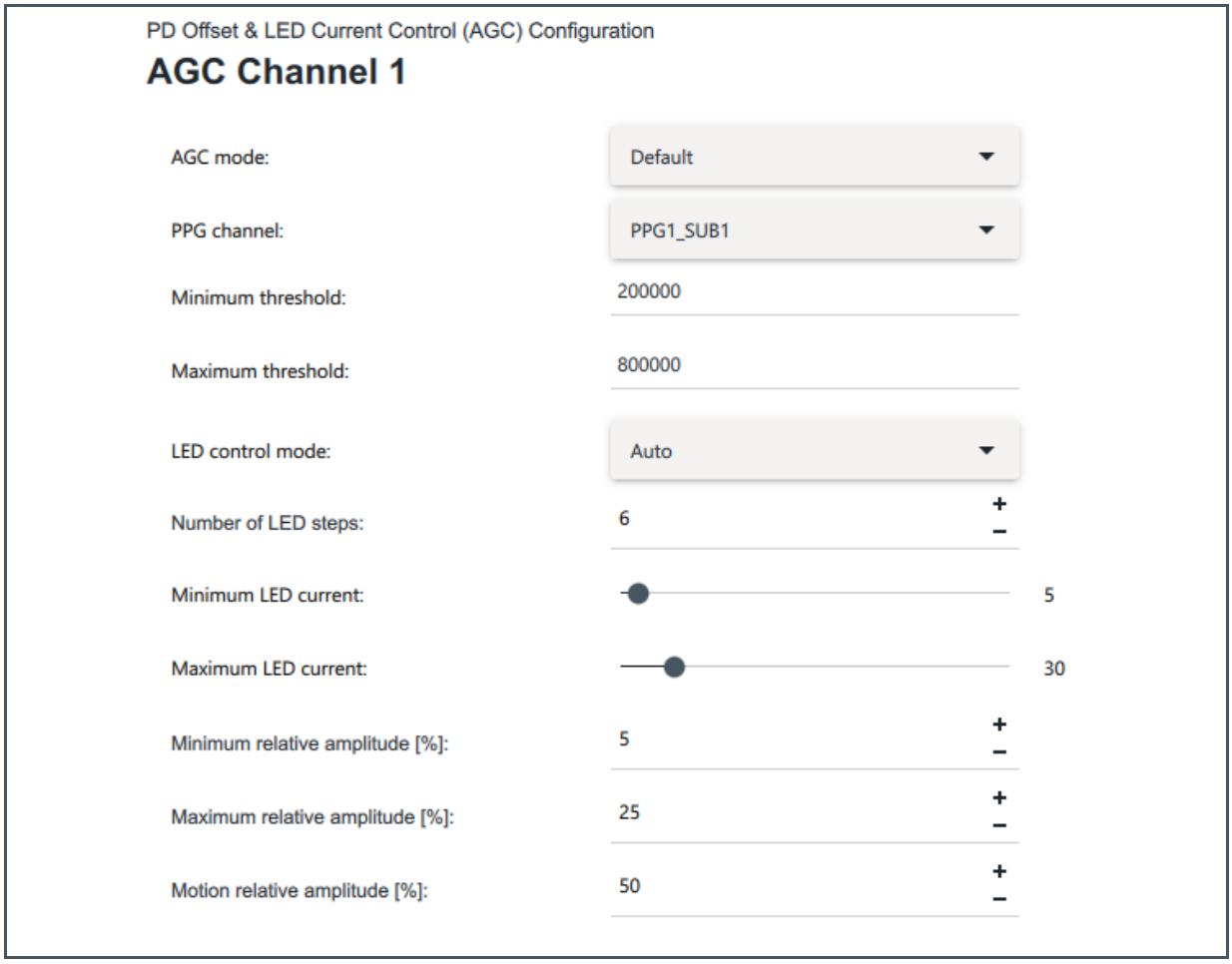


Step 5

Change the AGC current range.

1. Go to “Applications” => click on the “Software AGC” => Change the “Minimum threshold” & “Maximum threshold”, also, change “Minimum LED current” & “Maximum LED current”, as shown in Figure 53.

Figure 53:
AGC Algorithm for HRM



2. Save the new configuration file.
3. Afterward, start the measurement.

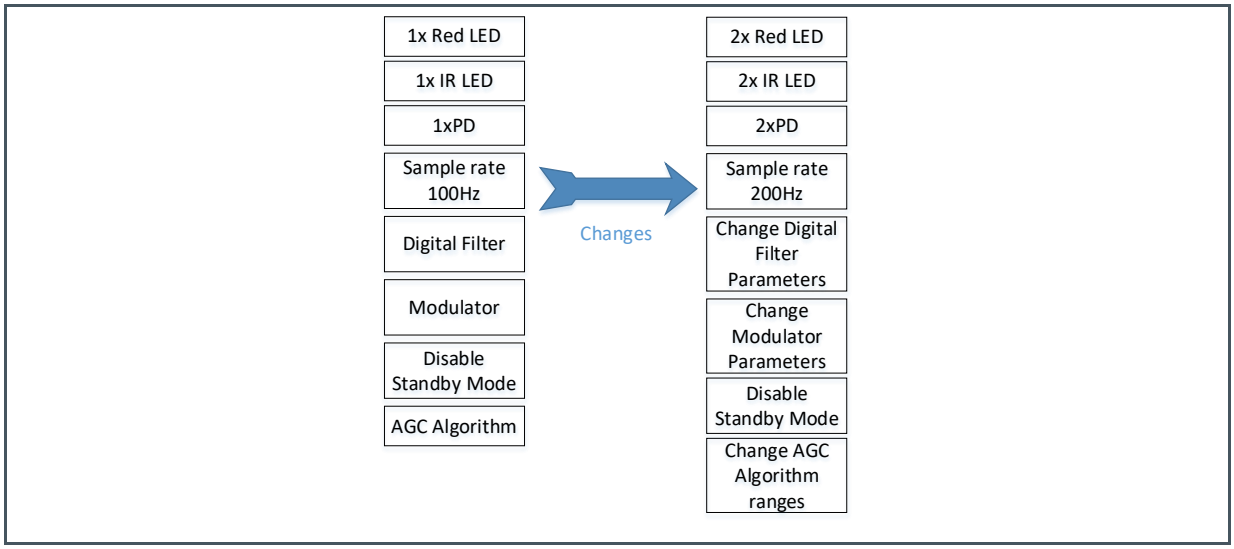
Information

This example is for demonstration purposes only to show the user how to change the parameters of the existing configuration presets.

6.1.2 Changing the SpO_2 Parameters

This example provides a step-by-step configuration for creating a new SpO_2 configuration file.

Figure 54:
SpO_2 Configuration

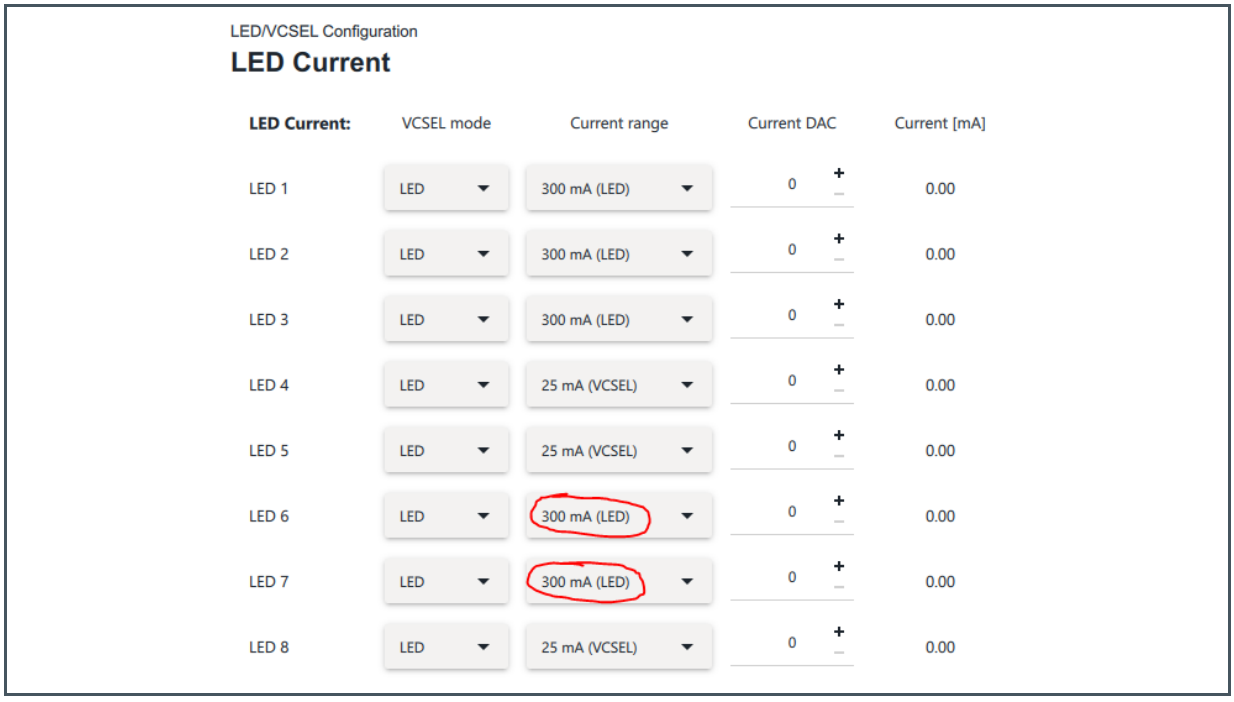


Step 1

There are two red and IR LEDs on the optical part of the AS7058 EVK, but only one red and IR LED was used for the SpO_2 configuration. Afterward, two red and IR LEDs are activated, as shown in Figure 55.

1. Select the “AS7058 EVK: SpO_2 100 Hz on finger” configuration preset.
2. Afterward, go to “Sensor Configuration” => click on the “LED configuration” block => LED2 & LED3 under “LED Current” are already set to 300 mA => Set LED6 & LED7 to 150 mA current range, as shown below in Figure 55.

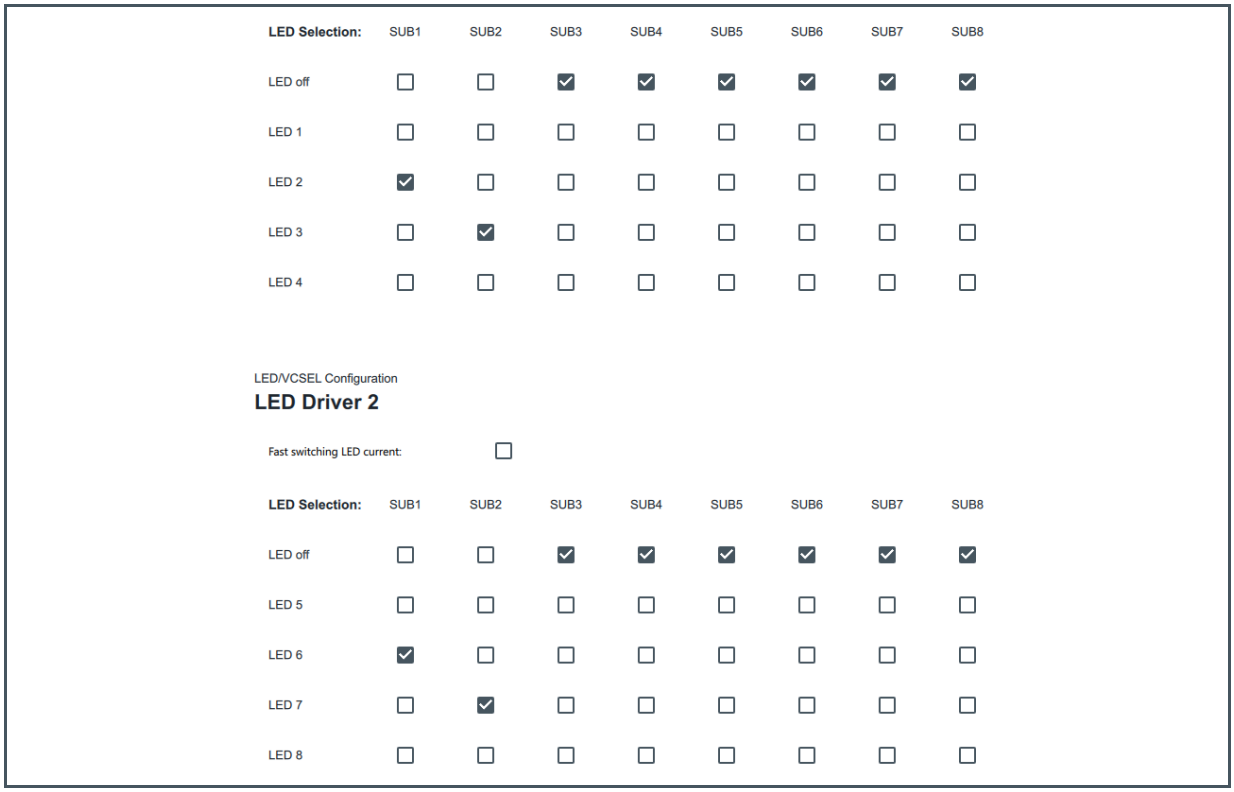
Figure 55:
LED Current Selection for SpO_2



3. LED2 and LED3 under “LED Driver1” will already be selected => Select LED6 & LED7 under “LED Driver2”, as shown in Figure 56.

4. There is no need to change the LED current since the AGC algorithm has been used for SpO_2 to control the LED current.

Figure 56:
Enabling LEDs for SpO_2



Step 2

There are two broadband PDs on the optical part of the AS7058 EVK, but only one PD was used for the SpO_2 configuration. Here, two PDs are activated.

- Click on the “Photodiodes” block => PD2 under “PPG1 – PD Selection” is already selected => Select PD5 for three subsamples, as shown below in Figure 57.

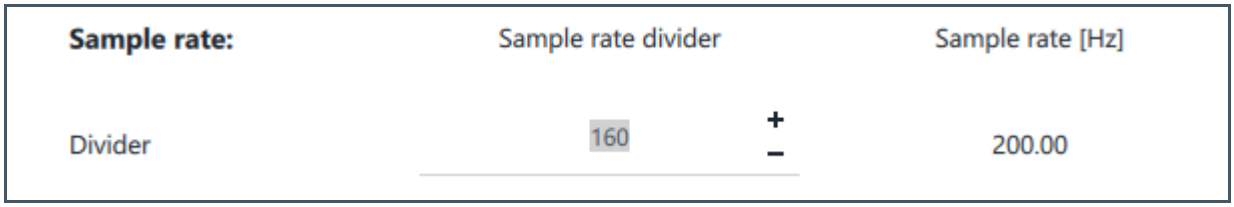
Figure 57:
PD Selection for SpO_2

Step 3

In the preset SpO_2 configuration file, the sampling frequency is set to 100 Hz. Here, it is set to 100 Hz as shown in Figure 58.

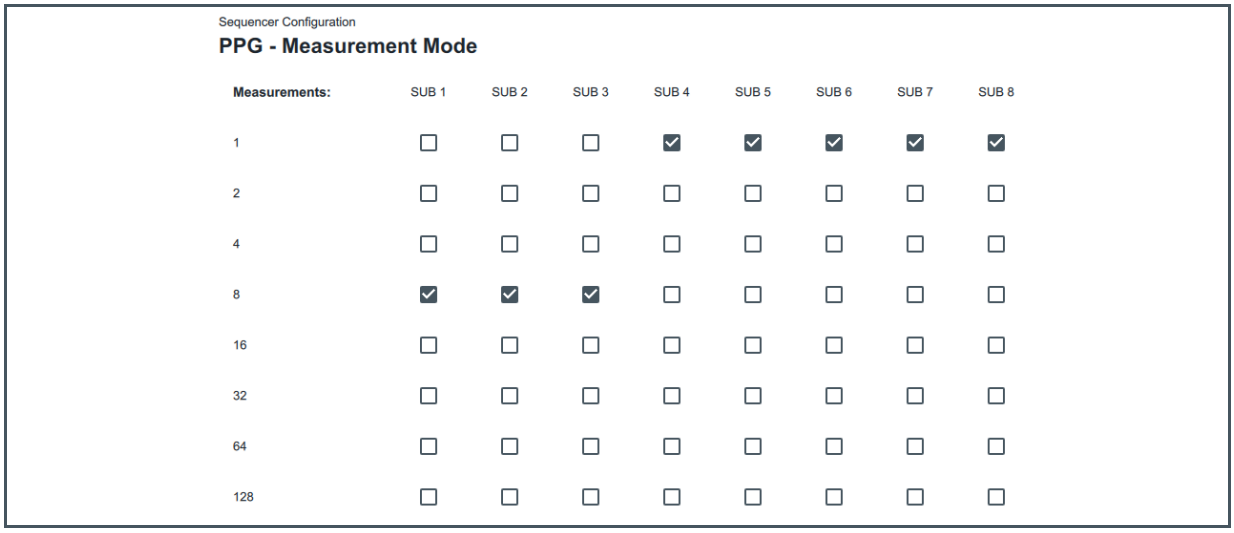
1. Click on the “Sequencer” block => change the divider from 320 to 160, to set 200 Hz from 100 Hz under “PPG – Sample rate”, as shown below in Figure 58.

Figure 58:
Sequencer Setup for SpO_2



2. Execution of each subsample after an average of 8.
3. “PPG – Measurement Mode” => Select number of measurement 8 for SUB1, SUB2 and SUB3, as shown in Figure 59.

Figure 59:
PPG – Measurement Mode for SpO_2

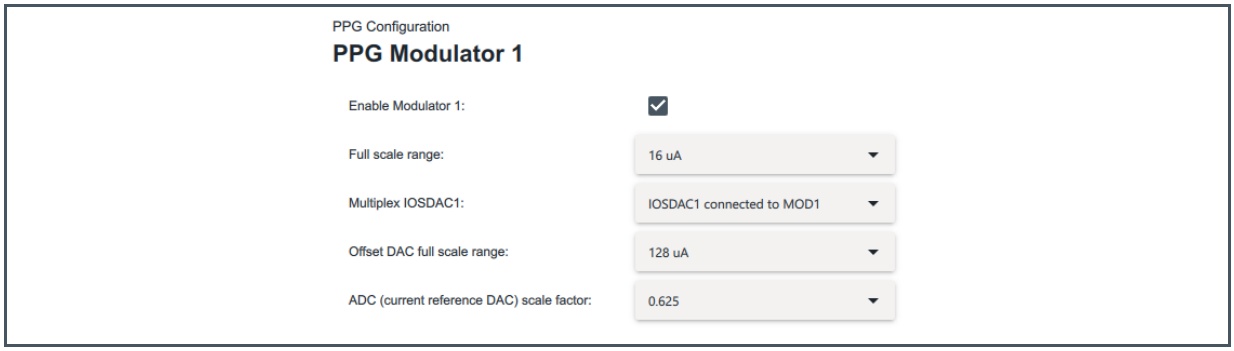


Step 4

The PPG ADC Input full-scale and reference offset DAC current were programmed for the SpO_2 finger measurement. Here, another full-scale is set as shown below in Figure 60.

- Click on the “PPG” block => change the “Full scale range” 8 µA to 16 µA and change the “Offset DAC full scale current” 64 µA to 128 µA under “PPG Modulator 1”, as shown in Figure 60.

Figure 60:
PPG Modulator for SpO_2

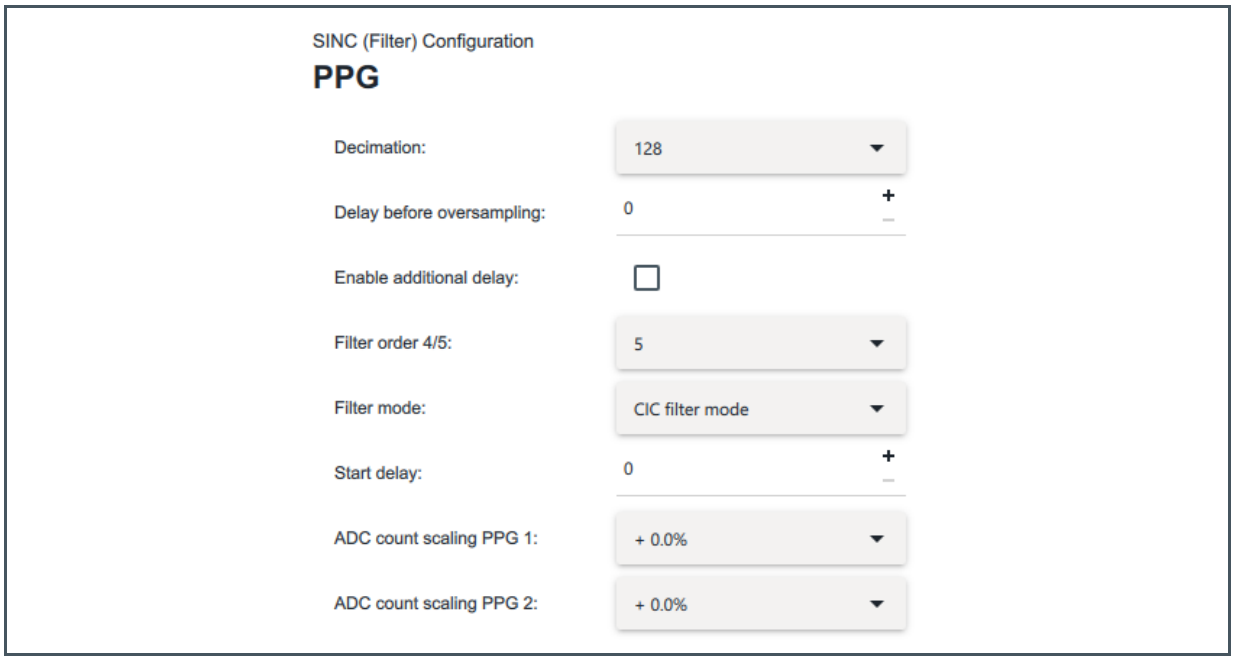


Step 5

The following can be flexibly configured with the digital filter: filter type, filter order, and filter decimation rate. The configuration of the digital filter results in a different ADC conversion time or integration time.

- Click on the “Filter (SINC)” block => change the “Decimation” from 256 to 128 under “PPG”, as shown in Figure 61.

Figure 61:
Digital Filter for SpO_2

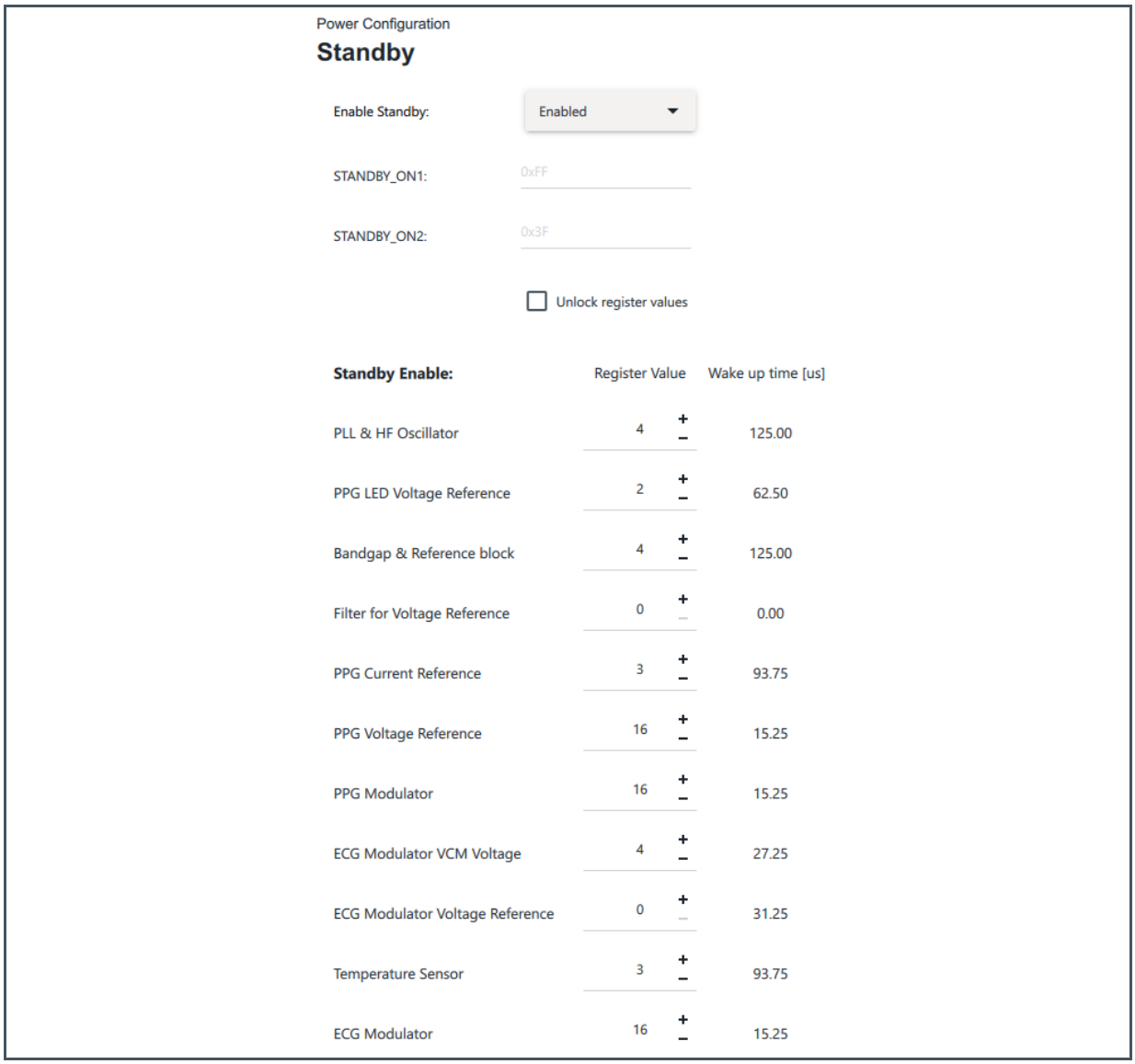


Step 6

Enable the standby mode to reduce the power consumption.

- Click on the “Power” block => Enable “Standby” under “Power Configuration - Standby”, as shown Figure 62.

Figure 62:
Standby Mode for SpO_2



Step 7

Change the AGC current range.

1. Go to “Applications” => click on the “PD Offset & LED Control (AGC)” => Change the “Minimum threshold” & “Maximum threshold”, also change “Minimum LED current” & “Maximum LED current”, as shown in Figure 63.

Figure 63:
AGC Algorithm for SpO_2

2. Save the new configuration file.
3. Afterward, start the measurement.

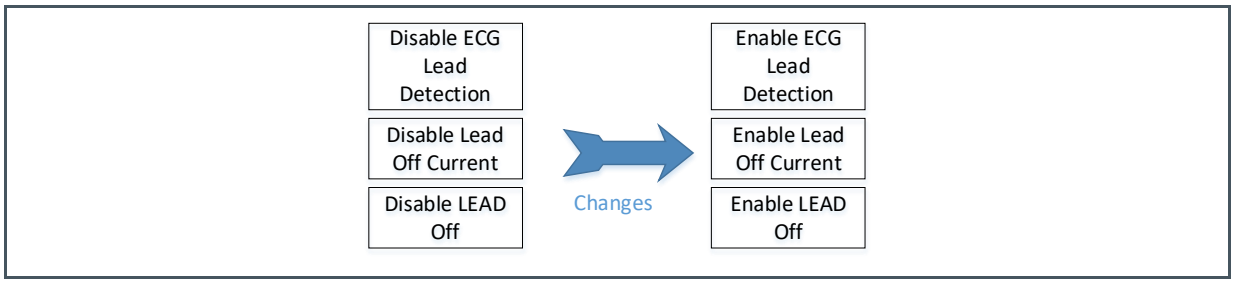
Information

This example is for demonstration purposes only to show the user how to change the parameters of the existing configuration presets.

6.1.3 Changing the ECG Parameters

This example provides a step-by-step configuration of how to create a anew ECG configuration file.

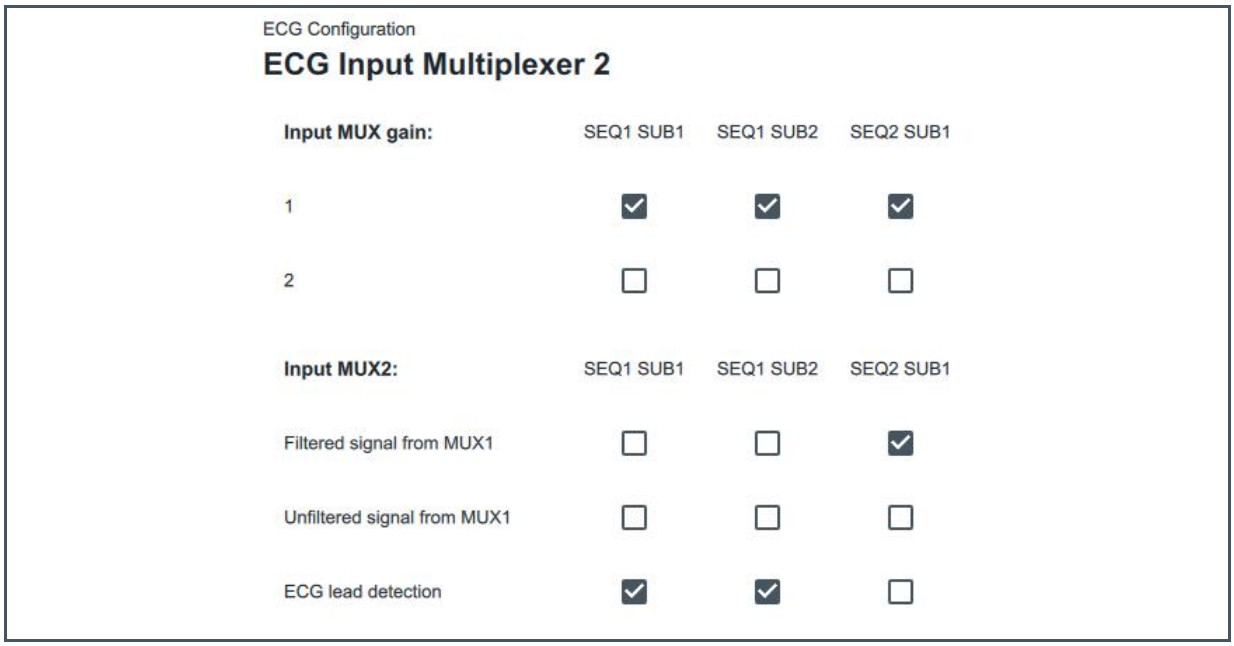
Figure 64:
ECG Configuration



The ECG configuration preset does not use the LEAD off function. Here, the LEAD off detection will be activated as listed below.

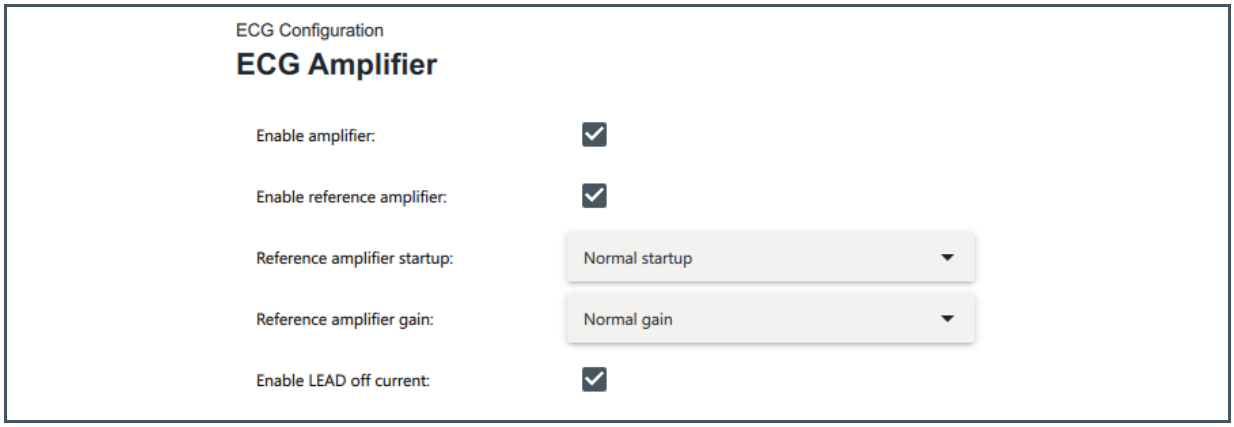
1. Select the “AS7058 EVK: ECG 1 kHz” configuration preset.
2. Afterward, go to “Sensor Configuration” => click on the “ECG” block => Enable “ECG lead detection” for “SEQ1 SUB1” and “SEQ1 SUB2” under “ECG Input Multiplexer 2 – Input MAX2”, as shown in Figure 65.

Figure 65:
ECG Lead Detection



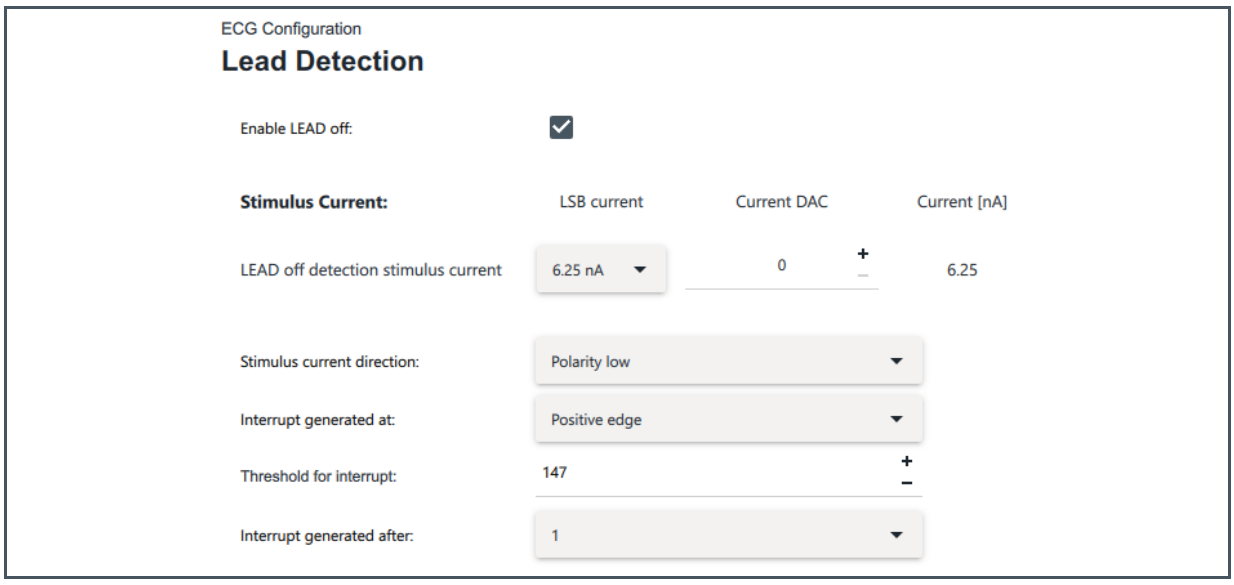
3. Enable “ECG LEAD off current” under “ECG Amplifier” as shown in Figure 66.

Figure 66:
ECG Lead-off Current



4. Enable “ECG LEAD off” under “Lead Detection” as shown in Figure 67.
5. Change to “Positive edge” for “Interrupt generated at”.
6. Put a specific value in the “Threshold for Interrupt”.

Figure 67:
LEAD off



7. Save the new configuration file.
8. Afterward, start the measurement.

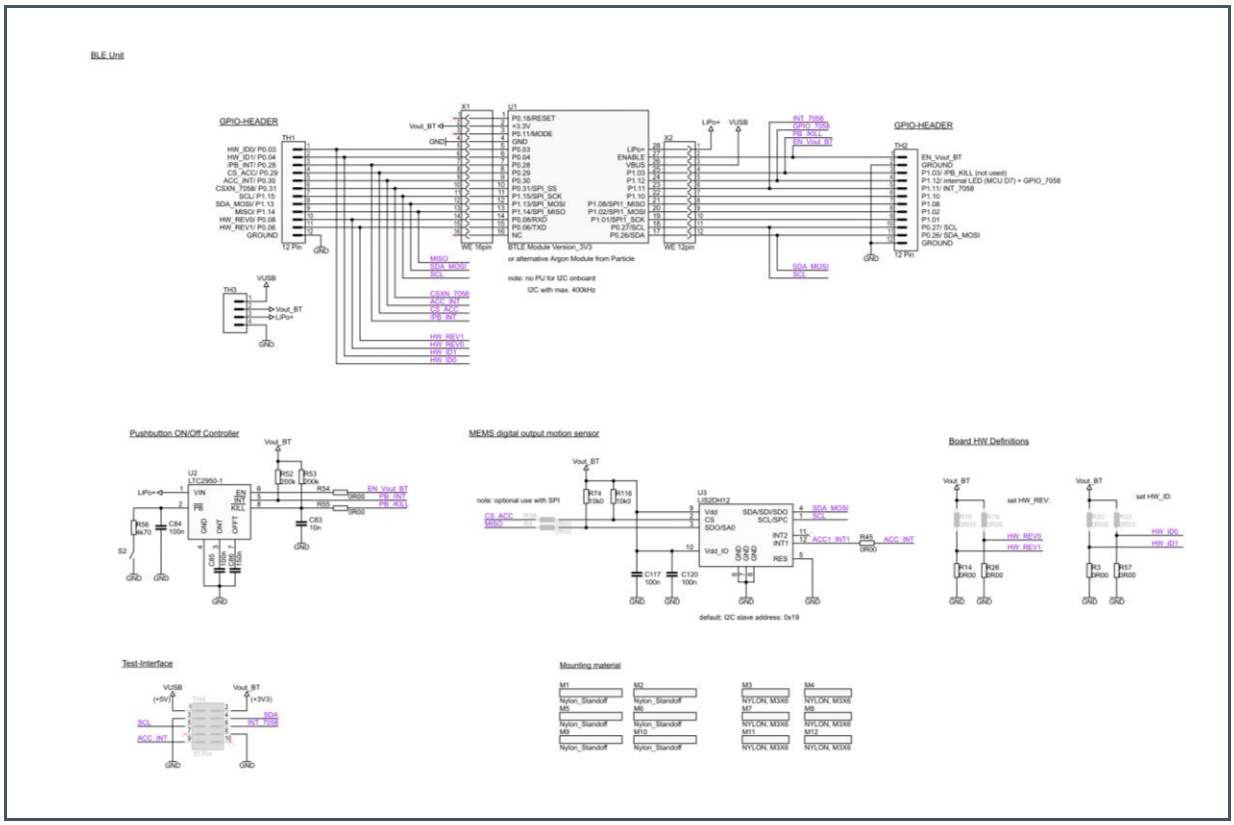
Information

This example is for demonstration purposes only to show the user how to change the parameters of the existing configuration presets.

7 Schematics

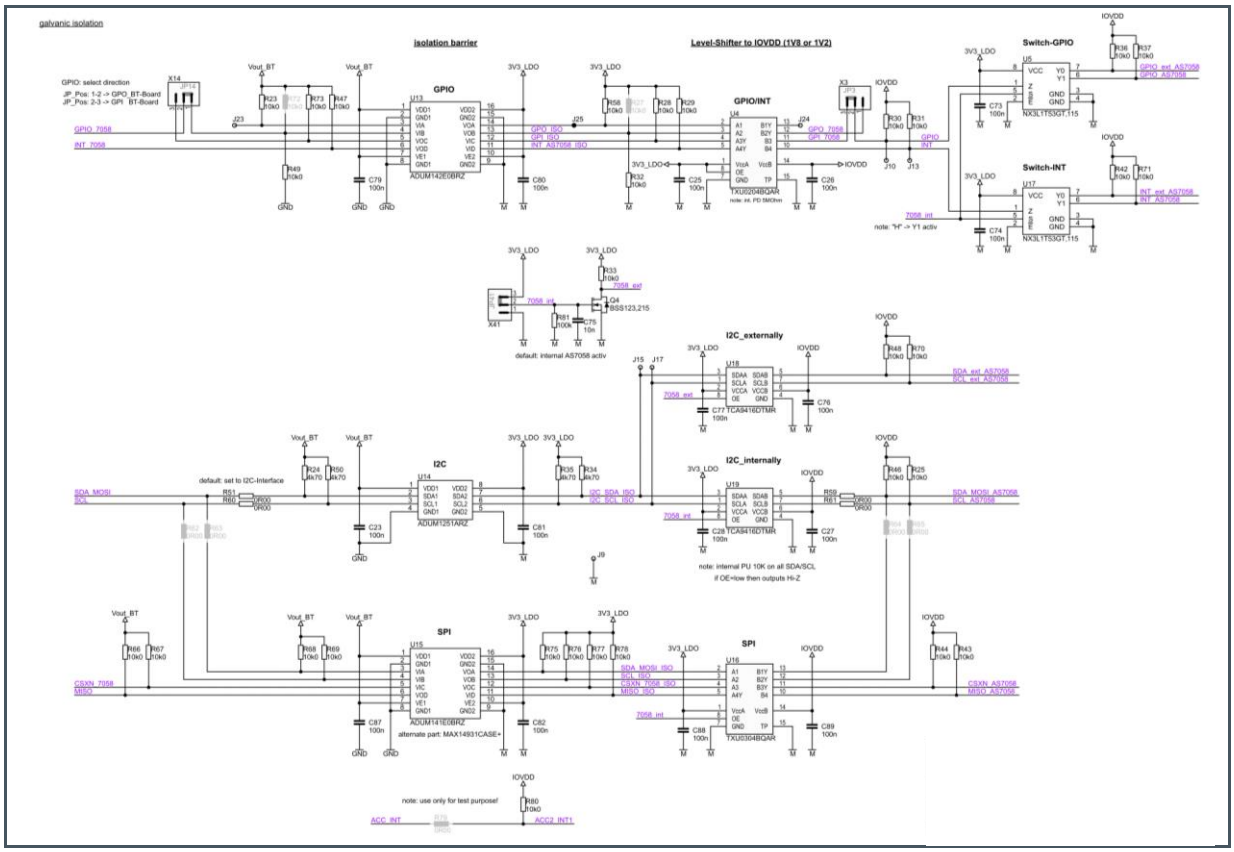
7.1 Schematic of Microcontroller with USB and BLE Module

Figure 68:
BLE Unit



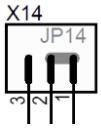
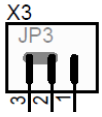
7.2 Galvanic Isolator Schematic

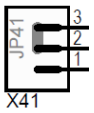
Figure 69:
Galvanic Isolation



Jumper Connection Galvanic Isolation

Figure 70:
Jumpers for Galvanic Isolation

Jumper	Default Connection	Other Possibilities
	GPIO: Select direction JP_Pos: 1-2 -> GPO_BT-Board (BTLE GPIO as GPO)	JP_Pos: 2-3 -> GPI_BT-Board (BTLE GPIO as GPI)
	GPIO: Select direction JP_Pos: 2-3 -> GPI 7058 to GPIO (GPI AS7058 to BTLE GPIO)	JP_Pos: 1-2 -> GPO 7058 to GPIO (GPO AS7058 to BTLE GPIO)

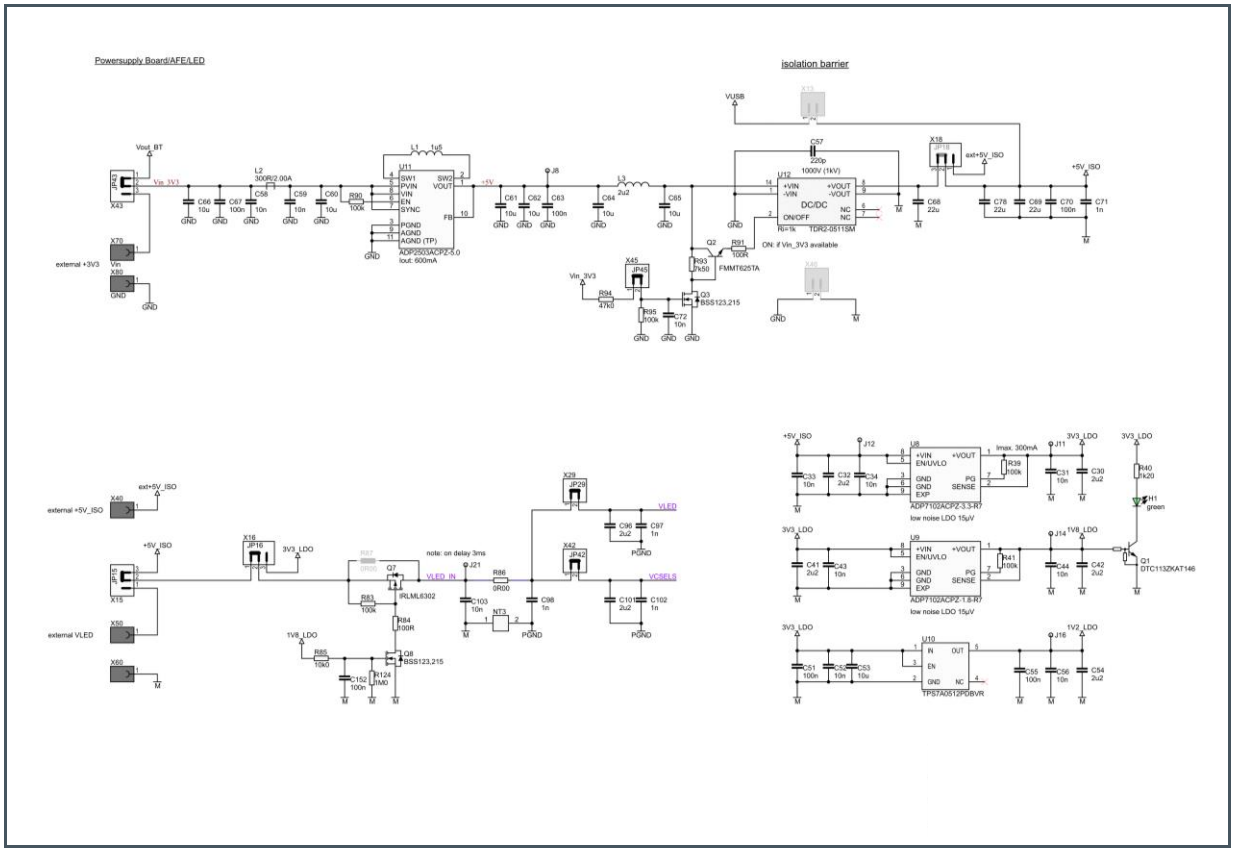
Jumper	Default Connection	Other Possibilities
	Internal AS7058 Active JP_Pos: 2-3	External AS7058 Active JP_Pos: 1-2

Information

2-pin jumpers should be connected to the 2-pin connector to operate the AS7058 EVK. 2-pin jumpers should be checked and connected with the 3-pin connector before operating the AS7058 EVK.

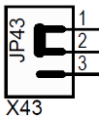
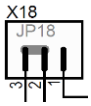
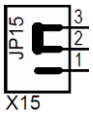
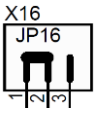
7.2.2 Schematic of the Power Supply for the AS7058 AFE

Figure 71:
Power Supply for the AS7058 AFE



Jumper Connection for the Power Supply

Figure 72:
Jumpers for the Power Supply

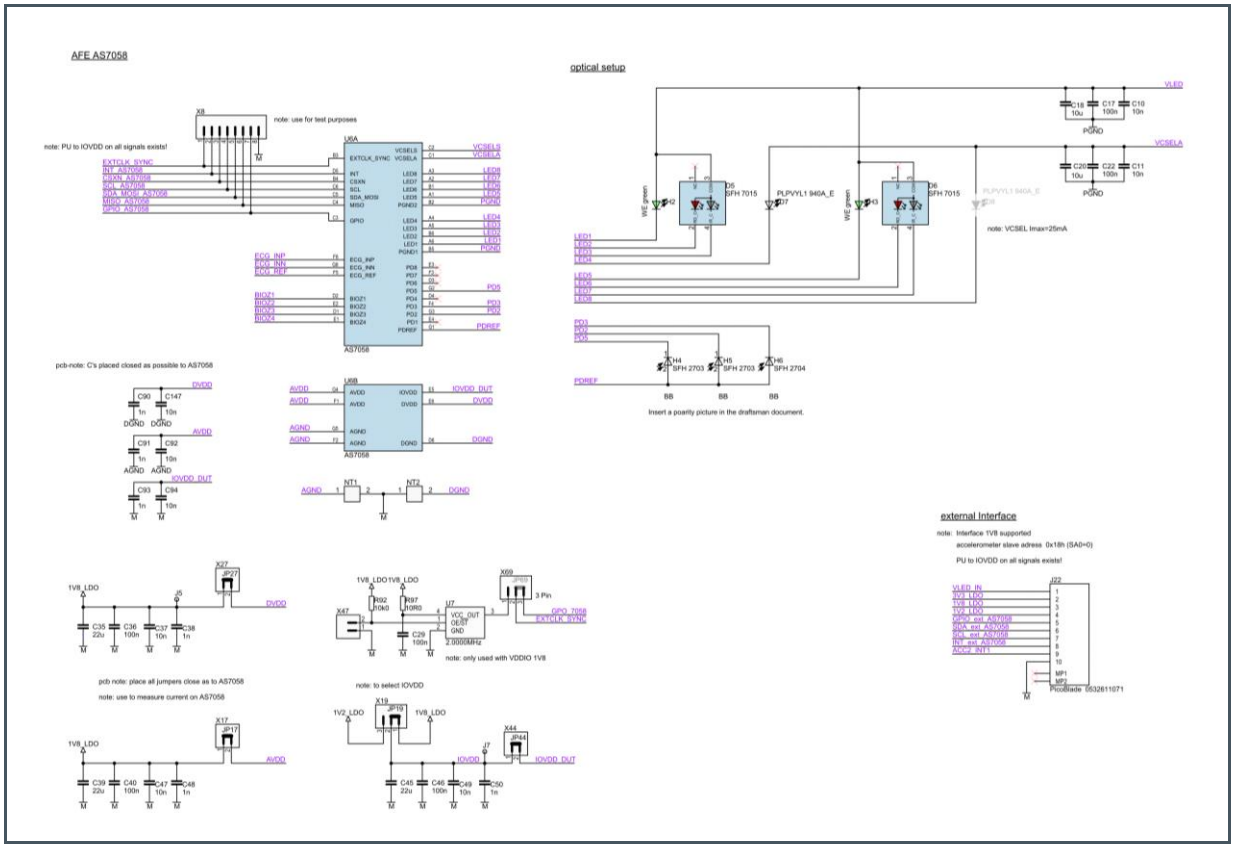
Jumper	Default Connection	Other Possibilities
	Power Supply JP_Pos: 1-2 -> Vout_BT	JP_Pos: 2-3 -> External +3V3
	Power Supply from the board JP_Pos: 2-3 -> +5V	Power Supply from the external source JP_Pos: 1-2 -> ext+5V_ISO
	JP_Pos: 2-3 -> +5V_ISO	External LDO JP_Pos: 1-2 -> external LDO
	+5V Power Supply JP_Pos: 1-2 -> +5V_ISO	+3V3 LDO Power Supply JP_Pos: 2-3 -> 3V3_LDO

Information

2-pin jumpers should be connected to the 2-pin connector to operate the AS7058 EVK. 2-pin jumpers should be checked and connected with the 3-pin connector before operating the AS7058 EVK.

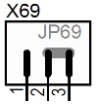
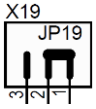
7.2.3 AS7058 AFE Schematic

Figure 73:
AS7058 AFE



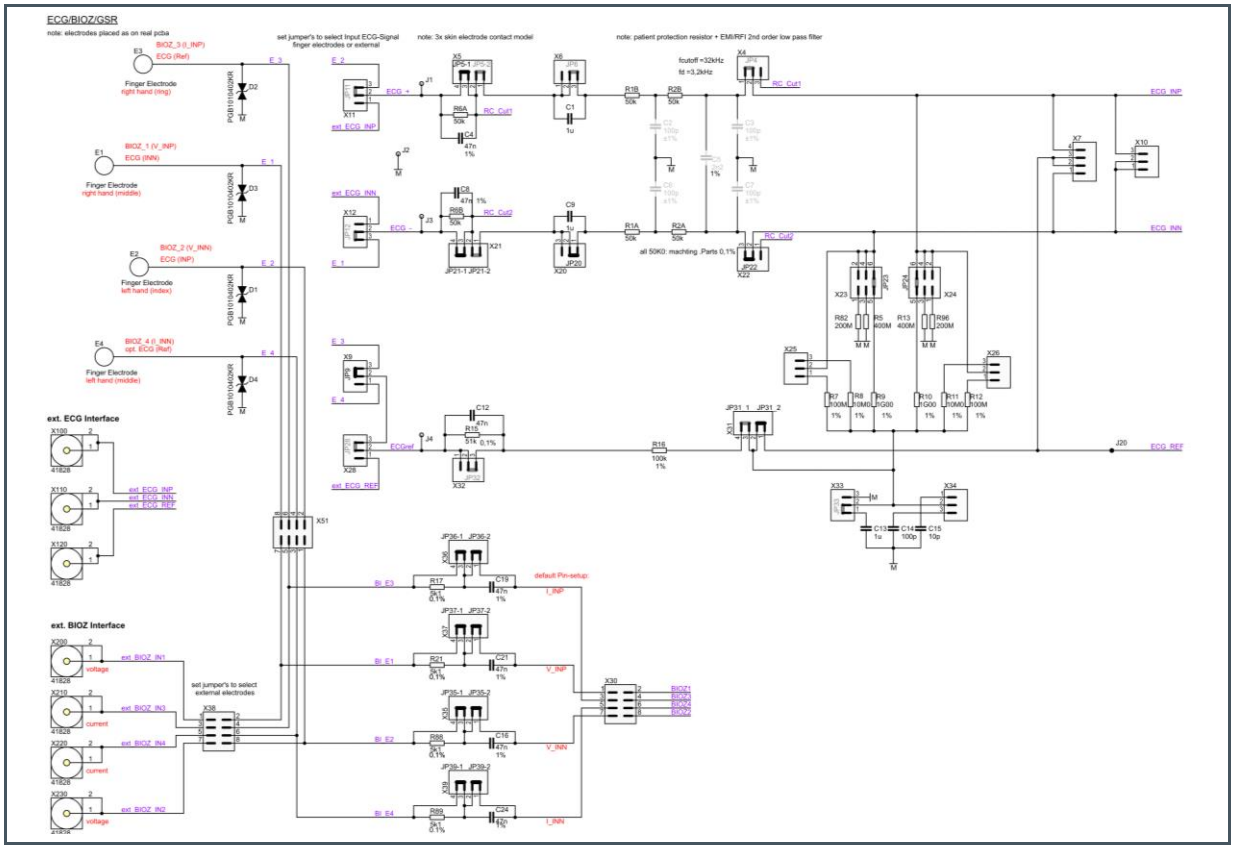
Jumper Connection for the AFE

Figure 74:
Jumpers for the AFE

Jumper	Default Connection	Other Possibilities
	External Clock Synchronization JP_Pos: 2-3 -> GPO 7058 to External clock	2MHz External Clock JP_Pos: 1-2 -> 2MHz clock to External clock
	Select IOVDD: JP_Pos: 1-2 -> 1V8_LDO (Select IOVDD for AS7058)	 JP_Pos: 2-3 -> 1V2_LDO (Select IOVDD for AS7058)

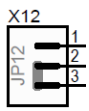
7.2.4 ECG/BIOZ/GSR Schematic

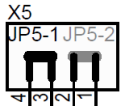
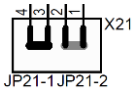
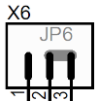
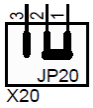
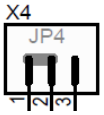
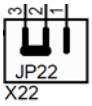
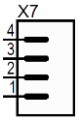
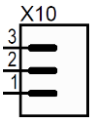
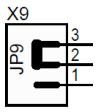
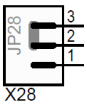
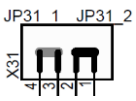
Figure 75:
ECG/BIOZ/GSR

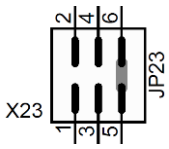
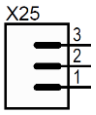
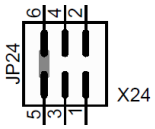
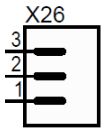
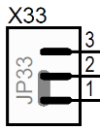
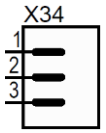
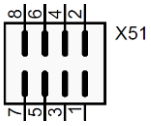
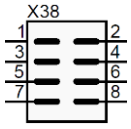
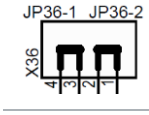
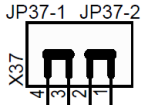
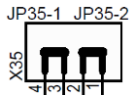


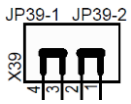
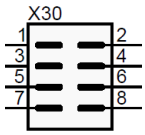
Jumper Connection for ECG/EDA/BioZ

Figure 76:
Jumpers for ECG/EDA/BioZ

Jumper	Default Connection	Other Possibilities
	E2 Electrode JP_Pos: 2-3 -> E2 to ECG + (Finger electrode E2 to ECG+)	External ECG INP JP_Pos: 2-3 -> ext_ECG_INP to ECG + (External electrode ECG_INP to ECG+)
	E1 Electrode JP_Pos: 2-3 -> E1 to ECG - (Finger electrode E1 to ECG-)	External ECG INN JP_Pos: 2-3 -> ext_ECG_INN to ECG - (External electrode ECG_INN to ECG-)

Jumper	Default Connection	Other Possibilities
	Exclude RC circuit to ECG + connection JP_Pos: 1-2 -> ECG + connection JP_Pos: 3-4 -> RC Cut1 exclude	Include RC circuit to ECG + connection JP_Pos: 1-2 -> ECG + connection JP_Pos: 3-4 -> RC Cut1 include
	Exclude RC circuit to ECG + connection JP_Pos: 1-2 -> ECG + connection JP_Pos: 3-4 -> RC Cut2 exclude	Include RC circuit to ECG + connection JP_Pos: 1-2 -> ECG + connection JP_Pos: 3-4 -> RC Cut2 include
	Exclude Capacitor JP_Pos: 2-3	Include Capacitor JP_Pos: 1-2
	Exclude Capacitor JP_Pos: 2-3	Include Capacitor JP_Pos: 1-2
	Patient protection circuit JP_Pos: 1-2 -> include	RC cut1 include JP_Pos: 2-3 -> RC cut1 to ECG INP
	Patient protection circuit JP_Pos: 1-2 -> include	RC cut2 include JP_Pos: 2-3 -> RC cut1 to ECG INN
	No jumper	ECG pins connection JP_Pos: 1-2 -> ECG_INN to ECG_ref JP_Pos: 3-4 -> ECG_INP to ECG_ref
	No jumper	ECG pins connection JP_Pos: 1-2 -> ECG_INN JP_Pos: 2-3 -> ECG_INP to ECG_INN
	E3 Electrode connection with ECG_ref JP_Pos: 2-3 -> E3	E4 Electrode connection with ECG_ref JP_Pos: 1-2 -> E4
	On board ECG_ref Electrode JP_Pos: 2-3	External ECG_ref Electrode JP_Pos: 1-2
	Exclude RC circuit to ECG_ref connection JP_Pos: 2-3 -> C exclude	Include RC circuit to ECG_ref connection JP_Pos: 1-2 -> RC include
	Exclude Capacitor circuit to ECG_ref connection JP_Pos: 1-2 -> ECG_ref connection JP_Pos: 3-4 -> Capacitor exclude	Include Capacitor circuit to ECG_ref connection JP_Pos: 1-2 -> ECG_ref connection JP_Pos: 3-4 -> Capacitor include

Jumper	Default Connection	Other Possibilities
	Select Bias Resistor: Resistor connection JP_Pos: 5-6 -> 1G00	Resistor connection JP_Pos: 1-2 -> 200M JP_Pos: 3-4 -> 400M
	Select Bias Resistor: No jumper	Resistor connection JP_Pos: 1-2 -> 100M JP_Pos: 2-3 -> 10M
	Select Bias Resistor: Resistor connection JP_Pos: 5-6 -> 1G00	Resistor connection JP_Pos: 1-2 -> 200M JP_Pos: 3-4 -> 400M
	Select Bias Resistor: No jumper	Resistor connection JP_Pos: 1-2 -> 100M JP_Pos: 2-3 -> 10M
	Include Capacitor circuit to ECG_ref connection JP_Pos: 1-2 -> 1µF	Connect with GND JP_Pos: 2-3
	No jumper	Include Capacitor circuit to ECG_ref connection JP_Pos: 1-2 -> 10pF JP_Pos: 2-3 -> 100pF
	Share electrodes ECG/BIOZ: No jumper	On board BioZ connection JP_Pos: 1-2 -> BioZ_2 or E2 JP_Pos: 3-4 -> BioZ_4 or E4 JP_Pos: 5-6 -> BioZ_3 or E3 JP_Pos: 7-8 -> BioZ_1 or E1
	Enable External BioZ or plug BioZ samples: No jumper	External BioZ connection JP_Pos: 1-2 -> BioZ_1 JP_Pos: 3-4 -> BioZ_3 JP_Pos: 5-6 -> BioZ_4 JP_Pos: 7-8 -> BioZ_2
	Exclude R&C from BioZ1 connection JP_Pos: 1-2 -> add jumper JP_Pos: 3-4 -> add jumper	Include R&C from BioZ1 connection JP_Pos: 1-2 -> no jumper for Resistor JP_Pos: 3-4 -> no jumper for capacitor
	Exclude R&C from BioZ3 connection JP_Pos: 1-2 -> add jumper JP_Pos: 3-4 -> add jumper	Include R&C from BioZ3 connection JP_Pos: 1-2 -> no jumper for Resistor JP_Pos: 3-4 -> no jumper for capacitor
	Exclude R&C from BioZ2 connection JP_Pos: 1-2 -> add jumper JP_Pos: 3-4 -> add jumper	Include R&C from BioZ2 connection JP_Pos: 1-2 -> no jumper for Resistor JP_Pos: 3-4 -> no jumper for capacitor

Jumper	Default Connection	Other Possibilities
	Exclude R&C from BioZ4 connection JP_Pos: 1-2 -> add jumper JP_Pos: 3-4 -> add jumper	Include R&C from BioZ4 connection JP_Pos: 1-2 -> no jumper for Resistor JP_Pos: 3-4 -> no jumper for capacitor
	Enable external BioZ or plug BioZ samples: No jumper	On board BioZ connection JP_Pos: 1-2 -> BioZ_1 JP_Pos: 3-4 -> BioZ_3 JP_Pos: 5-6 -> BioZ_4 JP_Pos: 7-8 -> BioZ_2

Information

Two pin jumpers should be connected to the two-pin connector - to operate the AS7058 EVK. Two pin jumpers should be checked and connected with the three-pin connector before operating the AS7058 EVK.

8 Revision Information

Definitions

Draft / Preliminary:
The draft / preliminary status of a document indicates that the content is still under internal review and subject to change without notice. ams-OSRAM AG does not give any warranties as to the accuracy or completeness of information included in a draft / preliminary version of a document and shall have no liability for the consequences of use of such information.

Changes from previous version to current revision v1-00	Page
Initial production version	all

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

9 Legal Information

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