AS5215

Programmable 360° Magnetic Angle Encoder with Buffered Sine & Cosine Output Signals

General Description

The AS5215 is a redundant, contactless rotary encoder sensor for accurate angular measurement over a full turn of 360° and over an extended ambient temperature range of -40°C to 150°C.

Based on an integrated Hall element array, the angular position of a simple two-pole magnet is translated into analog output voltages. The angle information is provided by means of buffered sine and cosine voltages. This approach gives maximum flexibility in system design, as it can be directly integrated into existing architectures and optimized for various applications in terms of speed and accuracy.

With two independent dies in one package, the device offers true redundancy. Usually the bottom die, which is exposed to slightly less magnetic field is employed for plausibility check.

An SSI Interface is implemented for signal path configuration as well as a one time programmable register block (OTP), which allows the customer to adjust the signal path gain to adjust for different mechanical constraints and magnetic field.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS5215, Programmable 360° Magnetic Angle Encoder with Buffered Sine & Cosine Output Signals are listed below:

Figure 1:
Added Value of Using AS5215

Benefits	Features
• Highest reliability and durability	• Contactless high resolution rotational position encoding over a full turn of 360 degrees
• Simple programming	• Simple user-programmable over serial interface (SSI)
• High precision analog output	• Buffered sine and cosine output signals
• Very low average power consumption	• Low power mode
• Easy setup	• Serial read-out of multiple interconnected devices using Daisy Chain mode
• Fully automotive qualified	• Fully automotive qualified to AEC-Q100, grade 0

Benefits	Features
• Small form factor	• Thin punched 32-pin MLF (7x7mm) package
• Robust environmental tolerance	• Wide temperature range: -40°C to 150°C

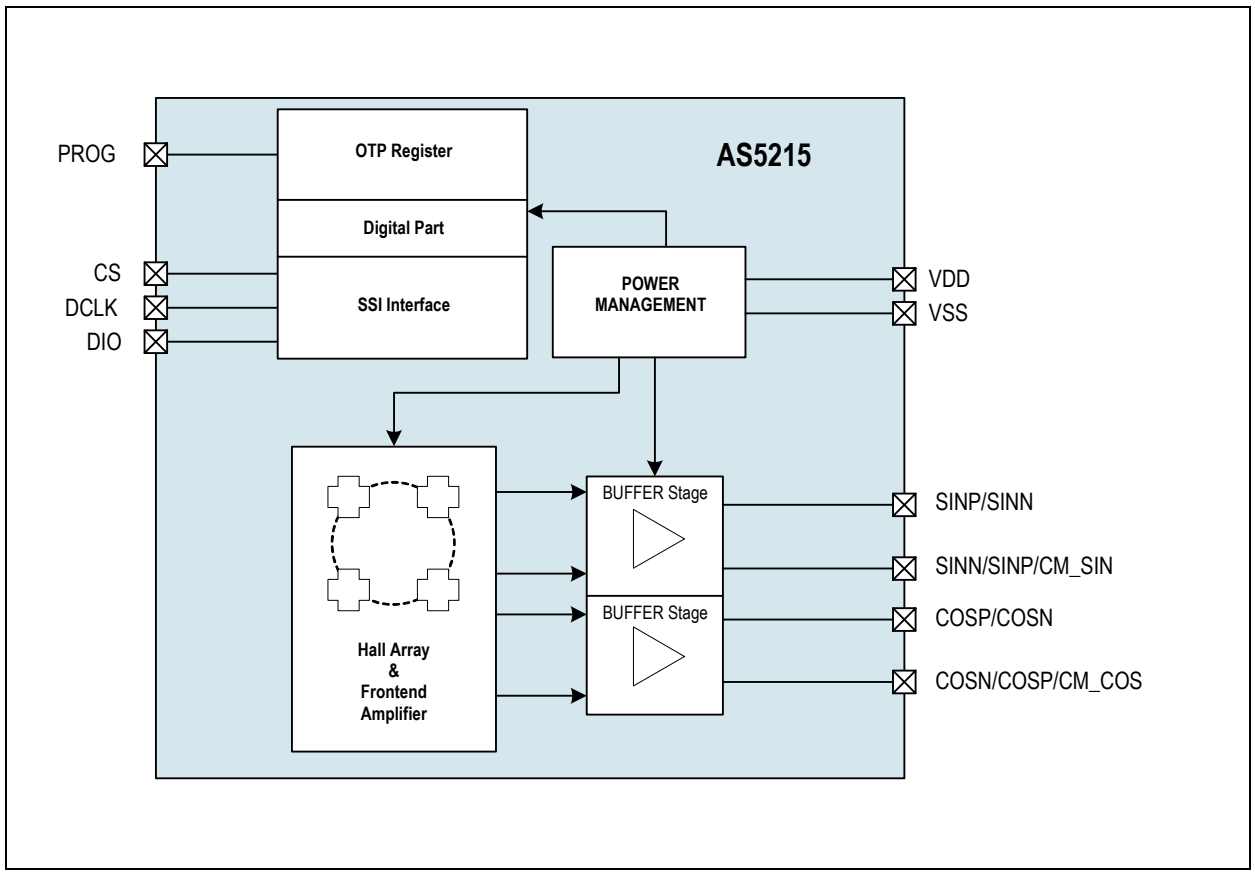
Applications

The AS5215 is ideal for Electronic Power Steering systems and general purpose for automotive or industrial applications in microcontroller-based systems.

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
AS5215 Block Diagram



Note(s):

1. This Block Diagram presents only one die.

Pin Assignment

Figure 3:
Pin Diagram (Top View)

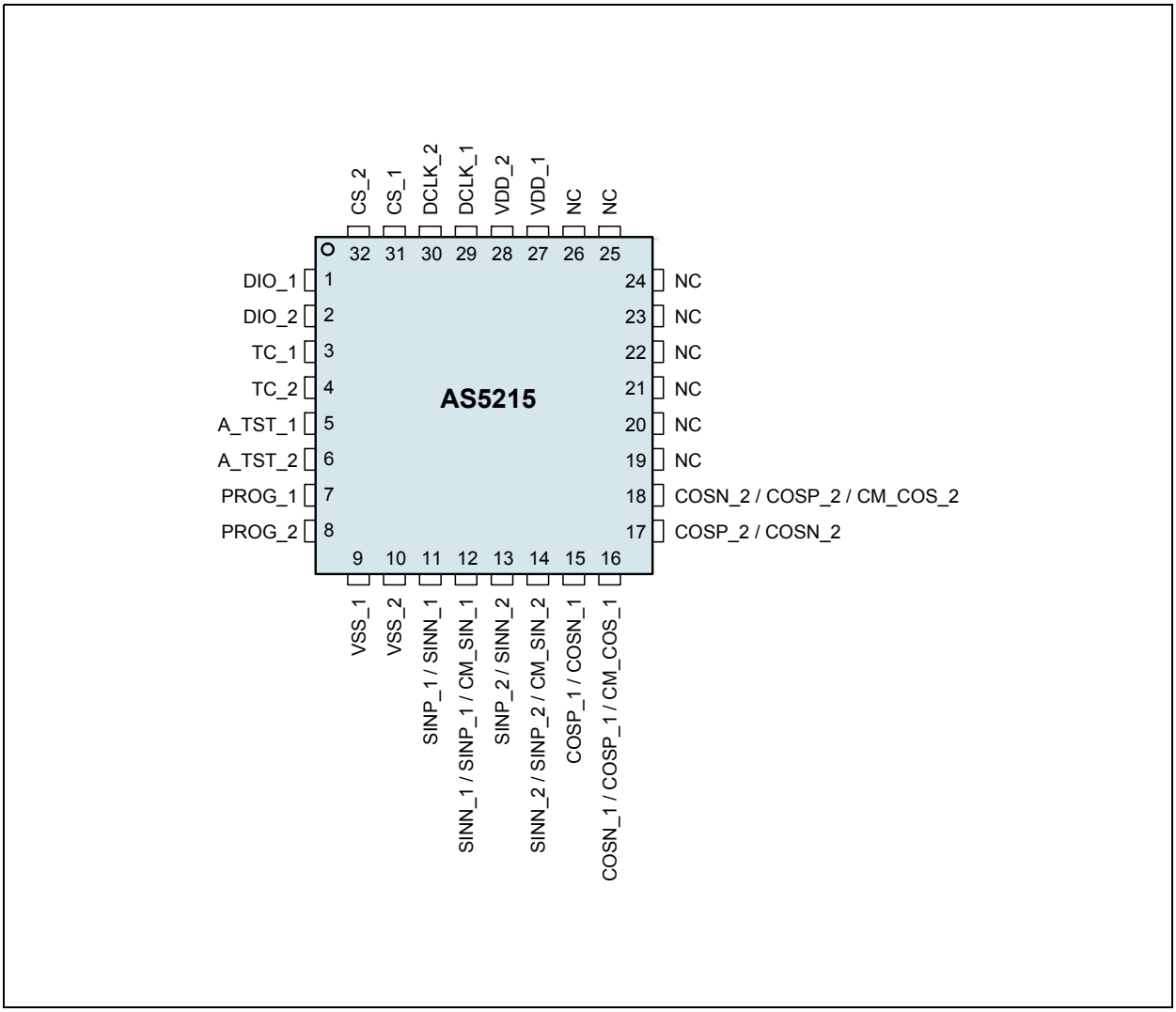


Figure 4:
Pin Description

Pin Name	Pin Number	Description
DIO_1	1	Data I/O for digital interface
DIO_2	2	
TC_1	3	Test coil
TC_2	4	
A_TST_1	5	Analog test pin
A_TST_2	6	

Pin Name	Pin Number	Description
PROG_1	7	OTP Programming Pad
PROG_2	8	
VSS_1	9	Supply ground
VSS_2	10	
SINP_1 / SINN_1	11	Switchable buffered analog output
SINN_1 / SINP_1 / CM_SIN_1	12	Switchable buffered analog or common mode output
SINP_2 / SINN_2	13	Switchable buffered analog output
SINN_2 / SINP_2 / CM_SIN_2	14	Switchable buffered analog or common mode output
COSP_1 / COSN_1	15	Switchable buffered analog output
COSN_1 / COSP_1 / CM_COS_1	16	Switchable buffered analog or common mode output
COSP_2 / COSN_2	17	Switchable buffered analog output
COSN_2 / COSP_2 / CM_COS_2	18	Switchable buffered analog or common mode output
NC	19	-
NC	20	
NC	21	
NC	22	
NC	23	
NC	24	
NC	25	
NC	26	
VDD_1	27	Digital + analog supply
VDD_2	28	
DCLK_1	29	Clock input for digital interface
DCLK_2	30	
CS_1	31	Clock input for digital interface
CS_2	32	

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
Electrical Parameters				
Supply voltage (VDD)	-0.3	7	V	
Input pin voltage (V_in)	-0.3	VDD+0.3	V	
Input current (latchup immunity), I_scr	-100	100	mA	EIA/JESD78 Class II Level A
Electrostatic Discharge				
Electrostatic discharge (ESD_{HBM})	±2		kV	JESD22-A114E
Continuous Power Dissipation				
Total power dissipation (P_{tot})		275	mW	
Package thermal resistance (Θ_JA)		27	°C/W	Velocity =0; Multi Layer PCB; Jedec Standard Testboard
Temperature Ranges and Storage Conditions				
Storage temperature (T_strg)	-65	150	°C	
Package body temperature (T_body)		260	°C	IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) specified is in accordance with IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-Hermetic Solid State Surface Mount Devices”. The lead finish for Pb-free leaded packages is matte tin (100% Sn).
Relative humidity, non-condensing (RH_{NC})	5	85	%	
Moisture sensitivity level (MSL)	3			Represents a maximum floor time of 168h

Electrical Characteristics

Unless otherwise noted all in this specification defined tolerances of parameters are assured over the whole operation conditions range and also over lifetime.

Figure 6:
Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VDD	Positive supply voltage		4.5		5.5	V
VSS	Negative supply voltage		0.0		0.0	V
T_amb	Ambient temperature		-40		150	°C

Figure 7:
DC/AC Characteristics for Digital Inputs and Outputs

Symbol	Parameter	Condition	Min	Typ	Max	Unit
CMOS Input						
V_IH	High level input voltage		0.7 * VDD			V
V_IL	Low level input voltage				0.3 * VDD	V
I_LEAK	Input leakage current				1	µA
CMOS Output						
V_OH	High level output voltage	4 mA	VDD - 0.5			V
V_OL	Low level output voltage	4 mA			VSS + 0.4	V
C_L	Capacitive load				35	pF
t_slew	Slew rate				30	ns
t_delay	Time rise fall				15	ns
CMOS Output Tristate						
I_OZ	Tristate leakage current				1	µA

Figure 8:
Magnetic Input Specification

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Two Pole Cylindrical Magnet, Diametrically Magnetized:						
d_{MAG}	Diameter		4	6		mm
B_{pp}	Magnetic input field amplitude	200 – 800 Gauss	20	50	80	mT
f_{rot}	Rotational speed	Max 30000 RPM	0		500	Hz

Figure 9:
Electrical System Specifications

Symbol	Parameter	Condition	Min	Typ	Max	Unit
IDD	Current consumption	Max value derived at maximum I_H (Hall Bias Current) For single die only	20		28	mA
t_{power_on}	Power up time				1.275	ms
t_{prop}	Propagation delay	-40 to 150ºC	18	22	30	µs
M	Magnetic sensitivity	1G = 0.1 mT	1		6	mV/G
V_{out}	Analog output range		Vss+ 0.25		Vdd- 0.5	V
AM_{Temp}	AM tracking accuracy over temperature	-40°C to 150°C	-1		1	%
AM	Sin / Cos amplitude mismatch	25°C	-2		2	%
$V_{offset1}$	DC offset	At no input signal; programmable OTP setting (see page 10)	1.47	1.5	1.53	V
$V_{offset2}$			2.45	2.5	2.55	V
$DC_{offdrift}$	DC offset drift	-40 to 150ºC	-50		+50	µV/ºC
THD	Total harmonic distortion				0.2	%
SR	Slew rate			1		V/µs
C_{LOAD}	Capacitive load				1000	pF

Figure 10:
Timing Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t1_3	Chip select to positive edge of DCLK		30		-	ns
t2_3	Chip select to drive bus externally		0		-	ns
t3	Setup time command bit Data valid to positive edge of DCLK		30		-	ns
t4	Hold time command bit Data valid after positive edge of DCLK		15		-	ns
t5	Float time Positive edge of DCLK for last command bit to bus float		-		$\frac{1}{(2+0)\cdot f\_DCLK}$	ns
t6	Bus driving time Positive edge of DCLK for last command bit to bus drive		$\frac{1}{(2+0)\cdot f\_DCLK}$		-	ns
t7	Data valid time Positive edge of DCLK to bus valid		$\frac{1}{(2+0)\cdot f\_DCLK}$		$\frac{1}{(2+30)\cdot f\_DCLK}$	ns
t8	Hold time data bit Data valid after positive edge of DCLK		$\frac{1}{(2+0)\cdot f\_DCLK}$		-	ns
t9_3	Hold time chip select Positive edge DCLK to negative edge of chip select		$\frac{1}{(2+0)\cdot f\_DCLK}$		-	ns

Symbol	Parameter	Condition	Min	Typ	Max	Unit
t10_3	Bus floating time Negative edge of chip select to float bus		-		30	ns
t11	Setup time data bit at write access Data valid to positive edge of DCLK		30		-	ns
t12	Hold time data bit at write access Data valid after positive edge of DCLK		15		-	ns
t13_3	Bus floating time Negative edge of chip select to float bus		-		30	ns

Note(s):

1. **T**he digital interface will be reset during the low phase of the CS signal.

Detailed Description

The AS5215 is a redundant rotary encoder sensor front end. Based on an integrated Hall element array, the angular position of a simple two-pole magnet is translated into analog output voltages. The angle information is provided by means of sine and cosine voltages. This approach gives maximum flexibility in system design, as it can be directly integrated into existing architectures and optimized for various applications in terms of speed and accuracy.

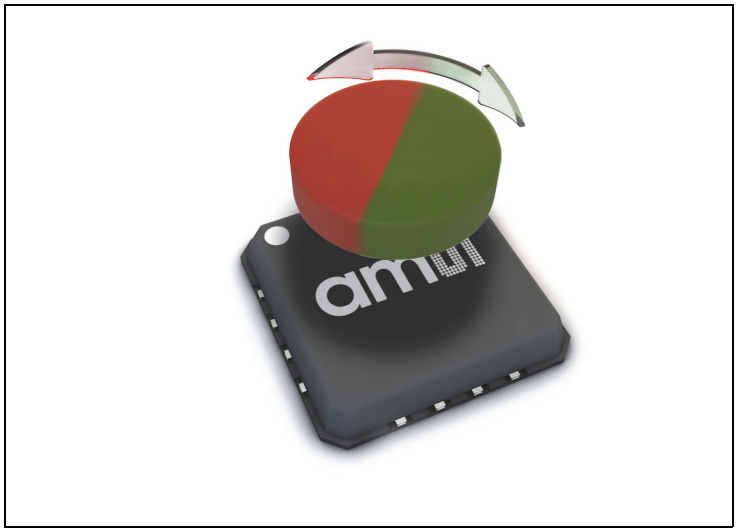
With two independent dies in one package, the device offers true redundancy. Usually the bottom die, which is exposed to slightly less magnetic field is employed for plausibility check.

An SSI (SPI standard) protocol is implemented for internal test access to the different circuit blocks and for signal path configuration.

A One Time Programmable register block (OTP) allows the customer to adjust the signal path gain to adjust for different mechanical constraints and magnetic field strengths. Furthermore, for internal use, the test mode can be enabled and the system oscillator is trimmable, DC offset of the output signal can be set to either 1.5V or 2.5V. A unique chip ID is stored to ensure traceability.

For operating point control, a band gap circuit is implemented together with a central bias block to distribute all reference bias currents for the analog signal conditioning. The digital signal part is based on a 2MHz system, CLK derived via. divider from a 4MHz system oscillator.

Figure 11:
Typical Arrangement of AS5215 and Magnet



Magnet Diameter and Vertical Distance

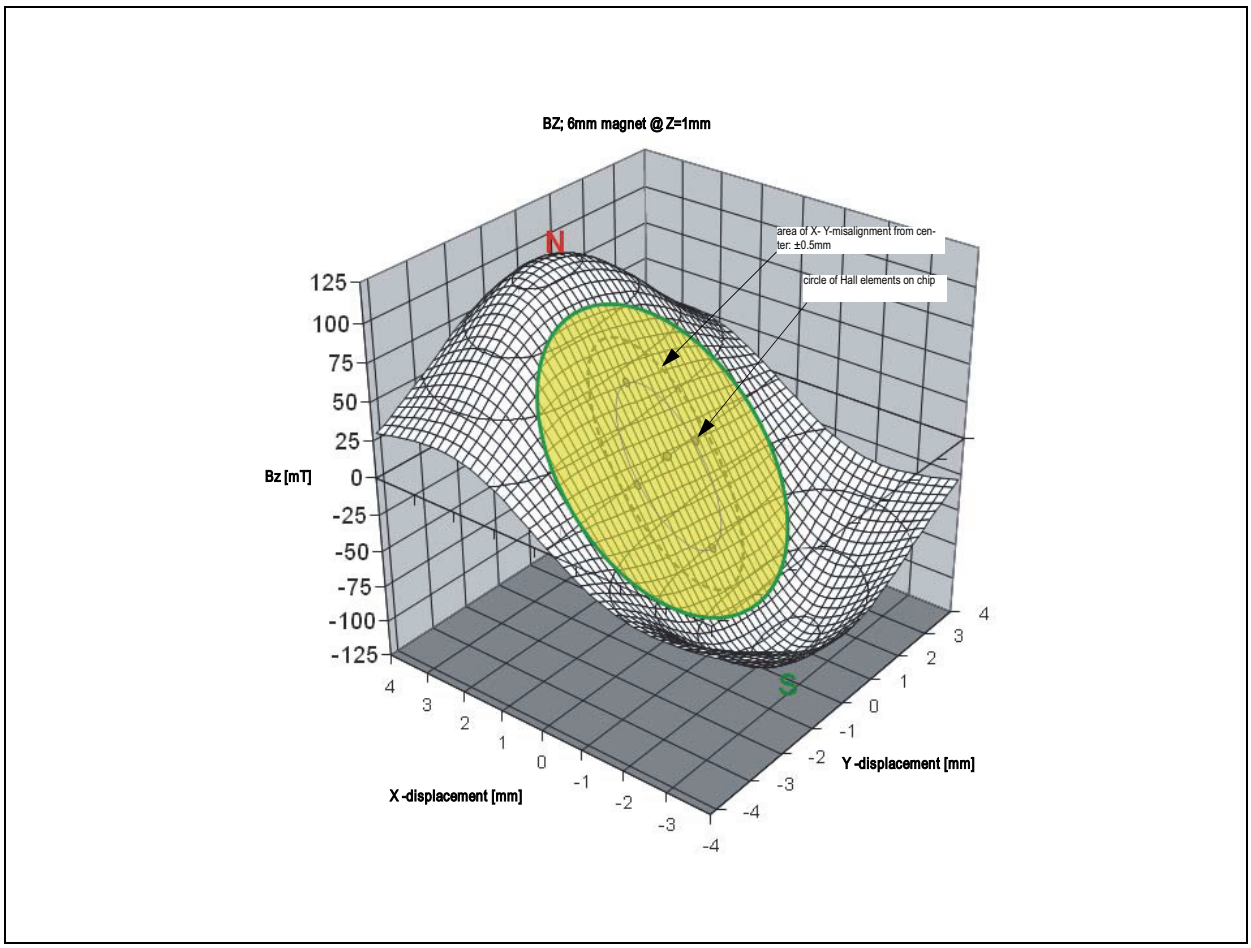
Note(s): Following is an abstract taken from the elaborate application note on the Magnet.
For more detailed information, please visit our homepage www.ams.com/eng/Products/Position-Sensors

The Linear Range

The Hall elements used in the AS5000-series sensor ICs are sensitive to the magnetic field component Bz, which is the magnetic field vertical to the chip surface. Figure 12 shows a 3-dimensional graph of the Bz field across the surface of a 6mm diameter, cylindrical NdFeB N35H magnet at an axial distance of 1mm between magnet and IC.

The highest magnetic field occurs at the north and south poles, which are located close to the edge of the magnet, at ~2.8mm radius (see Figure 14). Following the poles towards the center of the magnet, the Bz field decreases very linearly within a radius of ~1.6mm. This linear range is the operating range of the magnet with respect to the Hall sensor array on the chip. For best performance, the Hall elements should always be within this linear range.

Figure 12:
3D-Graph of Vertical Magnetic Field of a 6mm Cylindrical Magnet



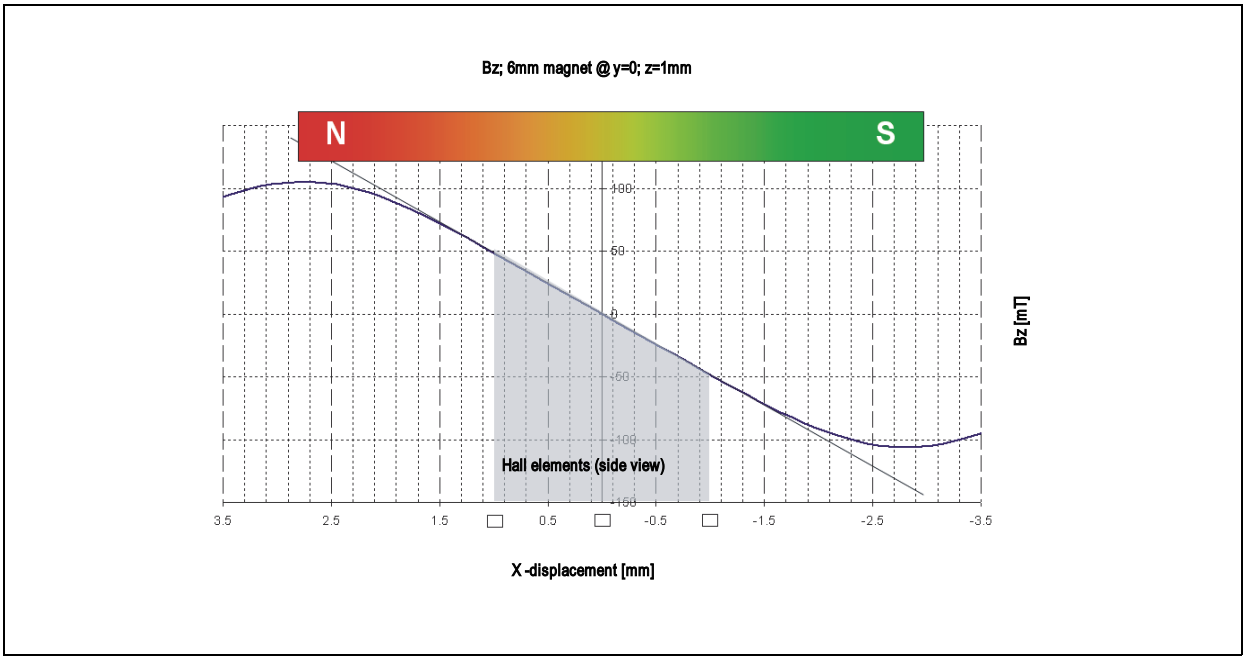
As shown in Figure 14 (grey zone), the Hall elements are located on the chip at a circle with a radius of 1mm. Since the difference between two opposite Hall sensors is measured, there will be no difference in signal amplitude when the magnet is perfectly centered or if the magnet is misaligned in any direction as long as all Hall elements stay within the linear range.

For the 6mm magnet (shown in Figure 14), the linear range has a radius of 1.6mm, hence this magnet allows a radial misalignment of 0.5mm (1.6mm linear range radius; 1mm Hall array radius). Consequently, the larger the linear range, the more radial misalignment can be tolerated. By contrast, the slope of the linear range decreases with increasing magnet diameter, as the poles are further apart. A smaller slope results in a smaller differential signal, which means that the magnet must be moved closer to the IC (smaller airgap) or the amplification gain must be increased, which leads to a poorer signal-to-noise ratio. More noise results in more jitter at the angle output. A good compromise is a magnet diameter in the range of 5mm to 8mm.

Figure 13:
Small Diameter vs. Large Diameter

Small Diameter Magnet (<6mm)	Large Diameter Magnet (>6mm)
+ stronger differential signal = good signal / noise ratio, larger airgaps	+ wider linear range = larger horizontal misalignment area
- shorter linear range = smaller horizontal misalignment area	- weaker differential signal = poorer signal / noise ratio, smaller airgaps

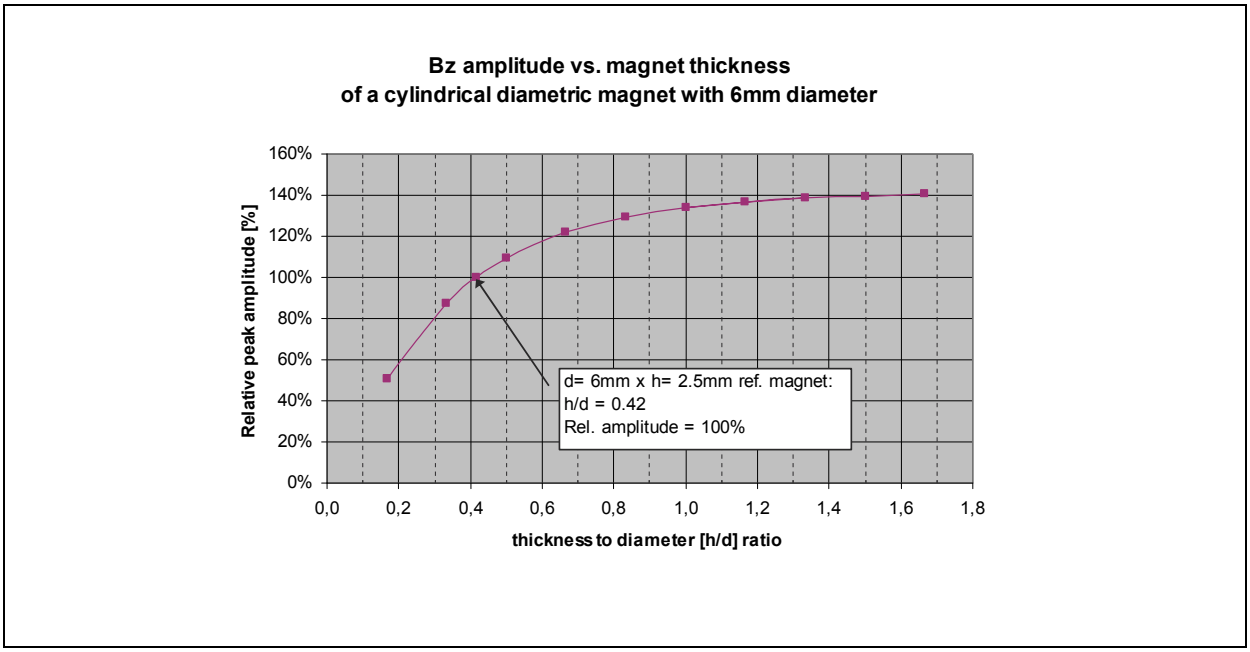
Figure 14:
Vertical Magnetic Field Across the Center of a Cylindrical Magnet



Magnet Thickness

Figure 15 shows the relationship of the peak amplitude in a rotating system (essentially the magnetic field strength of the Bz field component) in relation to the thickness of the magnet. The X-axis shows the ratio of magnet thickness (or height) [h] to magnet diameter [d] and the Y-axis shows the relative peak amplitude with reference to the recommended magnet (d=6mm, h=2.5mm). This results in an h/d ratio of 0.42.

Figure 15:
Relationship of Peak Amplitude vs. Magnet Thickness



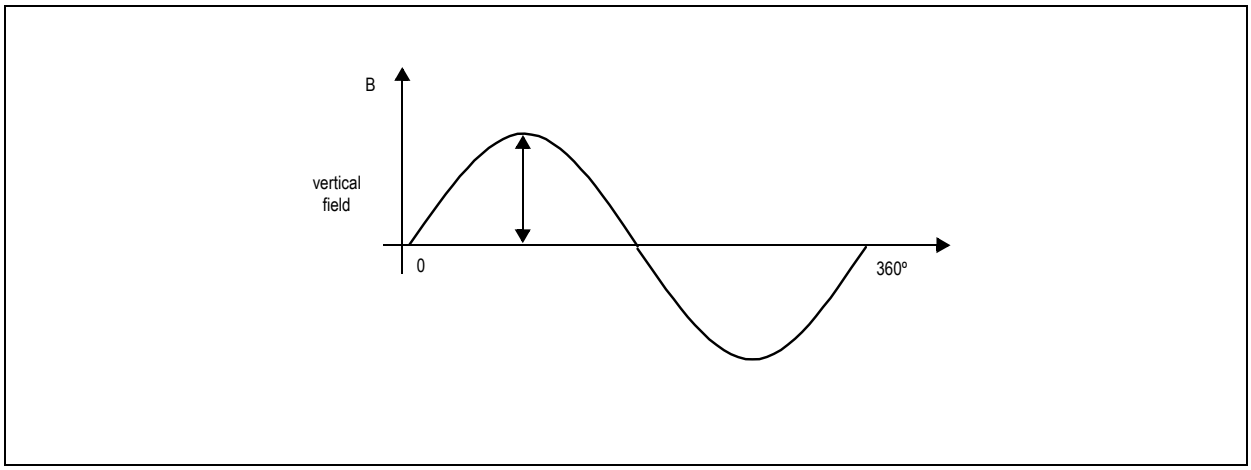
As the graph in Figure 15 shows, the amplitude drops significantly at h/d ratios below this value and remains relatively flat at ratios above 1.3.

Therefore, the recommended thickness of 2.5mm (at 6mm diameter) should be considered as the low limit with regards to magnet thickness.

It is possible to get 40% or more signal amplitude by using thicker magnets. However, the gain in signal amplitude becomes less significant for h/d ratios >~1.3. Therefore, the recommended magnet thickness for a 6mm diameter magnet is between 2.5 and ~8 mm.

Axial Distance (Airgap)

Figure 16:
Sinusoidal Magnetic Field Generated by the Rotating Magnet



The recommended magnetic field, measured at the chip surface on a radius equal to the Hall sensor array radius (typ 1mm) should be within a certain range. This range lies between 45 and 75mT or between 20 and 80mT, depending on the encoder product.

Linear position sensors are more sensitive as they use weaker magnets. The allowed magnetic range lies typically between 5 and 60mT.

Angle Error vs. Radial and Axial Misalignment

The angle error is the deviation of the actual angle vs. the angle measured by the encoder. There are several factors in the chip itself that contribute to this error, mainly offset and gain matching of the amplifiers in the analog signal path. On the other hand, there is the nonlinearity of the signals coming from the Hall sensors, caused by misalignment of the magnet and imperfections in the magnetic material.

Ideally, the Hall sensor signals should be sinusoidal, with equal peak amplitude of each signal. This can be maintained, as long as all Hall elements are within the linear range of the magnetic field Bz (see Figure 14).

Mounting the Magnet

Generally, for on-axis rotation angle measurement, the magnet must be mounted centered over the IC package. However, the material of the shaft into which the magnet is mounted, is also of big importance.

Magnetic materials in the vicinity of the magnet will distort or weaken the magnetic field being picked up by the Hall elements and cause additional errors in the angular output of the sensor.

Figure 17:
Magnetic Field Lines in Air

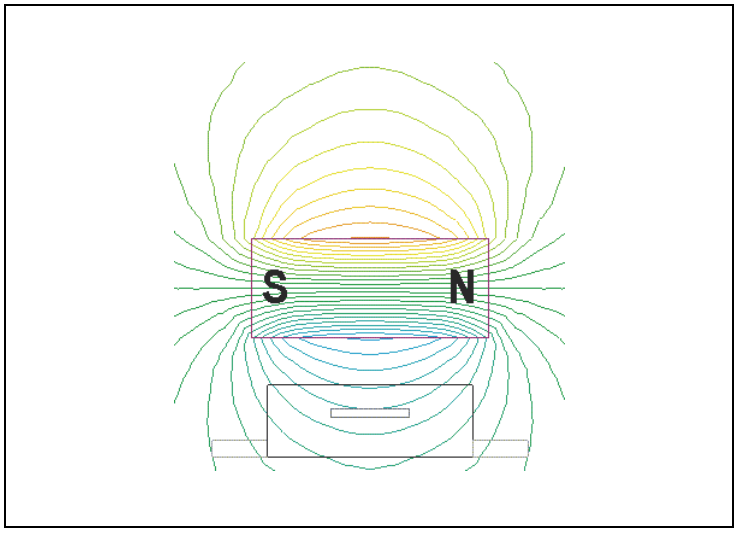
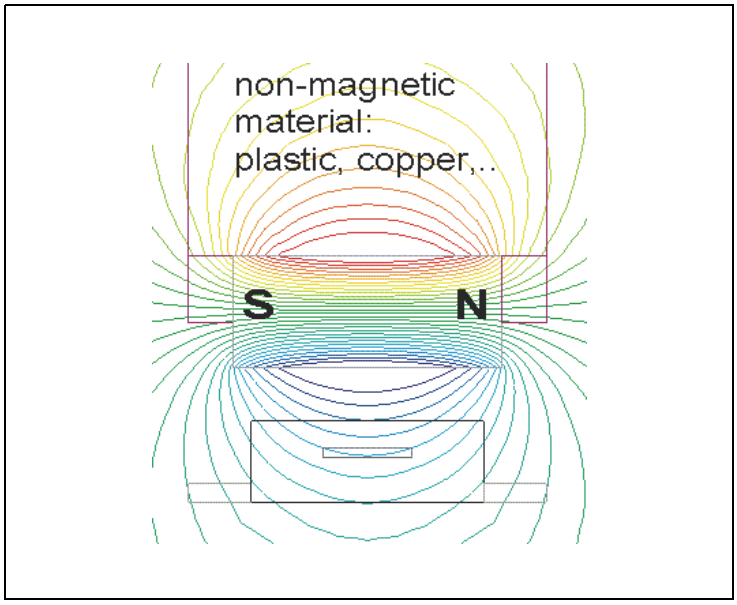


Figure 17 shows the ideal case with the magnet in air. No magnetic materials are anywhere nearby.

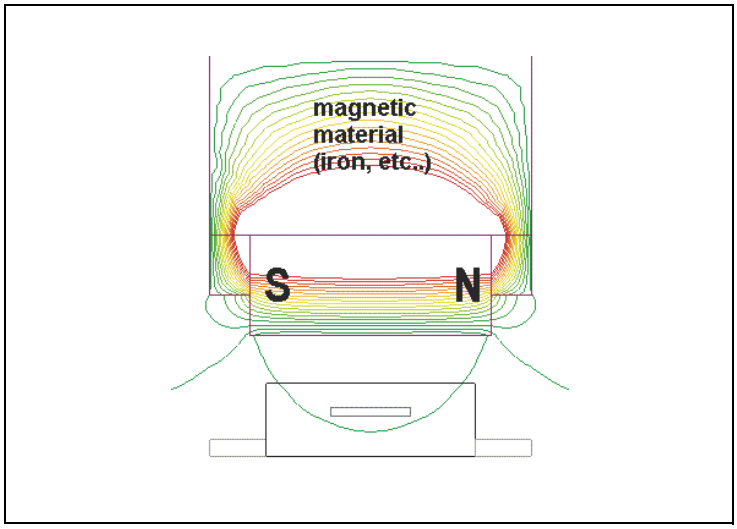
Figure 18:
Magnetic Field Lines in Plastic or Copper Shaft



If the magnet is mounted in non-magnetic material, such as plastic or diamagnetic material, such as copper, the magnetic field distribution is not disturbed. Even paramagnetic material, such as aluminium may be used. The magnet may be mounted directly in the shaft (see Figure 18).

Note(s): Stainless steel may also be used, but some grades are magnetic. Therefore, steel with magnetic grades should be avoided.

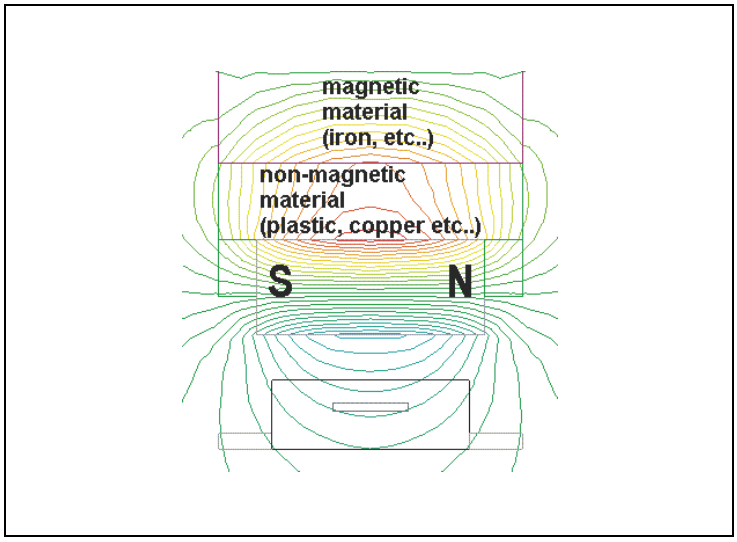
Figure 19:
Magnetic Field Lines in Iron Shaft



If the magnet is mounted in a ferromagnetic material, such as iron, most of the field lines are attracted by the iron and flow inside the metal shaft (see Figure 19). The magnet is weakened substantially.

This configuration should be avoided!

Figure 20:
Magnetic Field Lines with Spacer Between Magnet and Iron Shaft



If the magnet has to be mounted inside a magnetic shaft, a possible solution is to place a non-magnetic spacer between shaft and magnet, as shown in Figure 20. While the magnetic field is rather distorted towards the shaft, there are still adequate field lines available towards the sensor IC. The distortion remains reasonably low.

Summary

- Small diameter magnets (<6mm Ø) have a shorter linear range and allow less lateral misalignment. The steeper slope allows larger axial distances.
- Large diameter magnets (>6 mm Ø) have a wider linear range and allow a wider lateral misalignment. The flatter slope requires shorter axial distances.
- The linear range decreases with airgap; Best performance is achieved at shorter airgaps.
- The ideal vertical distance range can be determined by using magnetic range indicators provided by the encoder ICs. These indicators are named MagInc, MagDec, MagRngn, or similar, depending on product.

Application Information

Sleep Mode

The target is to provide the possibility to reduce the total current consumption. No output signal will be provided when the IC is in sleep mode. Enabling or disabling sleep mode is done by sending the SLEEP or WAKEUP commands via. the SSI interface. Analog blocks are powered down with respect to fast wake up time.

SSI Interface

The setup for the device is handled by the digital interface. Each communication starts with the rising edge of the chip select signal. The synchronization between the internal free running analog clock oscillator and the external used digital clock source for the digital interface is done in a way that the digital clock frequency can vary in a wide range.

Figure 21:
SSI Interface Pin Description

Port	Symbol	Function
Chip select	CS	Indicates the start of a new access cycle to the device CS = LO → reset of the digital interface
DCLK	DCLK	Clock source for the communication over the digital interface
Bidirectional data input output	DIO	Command and data information over one single line The first bit of the command defines a read or write access

Figure 22:
SSI Interface Parameter Description

Symbol	Parameter	Notes	Min	Typ	Max	Unit
f_DCLK	Clock frequency at normal operation	The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	no limit	5	6	MHz
f_EZ_RW	Clock frequency at easy zap read write access		no limit	5	6	kHz
f_EZ_PROG	Clock frequency at easy zap access program OTP	Correct access to the programmable zener diode block needs a strict timing – the zap pulse is exact one period. The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	200	-	650	kHz
f_EZ_ARB	Clock frequency at easy zap analog readback	20pF external load allowed. The nominal value for the clock frequency can be derived from a 10MHz oscillator source.	no limit	156.3	162.5	kHz
Interface General at normal mode						
Protocol: 5 command bit + 16 data input output						
Command		5 bit command: cmd<4:0> ← bit<21:16>				
Data		16 bit data: data<15:0> ← bit<15:0>				
Interface General at extended mode						
Protocol: 5 command bit + 46 data input output						
Command		5 bit command: cmd<4:0> ← bit<50:46>				
Data		34 bit data: data<45:0> ← bit<45:0>				
Interface Modes						
Normal read operation mode		cmd<4:0> = <00xxx> → 1 DCLK per data bit				
Extended read operation mode		cmd<4:0> = <01xxx> → 4 DCLK per data bit				
Normal write operation mode		cmd<4:0> = <10xxx> → 1 DCLK per data bit				
Extended write operation mode		cmd<4:0> = <11xxx> → 4 DCLK per data bit				

Device Communication / Programming

Figure 23:
Digital Interface at Normal Mode

#	Command	Bin	Mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
23	WRITE CONFIG 1	10111	write	go2sleep	gen_rst					analog_sig	OB_ bypassed								
16	EN_PROG	10000	write	1	0	0	0	1	1	0	0	1	0	1	0	1	1	1	0

Name	Functionality
go2sleep	Enter/leave low power mode (no output signals)
gen_rst	Generates global reset
analog_sig	Switches the channels to the test bus after the PGA
OB_bypassed	Disable and bypass output buffer for testing purpose

Figure 24:
Digital Interface at Extended Mode

#	Command	Bin	Mode	Factory Settings								User Settings					
				<45:44>	<43: 26>	<25:23>	<22: 20>	<19: 18>	<17: 14>	<13>	<12>	<11>	<10>	<9>	<8:7>	<6>	<5:0>
31	WRITE OTP	11111	xt write	otp test	ID	10µbiastrim		vref	osc	lock_ OTP	n.c.	invert_ channel	cm_sin	cm_cos	gain	dc_ offset	hall_ bias
25	PROG_OTP	11001	xt write	otp test	ID	10µbiastrim		vref	osc	lock_ OTP	n.c.	invert_ channel	cm_sin	cm_cos	gain	dc_ offset	hall_ bias
15	RD_OTP	01111	xt read	otp test	ID	10µbiastrim		vref	osc	lock_ OTP	n.c.	invert_ channel	cm_sin	cm_cos	gain	dc_ offset	hall_ bias

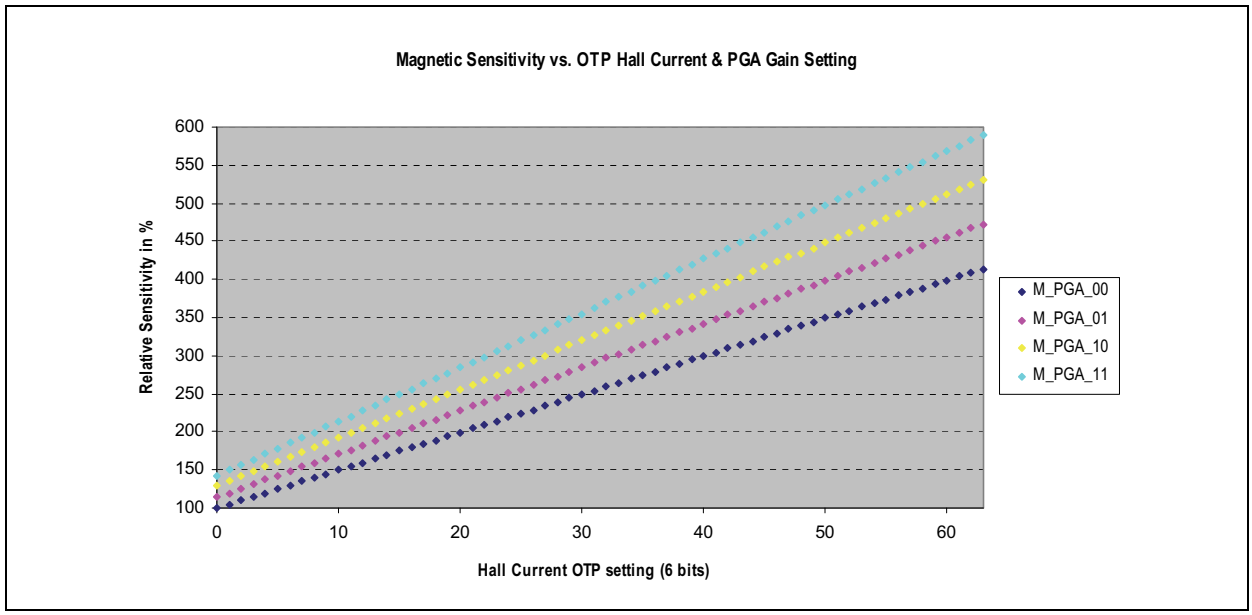
#	Command	Bin	Mode	Factory Settings								User Settings					
				<45:44>	<43:26>	<25:23>	<22:20>	<19:18>	<17:14>	<13>	<12>	<11>	<10>	<9>	<8:7>	<6>	<5:0>
9	RD_OTP_ANA	01001	xt read														

Name	Functionality
Otp_test	Dummy fuse bit used in production test
ID	Part identification
n.c.	Not connected
10µbiastrim	10µ bias current trim bits
vref	Bias Block reference voltage trim bits
osc	Oscillator trimming bits
lock_OTP	To disable the programming of the factory bits <45…14>
invert_channel	Inverts SIN and COS channel before the PGA for inverted output function (0 → SIN/COS, 1 → SINN/COSN)
cm_sin	Common mode voltage output enabled at SINN / CM pin (0 → differential, 1 → common)
cm_cos	Common mode voltage output enabled at COSN / CM pin (0 → differential, 1 → common)
gain	PGA gain setting (influences overall magnetic sensitivity), 2bit
dc_offset	Output DC offset (0 → Voffset1=1.5V, 1 → Voffset2=2.5V)
Hall_b	Hall bias setting (influences overall magnetic sensitivity), 6bit

Note(s):

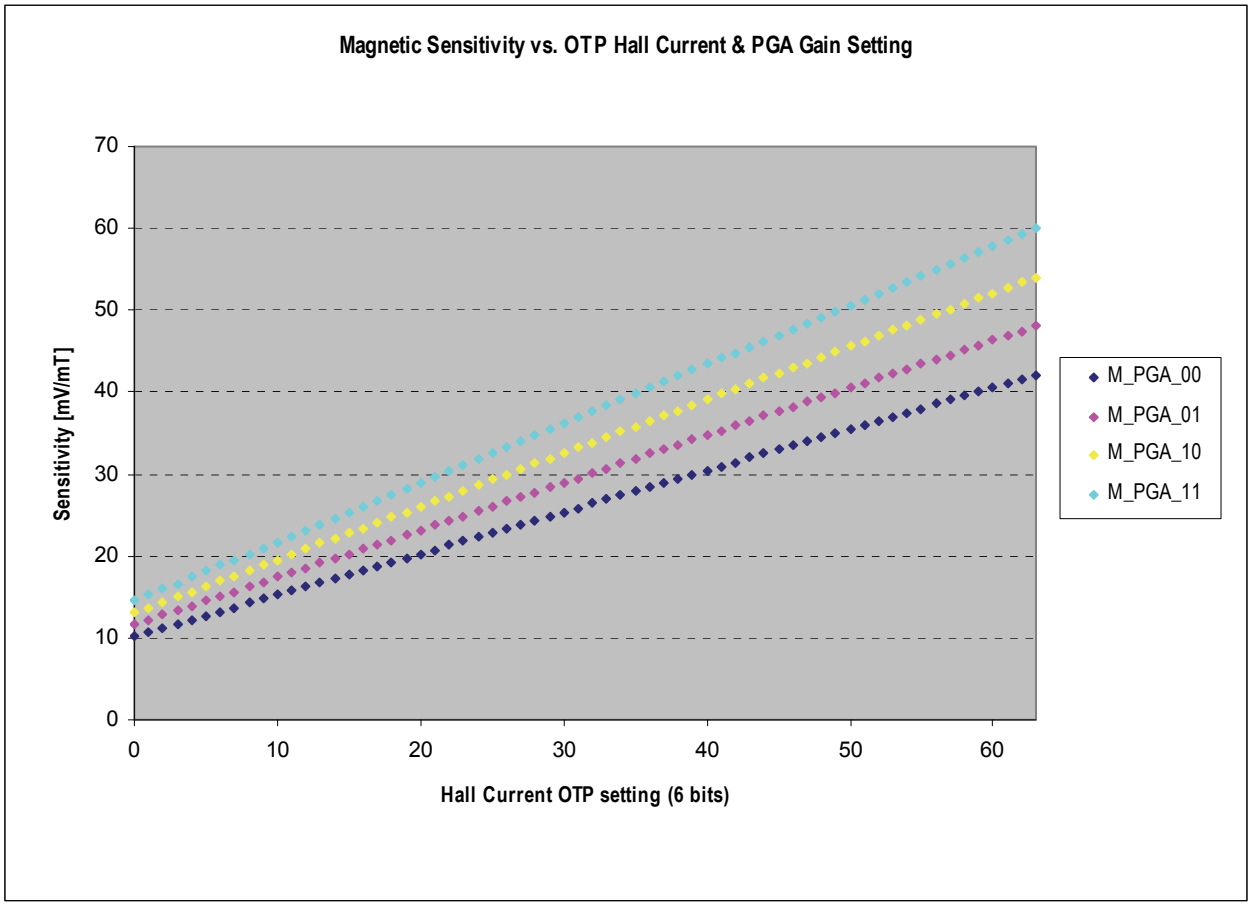
1. Send EN PROG (command 16) in normal mode before accessing the OTP in extended mode.
2. OTP assignment will be defined/updated.

Figure 25:
Sensitivity Gain Settings - Relative Sensitivity in %



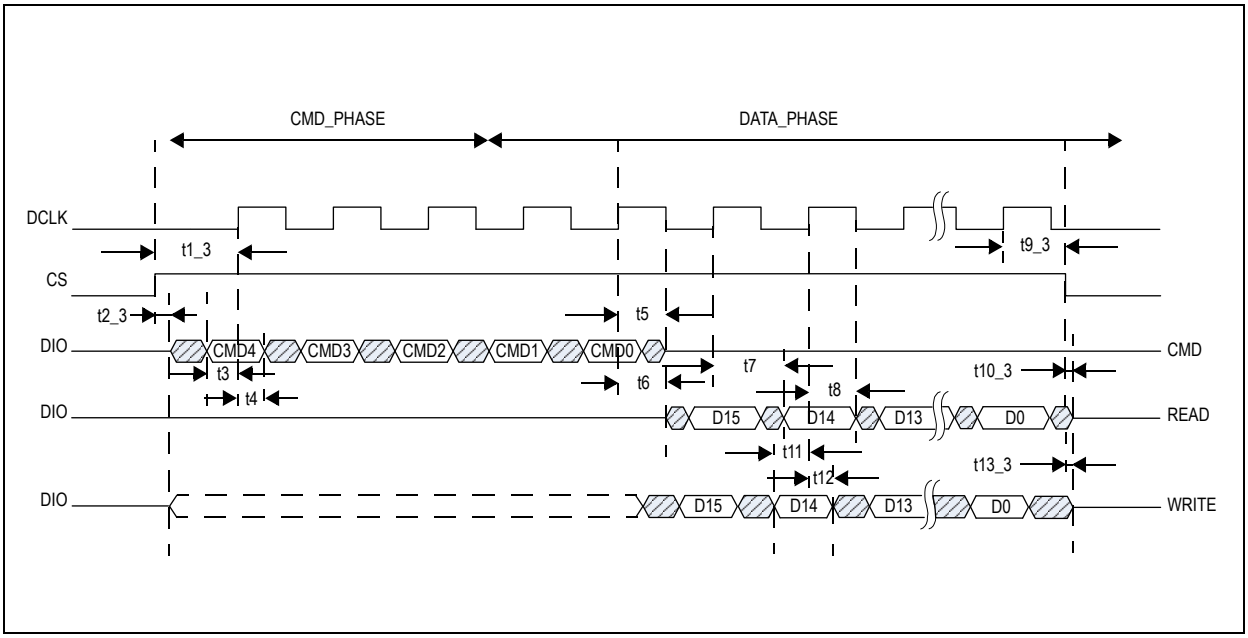
The amplitude of the output signal is programmable via sensitivity (6bit) and/or gain (2bit) settings (see Figure 25).

Figure 26:
Sensitivity Gain Settings - Sensitivity [mV/mT]



Waveform – Digital Interface at Normal Operation Mode

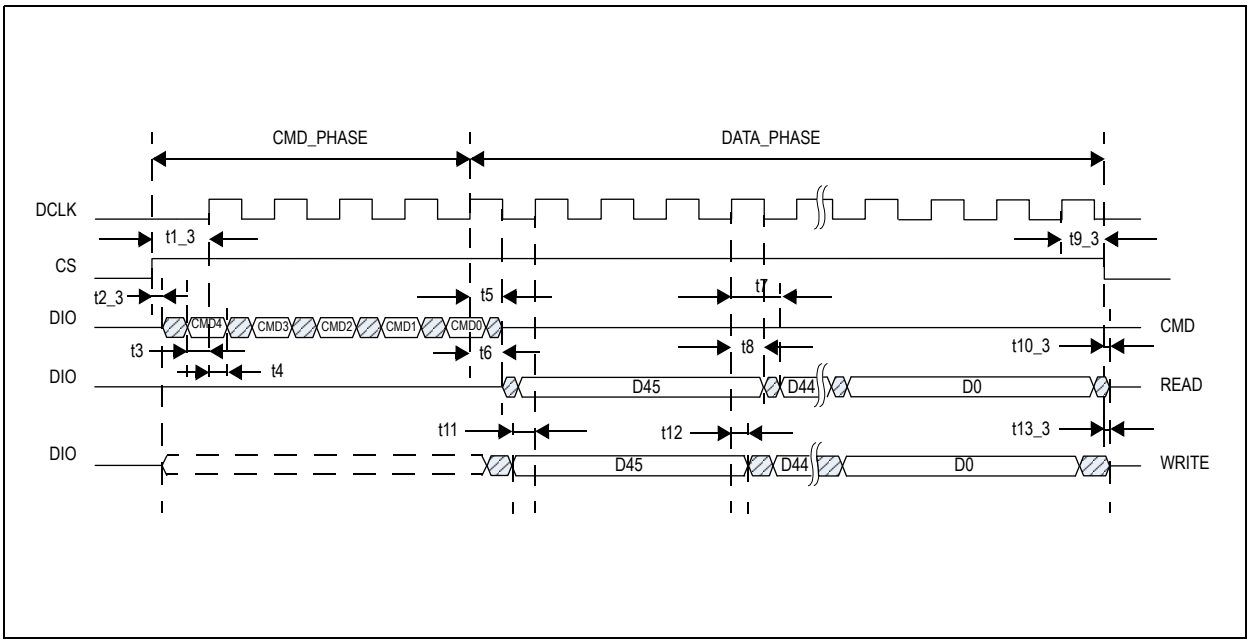
Figure 27:
Digital Interface at Normal Operation Mode



Waveform – Digital Interface at Extended Mode

In the extended mode, the digital interface needs four clocks for one data bit. During this time, the device is able to handle internal signals for special access (e.g. the easy zap interface).

Figure 28:
Digital Interface at Extended Mode



Waveform – Digital Interface at Analog Readback of the Zener Diodes

To be sure that all Zener-Diodes are correctly burned, an analog readback mechanism is defined. Perform the 'READ OTP ANA' sequence according to the command table and measure the value of the diode at the end of each phase.

Figure 29:
Digital Interface at Analog Readback of Zener Diodes

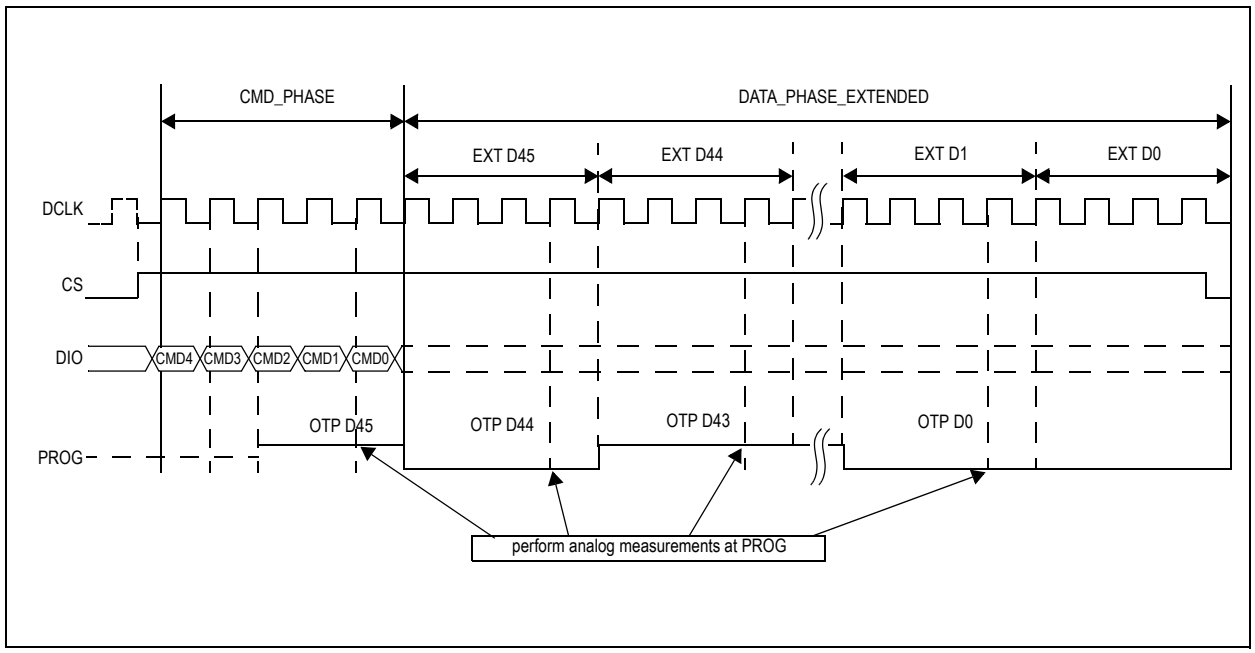


Figure 30:
Serial Bit Sequence (16-Bit Read / Write)

Write Command					Read / Write Data														
C4	C3	C2	C1	C0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

EasyZapp OTP Content

Each AS5215 die has an integrated 32-bit OTP ROM (Easyzapp) for trimming and configuration purposes. The PROM can be programmed via. the serial interface. For irreversible programming, an external programming voltage at PROG pin is needed. For security reasons, the factory trim bits can be locked by a lock bit.

Figure 31:
OTP ROM

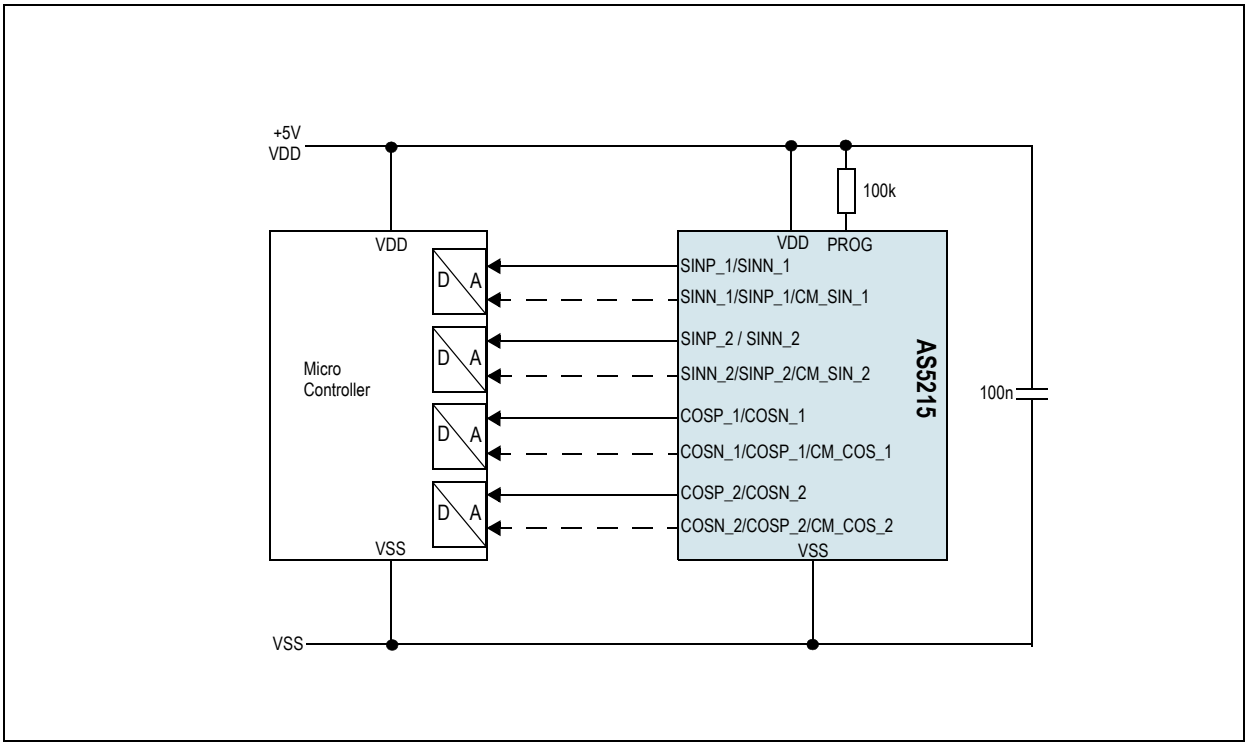
Name	Bit Count	OTP Start	OTP End	Access	Comments
Hall Bias	6	0	5	user	Sets overall sensitivity
DC offset	1	6	6	user	Output DC offset setting
gain	2	7	8	user	Programmable gain amplifier setting
Lock	1	13	13	**ams**	Set in production test
invert_ channel	1	11	11	user	Inverts SIN and COS channel before the PGA for inverted output function
cm_sin	1	10	10	user	Common mode voltage output enabled at SINN / CM pin
cm_cos	1	9	9	user	Common mode voltage output enabled at COSN / CM pin

Note(s):

1. OTP assignment will be defined/updated.

Analog Sin/Cos Outputs with External Interpolator

Figure 32:
Sine and Cosine Outputs for External Angle Calculation



Note(s):

1. We recommend to use a 100kOhm pull-up resistance.
2. Default conditions for unused pins are: DCLK_1/2, CS_1/2, DIO_1/2, TC_1/2, A_TST_1/2, TBO_1/2, TB1_1/2, TB2_1/2, TB3_1/2 connect to VSS.

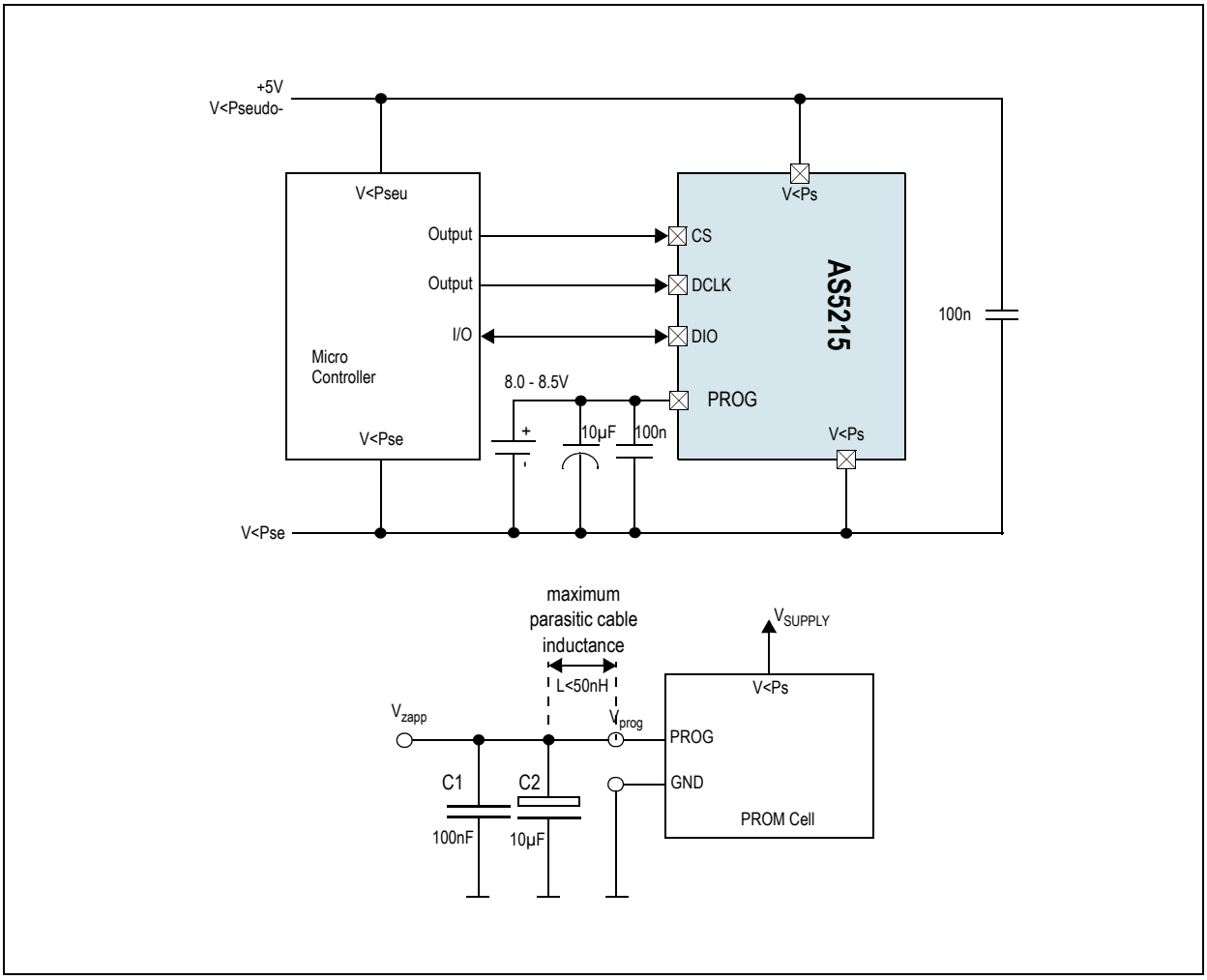
The AS5215 provides analog Sine and Cosine outputs (SINP, COSP) of the Hall array front-end for test purposes. These outputs allow the user to perform the angle calculation by an external ADC + µC, e.g. to compute the angle with a high resolution. The output driver capability is 1mA. The signal lines should be kept as short as possible, longer lines should be shielded in order to achieve best noise performance.

Through the programming of one bit, you have the possibility to choose between the analog Sine and Cosine outputs (SINP, COSP) and their inverted signals (SINN, COSN). Furthermore, by programming the bits <9:10> you can enable the common mode output signals of SIN and COS.

The DC bias voltage is 1.5 or 2.5 V.

OTP Programming and Verification

Figure 33:
OTP Programming Connection



For programming of the OTP, an additional voltage has to be applied to the pin PROG. It has to be buffered by a fast 100nF capacitor (ceramic) and a 10µF capacitor. The information to be programmed is set by command 25. The OTP bits 16 until 45 are used for **ams** factory trimming and cannot be overwritten.

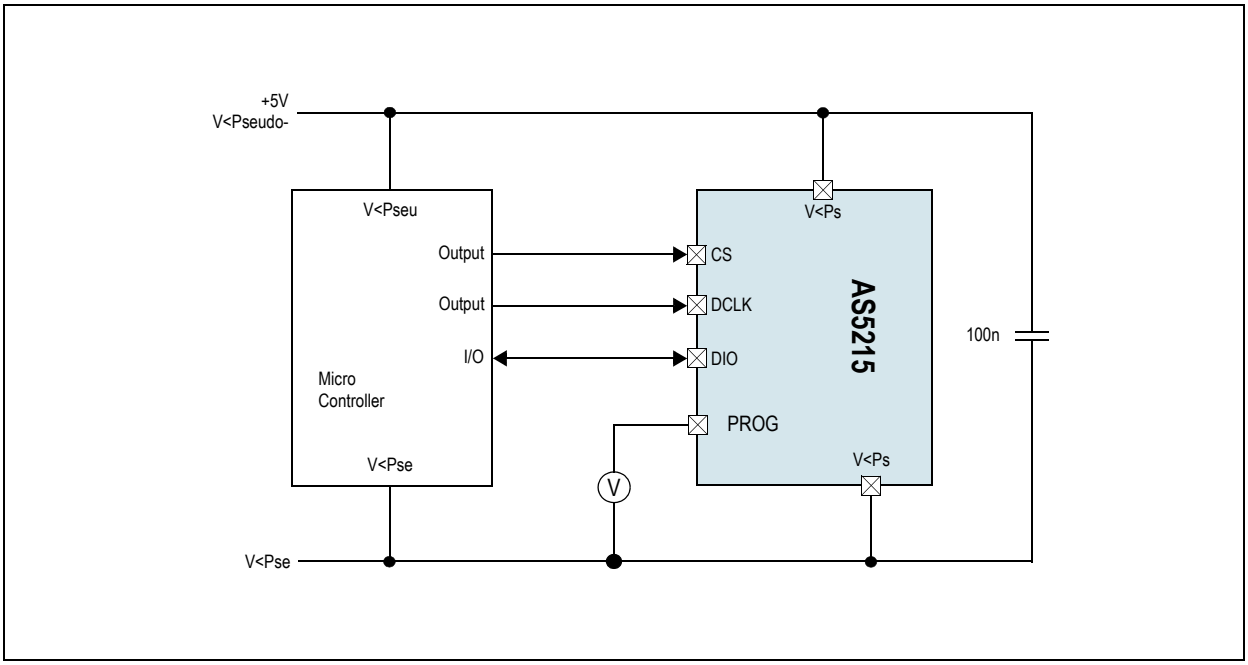
Figure 34:
OTP Programming Parameters

Symbol	Parameter	Min	Max	Unit	Note
VDD	Supply voltage	5	5.5	V	
GND	Ground level	0	0	V	
V_zapp	Programming voltage	8	8.5	V	At pin PROG
T_zapp	Temperature	0	85	°C	
f_clk	CLK frequency		100	kHz	At pin DCLK

After programming, the programmed OTP bits have to be verified by Analog Verification:

By switching into Extended Mode and sending an ANALOG OTP READ command (#9), pin PROG becomes an output, sending an analog voltage with each clock representing a sequence of the bits in the OTP register (starting with D45). A voltage of <500mV indicates a correctly programmed bit (“1”) while a voltage level between 2V and 3.5V indicates a correctly unprogrammed bit (“0”). Any voltage level in between indicates incorrect programming.

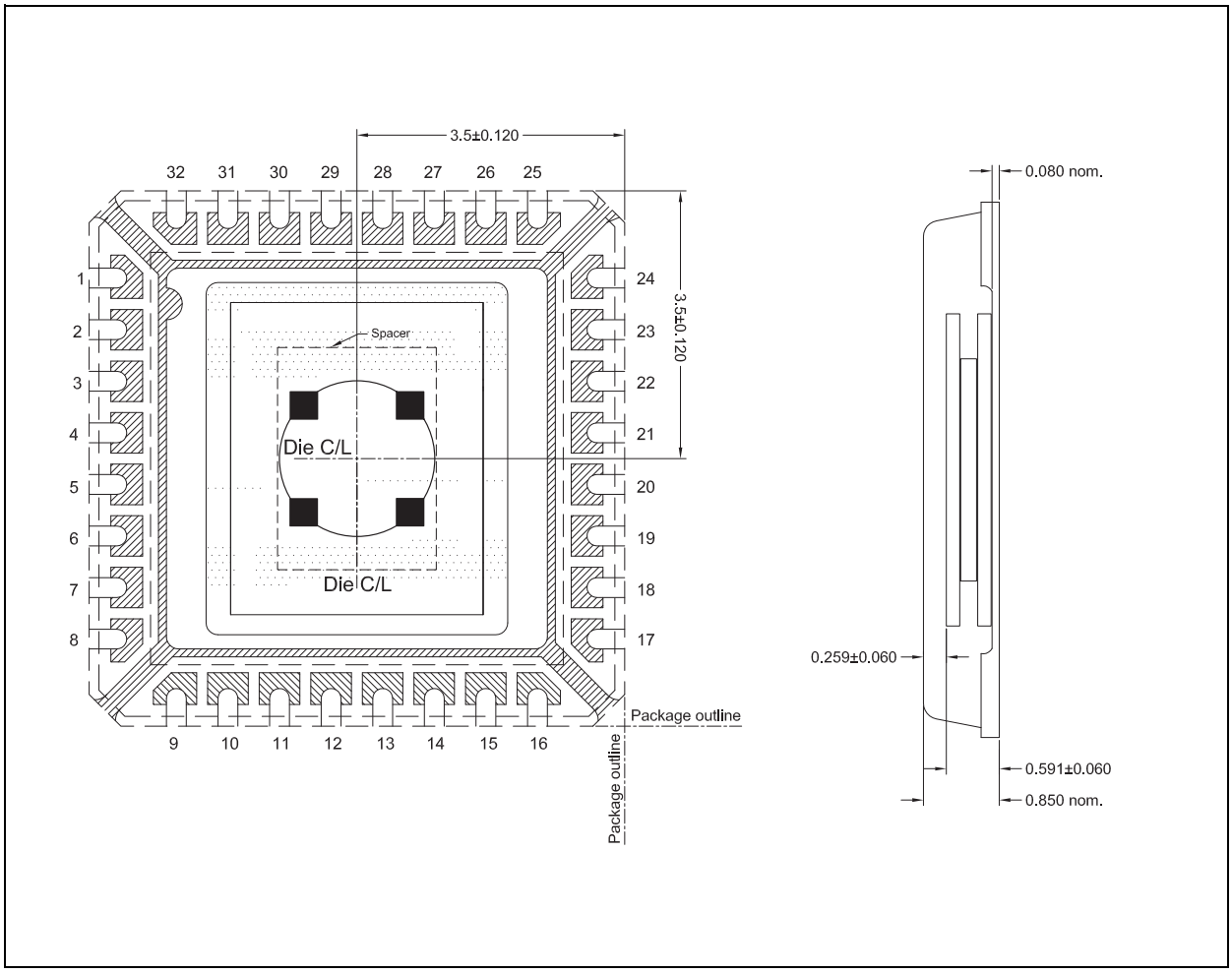
Figure 35:
Analog OTP Verification



Mechanical Data

The internal Hall elements are placed in the center of the package on a circle with a radius of 1 mm.

Figure 36:
Hall Element Position



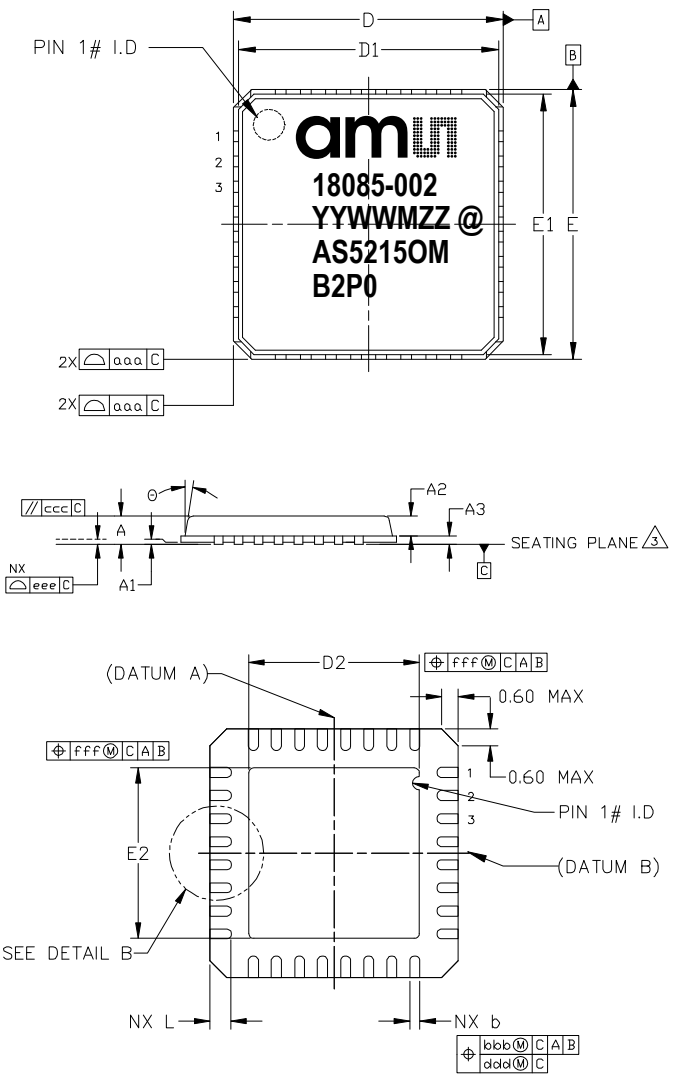
Note(s):

1. All dimensions in mm.
2. Die thickness 0.150mm nom.
3. Adhesive thickness 0.012mm nom.
4. Spacer thickness 0.203mm typ.

Package Drawings & Markings

The devices are available in a 32-pin MLF (7x7mm) package.

Figure 37:
Package Drawings and Dimensions



RoHS Green

Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A2	-	0.65	1.00
A3		0.20 REF	
L	0.50	0.60	0.75
Q	0°	-	14°
b	0.23	0.28	0.35
D		7.00 BSC	
E		7.00 BSC	
e		0.65 BSC	
D1		6.75 BSC	
E1		6.75 BSC	
D2	4.70	4.80	4.90
E2	4.70	4.80	4.90
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

Notes:

1. Dimensions and tolerancing conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Bilateral coplanarity zone applies to the exposed pad as well as the terminal.
4. Radius on terminal is optional.
5. N is the total number of terminals.

Figure 38:
Marking: YYWWVZZ

YY	WW	M	ZZ	@
Manufacturing year	Manufacturing week	Plant identifier	Assembly traceability code	Sublot identifier

Ordering & Contact Information

The devices are available as the standard products shown in Figure 39.

Figure 39:
Ordering Information

Ordering Code	Package	Description	Delivery Form	Delivery Quantity
AS5215OM-HMFP	32-pin MLF (7x7mm)	Sine and cosine analog output magnetic rotary encoder	Tape & Reel	4000 pcs/reel
AS5215OM-HMFM				500 pcs/reel

Buy our products or get free samples online at:
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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Revision Information

Changes from 1.11 (2011-Jun-27) to current revision 2-01 (2016-Mar-03)	Page
1.11 (2011-Jun-27) to 2-00 (2016-Mar-03)	
Content of austriamicrosystems datasheet was converted to latest **ams** design	
Updated Figure 9	7
Updated Figure 10	8
Updated Figure 24	20
Updated text above Figure 35	28
Added Mechanical Data	29
2-00 (2016-Mar-03) to 2-01 (2016-Mar-03)	
Updated notes under Figure 36	29

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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