

# AS3729B

## 8A Power Stage

### General Description

The AS3729B is a companion power stage, intended to be used with AS372x products.

It cannot be used without a DC/DC controller. It contains the power FETs for 2 phases and is capable to handle output currents of 4A per phase.

*Ordering Information and Content Guide appear at end of datasheet.*

### Key Benefits & Features

The benefits and features of AS3729B, 8A Power Stage are listed below:

**Figure 1:**  
**Added Value of Using AS3729B**

| Benefits  | Features   |
|---|--|
| <ul style="list-style-type: none"> <li>Support for single or dual phase operation</li> </ul>    | <ul style="list-style-type: none"> <li>2 phases with separate control input</li> </ul>   |
| <ul style="list-style-type: none"> <li>2 x 4A output stages are running up to 2.7MHz</li> </ul> | <ul style="list-style-type: none"> <li>Separate power NMOS &amp; PMOS for 4A per phase</li> <li>Separate coil current feedback per phase</li> <li>Stand-Alone zero-crossing operation</li> </ul> |
| <ul style="list-style-type: none"> <li>Over-temperature protection</li> </ul>                   | <ul style="list-style-type: none"> <li>Integrated temperature monitoring</li> </ul>  |
| <ul style="list-style-type: none"> <li>Cost effective, small package</li> </ul>                 | <ul style="list-style-type: none"> <li>WL-CSP16: 1.615mm x 1.615mm, 0.4mm pitch</li> </ul>   |

### Applications

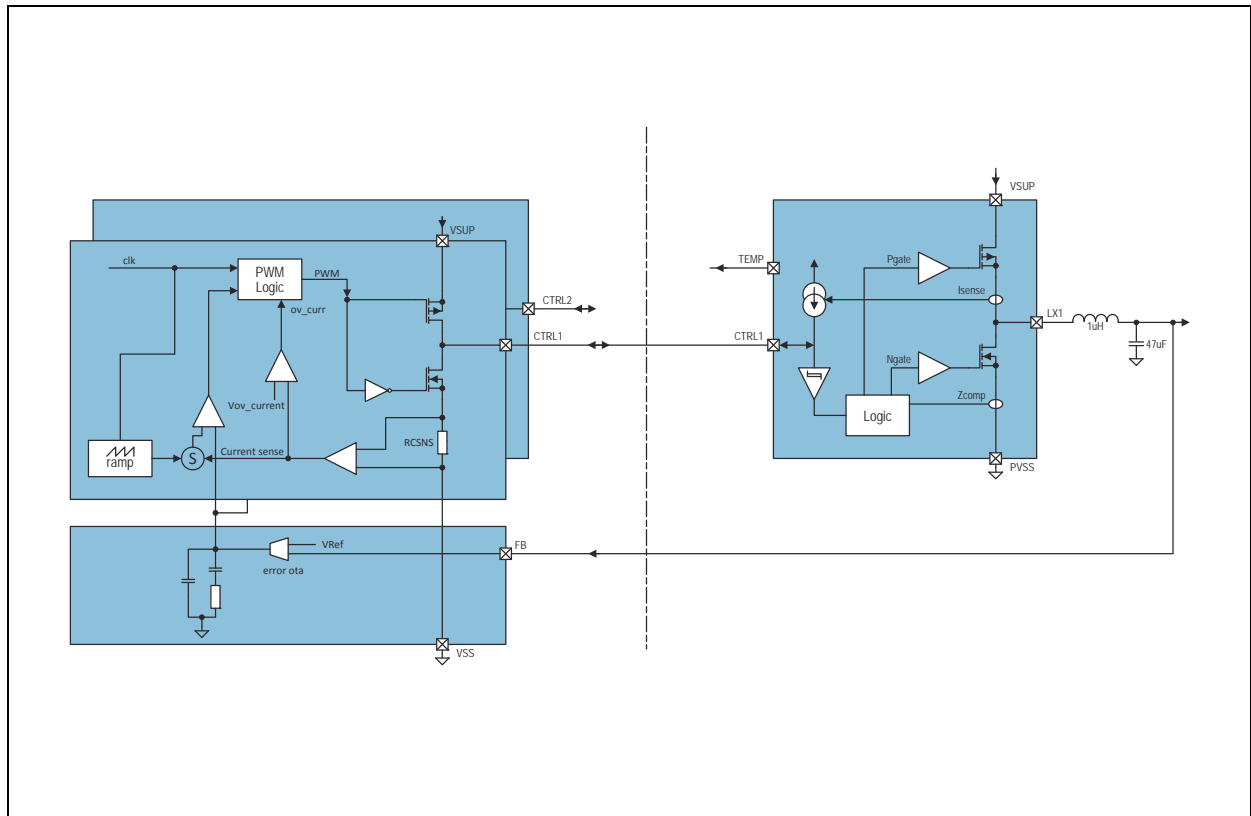
This device is a high current dual-phase DC/DC and ideal for:

- Mobile phones
- Tablets
- Notebooks

## Block Diagram

The functional blocks of this device are shown below:

**Figure 2:**  
**AS3729B Block Diagram**

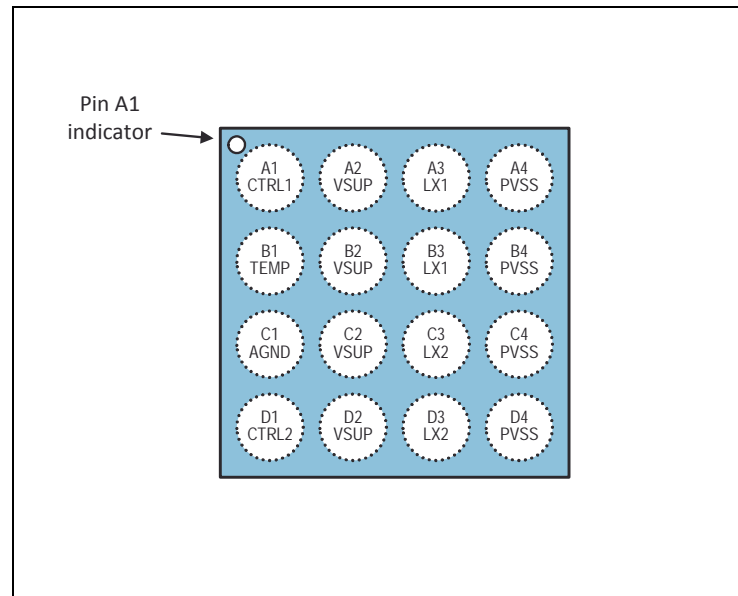


**AS3729B Block Diagram:** This figure shows the block diagram of the DC/DC controller inside the Main PMIC and the AS3729B Power Stage with all relevant system components.

## Pin Assignment

**Figure 3:**  
**16 Balls WL-CSP with 0.4mm Pitch**

**Pin Assignments:** Shows the top view pin assignment of the AS3729B



**Figure 4:**  
**Pin Description**

| Pin Number | Pin Name | Description                             |
|------------|----------|---|
| A1         | CTRL1    | Control IO for phase 1                  |
| B1         | TEMP     | On/Off control and temperature feedback |
| C1         | AGND     | Analog ground                           |
| D1         | CTRL2    | Control IO for phase 2                  |
| A2, B2     | VSUP     | Phase 1 positive supply terminal        |
| C2, D2     | VSUP     | Phase 2 positive supply terminal        |
| A3, B3     | LX1      | Phase 1 switching output to coil        |
| C3, D3     | LX2      | Phase 2 switching output to coil        |
| A4, B4     | PVSS     | Phase 1 negative supply terminal        |
| C4, D4     | PVSS     | Phase 2 negative supply terminal        |

# Absolute Maximum Ratings

Stresses beyond those listed under [Absolute Maximum Ratings](#) may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under [Electrical Characteristics](#) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Figure 5:**  
**Absolute Maximum Ratings**

| Symbol   | Parameter                                   | Min  | Max | Units | Comments   |
|--|---|------|-----|-------|--|
| <b>Electrical Parameters</b>                               |   |      |     |       |  |
|  | Supply voltage to ground 5V pins            | -0.5 | 7.0 | V     | Applicable for pins VSUPx, LXx, CTRLx  |
|  | Supply voltage to ground 3V pins            | -0.5 | 5.0 | V     | Applicable for pin TEMP  |
|  | Voltage difference between ground terminals | -0.5 | 0.5 | V     | Applicable for pins PVSS, AGND   |
|  | Input current (latch-up immunity)           | -100 | 100 | mA    | Norm: JEDEC JESD78   |
| <b>Continuous Power Dissipation (T<sub>A</sub> = 70°C)</b> |   |      |     |       |  |
| P <sub>T</sub>   | Continuous power dissipation                |      | 1   | W     | P <sub>T</sub> <sup>(1)</sup> for WL-CSP16 package (R <sub>THJA</sub> ~ 55K/W) |
| <b>Electrostatic Discharge</b>                             |   |      |     |       |  |
| ESD <sub>HBM</sub>   | Electrostatic discharge HBM                 | ±2   |     | kV    | Norm: JEDEC JESD22-A114F   |

| Symbol   | Parameter                              | Min | Max | Units | Comments                                |
|--|--|-----|-----|-------|---|
| <b>Temperature Ranges and Storage Conditions</b> |  |     |     |       |   |
| $T_A$  | Operating temperature                  | -40 | 85  | °C    |   |
| $R_{THJA}$                                       | Junction to ambient thermal resistance |     |     | °C/W  | $R_{THJA}$ typ. 55K/W                   |
| $T_J$  | Junction temperature                   |     | 125 | °C    |   |
| $T_{STRG}$                                       | Storage temperature range              | -55 | 125 | °C    |   |
| $T_{BODY}$                                       | Package body temperature               |     | 260 | °C    | Norm IPC/JEDEC J-STD-020 <sup>(2)</sup> |
| $RH_{NC}$  | Relative humidity (non condensing)     | 5   | 85  | %     |   |
| MSL  | Moisture sensitivity level             | 1   |     |       | Represents an unlimited floor life time |

**Note(s) and/or Footnote(s):**

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices"

## Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

**Figure 6:**  
Electrical Characteristics

| Symbol              | Parameter                             | Note                                 | Min | Typ | Max              | Unit |
|---------------------|---------------------------------------|--------------------------------------|-----|-----|------------------|------|
| $V_{IN}$            | Input voltage                         | Pin VSUPx                            | 2.5 |     | 5.5              | V    |
|                     |                                       | Pin CTRLx                            | 0   |     | 5.5              | V    |
|                     |                                       | Pin TEMP                             | 0   |     | 3.6              | V    |
| $I_{LIMIT}$         | Peak coil current limit               | Single phase                         |     |     | 4.8              | A    |
| $I_{LOAD}$          | Load current single phase             | Continuous load current              | 0   |     | 3                | A    |
|                     |                                       | Peak load current                    |     |     | 4 <sup>(1)</sup> |      |
| $R_{PMOS}$          | P-switch ON resistance <sup>(2)</sup> | Single phase                         |     | 40  | 70               | mΩ   |
| $R_{NMOS}$          | N-switch ON resistance <sup>(2)</sup> | Single phase                         |     | 20  | 35               | mΩ   |
| $f_{SW}$            | Switching frequency                   | Supplied by DC/DC controller         |     | 1.3 | 3                | MHz  |
| $I_{Q\_force\_PWM}$ | Quiescent current PWM                 | TEMP pin high, force PWM mode active |     | 6.2 |                  | mA   |
| $I_{Q\_low\_power}$ | Quiescent current LP                  | TEMP pin high, low power mode active |     | 21  |                  | μA   |
| $I_{power\_off}$    | Power-Off current                     | No current into pin TEMP             |     | ±1  |                  | μA   |
| $R_{discharge}$     | Active discharge                      | Single phase                         |     | 16  |                  | Ω    |

**Electrical Characteristics:** Shows the Electrical Characteristics of the Step Down DC/DC Power Stage. VSUP = 3.8V,  $T_A = 25^\circ\text{C}$  (unless otherwise specified)

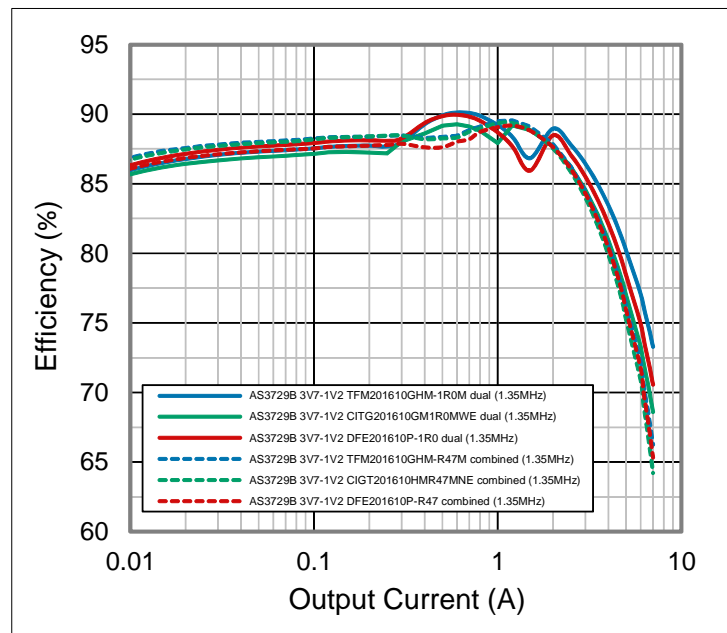
**Note(s) and/or Footnote(s):**

1. Maximum value only for pulsed peak current
2. MOS transistor only without package parasitic

## Typical Operating Characteristics

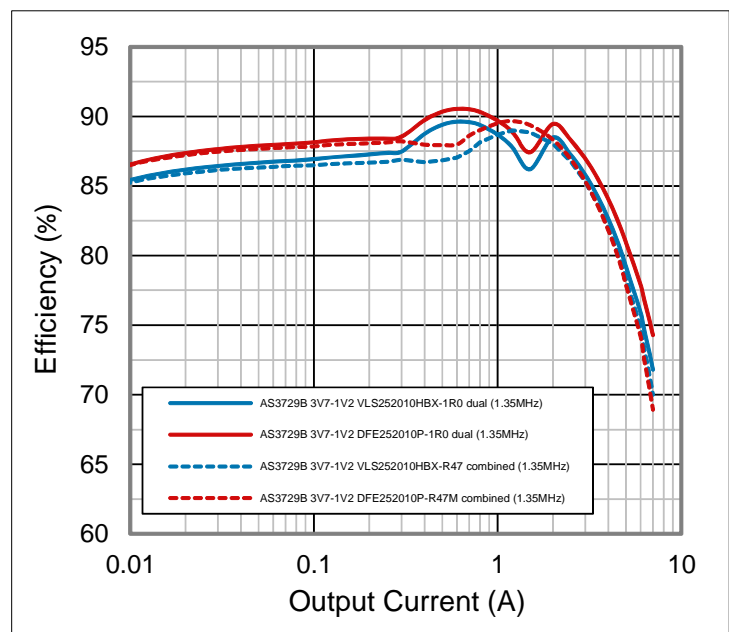
**AS3729B Step Down DC/DC:** Shows the Efficiency of AS3729B of various coil types in a 2016 package in dual and combined mode. For the dual mode two 1uH coils are used and for the combined mode one 470nH coil. VSUP = 3.7V, VOUT = 1.2V, 1.35MHz operation,  $T_A = 25^\circ\text{C}$

**Figure 7:**  
Efficiency vs. Output Current for 2016 Coil Types



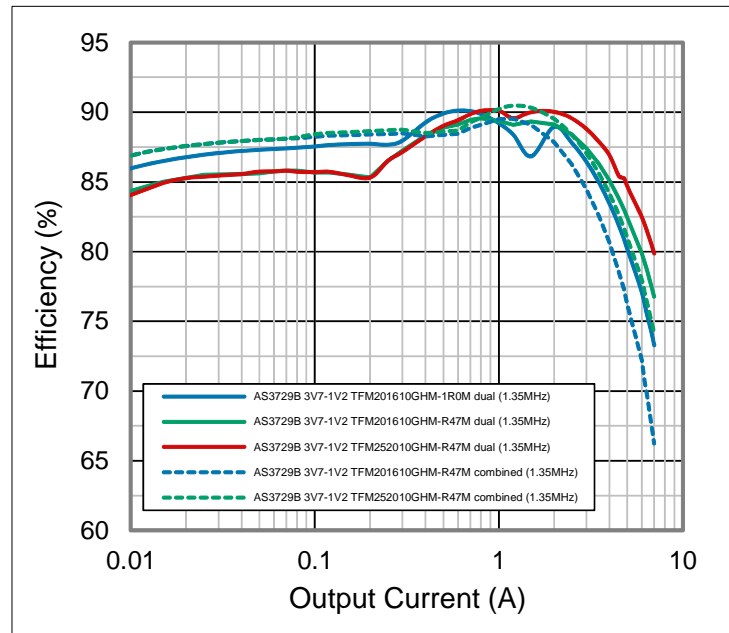
**Figure 8:**  
Efficiency vs. Output Current for 2520 Coil Types

**AS3729B Step Down DC/DC:** Shows the Efficiency of AS3729B of various coil types in a 2520 package in dual and combined mode. For the dual mode two 1uH coils are used and for the combined mode one 470nH coil. VSUP = 3.7V, VOUT = 1.2V, 1.35MHz operation,  $T_A = 25^\circ\text{C}$



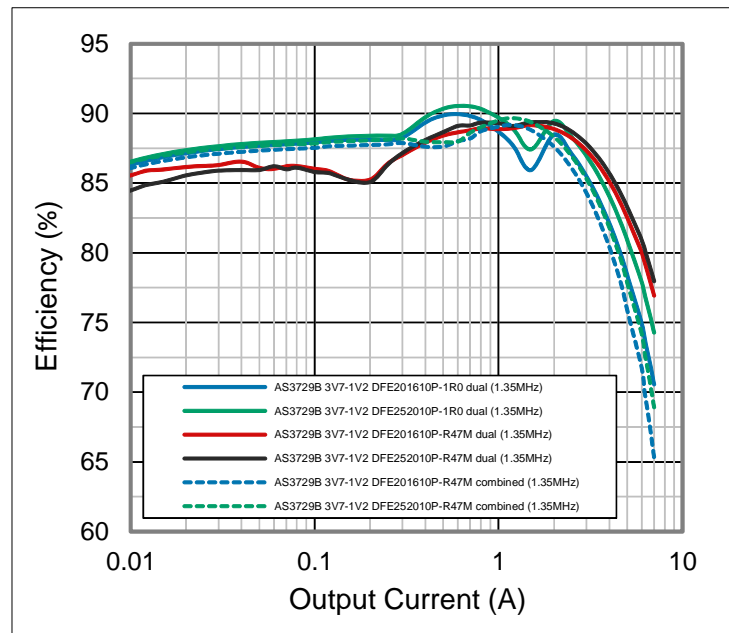
**Figure 9:**  
Efficiency vs. Output Current for Various TDK Coils

**AS3729B Step Down DC/DC:** Shows the Efficiency of AS3729B of various TDK coils in dual and combined mode. VSUP = 3.7V, VOUT = 1.2V, 1.35MHz operation,  $T_A = 25^\circ\text{C}$



**Figure 10:**  
Efficiency vs. Output Current for Various Toko Coils

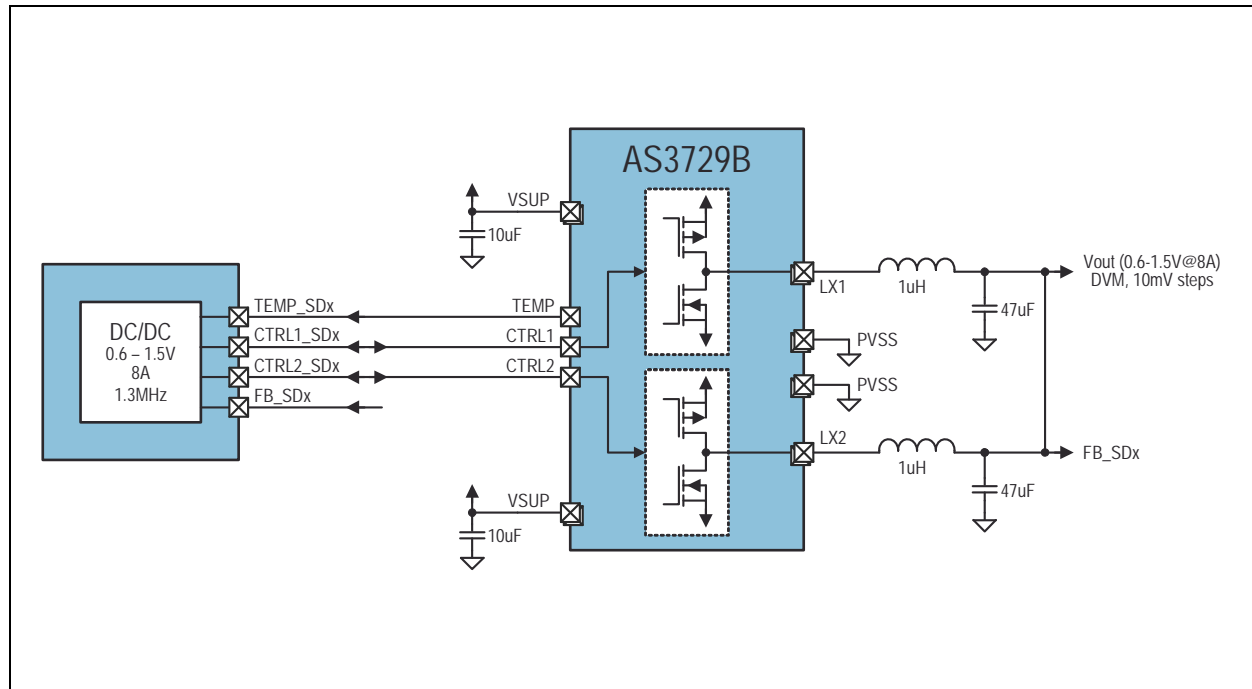
**AS3729B Step Down DC/DC:** Shows the Efficiency of AS3729B of various Toko coils in dual and combined mode. VSUP = 3.7V, VOUT = 1.2V, 1.35MHz operation,  $T_A = 25^\circ\text{C}$





## Application Information

**Figure 11:**  
Typical Application Circuit



**AS3729B Typical Application:** This figure shows the connection of the DC/DC controller and the AS3729B Power Stage.

## External Components

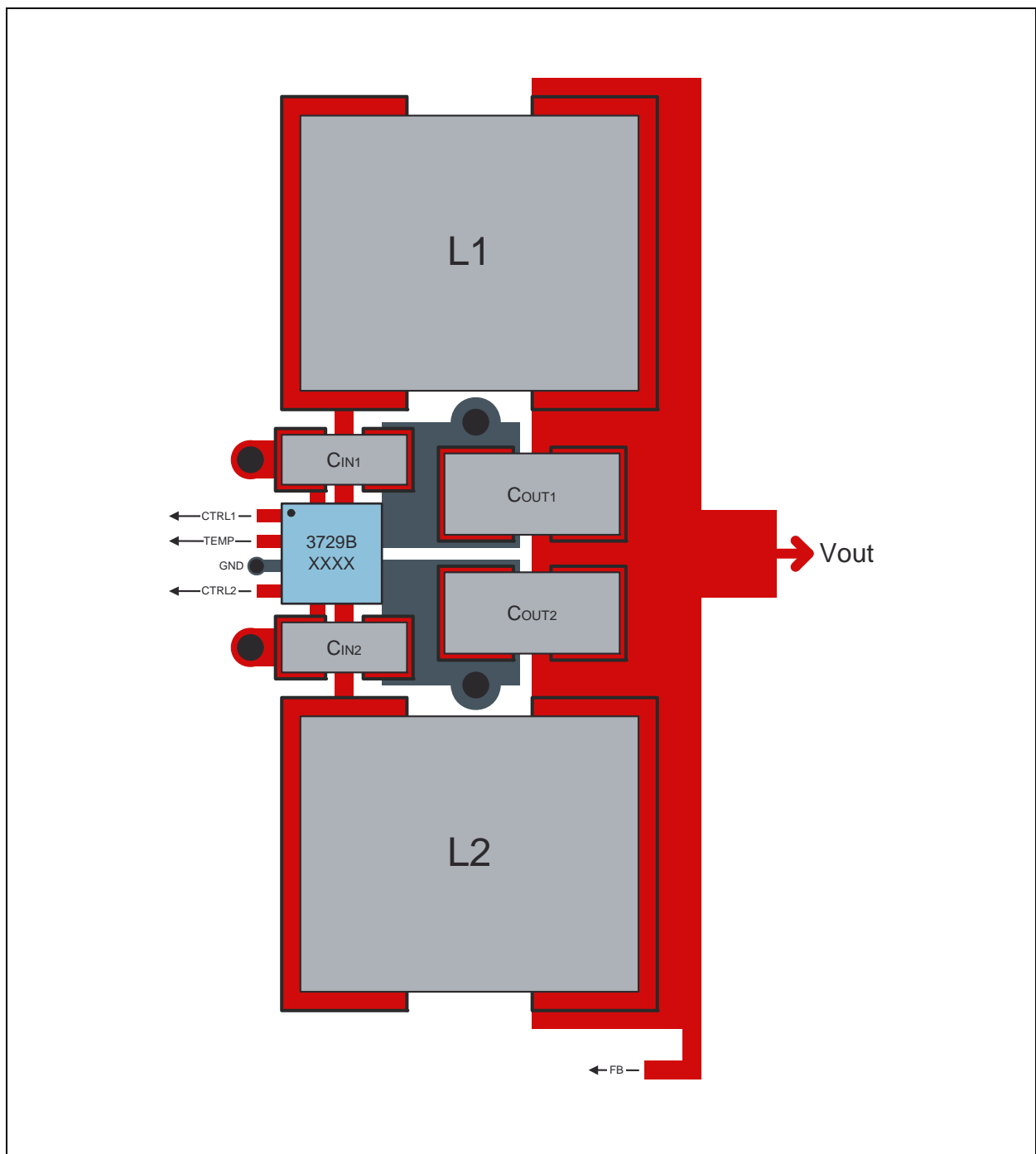
**Figure 12:**  
Step Down DC/DC Power Stage External Components

| Symbol                               | Parameter        | Note                                     | Min | Typ | Max | Unit    |
|--------------------------------------|------------------|--|-----|-----|-----|---------|
| <b>External Components per Phase</b> |                  |  |     |     |     |         |
| $C_{FB}$                             | Output Capacitor | Ceramic X5R or X7R, high performance     | 64  | 82  |     | $\mu F$ |
|                                      |                  | Ceramic X5R or X7R, cost optimized       | 32  | 47  |     | $\mu F$ |
| $C_{VSUP}$                           | Input Capacitor  | Ceramic X5R or X7R                       | 6   | 10  |     | $\mu F$ |
| L                                    | Inductor         | 5A rated, 1.3MHz operation, low $R_{ON}$ | 0.5 | 1   |     | $\mu H$ |

**External Components:** Shows the recommended values of the needed external components of the Step Down DC/DC Power Stage

## PCB Layout

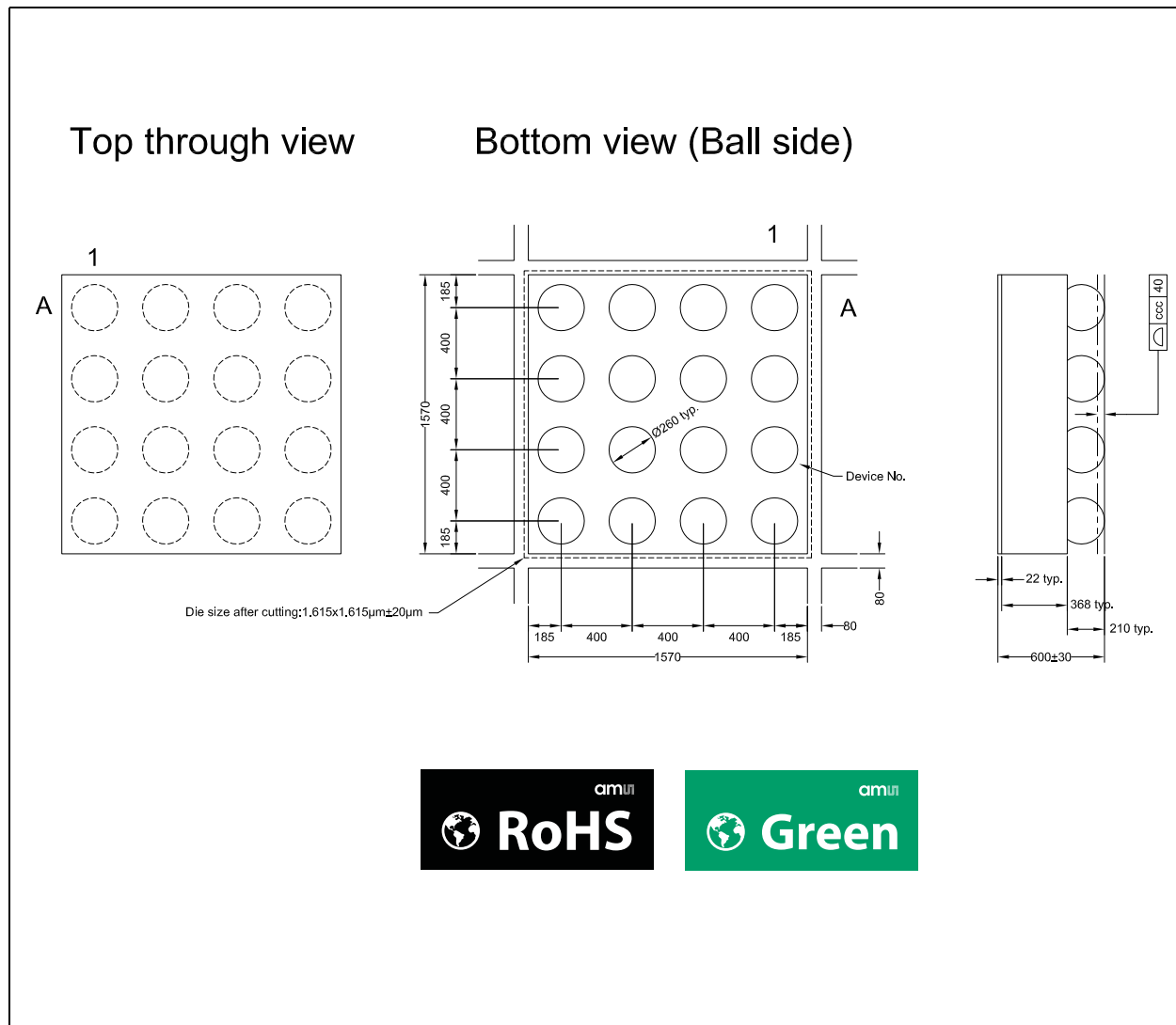
**Figure 13:**  
Layout Guidelines



**Layout Guidelines:** This figure shows the recommended layout and placement of the external components for the 2-phase AS3729B Power Stage

## Package Drawings & Markings

**Figure 14:**  
**16-Pin WL-CSP with 0.4mm Pitch**



**Note(s) and/or Footnote(s):**

1. Pin 1 = A1
2. ccc coplanarity
3. All dimensions in µm

Figure 15:  
16-Pin WL-CPS Marking

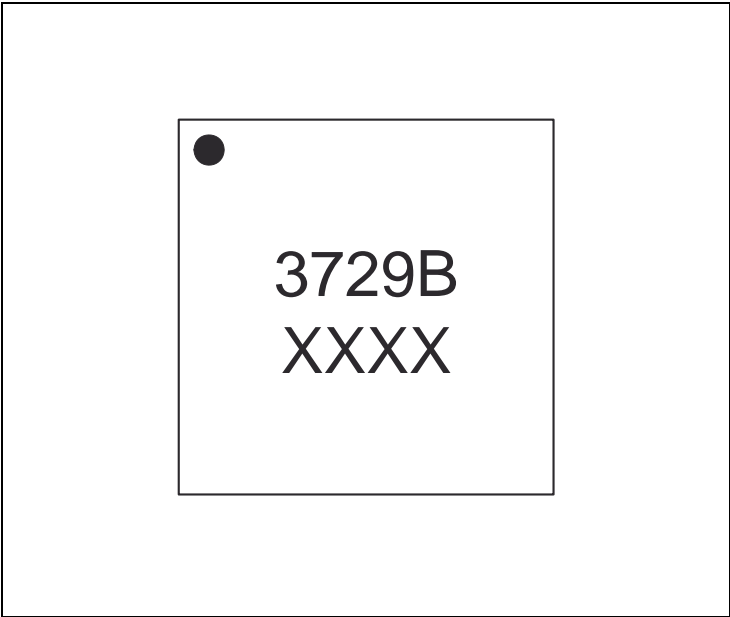


Figure 16:  
Packaging Code

|           |
|-----------|
| XXXX      |
| Tracecode |

## Ordering & Contact Information

**Figure 17:**  
**Ordering Information**

| Ordering Code | Package       | Marking | Delivery Form | Delivery Quantity |
|---------------|---------------|---------|---------------|-------------------|
| AS3729B-BWLM  | 16-pin WL-CSP | 3729B   | Tape & Reel   | 500 pcs/reel      |
| AS3729B-BWLT  |               |         |               | 12000 pcs/reel    |

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### Headquarters

ams AG  
Tobelbaderstrasse 30  
8141 Unterpremstaetten  
Austria, Europe

Tel: +43 (0) 3136 500 0

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| Document Status          | Product Status  | Definition   |
|--------------------------|-----------------|--|
| Product Preview          | Pre-Development | Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice  |
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## Revision Information

| Changes from 1-01 (2014-Mar) to current revision 1-03 (2015-Sep-28) | Page |
|---|------|
| <b>1-01 (2014-Mar) to 1-02 (2015-Sep-21)</b>                        |      |
| Content was updated to the latest <b>ams</b> design                 |      |
| Updated Figure 16   | 12   |
| Updated Figure 17   | 13   |
| <b>1-02 (2015-Sep-21) to 1-03 (2015-Sep-28)</b>                     |      |
| Updated Figure 14   | 11   |

**Note(s) and/or Footnote(s):**

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

## Content Guide

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| <b>17</b> | <b>Revision Information</b>                     |

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