

INTEGRATED COMPLEMENTARY BUFFERED-GATE SCRS FOR DUAL POLARITY SLIC OVERVOLTAGE PROTECTION

TISP9110MDM Overvoltage Protector

High Performance Protection for SLICs with +ve and -ve Battery Supplies

- Wide -110 V to +110 V Programming Range
- Low 5 mA max. Gate Triggering Current
- Dynamic Protection Performance Specified for International Surge Waveshapes

Applications include:

- Wireless Local Loop
- Access Equipment
- Regenerated POTS
- VOIP Applications

Rated for International Surge Wave Shapes

Wave Shape	Standard	I _{PPSM} A
2/10	GR-1089-CORE	150
10/700	ITU-T K.20/21/45	80
10/1000	GR-1089-CORE	50

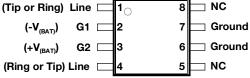
Description

The Model TISP9110MDM is a programmable overvoltage protection device designed to protect modern dual polarity supply rail ringing SLICs (Subscriber Line Interface Circuits) against overvoltages on the telephone line. Overvoltages can be caused by lightning, a.c. power contact and induction. Four separate protection structures are used; two positive and two negative to provide optimum protection during Metallic (Differential) and Longitudinal (Common Mode) protection conditions in both polarities. Dynamic protection performance is specified under typical international surge waveforms from Telcordia GR-1089-CORE, ITU-T K.44 and YD/T 950.

The Model TISP9110MDM is programmed by connecting the G1 and G2 gate terminals to the negative (-V $_{(BAT)}$) and positive (+V $_{(BAT)}$) SLIC Battery supplies respectively. This creates a protector operating at typically +1.4 V above +V $_{(BAT)}$ and -1.4 V below -V $_{(BAT)}$ under a.c. power induction and power contact conditions.

Agency Recognition Description UL File Number: E215609

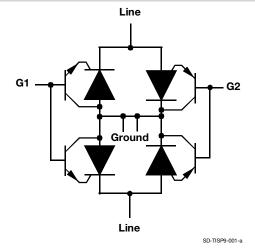
8-SOIC (210 mil) Package (Top View)



NC - No internal connection
Terminal typical application names shown in
parenthesis

MD-8SOIC(210)-003-a

Device Symbol



The protector gate circuitry incorporates 4 separate buffer transistors designed to provide independent control for each protection element. The gate buffer transistors minimize supply regulation issues by reducing the gate current drawn to around 5 mA, while the high voltage base emitter structures eliminate the need for expensive reverse bias protection gate diodes.

The Model TISP9110MDM is rated for common surges contained in regulatory requirements such as ITU-T K.20, K.45, Telcordia GR-1089-CORE, YD/T 950. With the use of appropriate overcurrent protection devices such as the Bourns® Multifuse® and Telefuse™ devices, circuits can be designed to comply with modern telecom standards.

How To Order

Device	Package	Carrier	Order As	Marking Code	Standard Quantity
TISP9110MDM	8-SOIC (210 mil)	Embossed Tape Reeled	TISP9110MDMR-S	9110M	2000

TISP9110MDM Overvoltage Protector

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Absolute Maximum Ratings, T_A = 25 °C (Unless Otherwise Noted)

Rating	Symbol	Value	Unit	
Repetitive peak off-state voltage				
$V_{G1(Line)} = 0, V_{G2} \ge +5 \text{ V}$		-120	V	
$V_{G2(Line)} = 0, V_{G1} \ge -5 V$		+120		
Non-repetitive peak impulse current (see Notes 1, 2, 3 and 4)				
2/10 μs (Telcordia GR-1089-CORE)		±150		
5/310 µs (ITU-T K.20, K.21 & K.45, K.44 open-circuit voltage wave shape 10/700 ms)	I _{PPSM}	±80	Α	
10/1000 μs (Telcordia GR-1089-CORE)		±50		
Non-repetitive peak on-state current, 50 Hz / 60 Hz (see Notes 1, 2, 3 and 5)				
0.2 s		9.0		
1 s	I _{TSM}	5.0	Α	
900 s		1.7		
Maximum negative battery supply voltage	V_{G1M}	-110	V	
Maximum positive battery supply voltage	V_{G2M}	+110	V	
Maximum differential battery supply voltage	$\Delta V_{(BAT)M}$	220	V	
Junction temperature	T_J	-40 to +150	°C	
Storage temperature range	T _{stg}	-65 to +150	°C	

- NOTES: 1. Initially the device must be in thermal equilibrium with T_J = 25 °C. The surge may be repeated after the device returns to its initial conditions.
 - 2. The rated current values may be applied to either of the Line to Ground terminal pairs. Additionally, both terminal pairs may have their rated current values applied simultaneously (in this case the Ground terminal current will be twice the rated current value of a single terminal pair).
 - 3. Rated currents only apply if pins 6 & 7 (Ground) are connected together.
 - 4. Applies for the following bias conditions: V_{G1} = -20 V to -110 V, V_{G2} = 0 V to +110 V.
 - 5. EIA/JESD51-2 environment and EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Electrical Characteristics for any Section, T_A = 25 °C (Unless Otherwise Noted)

	Parameter	Test Conditions		Min	Тур	Max	Unit
I _D	Off-state current	$V_D = V_{DRM}, V_{G1(Line)} = 0, V_{G2} \ge +5 \text{ V}$	T _A = 25 °C T _A = 85 °C			-5 -50	μΑ
טי		$V_D = V_{DRM}, V_{G2(Line)} = 0, V_{G1} \ge -5 \text{ V}$	T _A = 25 °C T _A = 85 °C	l .		+5 +50	μπ
I _{G1(Line)}	Negative-gate leakage current	V _{G1(Line)} = -220 V				- 5	μΑ
I _{G2(Line)}	Positive-gate leakage current	$V_{G2(Line)} = +220 \text{ V}$				+5	μΑ
V _{G1L(BO)}	Gate - Line impulse breakover voltage	$V_{G1} = -100 \text{ V}, I_T = -100 \text{ A (see Note 6)}$ $V_{G1} = -100 \text{ V}, I_T = -30 \text{ A}$	2/10 μs 10/1000 μs	l .		-15 -11	٧
V _{G2L(BO)}	Gate - Line impulse breakover voltage	V_{G2} = +100 V, I_T = +100 A (see Note 6) V_{G2} = +100 V, I_T = +30 A	2/10 μs 10/1000 μs			+15 +11	٧
I _H -	Negative holding current	$V_{G1} = -60 \text{ V}, I_T = -1 \text{ A}, di/dt = 1 \text{ A/ms}$		-150			mA
I _{G1T}	Negative-gate trigger current	$I_T = -5 \text{ A,t }_{p(g)} \ge 20 \ \mu\text{s, V}_{G1} = -60 \text{ V}$				+5	mA
I _{G2T}	Positive-gate trigger current	$I_T = 5 \text{ A,t }_{p(g)} \ge 20 \ \mu\text{s}, \ V_{G2} = 60 \text{ V}$				- 5	mA
C _O	Line - Ground off-state capacitance	f = 1 MHz, V _D = -3 V, G1 & G2 open circuit			33		pF

NOTE: 6. Voltage measurements should be made with an oscillosc ope with limited bandwidth (20 MHz) to avoid high frequency noise.

Thermal Characteristics, $T_A = 25$ °C (Unless Otherwise Noted)

ſ	Parameter	Test Conditions	Min	Тур	Max	Unit
ſ	R Illinction to ambient thermal registrance	EIA/JESD51-7 PCB, EIA/JESD51-2 Environment, P _{TOT} = 4 W (See Note 7)		55		°C/W

NOTE 7. EIA/JESD51-7 high effective thermal conductivity test board (multi-layer) connected with 0.6 mm printed wiring track widths.

Parameter Measurement Information

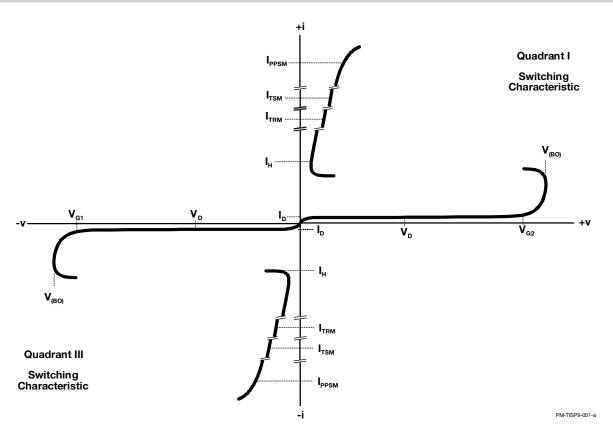


Figure 1. Voltage-Current Characteristic Unless Otherwise Noted, All Voltages are Referenced to the Ground Terminal

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Typical Characteristics

OFF-STATE CAPACITANCE

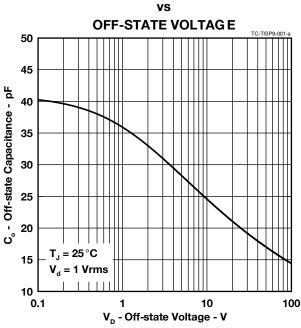
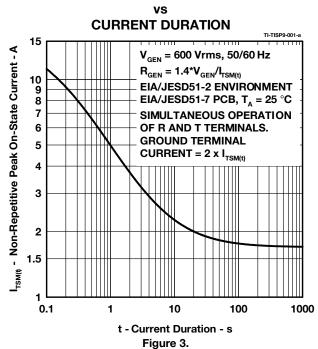


Figure 2.

Thermal Information

NON-REPETITIVE PEAK ON-STATE CURRENT



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APPLICATIONS INFORMATION

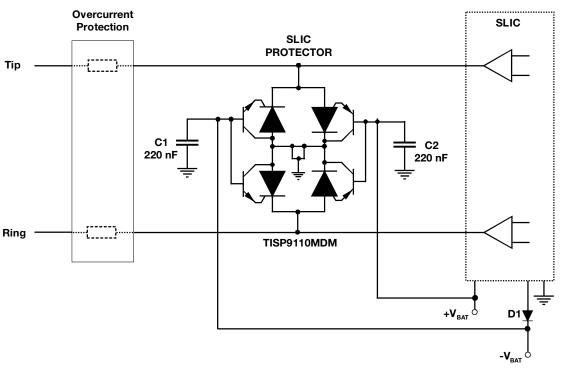


Figure 4. Typical Application Diagram

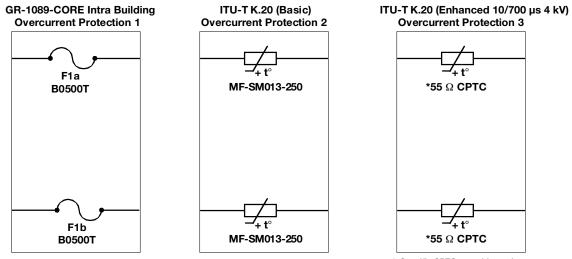


Figure 5. Typical Overcurrent Protection

* Specific CPTC can withstand 10/700 4 kV without primary protector.

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