

VCU110 EXAMAX® LOOPBACK CARD

Mimic IEEE 802.3 Reference Design Channels with 25 dB Loss

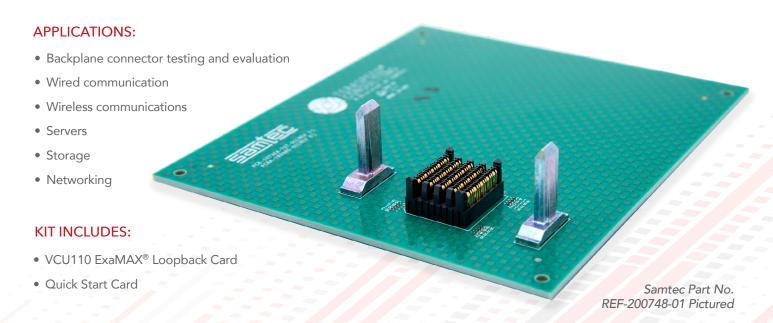
As FPGAs take over the data center, system-level architects require technical support over the entire high-speed serial channel data path. FPGA vendors like Xilinx are working with interconnect partners like Samtec to emulate next generation data center architectures in their FPGA evaluation, development and characterization kits.

As an example, the Xilinx Virtex® UltraScale™ FPGA VCU110 Development Kit features the ExaMAX® high-speed backplane connector system. Pairing these solutions together provides a platform for demonstrating 28 Gbps performance from an FPGA over a backplane.

The VCU110 ExaMAX® Loopback Card routes 8 GTY MGTs from the Xilinx Virtex® UltraScale™ FPGA through the ExaMAX® mated connector pair and back to the FPGA. Four GTY loopback channels contain little or no insertion loss. The summation of VCU110 insertion loss and the engineered loss on four additional GTY loopback channels satisfies the IEEE 802.3bj insertion loss requirements. The combined solution enables evaluation and development of routing FPGA transceivers in a table-top environment.

FEATURES:

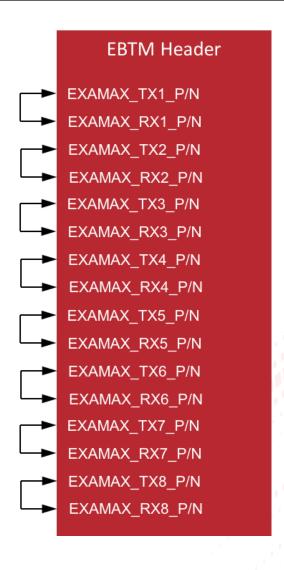
- Compact form factor (5.25" x 6") simplifies mating to traditional right-angle backplane receptacles
- ExaMAX[®] 2.00 mm pitch vertical header assembly (Samtec P/N: EBTM-4-10-2.0-S-VT-1)
- Attaches to J116 (Samtec P/N: EBTF-4-10-2.0-S-RA-1) on Xilinx Virtex[®] UltraScale[™] FPGA VCU110 Development Kit
- Features optimize SI performance via Samtec Final Inch® BOR PCB trace routing for EBTM series connector
- Supports 8 high-speed multi-gigabit transceivers (Tx and Rx) operating up to 28 Gbps



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For additional information or support on your next generation high-speed backplane connector design, please visit **www.samtec.com/backplane** or contact **HSBP@samtec.com**.

VCU110 EXAMAX® LOOPBACK CARD BLOCK DIAGRAM





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