

# UG412: Class 4, 30 W, 12 V EMI-Compliant, Isolated EVB for the Si34061

The Si34061 isolated Flyback evaluation board is a reference design for power supplies in Power over Ethernet (PoE) Powered Device (PD) applications.

The Si34061-EVB-EXT-12V maximum output is Class 4 power (30 W with isolated 12 V output).

The Si34061 IC integrates an IEEE 802.03at compatible PoE+ interface as well as a peak-current-control dc-dc controller.

#### KEY FEATURES

- IEEE 802.03at compatible
- High converter efficiency (> 90%)
- EMI compliant design
- · Synchronous rectification
- · High flexibility
- Integrated transient overvoltage protection
- Thermal shutdown protection
- 5x5 mm 24-pin QFN



Parameter	Condition	Specifications
Ordering part number	—	Si34061FB12V4KIT
DSE input voltago rango	Up to Pout = 25.5 W, Connector J1	42.5 to 57 V
PSE input voltage range	Up to Pout = 12.95 W, Connector J1	37 to 57 V
Wall adapter input voltage range	Connector J3	33 to 57 V
PoE Type/Class	Type 2/Class 4	IEEE 802.3at
Output voltage/current	Connectors J4-J5	12 V / 2.5 A
Efficiency, end-to-end	V <sub>IN</sub> = 48 V from wall adapter	92.5 %
Efficiency, dc-dc converter	V <sub>IN</sub> = 50 V from PSE	92.5 %
Efficiency, end-to-end	V <sub>IN</sub> = 50 V from PSE	89.8 %
Switching frequency	R <sub>FREQ</sub> (R14) = 95.3 kΩ	200 kHz
Conducted EMI	EN55032, average and peak detector	Passed
Radiated EMI	EN55032 Class B	Passed

## **Table of Contents**

1. Kit Description and Powering up the Si34061-EVB-EXT-12V
2. Si34061-EVB-EXT-12V Board Schematics.
3. Conversion Efficiency of the Si34061-EVB-EXT-12V Board
4. SIFOS PoE Compatibility Test Results
5. Feedback Loop Phase and Gain Measurement Results (Bode Plots)
6. Load Step Transient Measurement Results
7. Output Voltage Ripple
8. Soft Start Protection
9. Output Short Protection
10. Pulse Skipping at No-Load Condition
11. Adjustable EVB Current Limit.
12. Tunable Switching Frequency
13. Synchronous Rectification
14. Maintain Power Signature
15. Wall Adapter Support with Priority over PSE
16. Radiated Emissions Measurement Results—EN55032 Class B
16.1 Radiated EMI Measurement Process
17. Conducted Emissions Measurement Results—EN55032
18. Thermal Measurements
19. Layout
20. Bill of Materials
21. Design and Layout Checklist

#### 1. Kit Description and Powering up the Si34061-EVB-EXT-12V

The Si34061-EVB-EXT-12V Flyback based evaluation board is a reference design for power supplies in Power over Ethernet (PoE+) Powered Device (PD) applications. The Si34061 device is described more completely in the data sheet and application notes.

The Si34061-EVB-EXT-12V board is shown on the cover page.

To achieve high efficiency, this board is set up with external Schottky diode bridges; however, a silicon type external diode bridge can be used as well. In that case, the CT/SP pins should be connected to the PSE (RJ45 - J1).

To compensate for the reverse leakage of Schottky type diode bridges at high temperatures, the recommended detection resistor should be adjusted to the values listed in the following table:

#### Table 1.1. Recommended Detection Resistor Values

External Diode Bridge	R <sub>DET</sub> (R21)
Silicon Type	24.3 kΩ
Schottky Type	24.9 kΩ

Ethernet data and power are applied to the board through the RJ45 connector (J1). The Ethernet data can be obtained from J2. The design can be used in Gigabit (10/100/1000) systems as well.

Power may be applied in the following ways:

- Using any IEEE 802.3-2015-compliant, PoE-capable PSE, or
- Using a laboratory power supply unit (PSU)

Powering the PD using a PSU:

• Connecting a dc source between blue/white-blue and brown/white-brown of the Ethernet cable (either polarity), (End-span) as shown below:

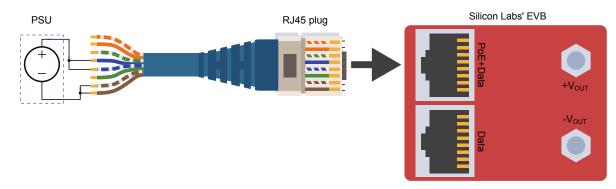
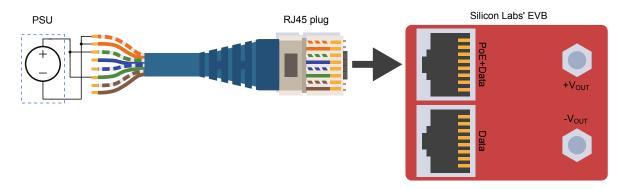
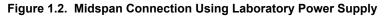


Figure 1.1. Endspan Connection Using Laboratory Power Supply

• Connecting a dc source between green/white-green and orange/white-orange of the Ethernet cable (either polarity), (Mid-span) as shown below:





#### 2. Si34061-EVB-EXT-12V Board Schematics

The following figure shows the input interface portion of the schematic:

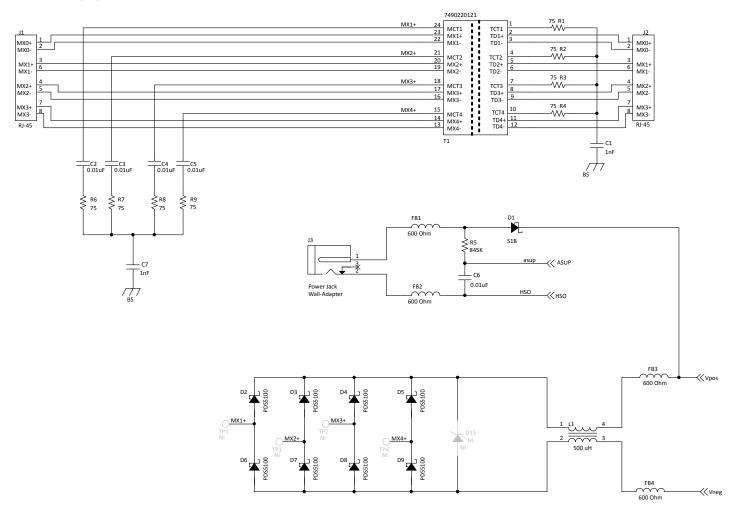


Figure 2.1. Si34061-EVB-EXT-12V Schematic: Input Interface

The Si34061 PD controller includes an integrated 100 V protection device that offers adequate protection for indoor applications and passes the IEC 61000-4-5 combination wave test (1.2/50  $\mu$ s open circuit voltage, 8/20  $\mu$ s short-circuit current) up to 4.4 kV common-mode and differentially to > 400 V.

In special installation classes where high differential and common-mode surge immunity are required, an external TVS protection device (e.g., SMDJ58A) may be installed between VNEG and VPOS to increase the surge immunity – D15.

With the external protection installed, common-mode surge immunity up to 6 kV and differential immunity up to 2 kV can be achieved.

The Si34061-EVB-EXT can also be powered from a wall adapter through connector J3. The following figure shows the dc-dc converter part of the schematic:

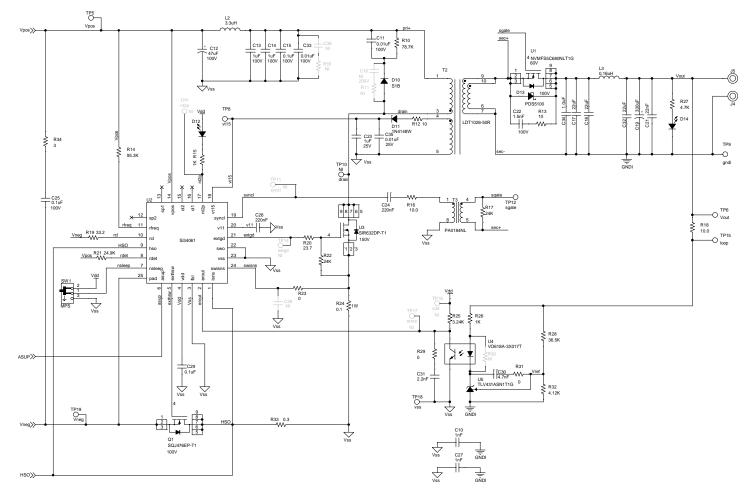


Figure 2.2. Si34061-EVB-EXT-12V Schematic: DC-DC Converter

#### 3. Conversion Efficiency of the Si34061-EVB-EXT-12V Board

The figures below show the conversion efficiency of the Si34061-EVB-EXT-12V board with 12 V output. The charts present:

- DC-DC converter efficiency at three different input voltages: 42.5, 50, and 57  $\mathsf{V}$
- End-to-end efficiency powered from a PSE at three different input voltages: 42.5, 50, and 57 V
- · End-to-end efficiency powered from a 48 V wall adapter

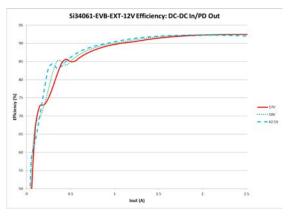


Figure 3.1. DC-DC Conversion Efficiency

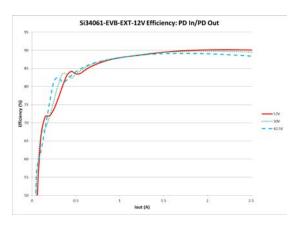


Figure 3.3. End-to-End Conversion Efficiency

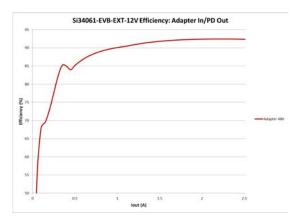


Figure 3.5. Conversion Efficiency Powered from 48 V Wall Adapter

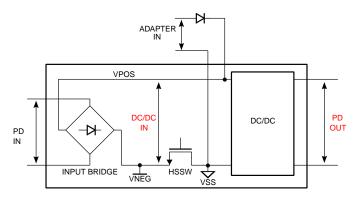


Figure 3.2. DC-DC Conversion Efficiency Measurement Setup

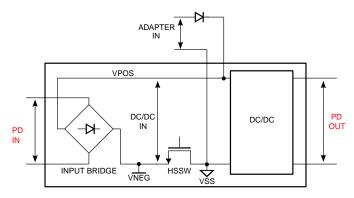


Figure 3.4. End-to-End Conversion Efficiency Measurement Setup

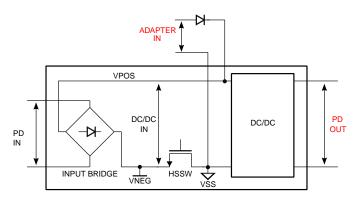


Figure 3.6. Wall Adapter Conversion Efficiency Measurement Setup

**Note:** During the efficiency measurements, D12 and D14 LEDs were removed since they are merely indicators and not required parts of the design.

#### 4. SIFOS PoE Compatibility Test Results

The PDA-300 Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at PoE Powered Devices (PDs). The following figure shows the passing SIFOS Test report of the Si34061-EVB-EXT-12V board.

						ive Version 3.2.6			-		PDA Interacti	ve version 5.2.0			- 0	
	Set	-up > 📃	i			Se	t-up >	i		_		Se	t-up > 💻	i		
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802.3at		Exit >			802.3	at	Exit>		an respect	_	802.3	at	Exit>		an mapan	_
PD Under Test	t Description		10000	ort Mode Cycle	PDUnde	r Test Description		0.025	oort Mode	Cycle	PDUeder	Test Description		1000	ort Mode	Cyc
SI34061-EVB-C4-12				ach Cycle 1	Si34061-EVB-				ach Cyde	1	\$134061-EVB4				ach Cycle	1
Alt.A. MDI Alt.	I.A. MDI-X	Alt-B, MDI	Alt-B, MDI-X	ccumulate	Alt-A, MDI	Alt-A, MDI-X	Alt-B, MDI	Alt-B, MDI-X	ccumulate		Alt-A, MDI	Alt-A, MDI-X	Alt-B, MDI	Alt-B, MDI-X	ccumulate	
	24.70k	24.75k	24.67k	Det. Resistance	8.96W	8.98W	8.99W	8.99W	Average	Power	1.90mA	1.90mA	1.90mA	1.90mA	Mark Cur	rrent
0.109uF	0.107uF	0.109uF	0.109uF	Det. Capacitance	9.05W	9.01W	9.04W	9.04W	Peak Po		9.10W	9.08W	9.09W	9.09W	Average	
40.7mA	40.7mA	40.7mA	40.7mA	Class Current	188.4mA	188.1mA	188.4mA	188.4mA	Max. Cu	rrent	9.16W	9.16W	9.14W	9.14W	Peak Pov	
4	4	4	4	Class Result	186.8mA	187.0mA	186.9mA	186.8mA	Min. Cu	rrent	0.25W	0.25W	0.23W	0.23W	Init Powe	HT
2	2	2	2	PD Type	187.1mA	187.2mA	187.3mA	187.3mA	Avg. Cu	rrent	169.3mA	170.0mA	169.5mA	169.7mA	Max. Cur	rent
37.4V	37.4V	37.5V	37.5V	Turn-On Voltage	20						167.7mA	167.6mA	167.7mA	167.7mA	Min. Curr	rent
32.5V	32.5V	32.5V	32.5V	Turn-Off Voltage							168.3mA	168.3mA	168.4mA	168.4mA	Avg. Cur	rent
0.100W-s	0.100W-s	0.100W-s	0.101W-s	Inrush Energy	On	e Classificat	tion Event	Result								
				Next Screen					Next		Tw	o Classifica	tion Event l	Result	Next Screen	

Figure 4.1. Si34061-EVB-EXT-12V PD SIFOS PoE Compatibility Test Results

#### 5. Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si34061 integrates a current-mode-controlled switching-mode power supply controller circuit; therefore, the application is a closed-loop system. To guarantee a stable power supply output voltage and reduce the influence of input supply voltage variations and load changes on the output voltage, the feedback loop must be stable.

To verify the stability of the loop, the loop gain and loop phase shift have been measured.

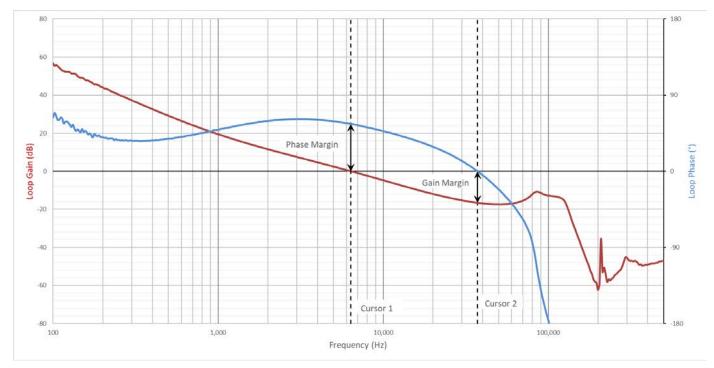


Figure 5.1. Si34061-EVB-EXT-12V Measured Loop-Gain and Phase-Shift Measured at Full Load

	Frequency	Gain	Phase
Phase Margin (Cursor 1)	6.4 kHz	0 dB	56°
Gain Margin (Cursor 2)	37 kHz	–16 dB	0 °

#### 6. Load Step Transient Measurement Results

The Si34061-ISO-FB EVB board's output has been tested with a step load function to verify the converter's output dynamic response.

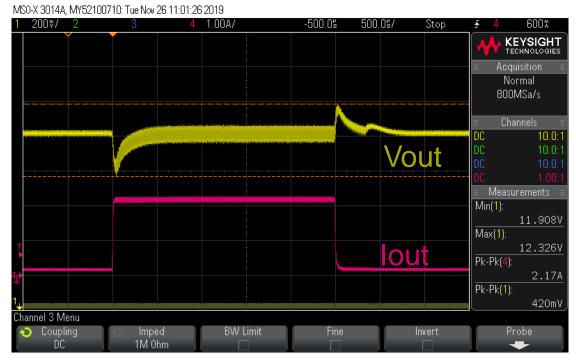


Figure 6.1. Si34061-EVB-EXT-12V Output Load Step Transient Test

Table 6.1. Output Load Step Transien	Table 6.1.	<b>Output Load Step</b>	Transient
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	From (Output Current)	To (Output Current)	V <sub>OUT</sub> Change
Load step	0.2 A	2.2 A	12 V – 210 mV
Load step	2.2 A	0.2 A	12 V + 210 mV

## 7. Output Voltage Ripple

The Si34061-EVB-EXT-12V board's output voltage ripple has been measured at no-load and full-load conditions. The following figures show the respective results.

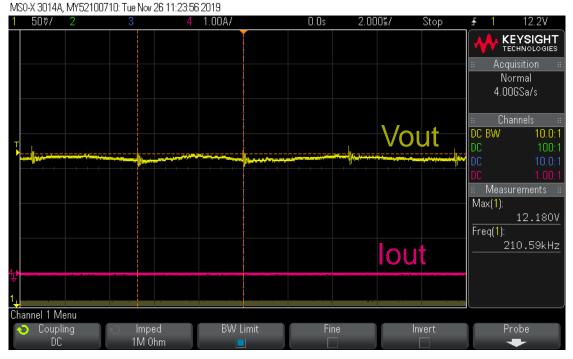


Figure 7.1. Si34061-EVB-EXT-12V Output Voltage Ripple at No-Load Condition: 25 mV

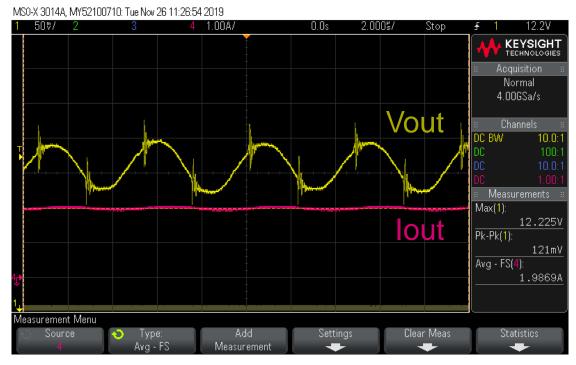


Figure 7.2. Si34061-EVB-EXT-12V Output Voltage Ripple at 2 A Output: 121 mV

#### 8. Soft Start Protection

The Si34061 has an integrated dynamic soft-start protection mechanism to avoid stressing the components with the sudden current or voltage changes associated with initial charging of the output capacitors.

The Si34061 intelligent adaptive soft-start mechanism does not require any external components to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal  $I_{PEAK}$  limit during soft-start, adjusting the output voltage ramp-up time as a function of the attached load.

The controller allows the output voltage to rise faster in a no-load (or light load) condition. With a heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

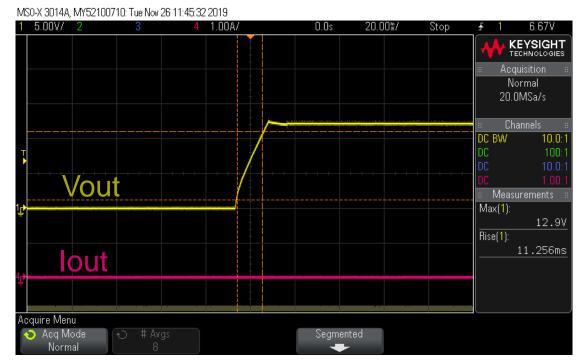


Figure 8.1. Si34061-EVB-EXT-12V Soft-Start with No Load

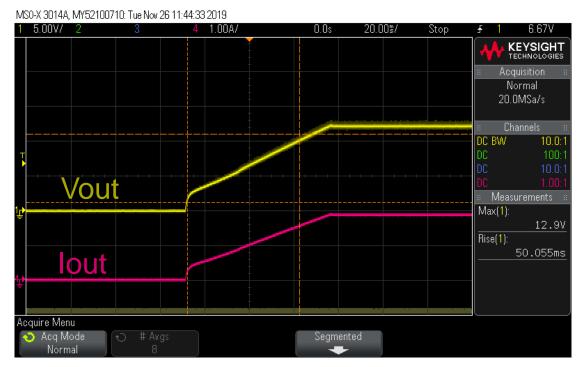


Figure 8.2. Si34061-EVB-EXT-12V Soft-Start with Heavy Load

#### 9. Output Short Protection

The Si34061 PD device has an integrated output short-protection mechanism that protects the IC itself and the surrounding external components from overheating in case of an electrical short on the output. This case is depicted in the figure below by showing the PD's input current and the PD's output voltage when the short is present.



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Figure 9.1. Si34061-EVB-EXT-12V Output Short Protection Mechanism

#### 10. Pulse Skipping at No-Load Condition

As the output load decreases, the controller starts to reduce the pulse width of the PWM signal (switcher ON time). At some point, even the minimum width pulse will provide higher energy than the application requires, which could result in loss of voltage regulation.

When the controller detects a light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or light-load skipping mode. This mode is shown in the figure below, which depicts the switching node of the primary FET (U3) at a no-load condition.

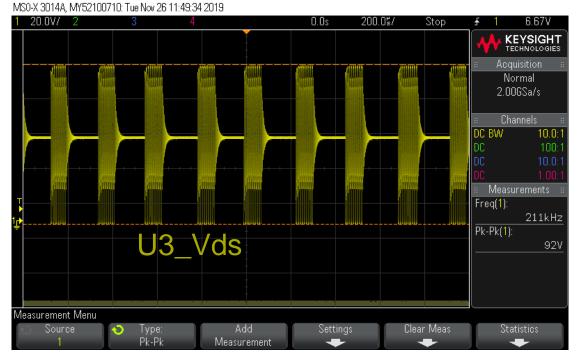


Figure 10.1. Pulse Skipping at No-load Condition

#### 11. Adjustable EVB Current Limit

For additional safety, the Si34061 has an adjustable EVB current limit feature.

The Si34061 controller measures the voltage on the  $R_{SENSE}$  (R33) through the ISNS pin. Attention must be paid when this voltage goes below VSS. When  $V_{RSENSE}$  reaches –270 mV (referenced to VSS), the current limiter restarts the circuit to protect the application.

The R<sub>SENSE</sub> value also defines the power level at which the external-HSSW (Q1) and synchronous-FET (U1) are enabled.

When the V<sub>RSENSE</sub> value is < –30 mV (referenced to VSS), the controller is in low-power mode:

- Q1 EXT-HSSW is disabled
- U1 Synchronous FET is disabled

When the  $V_{RSENSE}$  value is > -30 mV (referenced to VSS), the controller enters high-power mode:

- Q1 EXT-HSSW is enabled
- U1 Synchronous FET is enabled

When V<sub>RSENSE</sub> reaches –30 mV (referenced to VSS), the current EXTHSSW pin goes up, and the SYNCL pin starts to drive the synchronous FET.

The EVB current limit for Class 4 applications can be calculated with the following formula:

$$I_{LIMIT} = \frac{270mV}{R_{SENSE}} = -\frac{270mV}{0.3\Omega} = 0.9A$$

#### Equation 1.

With the selected R<sub>SENSE</sub> value, the external HSSW (Q1) and synchronous-FET (U1) are enabled at the input current calculated below:

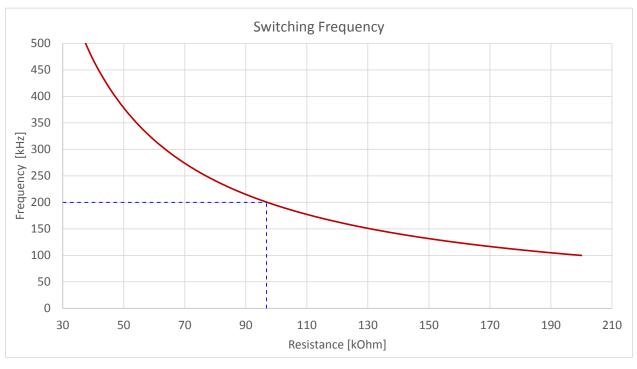
$$I_{power-mode} = \frac{30mV}{R_{SENSE}} = \frac{30mV}{0.3\Omega} = 0.1A$$

#### Equation 2.

Below the calculated value from Equation 2, the internal HSSW conducts, and rectification is accomplished through the D13 diode.

Above the value of Equation 2, the external HSSW conducts and synchronous rectification is accomplished by the U1 FET.

### **12. Tunable Switching Frequency**



The switching frequency of the oscillator is selected by choosing an external resistor, R14, connected between the RFREQ and VPOS pins. The following figure will aid in selecting the RFREQ value to achieve the desired switching frequency.

Figure 12.1. Switching Frequency vs. R<sub>FREQ</sub> Value

The selected switching frequency for Si34061-EVB-EXT-12V is 200 kHz, which is achieved by setting the R33 resistor to 95.3 kΩ.

## 13. Synchronous Rectification

The Si34061 device has a synchronous gate driver (SYNCL) to drive the synchronous-MOSFET.

At low-load (below Equation 1 value), the SYNCL driver is disabled, and the converter can work in discontinuous current mode (DCM). In this mode, the drain-source voltage waveform of U3 has a ringing waveform, which is typical for a DCM operation. The drain-source voltage waveform is depicted in the following figure:

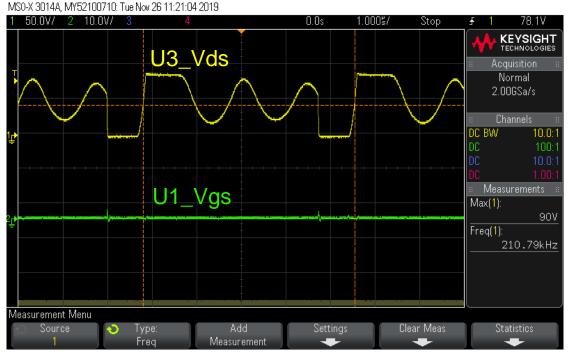


Figure 13.1. Discontinuous Current Mode at Low-Load Condition

At heavy load, the synchronous rectification driver is enabled, and the converter runs in continuous current mode (CCM) as shown in the following figure:

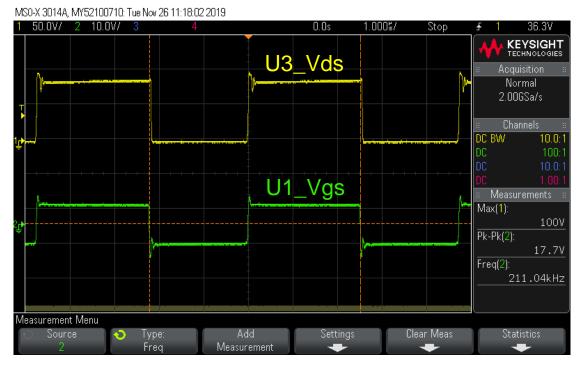


Figure 13.2. Continuous Current Mode at High-Load Condition

#### 14. Maintain Power Signature

The Si34061 device integrates an MPS circuit that ensures connection with the PSE if the PD application current drops below the PSE maintain-power-signature threshold level. When nSLEEP is low at startup, MPS generation depends on the total average current consumption. The controller detects the low consumption and, in order to keep the connection with the PSE, starts to generate the MPS pulses. This case is depicted in the following figure:

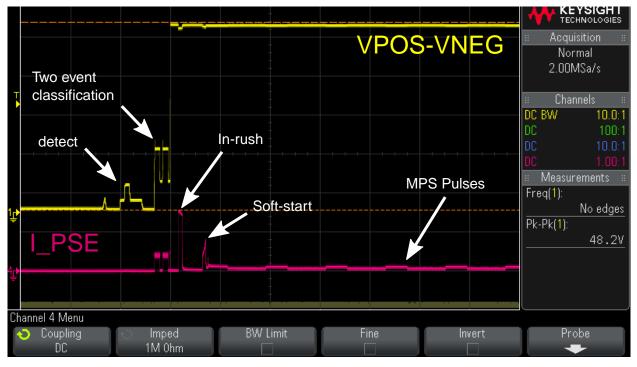


Figure 14.1. MPS Enabled: Connection is Kept with PSE

When nSLEEP is high at startup, MPS generation is disabled. Due to the low port current, the PSE will disconnect the port. In this mode (when nSLEEP is low at startup), MPS generation can be controlled (enabled/disabled) by the user by toggling nSLEEP between low and high.

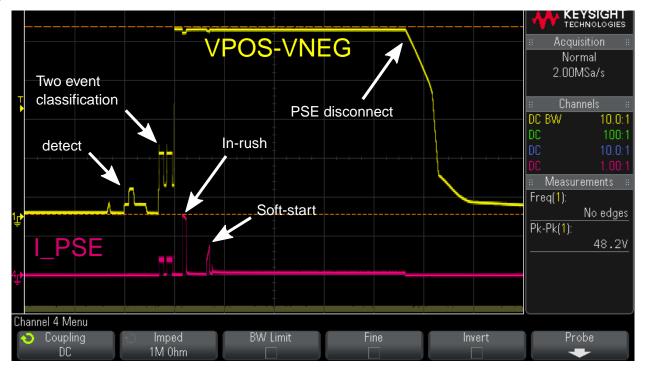


Figure 14.2. MPS Disabled: PSE Disconnects the Port

#### 15. Wall Adapter Support with Priority over PSE

The Si34061-EVB-EXT-12V board can be driven from a wall adapter instead of a PSE. The wall adapter has higher priority than the PSE.

The figure below shows a regular Type-2 startup sequence with the PSE; then, a wall adapter is plugged in. Through the ASUP digital input pin, the Si34061 automatically detects the presence of the wall adapter and starts drawing power from it.

During the transition from the PSE to the wall adapter, there is no interrupt on the output voltage (application).

In wall adapter mode, the Si34061 shows a non-valid detection signature toward the PSE. Therefore, until the wall adapter voltage is present, the PSE is unable to detect and turn ON the PD.

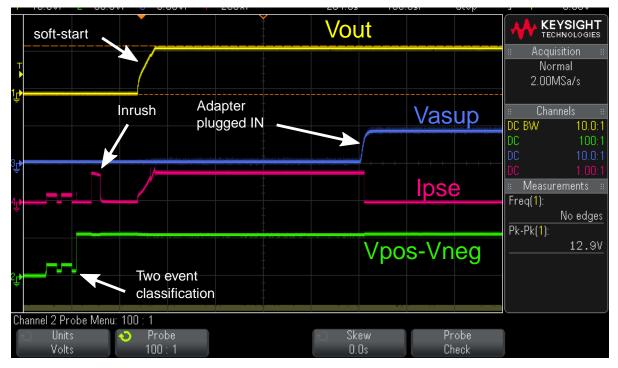


Figure 15.1. Wall Adapter Sequence Using ASUP Pin

#### 16. Radiated Emissions Measurement Results—EN55032 Class B

Radiated emissions of the Si34061-EVB-EXT-12V board have been measured with 50 V input voltage and a full load connected to the output (30 W).

As shown in the following figure, the Si34061-EVB-EXT-12V board is fully compliant with international EN 55032 Class B emissions standards:

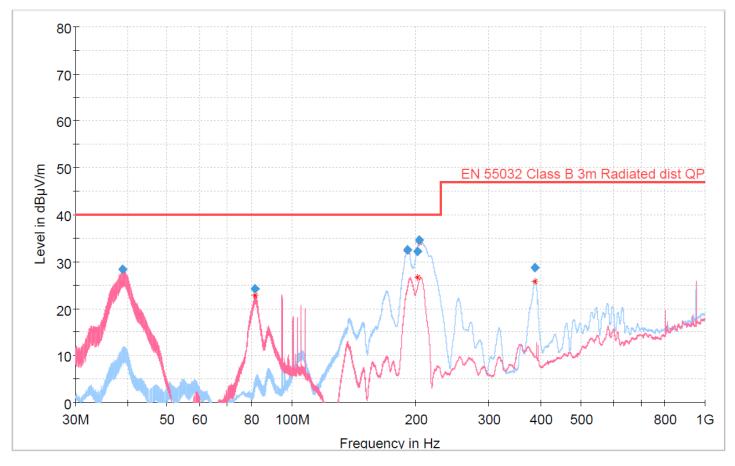


Figure 16.1. Si34061-EVB-EXT-12V Radiated Emissions Measurement Results with 50 V Input and 30 W Output Load

#### 16.1 Radiated EMI Measurement Process

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization).

Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

#### 17. Conducted Emissions Measurement Results—EN55032

The Si34061-EVB-EXT-12V board's conducted emissions have been measured with both peak and average detectors. The following figure shows the conducted EMI measurement setup.

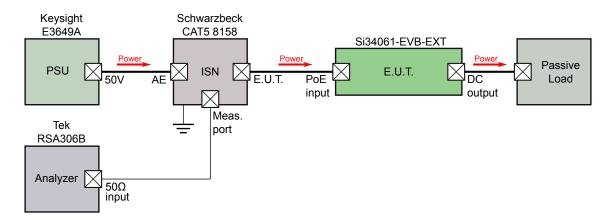


Figure 17.1. Conducted EMI Measurement Setup

The following figures show the measured results.

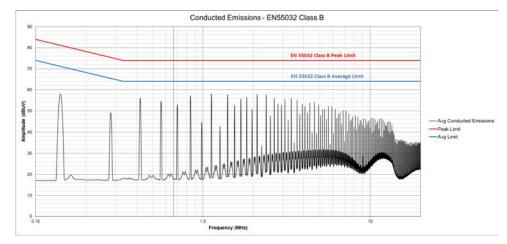


Figure 17.2. Si34061-EVB-EXT-12V Conducted Emissions Measurement Results with 50 V Input and 30 W Output Load

#### **18. Thermal Measurements**

The Si34061-EVB-EXT-12V board's top and bottom side thermal images at full load are shown in the following figures.

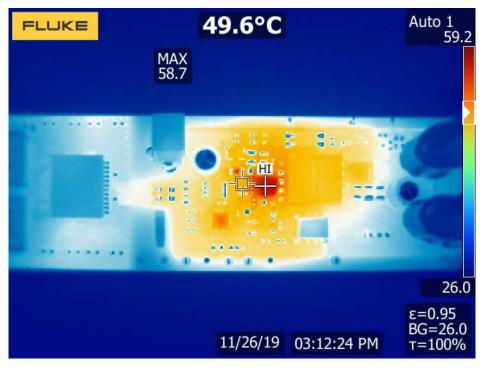


Figure 18.1. Si34061-EVB-EXT-12V Thermal Image at Full Load—Top Side

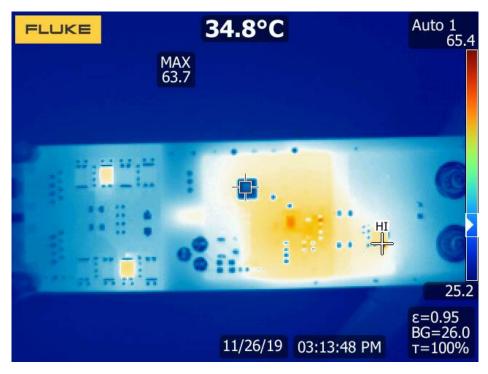


Figure 18.2. Si34061-EVB-EXT-12V Thermal Image at Full Load—Bottom Side

Note: Ambient temperature was 26 °C.

## 19. Layout

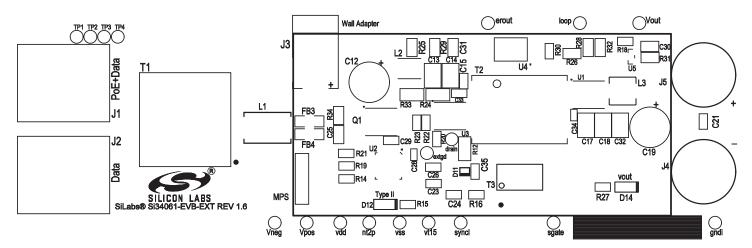


Figure 19.1. Primary Silkscreen

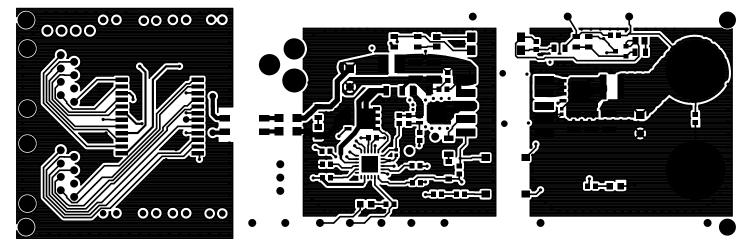


Figure 19.2. Top Layer

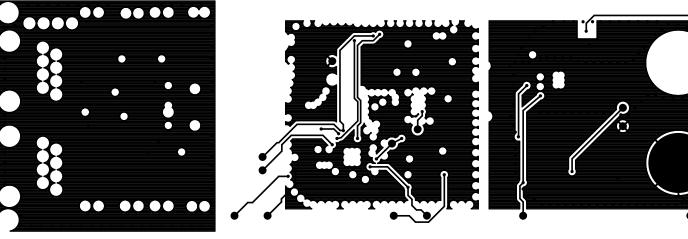
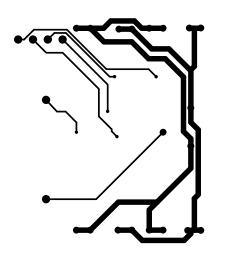


Figure 19.3. Internal 1 Layer



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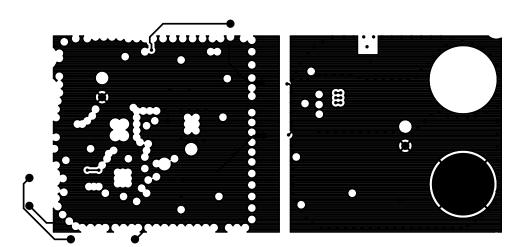


Figure 19.4. Internal 2 Layer

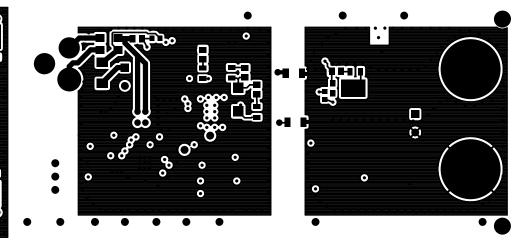
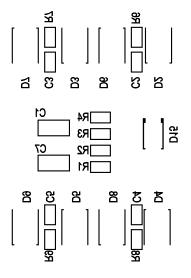
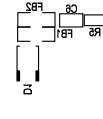


Figure 19.5. Bottom Layer





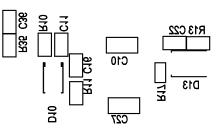


Figure 19.6. Bottom Silkscreen

## 20. Bill of Materials

Reference Designator	Quantity	Description	Manufacturer	Manufacturer PN
C1, C7, C10, C27	4	CAP, 1 nF, 2000 V, ±5%, X7R, 1206	Kemet	C1206C102JGRACTU
C2, C3, C4, C5, C33	5	CAP, 0.01 μF, 100 V, ±10%, X7R, 0603	Venkel	C0603X7R101-103K
C6, C11	2	CAP, 0.01 µF, 100 V, ±10%, X7R, 0805	Venkel	C0805X7R101-103K
C12	1	CAP, 47 µF, 100 V, ±20%, AL, RAD	Panasonic	ECA2AM470
C13, C14	2	CAP, 1 µF, 100 V, ±10%, X7R, 1210	Venkel	C1210X7R101-105K
C15	1	CAP, 0.1 µF, 100 V, ±10%, X7R, 0603	Venkel	C0603X7R101-104K
C16	1	CAP, 100 pF, 200 V, ±5%, NP0 HIGH Q, 0805	Venkel	C0805HQN201-101J
C17, C18, C32	3	CAP, 22 µF, 16 V, ±20%, X5R, 1206	KEMET	C1206C226M4PAC7800
C19	1	CAP, 330 µF, 16 V, ±20%, AL, 8X11.5MM, PTH	Panasonic	ECA-1CM331
C21	1	CAP, 22 nF, 16 V, ±20%, X7R, 0603	Venkel	C0603X7R160-223M
C22	1	CAP, 1.5 nF, 100 V, ±10%, X7R, 0805	Venkel	C0805X7R101-152K
C23	1	CAP, 1 μF, 25 V, ±10%, X5R, 0603	Venkel	C0603X5R250-105K
C24, C26	2	CAP, 220 nF, 16 V, ±5%, X7R, 0603	Kemet	C0603C224J4RACTU
C25	1	CAP, 0.1 µF, 100 V, ±10%, X7R, 0805	Venkel	C0805X7R101-104K
C29	1	CAP, 0.1 µF, 10 V, ±10%, X7R, 0603	Venkel	C0603X7R100-104K
C30	1	CAP, 4.7 nF, 25 V, ±2%, C0G, 0805	Venkel	C0805C0G250-472G
C31	1	CAP, 2.2nF, 16V, ±2%, C0G, 0805	Venkel	C0805C0G160-222G
C34	1	CAP, 1.0 µF, 16 V, ±10%, X5R, 0402	Venkel	C0402X5R160-105KN
C35	1	CAP, 0.01 µF, 25 V, ±10%, X8R, 0603	KEMET	C0603C103K3HACAUTO
D1	1	DIO, SINGLE, 100 V, 1.0 A, SMA	Fairchild	S1B
D2, D3, D4, D5, D6, D7, D8, D9, 13	9	DIO, SCHOTTKY, 100 V, 5 A, PowerDI-5 Diodes		PDS5100H-13
D10	1	DIO, SINGLE, 100 V, 1.0 A, SMA	Fairchild	RS1B
D11	1	DIO, fAST, 100 V, 2 A, SOD123	Diodes Inc	1N4148W
D12, D14	2	LED, GREEN, 0805	LITE_ON INC	LTST-C170GKT
FB1, FB2, FB3, FB4	4	FERRITE BEAD, 600 Ω @100 MHz, 1206	MuRata	BLM31PG601SN1
J1, J2	2	CONN, RJ-45, 1 Port, Tab Down, 0.050" Pitch, PTH	MOLEX	95001-2881
J3	1	CONN, POWER JACK, RA, 2.1 mm, PTH	Adam Tech	ADC-002-1
J4, J5	2	CONN, BANANA JACK, Threaded unin- sulated	ABBATRON HH SMITH	101
LB1	1	LABEL, PDB, POLYIMIDE, WHITE, 1.00 in. X 0.187 in., FONT 2	Silabs	LABEL-Si34061-EVB-EXT- BOM-R1.7-12V
L1	1	CM Choke, 500 $\mu H,$ 1 A, 1 k $\Omega,$ SMT	Bourns	SRF0905-501Y

#### UG412: Class 4, 30 W, 12 V EMI-Compliant, Isolated EVB for the Si34061 Bill of Materials

Reference Designator	Quantity	Description	Manufacturer	Manufacturer PN
L2	1	INDUCTOR, POWER, 3.3 µH, ±20%, 1.5 A, Unshielded	Murata	84332C
L3	1	INDUCTOR, POWER, Shielded, 0.16 µH, 31 A, SMD	Coilcraft	XAL5030-161ME
MH1, MH2, MH3, MH4	4	HDW, SCREW, 4-40 x 1/4 in. Pan Head, Slotted, Nylon Co		NSS-4-4-01
PCB1	1	PCB, BARE BOARD, Si34061-EVB-EXT REV 1.6	SiLabs	Si34061-EVB-EXT REV 1.6
Q1	1	TRANSISTOR, MOSFET, N-CHNL, 100 V, 23 A, POWERPAK-SO-8	Vishay	SQJ476EP-T1_GE3
R1, R2, R3, R4, R6, R7, R8, R9	8	RES, 75 Ω, 1/16 W, ±0.5%, ThinFilm, 0603	Susumu	RR0816Q-750-D
R5	1	RES, 845 kΩ, 1/10 W, ±1%, ThickFilm, 0603	Panasonic	ERJ-3EKF8453V
R10	1	RES, 78.7 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Yageo	RC0805FR-0778K7L
R11	1	RES, 100 Ω, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-1000F
R12	1	RES, 10 $\Omega,$ 1/4 W, ±1%, ThickFilm, 1206	Venkel	CR1206-4W-10R0F
R13	1	RES, 10 Ω, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-10R0F
R14	1	RES, 95.3 kΩ, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-9532F
R15	1	RES, 1 kΩ, 1/10 W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-1001F
R16, R18	2	RES, 10.0 Ω, 1/16 W, ±1%, ThickFilm, Ven		CR0603-16W-10R0F
R17, R22	2	RES, 24 kΩ, 1/10 W, ±1%, ThickFilm, 0603	Panasonic	ERJ-3EKF2402V
R19	1	RES, 33.2 Ω, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-33R2F
R20	1	RES, 23.7 Ω, 1/16 W, ±1%, ThickFilm, 0603	Venkel	CR0603-16W-23R7F
R21	1	RES, 24.9K, 1/10W, ±1%, ThickFilm, 0603	Venkel	CR0603-10W-2492F
R23	1	RES, 0 Ω, 1 A, ThickFilm, 0603	Panasonic	ERJ-3GEY0R00V
R24	1	RES, 0.1 Ω, 1 W, ±1%, ThickFilm, 1206	Panasonic	ERJ-8BWFR100V
R25	1	RES, 3.24 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Vishay	CRCW08053K24FKEA
R26	1	RES, 1 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-1001F
R27	1	RES, 4.7 kΩ, 1/10 W, ±5%, ThickFilm, 0603	Venkel	CR0603-10W-472J
R28	1	RES, 36.5 kΩ, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-3652F
R29, R31	2	RES, 0 Ω, 2 A, ThickFilm, 0805	Venkel	CR0805-10W-000

Reference Designator	Quantity	Description		Manufacturer	Manufacturer PN
R32	1	RES, 4.12K, 1/10 W, ±1%, <sup>-</sup> 0805	ThickFilm,	Venkel	CR0805-10W-4121F
R33	1	RES, 0.3 Ω, 1/2 W, ±1%, Thic	kFilm, 1206	Venkel	LCR1206-R300F
R34	1	RES, 3 Ω, 1/8 W, ±1%, Thick	Film, 0805	Venkel	CR0805-8W-3R00FT
SO1, SO2, SO3, SO4	4	HDW, STANDOFF, 4-40 x 1	/2" , Nylon	SPC Technolo- gy	2397
SW1	1	SWITCH, SPDT, SLIDE, OI PITCH, 12V, PTH	•	Apem Inc.	NK236H
TP1, TP2, TP3, TP4	4	TESTPOINT, BLACK,	PTH	Kobiconn	151-203-RC
TP5, TP6	2	TESTPOINT, RED, 0.050 in. I	LOOP, PTH	Keystone	5000
TP8, TP9, TP10, TP11, TP12, TP14, TP15, TP16, TP17, TP18, TP19	11	TESTPOINT, BLACK, 0.050"	LOOP, PTH	Keystone	5001
T1	1	Module, PoE+/PoE++ Magnet XFMR 1CT:1CT TX 1CT:1CT		Wurth	7490220121
T2	1	TRANSFORMER, Flyback, 3 SMD	0 W, 12 V,	LinkCom	LDT1026-50R
ТЗ	1	Gate XFMR, 1:1, 1500 Vrms 27.2 Vµsec	, 1200 μH,	Pulse Engi- neering	PA0184NL
U1	1	TRANSISTOR, MOSFET, N-C 21 A, POWERPAK-S		ON Semi	NVMFS5C680NLT1G
U2	1	IC, IEEE 802.3-Compliant PC terface, QFN24	DE+ PD In-	SiLabs	Si34061
U3	1	TRANSISTOR, MOSFET, N- V, 29 A, POWERPAK-		Vishay	SIR632DP-T1-RE3
U4	1	PHOTOCOUPLER, 5300 Vrm 4-PIN SMD	ns Isolation,	Vishay	VO618A-3X017T
U5	1	IC, ADJ PREC SHUNT REG Voltage-Output 1.24 ~		ON Semi	TLV431ASN1T1G
Not Installed Components					
C28	1	CAP, 470 pF, 25 V, ±20%, X7R, 0402	• • • • •		C0402X7R250-471M
C36	1	CAP, 0.01 μF, 100 V, ±10%, X7R, 0805		enkel	C0805X7R101-103K
D15	1			telfuse	SMAJ58A
R30	1	RES, 1 kΩ, 1/10 W, ±1%, Vo ThickFilm, 0603		enkel	CR0603-10W-1001F
R35	1	RES, 100 Ω, 1/10 W, ±1%, ThickFilm, 0805	V	enkel	CR0805-10W-1000F
TP7	4	TESTPOINT, BLACK, 0.050" LOOP, PTH	Ke	ystone	5001

### 21. Design and Layout Checklist

The complete EVB design databases are located at www.silabs.com/PoE link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

The following is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si34061 data sheet and AN1130: Si3404/06x PoE-PD ControllerDesign Guide when using the following checklist.

1. Design Planning checklist:

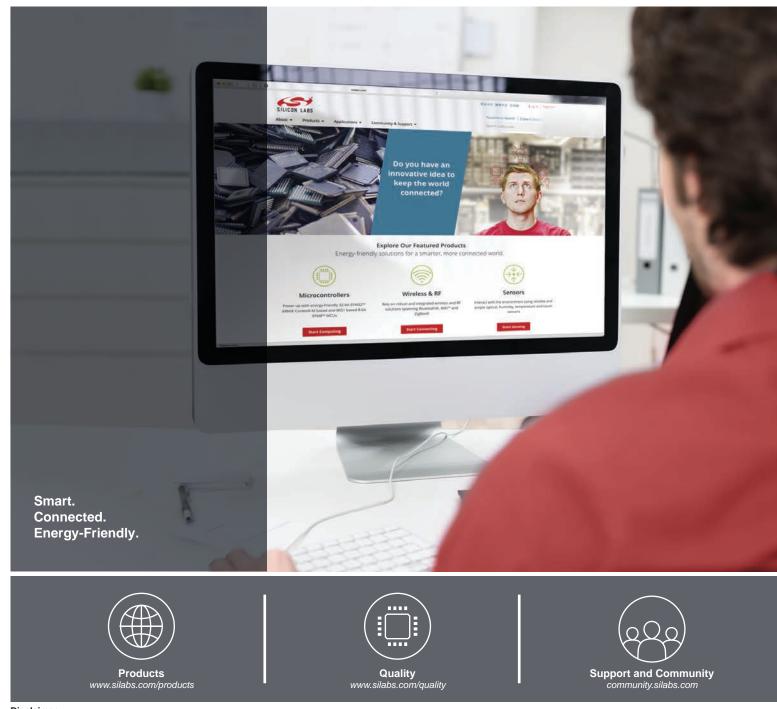
- a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
- b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si34061-EVB-EXT into your system design process.
- c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions).

d. Based on your required PD power level, select the appropriate class resistor RCLASS value by referring to AN1130.

2. General Design Checklist:

- a. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a 3Ω resistors in place of R34.
- 3. Layout Guidelines:
  - a. Make sure VNEG pin of the Si34061 is connected to the backside of the QFN package with an **adequate thermal plane**, as noted in the data sheet and AN1130.
  - b. Keep the trace length from the switching FET to VSS as short as possible. Make all the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
  - c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
  - d. Keep the circular area of the loop from the switching FET to the transformer and returning from the input filter capacitors (C13, C14, C15) to VSS as small a diameter as possible. Also, minimize the circular area of the loop from the output of the transformer to the syncFET (U1) and returning through the output filter capacitor back to the transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.
  - e. Keep the high-power traces as short as possible.
  - f. Keep the feedback and loop stability components as far from the transformer and noisy power traces as possible.
  - g. If the output has a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.



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