UG394: Isolated Dual Output Evaluation Board for the Si34062

The Si34062 isolated Flyback topology evaluation board is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application.

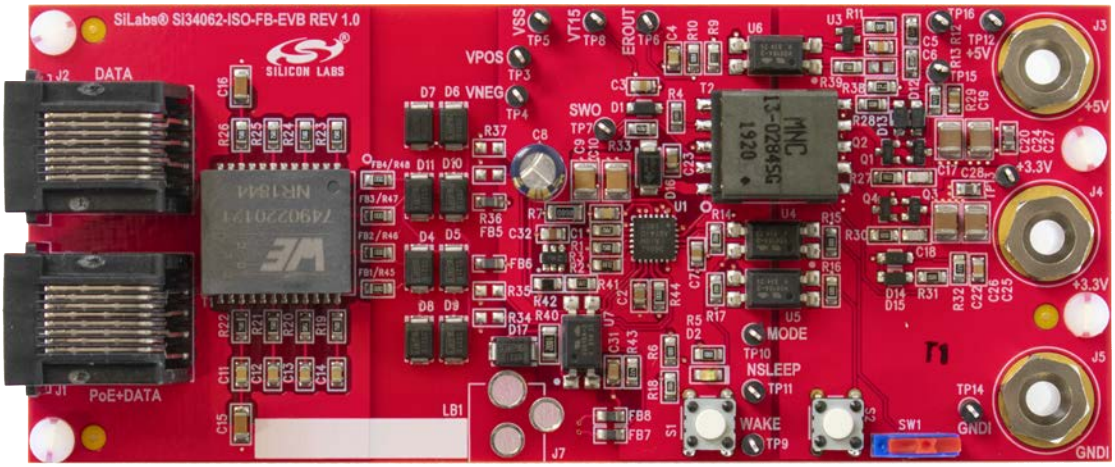
This Si34062-ISO-FB-EVB board maximum output level is 7.5W.

The Si34062-ISO-FB-EVB provides two isolated outputs: 5V/0.6A and 3.3V/1.4A

The Si34062-ISO-FB-EVB board is shown below. The Si34062 IC integrates an IEEE 802.03at compatible PoE interface as well as a current-control based dc/dc converter.

KEY FEATURES

- IEEE 802.03at Compliant
- High Efficiency
- High Integration
- EMI Compliant Design
- Optional MPS Function
- High Flexibility
- Integrated Transient Overvoltage Protection
- Thermal Shutdown Protection
- 5 x 5 mm 24-pin QFN



Parameter	Condition	Specifications
PSE input voltage range	Connector J1	37 V to 57 V
Wall adapter input voltage range	Connector J7	40 V to 57 V
PoE Type/Class	IEEE 802.3af	Type 1/Class 2
Output voltage/current	Connectors J4-J5	3.3 V / 1.4 A
Output voltage/current	Connectors J3-J5	5 V / 0.6 A
Efficiency, end-to-end	V_{IN} = 50 V, 3.3 V output	85.1 %
Efficiency, end-to-end	V_{IN} = 50 V, 5 V output	86.2 %

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1. Schematics

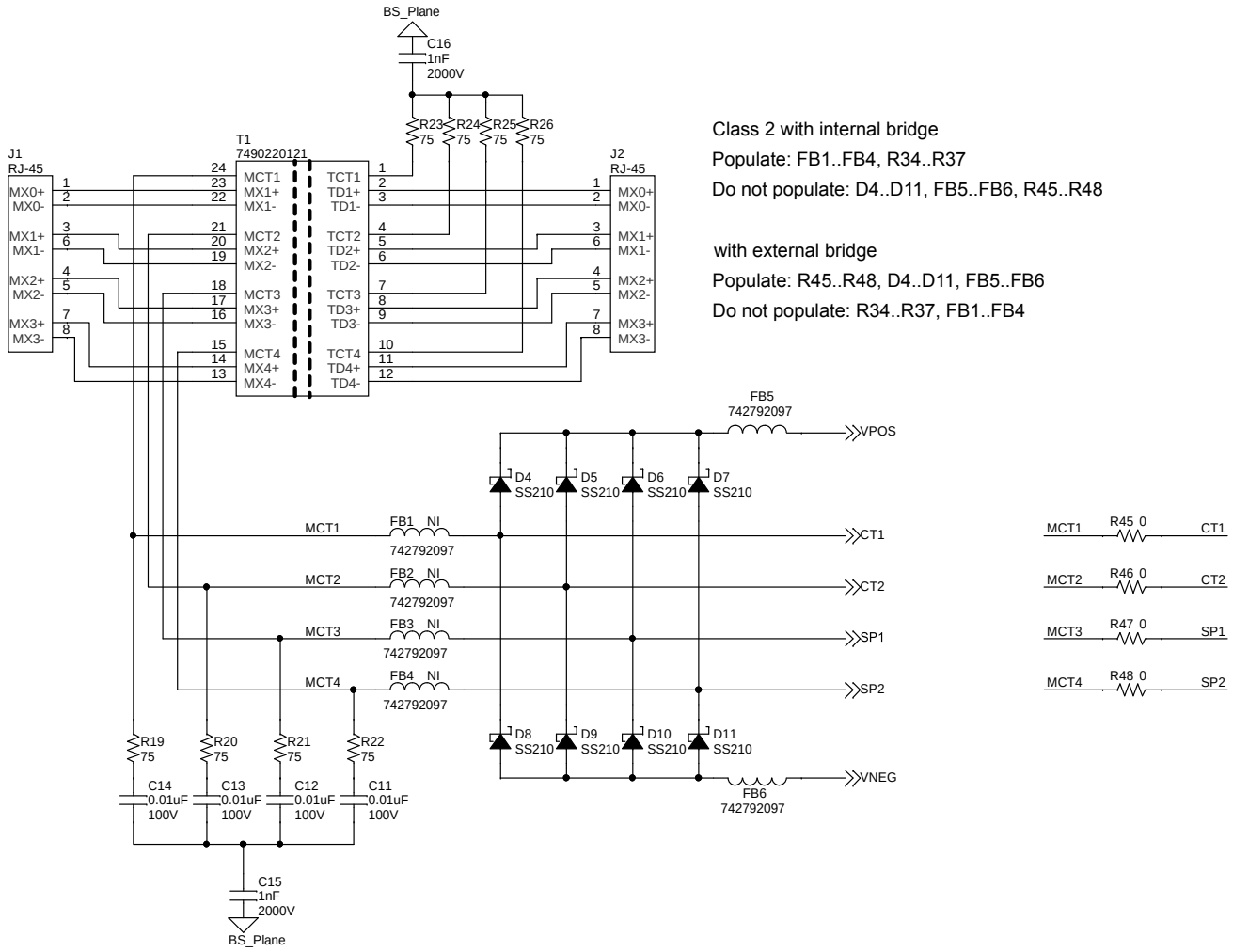


Figure 1.1. Si34062-ISO-FB-EVB Schematic: Input Interface

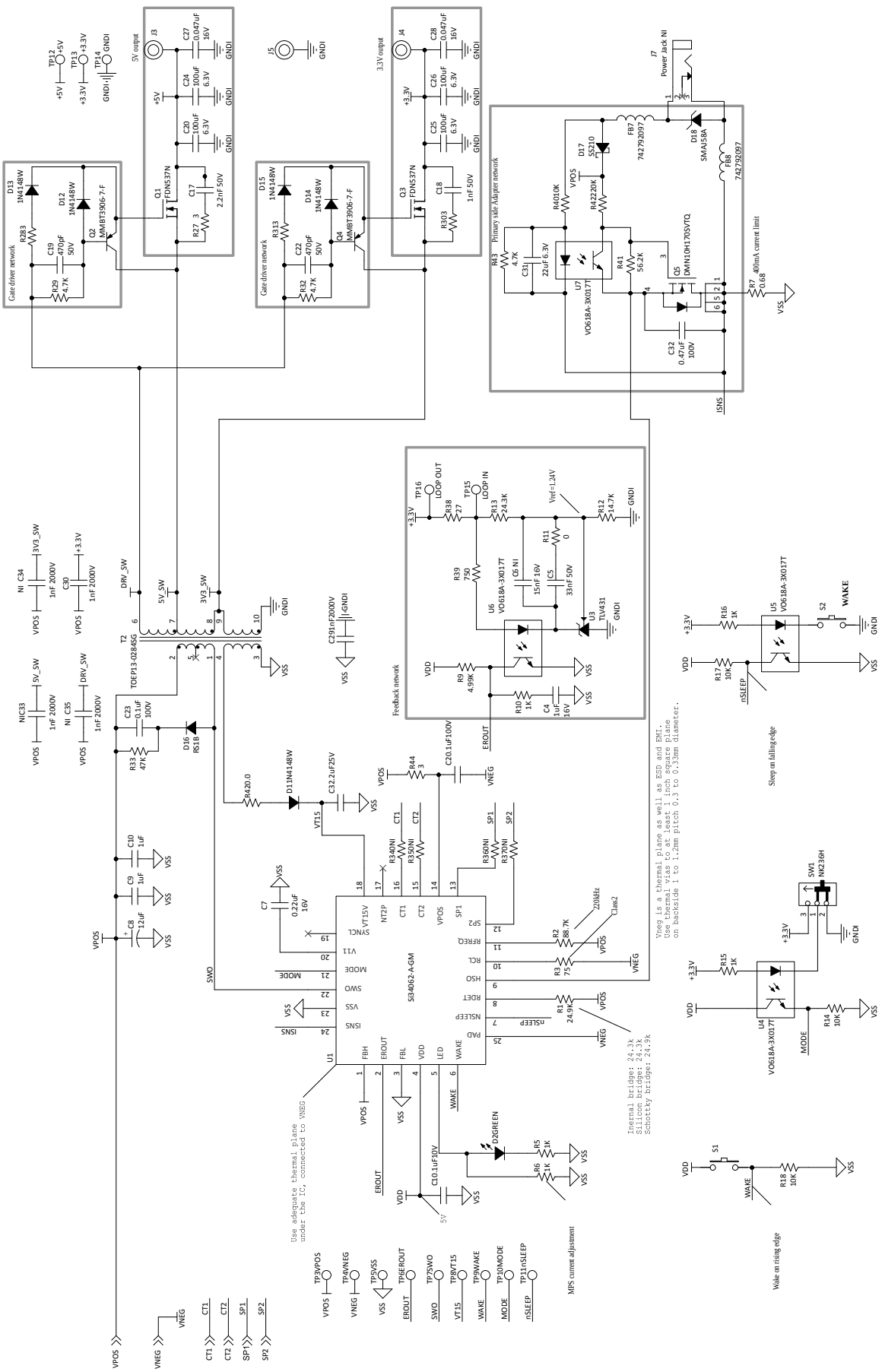


Figure 1.2. Si34062-ISO-FB-EVB Schematic: DC-DC Converter

2. Kit Description and Powering up the Si34062-ISO-FB-EVB Board

The Si34062-ISO-FB-EVB Flyback evaluation board is a 7.5 W output power Powered Device reference design for Power over Ethernet (PoE) applications.

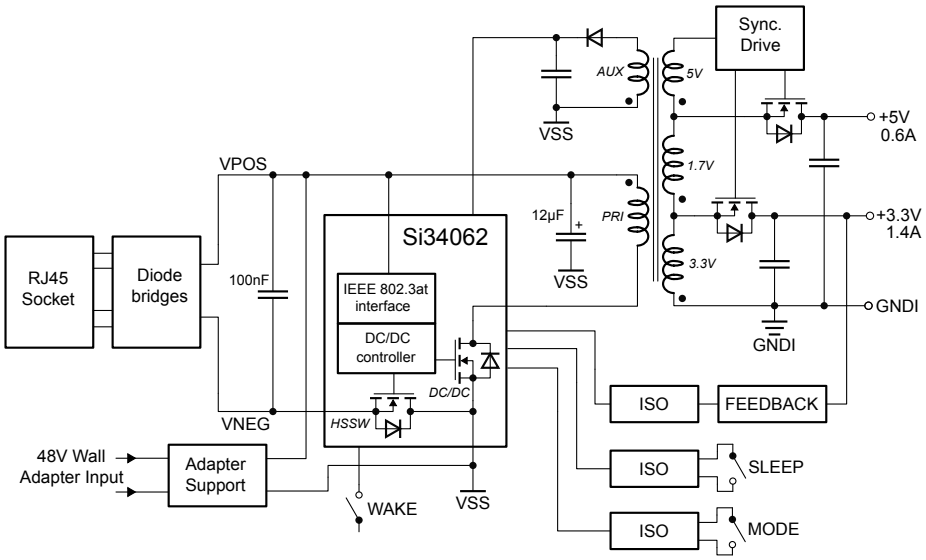


Figure 2.1. Simplified Block Diagram of the Si34062-ISO-FB-EVB

The Si34062 IC includes integrated diode bridge for both CT and SP connection, therefore the Si34062-ISO-FB-EVB can be configured to be powered through internal or external diode bridges. The integrated diode bridge can handle up to 200 mA input current. Above 200 mA input current, the external diode bridge is required. To get higher power conversion efficiency external schottky diode bridge is recommended. The shipped boards are set up in external schottky diode bridge configuration, the internal diode bridge is not connected (CT/SP pins are floating, R34..R37 are not installed). To compensate the reverse leakage of the schottky type diode bridges at high temperature, the recommended R1 detection resistor should be adjusted to the values listed in the following table.

Table 2.1. Recommended Detection Resistor Values

Diode Bridge Configuration	D4..D11	FB1..FB4	FB5..FB6	R34..R37	R1
Internal	Do not populate	Populate	0 Ω jumper	0 Ω jumper	24.3 kΩ
External Schottky	Schottky diodes	0 Ω jumper	Populate	Do not populate	24.9 kΩ
External silicon	Silicon diodes	Populate	0 Ω jumper	0 Ω jumper	24.3 kΩ

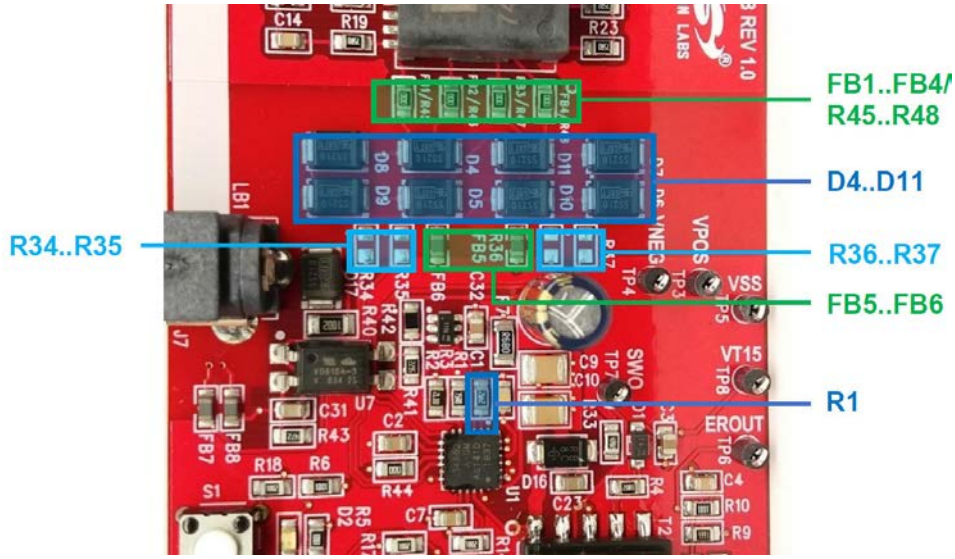


Figure 2.2. Components of Diode Bridge Configuration

Ethernet data and power are applied to the board through the RJ45 connector – J1(PoE+DATA). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet transformer secondary-side data is accessible at the other RJ45 connector – J2 (DATA).

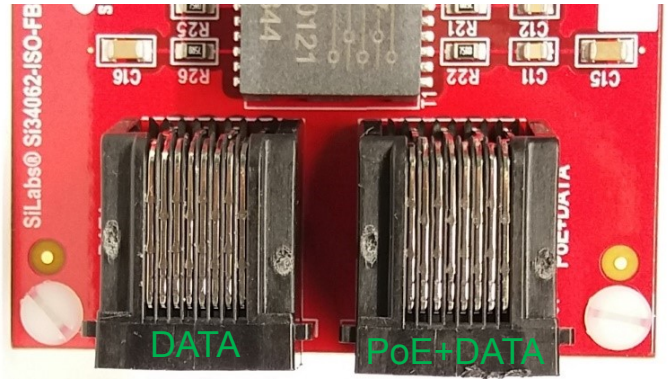


Figure 2.3. Input Connectors

There are two dc outputs, +5 V (J3) and +3.3 V (J4), both referenced to GNDI (J5). The maximum output power is 7.5 W; the 3.3 V output can be loaded up to 1.4 A, and the 5 V output can be loaded up to 0.6 A.

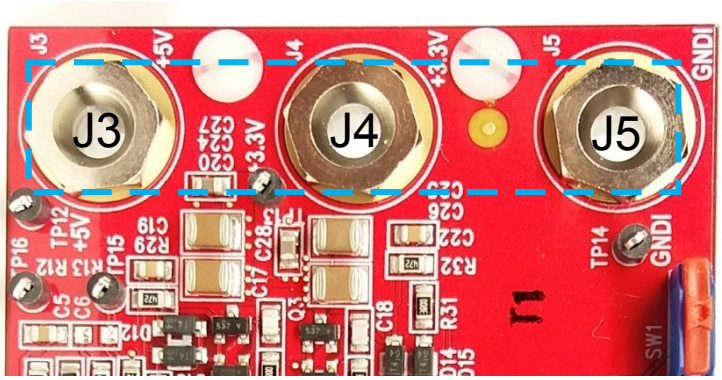


Figure 2.4. Output Connectors

The design can be used in Gigabit(10/100/1000) systems as well.

Power may be applied in the following ways:

- Using an IEEE 802.3-2015-compliant, PoE-capable PSE, or
- Using a laboratory power supply unit (PSU):
  - Connecting a dc source between blue/white-blue and brown/white-brown of the Ethernet cable (either polarity), (Endspan) as shown below:

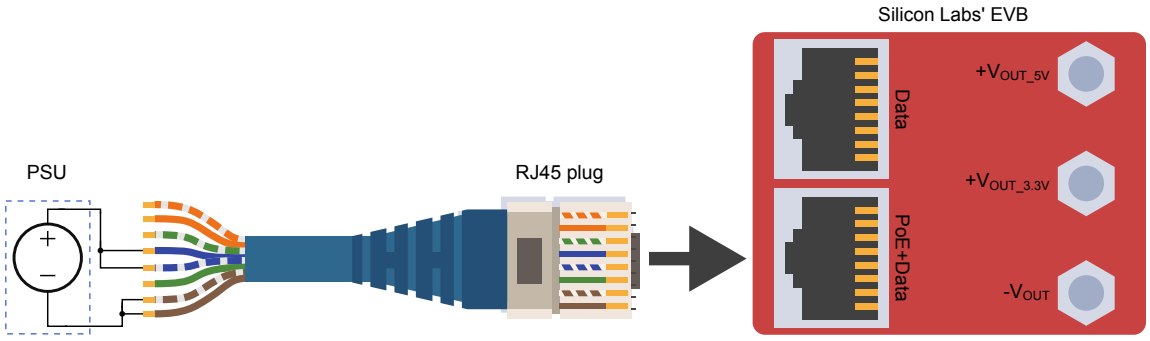


Figure 2.5. Endspan Connection Using Laboratory Power Supply

  - Connecting a dc source between green/white-green and orange/white-orange of the Ethernet cable (either polarity), (Midspan) as shown below

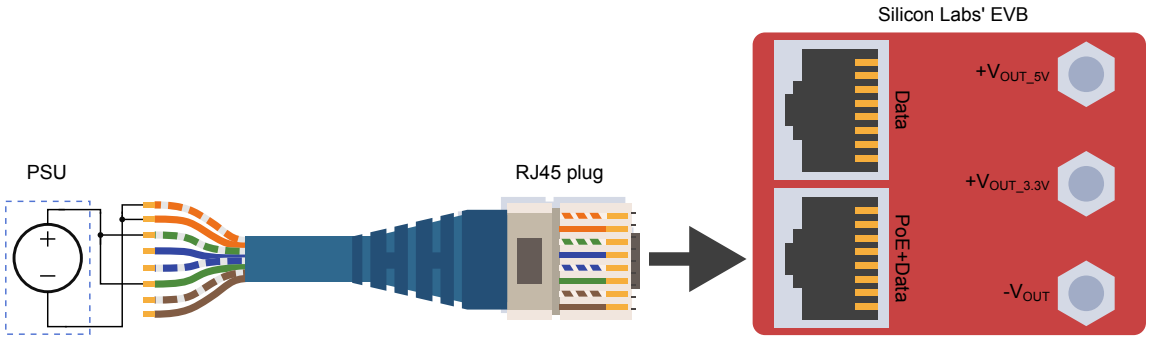


Figure 2.6. Midspan Connection Using Laboratory Power Supply

3. Conversion Efficiency of the Si34062-ISO-FB Board

The end-to-end efficiency measurement data of the Si34062-ISO-FB-EVB are shown below. Efficiency was measured from PoE (RJ45 connector) input to each output. The input voltage is 50 V. Onboard LEDs are disabled for the duration of the test.

The chart represents six separate measurements, each output measured with three different input bridge configurations:

- External Schottky
- External silicon and
- Internal bridge

During 3.3 V output measurement, the 5 V output was not loaded, and vice versa.

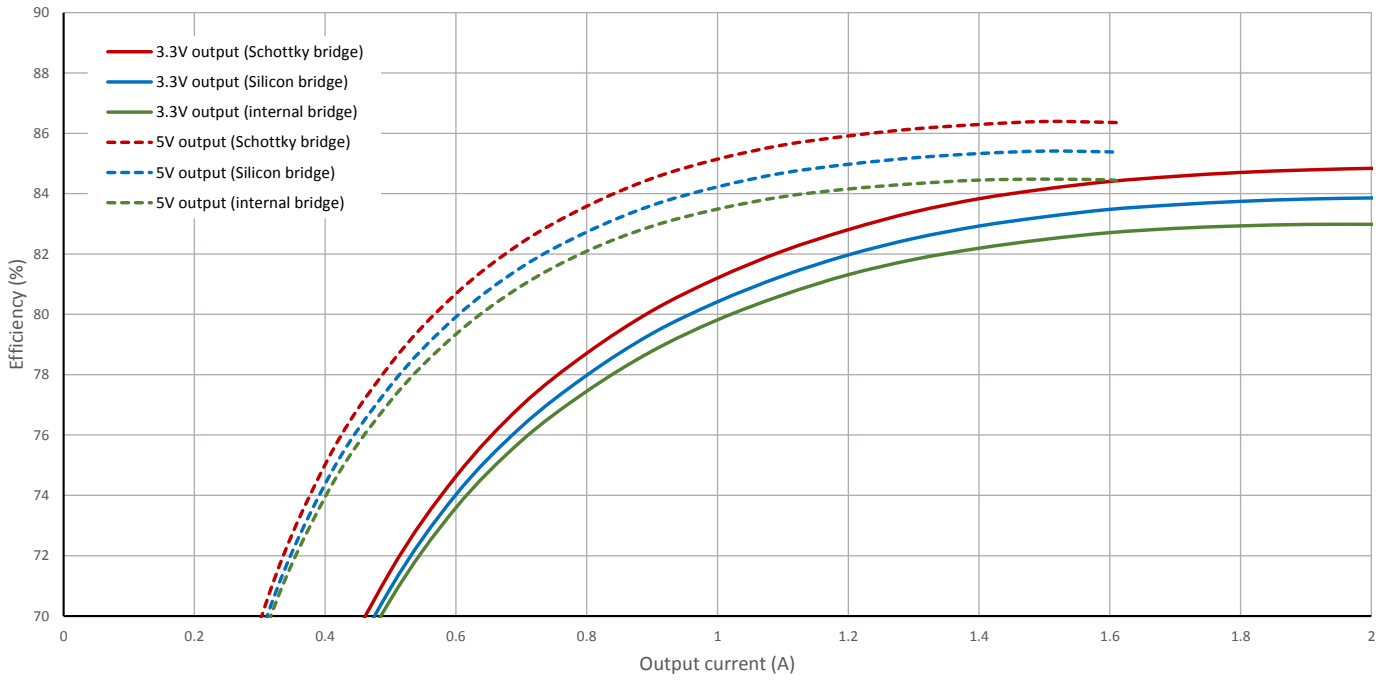


Figure 3.1. Si34062-ISO-FB-EVB End-to-End Efficiency Chart with Different Input Bridges

4. SIFOS PoE Compatibility Test Results

The PDA-300 Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at PoE Powered Devices (PDs).

The Si34062-ISO-FB-EVB board has been successfully tested with PDA-300 Powered Device Analyzer from SIFOS Technologies.

The following figure shows the passing SIFOS test result of the Si34062-ISO-FB-EVB board.

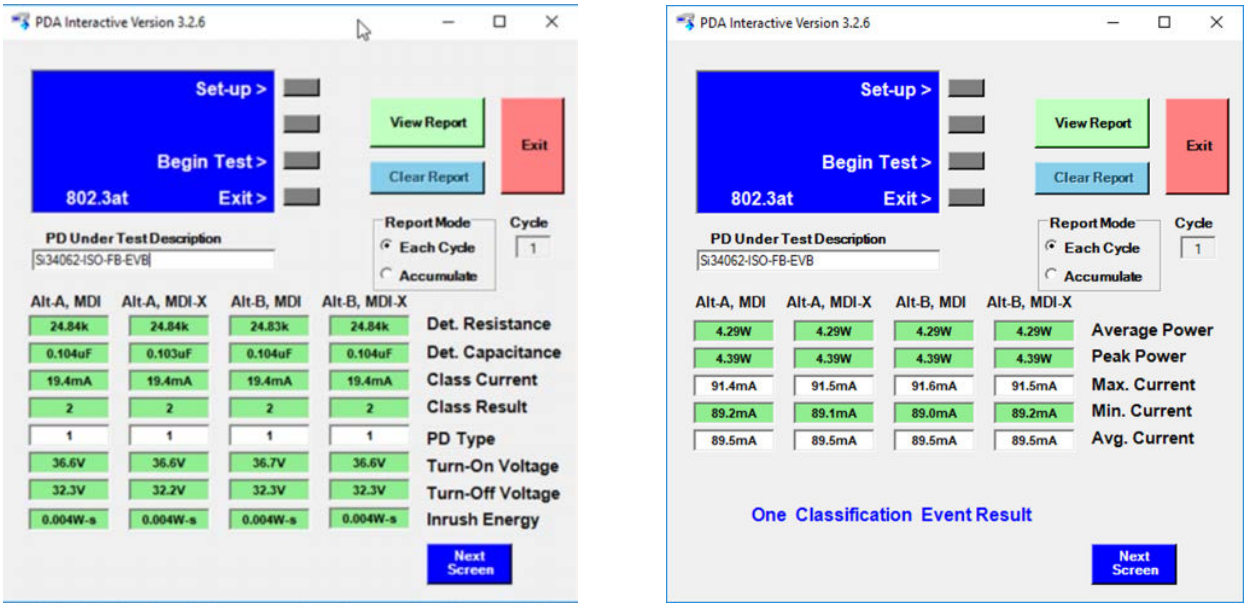


Figure 4.1. Si34062-ISO-FB-EVB PD SIFOS PoE Compatibility Test Results

5. Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si34062 device integrates a current mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee a stable output voltage of a power supply and to reduce the influence of input supply voltage variations and load changes on the output voltage, the feedback loop should be stable. To verify the stability of the loop, the loop gain and loop phase has been measured.

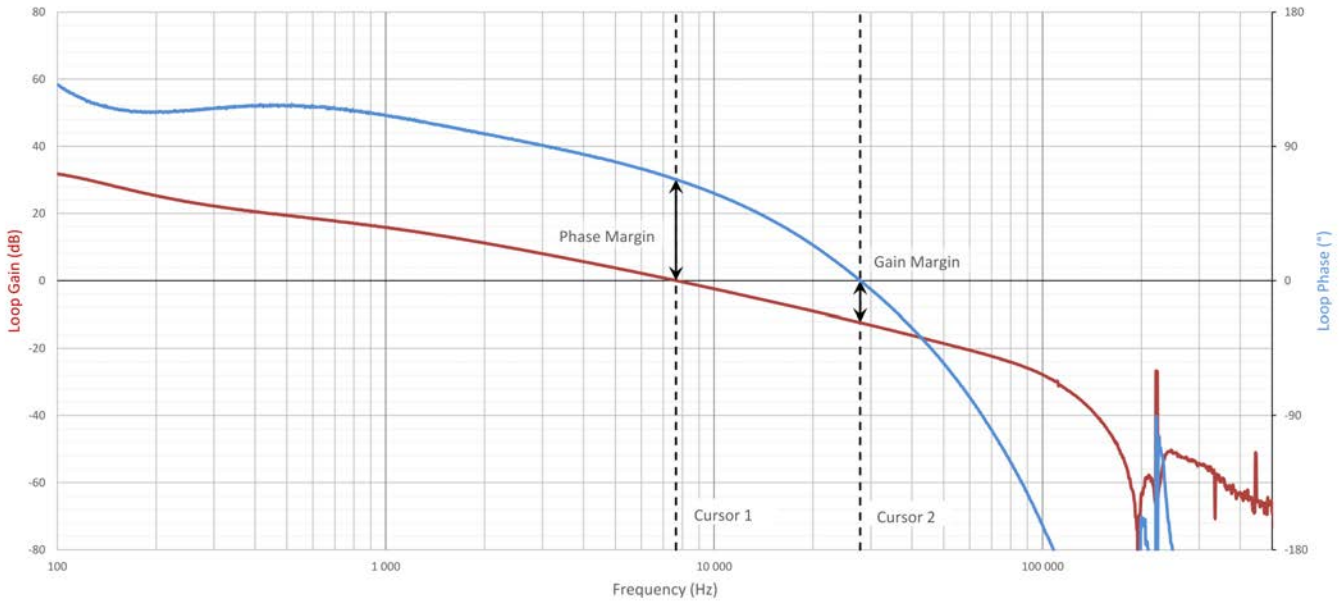


Figure 5.1. Si34062-ISO-FB-EVB Measured Loop-Gain and Phase with 7.5 W Load

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	7.6 kHz	0 dB	68°
Cursor 2 (Gain Margin)	27.8 kHz	–12.4 dB	0 °

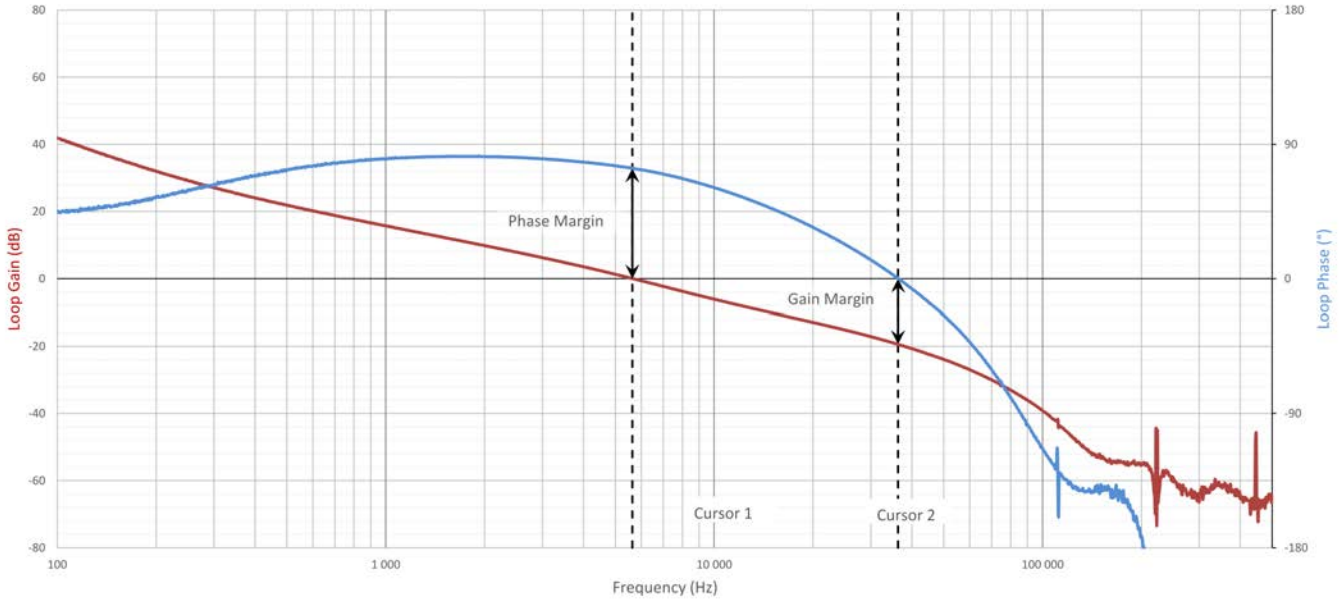


Figure 5.2. Si34062-ISO-FB-EVB Measured Loop-Gain and Phase with Unloaded Output

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	5.6 kHz	0 dB	74°
Cursor 2 (Gain Margin)	36.3 kHz	–19.4 dB	0 °

6. Load Step Transient Measurement Results

The Si34062-ISO-FB-EVB output has been tested with a load step function to verify the converters output dynamic response. Each output was tested separately, while one output was step-loaded, the other was unloaded.

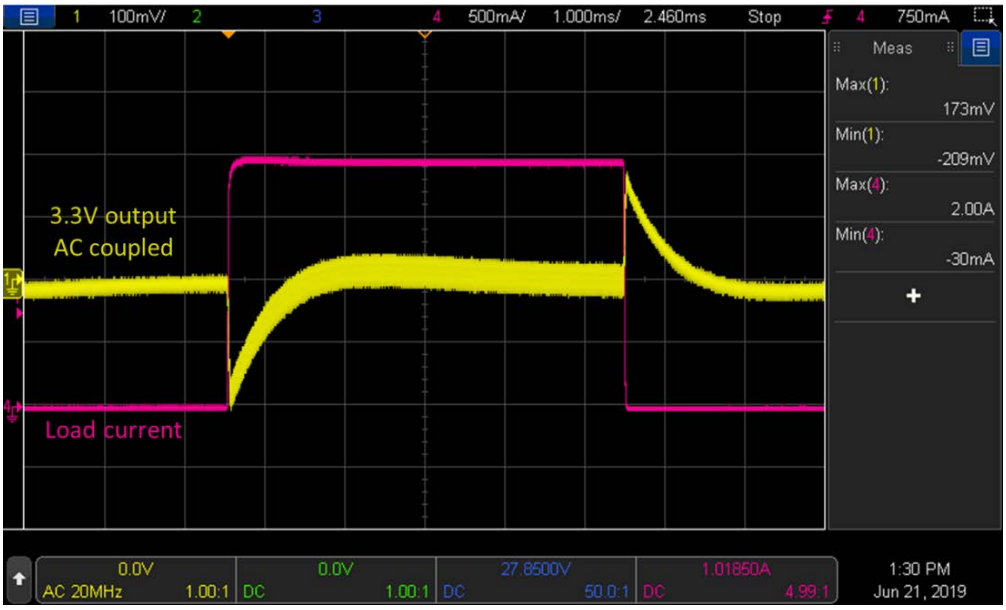


Figure 6.1. 3.3 V Output Load-Step Response (Current Step: 0 A ↔ 2 A)

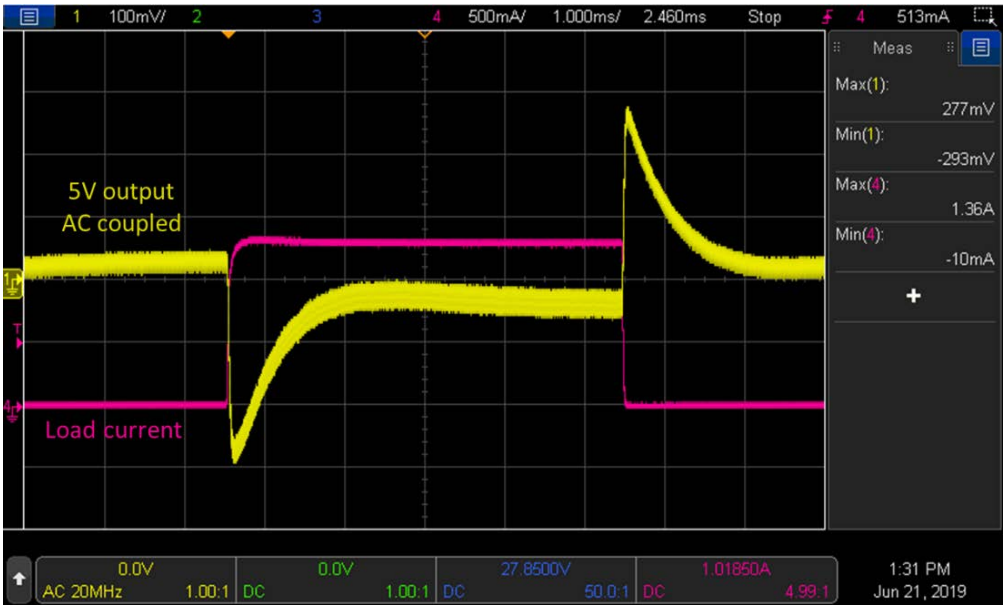


Figure 6.2. 5 V Output Load-Step Response (Current Step: 0 A ↔ 1.3 A)

Table 6.1. Output Load Step Transient

Output	Current Step	Undershoot	Overshoot
3.3 V	0 A ↔ 2 A	209 mV	173 mV
5 V	0 A ↔ 1.3 A	293 mV	277 mV

7. Output Voltage Ripple

The Si34062-ISO-FB-EVB board`s output voltage ripple has been measured at no-load and full-load conditions. The following figures show the respective results.

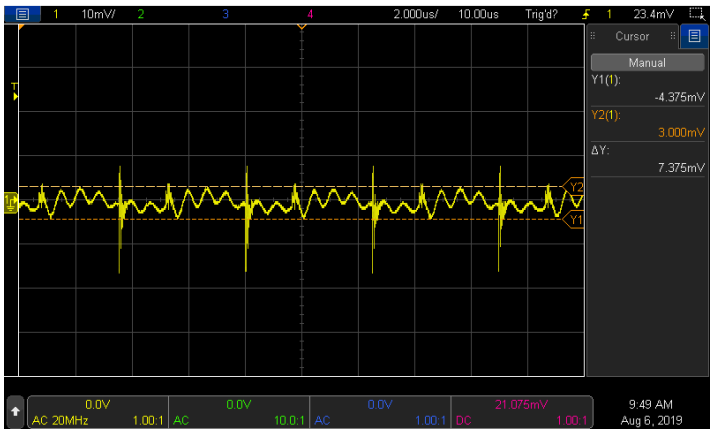


Figure 7.1. Si34062-ISO-FB-EVB 3.3 V Output Voltage Ripple at No-Load Condition (7 mV)

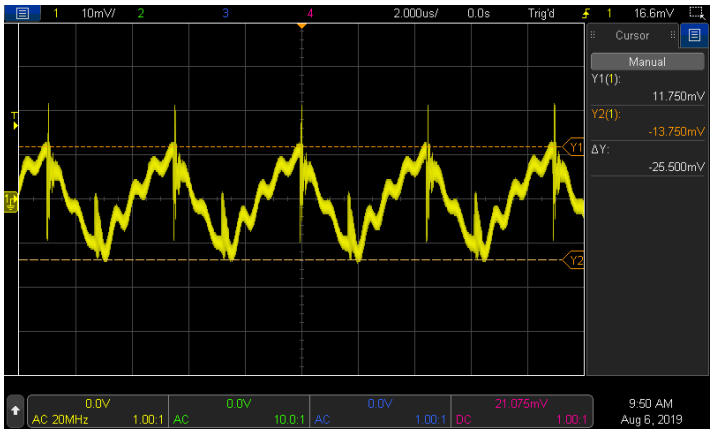


Figure 7.2. Si34062-ISO-FB-EVB 3.3 V Output Voltage Ripple at Full-Load Condition (25 mV)

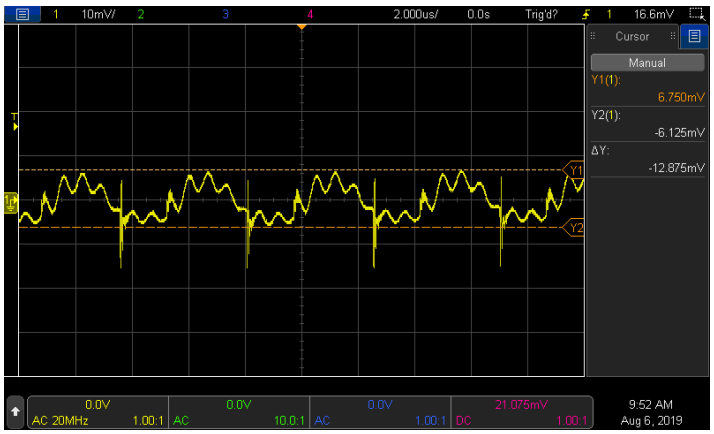


Figure 7.3. Si34062-ISO-FB-EVB 5 V Output Voltage Ripple at No-Load Condition (13 mV)

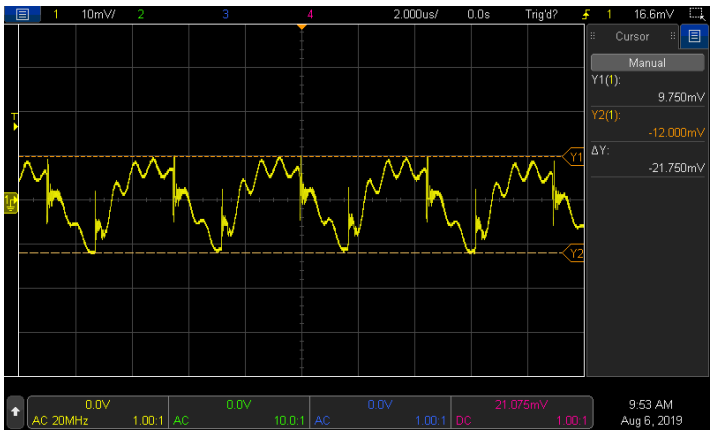


Figure 7.4. Si34062-ISO-FB-EVB 5 V Output Voltage Ripple at Full-Load Condition (22 mV)

8. Soft Start Protection

The Si34062 device has an integrated dynamic soft-start protection mechanism to protect components from sudden current or voltage changes associated with the initial charging of the output capacitors.

The Si34062 intelligent adaptive soft-start mechanism does not require any external components to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, thus adjusting the output voltage ramp-up time as a function of the attached load.

The controller alllows the output voltage to rise faster in a no-load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

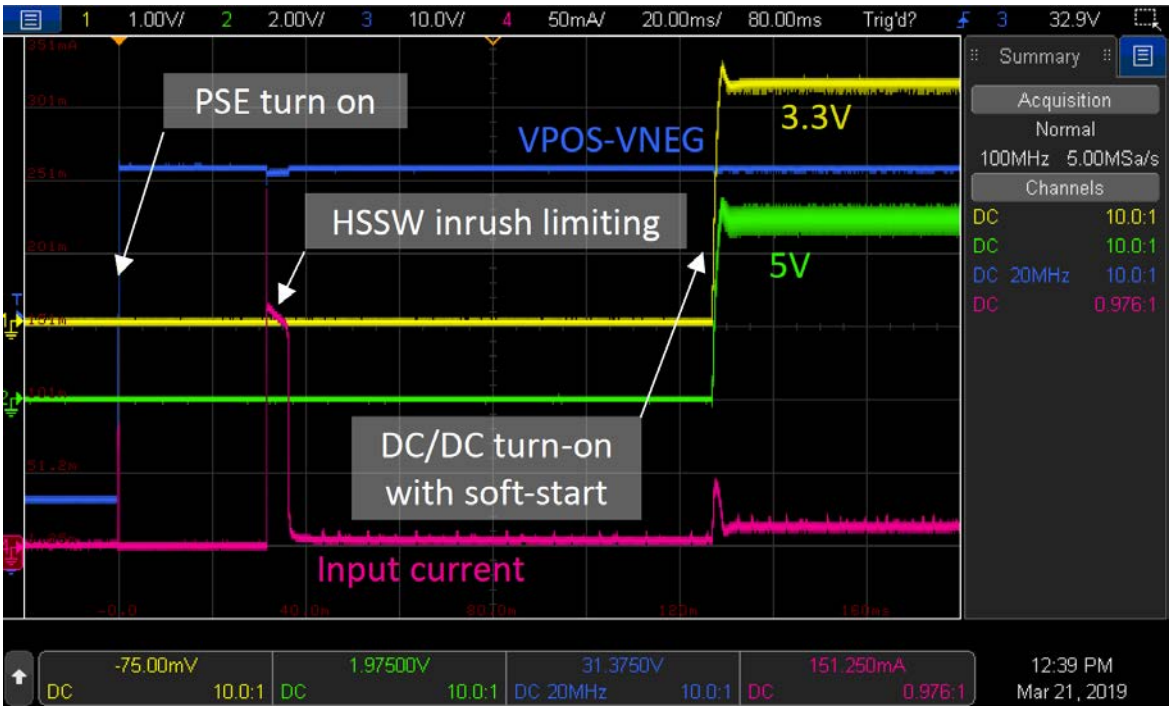


Figure 8.1. Soft Start Waveforms at No Load Condition

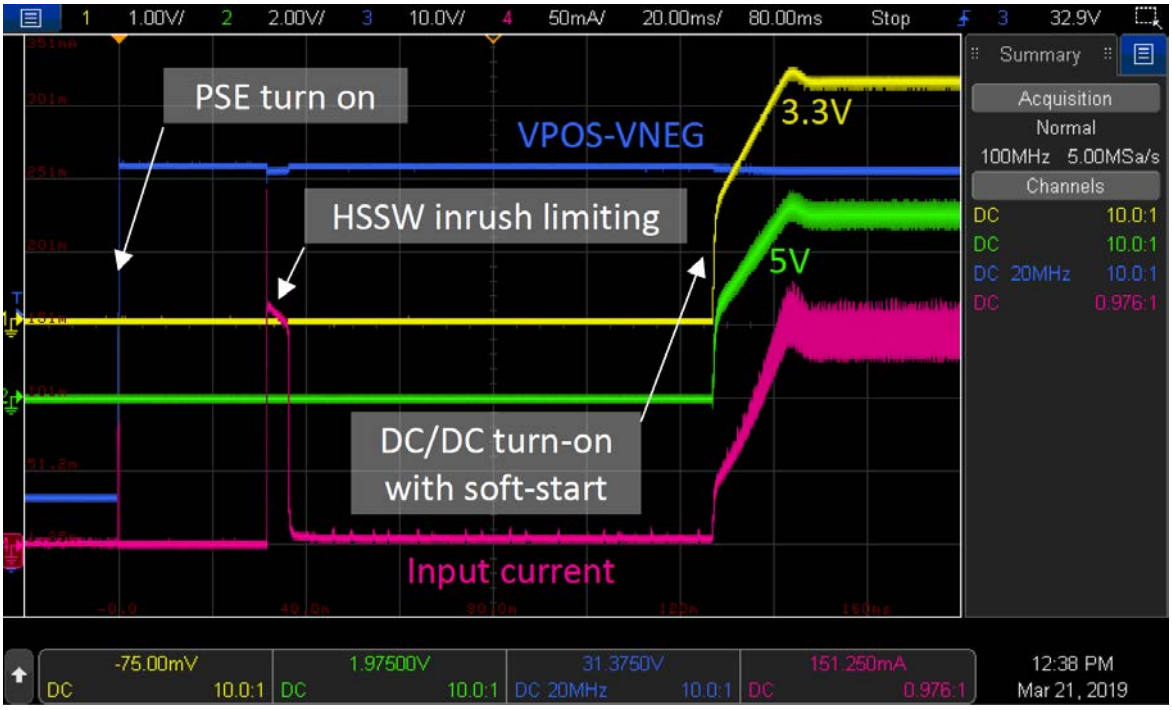


Figure 8.2. Soft Start Waveforms at Full Load Condition (7.5 W)

9. Output Short Protection

As the Si34062-ISO-FB-EVB uses a self-driven synchronous rectification technique, at output-short, the voltage on the SWO pin can rise above the absolute maximum rating of the SWO pin, which can cause immediate failure of the device. If output short protection is required, the SWO protection should be modified. Instead of using an RCD circuit, a Zener-clamp needs to be installed. If output short protection is required, D16-R33-C23 should be replaced with a Zener clamp as shown in the following figure.

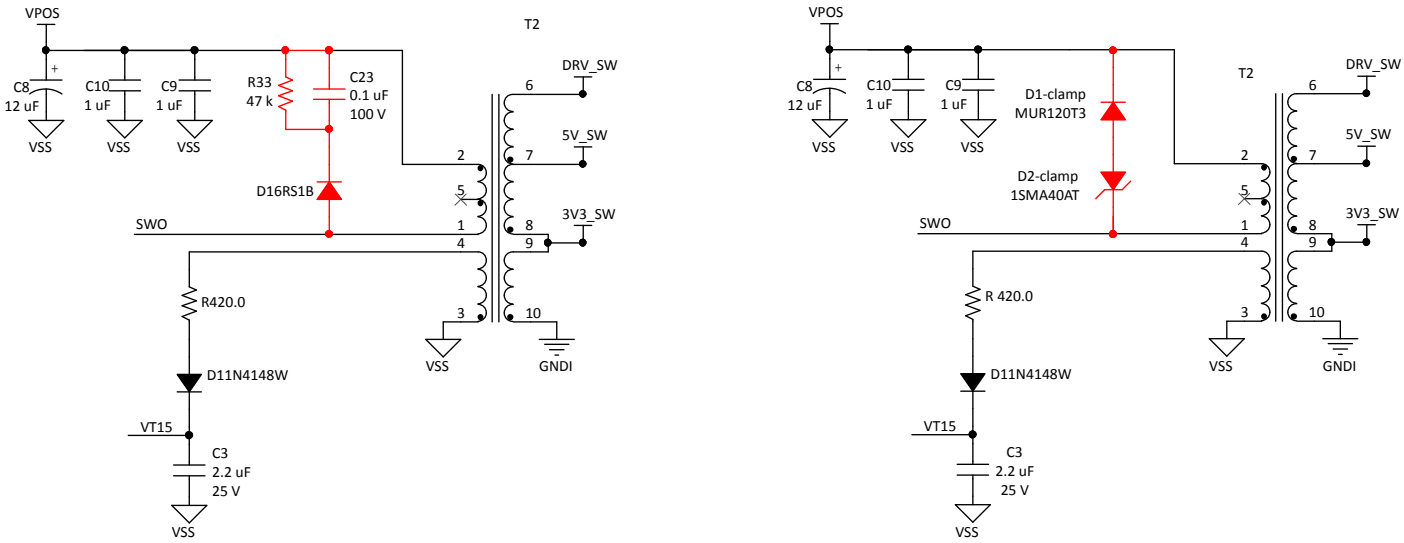


Figure 9.1. Circuit Modification for Output Short Protection

The modified circuit protects the IC if an accidental short occurs at the output for a short amount of time. If a steady short occurs at the output, the secondary side rectification FETs (Q1 and Q3) can overheat.

10. CCM Mode at No-Load Condition

The converter always runs in continuous conduction mode (CCM). There are two main benefits from this configuration:

- No need for a gate transformer (BOM cost reduction)
- Much better transient response due to the lack of DCM operation at low-load condition

The following figure shows that the circuit stays in CCM operation, even at no-load condition:

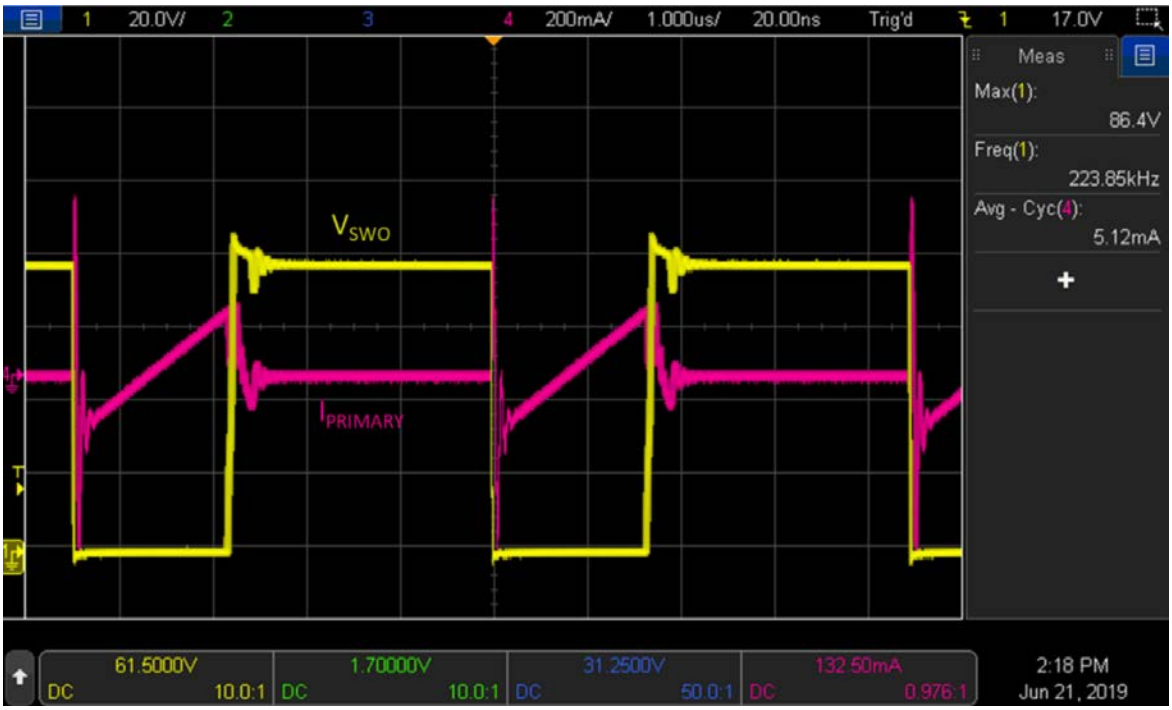


Figure 10.1. CCM Mode at No-Load Condition

11. Adjustable EVB Current Limit

For additional safety, the Si34062 has an adjustable EVB current limit feature.

The Si34061 controller measures the voltage on the R_{SENSE} (R7) through the ISNS pin. Attention must be paid that this voltage goes below V_{SS}.

When V_{RSENSE} reaches –270 mV (referenced to V_{SS}), the current limit circuit restarts the circuit to protect the application

The average input current limit for this Class 2 application can be calculated with the following formula:

$$R_{SENSE} = 680m\Omega$$

$$I_{LIMIT} = \frac{270mV}{R_{SENSE}} = \frac{270mV}{680m\Omega} = 397mA$$

Equation 1. Average Input Current Limiter

12. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor, R14, connected between the RFREQ and VPOS pins.

The following figure will aid in selecting the R_{FREQ} value to achieve the desired switching frequency.

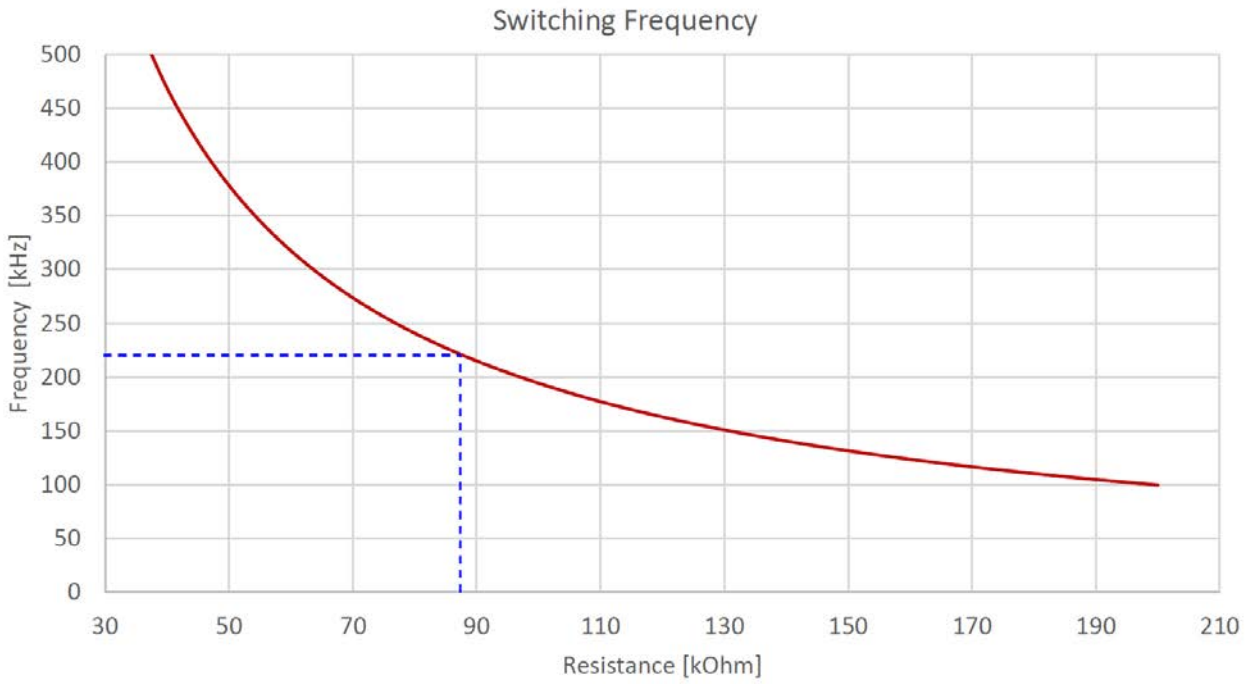


Figure 12.1. Switching Frequency vs. R_{FREQ} Value

The selected switching frequency for Si34062-ISO-FB-EVB is 220 kHz, which is achieved by setting resistor R2 to 88.7 kΩ.

13. Synchronous Rectification

The Si34062-ISO-FB-EVB uses self-driven synchronous rectification with a drive-winding on the flyback transformer. The secondary side rectifier MOSFETs are driven by the flyback transformer winding through pin 7 and pin 6 of T2. In this configuration, the converter always runs in continuous conduction mode (CCM).

There are two main benefits of this configuration:

- No need for a gate transformer (BOM cost reduction)
- No DCM operation at low load conditions improves transient response

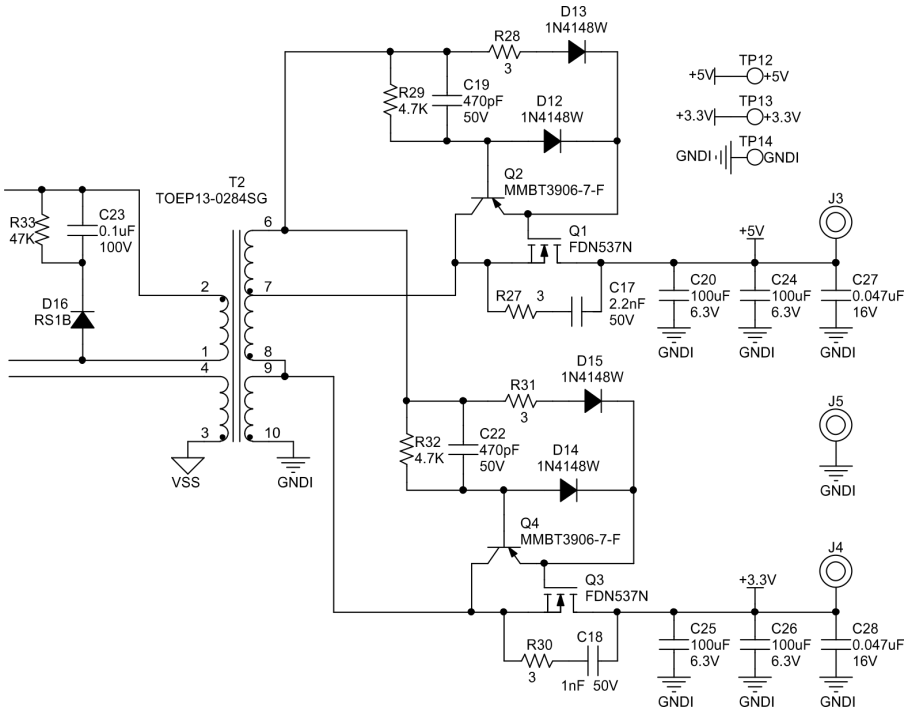


Figure 13.1. Self-Driven Synchronous Rectification

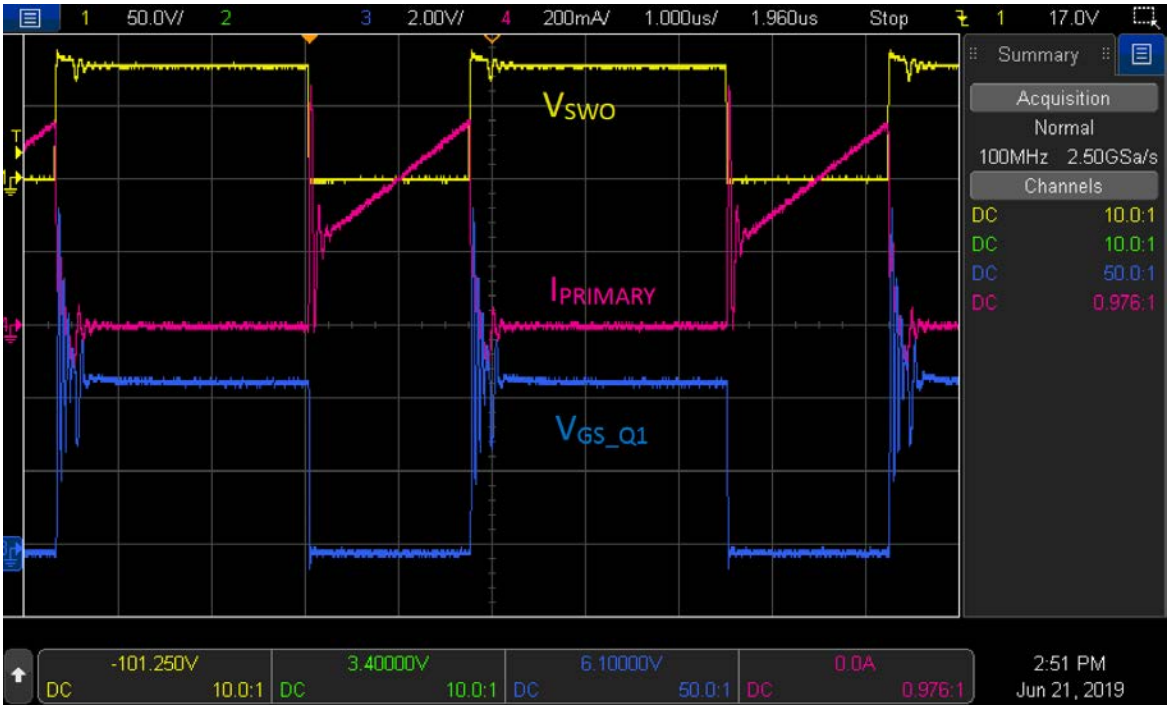


Figure 13.2. V_{GS} Voltage of Synchronous Rectifier MOSFET Q1 of 5 V Output

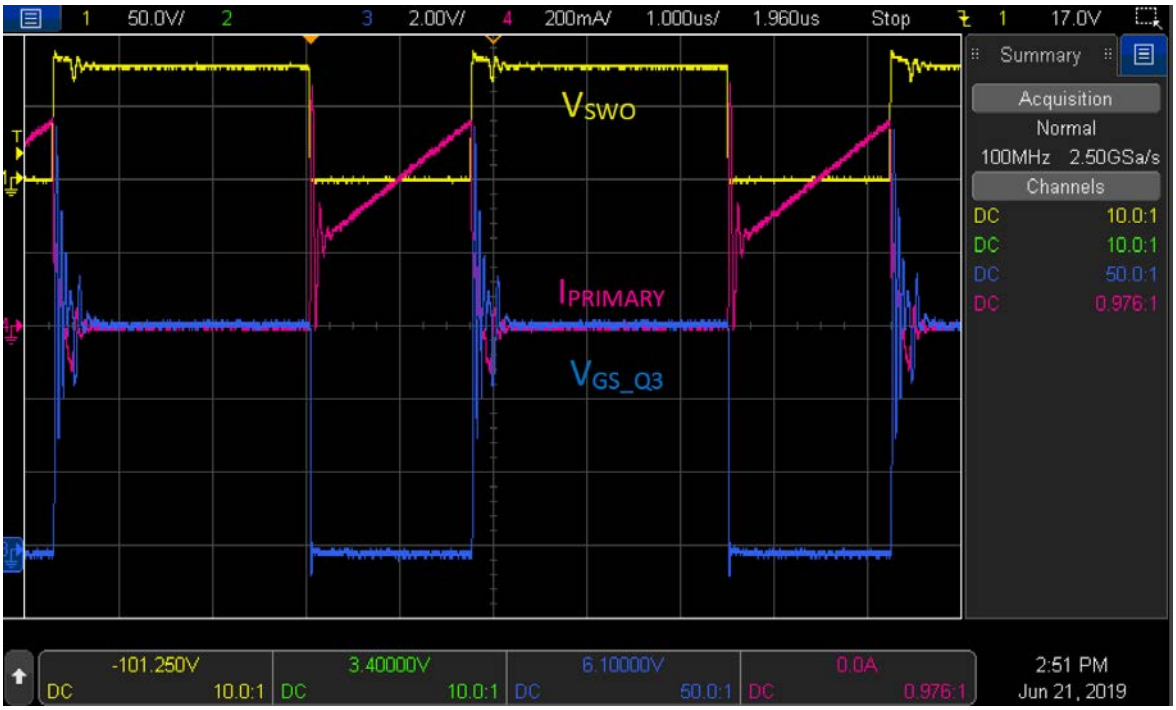


Figure 13.3. V_{GS} Voltage of Synchronous Rectifier MOSFET Q3 of 3.3 V Output

14. Maintain Power Signature

The Si34062-ISO-FB-EVB supports ultra-low power SLEEP mode by disabling the dc/dc converter but keeping the connection with the PSE. In SLEEP mode the circuit is able to generate Maintain Power Signature (MPS) pulses to ensure that PSE does not disconnect the power from the PD.

Pressing the SLEEP button during normal operation (in WAKE mode) disables the dc/dc converter and turns on LED D2, and the EVB's input current consumption falls to approximately 5 mA. Depending on the MODE switch state, it can enable the MPS current pulses in SLEEP mode. If MODE = Lo at the moment the SLEEP button is pressed, then MPS generation is enabled in SLEEP mode.

The MODE switch has two functions:

- It controls status LED D2 in WAKE mode and
- MPS generation in SLEEP mode

In WAKE mode, if MODE=Hi →LED D2 turns on; if MODE=Lo →LED D2 turns off. MPS generation depends on the logic state of the MODE switch at the moment when the SLEEP button is pressed, MODE = Lo →MPS generation enabled in SLEEP mode, MODE=Hi →MPS generation disabled in SLEEP mode.

Pushing the WAKE button in SLEEP mode enables the dc/dc converter and disables MPS generation.

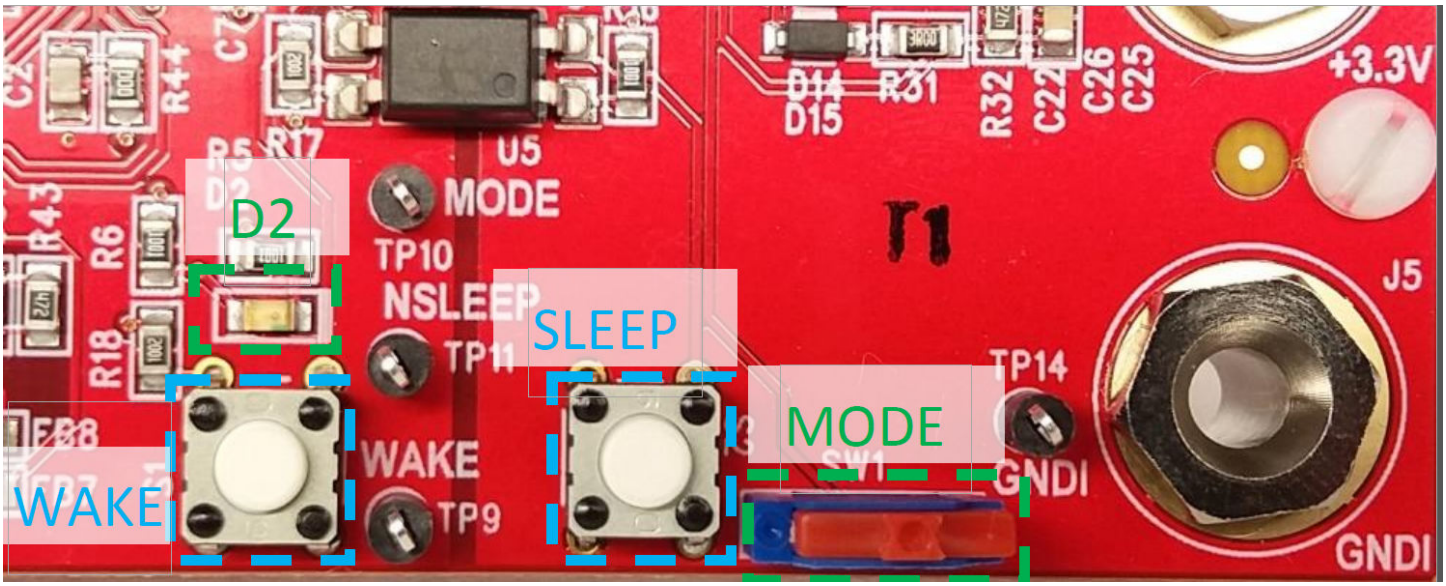


Figure 14.1. Control Switches for WAKE, SLEEP and MPS Generation

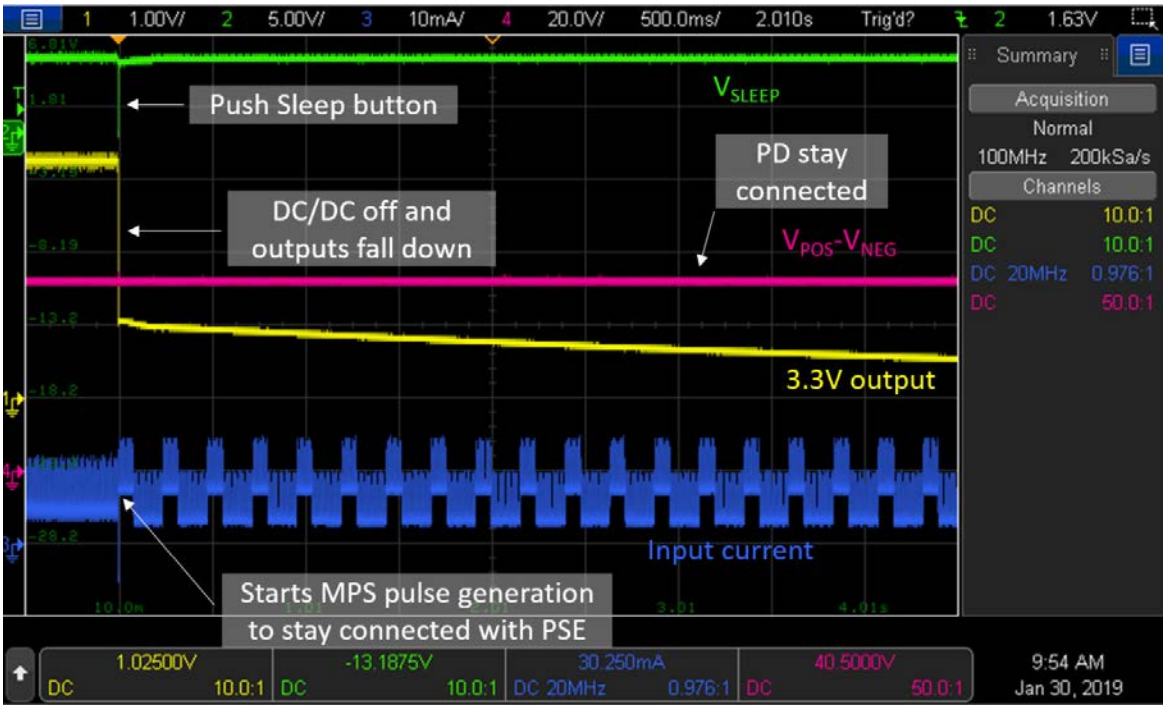


Figure 14.2. Sleep with Enabled MPS Generation

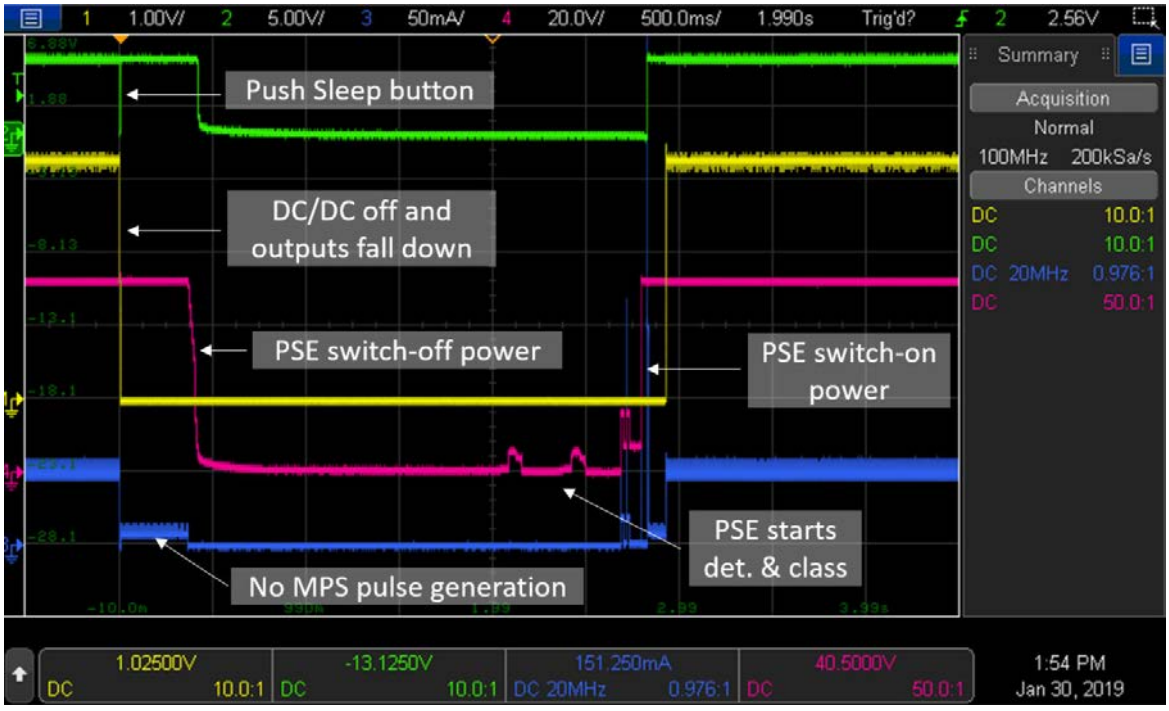


Figure 14.3. Sleep with Disabled MPS Generation

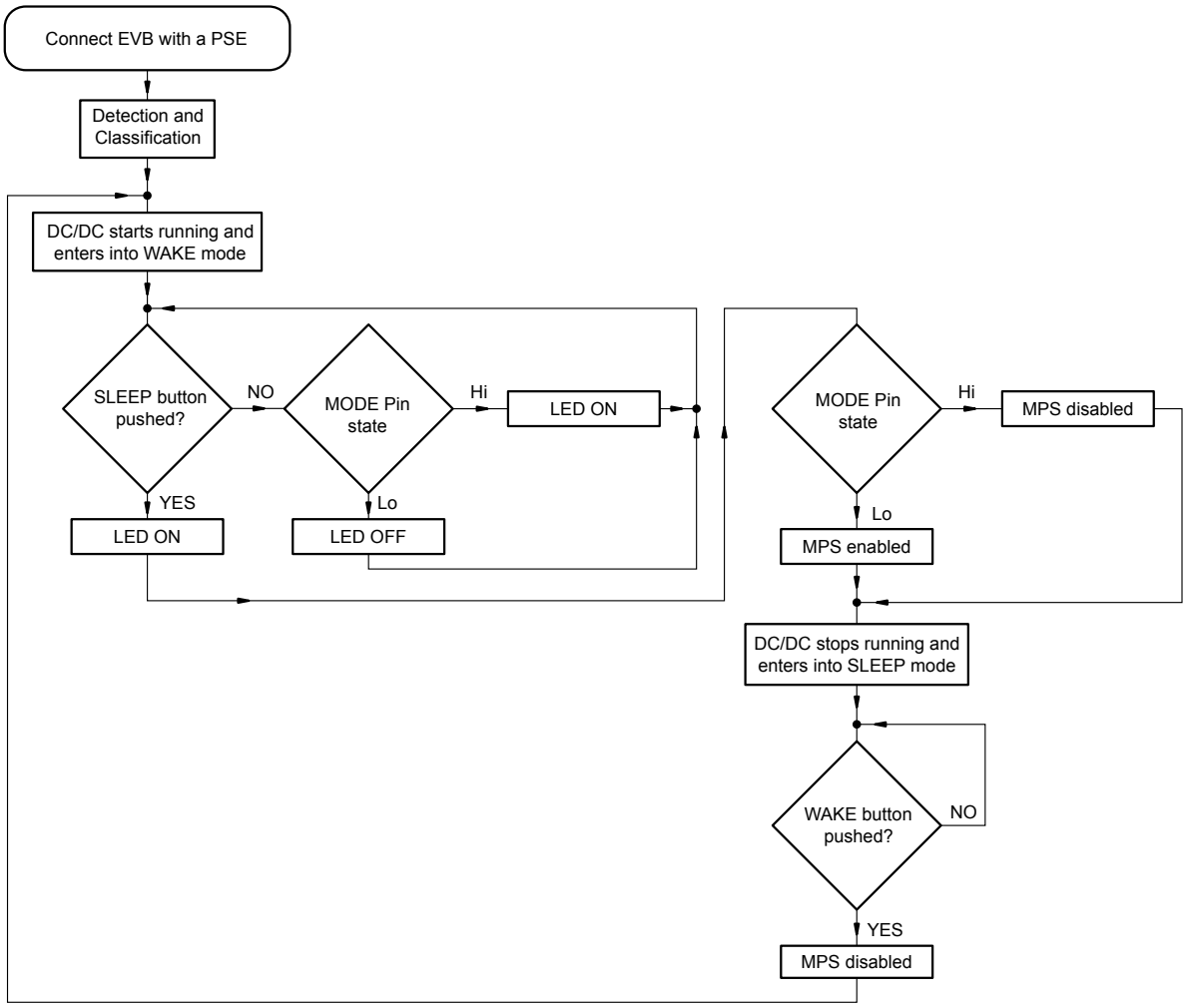


Figure 14.4. Flow Diagram of WAKE/SLEEP Modes

15. Wall Adapter Support with Priority over PSE

The Si34062-ISO-FB-EVB can operate from the PoE+DATA input (PSE) or a high-voltage auxiliary wall adapter delivering 48 V.

The adapter has higher priority over the PSE. Whenever the adapter is present, the PD will consume the power from the adapter. By connecting the adapter to connector J4, MOSFET Q5 turns off, and the PSE disconnects the port as the consumption is lower than 10 mA. The PWM controller keeps running continuously, which ensures no output voltage interrupt.

During adapter mode operation the PD shows an invalid detection signature toward the PSE, therefore the PSE is unable to turn ON the port until the PD is running from the wall adapter.

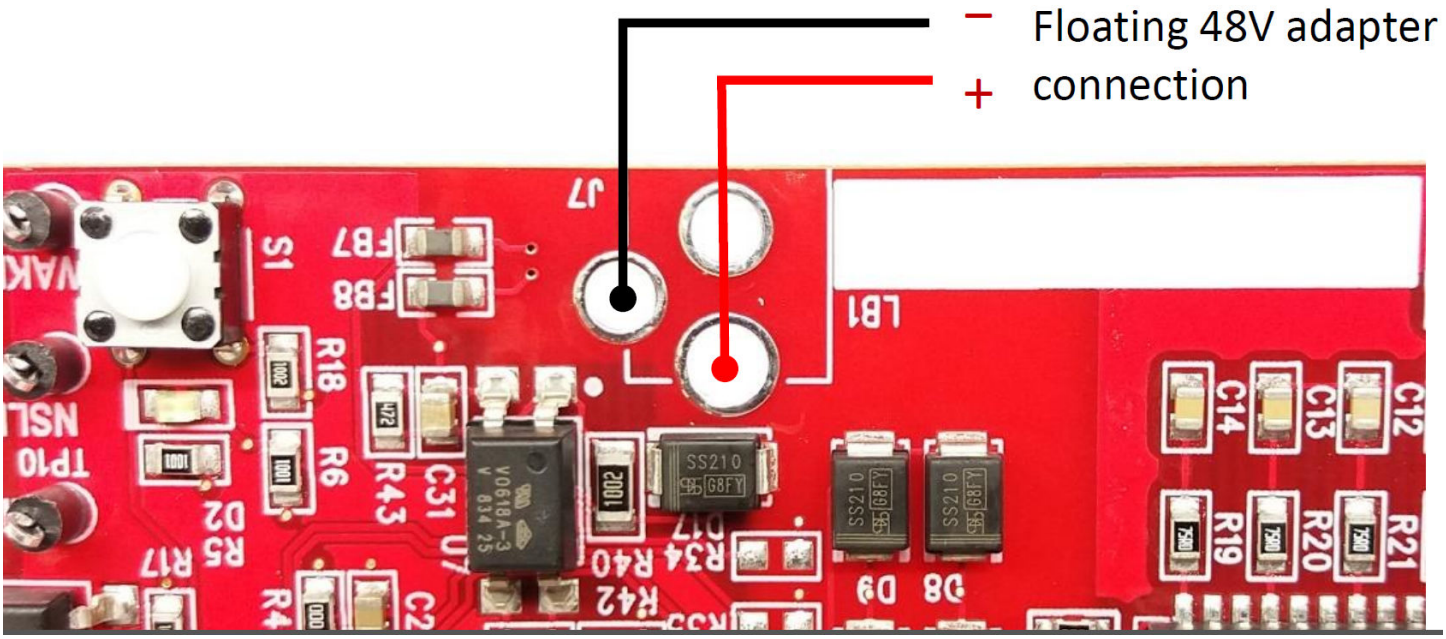


Figure 15.1. Auxiliary Wall Adapter Connection

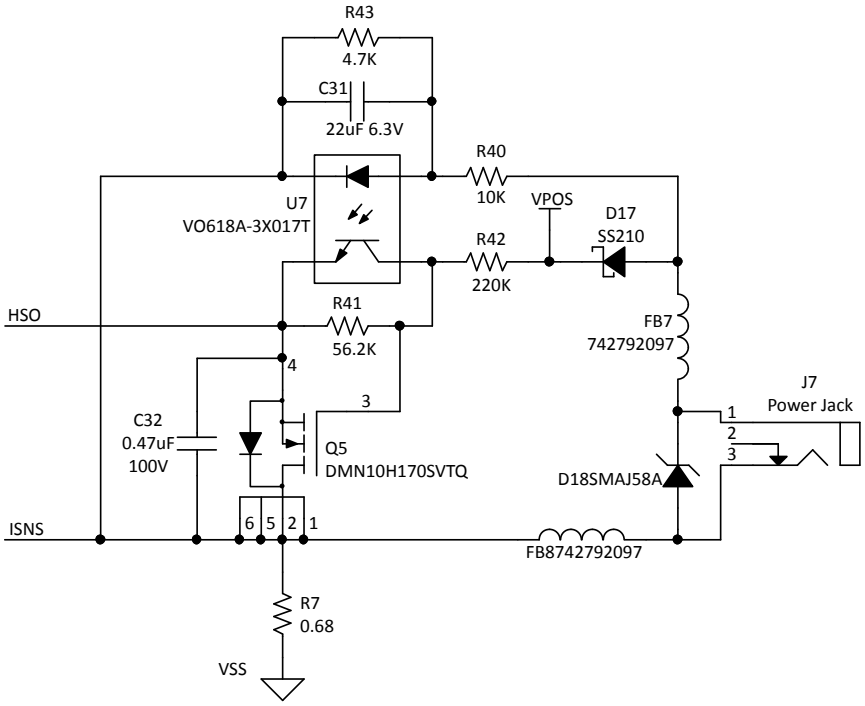


Figure 15.2. Wall Adapter Support Circuit with Adapter Priority

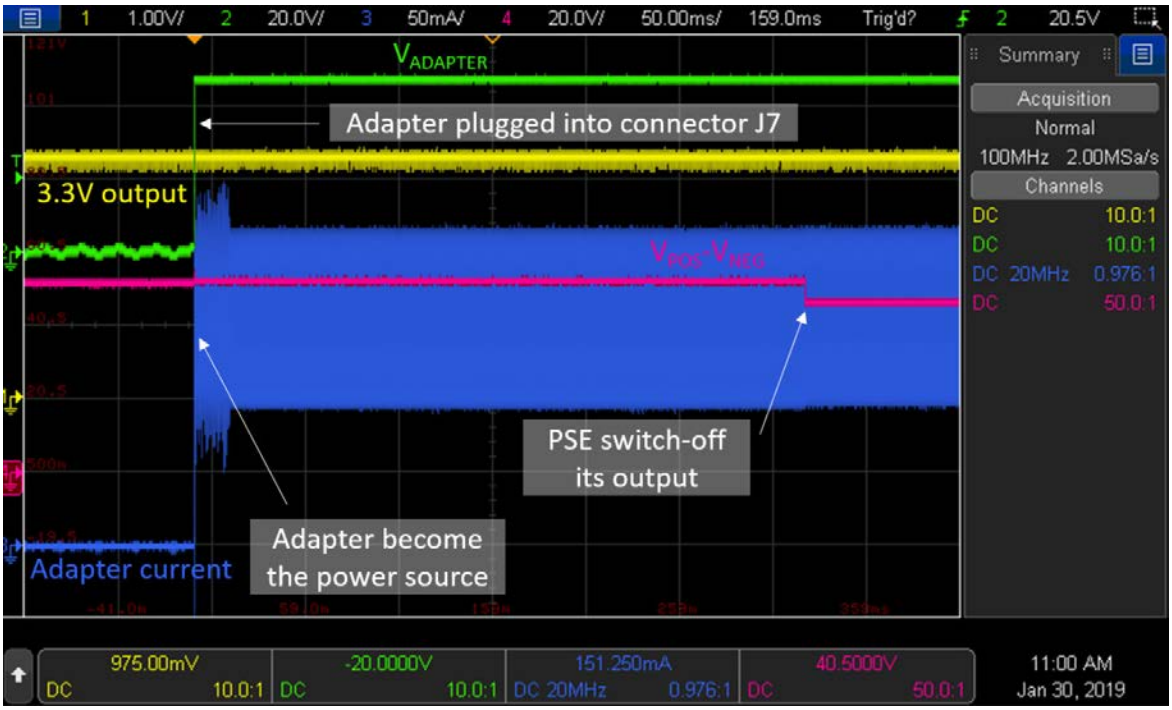


Figure 15.3. Wall Adapter Sequence Using ASUP Pin

16. Radiated Emissions Measurement Results—EN55032 Class B

Radiated emissions of the Si34062-ISO-FB-EVB board have been measured with 50 V input voltage and a full load connected to the output (7.5 W).

As shown below, the Si34062-ISO-FB-EVB is fully compliant with the international EN 55032 class B emissions standard:

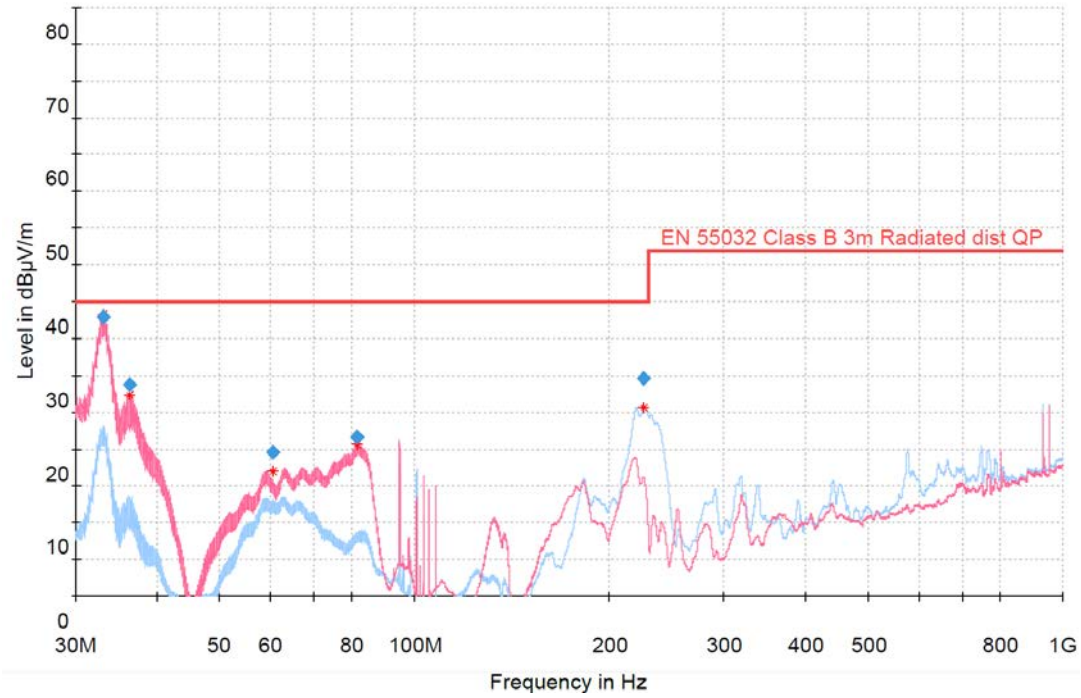


Figure 16.1. Si34062-ISO-FB-EVB Radiated Emission Measurement Results

Radiated EMI Measurement Process

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization).

Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

17. Conducted Emissions Measurement Results—EN55032

The Si34062-ISO-FB-EVB board's conducted emissions have been measured in two different configurations. In the first configuration, it is supplied and measured on its PoE input port as shown in the next figure below. The spectrum analyzer detector is set to average and peak detector, and both results are shown below.

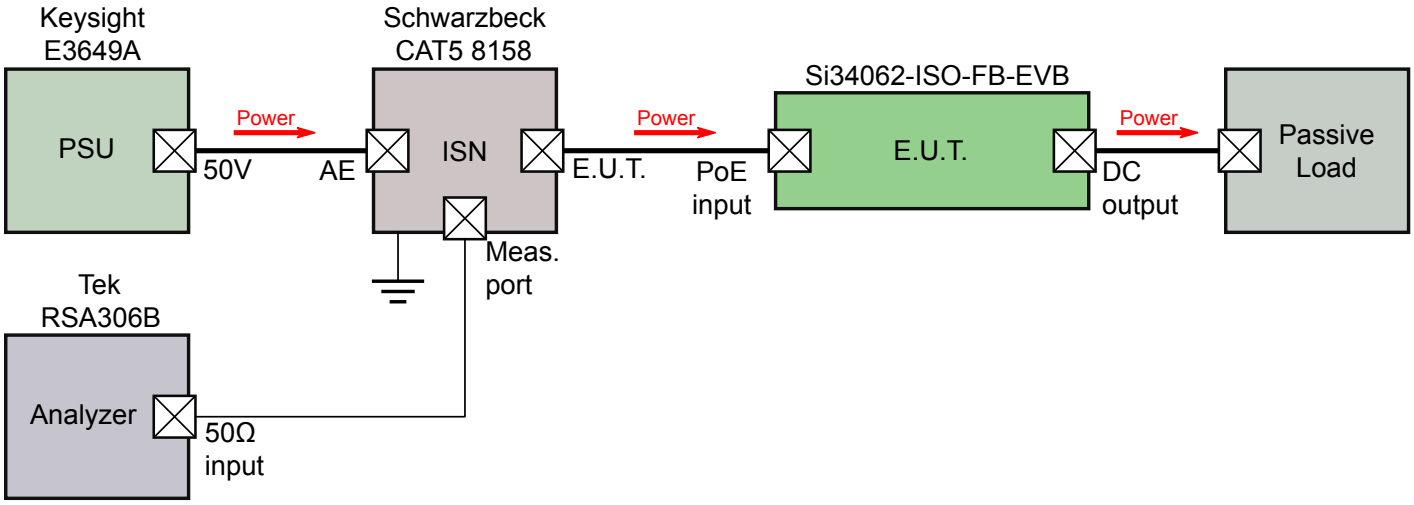


Figure 17.1. Conducted EMI Measurement Setup for PoE Input

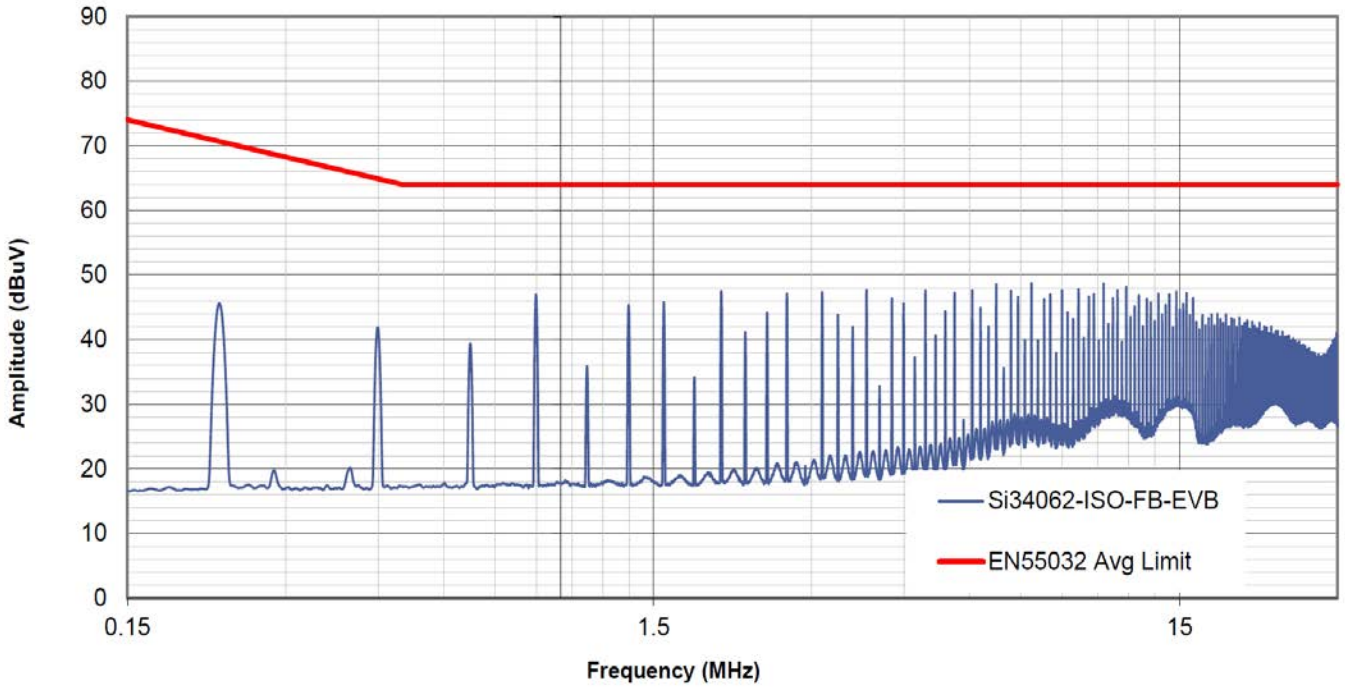


Figure 17.2. Conducted Emissions Measurement on PoE Input, 50 V Input, 7.5 W Load, Average Detector

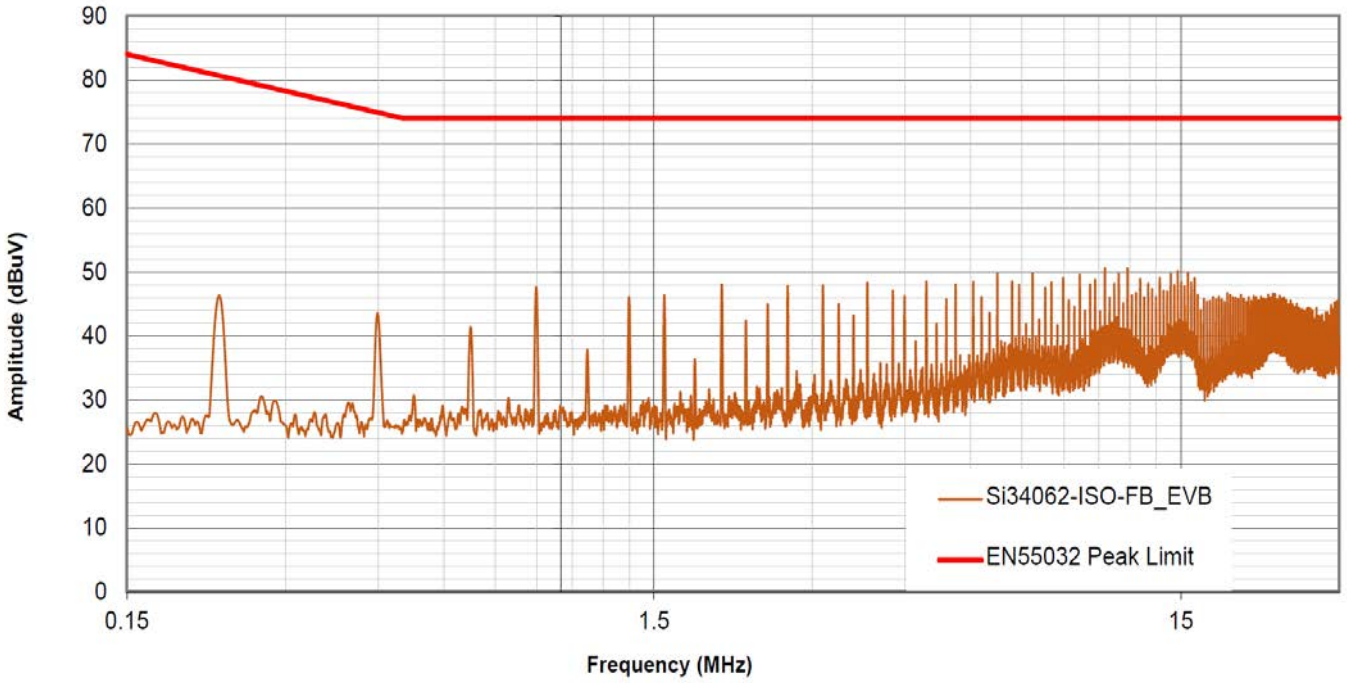


Figure 17.3. Conducted Emissions Measurement on PoE Input, 50 V Input, 7.5 W Load, Peak Detector

In the second configuration, the Si34062-ISO-FB-EVB is supplied from the adapter input and measured on the PoE port as shown in the next figure below. In this configuration, the PSE disconnects power while PD runs from adapter input port. The spectrum analyzer detector is set to average and peak detector; both results are shown below.

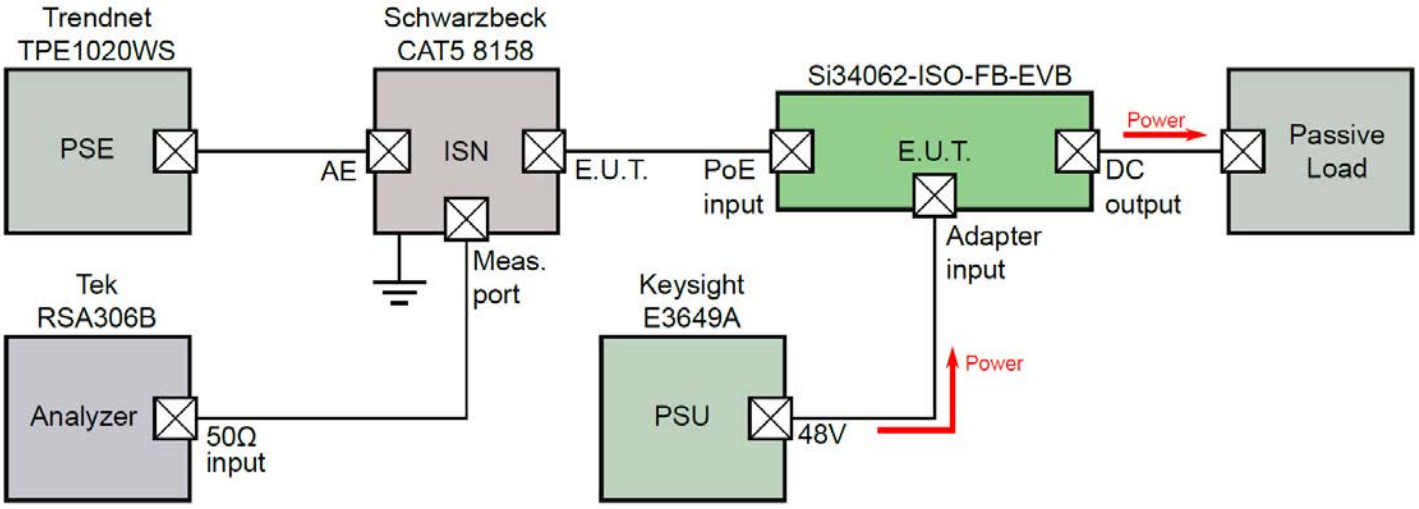


Figure 17.4. Conducted EMI Measurement Setup for Adapter Input

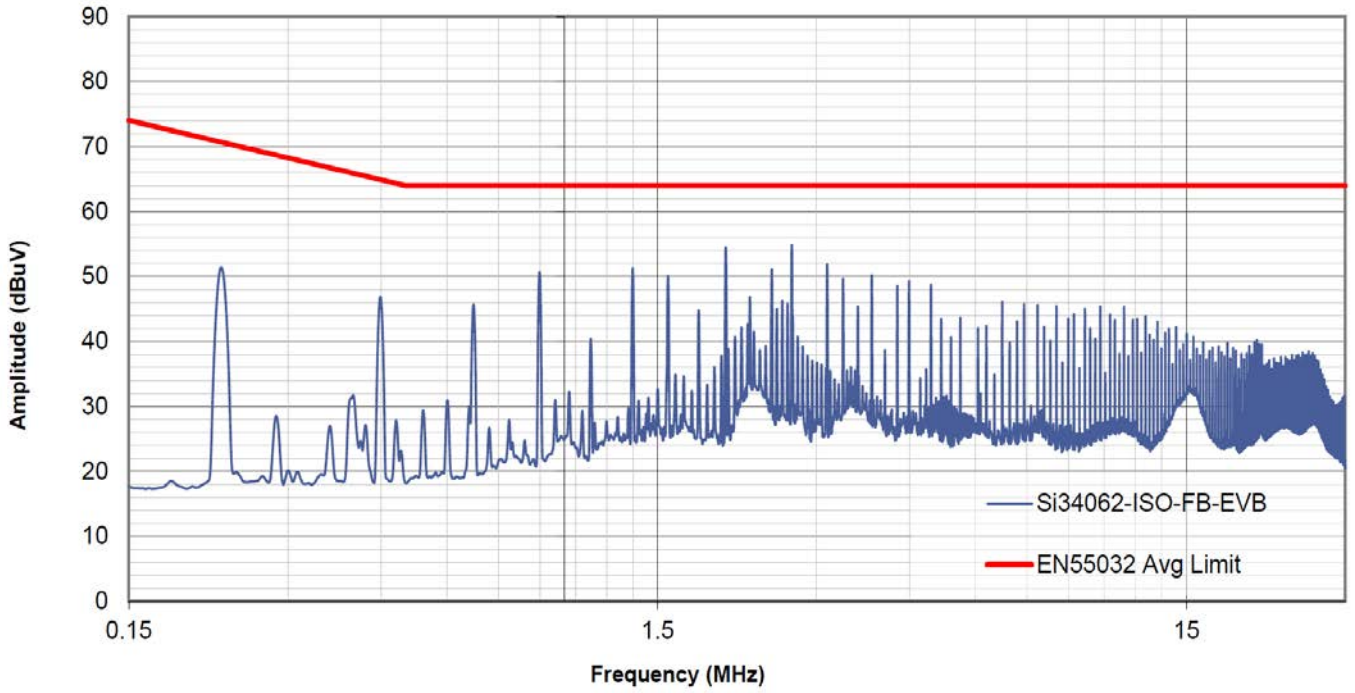


Figure 17.5. Conducted Emissions Measurement on Adapter Input, 48 V Input, 7.5 W Load, Average Detector

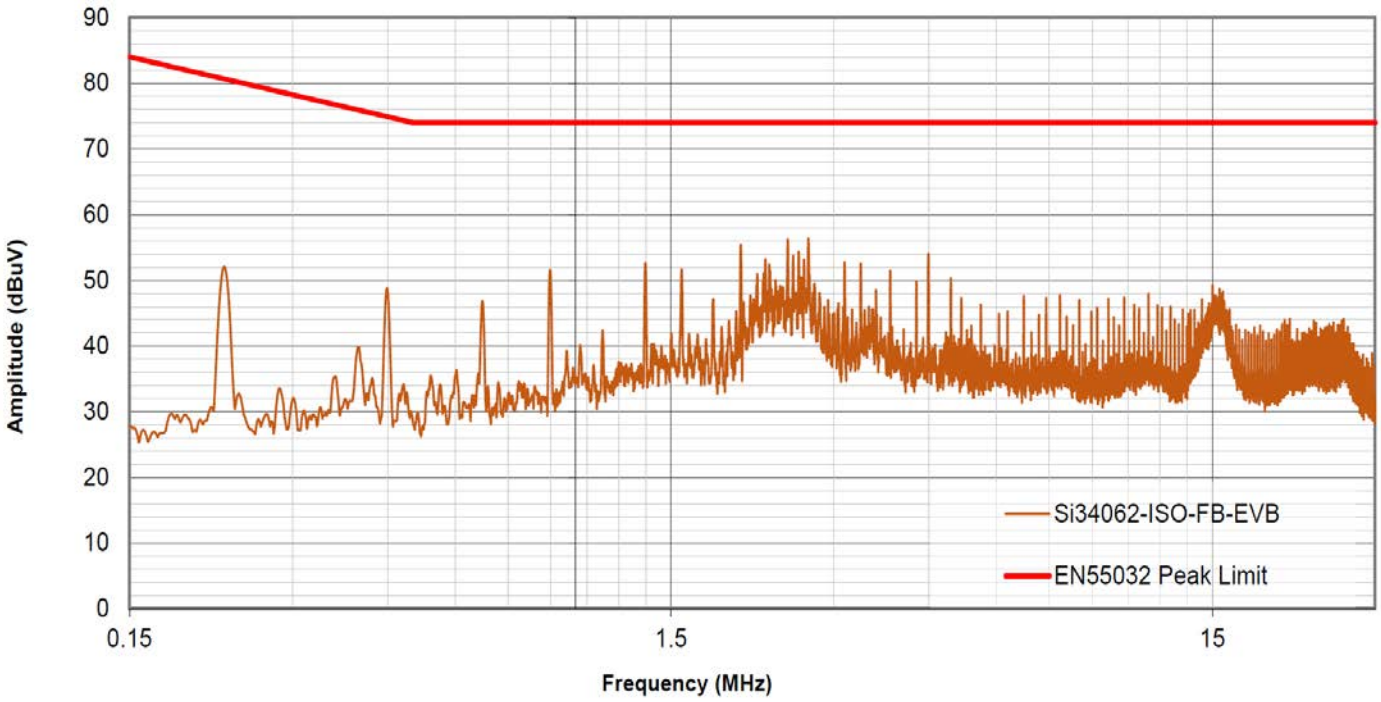


Figure 17.6. Conducted Emissions Measurement on Adapter Input, 48 V Input, 7.5 W Load, Peak Detector

18. Thermal Measurements

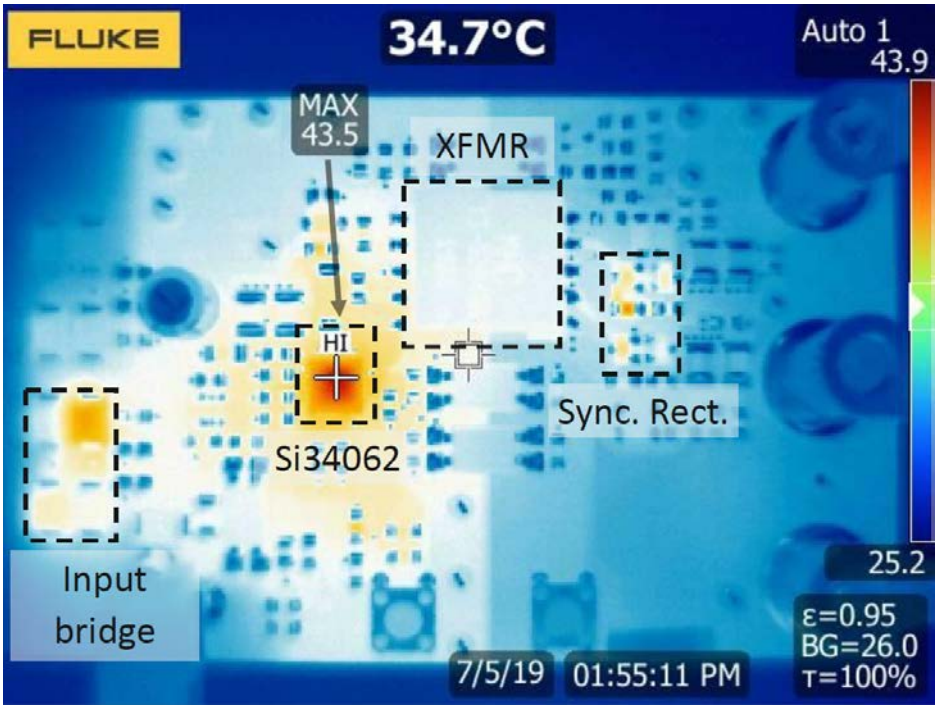


Figure 18.1. Thermal Image of the Top Side, 50 V Input Voltage and 7.5 W Load (3.3 V/3 Ω, 5 V/8 Ω)

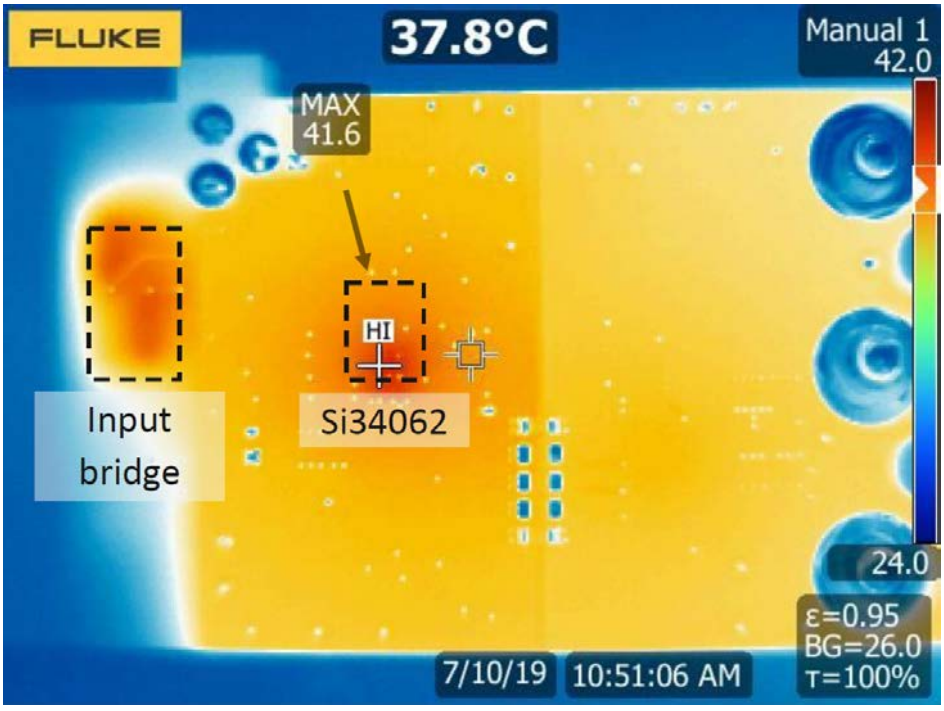


Figure 18.2. Thermal Image of the Bottom Side, 50 V Input Voltage and 7.5 W Load (3.3 V/3 Ω, 5 V/8 Ω

Note: Ambient temperature was 26 °C.

19. Layout

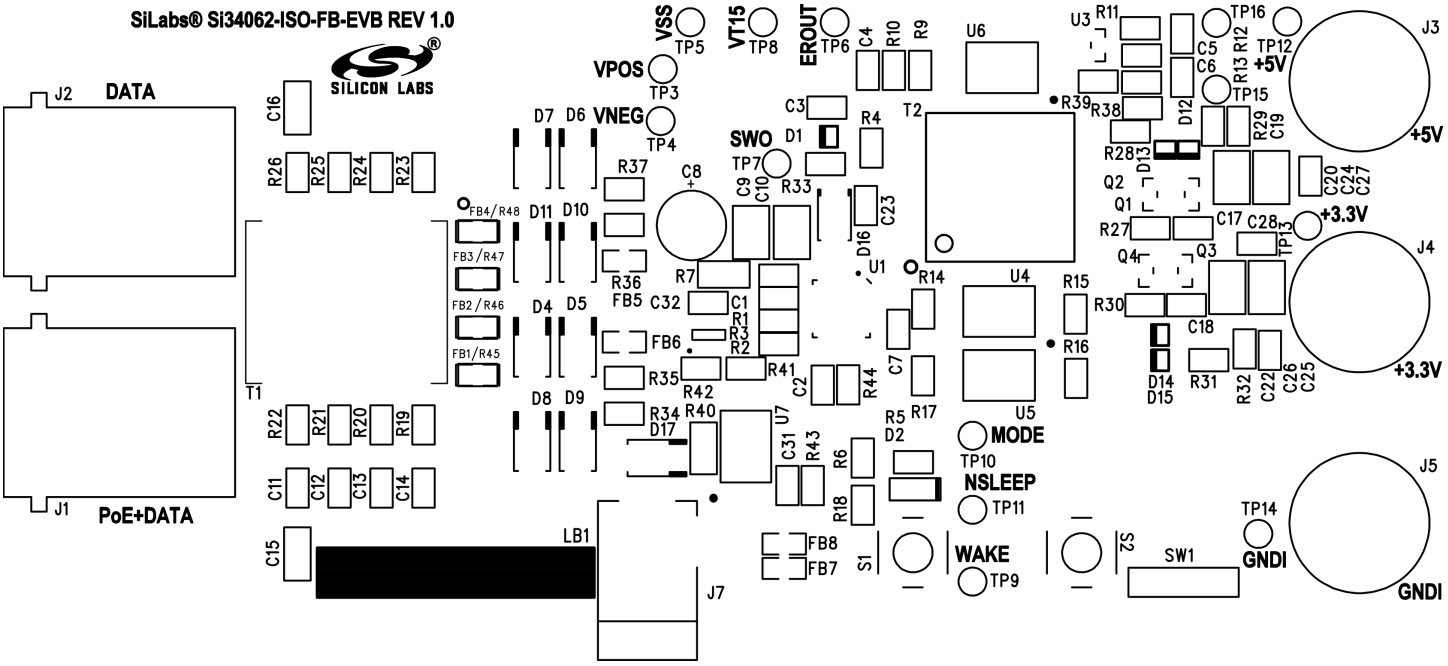


Figure 19.1. Primary Silkscreen

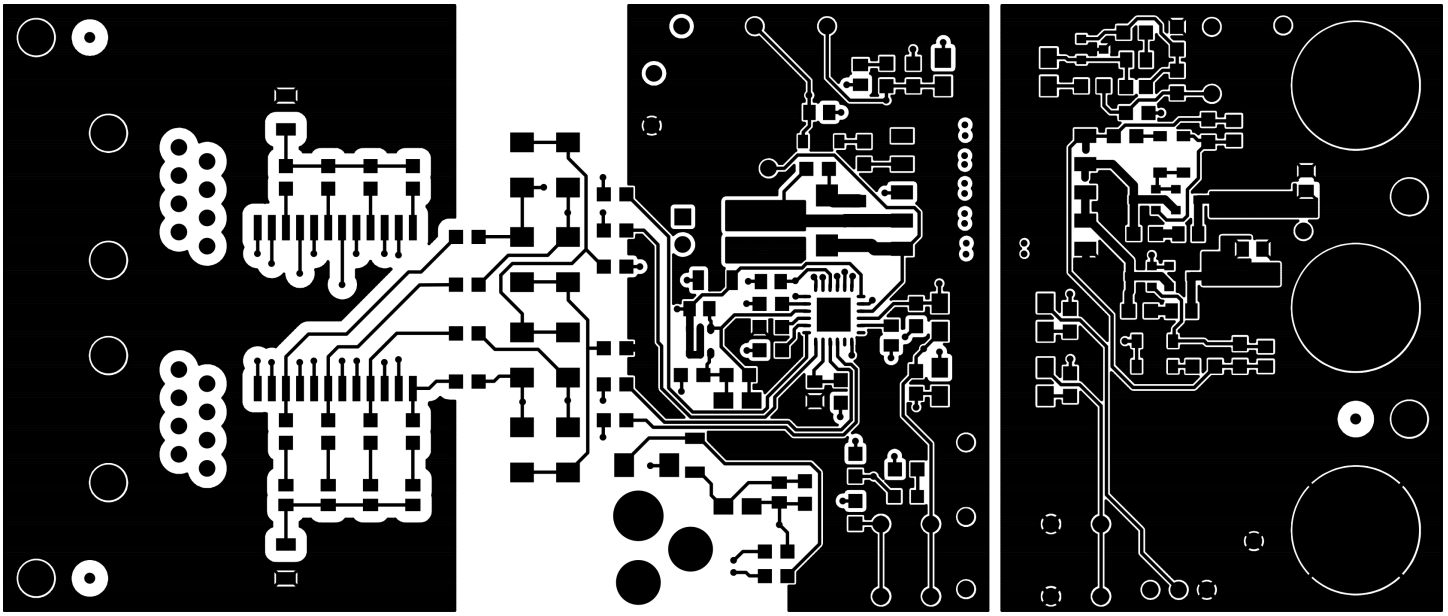


Figure 19.2. Top Layer

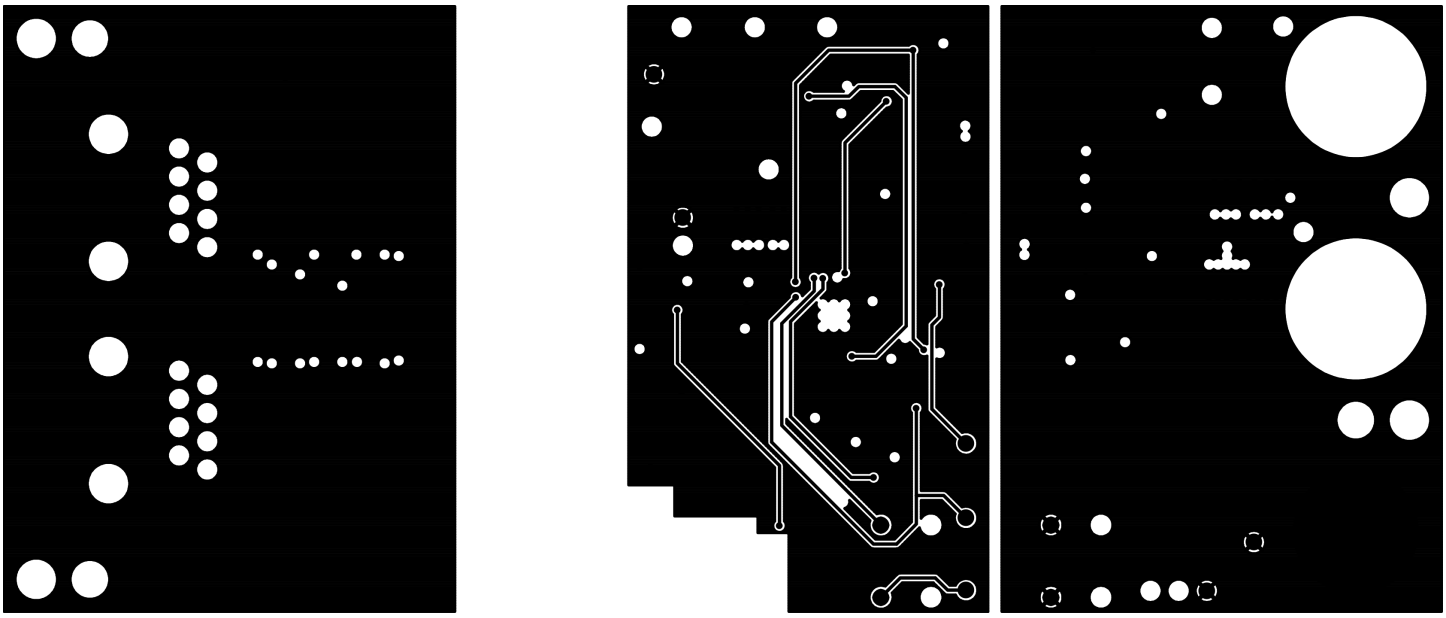


Figure 19.3. Internal 1 Layer

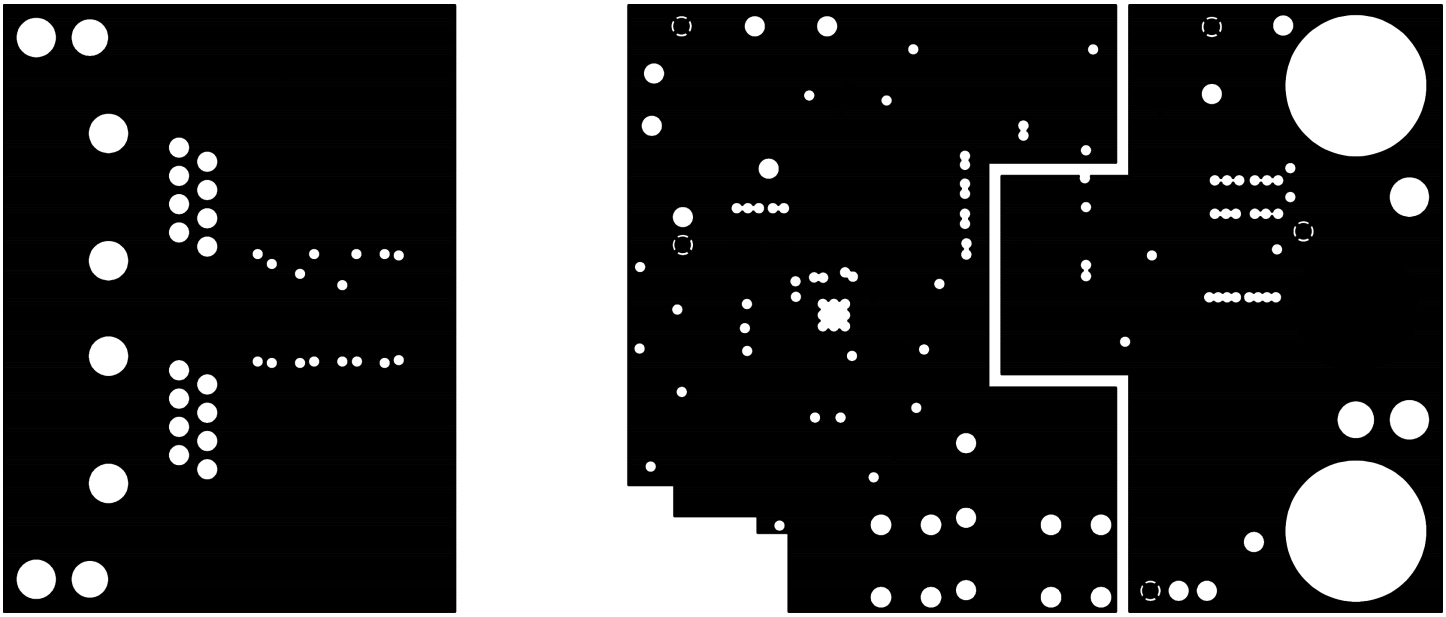


Figure 19.4. Internal 2 Layer

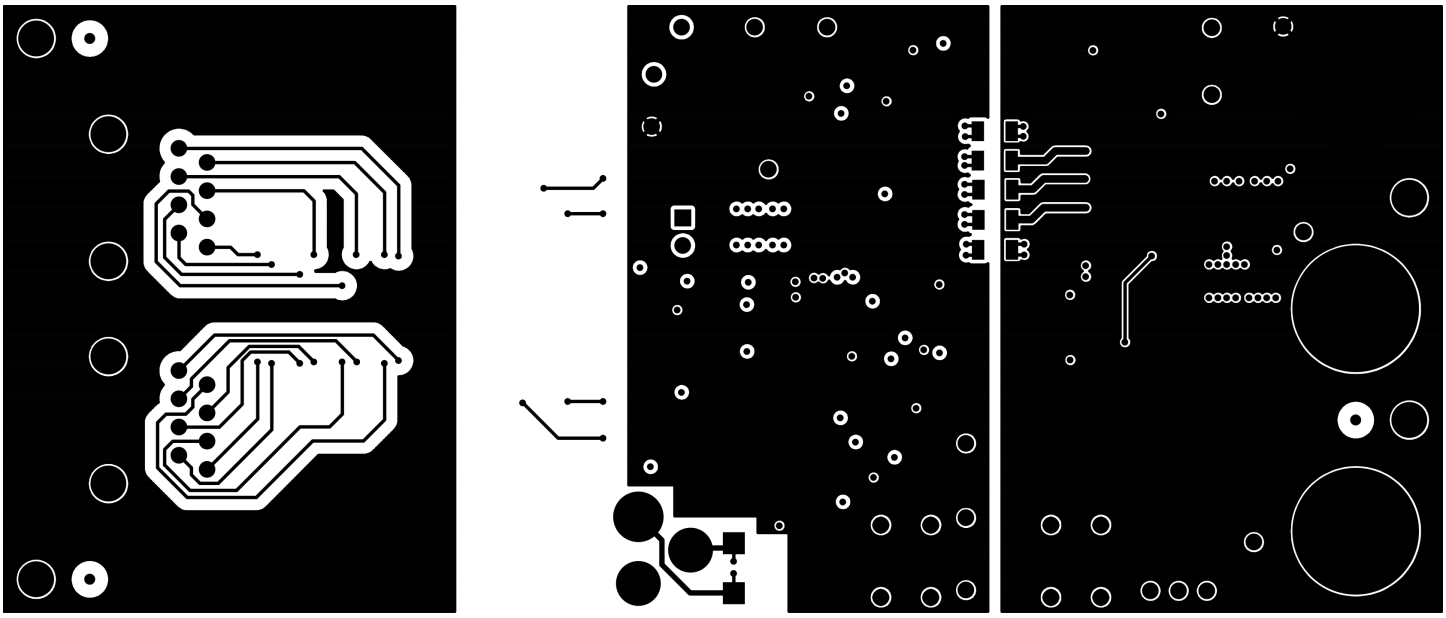
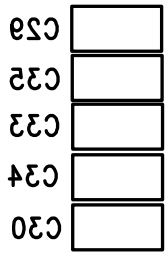


Figure 19.5. Bottom Layer



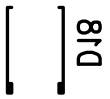


Figure 19.6. Bottom Silkscreen

20. Bill of Materials

The following table is the BOM listing for the Schottky external bridge option for PoE Class 2.

Table 20.1. Bill of Materials—Schottky External Bridge Option for PoE Class 2

Designator	Qty	Description	Manufacturer	Manufacturer PN
C1	1	CAP, 0.1 µF, 10 V, ±10%, X5R, 0805	Venkel	C0805X5R100-104KNE
C11, C12, C13, C14	4	CAP, 0.01 µF, 100 V, ±10%, X7R, 0805	Venkel	C0805X7R101-103K
C15, C16, C29, C30	4	CAP, 1 nF, 2000 V, ±5%, X7R, 1206	Kemet	C1206C102JGRACTU
C17	1	CAP, 2.2 nF, 50 V, ±10%, C0G, 0805	Venkel	C0805C0G500-222K
C18	1	CAP, 1 nF, 50 V, ±1%, C0G, 0805	Venkel	C0805C0G500-102F
C19, C22	2	CAP, 470 pF, 50 V, ±10%, X7R, 0805	Venkel	C0805X7R500-471K
C2, C23	2	CAP, 0.1 µF, 100 V, ±10%, X7R, 0805	Venkel	C0805X7R101-104K
C20, C24, C25, C26	4	CAP, 100 µF, 6.3 V, ±10%, X5R, 1210	Venkel	C1210X5R6R3-107K
C27, C28	2	CAP, 0.047 µF, 16 V, ±1%, C0G, 0805	KEMET	C0805C473F4GAC7800
C3	1	CAP, 2.2 µF, 25 V, ±20%, X7R, 0805	Venkel	C0805X7R250-225M
C31	1	CAP, 22 µF, 6.3V, ±20%, X5R, 0805	Venkel	C0805X5R6R3-226M
C32	1	CAP, 0.47 µF, 100 V, ±10%, X7R, 0805	Venkel	C0805X7R101-474KNE
C4	1	CAP, 1 µF, 16 V, ±10%, X5R, 0805	Murata	GRM21BR61C105KA01L
C5	1	CAP, 33 nF, 50 V, ±10%, X7R, 0805	Venkel	C0805X7R500-333KNE
C7	1	CAP, 0.22 µF, 16 V, ±10%, X7R, 0805	Venkel	C0805X7R160-224KNE
C8	1	CAP, 12 µF, 100 V, ±20%, AL, 6.3X11.2MM	Panasonic	EEUFC2A120
C9, C10	2	CAP, 1 µF, 100 V, ±10%, X7R, 1210	Venkel	C1210X7R101-105K
D1, D12, D13, D14, D15	5	DIO, SINGLE, 100 V, 300 mA, SOD123	DiodesInc.	1N4148W-7-F
D16	1	DIO, SINGLE, 100 V, 1.0 A, SMA	Fairchild	RS1B
D18	1	DIO, TVS,UNIDIR, 58 V, 400 W	Littelfuse	SMAJ58A
D2	1	LED, GREEN, 0805	LITE_ON INC	LTST-C170GKT
D4, D11, D17	9	DIO, SINGLE, 100 V, 2.0 A, SMB	Taiwan Semi	SS210
FB5, FB6, FB7, FB8	4	FERRITEBEAD, 1500 Ohm @100 MHZ, 0805	Wurth	742792097
J1, J2	2	CONN, RJ-45, 8P, SIDE ENTRY, PTH	TE Connectivity	5520252-4
J3, J4, J5	3	CONN, BANANA JACK, Threaded uninsulated	ABBATRON HH	101
Q1, Q3	2	TRANSISTOR, MOSFET, N-CHNL, 30 V, 6.5 A, SOT23	Fairchild	FDN537N
Q2, Q4	2	TRANSISTOR, PNP, 40 V, 200 mA, SOT23	DiodesInc.	MMBT3906-7-F
Q5	1	TRANSISTOR, MOSFET, NFET, 100 V, 2.6 A, TSOT26	DiodesInc.	DMN10H170SVTQ
R1	1	RES, 24.9 kΩ, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-2492FT
R11, R45, R48	5	RES, 0 Ω, 2 A, ThickFilm, 0805	Venkel	CR0805-10W-000

Designator	Qty	Description	Manufacturer	Manufacturer PN
R12	1	RES, 14.7 kΩ, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-1472F
R13	1	RES, 24.3 kΩ, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-2432F
R14, R17, R18	3	RES, 10 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-1002F
R2	1	RES, 88.7 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Vishay	CRCW080588K7FKEA
R27, R28, R30, R31, R44	5	RES, 3 Ω, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-3R00FT
R29, R32, R43	3	RES, 4.7 kΩ, 1/8 W, ±5%, ThickFilm, 0805	Venkel	CR0805-8W-472J
R3, R19, R26	9	RES, 75 Ω, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-75R0F
R33	1	RES, 47 kΩ, 1/10 W, ±5%, ThickFilm, 0805	Venkel	CR0805-10W-473J
R38	1	RES, 27 Ω, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-27R0F
R39	1	RES, 750 Ω, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-7500FT
R4	1	RES, 20.0 Ω, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-20R0F
R40	1	RES, 10 kΩ, 1/4 W, ±5%, ThickFilm, 1206	Venkel	CR1206-4W-103J
R41	1	RES, 56.2 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-5622FT
R42	1	RES, 220 kΩ, 1/8 W, ±1%, ThickFilm, 0805	Venkel	CR0805-8W-2203FT
R5, R6, R10, R15, R16	5	RES, 1 kΩ, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-1001F
R7	1	RES, 0.68 Ω, 1/2 W, ±1%, ThickFilm, 1206	Vishay	RCWE1206R680FKEA
R9	1	RES, 4.99 kΩ, 1/10 W, ±1%, ThickFilm, 0805	Venkel	CR0805-10W-4991F
S1, S2	2	SWITCH, PB, NO, MOMENTARY, TACTILE	PANASONIC CORP	EVQ-PAD04M
SW1	1	SWITCH, SPDT, SLIDE, ON-ON, 0.1 PITCH, 12 V, PTH	Apem Inc.	NK236H
T1	1	Module, PoE+/PoE++ Magnetics, PULSE XFMR	Wurth	7490220121
T2	1	TRANSFORMER, Flyback, 15 W, SMT	Mentech	TOEP13-0284SG
TP3, TP16	14	TESTPOINT, BLACK, 0.050" LOOP, PTH	Keystone	5001
U1	1	IC, IEEE 802.3-Compliant POE+ PD Interface, QFN24	SiLabs	Si34062-A-GM
U3	1	IC, ADJ PREC SHUNT REG LV SOT-23	TI	TLV431BCDBZR
U4, U5, U6,U7	4	PHOTOCOUPLER, 5300 Vrms Isolation, 4-PIN SMD	Vishay	VO618A-3X017T
Not Installed Components				
C6	1	CAP, 15 nF, 16 V, ±10%, X7R, 0805	Venkel	C0805X7R160-153K
R34, R35, R36, R37	4	RES, 0 Ω, 2 A, ThickFilm, 0805	Venkel	CR0805-10W-000
FB1, FB2, FB3, FB4	4	FERRITE BEAD, 1500 Ω @100 MHZ, 0805	Wurth	742792097
C33, C34, C35	3	CAP, 1 nF, 2000 V, ±5%, X7R, 1206	Kemet	C1206C102JGRACTU
J7	1	CONN, POWERJACK, RA, 2.1 mm, PTH	Adam Tech	ADC-002-1

21. Design and Layout Checklist

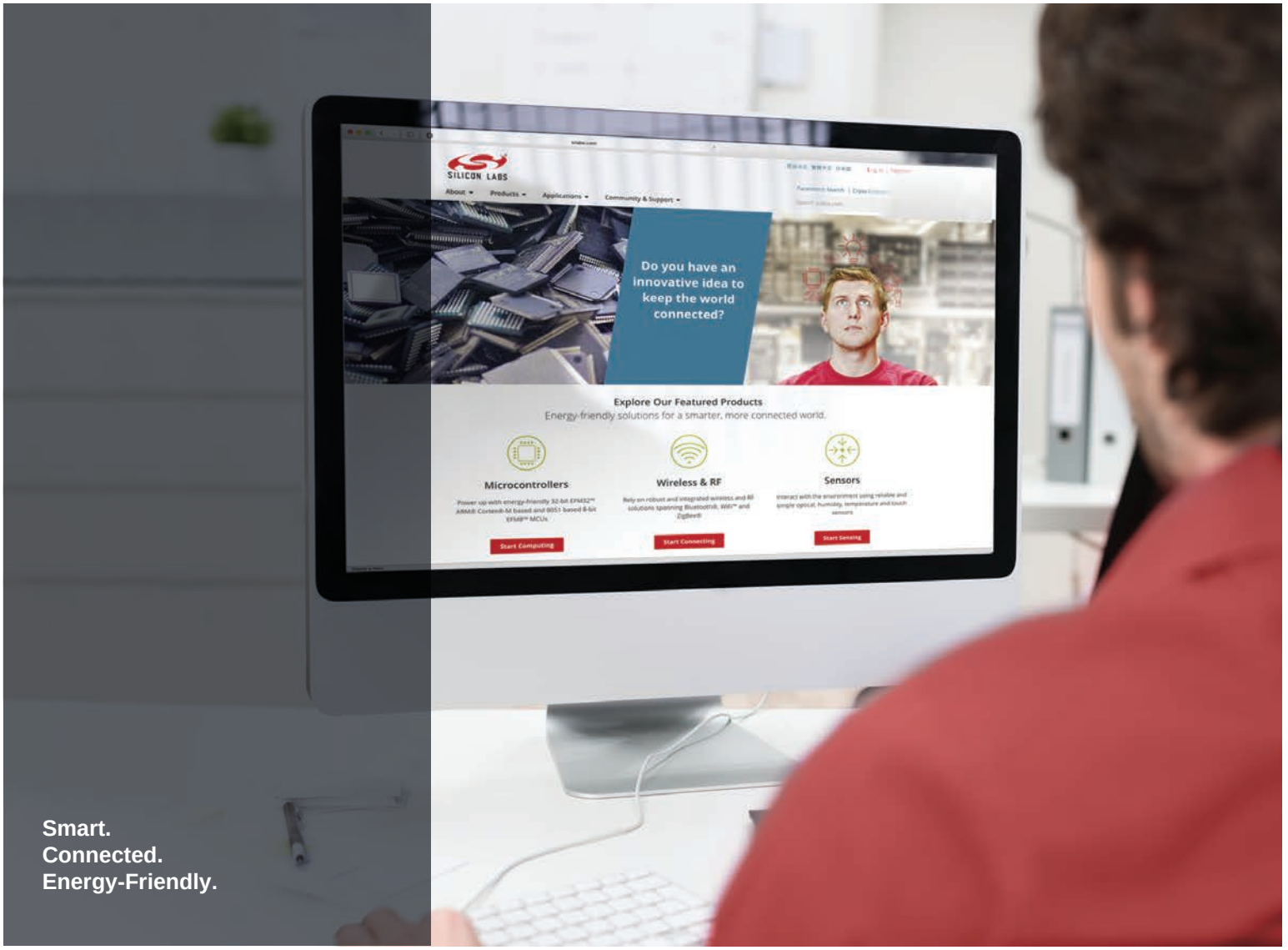
The complete EVB design databases are located at www.silabs.com/PoE. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Below is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si34062 data sheet and AN1130 when using the following checklist.

1. Design Planning Checklist:
   a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
   b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si34062-ISO-FB-EVB into your system design process.
   c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions).
   d. Based on your required PD power level, select the appropriate class resistor RCLASS value by referring to AN1130
2. General Design Checklist:
   a. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a 3Ω resistors inplace of R44.
3. Layout Guidelines:
   a. Makesure VNEG pin of the Si34062 is connected to the backside of the QFN package with an **adequate thermal plane**.
   b. Keep the trace length from SWO to VSS as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
   c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
   d. Keep the circular area of the loop from the internal FET (SWO) output to the transformer and returning from the input filter capacitors (C8, C9, C10) to VSS as small a diameter as possible. Also, minimize the circular area of the loop from the output of the transformer to the sync-FETs (Q1 and Q3) and returning through the output filter capacitor back to the transformer as small as possible. If possible, keep the direction of current flow in these two loops the same.
   e. Keep the high-power traces as short as possible.
   f. Keep the feedback and loop stability components as far from the transformer and noisy power traces as possible.
   g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.



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