Si55xx, Si540x, and Si536x Recommended XTAL, XO, VCXO, TCXO, and OCXO Reference Manual

Description

The purpose of this document is to provide a list of Crystals (XTALs), Crystal Oscillators (XOs), Voltage Controlled Crystal Oscillators (VCXOs), Temperature Compensated Crystal Oscillators (TCXOs), and Oven Controlled Crystal Oscillators (OCXOs), that are recommended for use with Skyworks high-performance network synchronizers, jitter attenuators and clock generators that utilize fifth-generation DSPLL™ and MultiSynth™ technologies.

In this document, the Si5508/10/12/18 RF jitter attenuators and network synchronizers will be referred to as the Si55xx product family, the Si5401/02/03 network synchronizers will be referred to as the Si540x product family, and the Si5360/61/62/63 clock generators and jitter attenuators will be referred to as the Si536x product family. The recommended references and reference frequencies for each product family are selected to give best performance in their intended applications.

Customers should qualify any reference device using their own internal standards and monitor specification compliance and quality of these devices over time. In circuit evaluation, it is recommended to verify that the reference meets all application requirements.

See relevant device data sheets and reference manuals for external reference termination and layout recommendations. This document is purely intended to guide the selection of the reference oscillators that are paired with the Si55xx/Si540x/Si536x chip sets.

Related Documents

- Si55xx Reference Manual
- Si540x Reference Manual
- Si536x Reference Manuals
- Schematic Design and Layout Guidelines
  - AN1293: Si55xx
  - AN1347: Si540x
  - AN1357: Si536x

Related Skyworks Parts

- Si5512/18 RF Jitter Attenuator + NetSync™ wireline network synchronizer clocks
- Si5510/08 RF Jitter Attenuators
- Si5401/02/03 NetSync™ Wireline Network Synchronizer Clocks
- Si5361/62/63 Jitter Attenuators
- Si5360 Clock Generator

March 7, 2024

1. Phase Noise References (XTALs, XOs, VCXOs)

Si55xx/Si540x/Si536x devices use an external quartz-based oscillator in conjunction with a high performance on-chip voltage controlled oscillator (VCO) to generate ultra-low jitter and phase noise output clocks. **This oscillator is referred to as the phase noise reference and is required for all applications using the Si55xx/Si540x/Si536x devices**. It is critical to select the proper phase noise reference for the given device and application to optimize board design for both performance and cost. It is highly recommended to use one of the qualified phase noise references from this document as they will result in phase noise performance in line with the data sheet.

The Si540x wireline network synchronizers and the Si536x jitter attenuators/clock generators support either an XO or a XTAL as the phase noise reference. The output clock jitter will be roughly equivalent between any device from the recommended list of XOs or XTALs.

The Si55xx wireless jitter attenuators/network synchronizers support a crystal oscillator (XO), crystal (XTAL), or voltage-controlled crystal oscillator (VCXO) as the phase noise reference. **An XO is recommended for most Si55xx wireless applications**. This is due to the fact that an XO will provide the lowest close-in phase noise (10 Hz to 1 kHz). For wireless applications that are not as sensitive to close-in phase noise either an XO or a XTAL can be used as the phase noise reference. The phase noise above a few kHz and integrated 12 kHz to 20 MHz jitter will be roughly equivalent when using any of the approved XOs/XTALs.

The Si55xx products are the only devices that support a VCXO phase noise reference. **The VCXO phase noise reference is recommended for the Si55xx devices when used in the highest performance 5G wireless applications such as mm wave and massive MIMO**. It is extremely important to select an ultra-low phase noise VCXO with a low tuning gain (kV) like the ones recommended in this document. A mid-tier VCXO will likely result in higher phase noise outputs clocks and a more expensive BOM cost than using one of the recommended XOs. See the data sheet for phase noise comparisons between XO and VCXO modes.

Table 1 provides a summary of the supported phase noise references for each product family.

Table 1. Recommended Phase Noise References

Si5xxx Device	Supported PN References	Applications
Si5508/10/18	XO, XTAL, VCXO	Wireless RU, Small Cell, Integrated Small Cell, DAS.
Si5512	XO, XTAL	Wireless RU, Small Cell, Integrated Small Cell, DAS, designs that split digital and RF functions on separate board.
Si5401/02/03	XO, XTAL	Core/metro/access switch and routers, Wireless CU, DU and front-haul switch, smart NIC.
Si5361/62/63	XO, XTAL	56G/112G SerDes clocking, OTN muxponders/transponders, switches and routers, medical imaging, test and measurement.
Si5360	XO, XTAL	FPGAs/processors/memory, switches and routers, OTN framers/mappers/processors, test equipment and instrumentation, broad- cast video.

1.1. Recommended Crystals (XTALs)

A crystal (XTAL) refers to a quartz crystal, which has the piezoelectric property that it vibrates at a fixed frequency when an electric field is applied. The XTAL is driven by an on-chip circuit to form a crystal oscillator, which uses the mechanical resonance of the vibrating crystal to yield a fixed frequency electrical oscillation. This provides an ultra-low jitter oscillator input to the Si55xx/Si540x/Si536x device that is used as the phase noise reference for the phase locked loop (PLL). The allowed frequency range for the XTAL is 48 to 54 MHz. Figure 1 shows the crystal reference connected to the XA/XB pins of the device.
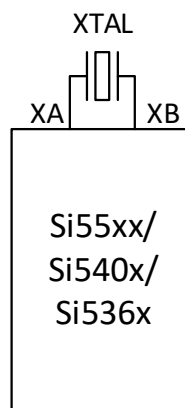
Figure 1. Si55xx/Si540x/Si536x Clock with XTAL Phase Noise Reference on XA/XB

Table 2 on page 4 lists the XTALs that are recommended for use as the phase noise reference on the XA/XB pins of Si55xx/Si540x/Si536x devices. While it is encouraged to use one of the recommended XTALs, which have been tested and qualified, other XTALs may be used. See " Appendix A—Selecting an XTAL for Your Application" on page 13, in particular the ESR vs C0 requirement, will be guaranteed to oscillate.

XTALs that meet the specifications outlined in this document may be submitted to Skyworks for future qualification consideration for   use with the clocks listed above. Some of the part numbers in this table are custom generated for Skyworks. Part Family information is included in the table to enable searching through vendor websites. Users can also contact the vendor directly and ask for the specific part number listed.
The oscillation frequency vs temperature curve of the XTALS specified will have a shape of an S-curve. However, there can be small deviations from the S-curve primarily due to imperfect internal connections to the actual physical XTAL blank. These deviations are called Frequency Perturbations. In some applications, it is important that the Frequency Perturbation be limited to a maximum value. Some XTALS specify a maximum for Frequency Perturbations and others do not. It is recommended that an XTAL have a max Frequency Perturbations spec of no more than 2 ppm/2 °C. This means that over a 2 °C temperature range that the XTAL frequency will not change by more than 2 ppm from the normal S-curve shape.

Note: The figures in this document are meant to be high level. For example, design details like the XTAL ground shield (XV) are not shown in Figure 1. See the appropriate product reference manual and Si55xx/Si540x/Si536x Schematic Design and Layout Guidelines application notes for more detailed XTAL connections and layout recommendations.

Table 2. Recommended Crystals, XTALs

Supplier	Part Number	Freq (MHz)	Initial Tolerance (±ppm)	Operating Temp (C)	Freq Error over Operating Temp Range (±ppm)	C0 Max (pF)	ESR Max (ohms)	CL (pF)	Pull-ability max[1] (ppm/pf)	Qmin	Activity Dip Guaranteed 2ppm/C Max?	Drive Level Max (µW)	Package Size (mm)
TXC[2]	7M48072009	48	10	−40 to 105	20	2.0	22	8.0	35	30k	Yes	200	3.2 x 2.5
TXC[2]	7M50072003	50	10	−40 to 85	15	2.0	22	8.0	35	30k	Yes	200	3.2 x 2.5
TXC[2]	7M54072006	54	10	−40 to 105	20	2.0	22	8.0	35	30k	Yes	200	3.2 x 2.5
Kyocera[3]	CX3225SB48000 D0FRRC1	48	10	−40 to 105	40	2.0	25	8.0	35	—	Yes	200	3.2 x 2.5
Kyocera[3]	CX3225SB54000 D0FRRC1	54	10	−40 to 105	40	2.0	25	8.0	35	—	Yes	200	3.2 x 2.5
Taitien	S0242-X-004-3	48	15	−40 to 105	35	2.0	25	8.0	35	30k	Yes	200	3.2 x 2.5
Taitien	S0242-X-005-3	54	10	−40 to 105	45	2.0	30[4]	8.0	35	30k	Yes	200	3.2 x 2.5

1. Pull-ability is the change in oscillation frequency when CL is not exactly 8 pF.
2. TXC contact information: www.txccorp.com, USA office phone number 714-990-5510.
3. Kyocera part search page: https://global.kyocera.com/prdct/electro/
4. To be updated by the vendor.

1.2. Recommended Crystal Oscillators (XOs)

Some applications, in particular RF/wireless clocking (Si55xx), are sensitive to close-in phase noise. For these applications, a crystal oscillator (XO) is recommended as the phase noise reference. Some customers also tend to use an XO instead of a XTAL, for its superior reliability and performance over temperature. The recommended frequency range for the XO is 48 to 54 MHz, for best performance. However, as specified in the device data sheet, a wider range of XO frequencies is supported.

Compared to a discrete XTAL, an XO will have less total frequency error when taking into account all factors. Using an XO instead of a XTAL will produce the following:

- Output clocks with lower phase noise for offsets less than 1 kHz.
- Greater immunity to vibration and airflow effects. This may result in lower phase noise below ~50 Hz.
- Better temperature stability with the frequency changes of an XO being less than that of a XTAL. Because of this, a jitter attenuator device can have a lower bandwidth and still filter out these oscillation frequency changes.
- Better accuracy in free-run since the accuracy of an XO is far better than that of a XTAL.

The jitter of the XO applied to the Si55xx/Si540x/Si536x device has a large effect on the output jitter/phase noise for offset frequencies up to ~1.5 MHz. The following figure shows the XO phase noise reference connected to the clock. Note the distinction that XOs should be connected to the REF_IN pins for Si55xx devices and the XO_IN for Si540x/Si536x devices whereas XTALs are always connected to the XA/XB pins. The REF_IN/XO_IN can support a DC coupled single-ended CMOS XO input or an AC coupled differential XO input to REF_IN/XO_IN and REF_INB/XO_INB. In general, single ended CMOS XO inputs are far more common for the recommended XO frequency range as they can achieve lower phase noise floor with respect to differential XOs.
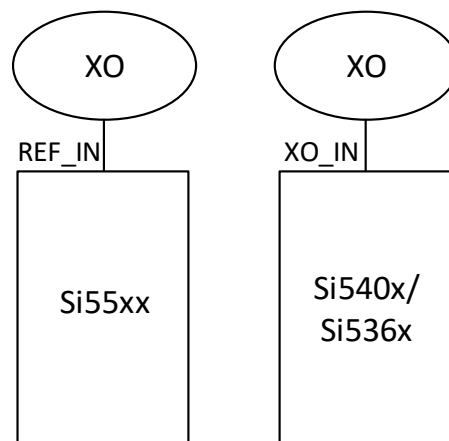
Figure 2. Si55xx/Si540x/Si536x Clocks with XO Phase Noise Reference on REF_IN Input

The figures in this document are meant to be high level. See the appropriate product reference manual and Si55xx/Si540x/Si536x Schematic Design and Layout Guidelines Application Note for XO input connections and specification limits, rise/fall times, input circuits, input level specifications, and performance trade-offs. Also, see the design/layout guideline application notes for how to power XOs.

Table 3 on page 6 lists the XOs that are recommended for use as the phase noise reference of the Si55xx/Si530x/Si536x devices. To deliver optimum performance, either these recommended XOs or one of equivalent phase noise and jitter performance must be selected.

Note: Some of the part numbers in Table 3 are custom generated for Skyworks. Part family information is included in the table to enable searching through vendor websites. Users may also contact the vendor directly and ask for the specific part number listed.

Table 3. Recommended XO Phase Noise References

Supplier	Part Number	Part Family	Freq (MHz)	Temp °C	Total Frequency Stability (±ppm)[1]	Supply Voltage[2]	Package Size (mm)
NDK	NZ2520SDA-48M- CUS5242A[3]	NZ2520SDA	48	−40 to 105	50	3.3 V	2.5 x 2.0
TXC	7X48070007[3]	7X	48	−40 to 105	50	3.3 V	3.2 x 2.5
TXC	8W48070009[3]	8W	48	−40 to 85	25	3.3 V, 1.8 V	2.5 x 2.0
TXC	8W50070006[3]	8W	50	−40 to 105	50	3.3 V	2.5 x 2.0
NDK	NZ2520SDA-54M- CUS5094C[3,4]	NZ2520SDA	54	−40 to 105	50	3.3 V	2.5 x 2.0
TXC	7X54070001[3,4]	7X	54	−40 to 105	50	3.3 V	3.2 x 2.5
TXC	7X54070002[3,4]	7X	54	−40 to 105	50	1.8 V	3.2 x 2.5
TXC	8W54070002[3,4]	8W	54	−40 to 105	50	3.3 V	2.5 x 2.0
TXC	8W54070004[3,4]	8W	54	−40 to 85	25	3.3 V, 1.8 V	2.5 x 2.0

1. Includes initial accuracy, temperature, aging, and soldering effects.
2. 1.8 V supply voltage should only be used for low-power mode applications in which VDDRED = VDDA = 1.8 V.
3. Recommended for use on Si540x (Si5401/02/03) and Si536x (Si5360/61/62/63) devices.
4. Recommended for use on Si55xx (Si5508/10/12/18) devices.

Skyworks Solutions, Inc. • Phone [949] 231-3000 • sales@skyworksinc.com • www.skyworksinc.com
206422C • Skyworks Proprietary Information • Products and Product Information are Subject to Change without Notice
6   March 7, 2024

1.3. Recommended Voltage-Controlled Oscillators (VCXOs)

The Si5508/10/18 devices support a voltage-controlled crystal oscillator (VCXO) phase noise reference. The Si5512 is the only device in the Si55xx product family that does not support a VCXO phase noise reference. Although for most wireless 5G applications the Si55xx + XO phase noise reference is sufficient, in some high-end RF applications, such as mmWave and massive MIMO, a VCXO may be advantageous due to the slightly lower mid-band phase noise and RMS jitter. The recommended VCXOs, as shown in Table 4, have an ultra-low phase noise floor along with a low tuning gain (kV), which is critical for achieving low close-in phase noise with a VCXO often required for wireless applications. It is extremely critical to use a VCXO from Table 4 or one of equal performance. **If a customer selects a VCXO that is not on the recommended lists in this document, the Si55xx output phase noise will likely be WORSE than using a recommended XO**. A mid-tier VCXO will likely result in higher phase noise outputs clocks and a more expensive BOM cost than using one of the recommended XOs. See the Si55xx data sheets for phase noise comparisons between XO and VCXO modes.

One key distinction between an XO/XTAL and a VCXO phase noise reference is that the VCXO frequency is steered by the voltage control (VC) output from the on-chip high resolution DAC compared to a free-running XTAL/XO phase noise reference in which the PLL output frequency is steered internally by an on-chip high resolution digital divider. Because the VCXO frequency matches the desired output frequency, VCXO buffer mode outputs are supported. The buffered copy of the VCXO can provide the lowest midband phase noise output clock (1k to 1M) to meet the most stringent phase noise masks for output clocks, providing synchronization to radio equipment such as an RF LO, phased-array antenna or high performance ADC/DAC.

The Si5508/10/18 devices support both DC coupled single ended CMOS and AC coupled differential VCXOs. It is recommended to use a VCXO with a frequency greater than or equal to 122.88 MHz. The desired high-performance RF clock output frequency should be integer related to the VCXO frequency.
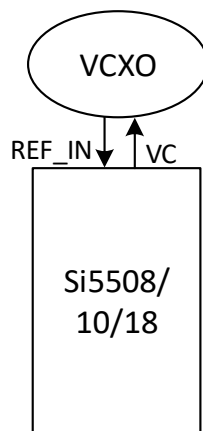

Figure 3. Si5508/10/18 Clock with VCXO Phase Noise Reference on REF_IN Input

The figures in this document are meant to be high level. See the appropriate Product reference manual for input connections and terminations.

Table 4. Recommended VCXO Phase Noise References for Si5508/10/18 Devices[1]

Supplier	Part Number	Part Family	Freq (MHz)	Temp °C	Package Size (mm)	Absolute Pull Range, APR (±ppm)
Rakon	V4104[2]	RVX1490U	122.88	−40 to 85	9 x 14	5
Rakon	V4185	RVX1490U	122.88	−40 to 95	9 x 14	10
Rakon	V4173	RVX1490U	153.6	−40 to 85	9 x 14	5
TXC	DRA5370001		153.6	−40 to 85	3.2 x 5	5
Epson	CJGHMA	VG3225EFN	204.8	−40 to 85	3.2 x 2.5	20
TXC	CJB0470001		204.8	−40 to 85	3.2 x 5	50
Epson	CJGHSA	VG332EFN	491.52	−40 to 85	3.2 x 2.5	10

1. Includes initial calibration, temperature range, aging, soldering effects, and supply-and-load variation.
2. V4104 is not recommended for new designs. Use V4185 for new designs.

2. Stability and Holdover References (TCXOs/OCXOs)

Network synchronization applications, such as IEEE-1588 and Synchronous Ethernet ITU-T G.8262/G.8262.1 (SyncE), require low wander in addition to the traditional low jitter/phase noise requirement. A compensated crystal oscillator such as a TCXO or OCXO is required to provide stability to support the low bandwidths specified for SyncE PLLs (0.1 to 10 Hz BW) and/or IEEE-1588 servo loops (1 to 100 mHz BW). For SyncE and/or full timing support (FTS) applications as described in ITU-T G.8275.1 a TCXO is recommended. For applications that require PLL or servo loop bandwidths less than 100 mHz or for applications that require SyncE and/or time holdover an OCXO is recommended. This includes 1PPS (Pulse Per Second)/PP2S (Pulse Per 2 Seconds) PLLs, which are commonly required to lock to GNSS receivers for partial/assisted partial timing support (PTS/APTS) applications as described in ITU-T G.8275.2. See Sections 2.1 and 2.2 for more details on selecting the right quality oscillator for a given application.

The Si540x and Si5512/18 network synchronizer devices support these applications using two reference oscillators in dual reference mode. In this mode, the phase noise reference is applied to the device in the same manner as described in Section 1 (for example to the XA/XB pins when using a XTAL) along with a second TCXO/OCXO reference for stability and optional holdover. The TCXO/OCXO is applied to the input pins (INx) in the case of the Si5512/18 and the dedicated REF pin in the case of the Si540x. The Si540x require dual reference mode while the Si5512/18 can support either dual or single reference modes configurable in ClockBuilder Pro. The Si536x and Si5508/10 do not support dual reference mode.

Note: See the applicable Skyworks product Reference Manual for rise/fall time, input circuits, input level specifications and performance trade offs.
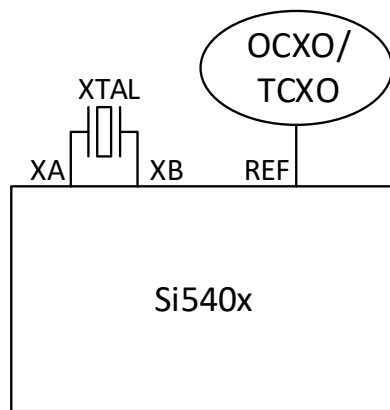

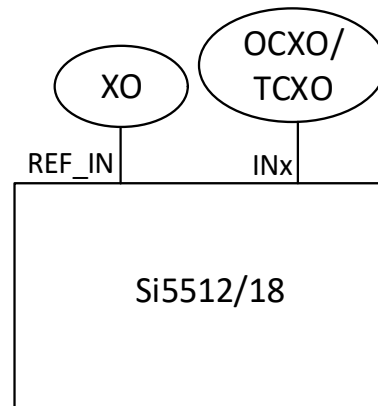**Figure 4. Si540x Network Synchronizer with OCXO/TCXO and XTAL Reference**

Figure 5. Si5512/18 RF JA + Network Synchronizer with OCXO/TCXO and XO Reference

2.1. TCXOs

A TCXO is recommended for network synchronization applications supporting SyncE and when used in a full timing support network (FTS) as described in ITU-T G.8275.1. An FTS network is engineered such that every node in the network supports IEEE-1588. This results in a nearly ideal case for low Ethernet packet delay variation (PDV) throughout the network and allows for a wider servo loop bandwidth of 50 to 100 MHz. The timing characteristics and transfer functions between SyncE and IEEE-1588 input/outputs are outlined in ITU-T G.8273.2, which defines a Telecom Boundary Clock (T-BC) or Telecom Slave Clock (T-TSC) for an FTS network. **Relying on SyncE stabilization allows the designer to select a lower cost TCXO. In the absence of SyncE or if time holdover is required, an OCXO is recommended as described in Section 2.2**.

Table 5 lists the TCXOs that have been tested and approved for use with the Si5512/18 and Si540x network synchronizer devices for ITU-T G.8262 EEC Options 1 and 2 (SyncE) and ITU-T eEEC G.8262.1 (Enhanced SyncE) and T-BC/T-TSC G.8273.2 applications. Contact Skyworks support for SyncE, Enhanced SyncE, and G.8273.2 compliance reports. All recommended TCXOs are required to be Stratum 3 level of performance.

Note: Some of the part numbers in this table are custom-generated for Skyworks. Part family information is included in the table to enable searching through vendor web sites. Users can also contact vendors directly and ask for specific listed part numbers.

Table 5. Recommended TCXO Approved For SyncE and T-BC/T-TSC Applications

Supplier	Part Number[1]	Part Family	Freq (MHz)[2]	Stability Over Temp (±ppb)	Temp °C	Stratum	Package Size (mm)
Rakon	E8268LF	RNT7050A	10	50	–40 to 85	3	7 x 5
Rakon	N8948	RNT7050A	10	140	–40 to 95	3	7 x 5
TXC	7N10071003	7N	10	250	–40 to 105	3	7 x 5
TXC	7N10070005	7N	10	140	–40 to 85	3	7 x 5
Rakon	E6413LF	RPT7050J	12.8	140	–40 to 85	3	7 x 5
Rakon	N8900	RTN7050A	19.44	100	–40 to 85	3	7 x 5
TXC	7N19471003	7N	19.44	250	–40 to 105	3	7 x 5
TXC	7N19471005	7N	19.44	140	–40 to 85	3	7 x 5
TXC	7P19472002	7P	19.44	250	–40 to 105	3	5 x 3.2
Rakon	N8998	RTN7050A	20	100	–40 to 85	3	7 x 5
TXC	7N20070004	7N	20	250	–40 to 105	3	7 x 5
TXC	7N20071005	7N	20	140	–40 to 85	3	7 x 5
Rakon	N8903	RTN7050A	38.88	100	–40 to 85	3	7 x 5
TXC	7N38871002	7N	38.88	250	–40 to 85	3	7 x 5
TXC	7N38871003	7N	38.88	140	–40 to 85	3	7 x 5
TXC	7P38872001	7P	38.88	250	–40 to 105	3	5 x 3.2
Rakon	N8997	RTN7050A	48	100	–40 to 85	3	7 x 5
TXC	7N48071001	7N	48	250	–40 to 105	3	7 x 5
TXC	7N48071005	7N	48	140	–40 to 85	3	7 x 5

1. All listed part numbers are recommended for use on Si5512/18 and Si5401/02/03 devices.
2. TCXO frequencies of 10*N MHz should be avoided for applications in which a 10 MHz input will be applied to the Si5xxx network synchronizer as they may cause coupling. Avoid this TCXO frequency for applications which have a 10 MHz input from a GNSS receiver.

2.2. OCXOs

An OCXO is recommended for network synchronization applications that do not support SyncE, require time holdover and/or when used in partial/assisted partial timing support (PTS/APTS) network as described in ITU-T G.8275.2. A PTS network is defined as a network that does not support IEEE-1588 at every node. APTS is a technique of deploying Global Navigation Satellite Systems (GNSS) receivers throughout a PTS network to serve as the primary source of timing for all downstream nodes. In APTS when GNSS becomes unavailable, the IEEE-1588 protocol is used to maintain synchronization. The timing characteristics for a PTS network are outlined in ITU-T G.8273.4 which defines a T-BC-P and T-TSC-P for partial timing support and a T-BC-A and T-TSC-A for assisted partial timing support.

Since a PTS network has nodes that do not support IEEE-1588, the Ethernet packets transmitted throughout the network experience significantly more packet delay variation (PDV). To support the PTS profile, typically a lower servo loop bandwidth (1 mHz or less) must be used to filter out the PDV. In addition to more PDV, many PTS networks do not support SyncE so the output clock stability and wander tracks the oscillator all the way down to the low servo loop bandwidth. A TCXO will likely not provide low enough wander to support PTS and an OCXO is strongly recommended.

Table 6 on page 12 lists the OCXOs recommended for use with the Si5512/18 and Si540x network synchronizer devices for
T-BC-A/T- TSC-A/T-BC-P/T-TSC-P G.8273.4, ITU-T G.8262 EEC Options 1 and 2, ITU-T eEEC G.8262.1, and T-BC/T-TSC G.8273.2 applications. Additionally approximate holdover times supported for each OCXO are provided. It is recommended to verify holdover times with the OCXO vendor as they will vary depending on parameters such as temperature variation for the given application. A Stratum 3E level OCXO or better should be used for all applications requiring time holdover.

Note: Some of the part numbers in Table 6 are custom generated for Skyworks. Part Family information is included in the table to enable searching through vendor web sites. Users can also contact the vendor directly and ask for specific listed part numbers.

Table 6. Recommended OCXOs for SyncE, Time Holdover, and T-BC-A/T-TSC-A, T-BC-P/T-TSC-P Applications

Supplier	Part Number[1]	Part Family	Freq (MHz)[2]	Temp (°C)	Stability Over Temp (±ppb)	Stratum Level	ADEV @ Tau = 1s (ppt)	Package Size (mm)	Approx. Holdover Time Supported (hours)[3]
Rakon	STP3541LF[4]	ROX2522S3	10	−40 to 85	1	3E	5	25.4 x 22	4 to 8
Rakon	STP3703LF[4]	ROD2522S2H	10	−40 to 85	2	3E	5	25.4 x 22	24
Rakon	U8323LF[4]	RTH7050PA	10	−40 to 85	20	3	20	7.5 x 5.5	0 to 0.5
Rakon	U9006LF	ROM1490X	10	−40 to 95	3	3E	20	14.2 x 19.2	4 to 8
TXC	OG10070001[4]	OG	10	−40 to 95	20	3	20	9.5 x 7.3	0.5 to 1
Rakon	STP3158LF	ROX2522S4	12.8	−40 to 85	10	3E	5	25.4 x 22	1 to 4
CTS	1498010-19M440[4]	Model 149	19.44	−40 to 85	10	3E	50	14.9 x 9.7	2 to 4
Rakon	STP3609LF[4]	ROX2522S3	19.44	−40 to 85	5	3E	5	25.4 x 22	4 to 8
Rakon	U8565LF	RTH7050PA	19.44	−40 to 85	20	3	20	7.5 x 5.5	0 to 0.5
Rakon	U8567LF[4,5]	ROM1490E	19.44	−40 to 85	5	3E	20	14.2 x 9.2	2 to 4
TXC	OG19470001[4]	OG	19.44	−40 to 85	20	3	20	9.5 x 7.3	0.5 to 1
TXC	OH19470002[4,5]	OH	19.44	−40 to 95	50	3	20	7 x 5	0 to 0.5
TXC	OK19470002[4,5]	OK	19.44	−40 to 95	50	3	20	5.5 x 3.7	0 to 0.5
TXC	OG20070003[4]	OG	20	−40 to 85	20	3	20	9.5 x 7.3	0.5 to 1
NDK	ENA5930[4]	NH7050SA	38.88	−40 to 95	50	3	40	7 x 5	0 to 0.5
Rakon	STP3608LF[4]	ROX2522S3	38.88	−40 to 85	3	3E	5	25.4 x 22	4 to 8
Rakon	U8050LF[4]	ROM9070PA	38.88	−40 to 85	20	3	20	9.7 x 7.5	0 to 0.5
Rakon	U8429LF[4]	RTH7050PA	38.88	−40 to 85	20	3	20	7.5 x 5.5	0 to 0.5
Rakon	U8568LF[4]	ROM1490E	38.88	−40 to 85	5	3E	20	14.2 x 9.2	2 to 4
Rakon	U8868LF[4]	ROM1490X	38.88	−40 to 95	3	3E	20	14.2 x 9.2	4 to 8
TXC	OG38870003[4,5]	OG	38.88	−40 to 85	10	3	20	9.8 x 7.6	0.5 to 1
TXC	OH38870003[4]	OH	38.88	−40 to 95	50	3	20	7 x 5	0 to 0.5
TXC	OK38870001[4]	OK	38.88	−40 to 85	50	3	20	5.5 x 3.7	0 to 0.5
Rakon	U7958LF[4]	ROM9070PA	48	−40 to 85	20	3	20	9.7 x 7.5	0 to 0.5
TXC	OG48070001[4]	OG	48	−40 to 85	20	3E	20	9.7 x 7.3	0.5 to 1

1. All listed parts are recommended for use on Si5401/02/03 devices.
2. OCXO frequencies of 10 x N MHz should be avoided for applications in which a 10 MHz input from will be applied to the Si5xxx network synchronizer as they may cause coupling. Avoid this OCXO frequency for applications which have a 10 MHz input from a GNSS receiver.
3. The holdover times listed are approximates provided by the supplier. Skyworks does not test holdover. Contact the supplier for more detailed holdover questions and test reports.
4. Recommended for use on Si5512/18 devices.
5. Not yet tested by Skyworks but expected to be compliant based on vendor data sheet specifications.

Appendix A—Selecting an XTAL for Your Application

The purpose of this section is to enumerate the properties of the XTAL and how it affects the final performance. As mentioned above, XTALs operate by the piezoelectric effect. As a result, the electrical and the mechanical aspects of the XTAL have a role in determining its aptness for the given purpose.

Data Sheet Electrical Specifications

Frequency

An XTAL is designed to oscillate at a particular frequency as discussed in the section below. XTALs can operate at either the fundamental frequency or at overtones of the fundamental. However, the rest of this document is about fundamental crystals which are AT cut. AT cut refers to the way the crystal is physically cut to cause it to resonate when connected to an oscillator circuit.

Frequency Accuracy

The construction and manufacturing process determines the accuracy and performance of the XTAL. These factors can be analyzed in terms of the variation they cause from the ideal operating point of the XTAL.

Frequency error is a cumulative value which is a combination of multiple factors. This number needs to be within the limit specified by the Si55xx/Si540x/Si536x device to guarantee proper PLL operation and specified performance. Accuracy is represented in parts per million (ppm) or parts per billion (ppm).

$$ppm \ error = \left(\left(Actual \ frequency \ - \ ideal \ frequency\right) \ / \ ideal \ frequency\right) \ \times 10^6$$

$$ppb \ error = \left(\left(Actual \ frequency \ - \ ideal \ frequency\right) \ / \ ideal \ frequency\right) \ \times 10^9$$

Because the XTAL accuracy directly affects the output accuracy during free run, it is important that the XTAL frequency error be tight on the temperature drift and total ppm error. The factors contributing to frequency accuracy are.

1. **Initial offset or frequency tolerance**: Impurities in the XTAL growth, imprecision in the cutting process, and uneven thickness of the processed XTAL lead to slightly different nominal oscillation frequencies across a batch of XTALs. It is usually specified at a typical room temperature of 25 °C.

2. **Frequency stability over temperature**: The XTAL oscillation frequency varies with temperature. Data sheet specifications give the minimum and maximum variation above and below the oscillation frequency at 25 °C.

3. **Aging**: XTALs are electromechanical devices and are therefore subject to aging due to internal and external factors. Aging is typically higher during the first year of operation and slows down over time. For the Si55xx/Si540x/Si536x products, Skyworks specifies aging for 10 years at 50 °C. Most of the aging occurs in the first year.

4. **Pulling sensitivity or pull-ability**: The oscillation frequency of the XTAL depends on the load capacitance and will be affected by the tolerance of the loading capacitors. It is usually expressed in ppm/pF of capacitance variation.

5. **Effects of high-temperature reflow**: The reflow process subjects the XTAL to high temperature soldering followed by cooling. This may cause a small shift in the frequency, specified in ppm. This specification may also list how many reflows are accounted for in the measurement to account for re-work.

6. **Activity dips (frequency perturbation)**: Variations in the XTAL oscillation frequency from its S curve are called activity dips. One common reason for activity dips is imperfections in the mechanical contact of the bond wire to the XTAL blank. About 2% of XTALs will have activity dips of more than 2 ppm/C. In some cases it is important to buy XTALs that are tested to eliminate all activity dips of more than 2 ppm/C. However, many applications do not require the extra test.

The total frequency error is a sum of individual errors. For example, to understand how to calculate the total error, consider a scenario where a 48 MHz XTAL has a frequency tolerance of ±13 ppm, frequency stability of ±30 ppm over temperature, long term aging at 50 C of ± 10 ppm, pulling sensitivity of 30 ppm/pF, frequency perturbation of ±2 ppm, and a frequency drift after reflow of ±2ppm. Lastly, assuming a ± 0.5 pf total variation in the capacitance across the crystal pins, the total error from the XTAL is a sum of all these factors.

Total error = 13 + 30 + 10 + (0.5 *30) + 2 + 2 = 72 ppm

Operating Temperature

This is the temperature range that guarantees the operation of the XTAL per data sheet specifications. This temperature range should be wide enough to meet the expected system operating temperature range.

XTAL Equivalent Model

A quartz XTAL can be modeled electrically as a series RLC in parallel with a capacitance indicating the connections, as shown in Figure 6.
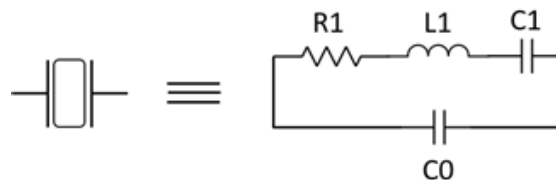
Figure 6. XTAL Symbol and its Equivalent Electrical Model

L1 (Motional Inductance), C1 (Motional Capacitance), C0 (Shunt Capacitance): L1, C1 and C0 along with the total capacitance across C0 (oscillator connections) determine the oscillation frequency of the XTAL.

ESR (Equivalent Series Resistance): The equivalent impedance of the XTAL at resonance is the Equivalent Series Resistance. It is mostly dominated by the resistive component R1 given that the ratio of C1/C0 is very small.

$$ESR = R_1$$

The ESR (R1) of the crystal must not be too high or else the on-chip oscillator will be unable to oscillate. The following plot shows the maximum ESR requirement of the oscillator circuit within the Si55xx for oscillation to be guaranteed. To ensure stable oscillation, the XTAL must have an ESR below the curve at the maximum C0 specified for that XTAL. Using a XTAL with a maximum ESR above this curve may not ensure stable oscillation over all conditions.
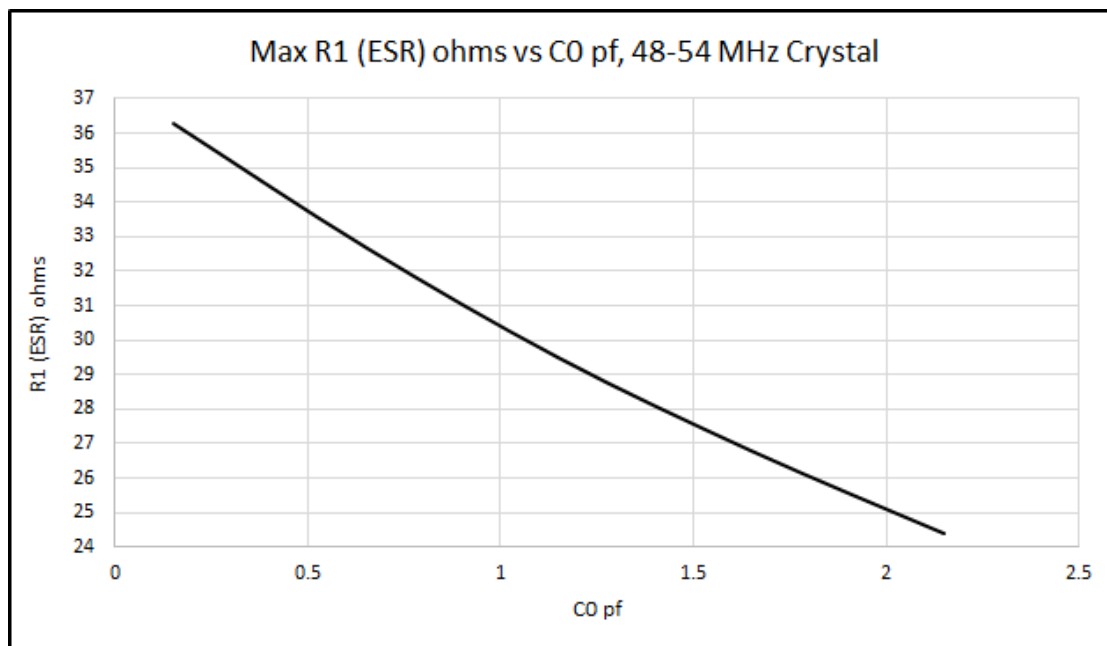
Figure 7. Maximum ESR vs Shunt Capacitance, C0 for 48 to 54 MHz XTAL

The XTAL oscillator in the Si55xx/Si540x/Si536x device provides a parallel load capacitance to the XTAL of 8 pf which includes the estimated capacitance of the traces between the crystal and the XA/XB pins.

Q (Quality Factor)

This determines the width of the frequency resonance peak of the XTAL. It is defined as the ratio of reactance to series resistance at the oscillation frequency. XTALs typically have a high Q of around 30,000 to 150,000.

$$Q = \frac{\omega L_1}{R_1}$$

A high Q generally implies a better close in phase noise. It also means less frequency shift for a change in oscillator load capacitance. Higher ESR reduces Q.

CL (Load Capacitance)

This is the total capacitance needed to load the XTAL for proper oscillation frequency. This specification should match the loading provided internally by the built-in Si55xx/Si540x/Si536x oscillator, nominally 8pF. Mismatch of the loading capacitance will shift the XTAL oscillation frequency.

Drive Level

The power dissipated in the XTAL must be limited or the XTAL may become less reliable. The maximum drive level a XTAL must tolerate is usually specified in its data sheet in units of micro-Watts (μW).

Aside from these electrical specifications, XTAL vendors also specify mechanical performance and manufacturing information. XTAL dimensions could also be important as it determines the area it occupies.

XTAL Physical Size

XTALs come in many sizes, and include both thru-hole components with leads as well as surface mount components. The most common surface mount packages are rectangular 4-pin packages with a welded or soldered metal lid. Two of the four pins are used to connect to each side of the XTAL. The remaining 2 pins are connected to the XTAL shield pin on the Si55xx/Si540x/Si536x devices, labeled as "XV". These packages are specified in terms of the X and Y dimensions of the package. For example, a common case size may be specified either as "3.2 mm x 2.5 mm", or simplified to "3225". Similarly, there are 2520, 2016 etc. sizes. For the larger package sizes, there is not usually much effect on the electrical parameters of the XTAL. However, at smaller sizes, the ESR and Q may be affected due to the physically smaller XTAL required to fit in these packages.

Steps to Choose the Right XTAL for your Application

1. The nominal XTAL frequency must match the value set in the ClockBuilder™ Pro (CBPro) frequency plan on the Reference page of the CBPro Wizard. The Si55xx/Si540x/Si536x cannot operate in a stable way if the XTAL frequency is different.

2. The XTAL maximum ESR must be below the C0/ESR curve shown previously. Higher ESR XTALs may not reliably oscillate over all conditions.

3. The XTAL CL must be 8.0 pf.

4. The XTAL must be specified to operate with a maximum drive level of 200 μW.

Appendix B—Selecting an XTAL Oscillator for Your Application

Introduction to XTAL Oscillators

XTAL Oscillator (XO): This is the most basic oscillator type which has a XTAL and a driver circuit in the package. The frequency stability is in the order of tens of ppm. These are very cost effective.

Temperature Compensated XTAL Oscillator (TCXO): As the name suggests, the oscillator is compensated for the change in its temperature. From the properties of XTALs, its frequency changes with temperature and the load capacitance. In the case of a TCXO, the temperature effect is balanced by purposeful capacitive loading, which enhances the frequency accuracy and stability compared to an XO. Sub-1 ppm of accuracy can be obtained. However, it comes at an additional cost. The phase noise floor/jitter of an XO is typically lower than a VCXO, which is why Si55xx/Si540x/Si536x devices rely on an XO for phase noise and a TCXO for stability in the dual reference mode.

Oven Controlled XTAL Oscillator (OCXO): OCXO has an oven built into the package and instead of compensating for the temperature effects, it heats the oven to the zero-ppm temperature of the XTAL. An XTAL used in a OCXO is specially cut (usually SC type) so that at higher temperatures the change is frequency as a function of temperature is very small. In this case, the XTAL used needs to have its zero-ppm temperature higher than the expected ambient as the oven cannot cool the XTAL. OCXOs have a very high stability, on the order of ppb and slow aging, as well. Additionally, there is a double oven version of this oscillator, namely the oven controlled OCXO which places the entire OCXO inside the oven to maintain the temperature. The oven and the control circuit add significant cost to the OCXO and are usually the most expensive amongst the oscillators. OCXOs are used in the dual reference configuration for stability in conjunction with the XO for phase noise/jitter.

Table 7. XO Comparison

Parameter	XO	TCXO	OCXO
Frequency Accuracy (tolerance)	±15 to ±50 ppm	±1 to ±4.6 ppm	Less than ±1 ppm
Frequency stability (over temperature)	±10 to ±30 ppm	±10 to ±280 ppb	±1 to ±100 ppb
Power	Low < 50 mW	>100 mW but <1 W	2–4 W initial, 1–2 W once stabilized
Start-up time	5–10 ms	10–20 ms	5–10 minutes.
Cost	Low	Medium	High
Size	Small-Medium	Small-Medium	Large

Voltage Controlled XTAL Oscillator (VCXO): An XO/TCXO/OCXO is designed to be a fixed frequency as much as possible. A VCXO is designed to have its frequency controlled over a range of ppm defined by the absolute pull range (APR). The frequency of the VCXO can be adjusted within 10s to 1000s of ppb by applying a control voltage however, the tuning range is not as wide as a VCO. When used as a phase noise reference for Si5xxx device, the tuning of the VCO frequency is achieved by tuning the VCXO instead of an internal fractional divider so the VCXO phase noise reference will yield the most optimum phase noise for the Si55xx/Si540x/Si536x devices. VCXOs cost somewhere between an XO and a TCXO.

Similar to the process of choosing a XTAL, an XO also needs to be evaluated for its properties and performance versus the requirements.

XO/TCXO/OCXO Electrical Specifications

Frequency: The frequency of operation is determined by resonance of the XTAL inside the oscillator. Oscillators come in various frequencies up to hundreds of MHz.

Frequency accuracy and stability: In timing and synchronization applications, frequency accuracy is one of the major concerns. Even small frequency deviations can cause a loss of sync. Hence, it is of utmost importance that the frequency remains stable over time and temperature. This error is defined in terms of ppm (parts per million) or ppb (parts per billion).

$$ppm = \left(\left(Actual\ frequency\ -\ ideal\ frequency\right)\ /\ ideal\ frequency\right) \times 10^6$$

$$ppb = \left(\left(Actual\ frequency\ -\ ideal\ frequency\right)\ /\ ideal\ frequency\right) \times 10^6$$

The factors that contribute to this error are:

Initial tolerance: This is due to the XTAL inside the oscillator. The imprecision of the cut and uneven width of the XTAL leads to an inherent frequency offset. This is defined at room temperature of 25°C.

Temperature stability: The variation arises due to the XTAL. The data sheet spec indicates the minimum and maximum variation above and below the 0 ppm temperature. For a simple XO, the stability follows the XTAL's 3rd order temperature curve. The maximum deviation is in 10's of ppm.

For a TCXO, the 3rd order curve is compensated by changing the loading capacitance. As a result, a TCXO has a better temperature stability over a simple XO, typically 100 to 500 ppb. The OCXO has the best temp stability as the XTAL inside the oven is maintained around its 0 ppm temperature. The accuracy of OCXO is around 10 to 100 ppb.

Supply voltage sensitivity: The change in the nominal frequency due to power supply variations defines this sensitivity. Usually, ±5% of supply voltage variation is tolerated. An OCXO has a sensitivity in tens of ppb and a TCXO typically has a sensitivity around 50 ppb. For an XO, it is usually combined with the overall accuracy spec indicating that it is not very significant.

Load sensitivity: The change in the load capacitance influences the nominal frequency, although not significantly. For a ±10% of the load condition change (standard load is usually 10 pF || 10 kΩ), the change in frequency (in ppb) defines load sensitivity. This value for an OCXO is tens of ppb and hundreds of ppb for TCXO. For an XO, it is usually combined with the overall accuracy specification.

Reflow sensitivity: The oscillator is subjected to high temperature followed by a cool down during reflow soldering. This can cause a frequency shift called the reflow sensitivity. It is expressed in ppm.

Aging: The XTAL inside the oscillator is an electromechanical device and thus is subject to aging. Aging is typically higher during the first year of operation and slows down over time. Since aging is specified in multiple ways, the most appropriate value to use is a long-term aging spec at the highest average temperature the oscillator sees in the system.

Activity dips: A sudden change in the value of the output from the oscillator is termed as activity dip. The vendor must test for dips and specify the value. A typical test is to eliminate the activity dips that are larger than 2 ppm/°C across the temperature range.

For example, consider a scenario where a typical 40 MHz TCXO has an initial tolerance of 1 ppm, temperature stability of 0.3 ppm, supply voltage tolerance of 0.1 ppm, load sensitivity for a maximum 10% load change of 0.2 ppm, a per reflow shift of 1ppm and 1ppm aging. The overall error from this TCXO is the sum of individual errors.

Total error = 1 + 0.3 + 0.1 + 0.2 + 1 + 1 = 3.6 ppm

Output characteristics: The output format can be a differential or a single ended type. The Si55xx/Si540x/Si536x support either a differential or single ended XO to the REF_IN/REF_INB pins (Si55xx) or the XO_IN/XO_INB pins (Si540x/Si536x). The Si5518/12 and Si540x support a differential or single ended OCXO/TCXO to the INx/INxb pins (Si5518/12) or the REF/REFB pins (Si540x).The lowest phase noise XOs have a single ended (CMOs) output. TCXOs, OCXOs, and VCXOs may use differential output formats which can help reduce crosstalk that might be coupled onto the XO input to the Si55xx/Si540x/Si536x. See the Si55xx/Si540x/Si536x device reference manual for more details on the connections between the XO/TCXO/OCXO and the Si55xx/Si540x/Si536x. For lowest output phase noise, the REF_IN/XO_IN and INx inputs to the Si55xx/Si540x/Si536x require the input slew rate to be at equal or greater to the minimum slew rate specified in the Si55xx/Si540x/Si536x data sheet.

Operating temperature: This is the range of temperature which guarantees the operation of the oscillator per the data sheet specs. Operating temperature range should accommodate the system temperature range.

Power: Since an OCXO has an oven built in, it initially consumes high power to heat up until the frequency settles. Since the oven is always present, the overall power consumed by an OCXO is higher than a TCXO or XO. A TCXO and XO power is fairly constant from the time power is applied.

Startup time: An OCXO takes a few minutes to stabilize to the correct frequency due to heat-up time for the oven. The other oscillators take tens of milliseconds to reach the stable frequency at 25C operating conditions.

Power Supply Noise: Since XTAL oscillators are sensitive to noise on their supply voltage, it is important to follow the recommended filtering circuit provided by the XTAL oscillator supplier.

Phase Noise Performance: Phase noise is a frequency domain measure of random phase fluctuations of a signal such as a clock's carrier frequency. It is defined as power at an offset from the main carrier frequency in terms of dBc/Hz. The input clock phase noise   to the Si55xx/Si540x/Si536x dominates the output clock phase noise in the frequencies below the outer-loop bandwidth whereas the phase noise of the reference oscillator dominates the output clock phase noise in the frequencies above the outer loop bandwidth. For wireless applications, the phase noise from 10 Hz to >40 MHz needs to be optimized. In a wireless application the spurs usually need to be limited to a maximum level in dBc/Hz even when the jitter is sufficiently low. For Ethernet and SONET applications, the 12 kHz to 20 MHz band is what matters and spurs are generally not an issue unless they cause the integrated jitter to exceed the specified limits.

Phase noise integrated over the frequency band of interests yields RMS jitter. The band of integration and the RMS value are specified by different standards although 12 kHz to 20 MHz is a very common band of integration.

Wander generation: The ITU-T G.8262/ITU-T G.8262.1 standard specifies the wander generated in locked mode in terms of MTIE and TDEV. This measures the wander generated by this timing source alone. The device is locked to a wander-free input with a very low   (3 Hz or 100 mHz) outer-loop bandwidth. Thus, the choice of OCXO/TCXO reference input to the RFPLL/REFPLL plays an important role as the wander on the output comes directly from the reference. So, the reference oscillator needs to meet the defined wander specification at room temperature and over varying temperature as well.

Long term holdover accuracy: ITU-T G.8262 standard specifies wander in another term: long-term phase transient in holdover mode. It is the phase difference in the output clock with respect to the last input clock edge just before the moment it loses the input. The stability of the Si55xx/Si540x/Si536x device in holdover depends directly on the stability of the reference. So, it is necessary to test the reference accuracy. Section 11 of the G.8262 specifies the limits.

Jitter/Wander transfer: This is a function of the timing chip. The jitter and wander at the output of the Si55xx/Si540x/Si536x device primarily depends on the jitter from the input clock that is below the outer-loop cutoff frequency. ITU-T GR.8262 section 10 provides more details about jitter/wander transfer.

Jitter/wander tolerance: This is again a function of the timing chip which determined how much input jitter can be tolerated until it loses lock. ITU-TG.8262/ITU-TG.8262.1 section 9 specifies the tolerance masks for Ethernet applications.

VCXO Electrical Specifications

Absolute Pull Range (APR): This spec defines the number of ± ppm the VCXO can have its output pulled with respect to its nominal output frequency. For Synchronous Ethernet (SyncE) applications the APR of the VCXO chosen must be greater than ±4.6 ppm to support the worst case frequency deviation of the Ethernet recovered clock.

Tuning Gain (Kv): There is a trade-off between APR and tuning gain. For low close-in phase noise which is desired in Si55xx wireless applications a low tuning gain (in ppm/V) is required. A low Kv improves the resolution of the frequency tuning of the VCXO which results in lower phase noise close to the carrier. That being said a low Kv also makes it challenging to meet the desired APR specs. For wireless applications a Kv less than 20 ppm/V is recommended. By applying temperature compensation to the VCXO (VC-TCXO) the vendor can accommodate a lower Kv and still meet the APR spec. However, VC-TCXOs are typically significantly more expensive than VCXOs.

Steps to Choose the Right XTAL Oscillator for your Application

1. Choose the type of XO you need for your application. You can use Table 7 on page 17 as initial guidance.

2. Table 8 on page 21 and Table 9 on page 21 outline the key phase noise oscillator specifications you should consider for different applications.

3. The nominal XO frequency must be within the specified limits of the Si5xxx timing chip as defined in the data sheet. This value must be entered in the Reference step of the CBPro Wizard.

4. The peak to peak amplitude should be compatible with the Si55xx input pin for the oscillator input.

5. The oscillators output slew rate needs to meet the Si5xxx device data sheet specification.

6. An XO connected to the REF_IN pin will have a dominant effect upon the output phase noise up to ~2 MHz. Therefore, it is critical to choose an XO that has sufficiently low phase noise and use a low noise LDO for the XO supply voltage.

7. Generally, a TCXO or OCXO will be input to INx. In this case, the TXCO/OCXO phase noise will affect the output phase noise up to about 10 times the RFPLL loop bandwidth. The TCXO and OCXO wander and stability parameters are essential for compliance to the applicable standards.

8. A VCXO is only used on the Si55xx wireless devices for high end applications that require the lowest possible jitter and lowest mid band phase noise. Only the approved VCXOs should be used and a very low noise LDO must be used to provide the supply voltage to the VCXO.

9. Your application may require compliance to some or all of the following standards, G.8262, G.8262.1, G.8273.2, G.8273.4. Choosing the correct TCXO/OCXO is essential to meet these standards.

Table 8. XO Specifications

Parameter	Min	Typ	Max	Unit	Additional Information
Frequency	30.72	48, 54	300	MHz	Jitter increases below 48 MHz
Temperature range	−40	—	+95	C	Some applications require a max or +105
Total frequency error[1]	—	50	100	ppm	± the value shown, ±50 ppm are available
Spurs	—	—	−100	dBc/Hz	Normalize to 122.88 MHz[2, 3]
Jitter	—	<50	100	fs rms	The higher the XO jitter the higher the output clock jitter
Duty cycle	40	—	60	%	

1. Includes initial accuracy, variation over temp, aging over 10 years, soldering effects
2. If Fxo = 54 MHz, spurs need to be no higher than -100 + 20*LOG10(54/122.88) = -107.1 dBc/Hz.
3. XO to Fout transfer function of a Low Pass Filter of ~1 MHz will attenuate XO spurs that are above filter bandwidth

Table 9. VCXO Specifications

Parameter	Min	Typ	Max	Unit	Additional Information
Frequency	30.72	122.88	983.04	MHz	VCXO Frequency = N*1.92 MHz only (Si55xx only)
Temperature range	−40	—	+95	C	Some applications require a max of +105
Control voltage input impedance	50	—	—	K ohm	
Control input voltage low	0	—	0.3	V	
Control input voltage high	VDD-0.5	—	VDD	V	
Gain Kv		25		ppm/V	Pick the lowest that can meet the required minimum APR
Absolute pull range (APR)	5			±ppm	APR, the amount the frequency can be changed by the control voltage
Duty cycle	40	—	60	%	
Modulation bandwidth	10			kHz	Lower than the specified minimum may cause PLL instability
Spurs			−100	dBc/Hz	Normalize to 122.88 MHz[1, 2]
Jitter		<50	100	fs rms	12 kHz to 20 MHz, This jitter has a large effect upon the output clock jitter

1. If Fvcxo = 245.76 MHz, spurs need to be no higher than -100 + 20*LOG10(245.76/122.88) = -94 dBc/Hz.
2. VCXO to Fout transfer function of a Low Pass Filter of ~1 MHz will attenuate XO spurs that are above ~1 MHz.

Revision History

Revision	Date	Description	Notes

C	March, 2024	• Table 2: Added TXC 7M50072003 50 MHz XTAL.
		• Table 3: Added TXC 8W50070006 50 MHz XO.
		• Table 4: Corrected Epson P/N for 204.8 MHz VCXO.
		• Table 5: Added Epson N9848 10 MHz TCXO.
		  - Added Rakon N8900 19.44 MHz TCXO.
		  - Added TXC 7P 19.44 MHz and 38.88 MHz TCXO.
		  - Added Rakon N8998 20 MHz, N8903 38.88 MHz, N8997 48 MHz TCXO.
		• Table 6: Added Rakon STP3703LF, U9006LF 10 MHz OCXO.
		  - Removed TXC OH1947001, OK19470001 19.44 MHz OCXO.
		  - Added Rakon U8565LF 19.44 MHz, U8868LF 38.888 MHz OCXO.
		  - Corrected Rakon ROX OCXO package size from 25 x 22 mm to 25.4 x 22 mm.
		  - Corrected Rakon OCXO U8429LF package size.
		  - Added TXC OG38870003, OH38870003 38.88 MHz OCXO.
			CN0121442

B	June, 2023	• Added NDK ENA5930 to Table 6. • Modified power supply sensitivity and noise guidance (Appendix B).	CN0108827
A	November, 2022	• Initial release with alphanumeric revision code. • Modified content throughout.	CN0097868

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[Skyworks](#):

SI5360A-A10000-GM SI5360A-A10000-GMR SI5360A-A14360-GM SI5360A-A14360-GMR SI5360A-A14639-GM
SI5360A-A14639-GMR SI5360A-A14824-GM SI5360A-A14824-GMR