Si5512 Data Short

NetSync™ Low Phase Noise Jitter Attenuating Clock for 5G/ eCPRI/SyncE/IEEE 1588

The Si5512 is a 12-output variant of the 18-output Si5518 device. The Si5512 fully supports all of the network synchronization functionality of the Si5518 but does not support some RF functionality, such as a VCXO phase noise reference or OSYNC for JESD204B/C Subclass 2. The Si5512 is intended to support wireless network synchronization applications that split digital and RF functions onto separate PCBs. Split-board applications, such as massive MIMO, require an Si5512 network synchronizer on the digital board followed by an RF jitter attenuator or buffer for each of the RF cards residing on physically-separated boards.

The Si5512 may also be combined with optional AccuTime™ IEEE 1588 software offering a complete IEEE 1588v2 solution for phase and frequency synchronization. AccuTime 1588 software consists of a unique servo algorithm paired with a protocol stack that runs on the host processor.

The RFPLL generates high performance low phase noise CPRI clocks for wireless remote radio heads (RRH). Each of the 12 clock outputs are configurable in any combination of DCLK, SYSREF, or other system clocks. The DSPLLs are fully featured network synchronization phase-locked-loops with adjustable DCO for IEEE 1588 Ethernet fronthaul synchronization.

Applications:

- LTE-A and 5G Remote Radio Units (RRU)
- JESD204B/C clock generation
- IEEE1588 slave clocks (T-TSC), Telecom Boundary Clocks (T-BC)
- IEEE1588 Assisted Partial Timing support clocks (T-BC-A, T-TSC-A), Partial Timing Support (T-BC-P, T-TSC-P)
- IEEE 1588 Grandmaster clocks (T-GM)
- Remote Access Networks (RAN), picocells, small cells
- Remote Radio Heads (RRH), wireless repeaters, mobile fronthaul and backhaul

KEY POINTS

Si5512

- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Ultra high-performance clock generation for LTE-A and 5G RRUs with IEEE 1588/ SyncE
- Optional AccuTime™ IEEE 1588 software
- Integer output frequencies up to 1.2288 GHz
- Fractional output frequencies up to 650 MHz
- JESD204B/C clock generation (DCLK/ SYSREF) with synchronization across multiple devices
- Programmable delay at each output
- Ultra-low jitter: 47 fs RMS typical
- Phase Noise:
  - Noise floor –164 dBc/Hz at 491.52 MHz
  - –145 dBc/Hz at 800 kHz offset for a 491.52 MHz carrier frequency
- Spurs < –95 dBc at 122.88 MHz
- Support IEEE1588 with DCO adjustable at 1 ppt resolution
- Locks to 1PPS and PP2S
- Full suite of status monitors
- Supports ITU-T G.8273.2 (T-TSC, T-BC), ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A), G.8262 (EEC Options 1 and 2), G.8262.1 (eEEC), G.8273.1 (T-GM), and G.8261 (TC12-17)
- Low-Power Mode
- 72 QFN 10x10 mm, 6 inputs, 12 outputs
- AccuTime™ IEEE 1588 Software
  - Field tested and proven with compliance reports available
  - Demo Platform Support
  - O-RAN compatible
  - IEEE 1588 servo loop and protocol stack software runs on host processor

1. Feature List

- RFPLL
  - Supports JESD204B/C Subclass 0, 1
  - Ultra-low Phase Noise (example at 491.52 MHz carrier):
    - –164 dBc/Hz noise floor
    - –145 dBc/Hz at 800 kHz offset
  - Ultra-low jitter performance:
    - <50 fs typ XO (12 kHz–20 MHz at 491.52 MHz)
  - Selectable jitter attenuation bandwidth: 10 Hz to 4 kHz, 30 Hz to 4 kHz Dual Reference JA
- DSPLL A, DSPLL B
  - Independent network synchronization DSPLLs
  - Supports ITU-T G.8273.2 (T-TSC, T-BC) and ITU-T G.8273.4 (T-BC-P, T-BC-A, T-TSC-P, T-TSC-A)
  - Programmable loop bandwidth: 1 mHz to 4 kHz
  - Automatic Free-Run, Holdover, and Locked modes
  - Hitless input clock switching: automatic or manual with < 150 ps phase transient
- PPSPLL
  - Instant lock for 1PPS/PP2S
  - Programmable loop bandwidth 1 mHz to 25 mHz
  - Programmable phase slope limiting (PSL) and phase pull-in rate (PPI)
- 12 Programmable Clock Outputs:
  - JESD204B/C DCLK or SYSREF. Up to six DCLK/SYSREF pairs
  - Integer Q dividers: PP2S/1PPS to 1.2288 GHz
  - JESD204B/C SYSREF Pulser Mode
  - Multisynth Fractional Dividers: PP2S/1PPS to 650 MHz
  - Output-to-Output Static Delay: ±10 ns
  - Output-output skew: ±50 ps
  - LVDS, S-LVDS, AC coupled LVPECL, LVCMOS, Slew Rate Limited (SRL) LVCMOS, HCSL, CML
- Utilizes fifth-generation DSPLL™ and MultiSynth™ technologies
- Zero Delay Mode for all PLLs
- 4/6 clock inputs:
  - Differential: 8 kHz to 1 GHz
  - CMOS: 1PPS, PP2S, 8 kHz to 250 MHz
- Status monitoring (LOS, OOF, PHMON, FLOL and PLOL)
- Automatically generates free-running clocks at power up
- Automatically locks to a valid clock input
- Automatic Holdover Mode
- Core voltage: 3.3 V, 1.8 V
- Output driver supply voltages (VDDO): 3.3 V, 2.5 V, 1.8 V
- Serial Interface: I^2C or SPI (3 or 4-wire)
- ClockBuilder Pro™ software tool simplifies device configuration
- Package: 72-Lead QFN, 10x10 mm
- Extended temperature range:
  - –40 to +95 °C ambient
  - –40 to +105 °C board
- Pb-free, RoHS compliant

Note: Specifications given on this page are for reference only. Please refer to for device performance.

2. Package Outline

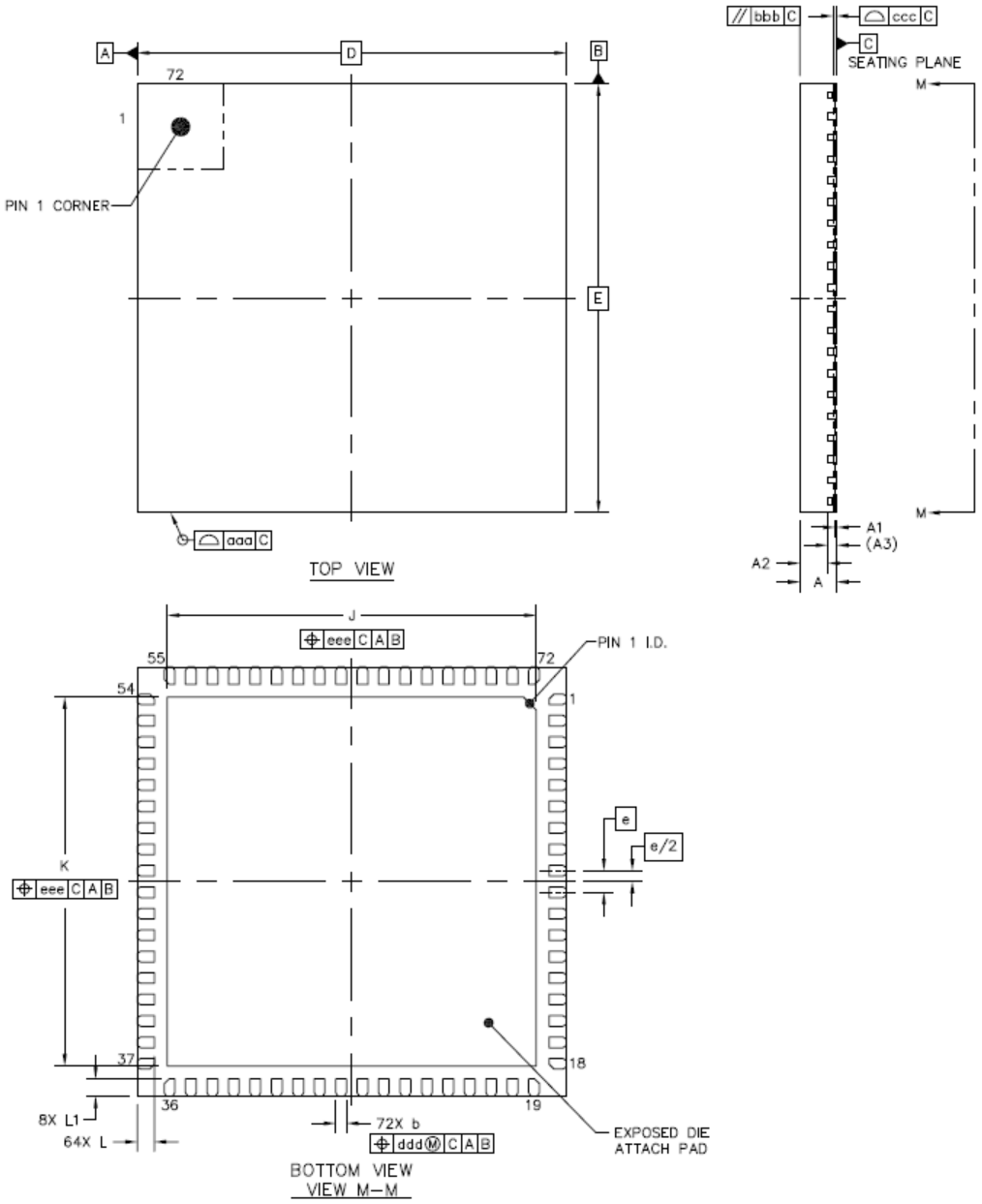

Figure 2.1. 72-QFN Package Diagram

Table 2.1. Package Dimensions

	Symbol	Min	Typ	Max
Total Thickness	A	0.8	0.85	0.9
Stand Off	A1	0	0.035	0.05
Mold Thickness	A2	–	0.65	–
L/F Thickness	A3		0.203 REF	
Lead Width	b	0.2	0.25	0.3

		Symbol	Min	Typ	Max
Body Size	X	D		10 BSC	
	Y	E		10 BSC	
Lead Pitch		e		0.5 BSC	
EP Size	X	J	8.5	8.6	8.7
	Y	K	8.5	8.6	8.7
Lead Length		L	0.35	0.4	0.45
		L1	0.3	0.4	0.45
Package Edge Tolerance		aaa		0.1	
Mold Flatness		bbb		0.1	
Coplanarity		ccc		0.08	
Lead Offset		ddd		0.1	
Exposed Pad Offset		eee		0.1	
Weight		N/A	—	0.35 g	—

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC Solid State Outline MO-220.

3. PCB Land Pattern

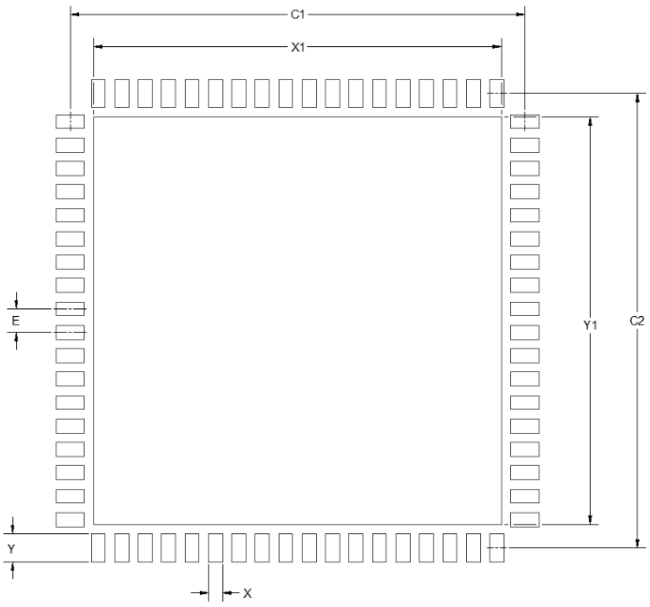

Figure 3.1. PCB Land Pattern

Table 3.1. PCB Land Pattern Dimensions

Dimension	mm
C1	9.70
C2	9.70
E	0.50
X	0.30
Y	0.60
X1	8.70
Y1	8.70

Note:

General

1. All dimensions shown are in millimeters (mm).
2. This Land Pattern Design is based on the IPC-7351 guidelines.
3. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all pads.
4. A 4x4 array of 1.45 mm square openings on a 2.00 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

**Above notes and stencil design are shared as recommendations only. A customer or user may find it necessary to use different parameters and fine tune their SMT process as required for their application and tooling.*

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