

# Si53358/4/2 数据表

# 10/8/4/2 输出时钟缓冲器

Si5335x 通用和引脚可选格式设备是业界性能高、功耗低的汽车级扇出缓冲器。该设备提供 10、8、4 和 2 路输出选项,支持差分和单端输出格式。这些设备具有典型的 120 fs 附加相位抖动特性,可在 10-250 MHz 的频率范围内工作。内置 LDO 具有高 PSNR 性能,并减少了对外部组件的需求,从而简化了在嘈杂环境中的低抖动时钟分配。

Si5335x 产品系列提供引脚可选输入/输出格式版本以及完全可自定义版本,在这些版本中,可以使用 ClockBuilder Pro 定义输入/输出格式和输入硬件引脚以满足确切系统要求。通过使用 ClockBuilder Pro,用户可以单独定义每个输出上的信号格式,启用 2:1 输入多路复用器,以及定义 输入/输出电压转换。除这些功能外,还可以启用输入时钟的 LOS 监视。

应用:

- 信息娱乐
- ADAS

- 雷达传感器
- 自动驾驶处理单元
- 网络网关

#### 主要特点

- 10、8、4、2 路输出订购选项
- 输入时钟丢失的信号丢失 (LOS) 监视
- 符合 AEC-Q100
- 符合 AEC-Q006
- 汽车级 2: -40 至 +105 °C
- 10 250 MHz 频率范围
- 使用 ClockBuilder Pro 实现完全可自定义的 配置
- 出色的附加抖动性能
- 120 fs RMS, 156.25 MHz 硬件控制引脚,用于输出使能
- •可选双输入功能,带 MUX
- 1.8 3.3 V 电源
- 无铅、符合 RoHS-6

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# 1. 功能列表

- 10、8、4、2 路输出订购选项
- 输入时钟丢失的信号丢失 (LOS) 监视
- ・符合 AEC-Q100
- ・符合 AEC-Q006
- 汽车级 2: -40 至 +105 °C
- 10 250 MHz 频率范围
- 自定义选项使用 ClockBuilder Pro
   单个输出格式标准可编程性
- 出色的附加抖动性能
- 120 fs RMS, 156.25 MHz
- 独立硬件控制引脚,用于输出使能
- •可选双输入功能,带 MUX
- 1.8 3.3 V 电源
- ・无铅、符合 RoHS-6

# 2. Ordering Guide

Input/Output Format Configuration	Number of Inputs	Number of Outputs	Part Number <sup>1</sup>	Package Type	Temperature		
	1	2					
	2	4	Si53354A-D01AM	40-pin QFN			
	2	8	Si53358A-D01AM	40-pin QFN			
	2	10	Si53350A-D01AM	48-pin QFN			
Pin-Selectable	1	2	Si53358BD12751-AM <sup>2</sup>	32-pin QFN			
	2	4	Si53358BD12750-AM <sup>2</sup>	40-pin QFN	-40 °C to +105 °C		
	2	8	Si53358BD12749-AM <sup>2</sup>	40-pin QFN	Automotive Grade 2		
	2	10	Si53350BD12748-AM <sup>2</sup>	48-pin QFN			
	1	2	Si53352BD-xxxxx-AM <sup>3</sup>	32-pin QFN			
User-Defined	2	4	Si53354BD-xxxxx-AM <sup>3</sup>	40-pin QFN			
(ClockBuilder Pro)	2	8	Si53358BD-xxxxx-AM <sup>3</sup>	40-pin QFN			
	2	10	Si53350BD-xxxxx-AM <sup>3</sup>	48-pin QFN			

## Note:

1. For tape and reel, add "R" to the end of the orderable part number.

2. These devices support complementary LVCMOS output format, please see section 3.2 for more details.

3. For user-defined devices, the "xxxxx" suffix is generated by ClockBuilder Pro after a configuration file is created.

# 3. Functional Description

# 3.1 Functional Block Diagrams

3.1.1 Si53352A-D01AM Functional Block Diagram



Figure 3.1. Si53352A-D01AM Functional Block Diagram

## 3.1.2 Si53354A-D01AM Functional Block Diagram



Figure 3.2. Si53354A-D01AM Functional Block Diagram



Figure 3.3. Si53358A-D01AM Functional Block Diagram



Figure 3.4. Si53350A-D01AM Functional Block Diagram

## 3.1.5 Si53352BDxxxxx-AM Functional Block Diagram







Figure 3.6. Si53354BDxxxxx-AM Functional Block Diagram

3.1.7 Si53358BDxxxxx-AM Functional Block Diagram



Figure 3.7. Si53358BDxxxxx-AM Functional Block Diagram



Figure 3.8. Si53350BDxxxxx-AM Functional Block Diagram

#### 3.2 Output Signal Formats

The differential output swing and common mode voltage are compatible with a wide variety of signal formats including HCSL, LVDS, and LVPECL. In addition to supporting differential signals, the Si5335x devices support LVCMOS in-phase output drivers as well as complementary LVCMOS output drivers. User-defined customization is available using ClockBuilder Pro, each individual output driver can be set to any single-ended of differential output format to exactly match system requirements without using external level translation circuits.

Si53352A-D01AM,	Si53354A-D01AM,	and Si53358A-D0	01AM signal	formats c	an be	set using	the pre-defined	hardware	input pins as
follows:									

Format_SEL1	Format_SEL0	Input Format	Output Format	Valid VDDO Voltages
0	0	LVCMOS	LVCMOS (in-phase, dual outputs)	1.8V – 3.3V
0	1		LVPECL	2.5V or 3.3V
1	0	Differential	LVDS	2.5V or 3.3V
1	1		HCSL (100 Ω)	1.8V – 3.3V

Using Si53352A-D01AM, Si53354A-D01AM, and Si53358A-D01AM in Format\_SEL[1:0]=00 mode (LVCMOS in-phase, dual outputs) is not recommended for new designs. Silicon Labs has performed extensive system level EMI/EMC testing to CISPR25 Class-4 and Class-5 specifications using both LVCMOS (in-phase dual outputs) and complementary LVCMOS output drivers. Results show that generating single-ended clocks using complementary LVCMOS output drivers have significantly lower impact on system EMI/EMC, therefore Silicon Labs recommends the use of complementary LVCMOS drivers for all single-ended clocks. A complete overview of the testing and recommended design guidelines is summarized in AN1237. The Si5335x automotive buffer products are customizable using ClockBuilder Pro, which provides the option of selecting complementary LVCMOS output drivers, Silicon Labs has created the following orderable part numbers, which are available and in production:

Orderable Part Number	Number of Outputs	Input Format	Output Format	Valid VDDO Voltages
Si53352BD12751-AM	2	LVCMOS	Complementary LVCMOS	1.8V – 3.3V
Si53354BD12750-AM	4	LVCMOS	Complementary LVCMOS	1.8V – 3.3V
Si53358BD12749-AM	8	LVCMOS	Complementary LVCMOS	1.8V – 3.3V
Si53350BD12748-AM	10	LVCMOS	Complementary LVCMOS	1.8V – 3.3V

Note:

1. Format\_SEL1 and Format\_SEL0 are unused for these part numbers, connect those pins to ground.

Pinout diagrams and descriptions can be found in the data sheet addendum for the devices noted above by typing in the orderable part number in the "Look Up or Customize an Oscillator or Clock" field at https://www.silabs.com/timing/lookup-customize.

#### 3.2.1 Differential Output Terminations

#### **LVDS Driver Termination**

For a general LVDS interface, the recommended value for the differential termination impedance ( $Z_T$ ) is between 90  $\Omega$  and 132  $\Omega$ . Select the actual value to match the differential impedance (Z0) of the transmission line. A typical point-to-point LVDS design uses a 100  $\Omega$  parallel resistor at the receiver and a 100  $\Omega$  differential transmission-line environment. To avoid any transmission-line reflection issues, surface mount the components and place them as close to the receiver as possible. The standard LVDS termination schematic as shown in Figure 3.9 on page 12 can be used with either type of output structure. Figure 3.10 on page 12, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 0.01 to 0.1  $\mu$ F. If using a non-standard termination, contact Silicon Labs to confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.



Figure 3.10. Optional LVDS Termination

#### **Termination for 3.3 V LVPECL Outputs**

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines. The differential outputs generate LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50  $\Omega$  transmission lines. Use matched impedance techniques to maximize operating frequency and minimize signal distortion. Figure 3.11 on page 13 and Figure 3.12 on page 13 show two different layouts. Other suitable clock layouts may exist, but it is recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.



Figure 3.11. 3.3 V LVPECL Output Termination, Option 1



Figure 3.12. 3.3 V LVPECL Output Termination, Option 2

#### **Termination for 2.5 V LVPECL Outputs**

Figure 3.13 on page 14 and Figure 3.14 on page 14 show examples of termination for the 2.5 V LVPECL driver option. These terminations are equivalent to terminating 50  $\Omega$  to VDDO – 2 V. For VDDO = 2.5 V, the VDDO – 2 V is very close to ground level. The R3 in Figure 3.14 on page 14 can be optionally eliminated using the termination shown in Figure 3.13 on page 14.



Figure 3.13. 2.5 V LVPECL Termination Example, Option 1



Figure 3.14. 2.5 V LVPECL Termination Example, Option 2

#### 3.2.2 LVCMOS Output Terminations

LVCMOS outputs can be dc-coupled, as shown in the figure below.





#### 3.2.3 LVCMOS Output Signal Swing

The signal swing (V<sub>OL</sub>/V<sub>OH</sub>) of the LVCMOS output drivers is set by the voltage on the VDDO pin for the respective bank.

#### 3.2.4 LVCMOS Output Polarity

When a driver is configured as an LVCMOS output, it generates a clock signal on both pins (OUTx and OUTxb). By default, the clock on the OUTxb pin is generated in phase with the clock on the OUTx pin, unless complementary LVCMOS is explicitly selected.

#### 3.2.5 Termination for HCSL Outputs

The Si5335x HCSL driver features integrated termination resistors to simplify interfacing to an HCSL receiver.

Si53352A-D01AM, Si53354A-D01AM, Si53358A-D01AM, and Si53350A-D01AM have pre-defined feature HCSL drivers set to match 100  $\Omega$  impedance and do not require any external termination.

Si53352BDxxxxx-AM, Si53354BDxxxxx-AM, Si53358BDxxxxx-AM, and Si53350ADxxxxx-AM have output feature programmable HCSL output drivers that can be set to match either 100  $\Omega$  or 85  $\Omega$  impedance in ClockBuilder Pro.



Figure 3.16. HCSL Internal Termination Mode

#### 3.3 Output Enable/Disable

Output enable hardware pins provide a convenient method of disabling or enabling the output drivers. When the output enable pin is held high all designated outputs will be disabled. When held low, the designated outputs will be enabled.

Si53352A-D01AM, Si53354A-D01AM, Si53358A-D01AM, Si53350A-D01AM, Si53350BD12751-AM, Si53350BD12750-AM, Si53350BD12749-AM, and Si53350BD12748-AM have pre-defined output enable pins. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take <20 µs for the output to have a clean clock. Output enabled/disabled for LVCMOS are done in pairs. Each differential buffer True and Compliment output can generate an LVCMOS clock and the OE pin associated with the True and Compliment output buffer will control the respective LVCMOS pair.

Users can opt to define universal hardware pins on Si53352BDxxxxx-AM, Si53354BDxxxxx-AM, Si53358BDxxxxx-AM, and Si53350ADxxxxx-AM as output enable for any output, or any combination of outputs. See Section 3.4 for more details.

#### 3.4 Universal Hardware Pins (Si53352BDxxxxx-AM, Si53354BDxxxxx-AM, Si53358BDxxxxx-AM, and Si53350BDxxxxx-AM)

Universal hardware input pins are user-configurable control input pins that can have one or more of the functions listed below assigned to them using ClockBuilder Pro.

Description	Туре	Function
OE	Input	Output enable for one or more outputs.
Input SEL	Input	Selects between input sources, if 2 input clocks are defined.
LOS	Output	Loss of signal monitor

Universal hardware pins can be utilized for the following functions:

#### **Output Enable**

A universal hardware input pin can be defined to control output enable of a differential output, a bank of differential outputs, or as a global output enable pin controlling all outputs. Upon de-assertion of an OE pin, the corresponding output will be disabled within 2-6 clock cycles. Asserting an OE pin from disable to enable will take <20 µs for the output to have a clean clock.

#### Input SEL

A universal hardware input pin can be defined to set the input source clock between the input clocks, if two input clock sources are defined. Upon switching the input clock source, the output will not be glitch free. It is intended for the user to set this pin to a known state before the system is powered up or have the receiver address any unintended output signals when switching to a different input source clock.

#### Loss of Signal (LOS)

LOS is a feature that can be implemented during configuration file development using ClockBuilder Pro on a customized device. The LOS indicator is used to check for the presence of an input reference source (crystal or clock). Users can choose either active high or active low logic when the LOS pin is defined. LOS will assert when the reference source frequency drops below the minimum input frequency (Fin) specifications noted in Table 5.3 Clock Input Specifications on page 19.

#### For Active High:

Poll the LOS pin to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin will assume a logic high (LOS = 1) state. When a reference source is present at the associated input clock pin, the LOS pin will assume a logic low (LOS = 0) state.

#### For Active Low:

Poll the LOS pin to check for the presence of the currently selected input clock. In the event that a reference source is not present, the associated LOS pin will assume a logic low (LOS = 0) state. When a reference source is present at the associated input clock pin, the LOS pin will assume a logic high (LOS = 1) state.

# 4. Power Supply Filtering Recommendations

The Si5335x features internal LDOs on each power supply pin, providing excellent power supply noise rejection. As a guideline, each power supply pin should use a parallel combination of a 1  $\mu$ f and a 0.1  $\mu$ F bypass capacitor placed as close to the supply pin as possible.

## 5. Electrical Specifications

#### Table 5.1. Recommended Operating Conditions

 $(V_{DD} = V_{DDA} = V_{DD DIG} = 1.8 \text{ V to } 3.3 \text{ V +5\%/-5\%}, V_{DDO} = 1.8 \text{ V \pm5\%}, 2.5 \text{ V \pm5\%}, \text{ or } 3.3 \text{ V \pm5\%}, T_A = -40 \text{ to } 105 \text{ °C})$ 

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Ambient Temperature	T <sub>A</sub>		-40	25	105	°C
Junction Temperature	TJ <sub>MAX</sub>			_	125	°C
Core Supply Voltage	V <sub>DDA</sub> , V <sub>DD_DIG</sub> , V <sub>DD</sub>		1.71	_	3.46	V
Output Driver Supply Voltage	V <sub>DDO</sub>		1.71	_	3.46	V

Note:

1. All minimum and maximum specifications are guaranteed and apply across the recommended operating conditions. Typical values apply at nominal supply voltages and an operating temperature of 25 °C unless otherwise noted.

#### Table 5.2. DC Characteristics

 $(V_{DD} = V_{DDA} = V_{DD\_DIG} = 1.8 \text{ V to } 3.3 \text{ V } +5\% / -5\%, V_{DDO} = 1.8 \text{ V } \pm5\%, 2.5 \text{ V } \pm5\%, \text{ or } 3.3 \text{ V } \pm5\%, T_A = -40 \text{ to } 105 \text{ °C})$ 

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Core Supply Current	I <sub>DD</sub>		_	11	18	mA
Output Buffer Supply	I <sub>DDOx</sub>	LVPECL Output <sup>1</sup> @ 156.25 MHz		33	35	mA
Current		HCSL Output <sup>1</sup> @ 100 MHz		20	22	mA
		LVDS Output <sup>1</sup> @ 156.25 MHz		11	13	mA
		3.3 V VDDO LVCMOS <sup>2</sup> output @ 170 MHz	_	16	19	mA
		2.5 V VDDO LVCMOS <sup>2</sup> output @ 170 MHz	_	9	11	mA
		1.8 VDDO LVCMOS <sup>2</sup> output @ 170 MHz	_	7.5	8.5	mA
Total Power Dissipation	Pd	48-pin	_	400	1150	mW
		40-pin	_	260	670	mW
		32-pin	_	80	215	mW

## Notes:

1. Differential outputs terminated into a 100  $\Omega$  load.

2. LVCMOS outputs measured into a 5 inch 50  $\Omega$  PCB trace with 4 pF load.



3. Detailed power consumption for any configuration can be estimated using ClockBuilderPro when an evaluation board (EVB) is not available. All EVBs support detailed current measurements for any configuration.

### Table 5.3. Clock Input Specifications

# $(V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 \text{ V to } 3.3 \text{ V +5\%/-5\%}, V_{DDO} = 1.8 \text{ V } \pm 5\%, 2.5 \text{ V } \pm 5\%, \text{ or } 3.3 \text{ V } \pm 5\%, T_A = -40 \text{ to } 105 \text{ °C})$

Parameter	Symbol	Test Condition	Min	Тур	Max	Units							
Input Clock (AC-coupled Differential Input Clock on CLKIN_2/CLKIN_2# or CLKIN_3/CLKIN_3#)													
Frequency	F <sub>IN</sub>	Differential	10	_	250	MHz							
Voltage Swing	V <sub>PP_DIFF</sub> <sup>3</sup>	Differential AC-coupled < 250 MHz	0.5	_	1.8	V <sub>PP_diff</sub>							
Slew Rate	SR/SF	20-80%	0.75	_	_	V/ns							
Duty Cycle	DC		40	_	60	%							
Input Impedance	R <sub>IN</sub>		10	_	_	kΩ							
Input Capacitance	C <sub>IN</sub>		2	3.5	6	pF							
Input Clock (AC-coupled LVCMOS	Input Clock o	n CLKIN_2 or CLKIN_3)											
Frequency	F <sub>IN</sub>		10	_	170	MHz							
Input High Voltage	V <sub>IH</sub>		0.8 × V <sub>DD</sub>	—	_	V							
Input Low Voltage	V <sub>IL</sub>		_	_	$0.2 \times V_{DD}$	V							
Slew Rate <sup>1,2</sup>	SR/SF	20-80%	0.75		_	V/ns							
Duty Cycle	DC		40	_	60	%							
Input Capacitance	C <sub>IN</sub>		2	3.5	6	pF							
Notes: 1. Imposed for jitter performance.	1		1 1		1								

2. Rise and fall times can be estimated using the following simplified equation:  $tr/tf_{80-20} = ((0.8 - 0.2) * V_{IN_Vpp_se}) / SR$ .

3. V<sub>PP DIFF</sub> = 2 x V<sub>PP SINGLE-ENDED</sub>

## Table 5.4. Control Pins

## $(V_{DD} = V_{DDA} = V_{DD_DIG} = 1.8 \text{ V to } 3.3 \text{ V } +5\%/-5\%, \text{ or } 3.3 \text{ V } \pm5\%, \text{ T}_A = -40 \text{ to } 105 \text{ }^{\circ}\text{C})$

Parameter	Symbol	Test Condition	Min	Тур	Мах	Units
Si5332 Control Input Pins (Universalx)						
Input Voltage	V <sub>IL</sub>		-0.1	—	0.3 × VDD <sup>1</sup>	V
	V <sub>IH</sub>		0.7 × VDD <sup>1</sup>	_	1.1 × V <sub>DD</sub>	V
Input Capacitance	C <sub>IN</sub>		_	—	4	pF
Pull-up/down Resistance	R <sub>IN</sub>		—	50	_	kΩ
Note:						
<ol> <li>1. V<sub>DD</sub> indicates all core voltages V<sub>DD_DI</sub></li> </ol>	<sub>G</sub> , V <sub>DDA</sub> , and V <sub>I</sub>	<sub>DD_XTAL</sub> which are req	uired to all be u	sing same no	ominal voltage.	

## Table 5.5. Differential Clock Output Specifications

# $(V_{DD} = V_{DDA} = V_{DD_{DIG}} = 1.8 \text{ V to } 3.3 \text{ V } +5\% / -5\%, V_{DDO} = 1.8 \text{ V } \pm5\%, 2.5 \text{ V } \pm5\%, \text{ or } 3.3 \text{ V } \pm5\%, T_{A} = -40 \text{ to } 105 \text{ }^{\circ}\text{C})$

Parameter	Symbol	Test Con	dition	Min	Тур	Max	Units
Output-Output Skew	Т <sub>SK</sub>	Within the sa	me bank	_	_	30	ps
		Across b	anks	_	_	80	ps
Output Voltage Swing	V <sub>SEPP</sub>	LVPECL		0.6	0.75	0.85	V <sub>PP</sub>
		LVDS	1.8/2.5/3.3 V	0.3	0.375	0.45	V <sub>PP</sub>
		HCSL		0.7	0.8	0.9	V <sub>PP</sub>
Common Mode Voltage	V <sub>CM</sub>	LVPECL		_	VDDO-1.4	—	V
		LVDS	2.5/3.3 V	1.125	1.2	1.275	V
		LVDS	1.8 V	0.75	0.8	0.85	V
		HCSL		0.35	0.4	0.45	V
HCSL Edge Rate	Edgr	Notes 2,	4, 6	1	_	4.5	V/ns
HCSL Delta Tr	D <sub>tr</sub>	Notes 4,	Notes 4, 5, 10			155	ps
HCSL Delta Tf	D <sub>tf</sub>	Notes 4,	5, 10	_	_	155	ps
HCSL Vcross Abs	V <sub>xa</sub>	Notes 1, 3	3, 4, 5	250	_	550	mV
HCSL Delta Vcross	D <sub>vcrs</sub>	Notes 4,	5, 9	_	_	140	mV
HCSL Vovs	V <sub>ovs</sub>	Notes 4,	5, 8	_	_	V <sub>HIGH</sub> +300	mV
HCSL Vuds	V <sub>uds</sub>	Notes 4,	5, 9	_	_	V <sub>LOW</sub> -300	mV
HCSL Vrng	V <sub>rng</sub>	Notes 4	4, 5	V <sub>HIGH</sub> -200	_	V <sub>LOW</sub> +200	mV
Rise and Fall Times	t <sub>R</sub> /t <sub>F</sub>	LVDS (fast mode)	3.3 V or 2.5 V	150	200	350	ps
(20% to 80%)		LVDS (slow mode)	3.3 V or 2.5 V	350	530	620	ps
			1.8 V	150	225	350	ps
Rise and Fall Times	t <sub>R</sub> /t <sub>F</sub>	LVPEC	CL	150		320	ps
(20% to 80%)		HCSI	L	_	_	420	ps



#### Table 5.6. LVCMOS Clock Output Specifications

 $(V_{DD} = V_{DDA} = V_{DD})_{DIG} = 1.8 \text{ V to } 3.3 \text{ V } +5\% -5\%, V_{DDO} = 1.8 \text{ V } \pm5\%, 2.5 \text{ V } \pm5\%, \text{ or } 3.3 \text{ V } \pm5\%, T_A = -40 \text{ to } 105 \text{ °C})$ 

Parameter	Symbol	Test Condition	Min	Тур	Max	Units
Frequency	fout	1.8-3.3 V CMOS	5	—	170	MHz
		1.5 V CMOS	5	—	133.33	MHz
Rise/Fall Time, 3.3 V (20-80%)	t <sub>R</sub> /t <sub>F</sub>	50 Ω impedance, 5" trace, CL = 4 pf	_	0.5	0.8	ns
Rise/Fall Time, 2.5 V (20-80%)	t <sub>R</sub> /t <sub>F</sub>	50 Ω impedance, 5" trace CL = 4 pf	_	0.6	0.95	ns
Rise/Fall Time, 1.8 V (20-80%)	t <sub>R</sub> /t <sub>F</sub>	50 Ω impedance, 5" trace CL = 4 pf	_	0.75	1.3	ns
Rise/Fall Time, 1.5 V (20-80%)	t <sub>R</sub> /t <sub>F</sub>	50 Ω impedance, 5" trace CL = 4 pf	_	0.9	1.3	ns
CMOS Output Resistance		3.3 V	_	46	—	Ω
(Single Strength)		2.5 V	_	48	_	Ω
		1.8 V	_	53	_	Ω
		1.5 V	_	58	—	Ω
CMOS Output Voltage	V <sub>OH</sub>	–4 mA load	VDDO-0.3	—	_	V
	V <sub>OL</sub>	4 mA load	_	_	0.3	V
Duty Cycle	DC	XO and PLL mode	45	_	55	%

#### Table 5.7. Performance Characteristics

 $(V_{DD} = V_{DDA} = V_{DD_{DIG}} = 1.8 \text{ V to } 3.3 \text{ V } +5\% -5\%, V_{DDO} = 1.8 \text{ V } \pm5\%, 2.5 \text{ V } \pm5\%, \text{ or } 3.3 \text{ V } \pm5\%, T_A = -40 \text{ to } 105 \text{ °C})$ 

Parameter	Symbol	Test Condition	Min	Тур	Мах	Units
Power Ramp	t <sub>VDD</sub>	0 V to V <sub>DDmin</sub>	0.1	_	10	ms
Clock Stabilization from Power-up	t <sub>STABLE</sub>	Time for clock outputs to appear after POR	_	15	25	ms

#### Table 5.8. Additive Jitter Performance Specifications

 $(V_{DD} = V_{DDA} = V_{DD DIG} = 1.8 \text{ V to } 3.3 \text{ V +5\%/-5\%}, V_{DDO} = 1.8 \text{ V \pm5\%}, 2.5 \text{ V \pm5\%}, \text{ or } 3.3 \text{ V \pm5\%}, T_A = -40 \text{ to } 105 \text{ °C})$ 

Parameter	Symbol	Test Condition	Тур	Мах	Units
Additive Phase Jitter		156.25 MHz, 12 kHz-20 MHz <sup>1</sup> , LVDS (slow mode)	130 (LVDS slow)	170	fs RMS
		156.25 MHz, 12 kHz-20 MHz, LVDS (fast mode)	120	150	fs RMS
		156.25 MHz, 12 kHz-20 MHz, LVPECL <sup>1</sup>	110	140	fs RMS
		156.25 MHz, 12 kHz-20 MHz, HCSL <sup>1</sup>	120	150	fs RMS
PCle Gen3/4 Addi- tive Phase Jitter	Addi- litter Includes PLL BW 2– 4 MHz, CDR = 10 MHz <sup>2, 3, 4, 5</sup>		54	69	fs RMS
PCle Gen5 Additive Phase Jitter		100 MHz HCSL in- put/outputs Includes PLL BW 500 kHz - 1.8 MHz, CDR = 20 MHz <sup>2, 3, 4,</sup> 5	21	27	fs RMS

Note:

1. Measured with differential input on CLKIN\_2, bypassing the PLL to any output.

Silicon Labs PCIe Clock Jitter Tool is used to obtain measurements for additive phase jitter. Additive Phase Jitter = sqrt(output jitter<sup>2</sup> - input jitter<sup>2</sup>). Input used is 100 MHz from Si5340.

3. Measurements on 100 MHz output use the template file in the PCIe Clock Jitter Tool.

4. For complete PCIe specifications, visit www.pcisig.com.

5. Input clock slew rate of 3.0 V/ns used for jitter measurements.

Table 5.9.	Thermal	Characteristics
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Parameter	Symbol	Test Condition <sup>1</sup>	Value	Units
Si53350 – 48 QFN				
		Still Air	12 <sup>2</sup>	
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Air Flow 1 m/s	9.7 <sup>2</sup>	
		Air Flow 2 m/s	8.7 <sup>2</sup>	
Thermal Resistance, Junction to Case	θ <sub>JC</sub>		2.2 <sup>2</sup>	°C/W
Thermal Desistance, Junction to Desire	θ <sub>JB</sub>		3.6	
Thermal Resistance, Junction to Board	ΨJB		3.2 <sup>2</sup>	
Thermal Resistance, Junction to Top Center	ΨJT		0.4 <sup>2</sup>	
Si53258 – 40 QFN				
	θ <sub>JA</sub>	Still Air	23.1 <sup>1</sup>	-
Thermal Resistance, Junction to Ambient		Air Flow 1 m/s	17.5 <sup>1</sup>	
		Air Flow 2 m/s	16.5 <sup>1</sup>	
Thermal Resistance, Junction to Case	θ <sub>JC</sub>		13.4 <sup>1</sup>	°C/W
	θ <sub>JB</sub>		8.7 <sup>1</sup>	
Thermal Resistance, Junction to Board	Ψјв		8.4 <sup>1</sup>	
Thermal Resistance, Junction to Top Center	ΨJT		0.3 <sup>1</sup>	
Si53254 — 32 QFN				
		Still Air	28.4 <sup>1</sup>	
Thermal Resistance, Junction to Ambient	$\theta_{JA}$	Air Flow 1 m/s	24 <sup>1</sup>	-
		Air Flow 2 m/s	23 <sup>1</sup>	
Thermal Resistance, Junction to Case	θ <sub>JC</sub>		15.9 <sup>1</sup>	°C/W
Thermal Desistance, Junction to Desire	θ <sub>JB</sub>		11.5 <sup>1</sup>	
mermai Resistance, Junction to Board	ΨJB		11.2 <sup>1</sup>	
Thermal Resistance, Junction to Top Center	ΨJT		0.4 <sup>1</sup>	
Note: 1. Based on JEDEC standard 4-layer PCB. 2. Based on Si53350-D01-AM-QFN48-EVB (PCB of	dimensions: 9"x9",	PCB thickness: 0.062", nun	nber of PCB layers	: 8).

Parameter	Symbol	Test Condition	Value	Units
Storage Temperature Range	T <sub>STG</sub>		–55 to +150	°C
	V <sub>DD</sub>		–0.5 to 3.8	V
DC Supply Voltage	V <sub>DDA</sub>		-0.5 to 3.8	V
	V <sub>DDO</sub>		–0.5 to 3.8	V
Input Voltage Range	VI		-0.3 to 1.3	V
Latch-up Tolerance	LU		JESD78 Com	pliant
ESD Tolerance	HBM	100 pF, 1.5 kΩ	2.0	kV
	CDM		500	V
Junction Temperature	T <sub>JCT</sub>		–55 to 125	°C
Soldering Temperature	T <sub>PEAK</sub>		260	°C
Soldering Temperature Time at $T_{PEAK}$	T <sub>P</sub>		20 to 40	sec

#### Table 5.10. Absolute Maximum Ratings<sup>1,2,3</sup>

Notes:

1. Permanent device damage may occur if the absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. For more packaging information, go to www.silabs.com/support/quality/pages/RoHSInformation.aspx.

3. The device is compliant with JEDEC J-STD-020.

## 6. Pin Descriptions

#### 6.1 Si53350A-D01AM and Si53350BD12748-AM Pin Descriptions (48-QFN)



Figure 6.1. Si53350A-D01AM and Si53350BD12748-AM (48-QFN)

# Table 6.1. Si53350A-D01AM and Si53350BD12748-AM Pin Descriptions (48-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Ρ	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	Ι	Clock input 1. These pins accept both differential and single-ended clock
3	CLKIN_1b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be terminated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Ρ	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC		Do not connect these pipe to enuthing
6	NC		- Do not connect these pins to anything.
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock
8	CLKIN_2b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating.
0		D	Core Supply Voltage. Connect to 1.8–3.3 V.
9	VUDA	P	Must be connected to same voltage as VDD_DIG and VDD.
10	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 19. Refer-
11	Format_SEL1	I	once Section 3.2 Output Signal Formats. If using Si53350BD12748-AM, do not connect these pins to anything.
			Output Enable for OUT0 and OUT1
12	OEB[1:0]	I	0 = outputs enabled
			1 = outputs disabled
13	GND	Р	
14	GND	Р	
15	OUT0b	0	Output Clock 0
16	OUTO	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0
17	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
18	OUT1b	0	Output Clock
19	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1 and OUT2
20	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.

Pin Number	Pin Name	Pin Type	Function
21	OUT2b	0	Output Clock
22	OUT2	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Input clock selection pin.
23	Input_SEL	I	0 = CLKIN_1/CLKIN_1b
			1 = CLKIN_2/CLKIN_2b
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT3, OUT4, and OUT5
24	VDDO2	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
25	OUT3b	0	Output Clock
26	OUT3	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
27	OUT4b	0	Output Clock
28	OUT4	0	Desired output signal format is defined by IN/OUT_SEL0 and IN/ OUT_SEL1. Termination recommendations are provided in Section 3.2 Out- put Signal Formats. Unused outputs should be left unconnected
29	OUT5b	0	Output Clock
30	OUT5	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
31	OUT6b	0	Output Clock
32	OUT6	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
33	OUT7b	0	Output Clock
34	OUT7	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
35	OUT8b	0	Output Clock
36	OUT8	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT6, OUT7, and OUT8
37	VDDO3	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
			Output Enable for OUT2, OUT3, and OUT4
38	OEB[4:2]	I	0 = outputs enabled
			1 = outputs disabled

Pin Number	Pin Name	Pin Type	Function
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT9
39	VDDO4	Ρ	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
40	OUT9b	0	Output Clock
41	OUT9	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Output enable for OUT5, OUT6, and OUT7.
42	OEB[7:5]	I	0 = outputs enabled
			1 = outputs disabled
			Output enable for OUT8 and OUT9.
43	OEB[9:8]	I	0 = outputs enabled
			1 = outputs disabled
44	NC	_	
45	NC	_	
46	NC	_	Do not connect these pins to anything.
47	NC	_	
48	NC	_	
			Ground Pad
49	Ground	GND	This pad provides electrical and thermal connection to ground and must be connected for proper operation.



Notes: 1. Internal 100 kohm pull-down.



Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Р	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock
3	CLKIN_1b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Р	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC		Do not connect these pipe to envithing
6	NC	—	
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock
8	CLKIN_2b	I	signals. Refer to Section 3.4 Universal Hardware input Pins - input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating.
0		P	Core Supply Voltage. Connect to 1.8–3.3 V.
9	VDDA	P	Must be connected to same voltage as VDD_DIG.
10	Universal1	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
11	Universal2	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
12	Universal3	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
13	GND	Р	Connect these pipe to Cround
14	GND	Р	
15	OUT0b	0	Output Clock
16	OUT0	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT0
17	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
18	OUT1b	0	Output Clock
19	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.

# Table 6.2. Si53350BDxxxxx-AM Pin Descriptions (48-QFN)

Pin Number	Pin Name	Pin Type	Function
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT1 and OUT2
20	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
21	OUT2b	0	Output Clock
22	OUT2	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
23	Universal4	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT3, OUT4, and OUT5
24	VDDO2	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
25	OUT3b	0	Output Clock
26	OUT3	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
27	OUT4b	0	Output Clock
28	OUT4	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
29	OUT5b	0	Output Clock
30	OUT5	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
31	OUT6b	0	Output Clock
32	OUT6	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
33	OUT7b	0	Output Clock
34	OUT7	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
35	OUT8b	0	Output Clock
36	OUT8	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT6, OUT7, and OUT8
37	VDDO3	Ρ	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
38	Universal5	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.

Pin Number	Pin Name	Pin Type	Function
			Supply Voltage (1.8–3.3 V, or 1.5 V for CMOS only) for OUT9
39	VDDO4	Ρ	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
40	OUT9b	0	Output Clock
41	OUT9	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
42	Universal6	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
43	Universal7	I	Universal HW Input pin. This hardware input pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware input pins can be used for.
44	NC	_	
45	NC	_	
46	NC	_	Do not connect these pins to anything.
47	NC	_	
48	NC	_	
			Ground Pad
49	Ground	GND	This pad provides electrical and thermal connection to ground and must be connected for proper operation.

## 6.3 Si53358A-D01AM and Si53352BD12749-AM Pin Descriptions (40-QFN)



Figure 6.3. Si53358A-D01AM and Si53352BD12749-AM (40-QFN)

# Table 6.3. Si53358A-D01AM and Si53352BD12749-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Р	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock
3	CLKIN_1b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Р	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC		
6	NC		- Do not connect these pins to anything.
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock
8	CLKIN_2b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating.
Q	νρρα	P	Core Supply Voltage. Connect to 1.8–3.3 V.
9	VDDA	Г	Must be connected to same voltage as VDD_DIG and VDD.
10	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 19. Reference Section 3.2 Output Signal Formats. If using Si53350BD12749-AM, do not connect this pin to anything.
11	GND	Р	Connect these pipe to ground
12	GND	Р	
13	OUT0b	0	Output Clock
14	OUTO	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
			Supply Voltage (1.8–3.3 V) for OUT0
15	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	0	Output Clock
17	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
			Supply Voltage (1.8–3.3 V) for OUT1
18	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Format_SEL1	I	Output clock format selection pin. Used in conjunction with Pin 10. Reference Section 3.2 Output Signal Formats. If using Si53350BD12749-AM, do not connect this pin to anything.

## Si53350/58/54/52 Data Sheet Pin Descriptions

Pin Number	Pin Name	Pin Type	Function
			Input clock selection pin.
20	Input_SEL	I	0 = CLKIN_1/CLKIN_1b
			1 = CLKIN_2/CLKIN_2b
21	OUT2b	0	Output Clock
22	OUT2	Ο	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
23	OUT3b	0	Output Clock
24	OUT3	Ο	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
			Supply Voltage (1.8–3.3 V) for OUT2 and OUT3
25	VDDO2	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	0	Output Clock
27	OUT4	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
			Supply Voltage (1.8–3.3 V) for OUT4 and OUT5
28	VDDO3	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	0	Output Clock
30	OUT5	Ο	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
			Output Enable for OUT0 and OUT1
31	OEb_OUT[1:0]	I	0 = outputs enabled
			1 = outputs disabled
			Output Enable for OUT2 and OUT3
32	OEb_OUT[3:2]	I	0 = outputs enabled
			1 = outputs disabled
			Supply Voltage (1.8–3.3 V) for OUT6
33	VDDO4	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	0	Output Clock
35	OUT6	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected

Si53350/58/54/52 Data Sheet Pin Descriptions

Pin Number	Pin Name	Pin Type	Function
			Output Enable for OUT4 and OUT5
36	OEb_OUT[5:4]	I	0 = outputs enabled
			1 = outputs disabled
			Output Enable for OUT6 and OUT7
37	OEb_OUT[7:6]	I	0 = outputs enabled
			1 = outputs disabled
38	OUT7b	0	Output Clock
39	OUT7	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected
			Supply Voltage (1.8–3.3 V) for OUT7
40	VDDO5	Ρ	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
			Ground Pad
41	Ground	GND	This pad provides electrical and thermal connection to ground and must be connected for proper operation.

## 6.4 Si53358BDxxxxx-AM Pin Descriptions (40-QFN)



Figure 6.4. Si53358Bxxxxx-AM 40-QFN

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Р	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock
3	CLKIN_1b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Р	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC		Do not connect these pipe to envithing
6	NC	_	- Do not connect these pins to anything.
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock
8	CLKIN_2b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
0		P	Core Supply Voltage. Connect to 1.8–3.3 V.
9	VDDA	P	Must be connected to same voltage as VDD_DIG.
10	Universal1	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
11	GND	Р	
12	GND	Р	Connect these pins to ground.
13	OUT0b	0	Output Clock
14	OUTO	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT0
15	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	0	Output Clock
17	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT1
18	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Universal2	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of defini- tions that hardware pins can be used for.

# Table 6.4. Si53358BDxxxxx-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
20	Universal3	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
21	OUT2b	0	Output Clock
22	OUT2	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
23	OUT3b	0	Output Clock
24	OUT3	Ο	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT2 and OUT3
25	VDDO2	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	OUT4b	0	Output Clock
27	OUT4	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT4 and OUT5
28	VDDO3	Ρ	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
29	OUT5b	0	Output Clock
30	OUT5	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
31	Universal4	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
32	Universal5	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
			Supply Voltage (1.8–3.3 V) for OUT6
33	VDDO4	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
34	OUT6b	0	Output Clock
35	OUT6	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
36	Universal6	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of defini- tions that hardware pins can be used for.
37	Universal7	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.

Pin Number	Pin Name	Pin Type	Function
38	OUT7b	0	Output Clock
39	OUT7	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
40	VDDO5	Ρ	Supply Voltage (1.8–3.3 V) for OUT7 Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
41	Ground	GND	Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation.

## 6.5 Si53354A-D01AM and Si53354BD12750-AM Pin Descriptions (40-QFN)



Figure 6.5. Si53354A-D01AM and Si53354BD12750-AM (40-QFN)

# Table 6.5. Si53354A-D01AM and Si53354BD12750-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Ρ	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	Ι	Clock input 1. These pins accept both differential and single-ended clock
3	CLKIN_1b	I	signals. Refer to Section 3.4 Universal Hardware input Pins - input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Р	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC		Do not connect these pipe to anything
6	NC		- Do not connect these pins to anything.
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock
8	CLKIN_2b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
0		D	Core Supply Voltage. Connect to 1.8–3.3 V.
9	VDDA	F	Must be connected to same voltage as VDD_DIG and VDD.
10	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 19. Reference Section 3.2 Output Signal Formats. If using Si53350BD12750-AM, do not connect this pin to anything.
11	GND	Р	
12	GND	Р	Connect these pins to ground.
13	OUT0b	0	Output Clock
14	OUTO	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT0
15	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	0	Output Clock
17	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT1
18	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Format_SEL1	I	Output clock format selection pin. Used in conjunction with Pin 10. Reference Section 3.2 Output Signal Formats. If using Si53350BD12750-AM, do not connect this pin to anything.

## Si53350/58/54/52 Data Sheet Pin Descriptions

Pin Number	Pin Name	Pin Type	Function
			Input clock selection pin.
20	Input_SEL	I	0 = CLKIN_1/CLKIN_1b
			1 = CLKIN_2/CLKIN_2b
21	OUT2b	0	Output Clock
22	OUT2	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
23	OUT3b	0	Output Clock
24	OUT3	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT2 and OUT3
25	VDDO2	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	NC	_	Do not connect these pips to anything
27	NC	_	
28	NC		Do not connect these pins to anything.
29	NC		Do not connect these pips to anything
30	NC		
			Output enable for OUT0
31	OEb_OUT0	I	0 = output enabled
			1 = output disabled
			Output enable for OUT1
32	OEb_OUT1	I	0 = output enabled
			1 = output disabled
33	NC	_	Do not connect these pins to anything.
34	NC	_	- Do not connect these pins to anything
35	NC	_	
			Output enable for OUT2
36	OEb_OUT2	I	0 = output enabled
			1 = output disabled
			Output enable for OUT3
37	OEb_OUT3	I	0 = output enabled
			1 = output disabled
38	NC		Do not connect these pins to anything
39	NC		
40	NC	_	Do not connect these pins to anything.

Pin Number	Pin Name	Pin Type	Function
41	Ground	GND	<b>Ground Pad</b> This pad provides electrical and thermal connection to ground and must be connected for proper operation.

## 6.6 Si53354BDxxxxx-AM Pin Descriptions (40-QFN)



Figure 6.6. Si53354BDxxxxx-AM 40-QFN

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Р	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD.
2	CLKIN_1	I	Clock input 1. These pins accept both differential and single-ended clock
3	CLKIN_1b	I	signals. Refer to Section 3.4 Universal Hardware input Pins - input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Р	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pips to anything
6	NC	_	
7	CLKIN_2	I	Clock input 2. These pins accept both differential and single-ended clock
8	CLKIN_2b	I	signals. Refer to Section 3.4 Universal Hardware Input Pins - Input_SEL for input termination options. These pins are high-impedance and must be ter- minated externally. If both the CLKIN_2 and CLKIN_2b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
0			Core Supply Voltage. Connect to 1.8–3.3 V.
9	VDDA	F	Must be connected to same voltage as VDD_DIG.
10	Universal1	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
11	GND	Р	
12	GND	Р	- Connect these pins to ground.
13	OUT0b	0	Output Clock
14	OUT0	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT0
15	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
16	OUT1b	0	Output Clock
17	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT1
18	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
19	Universal2	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of defini- tions that hardware pins can be used for.

# Table 6.6. Si53354BDxxxxx-AM Pin Descriptions (40-QFN)

Pin Number	Pin Name	Pin Type	Function
20	Universal3	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
21	OUT2b	0	Output Clock
22	OUT2	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
23	OUT3b	0	Output Clock
24	OUT3	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT2 and OUT3
25	VDDO2	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
26	NC		
27	NC		
28	NC		Do not connect these pins to anything.
29	NC		
30	NC	_	
31	Universal4	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
32	Universal5	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
33	NC		
34	NC	_	Do not connect these pins to anything.
35	NC	_	
36	Universal6	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
37	Universal7	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
38	NC	_	
39	NC		Do not connect these pins to anything.
40	NC		
			Ground Pad
41	Ground	GND	This pad provides electrical and thermal connection to ground and must be connected for proper operation.

#### 6.7 Si53352A-D01AM and Si53352BD12751-AM Pin Descriptions (32-QFN)



## Figure 6.7. Si53352A-D01AM and Si53352BD12751-AM (32-QFN)

# Table 6.7. Si53352A-D01AM and Si53352BD12751-AM Pin Descriptions (32-QFN)

Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Р	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA.
2	CLKIN	I	Clock input. These pins accept both differential and single-ended clock sig-
3	CLKINb	I	nais. Refer to Section 3.4 Universal Hardware input Pins - Input_SEL for in- put termination options. These pins are high-impedance and must be termi- nated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Ρ	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC	—	Do not connect these pips to anything
6	NC		bo not connect these pins to anything.
7	VDDA	Р	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
8	NC		Do not connect this pin to anything.
9	GND	Р	Connect these pips to ground
10	GND	Р	

Pin Number	Pin Name	Pin Type	Function	
11	OUT0b	0	Output Clock	
12	OUT0	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected	
			Supply Voltage (1.8–3.3 V) for OUT0	
13	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.	
14	OUT1b	0	Output Clock	
15	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected	
			Supply Voltage (1.8–3.3 V) for OUT1	
16	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate op- tion is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.	
17	Format_SEL0	I	Output clock format selection pin. Used in conjunction with Pin 17. Reference Section 3.2 Output Signal Formats. If using Si53350BD12751-AM, do not connect this pin to anything.	
18	NC	_		
19	NC			
20	NC	_	Do not connect these pipe to entitling	
21	NC		- Do not connect these pins to anything.	
22	NC	_		
23	NC			
24	Format_SEL1	I	Output clock format selection pin. Used in conjunction with Pin 8. Reference Section 3.2 Output Signal Formats. If using Si53350BD12751-AM, do not connect this pin to anything.	
25	NC			
26	NC	—	Do not connect these pins to anything.	
27	NC			
			Output enable for OUT0	
28	OEb_OUT0	I	0 = output enabled	
			1 = output disabled	
			Output enable for OUT1	
29	OEb_OUT1	I	0 = output enabled	
			1 = output disabled	
30	NC	—		
31	NC		Do not connect these pins to anything.	
32	NC			

Pin Number	Pin Name	Pin Type	Function
33	Ground	GND	Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation.



Figure 6.8. Si53352A-Dxxxxx-AM 32-QFN



Pin Number	Pin Name	Pin Type	Function
1	VDD_DIG	Р	Voltage supply for digital functions. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA.
2	CLKIN	I	Clock input. These pins accept both differential and single-ended clock sig-
3	CLKINb	I	nais. Refer to Section 3.4 Universal Hardware input Pins - Input_SEL for in- put termination options. These pins are high-impedance and must be termi- nated externally. If both the CLKIN_1 and CLKIN_1b inputs are unused and powered down, then both inputs can be left floating. ClockBuilder Pro will power down an input that is set as "Unused".
4	VDD	Р	Voltage supply. Connect to 1.8–3.3 V. Part of internal core VDD voltage. Must be connected to same voltage as VDDA and VDD_DIG.
5	NC		Do not connect these pipe to anything
6	NC		- Do hot connect these phils to anything.
7	VDDA	Р	Core Supply Voltage. Connect to 1.8–3.3 V. Must be connected to same voltage as VDD_DIG and VDD.
8	Universal1	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.

Pin Number	Pin Name	Pin Type	Function
9	GND	Р	
10	GND	Р	Connect these pins to ground.
11	OUT0b	0	Output Clock
12	OUTO	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT0
13	VDDO0	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
14	OUT1b	0	Output Clock
15	OUT1	0	These output clocks support a programmable signal swing and common mode voltage. Termination recommendations are provided in Section 3.2 Output Signal Formats. Unused outputs should be left unconnected.
			Supply Voltage (1.8–3.3 V) for OUT1
16	VDDO1	Р	Leave VDDOx pins of unused output drivers unconnected. An alternate option is to connect the VDDOx pin to a power supply and disable the output driver to minimize current consumption.
17	Universal2	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
18	NC		
19	NC		
20	NC		
21	NC		Do not connect these pins to anything.
22	NC		
23	NC		
24	Universal3	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
25	NC		
26	NC		Do not connect these pins to anything.
27	NC		
28	Universal4	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
29	Universal5	I	Universal HW pin. This hardware pin is user definable through ClockBuilder Pro. Refer to Section 3.4 Universal Hardware Input Pins for a list of definitions that hardware pins can be used for.
30	NC		
31	NC	_	Do not connect these pins to anything.
32	NC		

Pin Number	Pin Name	Pin Type	Function
33	Ground	GND	Ground Pad This pad provides electrical and thermal connection to ground and must be connected for proper operation.

# 7. Package Outline

## 7.1 7x7 mm 48-QFN Package Diagram

The figure below illustrates the package details for 48-QFN. The table below lists the values for the dimensions shown in the illustration.





## Table 7.1. Package Dimensions

Dimension	Min	Nom	Мах
А	0.80	0.85	0.90
A1	00	0.035	0.05
A2		0.65	0.67
A3	0.203 REF		
b	0.20	0.25	0.30
D		7 BSC	

Dimension	Min	Nom	Мах
E		7 BSC	
e		0.5 BSC	
J	5.55	5.65	5.75
К	5.55	5.65	5.75
L	0.35	0.40	0.45
ааа	0.10		
bbb	0.10		
CCC	0.08		
ddd	0.10		
eee		0.10	

## Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensions and Tolerances per ANSI Y14.5M-1994.

3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VLLD-5

4. Recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

#### 7.2 6x6 mm 40-QFN Package Diagram

The figure below illustrates the package details for 40-QFN. The table below lists the values for the dimensions shown in the illustration.



Figure 7.2. 40-Pin Quad Flat No-Lead (QFN)

Table 7.2.	Package	Dimensions
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Dimension	Min	Nom	Мах
А	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC	
D2	4.35	4.50	4.65
e		0.50 BSC	
E	6.00 BSC		
E2	4.35	4.50	4.65
L	0.30	0.40	0.50
ааа	—	—	0.15
bbb	—	—	0.15
ссс	—	—	0.08
ddd	—	—	0.10
eee			0.05

#### Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensions and Tolerances per ANSI Y14.5M-1994.

3. This drawing conforms to the JEDEC Solid State Outline MO-220.

4. Recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 7.3 5x5 mm 32-QFN Package Diagram

The figure below illustrates the package details for 32-QFN option. The table below lists the values for the dimensions shown in the illustration.







Dimension	MIN	NOM	МАХ
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.20 REF	
b	0.18	0.25	0.30
D/E	4.90	5.00	5.10
D2/E2	3.40	3.50	3.60
e		0.50 BSC	
L	0.30	0.40	0.50
К	0.20		
R	0.09		0.14
ааа	0.15		
bbb		0.10	
CCC		0.10	

Dimension	MIN	NOM	МАХ
ddd		0.05	
eee		0.08	
fff		0.10	

## Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. Dimensions and Tolerances per ANSI Y14.5M-1994.

3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VKKD-4.

4. Recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 8. PCB Land Pattern

## 8.1 48-QFN Land Pattern



Figure 8.1. 48-QFN Land Pattern

## Table 8.1. PCB Land Pattern Dimensions

Dimension	MIN	ТҮР	МАХ
C1	6.05	6.15	6.25
C2	6.05	6.15	6.25
e	0.50 BSC		
X1	0.17	0.25	0.37
Y1	0.69	0.8	0.89
X2	5.65	5.75	5.85
Y2	5.65	5.75	5.85

## Notes:

## General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.

2. This Land Pattern Design is based on the IPC-7351 guidelines.

#### Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

## Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.

2. The stencil thickness should be 0.125 mm (5 mils).

3. The ratio of stencil aperture to land pad size can be 1:1 for all perimeter pads.

4. The stencil aperture to center land pad size recommendation is 70% paste coverage.

## Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.

2. The recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

#### 8.2 40-QFN Land Pattern







Dimension	mm
C1	5.90
C2	5.90
e	0.50 BSC
X1	0.30
Y1	0.85
X2	4.65
Y2	4.65

Dimension	mm	
Notes: General		
1. All dimensions shown are in millimeters (mm) unless otherwise	e noted.	
2. This Land Pattern Design is based on the IPC-7351 guidelines <b>Solder Mask Design</b>		
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.		
1 A stainless steel laser-cut and electro-polished stencil with tra	pezoidal walls should be used to assure good solder paste release	
2. The stencil thickness should be 0.125 mm (5 mils).		
3. The stencil aperture to center land pad size recommendation is	s 70% paste coverage.	
4. A 3×3 array of 0.85 mm square openings on a 1.00 mm pitch of	an be used for the center ground pad.	
Card Assembly		
1. A No-Clean, Type-3 solder paste is recommended.		

2. The recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

## 8.3 32-QFN Land Pattern

The figure below illustrates the PCB land pattern details for 32-QFN package. The table below lists the values for the dimensions shown in the illustration.





Table 8.3.	PCB Land	Pattern	Dimensions
------------	----------	---------	------------

Dimension	mm
C1	4.90
C2	4.90
е	0.50 BSC
X1	0.30
Y1	0.85
X2	3.60
Y2	3.60

Dimension	mm	
Notes: General		
1. All dimensions shown are in millimeters (mm) unless otherwise	e noted.	
2. This Land Pattern Design is based on the IPC-7351 guidelines <b>Solder Mask Design</b>		
1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.		
1 A stainless steel laser-cut and electro-polished stencil with tra	pezoidal walls should be used to assure good solder paste release	
2. The stencil thickness should be 0.125 mm (5 mils).		
3. The stencil aperture to center land pad size recommendation is	s 70% paste coverage.	
4. A 3×3 array of 0.85 mm square openings on a 1.00 mm pitch of	an be used for the center ground pad.	
Card Assembly		
1. A No-Clean, Type-3 solder paste is recommended.		

2. The recommended card re-flow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

# 9. Top Marking



Figure 9.1. Top Marking

Table 9.1. Top Marking Explanation

Line	Characters	Description	
1	Si53350		
	Si53358		
	Si53354	Base part number	
	Si53352		
47044	A = Product grade		
	R = Product revision (see Ordering Guide for current revision)		
	AR01A	01 = Device ID	
2	A = Automotive temperature range (-40 $^{\circ}$ C to +105 $^{\circ}$ C) and Package (QFN)		
		B = Product grade	
	BDxxxxx	R = Product revision (see Ordering Guide for current revision)	
		XXXXX = Customer specific NVM sequence number. NVM code assigned for custom, factory pre-programmed devices using ClockBuilder Pro.	
3	ттттт	Manufacturing trace code	
	ATTTTT	AM = Automotive temperature range (-40 °C to +105 °C) and Package (QFN)	
		TTTTTT = Manufacturing trace code	
4	YYWW	Year (YY) and work week (WW) of package assembly	

# **10. Document Change List**

#### **Revision 1.1**

March 2021

• Corrected Pin 8 and Pin10 descriptions in Table 6.7 Si53352A-D01AM and Si53352BD12751-AM Pin Descriptions (32-QFN) on page 45 to match the pinout diagram in Figure 6.7 Si53352A-D01AM and Si53352BD12751-AM (32-QFN) on page 45.

## **Revision 1.0**

January 2021

- Added 10-output devices in 48-QFN.
- · Updated "Inputx" pin descriptions to "Universalx".
- Added AEC-Q100 qualified.
- · Added note not recommending use of LVCMOS in-phase, dual output drivers.
- · Added orderable part numbers supporting complementary LVCMOS output drivers.
- Switched Format\_SEL1 and Format\_SEL0 columns on the table in Section 3.2.

#### **Revision 0.7**

September 2019

· Initial release.

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