UG442: Non-Isolated Buck Evaluation Board for the Si3406

The Si3406 non-isolated Buck evaluation board is a reference design for a power supply in a Power over Ethernet (PoE) Powered Device (PD) application.

This Si3406-Buck EVB provides simple and low-cost solution with different output voltages and power levels.

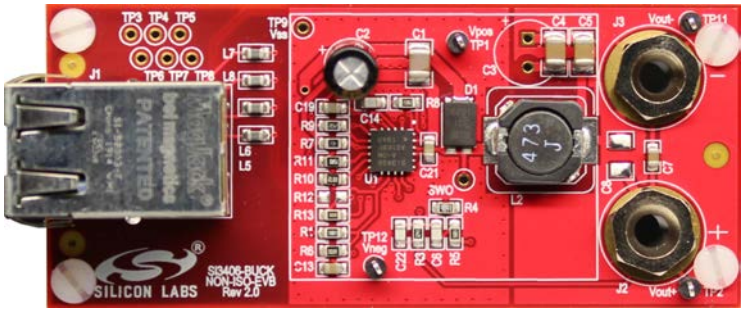
The Si3406-Buck-5V EVB board is shown below. The Si3406 IC integrates an IEEE 802.03at compatible PoE interface as well as a current control-based dc/dc converter.

The Si3406 PD integrates an internal rectifier bridge, detection circuit, classification circuit, dc/dc switch, hotswap switch, TVS overvoltage protection, dynamic soft-start circuit, cycle-by-cycle current limit, thermal shutdown, and inrush current protection.

The switching frequency is set to 220 kHz by installing R10 = 88.7 kΩ.

KEY FEATURES

- IEEE 802.03at compliant
- Very small application PCB surface
- High efficiency
- High integration
- Low-profile 4 x 4 mm 20-pin QFN
- Integrated diode bridge
- Integrated thermal shutdown protection
- Automatic and user mode MPS generation
- Integrated transient overvoltage protection



Parameter	Condition	Si3406-BUCK-3.3V	Si3406-BUCK-5V	Si3406-BUCK-12V	Si3406-BUCK-24V
PSE input voltage range	Connector J1	37 V to 57 V			
PoE Type/Class	IEEE 802.3at	Type 1/Class 2			
Output Voltage / Current	Connectors J2-J3	3.3 V* / 2.1 A	5 V / 1.4 A	12 V / 0.583 A	24 V / 0.291 A
Efficiency, End-to-End	VIN = 50 V, internal bridge	72.03 %	77.98 %	85.14 %	88.36 %
Switching frequency	RFREQ (R10) = 88.7 kΩ	220 kHz			
Conducted EMI	EN55032, average detector	Passed			
Conducted EMI	EN55032, peak detector	Passed			
Radiated EMI	EN55032 Class B	Passed			

***Note:** 3.3 V Buck designs using internal diode bridge are limited to 70 °C ambient due to the increased thermal rise. For 3.3 V Buck designs targeting a maximum ambient of 85 °C, an external diode bridge should be used.

Table of Contents

1. Selector Guide

The minimum possible output voltage of this evaluation board is 3.3 V, the maximum possible output voltage is 24 V.

This user guide presents 4 different output voltages: 3.3 V, 5 V, 12 V and 24 V.

The maximum power is 7 W and limited by the internal rectifier bridge, while the efficiency of the EVB highly depends on the output voltage. Higher output voltage configurations tend to have higher efficiency, meanwhile, lower output voltage configurations have lower efficiency.

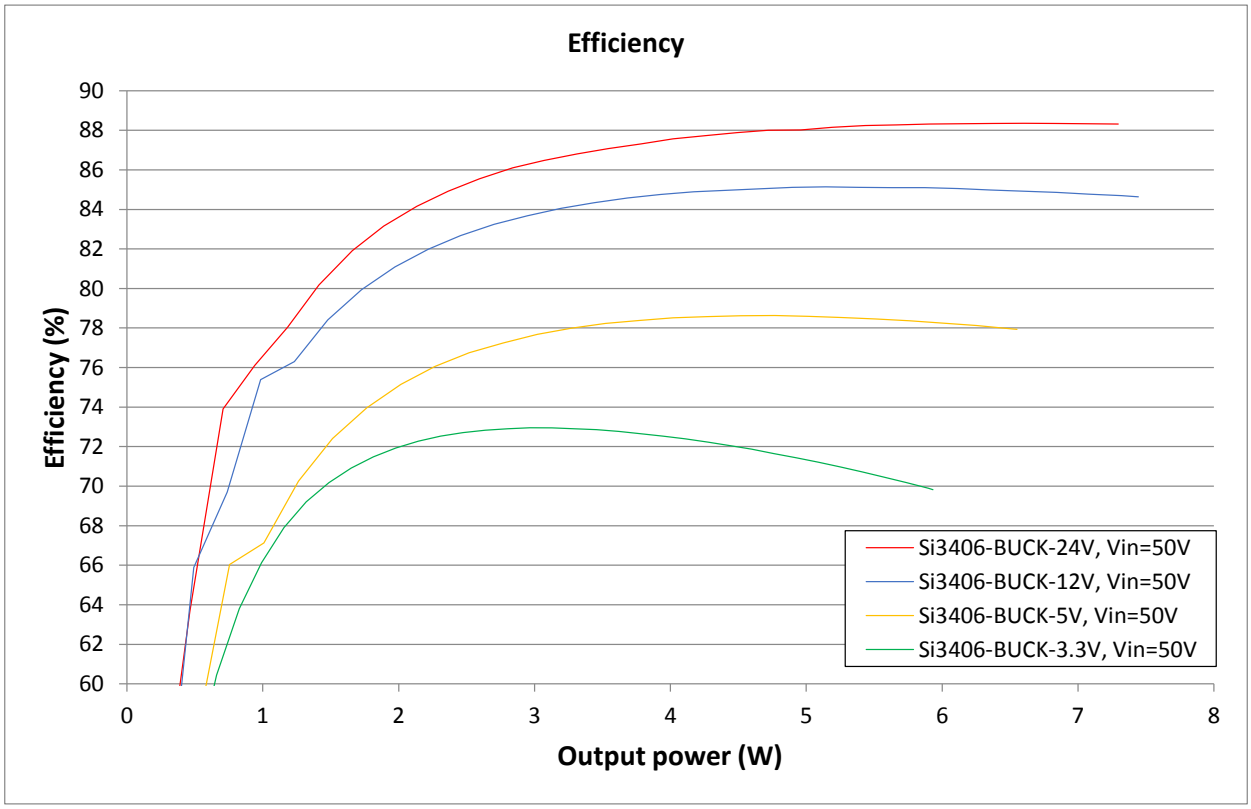


Figure 1.1. Si3406-Buck Non-Isolated EVB End-to-End Efficiency of Different Configurations: 50 V Input

Note: The chart shows the end-to-end EVB efficiency, where voltage drop on the diode bridge is included and LEDs are removed.

The standard Si3406-Buck-5V EVB is shown on the cover page. This document includes complete schematics and measurement data for the below 4 different output voltages:

- Si3406-Buck-3.3V-7W – Class 2
- Si3406-Buck-5V-7W – Class 2
- Si3406-Buck-12V-7W – Class 2
- Si3406-Buck-24V-7W – Class 2

The parts in red on the schematics represent the BOM differences between the four designs

On the board, the internal diode bridges are used as rectifier bridges. See the figure above for overall conversion efficiency results. The recommended detection resistor value is listed in the following table

Table 1.1. Recommended Detection Resistor Values

Diode Bridge	R_{DET}
Internal	24.3 kΩ

2. Powering up the Si3406-Buck Board

Ethernet data and power are applied to the board through the RJ45 connector (J1). The board itself has no Ethernet data transmission functionality, but, as a convenience, the Ethernet with secondary-side data is brought out to test points.

The design can be used in Gigabit (10/100/1000) systems as well by using PoE RJ45 Magjack, such as type L8BE-1G1T-BFH from Bel Fuse.

Power may be applied in the following ways:

- Using an any IEEE 802.3-2015-compliant, PoE-capable PSE, or
- Using a laboratory power supply unit (PSU):
  - Connecting a dc source between blue/white-blue and brown/white-brown of the Ethernet cable (either polarity), (End-span) as shown below:

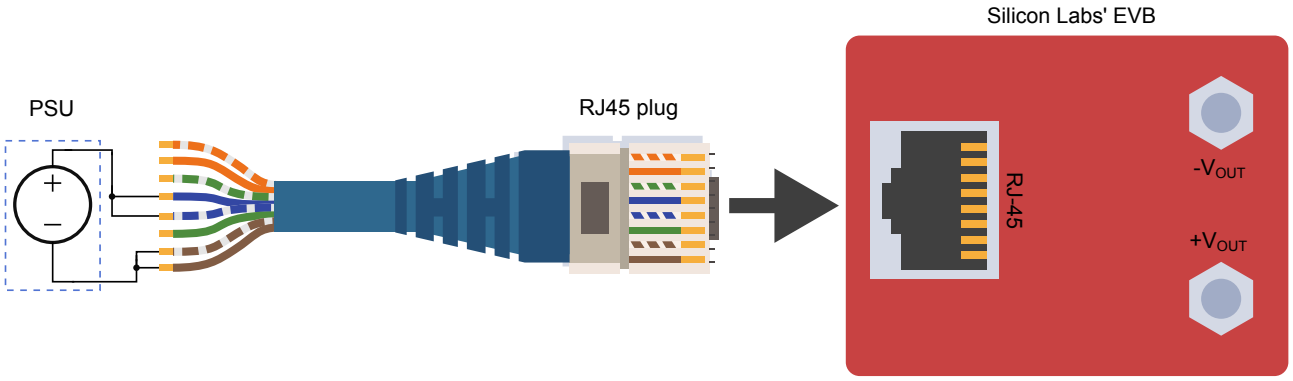


Figure 2.1. Endspan Connection using Laboratory Power Supply

  - Connecting a dc source between green/white-green and orange/white-orange of the Ethernet cable (either polarity), (Mid-span) as shown below:

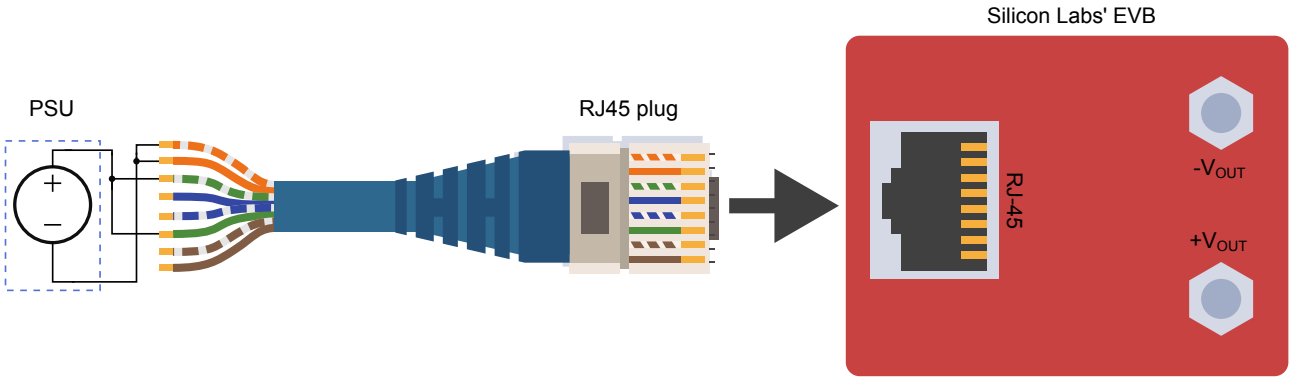


Figure 2.2. Midspan Connection using Laboratory Power Supply

3. Si3406 BOM Variants

3.1 Si3406-Buck EVB

The Si3406-BUCK EVB comes in a 5 V/7 W configuration. To change the EVB to other voltage levels, a few components must be replaced on the EVB. These are summarized in the following table.

Table 3.1. Si3406-Buck-5V / 7W Non-Isolated EVB BOM Changes for Different Voltage Levels

24 V									
Qty	**Ref**	**Value**	**Rating**	**Voltage**	**Tol**	**Type**	**PCB Footprint**	**Mfr Part Number**	**Mfr**
1	C14	1 nF		50 V	±1%	C0G	C0805	C0805C0G500-102F	Venkel
3	C4, C5, C8	22 µF		25 V	±10%	X7R	C1210	C1210X7R250-226M	Venkel
1	C7	1 µF		50 V	±10%	X7R	C0805	CL21B105KBFNNNE	Samsung
1	D1	PDS3100	3 A	100 V		Schottky	POWERDI-5	PDS3100-13	Diodes Inc.
1	L2	470 µH	0.43 A		±10%	Shielded	IND-MSS1038	MSS1048-474KL	Coilcraft
1	R1	7.5 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-7501F	Venkel
1	R3	1.37 kΩ	1/10 W		±0.1%	±25 PPM	R0805	TFCR0805-10W-E-1371B	Venkel
1	R4	23.7 kΩ	1/10 W		±0.1%	±25 PPM	R0805	TFCR0805-10W-E-2372B	Venkel
1	R8	100 kΩ	1/8 W		±1%	Thick Film	R0805	CR0805-8W-1003F	Venkel
Not Installed Components									
1	C22	200 pF		50 V	±1%	C0G	C0805	C0805C0G500-201FNE	Venkel
1	C6	39 pF		25 V	±1%	C0G	C0805	C0805C0G250-390FNP	Venkel
12 V									
Qty	**Ref**	**Value**	**Rating**	**Voltage**	**Tol**	**Type**	**PCB Footprint**	**Mfr Part Number**	**Mfr**
1	C14	470 pF		50 V	±1%	C0G	C0805	C0805C0G500-471F	Venkel
1	C22	430 pF		50 V	±2%	C0G	C0805	C0805C0G500-431GNP	Venkel
1	C4	47 µF		16 V	±20%	X5R	C1210	C1210X5R160-476MNE	Venkel
1	C6	220 pF		50 V	±1%	C0G	C0805	C0805C0G500-221FNE	Venkel
1	C7	10 µF		16 V	±10%	X5R	C0805	C0805X5R160-106K	Venkel
1	D1	PDS3100	3 A	100 V		Schottky	POWERDI-5	PDS3100-13	Diodes Inc.
1	L2	180 µH	0.75 A		±10%	Shielded	IND-MSS1038	MSS1048-184KL	Coilcraft
1	R1	3.24 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW08053K24FKEA	Vishay
1	R3	1.1 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1101F	Venkel
1	R4	9.09 kΩ	1/10 W		±0.5%	±25 PPM	R0805	RR1220P-9091-D-M	Susumu
1	R8	100 kΩ	1/8 W		±1%	Thick Film	R0805	CR0805-8W-1003F	Venkel
Not Installed Components									
2	C5, C8	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel

3.3 V									
Qty	**Ref**	**Value**	**Rating**	**Voltage**	**Tol**	**Type**	**PCB Footprint**	**Mfr Part Number**	**Mfr**
1	C14	330 pF		50 V	±1%	C0G	C0805	C0805C0G500-331F	Venkel
3	C4, C5, C8	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
1	C7	22 µF		6.3 V	±20%	X5R	C0805	C0805X5R6R3-226M	Venkel
1	D1	SDT5H100P5	5 A	100 V		Schottky	POWERDI-5	SDT5H100P5-7	Diodes Inc.
1	L2	100 µH	2.8 A		±20%	Shielded	IND-MSS1278	MSS1278-104ML	Coilcraft
1	R1	475	1/8 W		±1%	ThickFilm	R0805	CR0805-8W-4750FT	Venkel
1	R3	3.24 kΩ	1/8 W		±1%	ThickFilm	R0805	CRCW08053K24FKEA	Vishay
1	R4	4.87 kΩ	1/8 W		±1%	ThickFilm	R0805	RC0805FR-074K87L	Yageo
1	R8	210 kΩ	1/10 W		±1%	ThickFilm	R0805	CR0805-10W-2103F	Venkel
Not Installed Components									
1	C22	200 pF		50 V	±1%	C0G	C0805	C0805C0G500-201FNE	Venkel
1	C6	39 pF		25 V	±1%	C0G	C0805	C0805C0G250-390FNP	Venkel

4. Si3406-Buck EVB: 3.3 V, Class 2 Configuration

4.1 Si3406-Buck EVB Schematic: 3.3 V, Class 2, 7 W

The figure below shows the schematic of the Si3406-Buck 3.3 V, Class 2 EVB. The parts in red on the schematic represent the BOM differences compared to the core design.

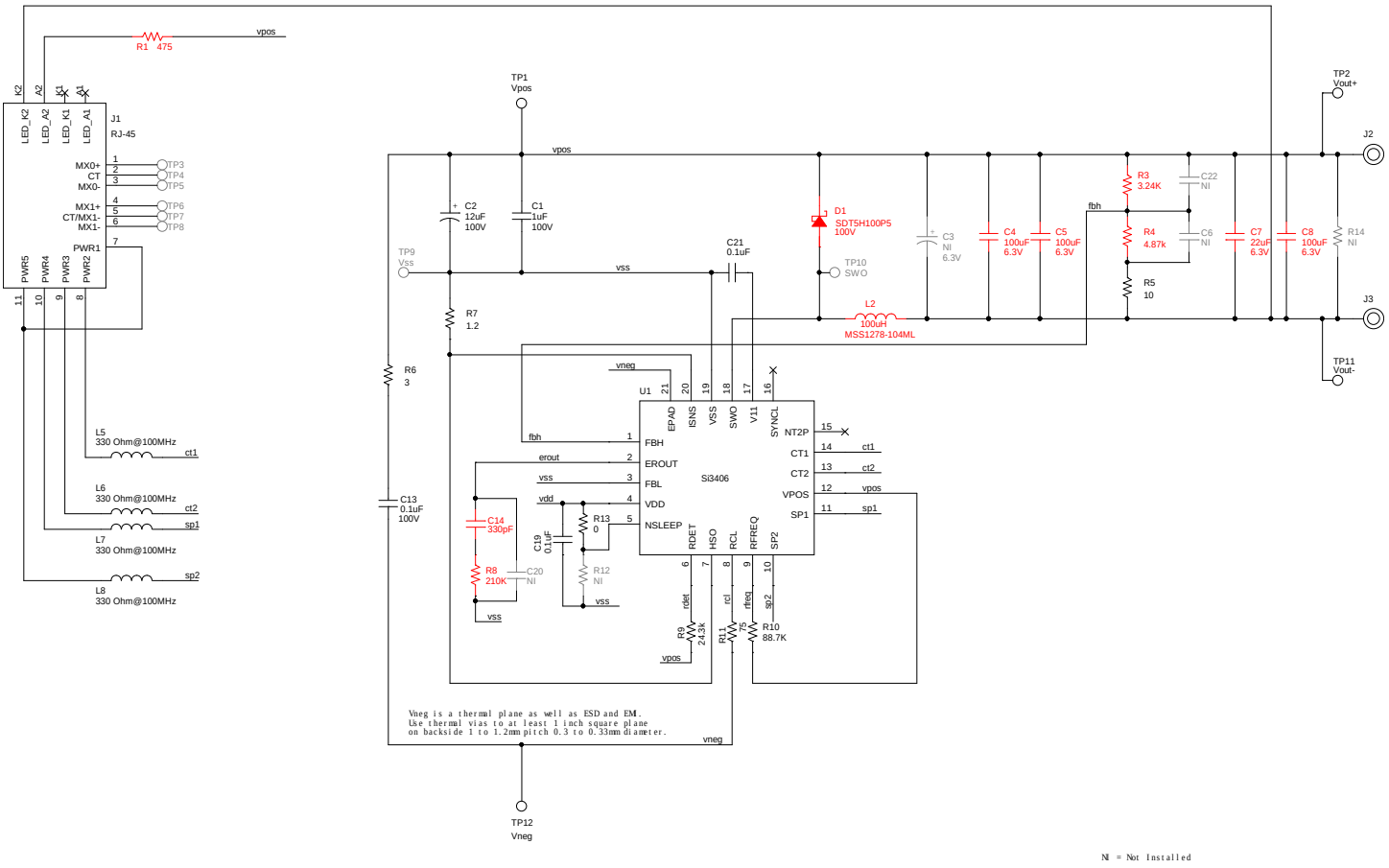


Figure 4.1. Si3406 Buck Non-Isolated EVB Schematic: 3.3 V, Class 2 PD, 7 W

4.2 End-to-End EVB Efficiency

The end-to-end conversion efficiency measurement data of the Si3406 3.3V Buck board is shown below with internal input bridges. The efficiency was measured at three different input voltage levels: 42 V, 50 V and 57 V.

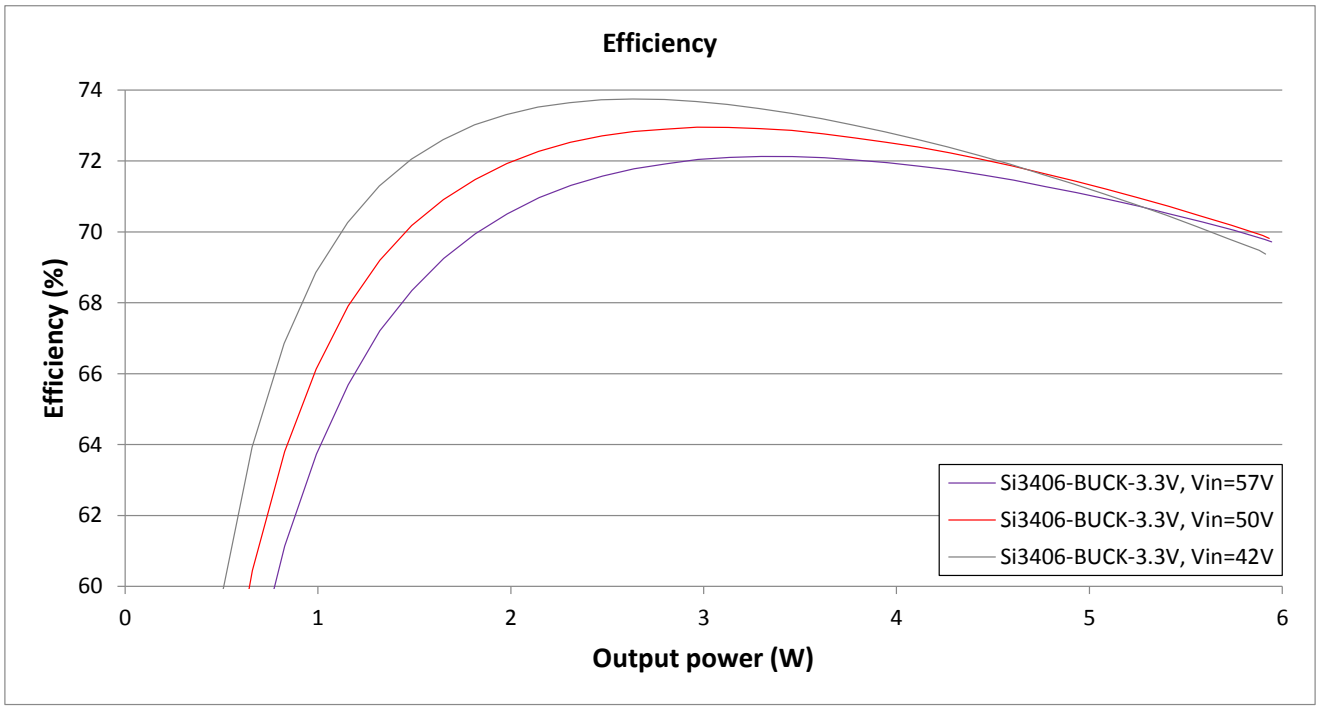


Figure 4.2. Si3406-Buck End-to-End Efficiency Chart with internal Diodes as Input Bridge: 42 V, 50 V and 57 V Input, 3.3 V Output, Class 2

Note: The chart shows end-to-end EVB efficiency. The voltage drop of the diode bridge is included. LEDs are removed.

4.3 Thermal Measurements

The Si3406-Buck EVB's temperature was measured at maximum **input power – 6.5 W**. The Si3406-Buck EVB is configured for 3.3 V output voltage and Class 2 power level. The following figure shows the thermal image taken of the top side of the PCB at maximum input power.

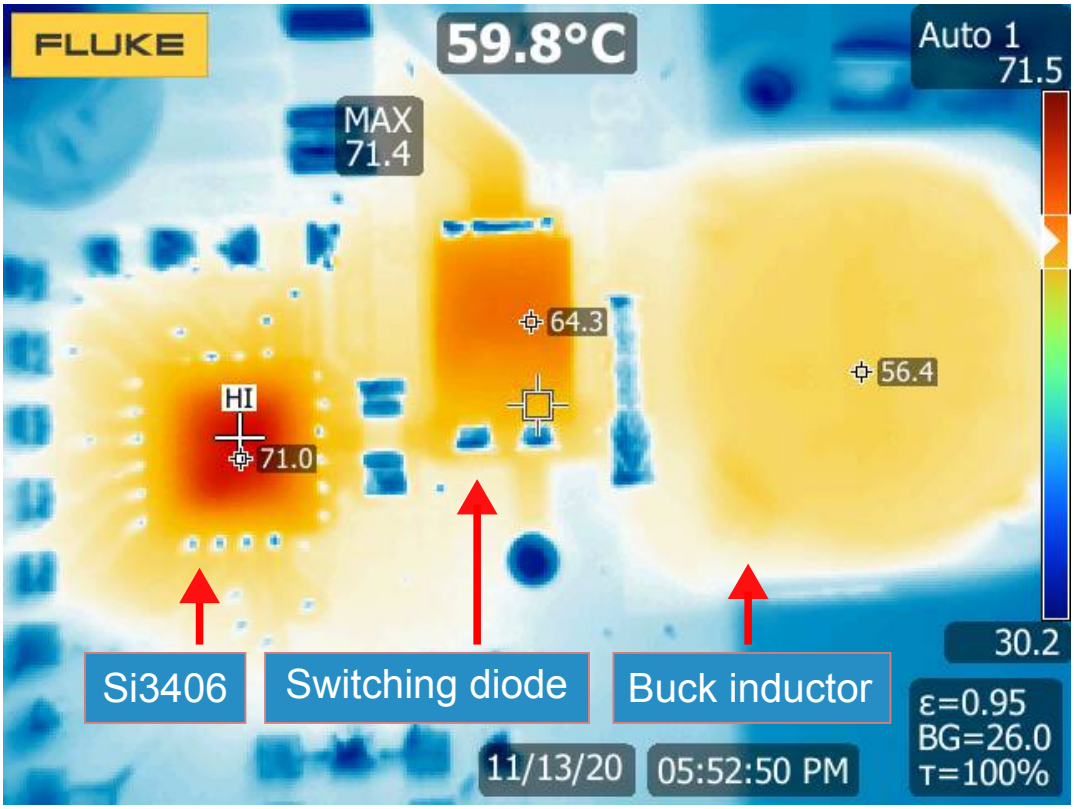


Figure 4.3. Thermal Measurements of the Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 PD

The following table lists the temperatures of the notable components across the board.

Table 4.1. Component Temperatures at Full Load

Component	Temperature
Si3406 – U1	71.4 °C
Switching Diode – D1	64.3 °C
Buck Inductor – L2	56.4 °C

Note:
1. The ambient temperature was 26 °C during the thermal measurements.

4.4 SIFOS PoE Compatibility Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices (PDs). The Si3406-Buck-3.3V EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies.

Table 4.2. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 PD SIFOS PoE Compatibility Test Results

ALT A MDI									
Detection and Classification		PSE Emulation		Pairs	A	Polarity	MDI	Det Cycles	3
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.53	kΩ	24.53	24.53	24.53	23.70	26.30	P
Rdet_final		24.51	kΩ	24.51	24.51	24.51	23.70	26.30	P
Rdet_unpwr		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin		24.48	kΩ	24.48	24.48	24.48	23.70	26.30	P
Rdet_at_Vmax		24.57	kΩ	24.57	24.57	24.57	23.70	26.30	P
Rdet_Voffset		1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification									
Iclass		18.4	mA	18.4	18.4	18.4	17.0	20.0	P
ClassNum		2		2	2	—	0	4	P
Tclass		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability		1					1	1	P
Iclass_at_Vmin		18.7	mA	18.7	18.7	18.7	17.0	20.0	P
Iclass_at_Vmax		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
2 Event Classification									
Iclass_event1		18.4	mA	18.4	18.4	18.4	17.0	20.0	P
Iclass_event2		18.4	mA	18.4	18.4	18.4	17.0	20.0	P
MarkI		1.58	mA	1.58	1.58	1.58	0.25	4.00	INFO
ClassNum2		2		2	2	—	0	4	P
Tclass_event1		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1		1					1	1	P
ClassStability_event2		1					1	1	P
Power-Up / Down									
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		155.8	mA	155.8	155.8	155.8	0.0	400.0	P
InrushI_2		156.6	mA	156.6	156.6	156.6	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P

Inrush_delayed	0		0	0	—	0	0	P
Von	37.2	VDC	37.2	37.2	37.2	30.0	42.0	P
Voff	33.1	VDC	33.1	33.1	33.1	30.0	42.0	P
Vhyst	4.0	VDC	4.0	4.0	4.0	0.0	12.0	P
BackfeedV	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	8.3	mA	8.3	8.3	8.3	0.0	174.2	P
MaxI_1	13.5	mA	13.5	13.5	13.5	10.0	174.2	P
Vport_1	48.0	VDC	48.0	48.0	48.0	37.0	57.0	INFO
Ppeak_1	0.65	W	0.65	0.65	0.65	0.0	8.4	P
Pavg_1	0.50	W	0.50	0.50	0.50	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	3.0	mA	3.0	3.0	3.0	0.0	154.7	P
MaxI_2	21.6	mA	21.6	21.6	21.6	10.0	154.7	P
Vport_2	54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2	1.17	W	1.17	1.17	1.17	0.0	8.4	P
Pavg_2	0.55	W	0.55	0.55	0.55	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT A MDI-X								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P
Rdet_final	24.51	kΩ	24.51	24.51	24.51	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.86	kΩ	24.86	24.86	24.86	23.70	26.30	P
Rdet_at_Vmax	24.65	kΩ	24.65	24.65	24.65	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P

Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.4	mA	18.4	18.4	18.4	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.3	mA	18.3	18.3	18.3	17.0	20.0	P
Iclass_at_Vmax	18.3	mA	18.3	18.3	18.3	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.4	mA	18.4	18.4	18.4	17.0	20.0	P
Iclass_event2	18.4	mA	18.4	18.4	18.4	17.0	20.0	P
MarkI	1.58	mA	1.58	1.58	1.58	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	155.8	mA	155.8	155.8	155.8	0.0	400.0	P
InrushI_2	156.6	mA	156.6	156.6	156.6	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.6	VDC	37.6	37.6	37.6	30.0	42.0	P
Voff	33.5	VDC	33.5	33.5	33.5	30.0	42.0	P
Vhyst	4.1	VDC	4.1	4.1	4.1	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	7.9	mA	7.9	7.9	7.9	0.0	172.9	P
MaxI_1	13.4	mA	13.4	13.4	13.4	10.0	172.9	P
Vport_1	48.3	VDC	48.3	48.3	48.3	37.0	57.0	INFO
Ppeak_1	0.65	W	0.65	0.65	0.65	0.0	8.4	P
Pavg_1	0.50	W	0.50	0.50	0.50	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P

DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.7	mA	2.7	2.7	2.7	0.0	153.9	P
MaxI_2	22.4	mA	22.4	22.4	22.4	10.0	153.9	P
Vport_2	54.4	VDC	54.4	54.4	54.4	42.5	57.0	INFO
Ppeak_2	1.22	W	1.22	1.22	1.22	0.0	8.4	P
Pavg_2	0.55	W	0.55	0.55	0.55	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT B MDI								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.40	kΩ	24.40	24.40	24.40	23.70	26.30	P
Rdet_final	24.40	kΩ	24.40	24.40	24.40	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.98	kΩ	24.98	24.98	24.98	23.70	26.30	P
Rdet_at_Vmax	24.62	kΩ	24.62	24.62	24.62	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_at_Vmax	18.1	mA	18.1	18.1	18.1	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_event2	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
MarkI	1.65	mA	1.65	1.65	1.65	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P

ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	155.7	mA	155.7	155.7	155.7	0.0	400.0	P
InrushI_2	157.0	mA	157.0	157.0	157.0	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.3	VDC	37.3	37.3	37.3	30.0	42.0	P
Voff	33.3	VDC	33.3	33.3	33.3	30.0	42.0	P
Vhyst	3.9	VDC	3.9	3.9	3.9	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	7.5	mA	7.5	7.5	7.5	0.0	174.2	P
MaxI_1	12.9	mA	12.9	12.9	12.9	10.0	174.2	P
Vport_1	47.9	VDC	47.9	47.9	47.9	37.0	57.0	INFO
Ppeak_1	0.62	W	0.62	0.62	0.62	0.0	8.4	P
Pavg_1	0.48	W	0.48	0.48	0.48	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.5	mA	2.5	2.5	2.5	0.0	154.8	P
MaxI_2	16.3	mA	16.3	16.3	16.3	10.0	154.8	P
Vport_2	54.0	VDC	54.0	54.0	54.0	42.5	57.0	INFO
Ppeak_2	0.88	W	0.88	0.88	0.88	0.0	8.4	P
Pavg_2	0.52	W	0.52	0.52	0.52	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT B MDI-X								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P

Rdet_final	24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.88	kΩ	24.88	24.88	24.88	23.70	26.30	P
Rdet_at_Vmax	24.62	kΩ	24.62	24.62	24.62	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_at_Vmax	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_event2	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
MarkI	1.65	mA	1.65	1.65	1.65	0.25	4.00	INFO
ClassNum2	2		2	2	-	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Lim**	**High Lim**	**P/F**
InrushI_1	155.5	mA	155.5	155.5	155.5	0.0	400.0	P
InrushI_2	156.9	mA	156.9	156.9	156.9	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.6	VDC	37.6	37.6	37.6	30.0	42.0	P
Voff	33.6	VDC	33.6	33.6	33.6	30.0	42.0	P
Vhyst	4.0	VDC	4.0	4.0	4.0	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	7.5	mA	7.5	7.5	7.5	0.0	173.4	P

MaxI_1	13.0	mA	13.0	13.0	13.0	10.0	173.4	P
Vport_1	48.2	VDC	48.2	48.2	48.2	37.0	57.0	INFO
Ppeak_1	0.63	W	0.63	0.63	0.63	0.0	8.4	P
Pavg_1	0.48	W	0.48	0.48	0.48	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.5	mA	2.5	2.5	2.5	0.0	154.2	P
MaxI_2	22.0	mA	22.0	22.0	22.0	10.0	154.2	P
Vport_2	54.3	VDC	54.3	54.3	54.3	42.5	57.0	INFO
Ppeak_2	1.19	W	1.19	1.19	1.19	0.0	8.4	P
Pavg_2	0.52	W	0.52	0.52	0.52	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P

4.5 Adjustable EVB Current Limit

For additional safety, the Si3406 has an adjustable EVB current limit feature.

The Si3406 controller measures the voltage on the RSENSE resistor (R7) through the ISNS pin. Care must be taken that this voltage goes below V_{SS}. When the voltage on R7 is V_{ISNS} = –270 mV (referenced to V_{SS}), the internal current limit circuit restarts the PD to protect the application.

The EVB current limit for this Class 2 application can be calculated with the following formula:

$$R_{SENSE} = 1.2\Omega$$

$$I_{LIMIT} = \frac{270mV}{1.2\Omega} = \quad 225mA$$

Equation 4.1. EVB Class 2 Current Limit

4.6 Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si3406 device integrates a current-mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee stable output voltage of the power supply and to reduce the influence of the input voltage variations and load changes on the output voltage, the feedback loop should be stable.

To verify the stability of the loop, the gain and phase of the loop have been measured.

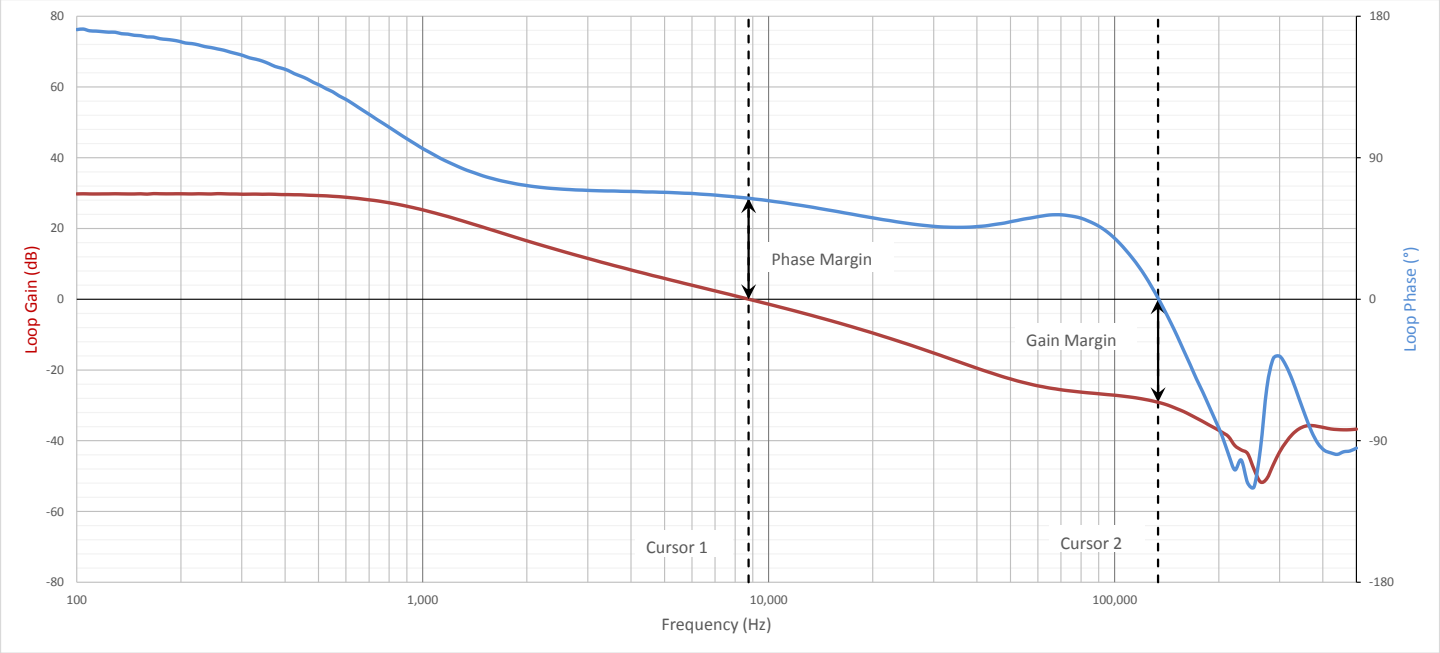


Figure 4.4. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 PD Feedback Loop Measurement Results at Full Load

Table 4.3. Measured Loop Gain and Phase Margin

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	8.75 kHz	0 dB	64.28 °
Cursor 2 (Gain Margin)	133.55 kHz	–29.13 dB	0 °

4.7 Load Step Transient Measurement Results

The Si3406-Buck EVB board's output has been tested with a load step function to verify the converter's output dynamic response.

Load Step: from 0.14 A to 1.28 A Output Current:
ΔV_{OUT} = 114.07 mV

Load Step, from 1.28 A to 0.14 A Output Current:
ΔV_{OUT} = 157.29 mV

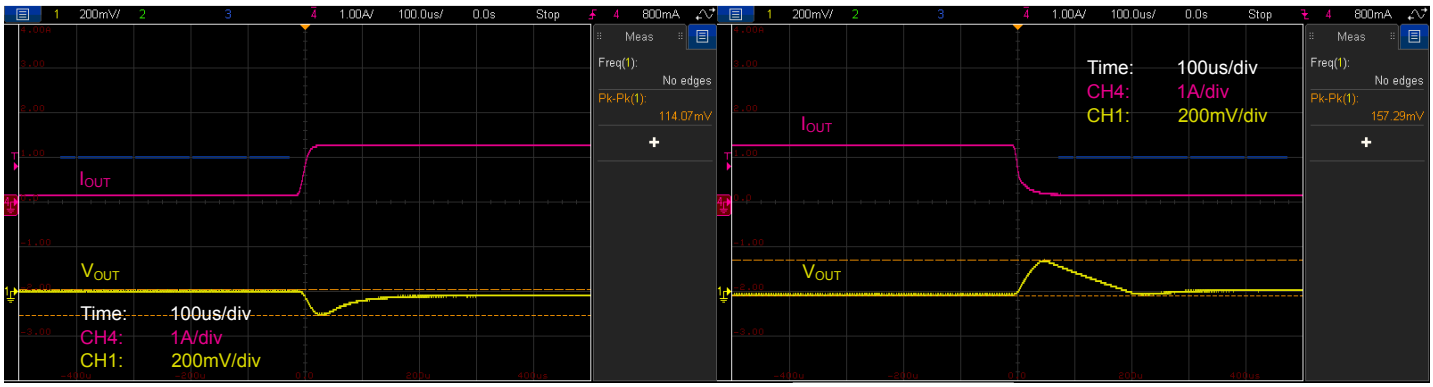


Figure 4.5. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 PD Output Load Step Transient Test

4.8 Output Voltage Ripple

The Si3406-Buck EVB output voltage ripple has been measured in both no-load and heavy-load conditions.

No-Load V_{OUT} Ripple = 9.46 mV **Heavy-Load V_{OUT} Ripple = 4.25 mV**

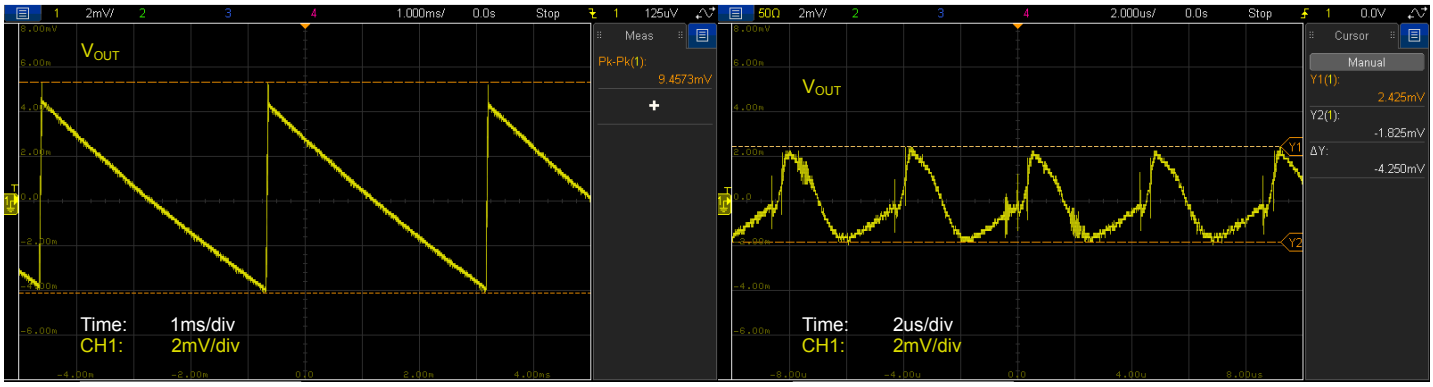


Figure 4.6. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 Output Voltage Ripple No-Load (Left) and Heavy-Load (Right) Conditions

4.9 Soft-Start Protection

The Si3406 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

The Si3406 intelligent adaptive soft-start mechanism does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, that way adjusting the output voltage ramping up time in a function of the attached load.

The controller lets the output voltage to rise faster in no load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

No-Load Soft-Start:
t_{RISE} = 5.53 ms

Heavy-Load Soft-Start:
t_{RISE} = 82.80 ms

Figure 4.7. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 Output Voltage Soft-Start at Low Load (Left) and Heavy Load (Right) Conditions

4.10 Output Short Protection

The Si3406 device has an integrated output short protection mechanism, which protects the IC itself and the surrounding external components from overheating in the case of electrical short on the output.

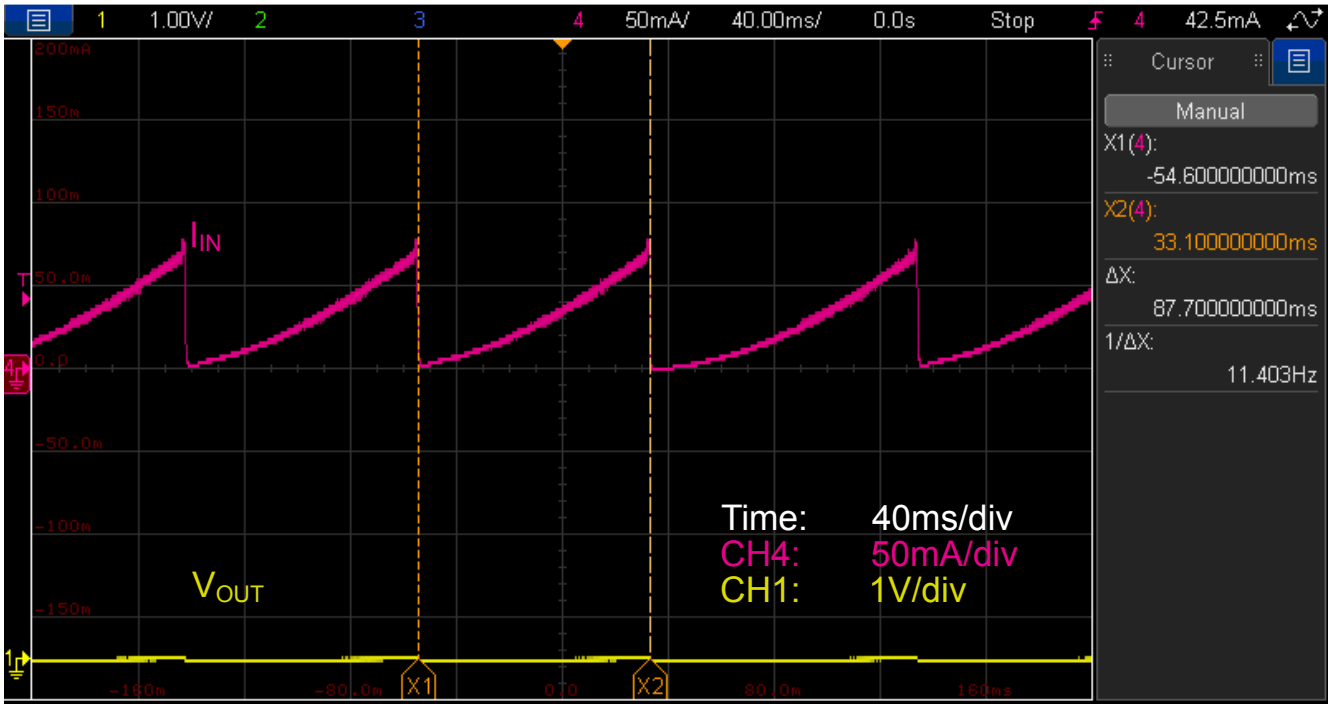


Figure 4.8. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 Output Short Circuit Protection

4.11 Pulse Skipping at No-Load Condition

The Si3406 device has an integrated pulse skipping mechanism to ensure ultra-low power consumption at light load condition.

As the output load decreases, the controller starts to reduce the pulse-width of the PWM signal (switcher ON time). At some point, even the minimum width pulse would provide higher energy than the application requires, which could result in loss of voltage regulation.

When the controller detects light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or light-load skipping mode. This mode is shown in the figure below by depicting the switching node of the integrated switching FET at no load condition.

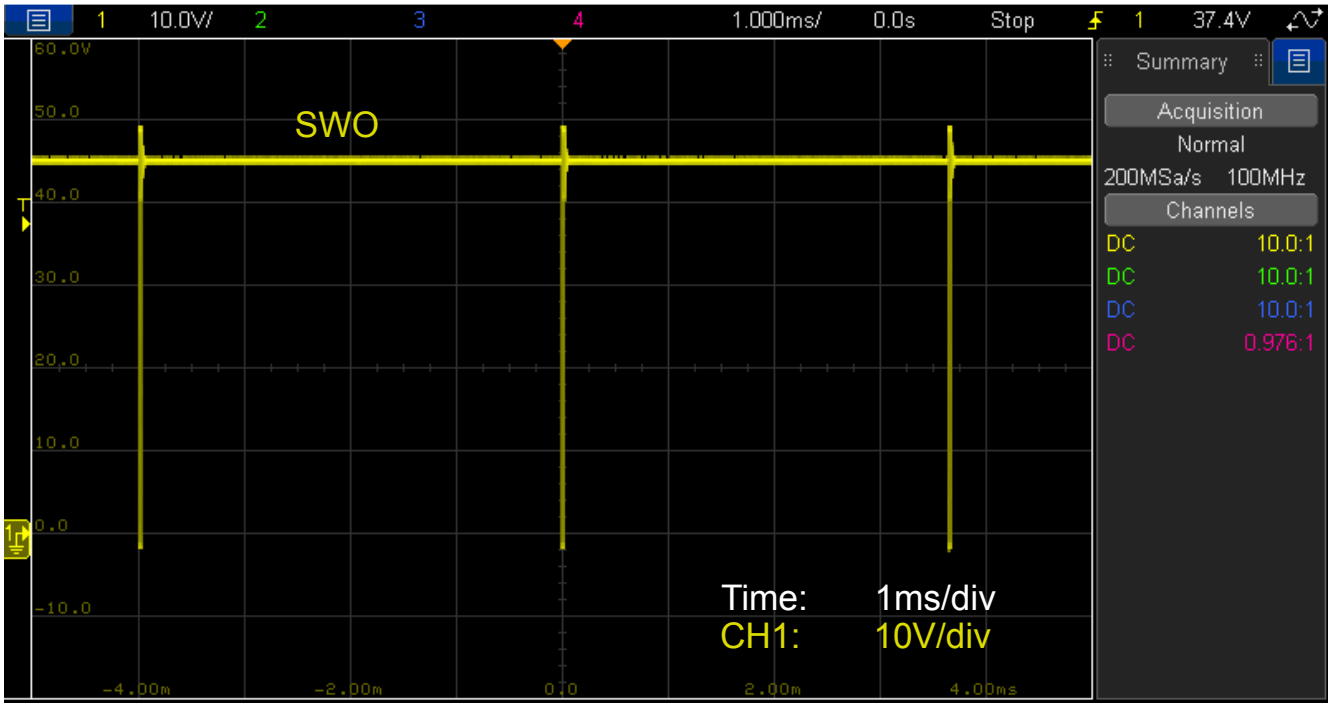


Figure 4.9. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 Pulse Skipping at No-load Condition: SWO Waveform

4.12 Discontinuous (DCM) and Continuous (CCM) Current Modes

At low load, the converter works in discontinuous current mode (DCM). At heavy load, the converter runs in continuous current mode (CCM). At low load, the SWO voltage waveform has a ringing waveform, which is typical for DCM operation.

Low-Load, DCM **Heavy-Load, CCM**

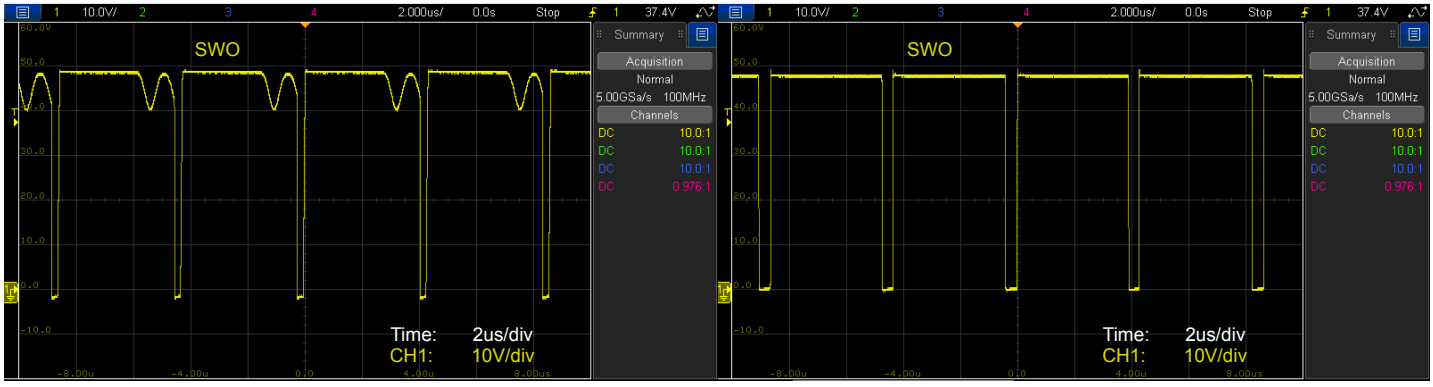


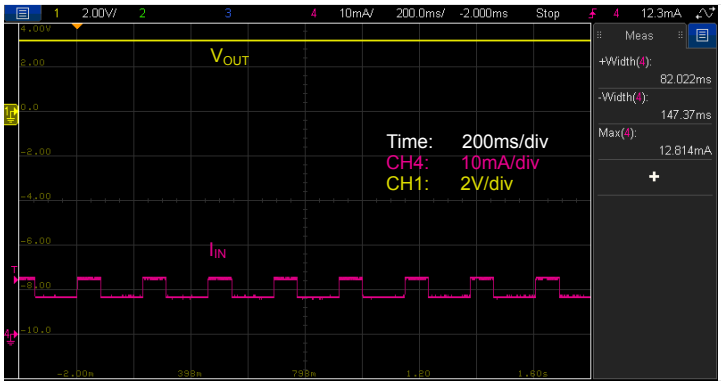
Figure 4.10. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2: SWO Waveform in Discontinuous Current Mode (DCM) at Low Load (Left), and in Continuous Current Mode (CCM) at Heavy Load (Right)

4.13 Maintain Power Signature (MPS)

The Si3406-Buck EVB board has a built-in MPS feature that enables the Si3406 to maintain the connection with the PSE when the PD is in a low-current consumption mode. MPS can be used in user mode or in automatic mode. In user mode, nSLEEP shall be tied to VDD at startup (R13), and the host controller needs to manually start/stop MPS generation by pulling the nSLEEP line low or high respectively. To enable automatic MPS feature, nSLEEP shall be tied to VSS at startup (R12). In automatic mode, Si3406 monitors the input current and turns off MPS automatically when it is below a predefined level.

Note: Si3406 assumes a minimum consumption of the host controller therefore to pass Sifos MPS tests, a dummy load is recommended to be installed on the EVB (R14) to keep the consumption above the predefined current threshold. The figure below shows the automatic MPS pulses generated by the EVB when an 82 Ω dummy load is installed.

Automatic MPS Pulse Generation by Si3406
VON = 82.02 ms, VOFF = 147.37 ms, IMAX = 12.81 mA



Automatic MPS Pulse Generation by Si3406
Sifos Startup Trace

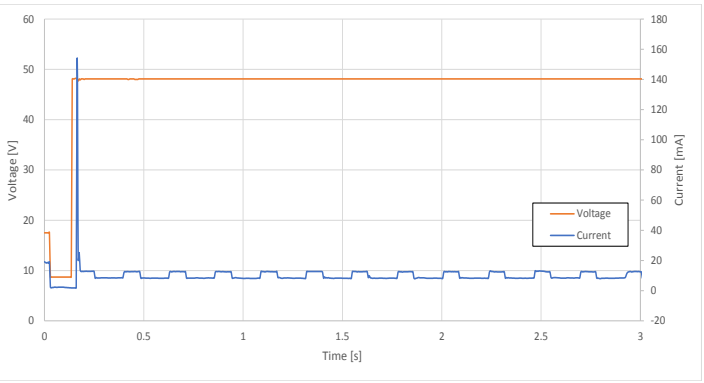


Figure 4.11. Si3406-Buck Non-Isolated EVB, 3.3 V, Class 2 PD Automatic Maintain Power Signature (MPS) Generation

4.14 Radiated Emissions Measurement Results

Radiated emissions have been measured of the Si3406-Buck, 3.3 V, Class 2 EVB board with 50 V input voltage and full load connected to the output – 6.5 W.

As shown below, the Si3406-Buck, 3.3 V, Class 2 EVB is fully compliant with the international EN 55032 class B emissions standard.

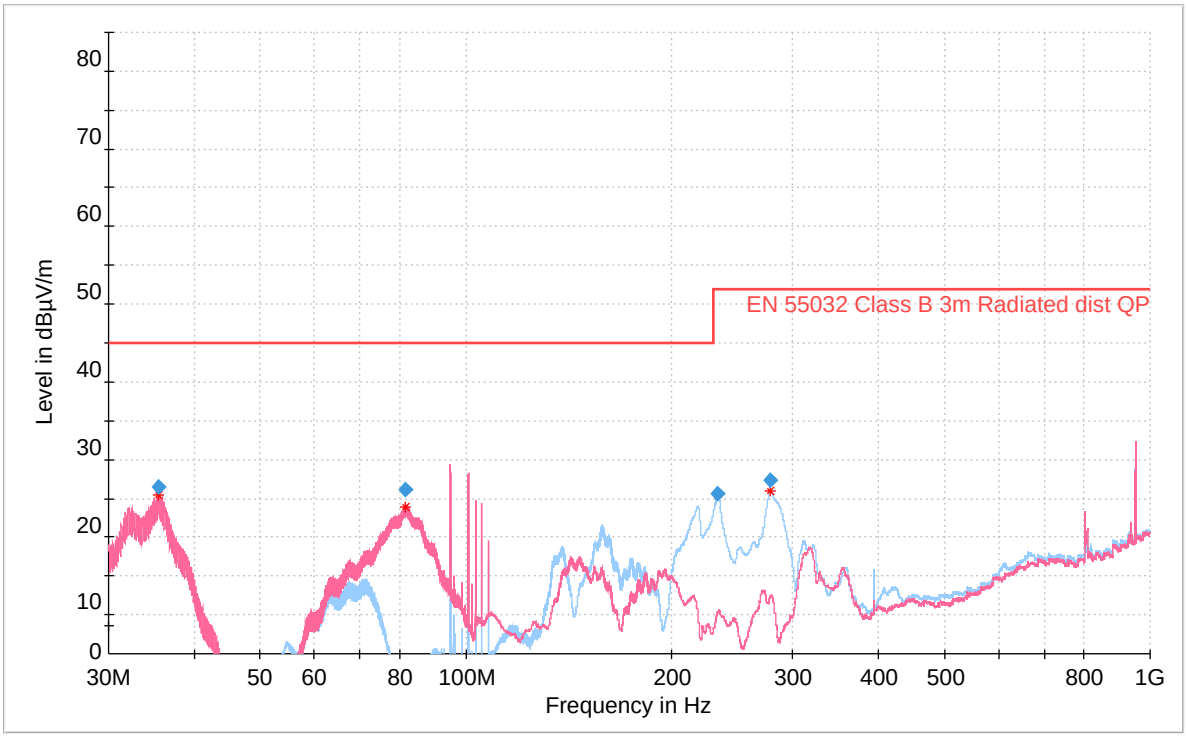


Figure 4.12. Si3406-Buck Non-Isolated EVB Radiated Emissions Measurements Results; 50 V Input, 3.3 V Output, 6.5 W Input Load

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization). Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

4.15 Conducted Emissions Measurement Results

The Si3406-Buck, 3.3 V, Class 2 EVB board's conducted emissions have been measured in two different measurement methods to comply with the international EN 55032 standard. The EVB is supplied and measured on its PoE input port as shown in the following figure.

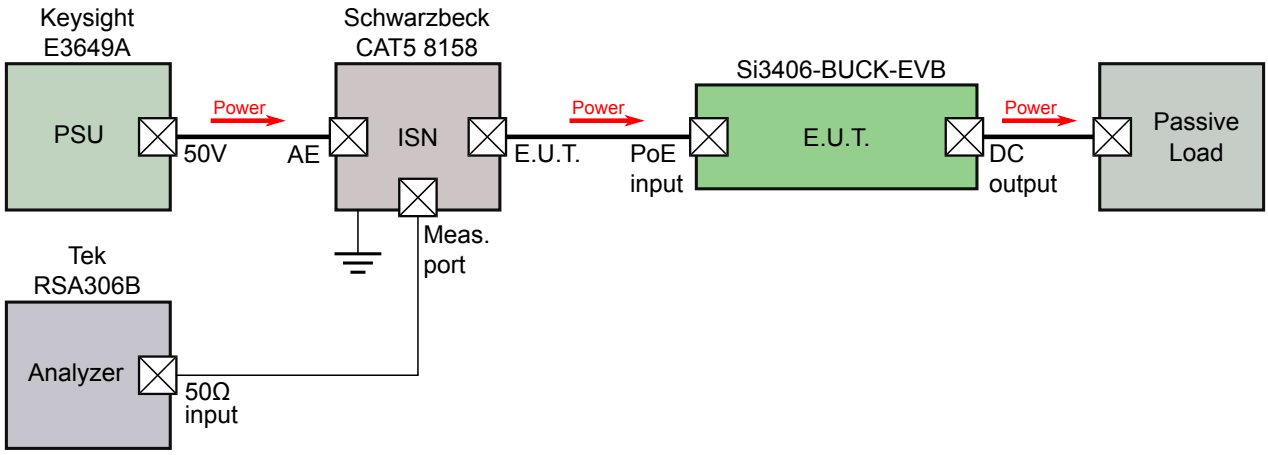


Figure 4.13. Conducted EMI Measurement Setup

The detector in the spectrum analyzer is set to:

- Peak detector and
- Average detector

Both results are shown below.

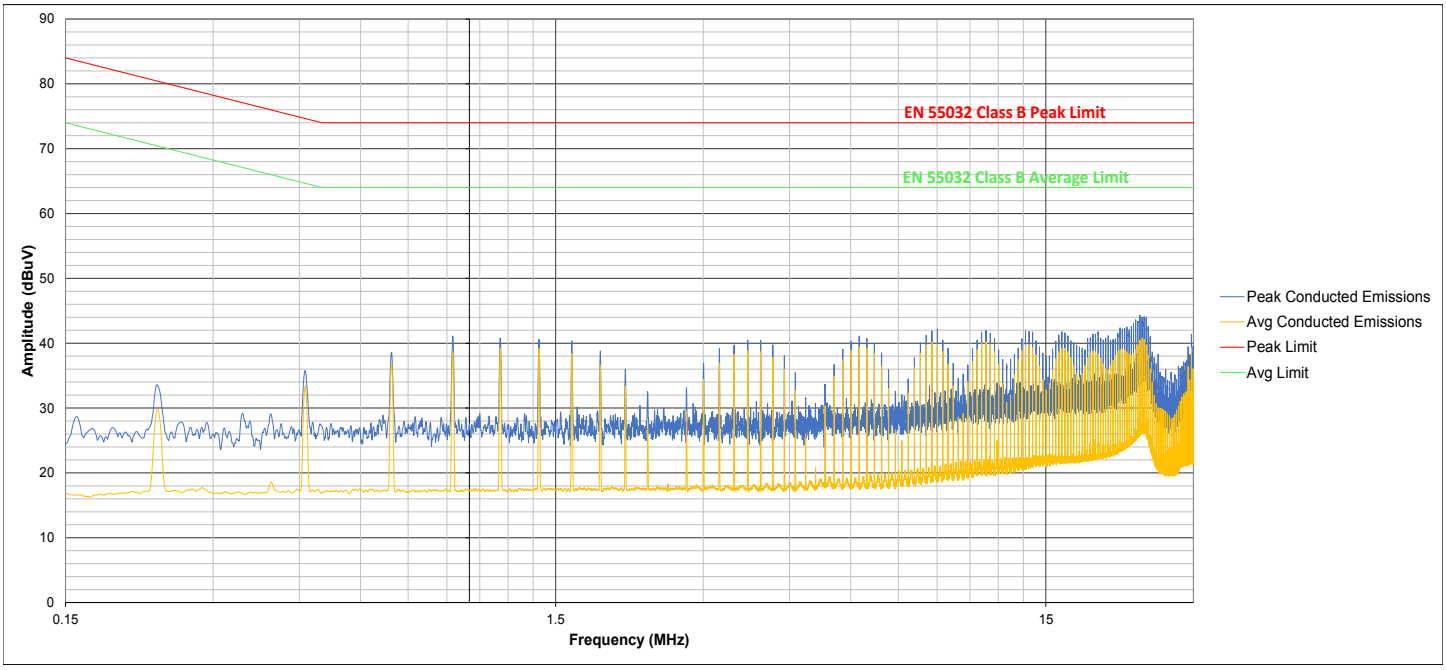


Figure 4.14. Si3406-Buck Non-Isolated EVB Conducted Emissions Measurements Results; 50 V Input, 3.3 V Output, 6.5 W Input Load

4.16 Bill of Materials

The following table is the BOM listing for the standard 3.3 V output evaluation board with option PoE Class 2.

Table 4.4. Si3406-BUCK-3.3 V Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	C1	1 µF		100 V	±10%	X7R	C1210	C1210X7R101-105K	Venkel
1	C13	0.1 µF		100 V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
1	C14	330 pF		50 V	±1%	C0G	C0805	C0805C0G500-331F	Venkel
2	C19, C21	0.1 µF		16 V	±10%	X7R	C0805	C0805X7R160-104K	Venkel
1	C2	12 µF		100 V	±20%	Alum_Elec	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
3	C4, C5, C8	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
1	C7	22 µF		6.3 V	±20%	X5R	C0805	C0805X5R6R3-226M	Venkel
1	D1	SDT5H100P5	5 A	100 V		Schottky	POWERDI-5	SDT5H100P5-7	Diodes Inc.
1	J1	RJ-45				Receptacle	RJ45-SI-52004	SI-52003-F	Bel
1	L2	100 µH	2.8 A		±20%	Shielded	IND-MSS1278	MSS1278-104ML	Coilcraft
4	L5, L6, L7, L8	330 Ω	1500 mA			SMT	L0805	BLM21PG331SN1	Murata
1	R1	475 Ω	1/8 W		±1%	Thick Film	R0805	CR0805-8W-4750FT	Venkel
1	R10	88.7 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080588K7FKEA	Vishay
1	R11	75 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-75R0F	Venkel
1	R13	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R3	3.24 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW08053K24FKEA	Vishay
1	R4	4.87 kΩ	1/8 W		±1%	Thick Film	R0805	RC0805FR-074K87L	Yageo
1	R5	10 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-10R0F	Venkel
1	R6	3 Ω	1/8 W		±1%	Thick Film	R0805	CR0805-8W-3R00FT	Venkel
1	R7	1.2 Ω	1/10 W		±5%	Thick Film	R0805	CR0805-10W-1R2J	Venkel
1	R8	210 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-2103F	Venkel
1	R9	24.3 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080524K3FKEA	Vishay
4	TP1, TP2, TP11, TP12	Black				Loop	Testpoint	5001	Keystone
1	U1	Si3406		120 V		PD	QFN20N5X5P0.8	Si3406-A-GM	Silicon Labs
Not Installed Components									
1	C20	330 pF		50 V	±1%	C0G	C0805	C0805C0G500-331F	Venkel
1	C22	200 pF		50 V	±1%	C0G	C0805	C0805C0G500-201FNE	Venkel
1	C3	560 µF		6.3 V	±20%	Alum_Elec	C3.5X8MM-RAD	EEUFM0J561	Panasonic
1	C6	39 pF		25 V	±1%	C0G	C0805	C0805C0G250-390FNP	Venkel

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	R12	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R14	120 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1200F	Venkel
8	TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Black				Loop	Testpoint	5001	Keystone

5. Si3406-Buck EVB: 5 V, Class 2 Configuration

5.1 Si3406-Buck EVB Schematic: 5 V, Class 2, 7 W

In the figure below, the schematic of the Si3406-Buck 5 V, Class 2 EVB is shown. The parts in red on the schematic represent the BOM differences compared to the core design.

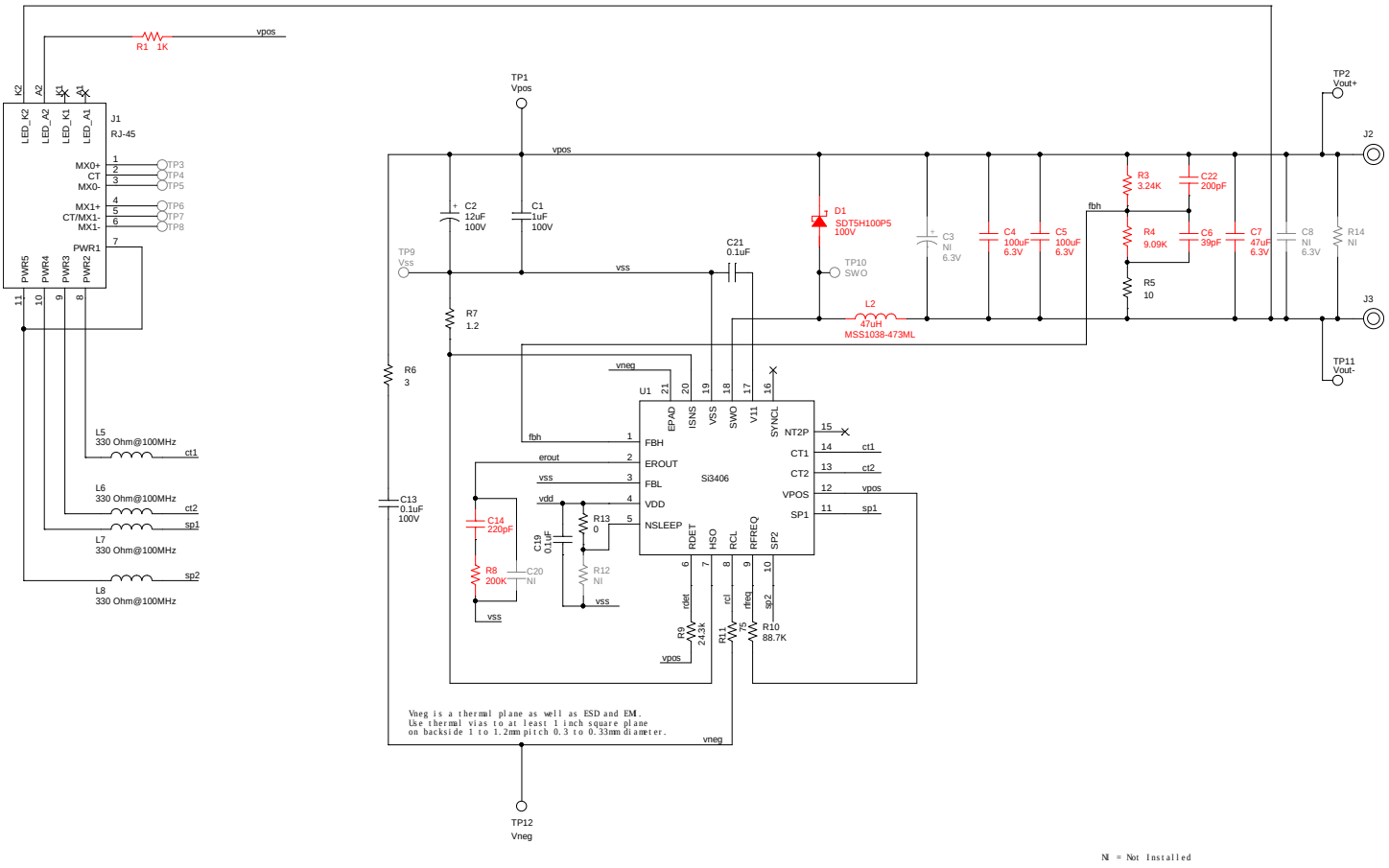


Figure 5.1. Si3406 Buck Non-Isolated EVB Schematic: 5 V, Class 2 PD, 7W

5.2 End-to-End EVB Efficiency

The end-to-end conversion efficiency measurement data of the Si3406 5V Buck EVB board is shown below with internal bridges. The efficiency was measured at three different input voltage levels: 42 V, 50 V and 57 V.

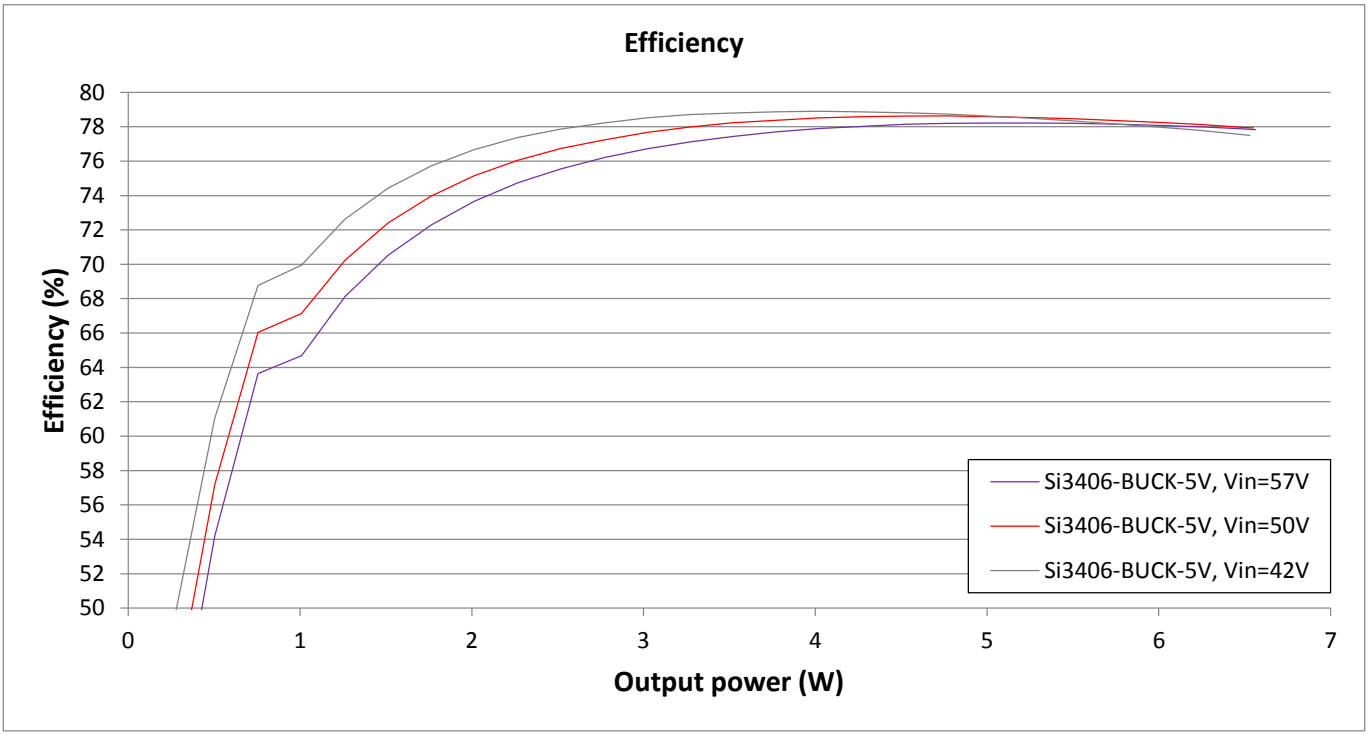


Figure 5.2. Si3406-Buck End-to-End Efficiency Chart with Internal Diodes as Input Bridge: 42 V, 50 V and 57V Input, 5 V Output, Class 2

Note: The chart shows end-to-end EVB efficiency. The voltage drop on the diode bridge is included. LEDs are removed.

5.3 Thermal Measurements

The Si3406-Buck EVB's temperature was measured at maximum **input power – 6.5 W**. The Si3406-Buck EVB is configured for 5 V output voltage and Class 2 power level. The following figure shows the thermal image taken of the top side of the PCB at maximum input power.

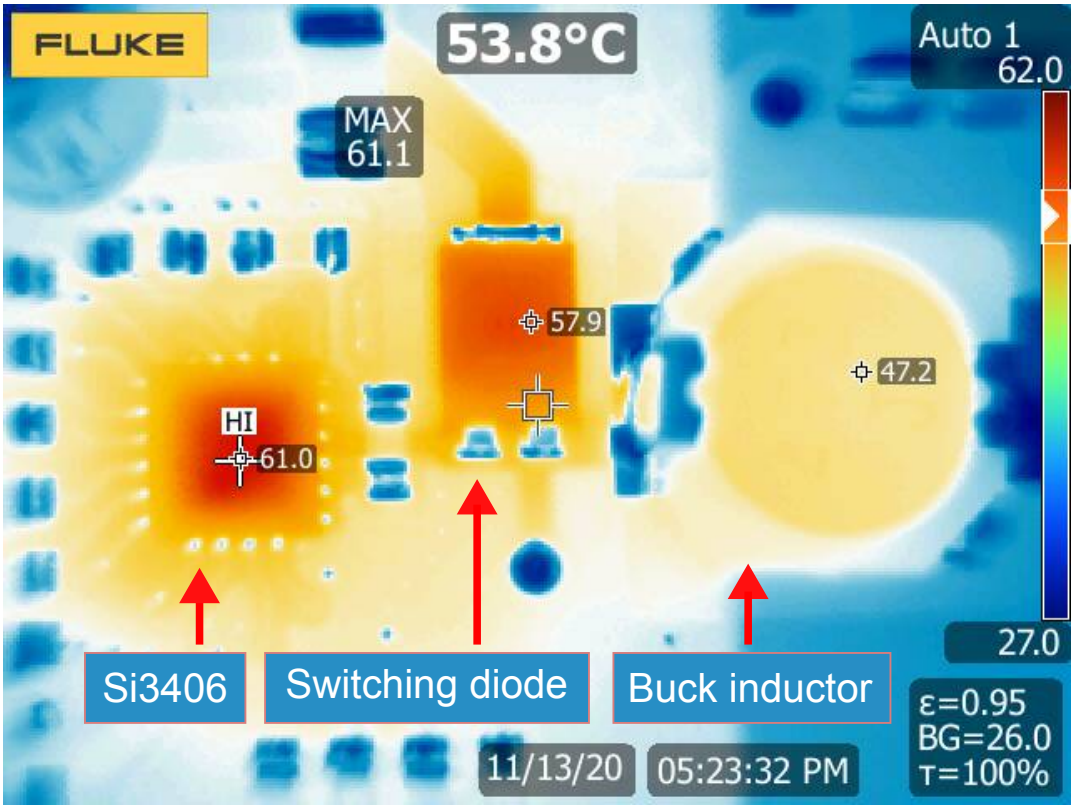


Figure 5.3. Thermal Measurements of the Si3406-Buck Non-Isolated EVB, 5 V, Class 2 PD

The following table lists the temperatures of the notable components across the board.

Table 5.1. Component Temperatures at Full Load

Component	Temperature
Si3406 – U1	61.1 °C
Switching Diode – D1	57.9 °C
Buck Inductor – L2	47.2 °C

Note:
1. The ambient temperature was 26 °C during the thermal measurements.

5.4 SIFOS PoE Compatibility Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices (PD's). The Si3406-Buck-5V EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies.

Table 5.2. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 PD SIFOS PoE Compatibility Test Results

ALT A MDI								
Detection and Classification		PSE Emulation		Pairs	A	Polarity	MDI	Det Cycles	3
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.42	kΩ	24.42	24.42	24.42	23.70	26.30	P
Rdet_final		24.46	kΩ	24.46	24.46	24.46	23.70	26.30	P
Rdet_unpwr		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin		24.56	kΩ	24.56	24.56	24.56	23.70	26.30	P
Rdet_at_Vmax		24.46	kΩ	24.46	24.46	24.46	23.70	26.30	P
Rdet_Voffset		1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification									
Iclass		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
ClassNum		2		2	2	—	0	4	P
Tclass		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability		1					1	1	P
Iclass_at_Vmin		18.7	mA	18.7	18.7	18.7	17.0	20.0	P
Iclass_at_Vmax		18.6	mA	18.6	18.6	18.6	17.0	20.0	P
2 Event Classification									
Iclass_event1		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_event2		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
MarkI		1.54	mA	1.54	1.54	1.54	0.25	4.00	INFO
ClassNum2		2		2	2	—	0	4	P
Tclass_event1		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1		1					1	1	P
ClassStability_event2		1					1	1	P
Power-Up / Down									
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		163.7	mA	163.7	163.7	163.7	0.0	400.0	P
InrushI_2		165.1	mA	165.1	165.1	165.1	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P

Inrush_delayed	0		0	0	—	0	0	P
Von	37.7	VDC	37.7	37.7	37.7	30.0	42.0	P
Voff	33.4	VDC	33.4	33.4	33.4	30.0	42.0	P
Vhyst	4.2	VDC	4.2	4.2	4.2	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	10.7	mA	10.7	10.7	10.7	0.0	173.9	P
MaxI_1	15.9	mA	15.9	15.9	15.9	10.0	173.9	P
Vport_1	48.1	VDC	48.1	48.1	48.1	37.0	57.0	INFO
Ppeak_1	0.77	W	0.77	0.77	0.77	0.0	8.4	P
Pavg_1	0.62	W	0.62	0.62	0.62	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.8	mA	2.8	2.8	2.8	0.0	154.5	P
MaxI_2	22.8	mA	22.8	22.8	22.8	10.0	154.5	P
Vport_2	54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2	1.23	W	1.23	1.23	1.23	0.0	8.4	P
Pavg_2	0.66	W	0.66	0.66	0.66	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT A MDI-X								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.42	kΩ	24.42	24.42	24.42	23.70	26.30	P
Rdet_final	24.42	kΩ	24.42	24.42	24.42	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.91	kΩ	24.91	24.91	24.91	23.70	26.30	P
Rdet_at_Vmax	24.52	kΩ	24.52	24.52	24.52	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P

Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.8	mA	18.8	18.8	18.8	17.0	20.0	P
Iclass_at_Vmax	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_event2	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
MarkI	1.54	mA	1.54	1.54	1.54	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	163.2	mA	163.2	163.2	163.2	0.0	400.0	P
InrushI_2	164.8	mA	164.8	164.8	164.8	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.8	VDC	37.8	37.8	37.8	30.0	42.0	P
Voff	33.6	VDC	33.6	33.6	33.6	30.0	42.0	P
Vhyst	4.2	VDC	4.2	4.2	4.2	0.0	12.0	P
BackfeedV	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	10.3	mA	10.3	10.3	10.3	0.0	173.4	P
MaxI_1	16.2	mA	16.2	16.2	16.2	10.0	173.4	P
Vport_1	48.2	VDC	48.2	48.2	48.2	37.0	57.0	INFO
Ppeak_1	0.78	W	0.78	0.78	0.78	0.0	8.4	P
Pavg_1	0.61	W	0.61	0.61	0.61	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P

DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.7	mA	2.7	2.7	2.7	0.0	154.3	P
MaxI_2	17.1	mA	17.1	17.1	17.1	10.0	154.3	P
Vport_2	54.2	VDC	54.2	54.2	54.2	42.5	57.0	INFO
Ppeak_2	0.93	W	0.93	0.93	0.93	0.0	8.4	P
Pavg_2	0.66	W	0.66	0.66	0.66	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT B MDI								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.40	kΩ	24.40	24.40	24.40	23.70	26.30	P
Rdet_final	24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.83	kΩ	24.83	24.83	24.83	23.70	26.30	P
Rdet_at_Vmax	24.57	kΩ	24.57	24.57	24.57	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_at_Vmax	18.4	mA	18.4	18.4	18.4	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_event2	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
MarkI	1.61	mA	1.61	1.61	1.61	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P

ClassStability_event2		1					1	1	P
Power-Up / Down									
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		163.9	mA	163.9	163.9	163.9	0.0	400.0	P
InrushI_2		165.7	mA	165.7	165.7	165.7	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed		0		0	0	—	0	0	P
Von		37.7	VDC	37.7	37.7	37.7	30.0	42.0	P
Voff		33.5	VDC	33.5	33.5	33.5	30.0	42.0	P
Vhyst		4.2	VDC	4.2	4.2	4.2	0.0	12.0	P
BackfeedV		0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover		0		0	0	—	0	0	P
SigRecoverTime		0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1		**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1		10.2	mA	10.2	10.2	10.2	0.0	174.1	P
MaxI_1		15.5	mA	15.5	15.5	15.5	10.0	174.1	P
Vport_1		48.0	VDC	48.0	48.0	48.0	37.0	57.0	INFO
Ppeak_1		0.75	W	0.75	0.75	0.75	0.0	8.4	P
Pavg_1		0.59	W	0.59	0.59	0.59	0.0	6.5	P
MPSViolation_1		0		0	0	—	0	0	P
TcutWindowViolation_1		0		0	0	—	0	0	P
DutyCycleViolation_1		0		0	0	—	0	0	P
MDI Powered Type-2 PHY		**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2		2.3	mA	2.3	2.3	2.3	0.0	154.7	P
MaxI_2		21.6	mA	21.6	21.6	21.6	10.0	154.7	P
Vport_2		54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2		1.17	W	1.17	1.17	1.17	0.0	8.4	P
Pavg_2		0.64	W	0.64	0.64	0.64	0.0	6.5	P
MPSViolation_2		0		0	0	—	0	0	P
TcutWindowViolation_2		0		0	0	—	0	0	P
DutyCycleViolation_2		0		0	0	—	0	0	P
ALT B MDI-X									
Detection and Classification		**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P

Rdet_final	24.42	kΩ	24.42	24.42	24.42	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.74	kΩ	24.74	24.74	24.74	23.70	26.30	P
Rdet_at_Vmax	24.56	kΩ	24.56	24.56	24.56	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_at_Vmax	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_event2	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
MarkI	1.61	mA	1.61	1.61	1.61	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	163.6	mA	163.6	163.6	163.6	0.0	400.0	P
InrushI_2	165.2	mA	165.2	165.2	165.2	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.8	VDC	37.8	37.8	37.8	30.0	42.0	P
Voff	33.5	VDC	33.5	33.5	33.5	30.0	42.0	P
Vhyst	4.2	VDC	4.2	4.2	4.2	0.0	12.0	P
BackfeedV	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	9.9	mA	9.9	9.9	9.9	0.0	173.8	P

MaxI_1	15.6	mA	15.6	15.6	15.6	10.0	173.8	P
Vport_1	48.1	VDC	48.1	48.1	48.1	37.0	57.0	INFO
Ppeak_1	0.75	W	0.75	0.75	0.75	0.0	8.4	P
Pavg_1	0.59	W	0.59	0.59	0.59	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.2	mA	2.2	2.2	2.2	0.0	154.6	P
MaxI_2	20.4	mA	20.4	20.4	20.4	10.0	154.6	P
Vport_2	54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2	1.10	W	1.10	1.10	1.10	0.0	8.4	P
Pavg_2	0.64	W	0.64	0.64	0.64	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P

5.5 Adjustable EVB Current Limit

For additional safety, the Si3406 has an adjustable EVB current limit feature.

The Si3406 controller measures the voltage on the R_{SENSE} resistor (R7) through the ISNS pin. Care must be taken that this voltage goes below V_{SS}. When the voltage on R7 is V_{ISNS} = –270 mV (referenced to V_{SS}), the internal current limit circuit restarts the PD to protect the application.

The EVB current limit for this Class 2 application can be calculated with the following formula:

$$R_{SENSE} = 1.2\Omega$$

$$I_{LIMIT} = \frac{270mV}{1.2\Omega} = \quad 225mA$$

Equation 5.1. EVB Class 2 Current Limit

5.6 Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si3406 device integrates a current-mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee stable output voltage of the power supply and to reduce the influence of the input voltage variations and load changes on the output voltage, the feedback loop should be stable.

To verify the stability of the loop, the gain and phase of the loop has been measured.

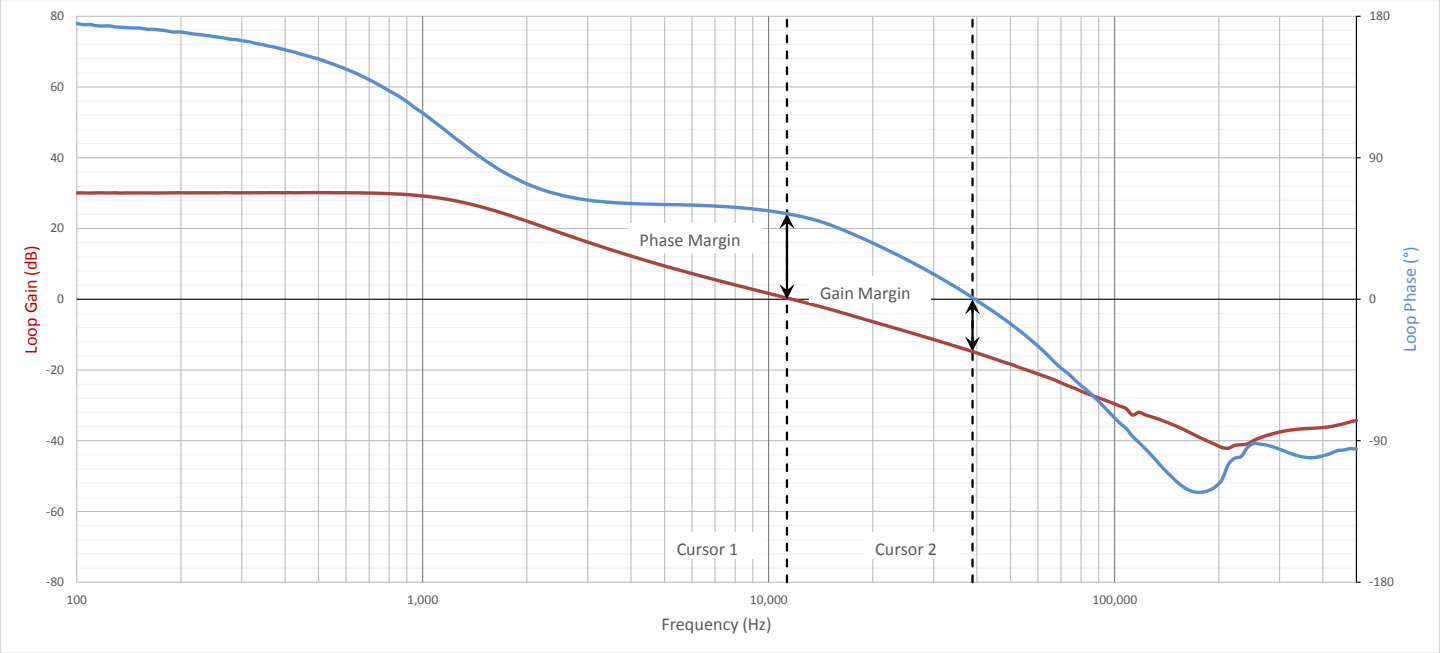


Figure 5.4. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 PD Feedback Loop Measurement Results at Full Load

Table 5.3. Measured Loop Gain and Phase Margin

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	11.30 kHz	0 dB	54.42 °
Cursor 2 (Gain Margin)	38.84 kHz	–14.78 dB	0 °

5.7 Load Step Transient Measurement Results

The Si3406-Buck EVB board's output has been tested with a load step function to verify the converter's output dynamic response.

Load Step: from 0.1 A to 0.92 A Output Current:
ΔV_{OUT} = 114.07 mV

Load Step, from 0.92 A to 0.1 A Output Current:
ΔV_{OUT} = 101.01 mV

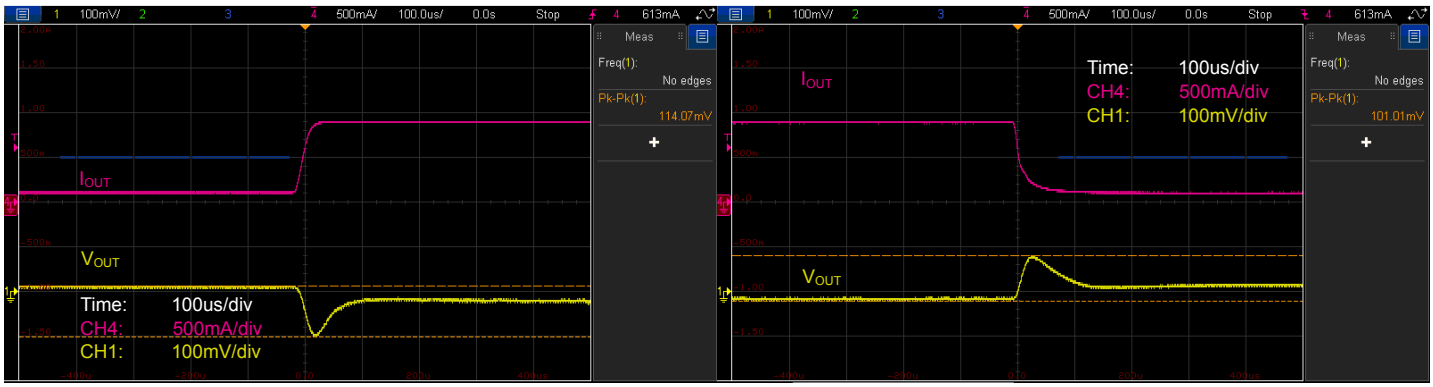


Figure 5.5. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 PD Output Load Step Transient Test

5.8 Output Voltage Ripple

The Si3406-Buck EVB output voltage ripple has been measured in both no-load and heavy-load conditions.

No-Load V_{OUT} Ripple = 11.40 mV **Heavy-Load V_{OUT} Ripple = 4.18 mV**

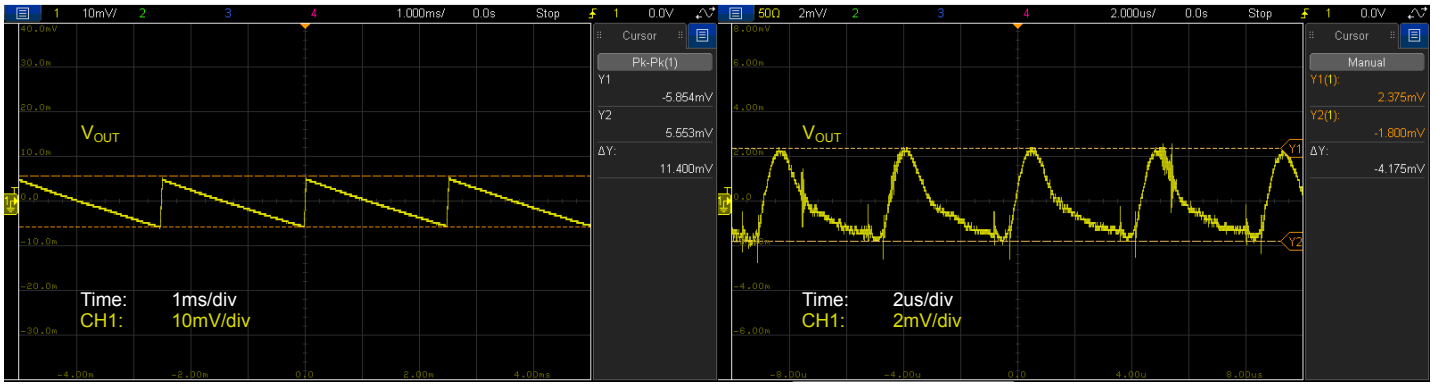


Figure 5.6. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 Output Voltage Ripple No-Load (Left) and Heavy-Load (Right) Conditions

5.9 Soft-Start Protection

The Si3406 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

The Si3406 intelligent adaptive soft-start mechanism does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, that way adjusting the output voltage ramping up time in a function of the attached load.

The controller lets the output voltage to rise faster in no load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

No-Load Soft-Start:
t_{RISE} = 5.76 ms

Heavy-Load Soft-Start:
t_{RISE} = 67.6 ms

Figure 5.7. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 Output Voltage Soft-Start at Low Load (Left) and Heavy Load (Right) Conditions

5.10 Output Short Protection

The Si3406 device has an integrated output short protection mechanism, which protects the IC itself and the surrounding external components from overheating in the case of electrical short on the output.

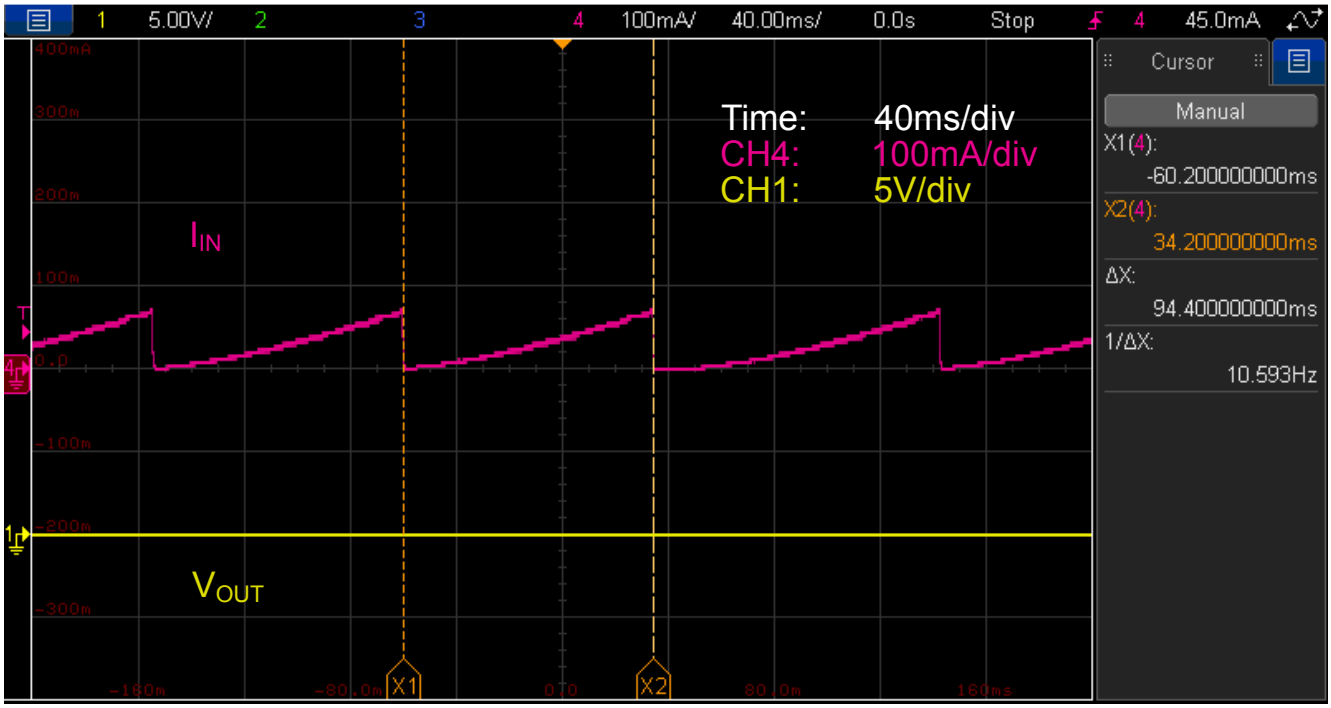


Figure 5.8. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 Output Short Circuit Protection

5.11 Pulse Skipping at No-Load Condition

The Si3406 device has an integrated pulse skipping mechanism to ensure ultra-low power consumption at light load condition.

As the output load decreases, the controller starts to reduce the pulse-width of the PWM signal (switcher ON time). At some point, even the minimum width pulse would provide higher energy than the application requires, which could result in loss of voltage regulation.

When the controller detects light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or light-load skipping mode. This mode is shown in the figure below by depicting the switching node of the integrated switching FET at no load condition.

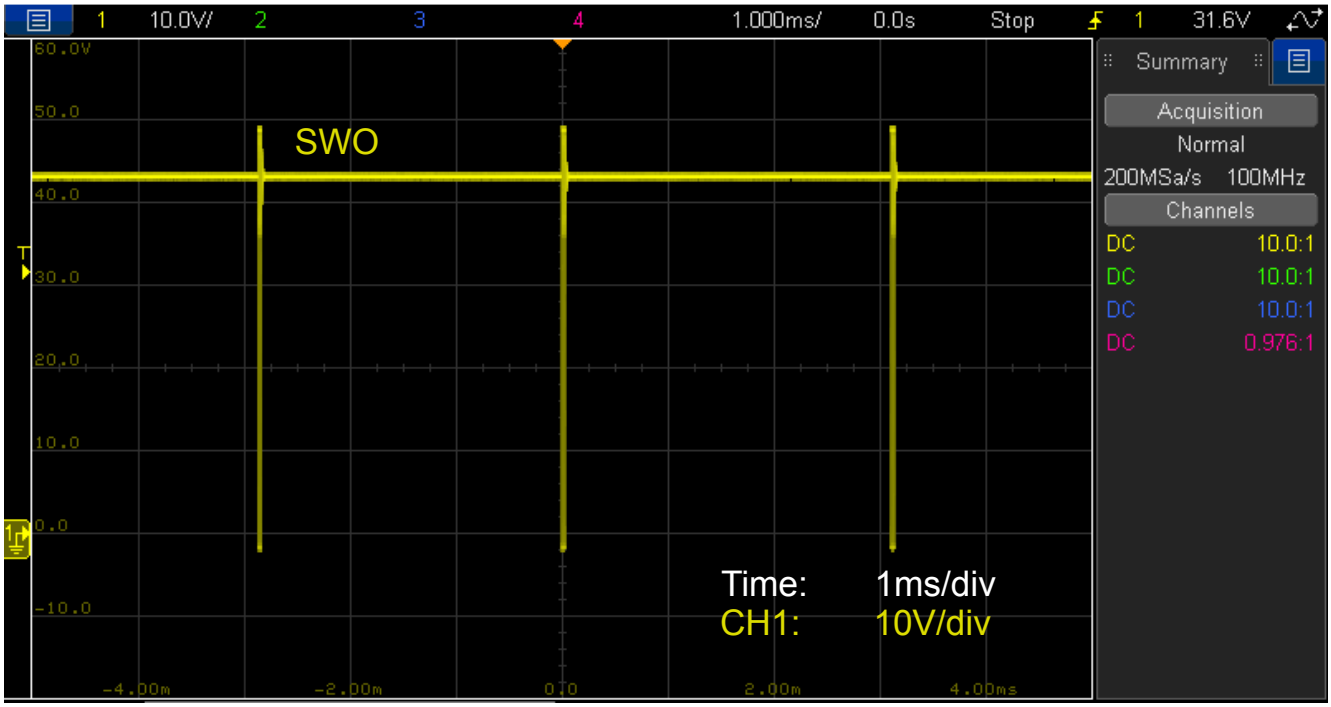


Figure 5.9. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 Pulse Skipping at No-load Condition: SWO Waveform

5.12 Discontinuous (DCM) and Continuous (CCM) Current Modes

At low load, the converter works in discontinuous current mode (DCM). At heavy load, the converter runs in continuous current mode (CCM). At low load, the SWO voltage waveform has a ringing waveform, which is typical for DCM operation.

Low-Load, DCM **Heavy-Load, CCM**

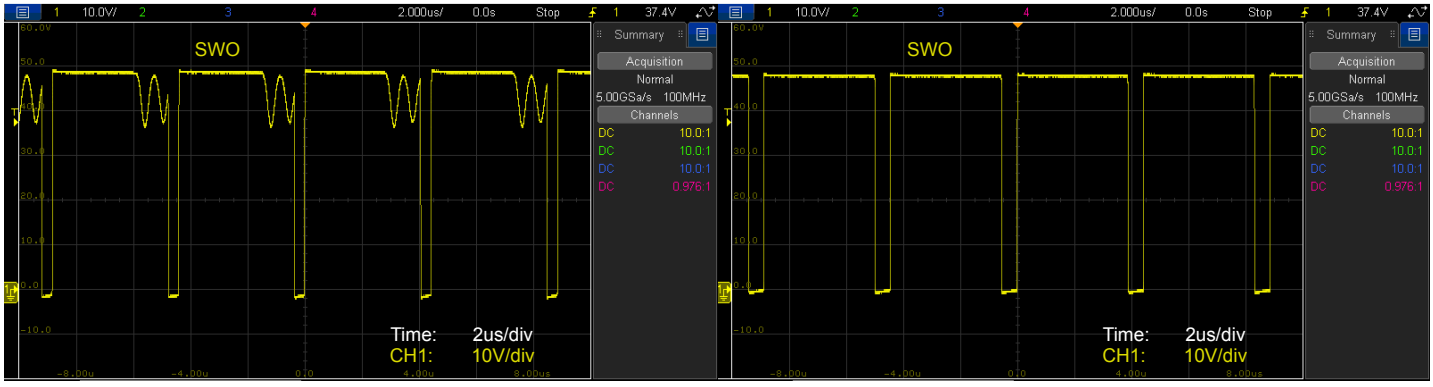


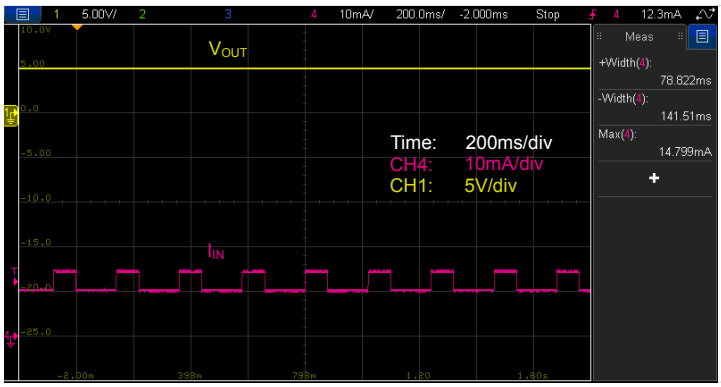
Figure 5.10. Si3406-Buck Non-Isolated EVB, 5 V, Class 2: SWO Waveform in Discontinuous Current Mode (DCM) at Low Load (Left), and in Continuous Current Mode (CCM) at Heavy Load (Right)

5.13 Maintain Power Signature (MPS)

The Si3406-Buck EVB board has a built-in MPS feature that enables the Si3406 to maintain the connection with the PSE when the PD is in a low-current consumption mode. MPS can be used in user mode or in automatic mode. In user mode, nSLEEP shall be tied to VDD at startup (R13), and the host controller needs to manually start/stop MPS generation by pulling the nSLEEP line low or high respectively. To enable the automatic MPS feature, nSLEEP shall be tied to VSS at startup (R12). In automatic mode, the Si3406 monitors the input current and turns off MPS automatically when it is below a predefined level.

Note: Si3406 assumes a minimum consumption of the host controller therefore to pass Sifos MPS tests, a dummy load is recommended to be installed on the EVB (R14) to keep the consumption above the predefined current threshold. The figure below shows the automatic MPS pulses generated by the EVB when an 100 Ω dummy load is installed.

Automatic MPS Pulse Generation by Si3406
V_{ON} = 78.80 ms, V_{OFF} = 141.51 ms, I_{MAX} = 14.80 mA



Automatic MPS Pulse Generation by Si3406
Sifos Startup Trace

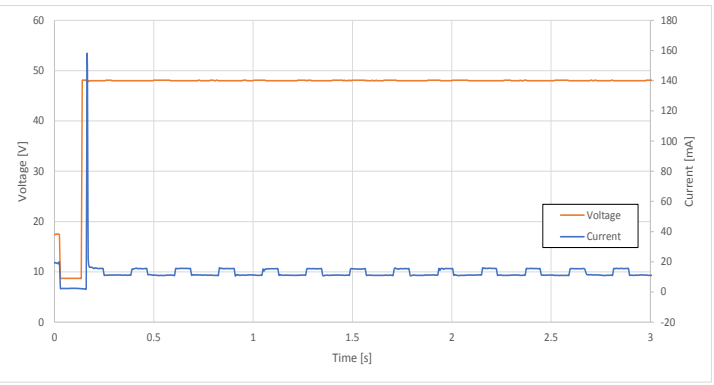


Figure 5.11. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 PD Automatic Maintain Power Signature (MPS) Generation

5.14 Radiated Emissions Measurement Results

Radiated emissions have been measured of the Si3406-Buck EVB board with 50 V input voltage and full load connected to the output – 6.5 W.

As shown below, the Si3406-Buck, 5 V, Class 2 EVB is fully compliant with the international EN 55032 class B emissions standard.

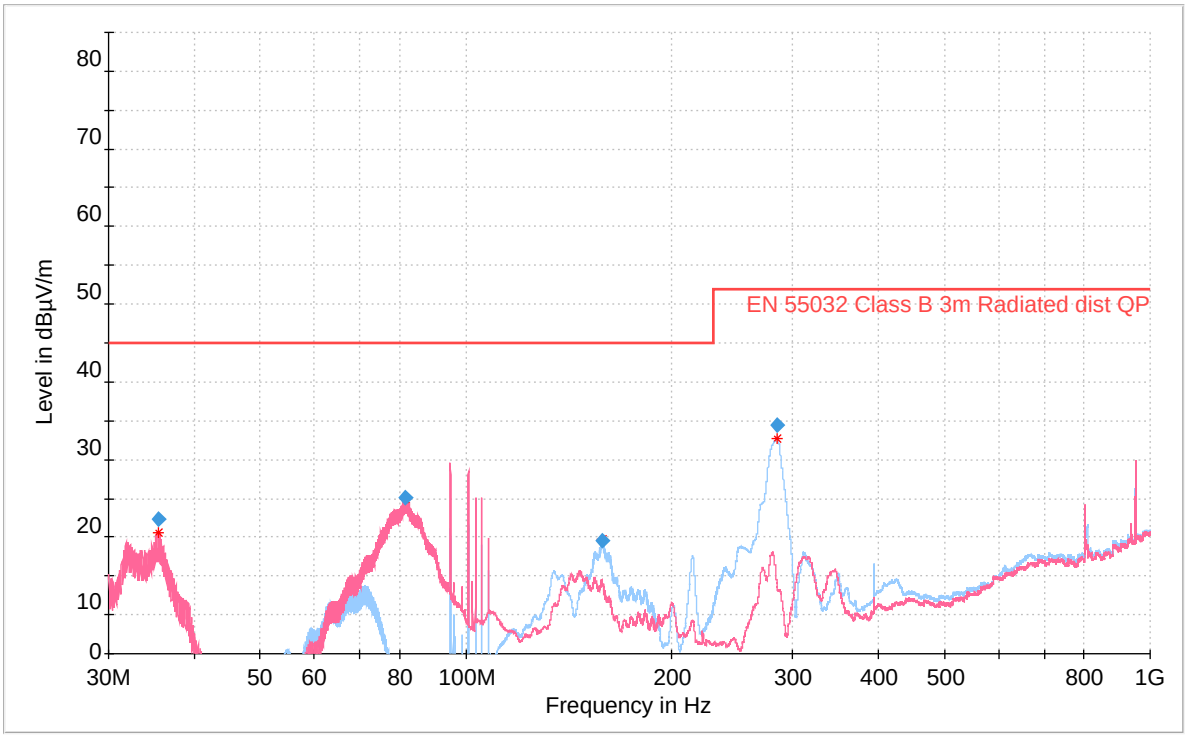


Figure 5.12. Si3406-Buck Non-Isolated EVB Radiated Emissions Measurements Results; 50 V Input, 5 V Output, 6.5 W Input Load

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization). Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

5.15 Conducted Emissions Measurement Results

The Si3406-Buck, 5 V, Class 2 EVB board's conducted emissions have been measured in two different measurement methods to comply with the international EN 55032 standard. The EVB is supplied and measured on its PoE input port as shown in the following figure.

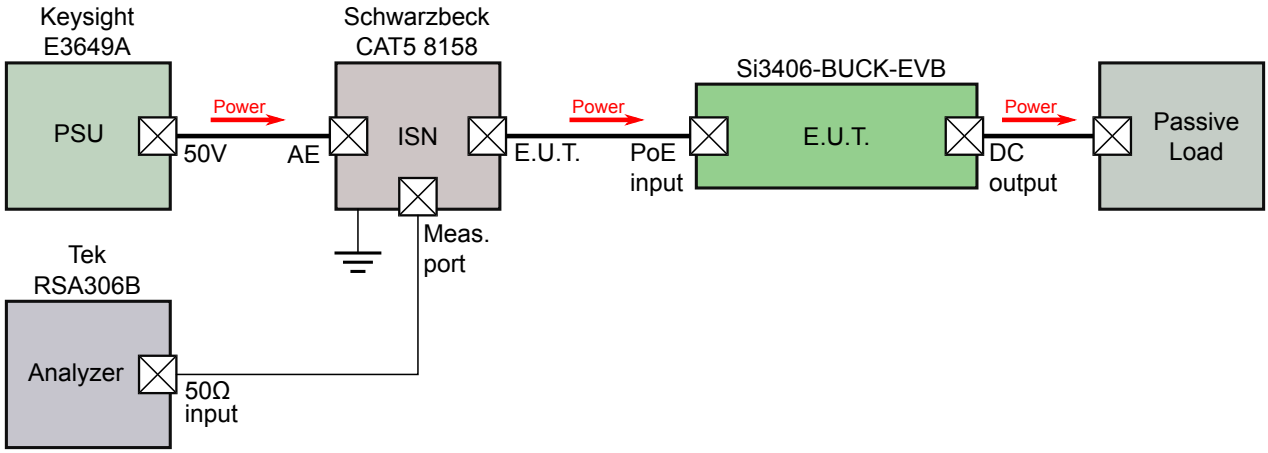


Figure 5.13. Conducted EMI Measurement Setup

The detector in the spectrum analyzer is set to:

- Peak detector and
- Average detector

Both results are shown below.

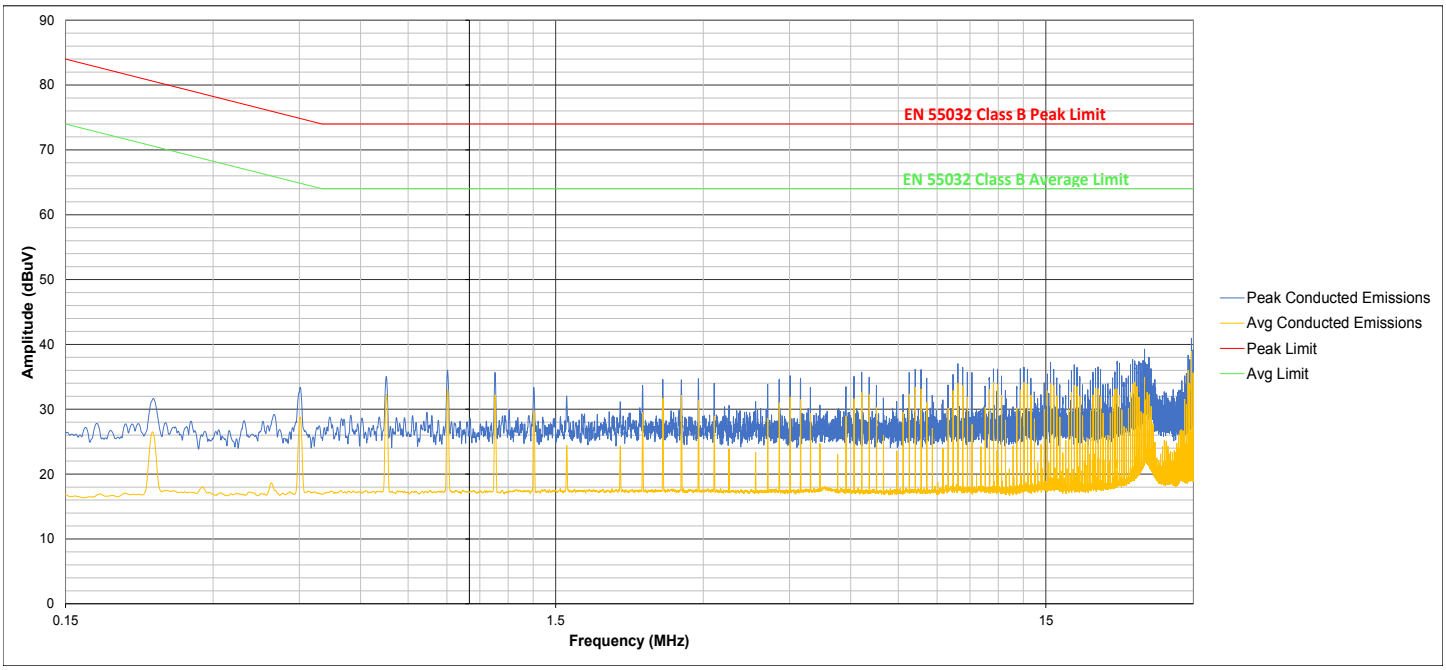


Figure 5.14. Si3406-Buck Non-Isolated EVB Conducted Emissions Measurements Results; 50 V Input, 5 V Output, 6.5 W Input Load

5.16 Bill of Materials

The following table is the BOM listing for the standard 5 V output evaluation board with option PoE Class 2.

Table 5.4. Si3406-BUCK-5 V Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	C1	1 µF		100 V	±10%	X7R	C1210	C1210X7R101-105K	Venkel
1	C13	0.1 µF		100 V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
1	C14	220 pF		50 V	±1%	C0G	C0805	C0805C0G500-221FNE	Venkel
2	C19, C21	0.1 µF		16 V	±10%	X7R	C0805	C0805X7R160-104K	Venkel
1	C2	12 µF		100 V	±20%	Alum_Elec	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
1	C22	200 pF		50 V	±1%	C0G	C0805	C0805C0G500-201FNE	Venkel
2	C4, C5	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel
1	C6	39 pF		25 V	±1%	C0G	C0805	C0805C0G250-390FNP	Venkel
1	C7	47 µF		6.3 V	±20%	X5R	C0805	C0805X5R6R3-476M	Venkel
1	D1	SDT5H100P5	5 A	100 V		Schottky	POWERDI-5	SDT5H100P5-7	Diodes Inc.
1	J1	RJ-45				Receptacle	RJ45-SI-52004	SI-52003-F	Bel
1	L2	47 µH	1.6 A		±20%	Shielded	IND-MSS1038	MSS1038-473ML	Coilcraft
4	L5, L6, L7, L8	330 Ω	1500 mA			SMT	L0805	BLM21PG331SN1	Murata
1	R1	1 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1001F	Venkel
1	R10	88.7 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080588K7FKEA	Vishay
1	R11	75 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-75R0F	Venkel
1	R13	0 Ω	2A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R3	3.24 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW08053K24FKEA	Vishay
1	R4	9.09 kΩ	1/10 W		±0.5%	±25 PPM	R0805	RR1220P-9091-D-M	Susumu
1	R5	10 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-10R0F	Venkel
1	R6	3 Ω	1/8W		±1%	Thick Film	R0805	CR0805-8W-3R00FT	Venkel
1	R7	1.2 Ω	1/10 W		±5%	Thick Film	R0805	CR0805-10W-1R2J	Venkel
1	R8	200 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-2003F	Venkel
1	R9	24.3 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080524K3FKEA	Vishay
4	TP1, TP2, TP11, TP12	Black				Loop	Testpoint	5001	Keystone
1	U1	Si3406		120 V		PD	QFN20N5X5P0.8	Si3406-A-GM	Silicon Labs
Not Installed Components									
1	C20	330 pF		50 V	±1%	C0G	C0805	C0805C0G500-331F	Venkel
1	C3	560 µF		6.3 V	±20%	Alum_Elec	C3.5X8MM-RAD	EEUFM0J561	Panasonic
1	C8	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	R12	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R14	120 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1200F	Venkel
8	TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Black				Loop	Testpoint	5001	Keystone

6. Si3406-Buck EVB: 12 V, Class 2 Configuration

6.1 Si3406-Buck EVB Schematic: 12 V Class 2, 7 W

In the following figure, the schematic of the Si3406-Buck 12 V, Class 2 EVB is shown. The parts in red on the schematic represent the BOM differences compared to the core design.

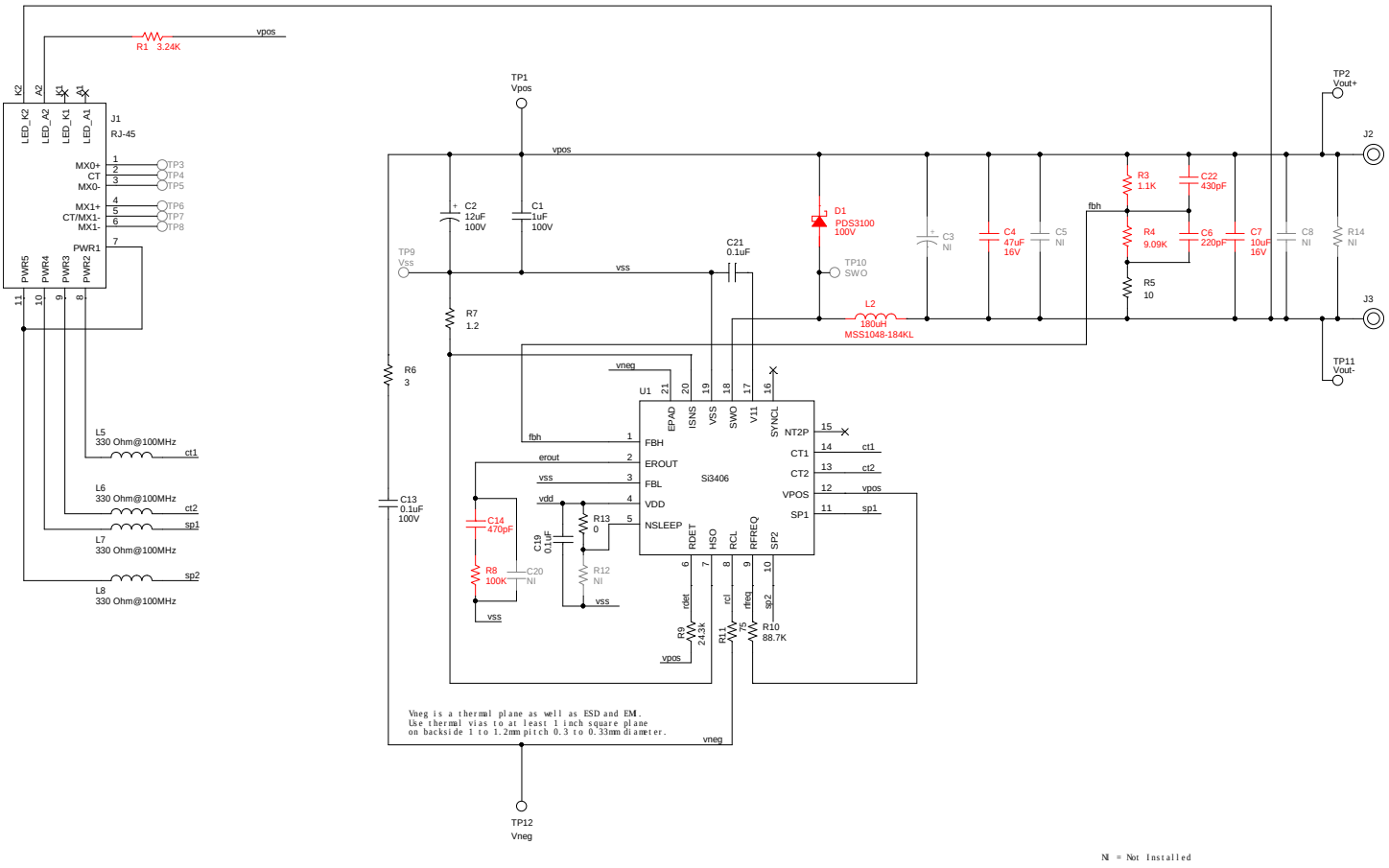


Figure 6.1. Si3406 Buck Non-Isolated EVB Schematic: 12 V, Class 2 PD

6.2 End-to-End EVB Efficiency

The end-to-end conversion efficiency measurement data of the Si3406 12 V Buck board is shown below with internal input bridges. The efficiency was measured at three different input voltage levels: 42 V, 50 V and 57 V.

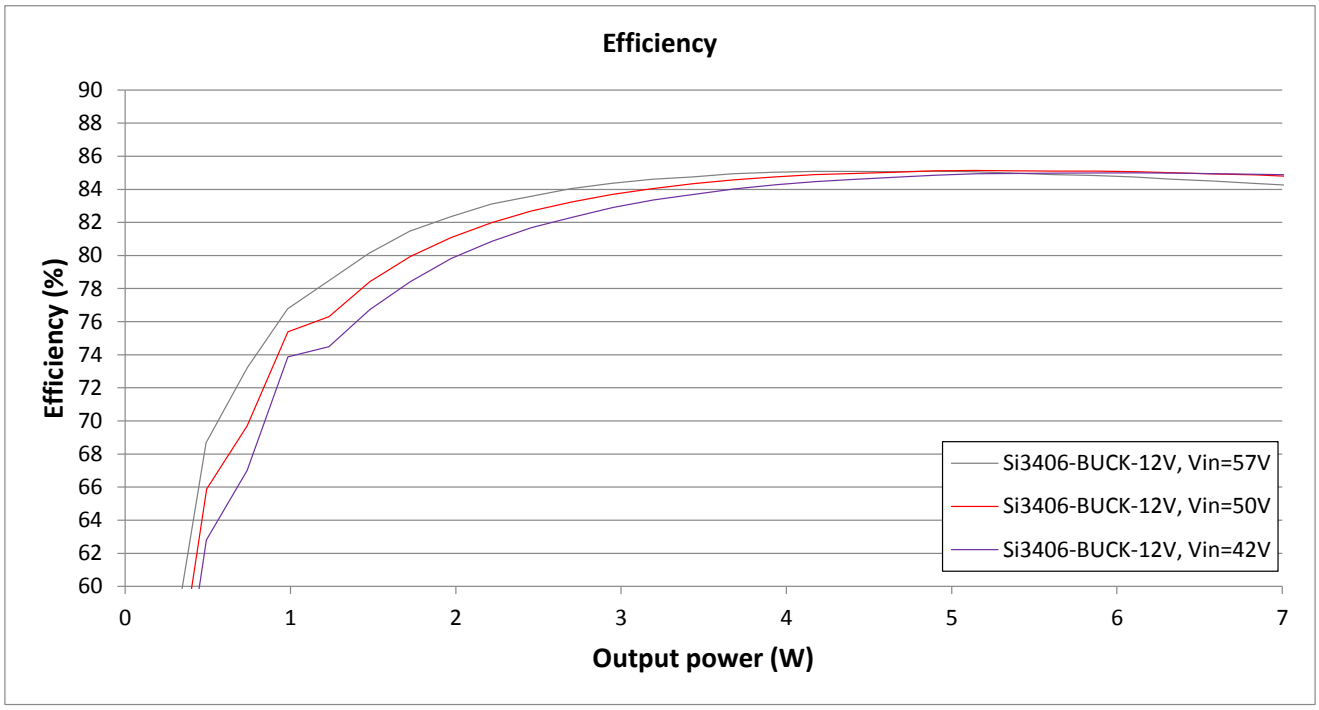


Figure 6.2. Si3406-Buck End-to-End Efficiency Chart with internal Diodes as Input Bridge: 42V, 50 V and 57V Input, 12 V Output, Class 2

Note: The chart shows end-to-end EVB efficiency. The voltage drop of the diode bridge is included. LEDs are removed.

6.3 Thermal Measurements

The Si3406-Buck EVB's temperature was measured at maximum **input power – 6.5 W**. The Si3406-Buck EVB is configured for 12 V output voltage and Class 2 power level. The following figure shows the thermal images taken of the top side of the PCB at maximum input power.

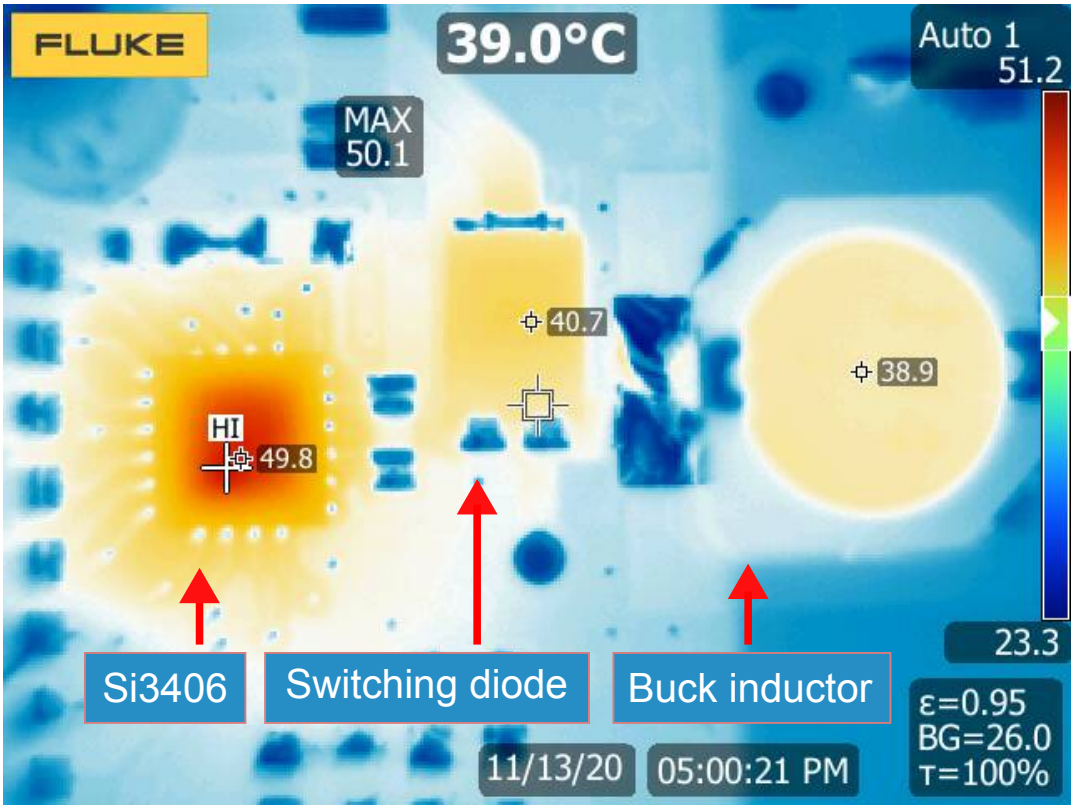


Figure 6.3. Thermal Measurements of the Si3406-Buck Non-Isolated EVB, 12 V, Class 2 PD

The following table lists the temperatures of the notable components across the board.

Table 6.1. Component Temperatures at Full Load

Component	Temperature
Si3406 – U1	50.1 °C
Switching Diode – D1	40.7 °C
Buck Inductor – L2	38.9 °C

Note:
1. The ambient temperature was 26 °C during the thermal measurements.

6.4 SIFOS PoE Compatibility Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices (PD's). The Si3406-Buck-12V EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies.

Table 6.2. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 PD SIFOS PoE Compatibility Test Results

ALT A MDI								
Detection and Classification		PSE Emulation		Pairs	A	Polarity	MDI	Det Cycles	3
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.51	kΩ	24.51	24.51	24.51	23.70	26.30	P
Rdet_final		24.37	kΩ	24.37	24.37	24.37	23.70	26.30	P
Rdet_unpwr		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin		24.62	kΩ	24.62	24.62	24.62	23.70	26.30	P
Rdet_at_Vmax		24.48	kΩ	24.48	24.48	24.48	23.70	26.30	P
Rdet_Voffset		1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet		0.11	µF	0.11	0.11	0.11	0.05	0.12	P
Cdet_final		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification									
Iclass		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
ClassNum		2		2	2	—	0	4	P
Tclass		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability		1					1	1	P
Iclass_at_Vmin		18.7	mA	18.7	18.7	18.7	17.0	20.0	P
Iclass_at_Vmax		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
2 Event Classification									
Iclass_event1		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_event2		18.5	mA	18.5	18.5	18.5	17.0	20.0	P
MarkI		1.54	mA	1.54	1.54	1.54	0.25	4.00	INFO
ClassNum2		2		2	2	—	0	4	P
Tclass_event1		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1		1					1	1	P
ClassStability_event2		1					1	1	P
Power-Up / Down									
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		160.2	mA	160.2	160.2	160.2	0.0	400.0	P
InrushI_2		161.2	mA	161.2	161.2	161.2	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P

Inrush_delayed	0		0	0	—	0	0	P
Von	37.2	VDC	37.2	37.2	37.2	30.0	42.0	P
Voff	36.0	VDC	36.0	36.0	36.0	30.0	42.0	P
Vhyst	1.2	VDC	1.2	1.2	1.2	0.0	12.0	P
BackfeedV	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	9.1	mA	9.1	9.1	9.1	0.0	174.2	P
MaxI_1	14.7	mA	14.7	14.7	14.7	10.0	174.2	P
Vport_1	48.0	VDC	48.0	48.0	48.0	37.0	57.0	INFO
Ppeak_1	0.71	W	0.71	0.71	0.71	0.0	8.4	P
Pavg_1	0.55	W	0.55	0.55	0.55	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.9	mA	2.9	2.9	2.9	0.0	154.7	P
MaxI_2	27.6	mA	27.6	27.6	27.6	10.0	154.7	P
Vport_2	54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2	1.49	W	1.49	1.49	1.49	0.0	8.4	P
Pavg_2	0.58	W	0.58	0.58	0.58	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT A MDI-X								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P
Rdet_final	24.49	kΩ	24.49	24.49	24.49	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	25.02	kΩ	25.02	25.02	25.02	23.70	26.30	P
Rdet_at_Vmax	24.60	kΩ	24.60	24.60	24.60	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.11	µF	0.11	0.11	0.11	0.05	0.12	P

Cdet_final	0.11	µF	0.11	0.11	0.11	0.05	0.12	P
1 Event Classification								
Iclass	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_at_Vmax	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_event2	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
MarkI	1.54	mA	1.54	1.54	1.54	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	159.7	mA	159.7	159.7	159.7	0.0	400.0	P
InrushI_2	161.0	mA	161.0	161.0	161.0	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.6	VDC	37.6	37.6	37.6	30.0	42.0	P
Voff	34.4	VDC	34.4	34.4	34.4	30.0	42.0	P
Vhyst	3.1	VDC	3.1	3.1	3.1	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	9.1	mA	9.1	9.1	9.1	0.0	173.1	P
MaxI_1	14.3	mA	14.3	14.3	14.3	10.0	173.1	P
Vport_1	48.3	VDC	48.3	48.3	48.3	37.0	57.0	INFO
Ppeak_1	0.69	W	0.69	0.69	0.69	0.0	8.4	P
Pavg_1	0.54	W	0.54	0.54	0.54	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P

DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.9	mA	2.9	2.9	2.9	0.0	154.0	P
MaxI_2	28.4	mA	28.4	28.4	28.4	10.0	154.0	P
Vport_2	54.4	VDC	54.4	54.4	54.4	42.5	57.0	INFO
Ppeak_2	1.54	W	1.54	1.54	1.54	0.0	8.4	P
Pavg_2	0.59	W	0.59	0.59	0.59	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT B MDI								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.40	kΩ	24.40	24.40	24.40	23.70	26.30	P
Rdet_final	24.37	kΩ	24.37	24.37	24.37	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.90	kΩ	24.90	24.90	24.90	23.70	26.30	P
Rdet_at_Vmax	24.64	kΩ	24.64	24.64	24.64	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.11	µF	0.11	0.11	0.11	0.05	0.12	P
Cdet_final	0.11	µF	0.11	0.11	0.11	0.05	0.12	P
1 Event Classification								
Iclass	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.8	mA	18.8	18.8	18.8	17.0	20.0	P
Iclass_at_Vmax	18.3	mA	18.3	18.3	18.3	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_event2	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
MarkI	1.62	mA	1.62	1.62	1.62	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P

ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		160.1	mA	160.1	160.1	160.1	0.0	400.0	P
InrushI_2		161.4	mA	161.4	161.4	161.4	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed		0		0	0	—	0	0	P
Von		37.3	VDC	37.3	37.3	37.3	30.0	42.0	P
Voff		33.6	VDC	33.6	33.6	33.6	30.0	42.0	P
Vhyst		3.7	VDC	3.7	3.7	3.7	0.0	12.0	P
BackfeedV		0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover		0		0	0	—	0	0	P
SigRecoverTime		0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1		**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1		8.7	mA	8.7	8.7	8.7	0.0	174.2	P
MaxI_1		14.1	mA	14.1	14.1	14.1	10.0	174.2	P
Vport_1		47.9	VDC	47.9	47.9	47.9	37.0	57.0	INFO
Ppeak_1		0.67	W	0.67	0.67	0.67	0.0	8.4	P
Pavg_1		0.52	W	0.52	0.52	0.52	0.0	6.5	P
MPSViolation_1		0		0	0	—	0	0	P
TcutWindowViolation_1		0		0	0	—	0	0	P
DutyCycleViolation_1		0		0	0	—	0	0	P
MDI Powered Type-2 PHY		**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2		2.4	mA	2.4	2.4	2.4	0.0	154.8	P
MaxI_2		27.2	mA	27.2	27.2	27.2	10.0	154.8	P
Vport_2		54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2		1.47	W	1.47	1.47	1.47	0.0	8.4	P
Pavg_2		0.56	W	0.56	0.56	0.56	0.0	6.5	P
MPSViolation_2		0		0	0	—	0	0	P
TcutWindowViolation_2		0		0	0	—	0	0	P
DutyCycleViolation_2		0		0	0	—	0	0	P
ALT B MDI-X									
Detection and Classification		**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.35	kΩ	24.35	24.35	24.35	23.70	26.30	P

Rdet_final	24.42	kΩ	24.42	24.42	24.42	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.89	kΩ	24.89	24.89	24.89	23.70	26.30	P
Rdet_at_Vmax	24.58	kΩ	24.58	24.58	24.58	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.11	µF	0.11	0.11	0.11	0.05	0.12	P
Cdet_final	0.11	µF	0.11	0.11	0.11	0.05	0.12	P
1 Event Classification								
Iclass	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.1	mA	18.1	18.1	18.1	17.0	20.0	P
Iclass_at_Vmax	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
Iclass_event2	18.6	mA	18.6	18.6	18.6	17.0	20.0	P
MarkI	1.61	mA	1.61	1.61	1.61	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	159.8	mA	159.8	159.8	159.8	0.0	400.0	P
InrushI_2	161.4	mA	161.4	161.4	161.4	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.9	VDC	37.9	37.9	37.9	30.0	42.0	P
Voff	33.8	VDC	33.8	33.8	33.8	30.0	42.0	P
Vhyst	4.1	VDC	4.1	4.1	4.1	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	8.3	mA	8.3	8.3	8.3	0.0	173.4	P

MaxI_1	13.9	mA	13.9	13.9	13.9	10.0	173.4	P
Vport_1	48.2	VDC	48.2	48.2	48.2	37.0	57.0	INFO
Ppeak_1	0.67	W	0.67	0.67	0.67	0.0	8.4	P
Pavg_1	0.52	W	0.52	0.52	0.52	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.3	mA	2.3	2.3	2.3	0.0	154.3	P
MaxI_2	26.4	mA	26.4	26.4	26.4	10.0	154.3	P
Vport_2	54.3	VDC	54.3	54.3	54.3	42.5	57.0	INFO
Ppeak_2	1.43	W	1.43	1.43	1.43	0.0	8.4	P
Pavg_2	0.56	W	0.56	0.56	0.56	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P

6.5 Adjustable EVB Current Limit

For additional safety, the Si3406 has an adjustable EVB current limit feature.

The Si3406 controller measures the voltage on the R_{SENSE} resistor (R7) through the ISNS pin. Care must be taken that this voltage goes below V_{SS}. When the voltage on R7 is V_{ISNS} = –270 mV (referenced to V_{SS}), the internal current limit circuit restarts the PD to protect the application.

The EVB current limit for this Class 2 application can be calculated with the following formula:

$$R_{SENSE} = 1.2\Omega$$

$$I_{LIMIT} = \frac{270mV}{1.2\Omega} = \quad 225mA$$

Equation 6.1. EVB Class 2 Current Limit

6.6 Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si3406 device integrates a current-mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee stable output voltage of the power supply and to reduce the influence of the input voltage variations and load changes on the output voltage, the feedback loop should be stable.

To verify the stability of the loop, the gain and loop phase of the loop has been measured.

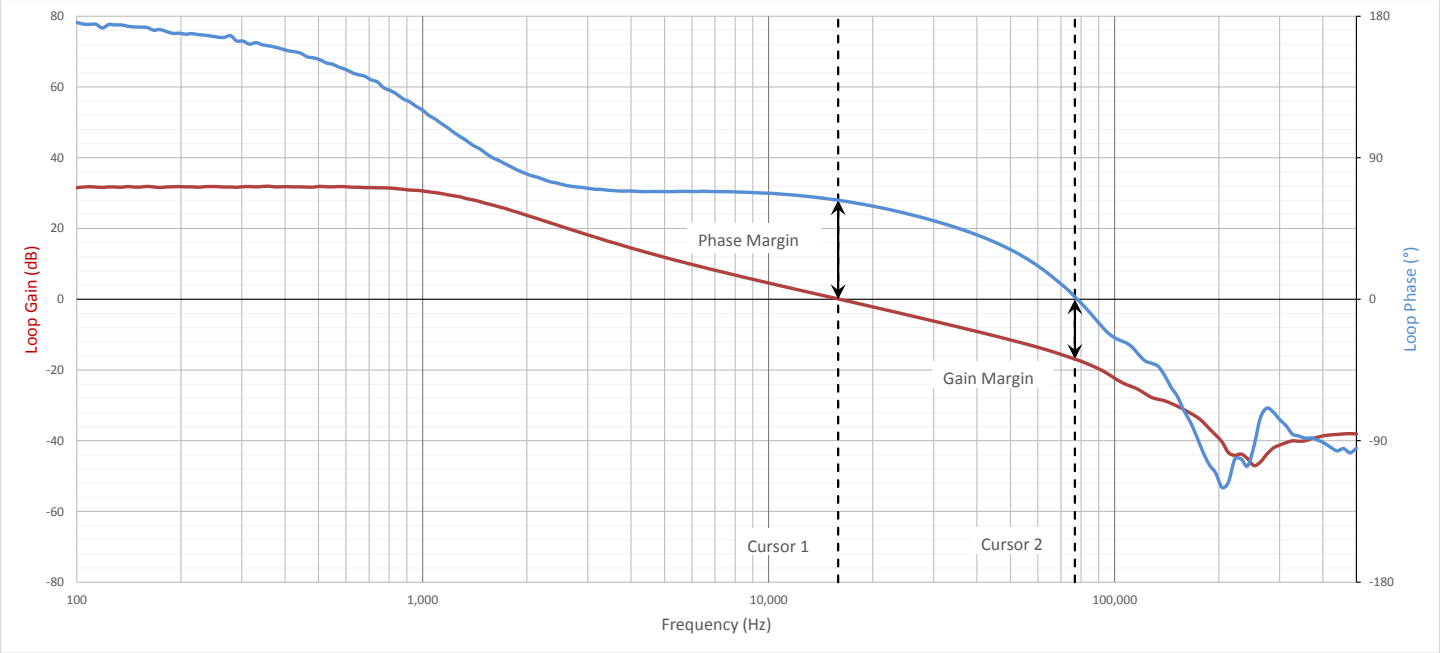


Figure 6.4. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 PD Feedback Loop Measurement Results at Full Load

Table 6.3. Measured Loop Gain and Phase Margin

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	15.88 kHz	0 dB	63.01°
Cursor 2 (Gain Margin)	76.77 kHz	–16.90 dB	0 °

6.7 Load Step Transient Measurement Results

The Si3406-Buck EVB board's output has been tested with a load step function to verify the converter's output dynamic response.

Load Step: from 0.05 A to 0.41 A Output Current:
ΔV_{OUT} = 209.55 mV

Load Step, from 0.41 A to 0.05 A Output Current:
ΔV_{OUT} = 185.43 mV

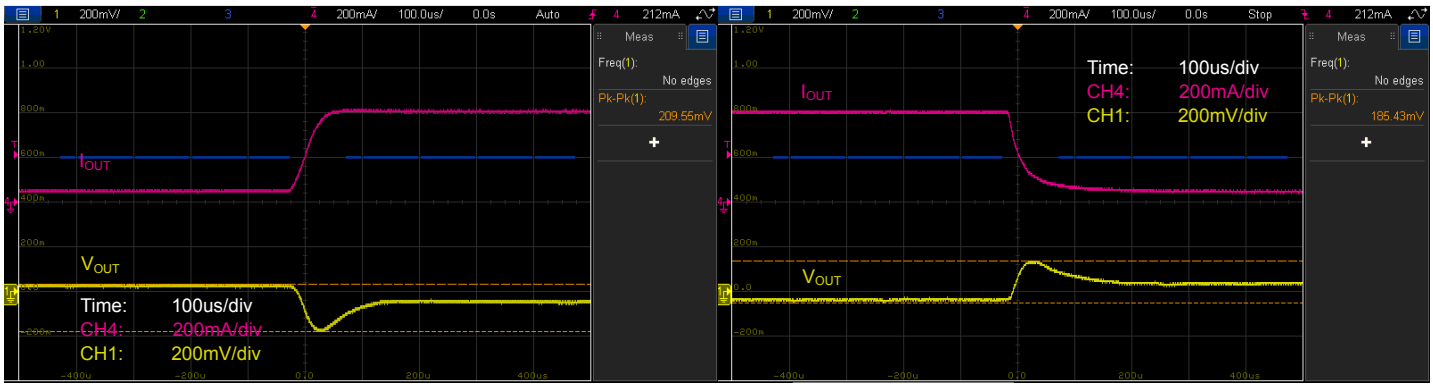


Figure 6.5. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 PD Output Load Step Transient Test

6.8 Output Voltage Ripple

The Si3406-Buck EVB output voltage ripple has been measured in both no-load and heavy-load conditions.

No-Load V_{OUT} Ripple = 88.19 mV **Heavy-Load V_{OUT} Ripple = 7.95 mV**

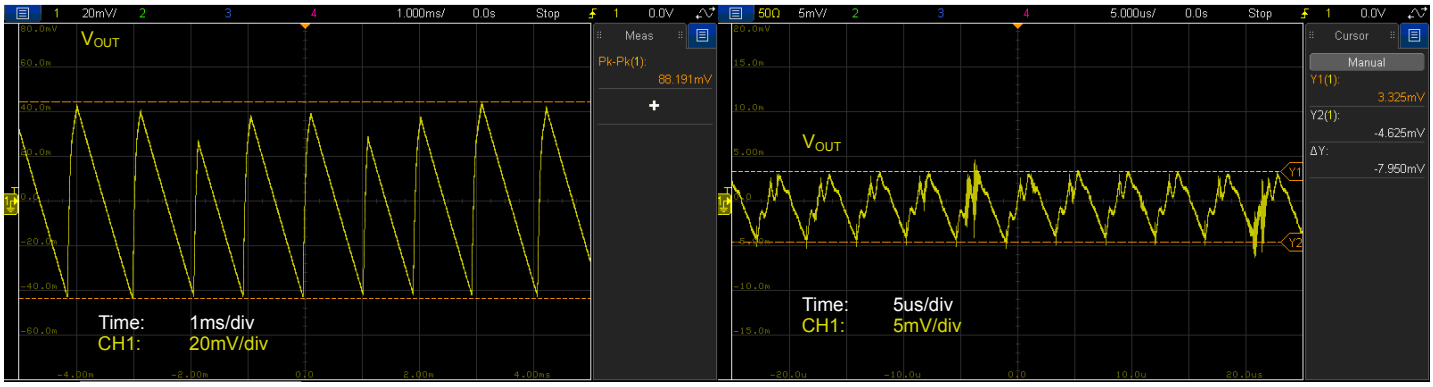


Figure 6.6. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 Output Voltage Ripple No-Load (Left) and Heavy-Load (Right) Conditions

6.9 Soft-Start Protection

The Si3406 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

The Si3406 intelligent adaptive soft-start mechanism does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, that way adjusting the output voltage ramping up time in a function of the attached load.

The controller lets the output voltage to rise faster in no-load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

No-Load Soft-Start:
t_{RISE} = 3.81 ms

Heavy-Load Soft-Start:
t_{RISE} = 37.5 ms

Figure 6.7. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 Output Voltage Soft-Start at Low-Load (Left) and Heavy-Load (Right) Conditions

6.10 Output Short Protection

The Si3406 device has an integrated output short protection mechanism, which protects the IC itself and the surrounding external components from overheating in the case of electrical short on the output.

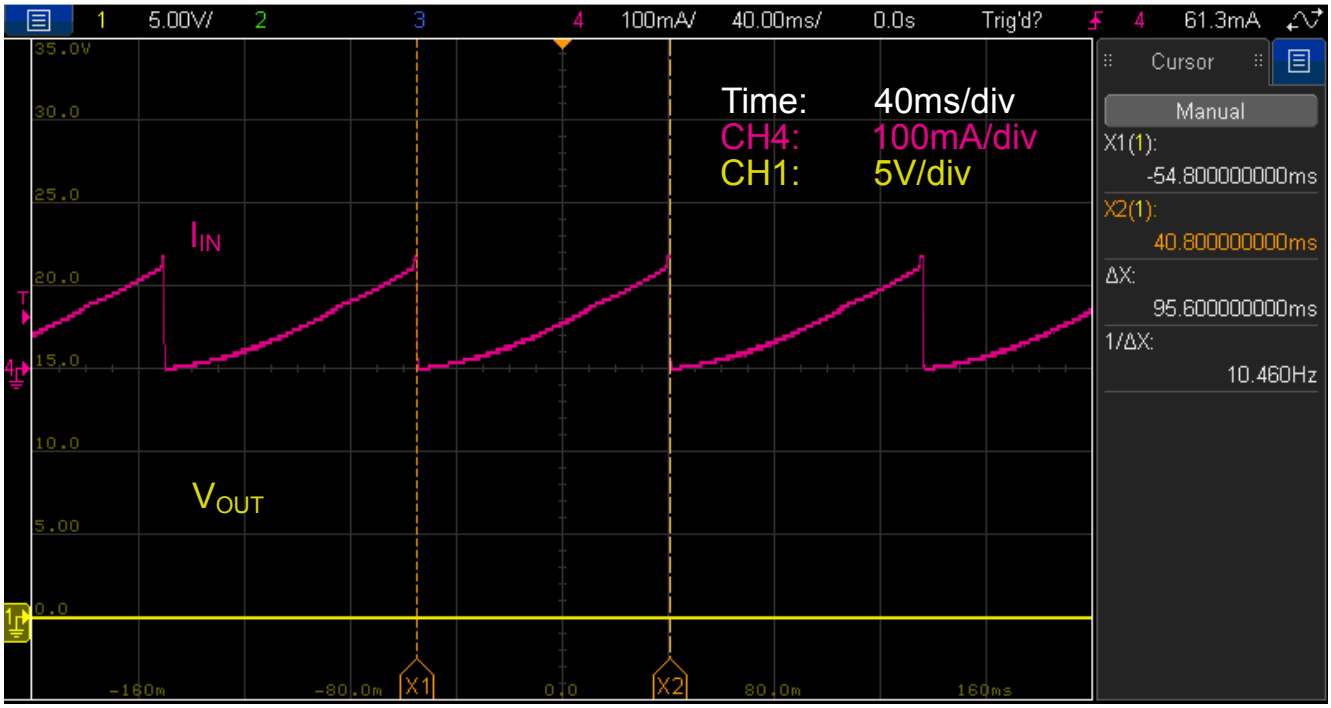


Figure 6.8. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 Output Short Circuit Protection

6.11 Pulse Skipping at No-Load Condition

The Si3406 device has an integrated pulse skipping mechanism to ensure ultra-low power consumption at light load condition.

As the output load decreases, the controller starts to reduce the pulse-width of the PWM signal (switcher ON time). At some point, even the minimum width pulse would provide higher energy than the application requires, which could result in loss of voltage regulation.

When the controller detects light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or light-load skipping mode. This mode is shown in the following figure by depicting the switching node of the integrated switching FET at no load condition.

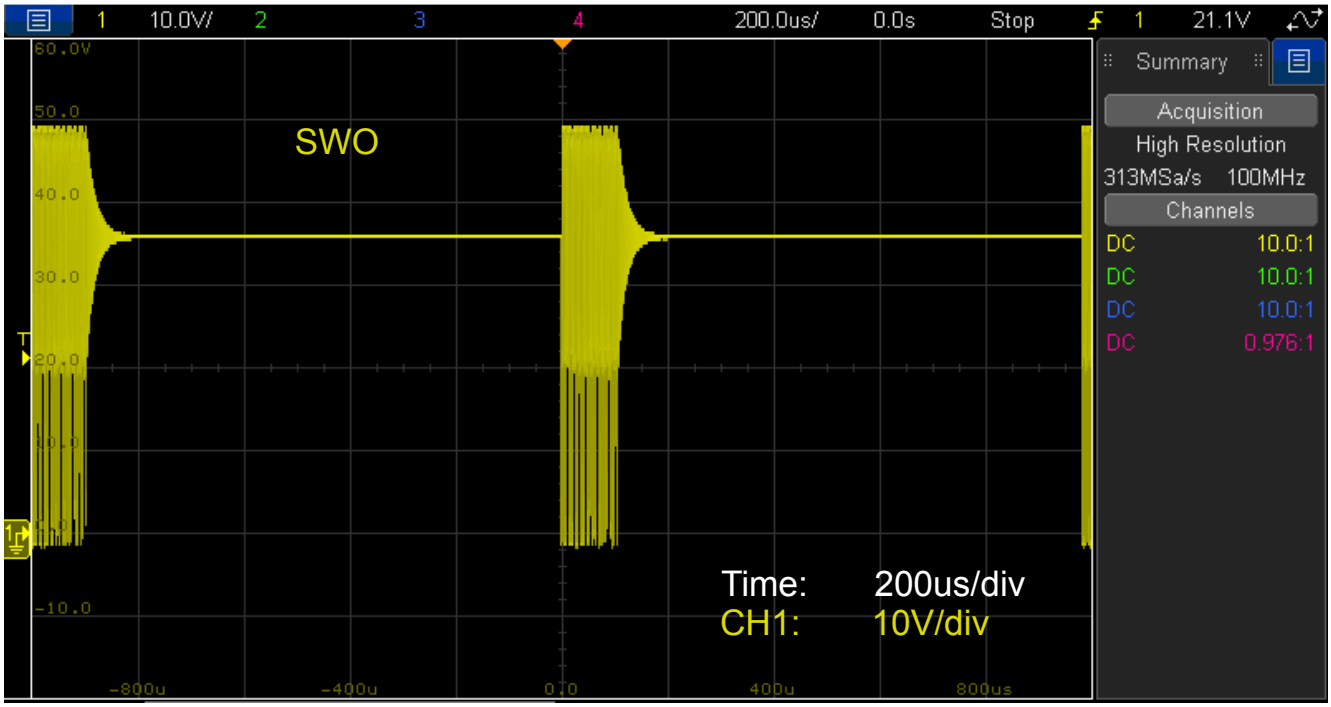


Figure 6.9. Si3406-Buck Non-Isolated EVB, 12 V, Class 2 Pulse Skipping at No-load Condition: SWO Waveform

6.12 Discontinuous (DCM) and Continuous (CCM) Current Modes

At low load, the converter works in discontinuous current mode (DCM). At heavy load, the converter runs in continuous current mode (CCM). At low load, the SWO voltage waveform has a ringing waveform, which is typical for DCM operation.

Low-Load, DCM **Heavy-Load, CCM**

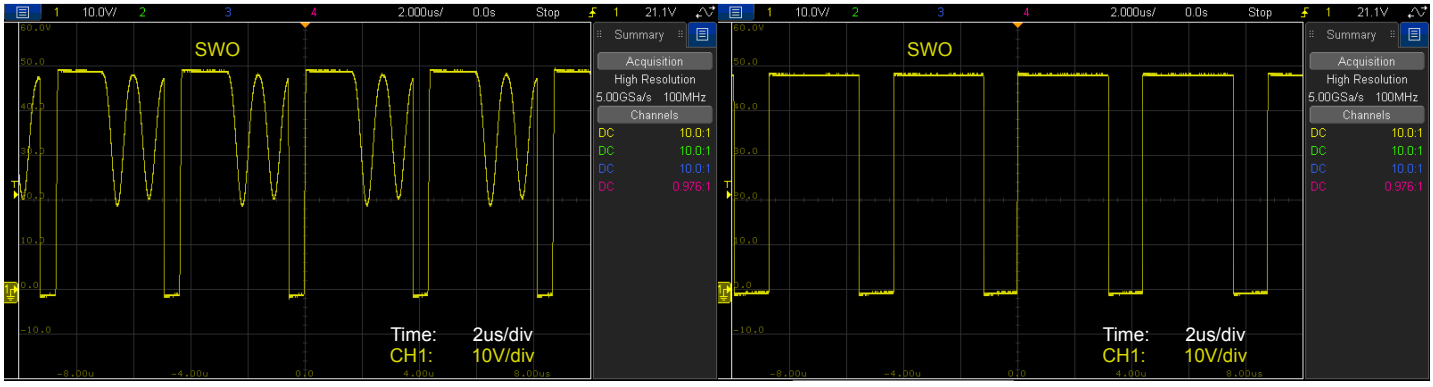


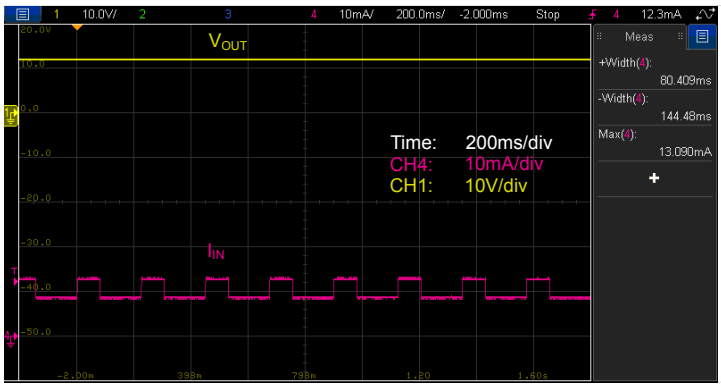
Figure 6.10. Si3406-Buck Non-Isolated EVB, 12 V, Class 2: SWO Waveform in Discontinuous Current Mode (DCM) at Low Load (Left), and in Continuous Current Mode (CCM) at Heavy Load (Right)

6.13 Maintain Power Signature (MPS)

The Si3406-Buck EVB board has a built-in MPS feature that enables the Si3406 to maintain the connection with the PSE when the PD is in a low-current consumption mode. MPS can be used in user mode or in automatic mode. In user mode, nSLEEP shall be tied to VDD at startup (R13), and the host controller needs to manually start/stop MPS generation by pulling the nSLEEP line low or high respectively. To enable the automatic MPS feature, nSLEEP shall be tied to VSS at startup (R12). In automatic mode, the Si3406 monitors the input current and turns off MPS automatically when it is below a predefined level.

Note: Si3406 assumes a minimum consumption of the host controller therefore to pass Sifos MPS tests, a dummy load is recommended to be installed on the EVB (R14) to keep the consumption above the predefined current threshold. The figure below shows the automatic MPS pulses generated by the EVB when a 750 Ω dummy load is installed.

Automatic MPS Pulse Generation by Si3406
V_{ON} = 80.41 ms, V_{OFF} = 144.48 ms, I_{MAX} = 13.09 mA



Automatic MPS Pulse Generation by Si3406
Sifos Startup Trace

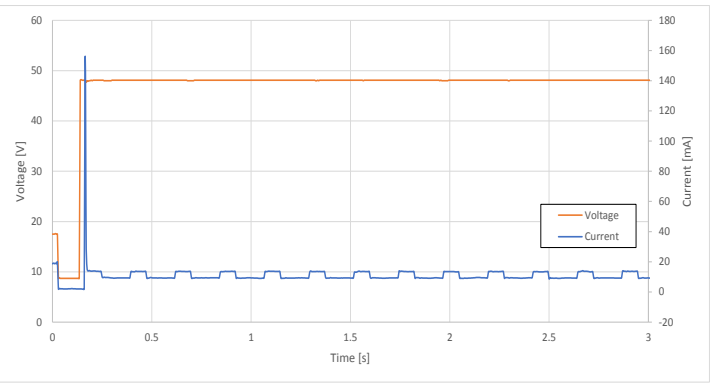


Figure 6.11. Si3406-Buck Non-Isolated EVB, 5 V, Class 2 PD Automatic Maintain Power Signature (MPS) Generation

6.14 Radiated Emissions Measurement Results

Radiated emissions have been measured of the Si3406-Buck, 12 V, Class 2 EVB board with 50 V input voltage and full load connected to the output – 6.5 W.

As shown in the following figure, the Si3406-Buck, 12 V, Class 2 EVB is fully compliant with the international EN 55032 class B emissions standard.

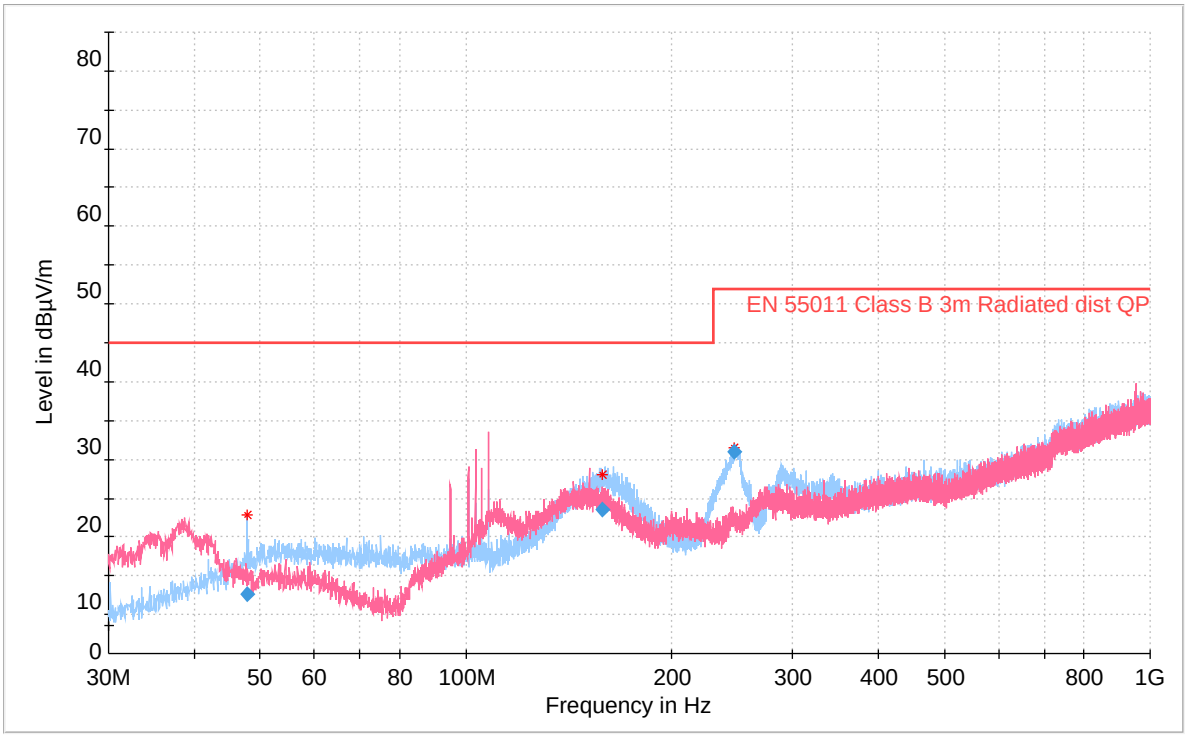


Figure 6.12. Si3406-Buck Non-Isolated EVB Radiated Emissions Measurements Results; 50 V Input, 12 V Output, 6.5 W Input Load

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization). Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

6.15 Conducted Emissions Measurement Results

The Si3406-Buck, 12 V, Class 2 EVB board's conducted emissions have been measured in two different measurement methods to comply with the international EN 55032 standard. The EVB is supplied and measured on its PoE input port as shown in the following figure.

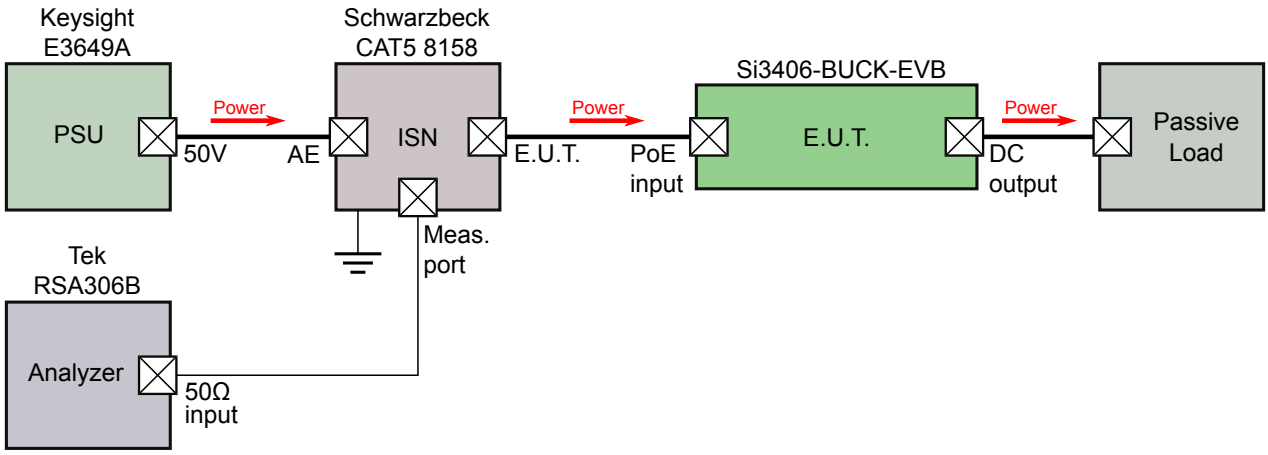


Figure 6.13. Conducted EMI Measurement Setup

The detector in the spectrum analyzer is set to:

- Peak detector and
- Average detector

Both results are shown below.

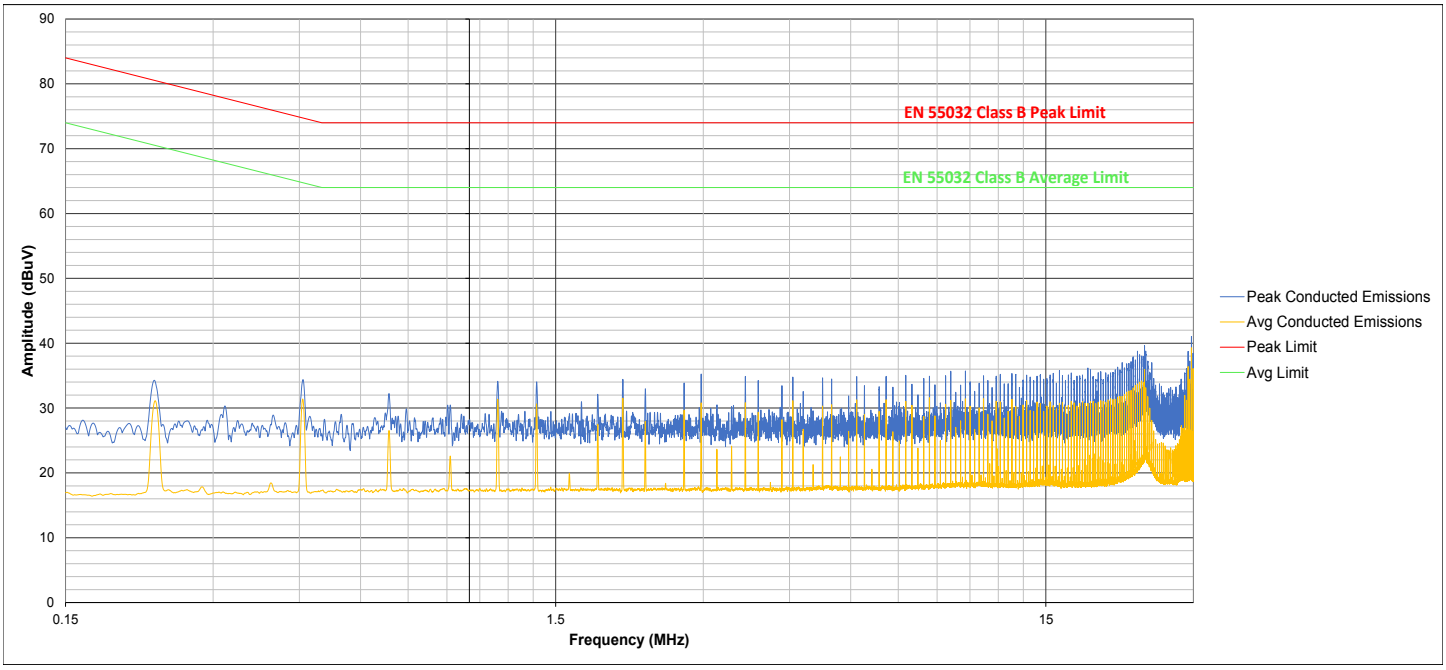


Figure 6.14. Si3406-Buck Non-Isolated EVB Conducted Emissions Measurements Results; 50 V Input, 12 V Output, 6.5 W Input Load

6.16 Bill of Materials

The following table is the BOM listing for the standard 12 V output evaluation board with option PoE Class 2.

Table 6.4. Si3406-BUCK-12 V Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	C1	1 µF		100 V	±10%	X7R	C1210	C1210X7R101-105K	Venkel
1	C13	0.1 µF		100 V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
1	C14	470 pF		50 V	±1%	C0G	C0805	C0805C0G500-471F	Venkel
2	C19, C21	0.1 µF		16 V	±10%	X7R	C0805	C0805X7R160-104K	Venkel
1	C2	12 µF		100 V	±20%	Alum_Elec	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
1	C22	430 pF		50 V	±2%	C0G	C0805	C0805C0G500-431GNP	Venkel
1	C4	47 µF		16 V	±20%	X5R	C1210	C1210X5R160-476MNE	Venkel
1	C6	220 pF		50 V	±1%	C0G	C0805	C0805C0G500-221FNE	Venkel
1	C7	10 µF		16 V	±10%	X5R	C0805	C0805X5R160-106K	Venkel
1	D1	PDS3100	3 A	100 V		Schottky	POWERDI-5	PDS3100-13	Diodes Inc.
1	J1	RJ-45				Receptacle	RJ45-SI-52004	SI-52003-F	Bel
1	L2	180 µH	0.75 A		±10%	Shielded	IND-MSS1038	MSS1048-184KL	Coilcraft
4	L5, L6, L7, L8	330 Ω	1500 mA			SMT	L0805	BLM21PG331SN1	Murata
1	R1	3.24 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW08053K24FKEA	Vishay
1	R10	88.7 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080588K7FKEA	Vishay
1	R11	75 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-75R0F	Venkel
1	R13	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R3	1.1 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1101F	Venkel
1	R4	9.09 kΩ	1/10 W		±0.5%	±25 PPM	R0805	RR1220P-9091-D-M	Susumu
1	R5	10 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-10R0F	Venkel
1	R6	3 Ω	1/8 W		±1%	Thick Film	R0805	CR0805-8W-3R00FT	Venkel
1	R7	1.2 Ω	1/10 W		±5%	Thick Film	R0805	CR0805-10W-1R2J	Venkel
1	R8	100 kΩ	1/8 W		±1%	Thick Film	R0805	CR0805-8W-1003F	Venkel
1	R9	24.3 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080524K3FKEA	Vishay
4	TP1, TP2, TP11, TP12	Black				Loop	Testpoint	5001	Keystone
1	U1	Si3406		120 V		PD	QFN20N5X5P0.8	Si3406-A-GM	Silicon Labs
Not Installed Components									
1	C20	330 pF		50 V	±1%	C0G	C0805	C0805C0G500-331F	Venkel
1	C3	560 µF		6.3 V	±20%	Alum_Elec	C3.5X8MM-RAD	EEUFM0J561	Panasonic
2	C5, C8	100 µF		6.3 V	±10%	X5R	C1210	C1210X5R6R3-107K	Venkel

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	R12	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R14	120 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1200F	Venkel
8	TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Black				Loop	Testpoint	5001	Keystone

7. Si3406-Buck EVB: 24 V, Class 2 Configuration

7.1 Si3406-Buck EVB Schematic: 24V, Class 2, 7W

In the following figure, the schematic of the Si3406-Buck 24V, Class 2 EVB is shown. The parts in red on the schematic represent the BOM differences compared to the core design.

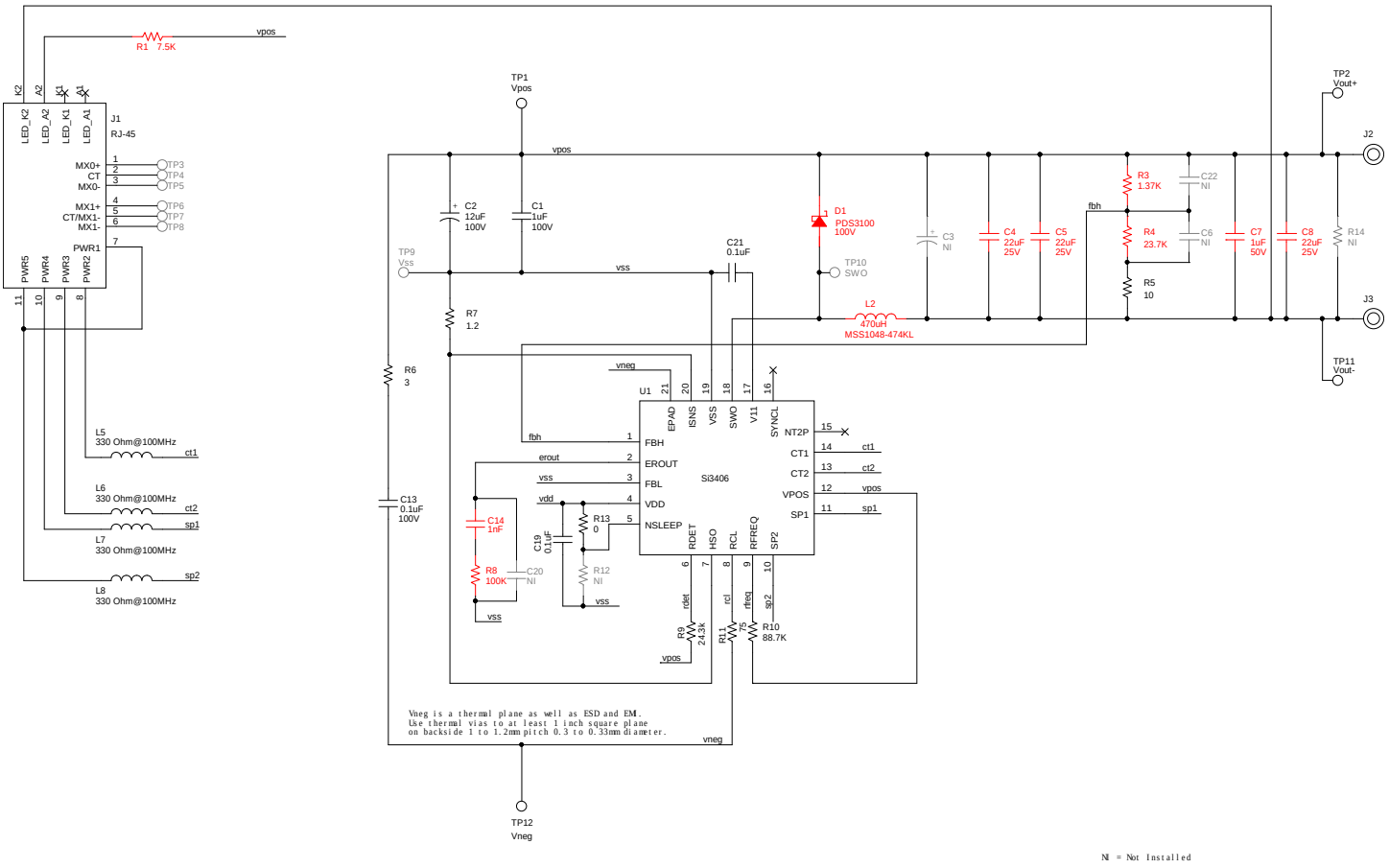


Figure 7.1. Si3406 Buck Non-Isolated EVB Schematic: 24 V, Class 2 PD

7.2 End-to-End EVB Efficiency

The end-to-end conversion efficiency measurement data of the Si3406 24 V Buck board is shown below with internal input bridges. The efficiency was measured at three different input voltage levels: 42 V, 50 V and 57 V.

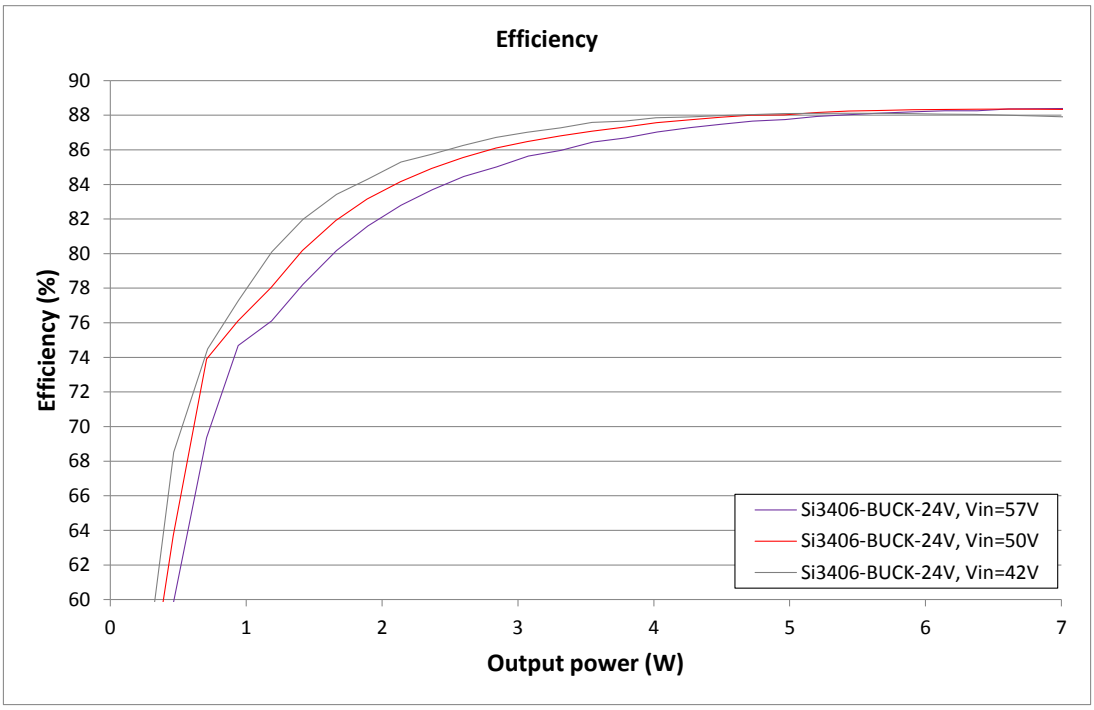


Figure 7.2. Si3406-Buck EVB End-to-End Efficiency Chart with internal Input Bridge Diodes: 42 V, 50 V, and 57 V Input, 24 V Output, Class 2

Note: The chart shows end-to-end EVB efficiency. The voltage drop of the diode bridge is included. LEDs are removed.

7.3 Thermal Measurements

The Si3406-Buck EVB's temperature was measured at maximum **input power – 6.5 W**. The Si3406-Buck EVB is configured for 24 V output voltage and Class 2 power level. The following figure shows the thermal images taken of the top side of the PCB at maximum input power.

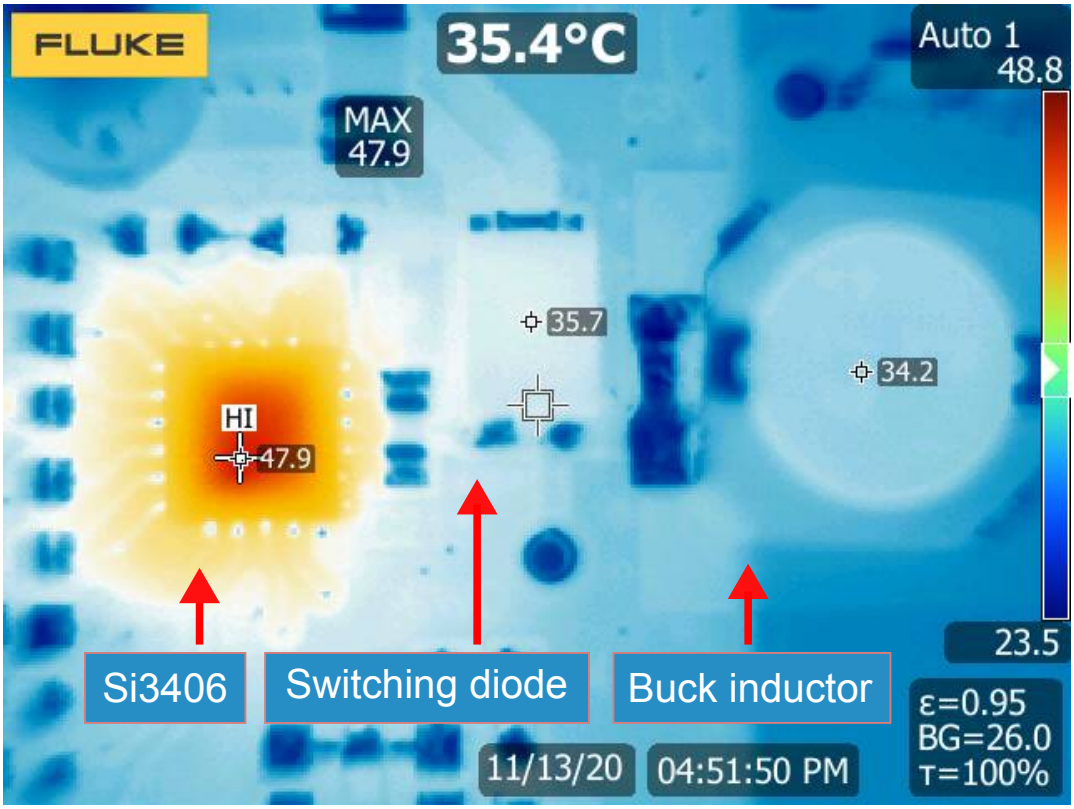


Figure 7.3. Thermal Measurements of the Si3406-Buck Non-Isolated EVB, 24 V, Class 2 PD

The following table lists the temperatures of the notable components across the board.

Table 7.1. Component Temperatures at Full Load

Component	Temperature
Si3406 – U1	47.9 °C
Switching Diode – D1	35.7 °C
Buck Inductor – L2	34.2 °C

Note:
1. The ambient temperature was 26 °C during the thermal measurements.

7.4 SIFOS PoE Compatibility Test Results

The PDA-604A Powered Device Analyzer is a single-box comprehensive solution for testing IEEE 802.3at and IEEE 802.3bt PoE Powered Devices (PD's). The Si3406-Buck-24V EVB board has been successfully tested with the PDA-604A Powered Device Analyzer from SIFOS Technologies.

Table 7.2. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 PD SIFOS PoE Compatibility Test Results

ALT A MDI									
Detection and Classification		PSE Emulation		Pairs	A	Polarity	MDI	Det Cycles	3
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.44	kΩ	24.44	24.44	24.44	23.70	26.30	P
Rdet_final		24.51	kΩ	24.51	24.51	24.51	23.70	26.30	P
Rdet_unpwr		>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin		24.80	kΩ	24.80	24.80	24.80	23.70	26.30	P
Rdet_at_Vmax		24.48	kΩ	24.48	24.48	24.48	23.70	26.30	P
Rdet_Voffset		1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final		0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification									
Iclass		18.1	mA	18.1	18.1	18.1	17.0	20.0	P
ClassNum		2		2	2	—	0	4	P
Tclass		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability		1					1	1	P
Iclass_at_Vmin		18.2	mA	18.2	18.2	18.2	17.0	20.0	P
Iclass_at_Vmax		18.0	mA	18.0	18.0	18.0	17.0	20.0	P
2 Event Classification									
Iclass_event1		18.1	mA	18.1	18.1	18.1	17.0	20.0	P
Iclass_event2		18.1	mA	18.1	18.1	18.1	17.0	20.0	P
MarkI		1.47	mA	1.47	1.47	1.47	0.25	4.00	INFO
ClassNum2		2		2	2	—	0	4	P
Tclass_event1		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2		0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1		1					1	1	P
ClassStability_event2		1					1	1	P
Power-Up / Down									
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		160.4	mA	160.4	160.4	160.4	0.0	400.0	P
InrushI_2		161.3	mA	161.3	161.3	161.3	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P

Inrush_delayed	0		0	0	—	0	0	P
Von	37.3	VDC	37.3	37.3	37.3	30.0	42.0	P
Voff	33.2	VDC	33.2	33.2	33.2	30.0	42.0	P
Vhyst	4.0	VDC	4.0	4.0	4.0	0.0	12.0	P
BackfeedV	0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	8.3	mA	8.3	8.3	8.3	0.0	173.9	P
MaxI_1	13.9	mA	13.9	13.9	13.9	10.0	173.9	P
Vport_1	48.1	VDC	48.1	48.1	48.1	37.0	57.0	INFO
Ppeak_1	0.67	W	0.67	0.67	0.67	0.0	8.4	P
Pavg_1	0.51	W	0.51	0.51	0.51	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.7	mA	2.7	2.7	2.7	0.0	154.5	P
MaxI_2	24.8	mA	24.8	24.8	24.8	10.0	154.5	P
Vport_2	54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2	1.34	W	1.34	1.34	1.34	0.0	8.4	P
Pavg_2	0.54	W	0.54	0.54	0.54	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT A MDI-X								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.42	kΩ	24.42	24.42	24.42	23.70	26.30	P
Rdet_final	24.46	kΩ	24.46	24.46	24.46	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.83	kΩ	24.83	24.83	24.83	23.70	26.30	P
Rdet_at_Vmax	24.58	kΩ	24.58	24.58	24.58	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P

Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.1	mA	18.1	18.1	18.1	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.7	mA	18.7	18.7	18.7	17.0	20.0	P
Iclass_at_Vmax	18.1	mA	18.1	18.1	18.1	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.1	mA	18.1	18.1	18.1	17.0	20.0	P
Iclass_event2	18.1	mA	18.1	18.1	18.1	17.0	20.0	P
MarkI	1.48	mA	1.48	1.48	1.48	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	160.0	mA	160.0	160.0	160.0	0.0	400.0	P
InrushI_2	161.6	mA	161.6	161.6	161.6	0.0	400.0	P
Pmax_Tdelay	0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.4	VDC	37.4	37.4	37.4	30.0	42.0	P
Voff	33.4	VDC	33.4	33.4	33.4	30.0	42.0	P
Vhyst	4.1	VDC	4.1	4.1	4.1	0.0	12.0	P
BackfeedV	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	7.9	mA	7.9	7.9	7.9	0.0	173.4	P
MaxI_1	13.7	mA	13.7	13.7	13.7	10.0	173.4	P
Vport_1	48.2	VDC	48.2	48.2	48.2	37.0	57.0	INFO
Ppeak_1	0.66	W	0.66	0.66	0.66	0.0	8.4	P
Pavg_1	0.50	W	0.50	0.50	0.50	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P

DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.6	mA	2.6	2.6	2.6	0.0	154.3	P
MaxI_2	25.2	mA	25.2	25.2	25.2	10.0	154.3	P
Vport_2	54.2	VDC	54.2	54.2	54.2	42.5	57.0	INFO
Ppeak_2	1.37	W	1.37	1.37	1.37	0.0	8.4	P
Pavg_2	0.54	W	0.54	0.54	0.54	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P
ALT B MDI								
Detection and Classification	**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet	24.58	kΩ	24.58	24.58	24.58	23.70	26.30	P
Rdet_final	24.46	kΩ	24.46	24.46	24.46	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.84	kΩ	24.84	24.84	24.84	23.70	26.30	P
Rdet_at_Vmax	24.61	kΩ	24.61	24.61	24.61	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.5	mA	18.5	18.5	18.5	17.0	20.0	P
Iclass_at_Vmax	17.8	mA	17.8	17.8	17.8	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
Iclass_event2	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
MarkI	1.55	mA	1.55	1.55	1.55	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P

ClassStability_event2		1					1	1	P
Power-Up / Down									
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1		160.5	mA	160.5	160.5	160.5	0.0	400.0	P
InrushI_2		162.2	mA	162.2	162.2	162.2	0.0	400.0	P
Pmax_Tdelay		0.2	W	0.2	0.2	0.2	0.0	8.4	P
Inrush_delayed		0		0	0	—	0	0	P
Von		37.3	VDC	37.3	37.3	37.3	30.0	42.0	P
Voff		33.3	VDC	33.3	33.3	33.3	30.0	42.0	P
Vhyst		4.0	VDC	4.0	4.0	4.0	0.0	12.0	P
BackfeedV		0.1	VDC	0.1	0.1	0.1	0.0	2.8	P
ClassRecover		0		0	0	—	0	0	P
SigRecoverTime		0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1		**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1		7.9	mA	7.9	7.9	7.9	0.0	174.0	P
MaxI_1		13.7	mA	13.7	13.7	13.7	10.0	174.0	P
Vport_1		48.0	VDC	48.0	48.0	48.0	37.0	57.0	INFO
Ppeak_1		0.66	W	0.66	0.66	0.66	0.0	8.4	P
Pavg_1		0.48	W	0.48	0.48	0.48	0.0	6.5	P
MPSViolation_1		0		0	0	—	0	0	P
TcutWindowViolation_1		0		0	0	—	0	0	P
DutyCycleViolation_1		0		0	0	—	0	0	P
MDI Powered Type-2 PHY		**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2		2.1	mA	2.1	2.1	2.1	0.0	154.6	P
MaxI_2		50.2	mA	50.2	50.2	50.2	10.0	154.6	P
Vport_2		54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2		2.71	W	2.71	2.71	2.71	0.0	8.4	P
Pavg_2		0.52	W	0.52	0.52	0.52	0.0	6.5	P
MPSViolation_2		0		0	0	—	0	0	P
TcutWindowViolation_2		0		0	0	—	0	0	P
DutyCycleViolation_2		0		0	0	—	0	0	P
ALT B MDI-X									
Detection and Classification		**PSE Emulation**		**Pairs**	**A**	**Polarity**	**MDI**	**Det Cycles**	**3**
Parameter	**Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
Rdet		24.49	kΩ	24.49	24.49	24.49	23.70	26.30	P

Rdet_final	24.53	kΩ	24.53	24.53	24.53	23.70	26.30	P
Rdet_unpwr	>99.00	kΩ	99.00	99.00	99.00	<12.00	>45.00	P
Rdet_at_Vmin	24.98	kΩ	24.98	24.98	24.98	23.70	26.30	P
Rdet_at_Vmax	24.61	kΩ	24.61	24.61	24.61	23.70	26.30	P
Rdet_Voffset	1.4	VDC	1.4	1.4	1.4	0.0	1.9	P
Cdet	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
Cdet_final	0.10	µF	0.10	0.10	0.10	0.05	0.12	P
1 Event Classification								
Iclass	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
ClassNum	2		2	2	—	0	4	P
Tclass	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability	1					1	1	P
Iclass_at_Vmin	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
Iclass_at_Vmax	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
2 Event Classification								
Iclass_event1	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
Iclass_event2	18.2	mA	18.2	18.2	18.2	17.0	20.0	P
MarkI	1.55	mA	1.55	1.55	1.55	0.25	4.00	INFO
ClassNum2	2		2	2	—	0	4	P
Tclass_event1	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
Tclass_event2	0.0005	s	0.0005	0.0005	0.0005	0.0005	0.0050	P
ClassStability_event1	1					1	1	P
ClassStability_event2	1					1	1	P
Power-Up / Down								
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
InrushI_1	160.2	mA	160.2	160.2	160.2	0.0	400.0	P
InrushI_2	161.7	mA	161.7	161.7	161.7	0.0	400.0	P
Pmax_Tdelay	0.1	W	0.1	0.1	0.1	0.0	8.4	P
Inrush_delayed	0		0	0	—	0	0	P
Von	37.4	VDC	37.4	37.4	37.4	30.0	42.0	P
Voff	33.4	VDC	33.4	33.4	33.4	30.0	42.0	P
Vhyst	4.1	VDC	4.1	4.1	4.1	0.0	12.0	P
BackfeedV	0.0	VDC	0.0	0.0	0.0	0.0	2.8	P
ClassRecover	0		0	0	—	0	0	P
SigRecoverTime	0.0	s	0.0	0.0	0.0	0.0	30.0	P
MDI Powered Type-1	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**48.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_1	7.9	mA	7.9	7.9	7.9	0.0	173.8	P

MaxI_1	13.4	mA	13.4	13.4	13.4	10.0	173.8	P
Vport_1	48.1	VDC	48.1	48.1	48.1	37.0	57.0	INFO
Ppeak_1	0.64	W	0.64	0.64	0.64	0.0	8.4	P
Pavg_1	0.48	W	0.48	0.48	0.48	0.0	6.5	P
MPSViolation_1	0		0	0	—	0	0	P
TcutWindowViolation_1	0		0	0	—	0	0	P
DutyCycleViolation_1	0		0	0	—	0	0	P
MDI Powered Type-2 PHY	**PSE Emulation**		**On Time**	**10 s**	**Off Time**	**10 s**	**Vport**	**54.0**
Parameter **Cycle**	**1**	**Units**	**Min**	**Max**	**Average**	**Low Limit**	**High Limit**	**P/F**
MinI_2	2.1	mA	2.1	2.1	2.1	0.0	154.6	P
MaxI_2	50.2	mA	50.2	50.2	50.2	10.0	154.6	P
Vport_2	54.1	VDC	54.1	54.1	54.1	42.5	57.0	INFO
Ppeak_2	2.71	W	2.71	2.71	2.71	0.0	8.4	P
Pavg_2	0.52	W	0.52	0.52	0.52	0.0	6.5	P
MPSViolation_2	0		0	0	—	0	0	P
TcutWindowViolation_2	0		0	0	—	0	0	P
DutyCycleViolation_2	0		0	0	—	0	0	P

7.5 Adjustable EVB Current Limit

For additional safety, the Si3406 has an adjustable EVB current limit feature.

The Si3406 controller measures the voltage on the R_{SENSE} resistor (R7) through the ISNS pin. Care must be taken that this voltage goes below V_{SS}. When the voltage on R7 is V_{ISNS} = –270 mV (referenced to V_{SS}), the internal current limit circuit restarts the PD to protect the application.

The EVB current limit for this Class 2 application can be calculated with the following formula:

$$R_{SENSE} = 1.2\Omega$$

$$I_{LIMIT} = \frac{270mV}{1.2\Omega} = \quad 225mA$$

Equation 7.1. EVB Class 2 Current Limit

7.6 Feedback Loop Phase and Gain Measurement Results (Bode Plots)

The Si3406 device integrates a current-mode-controlled switching mode power supply controller circuit. Therefore, the application is a closed-loop system. To guarantee a stable output voltage of the power supply and to reduce the influence of the input voltage variations and load changes on the output voltage, the feedback loop should be stable.

To verify the stability of the loop, the gain and phase of the loop has been measured.

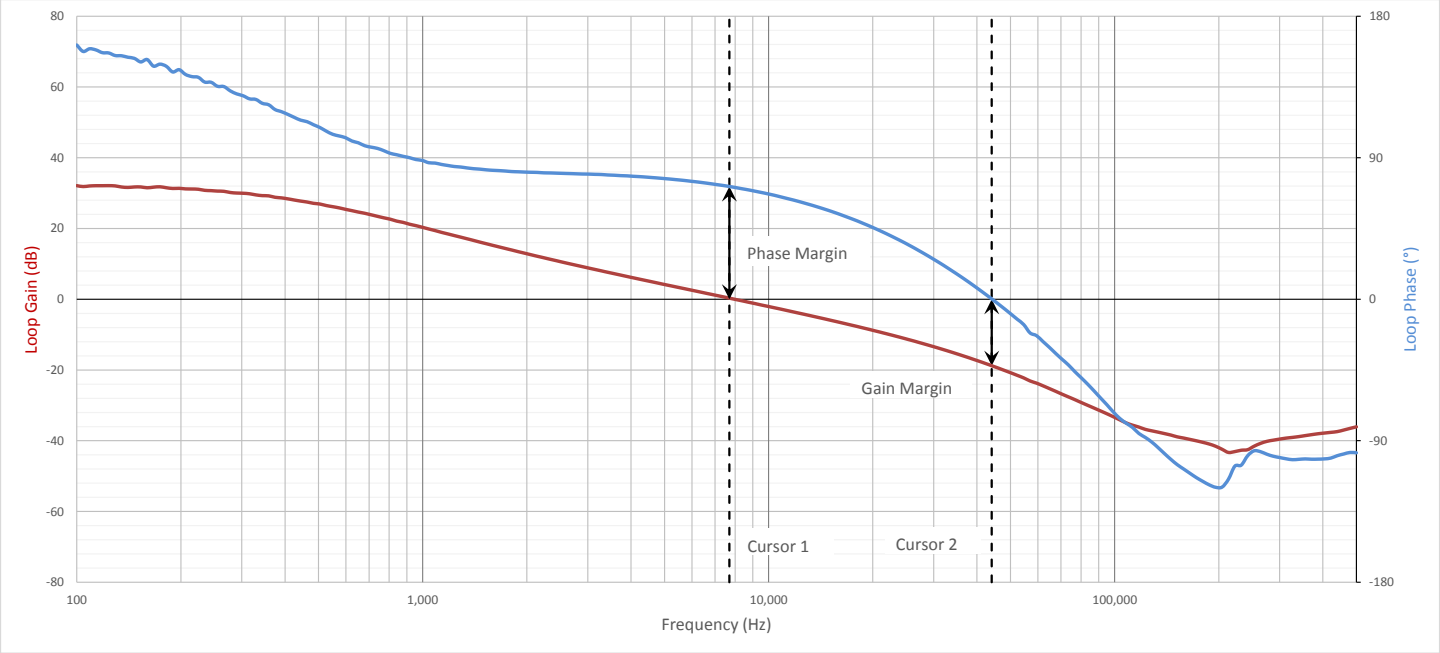


Figure 7.4. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 PD Feedback Loop Measurement Results at Full Load

Table 7.3. Measured Loop Gain and Phase Margin

	Frequency	Gain	Phase
Cursor 1 (Phase Margin)	7.70 kHz	0 dB	71.72 °
Cursor 2 (Gain Margin)	44.13 kHz	–18.79 dB	0 °

7.7 Load Step Transient Measurement Results

The Si3406-Buck EVB board's output has been tested with a load step function to verify the converter's output dynamic response.

Load Step: from 0.05 A to 0.22 A Output Current:
ΔV_{OUT} = 307.54 mV

Load Step, from 0.22 A to 0.05 A Output Current:
ΔV_{OUT} = 249.75 mV

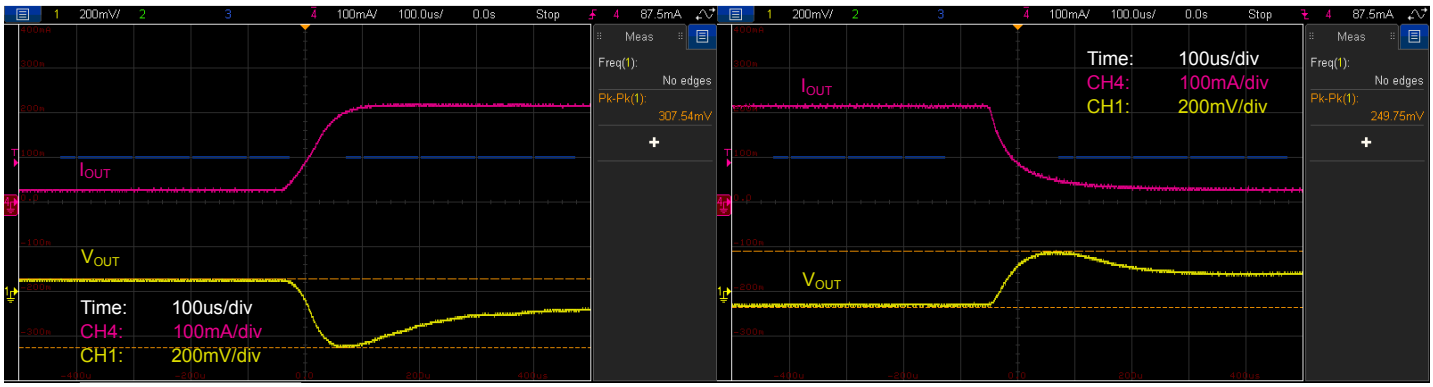


Figure 7.5. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 PD Output Load Step Transient Test

7.8 Output Voltage Ripple

The Si3406-Buck EVB output voltage ripple has been measured in both no-load and heavy-load conditions.

No-Load V_{OUT} Ripple = 96.23 mV **Heavy-Load V_{OUT} Ripple = 6.2 mV**

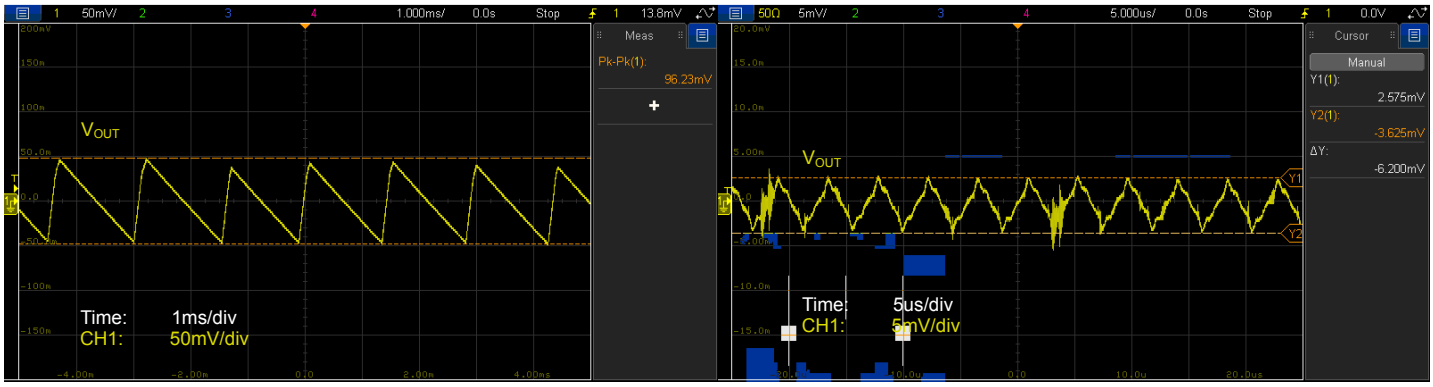


Figure 7.6. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 Output Voltage Ripple No Load (Left) and Heavy Load (Right) Conditions

7.9 Soft-Start Protection

The Si3406 device has an integrated dynamic soft-start protection mechanism to avoid stressing the components by the sudden current or voltage changes associated with the initial charging of the output capacitors.

The Si3406 intelligent adaptive soft-start mechanism does not require any external component to install. The controller continuously measures the input current of the PD and dynamically adjusts the internal I_{PEAK} limit during soft-start, that way adjusting the output voltage ramping up time in a function of the attached load.

The controller lets the output voltage to rise faster in no load (or light load) condition. With heavy load at the output, the controller slows down the output voltage ramp to avoid exceeding the desired regulated output voltage value.

No-Load Soft-Start:
t_{RISE} = 7.14 ms

Heavy-Load Soft-Start:
t_{RISE} = 23.18 ms

Figure 7.7. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 Output Voltage Soft-Start at Low Load (Left) and Heavy Load (Right) Conditions

7.10 Output Short Protection

The Si3406 device has an integrated output short protection mechanism, which protects the IC itself and the surrounding external components from overheating in the case of electrical short on the output.

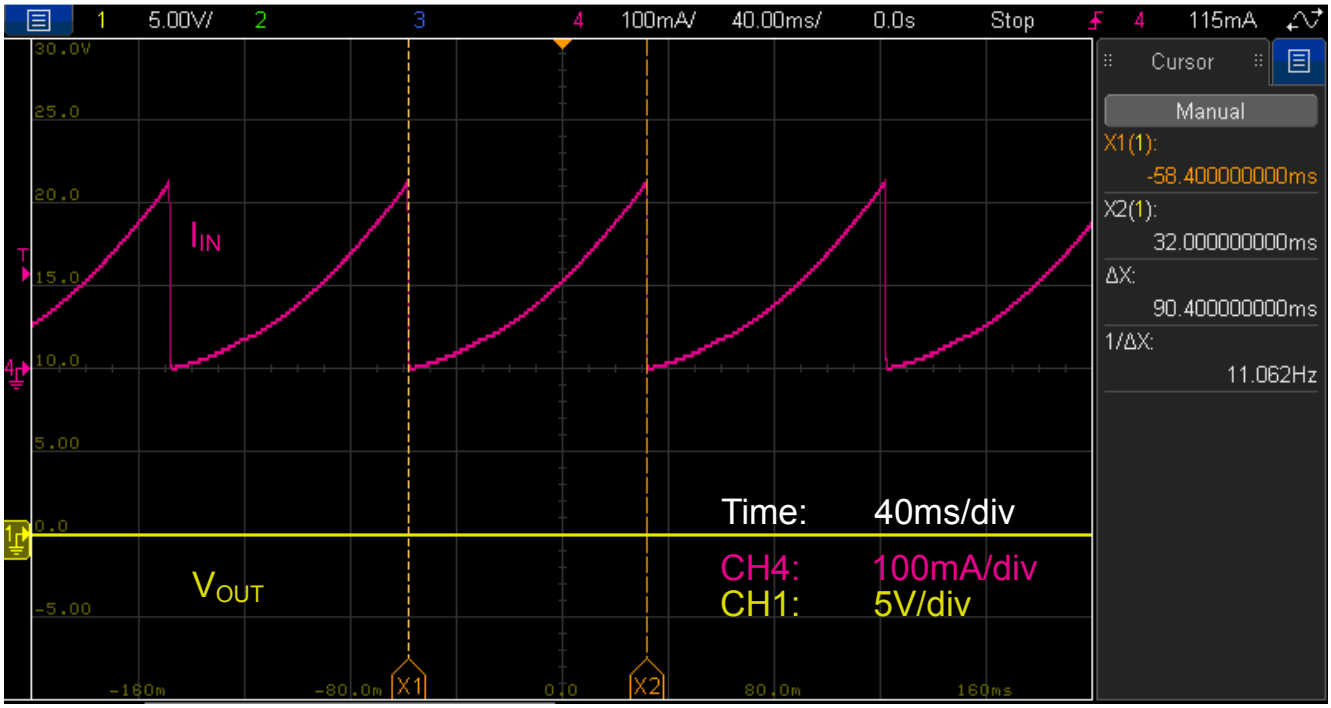


Figure 7.8. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 Output Short Circuit Protection

7.11 Pulse Skipping at No-Load Condition

The Si3406 device has an integrated pulse skipping mechanism to ensure ultra-low power consumption at light load condition.

As the output load decreases, the controller starts to reduce the pulse-width of the PWM signal (switcher ON time). At some point, even the minimum width pulse would provide higher energy than the application requires, which could result in loss of voltage regulation.

When the controller detects light load condition (which requires less ON time than the minimum pulse width), the controller enters into burst or light-load skipping mode. This mode is shown in the following figure by depicting the switching node of the integrated switching FET at no load condition.

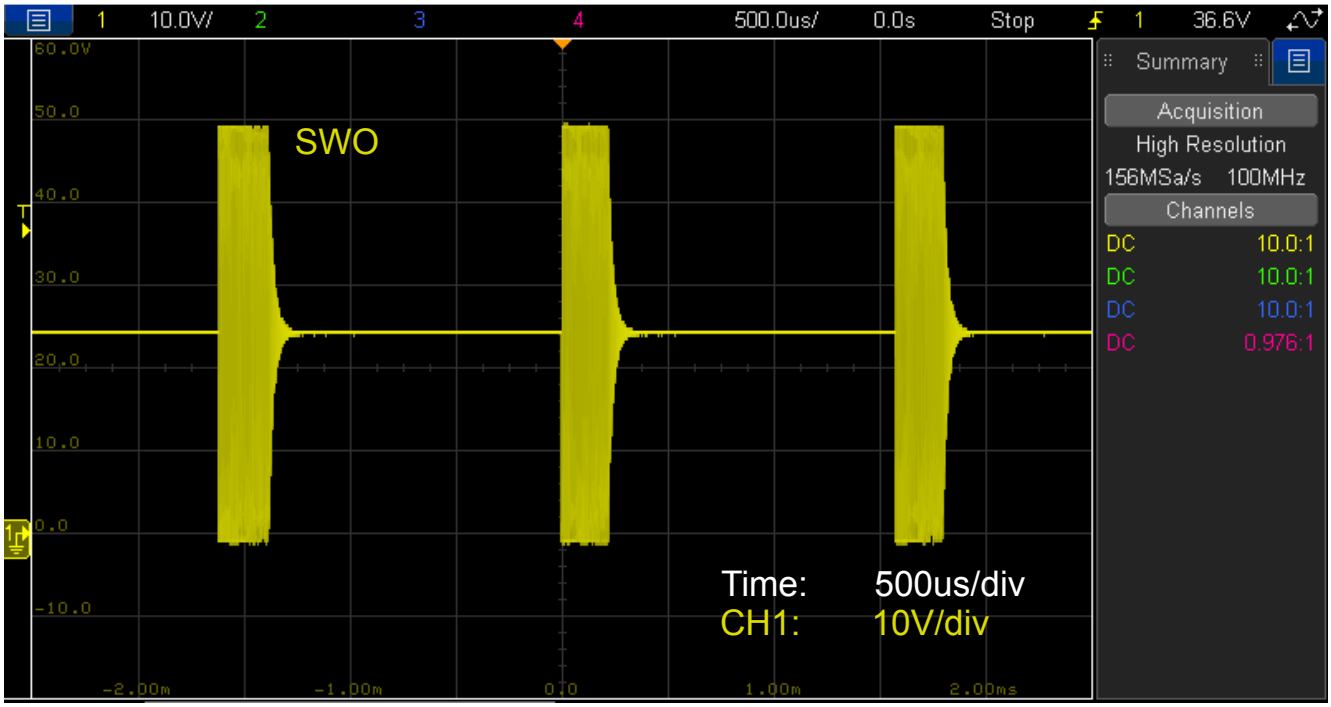


Figure 7.9. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 Pulse Skipping at No-Load Condition: SWO Waveform

7.12 Discontinuous (DCM) and Continuous (CCM) Current Modes

At low load, the converter works in discontinuous current mode (DCM). At heavy load, the converter runs in continuous current mode (CCM). At low load, the SWO voltage waveform has a ringing waveform, which is typical for DCM operation.

Low-Load, DCM **Heavy-Load, CCM**

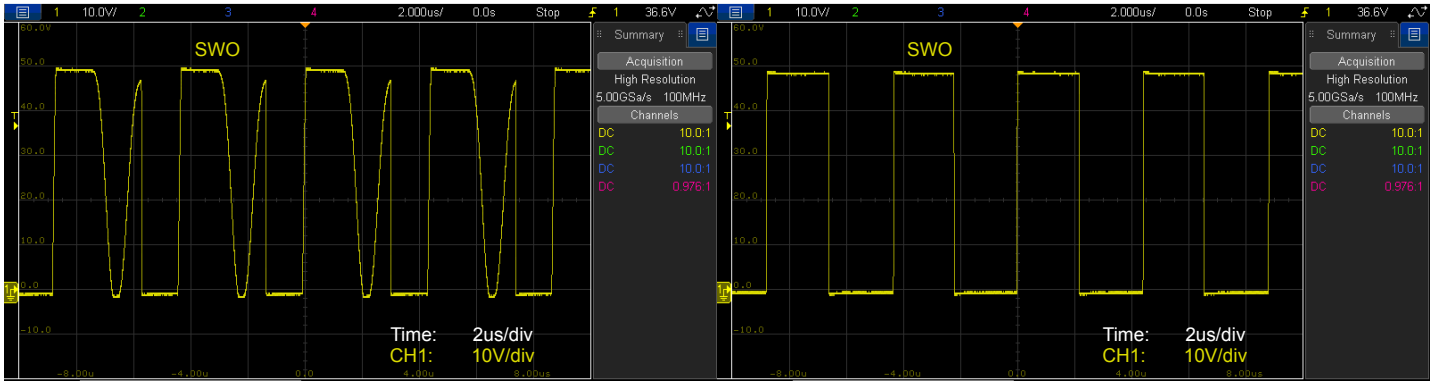


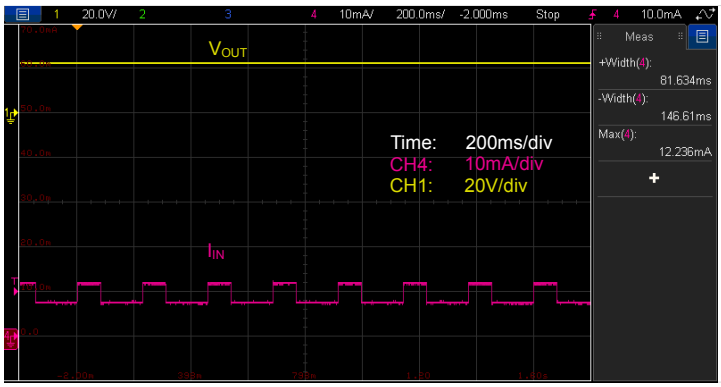
Figure 7.10. Si3406-Buck Non-Isolated EVB, 24 V, Class 2: SWO Waveform in Discontinuous Current Mode (DCM) at Low Load (Left), and in Continuous Current Mode (CCM) at Heavy Load (Right)

7.13 Maintain Power Signature (MPS)

The Si3406-Buck EVB board has a built-in MPS feature that enables the Si3406 to maintain the connection with the PSE when the PD is in a low-current consumption mode. MPS can be used in user mode or in automatic mode. In user mode, nSLEEP shall be tied to VDD at startup (R13), and the host controller needs to manually start/stop MPS generation by pulling the nSLEEP line low or high respectively. To enable the automatic MPS feature, nSLEEP shall be tied to VSS at startup (R12). In automatic mode, the Si3406 monitors the input current and turns off MPS automatically when it is below a predefined level.

Note: Si3406 assumes a minimum consumption of the host controller therefore to pass Sifos MPS tests, a dummy load is recommended to be installed on the EVB (R14) to keep the consumption above the pre-defined current threshold. The figure below shows the automatic MPS pulses generated by the EVB when a 3 kΩ dummy load is installed.

Automatic MPS Pulse Generation by Si3406
V_{ON} = 81.63 ms, V_{OFF} = 146.61 ms, I_{MAX} = 12.24 mA



Automatic MPS Pulse Generation by Si3406
Sifos Startup Trace

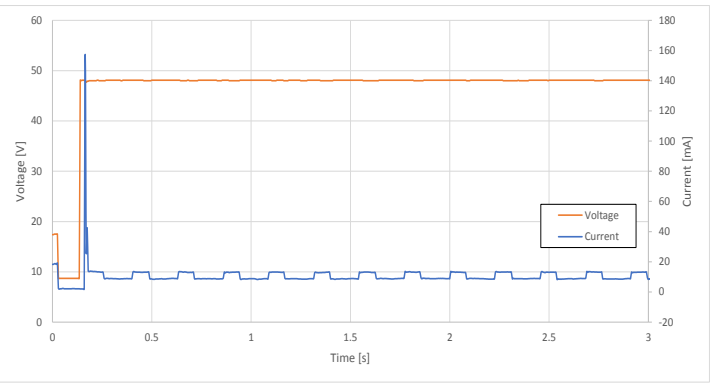


Figure 7.11. Si3406-Buck Non-Isolated EVB, 24 V, Class 2 PD Automatic Maintain Power Signature (MPS) Generation

7.14 Radiated Emissions Measurement Results

Radiated emissions have been measured of the Si3406-Buck 24 V, Class 2 EVB board with 50 V input voltage and full load connected to the output – 6.5 W.

As shown below, the Si3406-Buck, 24 V, Class 2 EVB is fully compliant with the international EN 55032 class B emissions standard.

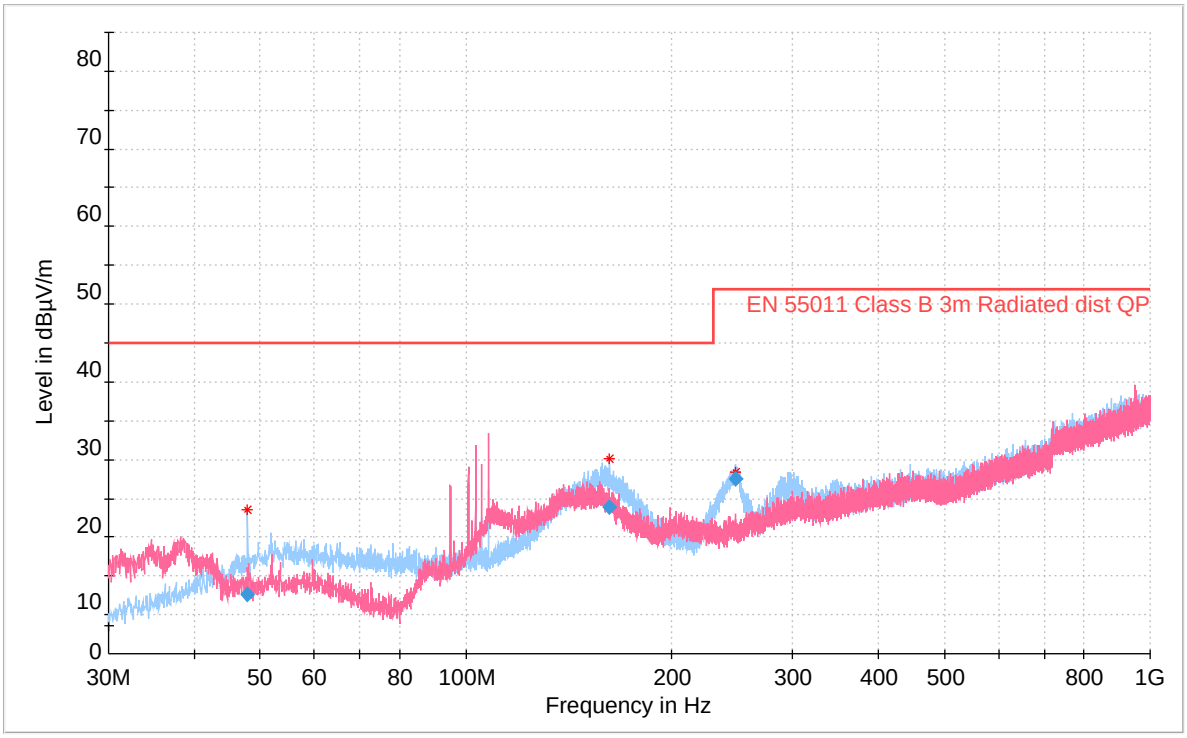


Figure 7.12. Si3406-Buck Non-Isolated EVB Radiated Emissions Measurements Results; 50 V Input, 24 V Output, 6.5 W Input Load

The EVB is measured at full load with peak detection in both vertical and horizontal polarizations. This is a relatively fast process that produces a red curve (vertical polarization) and a blue curve (horizontal polarization). Next, specific frequencies are selected (red stars) for quasi-peak measurements. The board is measured again at those specific frequencies with a quasi-peak detector, which is a very slow but accurate measurement. The results of this quasi-peak detector measurement are the blue rhombuses.

The blue rhombuses represent the final result of the measurement process. To have passing results, the blue rhombuses should be below the highlighted EN 55032 Class B limit.

7.15 Conducted Emissions Measurement Results

The Si3406-Buck, 24 V, Class 2 EVB board's conducted emissions have been measured in two different measurement methods to comply with the international EN 55032 standard. The EVB is supplied and measured on its PoE input port as shown in the following figure.

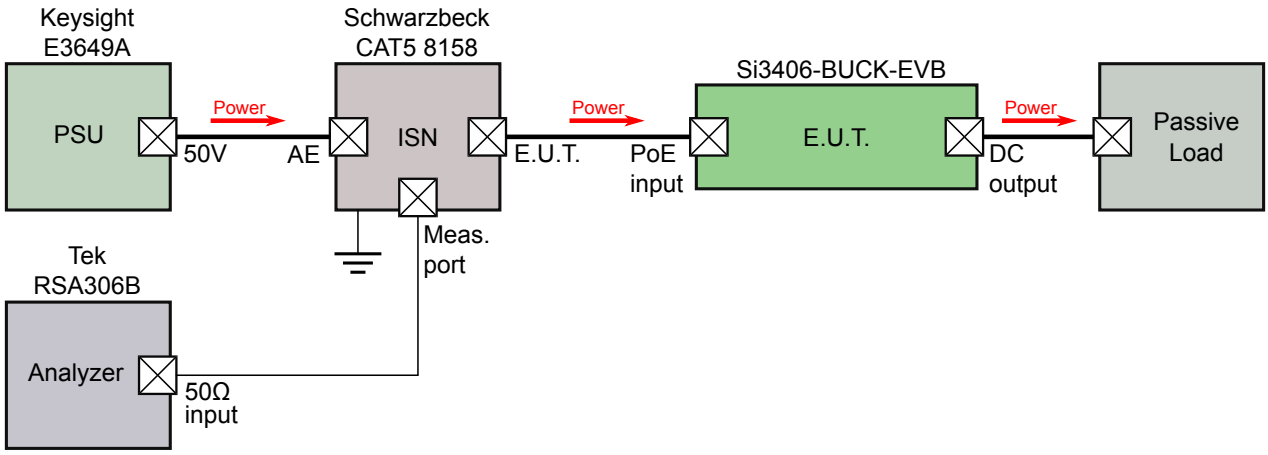


Figure 7.13. Conducted EMI Measurement Setup

The detector in the spectrum analyzer is set to:

- Peak detector and
- Average detector

Both results are shown below.

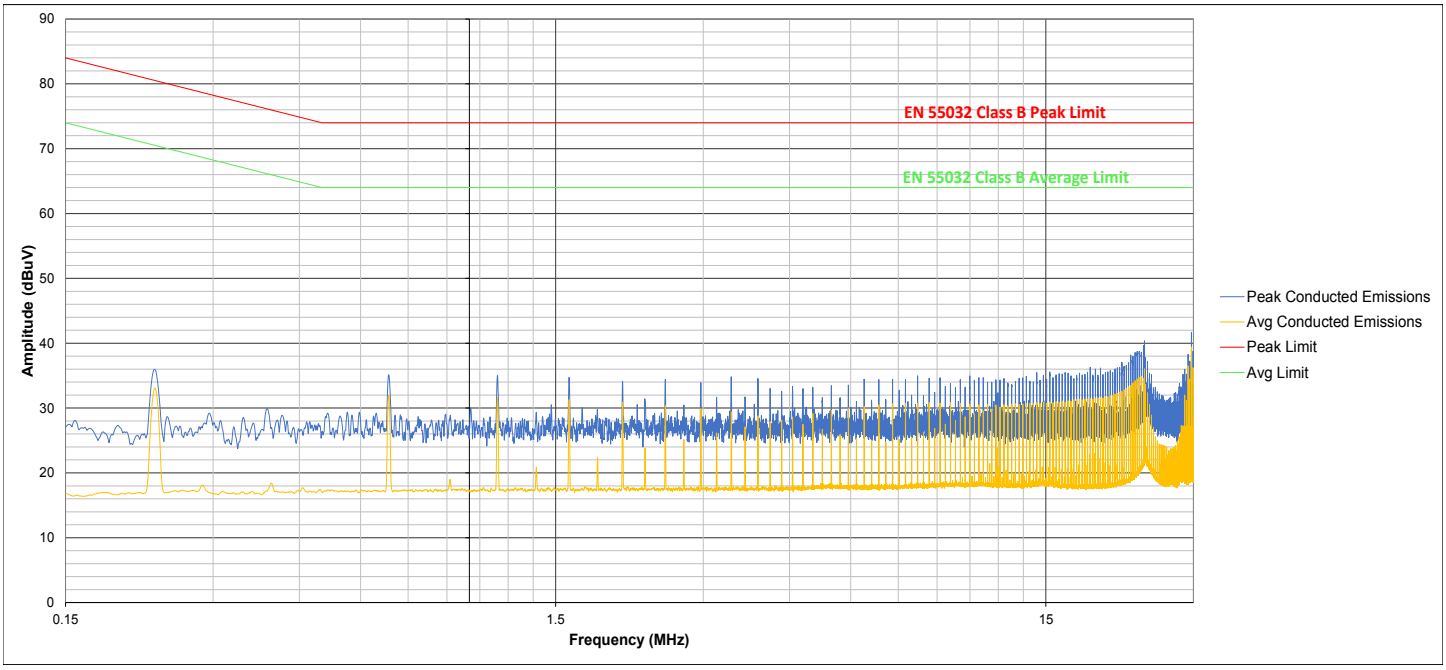


Figure 7.14. Si3406-Buck Non-Isolated EVB Conducted Emissions Measurements Results; 50 V Input, 24 V Output, 6.5 W Input Load

7.16 Bill of Materials

The following table is the BOM listing for the standard 24 V output evaluation board with option PoE Class 2.

Table 7.4. Si3406-BUCK-24 V Bill of Materials

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	C1	1 µF		100 V	±10%	X7R	C1210	C1210X7R101-105K	Venkel
1	C13	0.1 µF		100 V	±10%	X7R	C0805	C0805X7R101-104K	Venkel
1	C14	1 nF		50 V	±1%	C0G	C0805	C0805C0G500-102F	Venkel
2	C19, C21	0.1 µF		16 V	±10%	X7R	C0805	C0805X7R160-104K	Venkel
1	C2	12 µF		100 V	±20%	Alum_Elec	C2.5X6.3MM-RAD	EEUFC2A120	Panasonic
3	C4, C5, C8	22 µF		25 V	±10%	X7R	C1210	C1210X7R250-226M	Venkel
1	C7	1 µF		50 V	±10%	X7R	C0805	CL21B105KBFNNNE	Samsung
1	D1	PDS3100	3 A	100 V		Schottky	POWERDI-5	PDS3100-13	Diodes Inc.
1	J1	RJ-45				Receptacle	RJ45-SI-52004	SI-52003-F	Bel
1	L2	470 µH	0.43 A		±10%	Shielded	IND-MSS1038	MSS1048-474KL	Coilcraft
4	L5, L6, L7, L8	330 Ω	1500 mA			SMT	L0805	BLM21PG331SN1	Murata
1	R1	7.5 kΩ	1/10 W		±1%	Thick Film	R0805	CR0805-10W-7501F	Venkel
1	R10	88.7 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080588K7FKEA	Vishay
1	R11	75 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-75R0F	Venkel
1	R13	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R3	1.37 kΩ	1/10 W		±0.1%	±25 PPM	R0805	TFCR0805-10W-E-1371B	Venkel
1	R4	23.7 kΩ	1/10 W		±0.1%	±25 PPM	R0805	TFCR0805-10W-E-2372B	Venkel
1	R5	10 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-10R0F	Venkel
1	R6	3 Ω	1/8 W		±1%	Thick Film	R0805	CR0805-8W-3R00FT	Venkel
1	R7	1.2 Ω	1/10 W		±5%	Thick Film	R0805	CR0805-10W-1R2J	Venkel
1	R8	100 kΩ	1/8 W		±1%	Thick Film	R0805	CR0805-8W-1003F	Venkel
1	R9	24.3 kΩ	1/8 W		±1%	Thick Film	R0805	CRCW080524K3FKEA	Vishay
4	TP1, TP2, TP11, TP12	Black				Loop	Testpoint	5001	Keystone
1	U1	Si3406		120 V		PD	QFN20N5X5P0.8	Si3406-A-GM	Silicon Labs
Not Installed Components									
1	C20	330 pF		50 V	±1%	C0G	C0805	C0805C0G500-331F	Venkel
1	C22	200 pF		50 V	±1%	C0G	C0805	C0805C0G500-201FNE	Venkel
1	C3	560 µF		6.3 V	±20%	Alum_Elec	C3.5X8MM-RAD	EEUFM0J561	Panasonic
1	C6	39 pF		25 V	±1%	C0G	C0805	C0805C0G250-390FNP	Venkel

Qty	Ref	Value	Rating	Voltage	Tol	Type	PCB Footprint	Mfr Part Number	Mfr
1	R12	0 Ω	2 A			Thick Film	R0805	CR0805-10W-000	Venkel
1	R14	120 Ω	1/10 W		±1%	Thick Film	R0805	CR0805-10W-1200F	Venkel
8	TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	Black				Loop	Testpoint	5001	Keystone

8. Tunable Switching Frequency

The switching frequency of the oscillator is selected by choosing an external resistor (R_{FREQ}) connected between R_{FREQ} and VPOS pins. The following figure will aid in choosing the R_{FREQ} value to achieve the desired switching frequency.

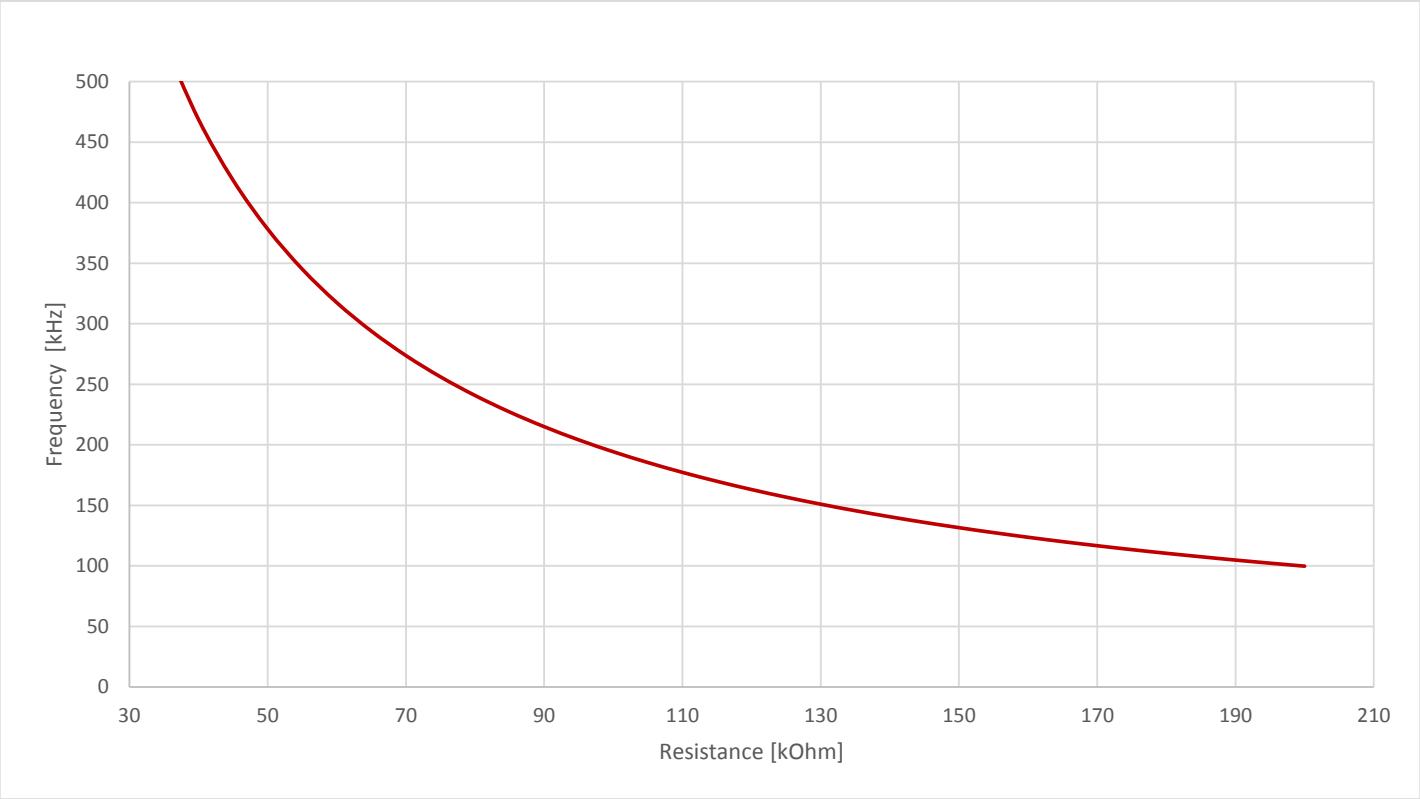


Figure 8.1. Switching Frequency vs R_{FREQ}

The selected switching frequency for these applications is 220 kHz, which is achieved by setting the R_{FREQ} resistor to 88.7 kΩ.

9. Board Layout

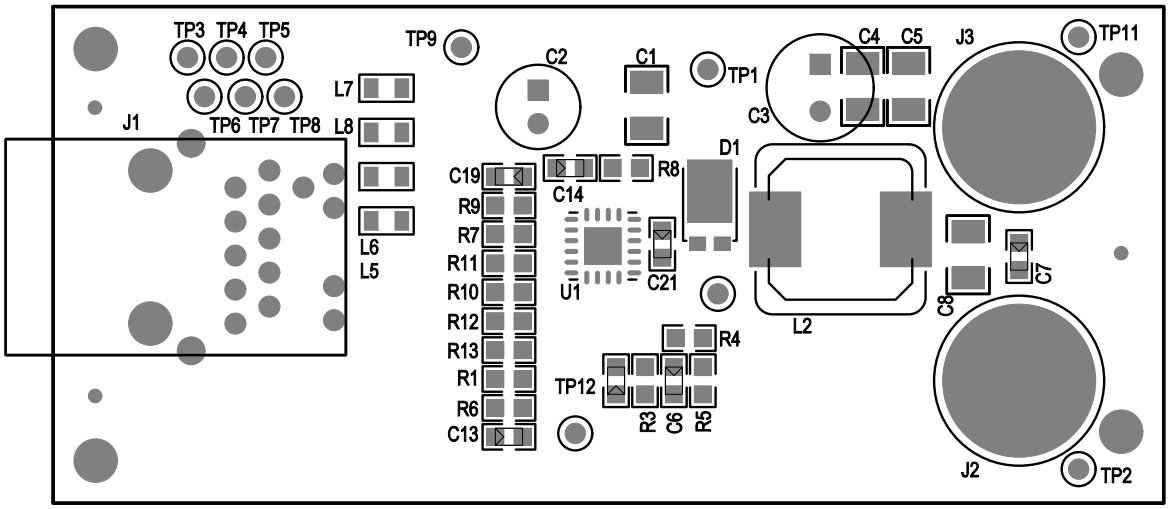


Figure 9.1. Top Silkscreen

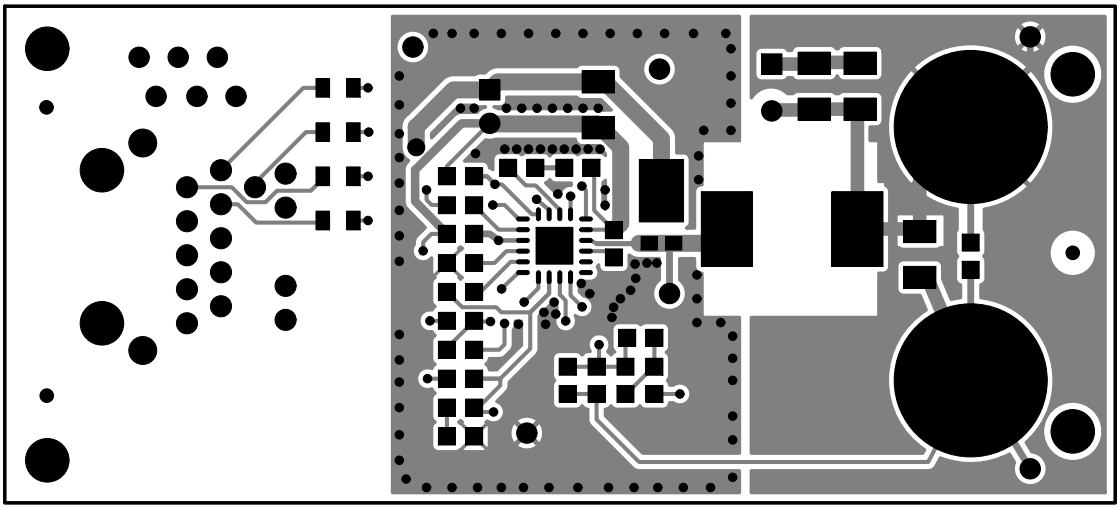


Figure 9.2. Top Layer

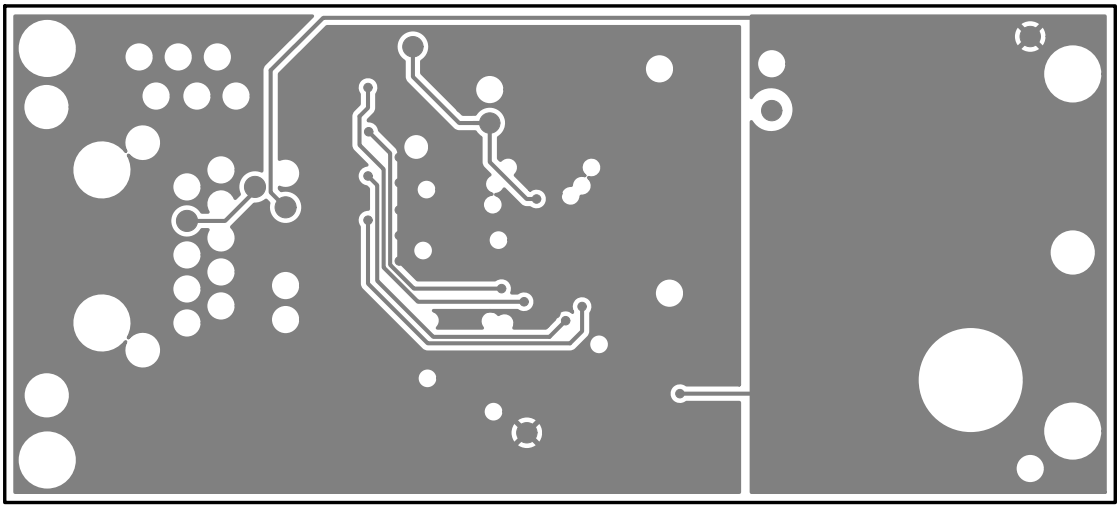


Figure 9.3. Internal 1 (Layer 2)

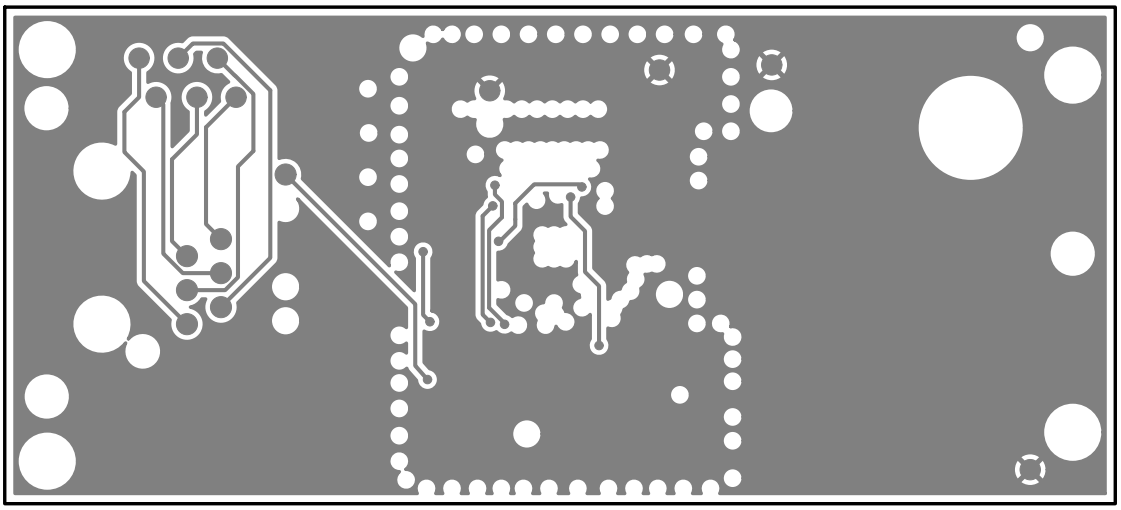


Figure 9.4. Internal 2 (Layer 3)

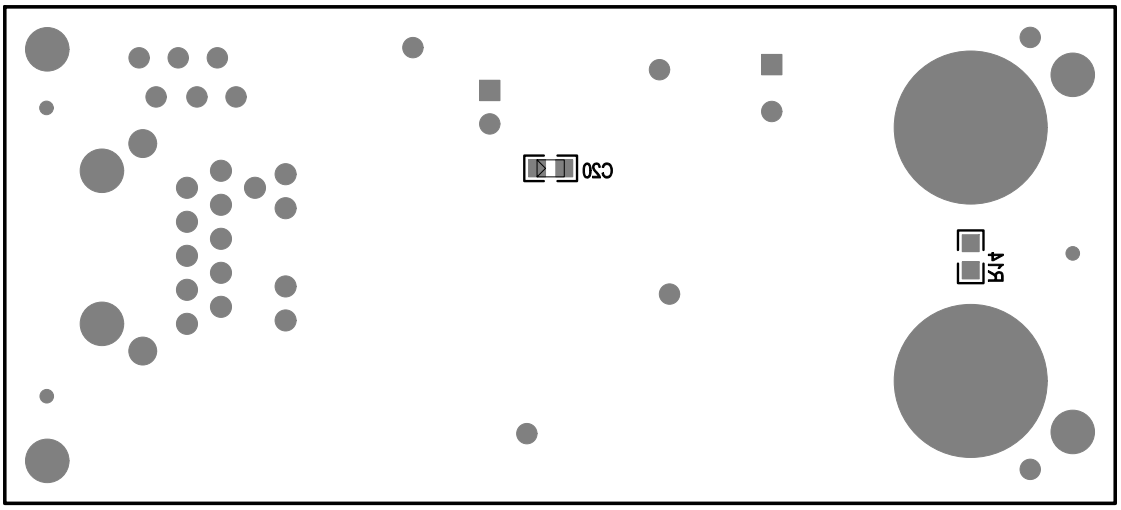


Figure 9.5. Bottom Layer

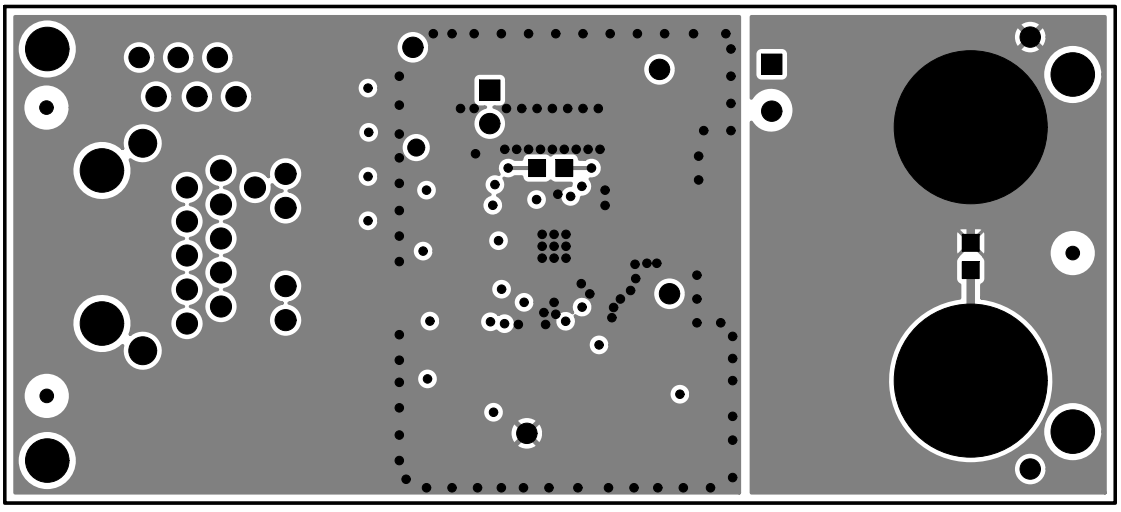


Figure 9.6. Bottom Layer

10. Design and Layout Checklist

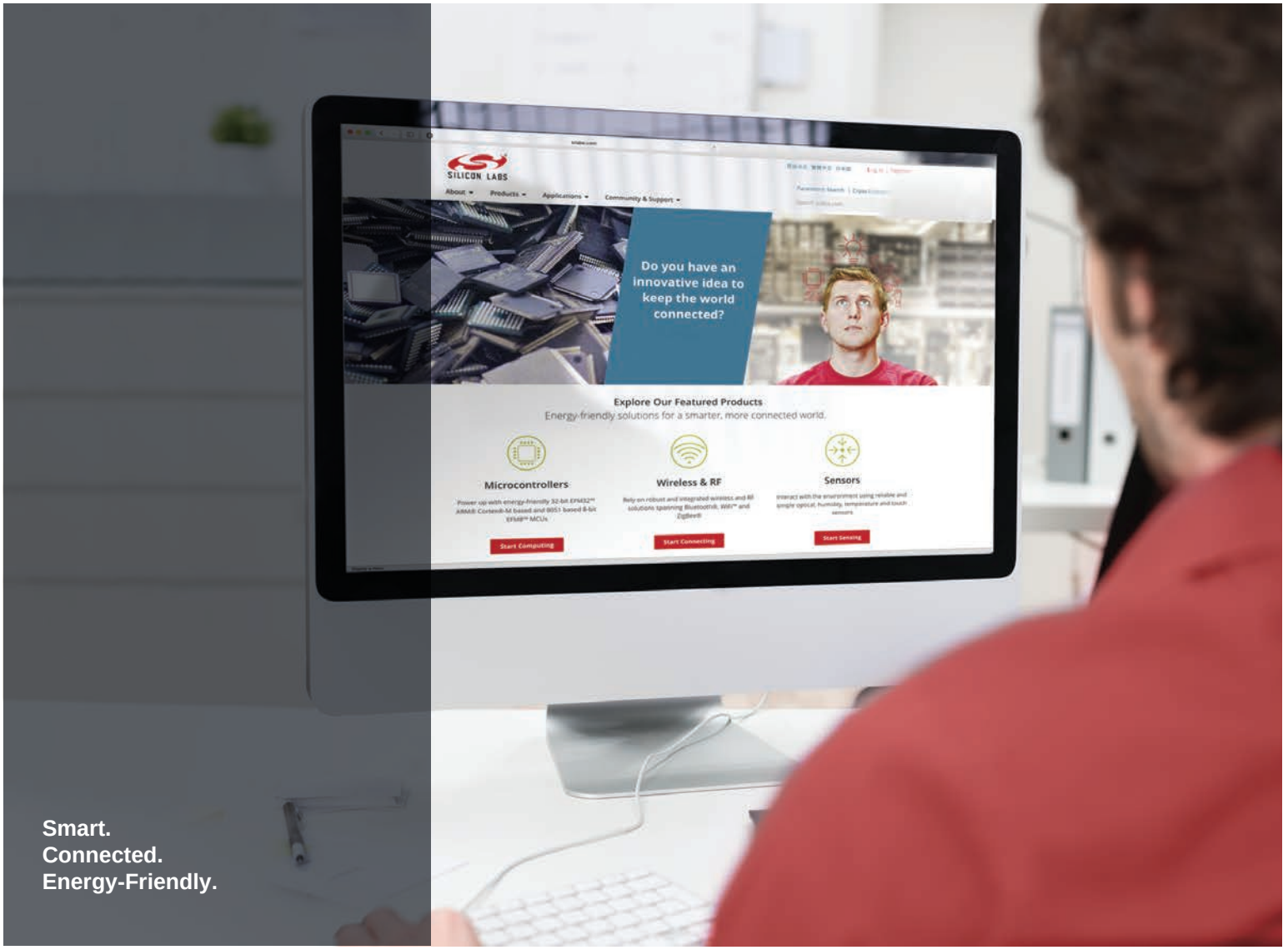
The complete EVB design databases for the 4 configurations are located at www.silabs.com/PoE link. Silicon Labs strongly recommends using these EVB schematics and layout files as a starting point to ensure robust performance and avoid common mistakes in the schematic capture and PCB layout processes.

Below is a recommended design checklist that can assist in trouble-free development of robust PD designs.

Refer also to the Si3406 data sheet and AN1130 when using the following checklist.

1. Design Planning Checklist:
   a. Determine if your design requires an isolated or non-isolated topology. For more information, see AN1130.
   b. Silicon Labs strongly recommends using the EVB schematics and layout files as a starting point as you begin integrating the Si3406-BUCK into your system design process.
   c. Determine your load's power requirements (i.e., VOUT and IOUT consumed by the PD, including the typical expected transient surge conditions). In general, to achieve the highest overall efficiency performance of the Si3406-BUCK, choose the highest output voltage option used in your PD and then post regulate to the lower supply rails, if necessary.
   d. Based on your required PD power level, select the appropriate class resistor RCLASS value by referring to AN1130.
2. General Design Checklist:
   a. ESD caps (in parallel with the diode bridges) are recommended for designs where system-level ESD (IEC6100-4-2) must provide >15 kV tolerance.
   b. If your design uses an AUX supply, be sure to include a 3 Ω surge limiting resistor in series with the AUX supply for hot insertion.
   c. Non-standard PoE injectors turns on the PD without detection and classification phases. In most cases, dV/dt is not controlled and could violate IEEE requirements. To ensure robustness with those injectors, please include a 3 Ω resistors in series with C13.
   d. If MPS is not used, Silicon Labs recommends the inclusion of a minimum load (250 mW) to avoid the PSE port being disconnected by the PSE. If your load is not at least 250 mW, add a resistor load to dissipate at least 250 mW.
3. Layout Guidelines:
   a. Make sure VNEG pin of the Si3406 is connected to the backside of the QFN package with an adequate thermal plane.
   b. Keep the trace length from SWO to VSS as short as possible. Make all of the power (high current) traces as short, direct, and thick as possible. It is a good practice on a standard PCB board to make the traces an absolute minimum of 15 mils (0.381 mm) per ampere.
   c. Usually, one standard via handles 200 mA of current. If the trace needs to conduct a significant amount of current from one plane to the other, use multiple vias.
   d. Keep the circular area of the loop from the Switcher FET output to the inductor and returning from the input filter capacitors (C1–C2) to VSS as small a diameter as possible. Also, minimize the circular area of the loop from the output of the inductor to the Schottky diode and returning through the output filter capacitor back to the inductor as small as possible. If possible, keep the direction of current flow in these two loops the same.
   e. Keep the high-power traces as short as possible.
   f. Keep the feedback and loop stability components as far from the inductor and noisy power traces as possible.
   g. If the outputs have a ground plane or positive output plane, do not connect the high current carrying components and the filter capacitors through the plane. Connect them together, and then connect to the plane at a single point.

To help ensure first-pass success, contact our customer support by submitting a help ticket and uploading your schematics and layout files for review.



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